

# LP8866S-Q1 6 つの 150mA チャンネルを備えた車載ディスプレイ用 LED バックライト・ドライバ

## 1 特長

- 車載アプリケーション用に AEC-Q100 認定取得済み
  - デバイス温度グレード 1 :  $-40^{\circ}\text{C} \sim +125^{\circ}\text{C}$ ,  $T_A$
  - デバイス HBM ESD 分類レベル 2
  - デバイス CDM ESD 分類レベル C4B
- 入力電圧動作範囲: 3V ~ 48V
- 6 つの高精度電流シンク
  - 電流シンクごとに最大 150mA の DC 電流
  - 電流マッチング 1% (標準値)
  - 152Hz の LED 出力 PWM 周波数を使用して、32,000 : 1 の調光率
  - I2C または PWM 入力により、最大 16 ビットの LED 調光分解能
  - 8 つの構成可能な LED ストリング構成
- 自動位相シフトの PWM 調光
- 12 ビットのアナログ調光
- 最高 48V の  $V_{OUT}$  昇圧または SEPIC DC/DC コントローラ
  - スイッチング周波数: 100kHz ~ 2.2MHz
  - 昇圧拡散スペクトラムによる EMI の低減
  - 昇圧同期入力により、外部クロックから昇圧スイッチング周波数を設定
  - 昇圧のデイスエーブル時に出力電圧を自動的に放電
- 広範なフォルト診断

## 2 アプリケーション

- 次の応用でのバックライト
  - 車載インフォテインメント
  - 車載用計器盤
  - スマート・ミラー
  - ヘッドアップ・ディスプレイ (HUD)

## 3 概要

LP8866S-Q1 は昇圧コントローラを備えた車載用、高効率の LED ドライバです。6 つの高精度電流シンクは、使用しているチャンネル数に応じて自動調整される位相シフトをサポートしています。LED の輝度は、I<sup>2</sup>C インターフェイスまたは PWM 入力によりグローバルに制御できます。

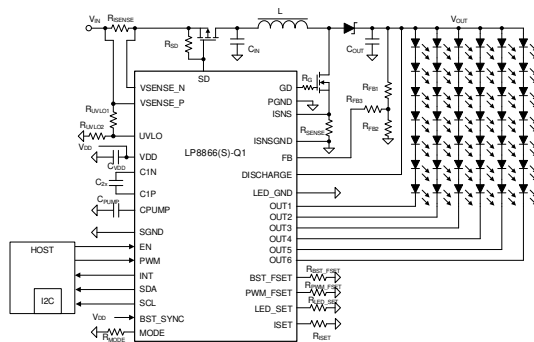
この昇圧コントローラは、LED 電流シンクのヘッドルーム電圧に基づいた適応型出力電圧制御機能を備えています。この機能により、すべての条件で、必要最低限のレベルに電圧を調整することで消費電力を最小化できます。周波数を広範囲に調整できるため、LP8866S-Q1 は AM ラジオ周波数帯に対する妨害を回避できます。

LP8866S-Q1 は組み込みのハイブリッド PWM 調光とアナログ電流調光をサポートしているため、EMI の削減、LED の寿命の延長、総合的な光学効率の向上を実現できます。

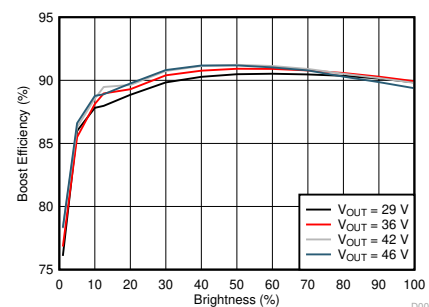
### 製品情報

| 部品番号 <sup>(1)</sup> | パッケージ                   | 本体サイズ (公称)      |
|---------------------|-------------------------|-----------------|
| LP8866S-Q1          | HTSSOP (38)             | 9.70mm × 4.40mm |
|                     | QFN (32) <sup>(2)</sup> | 5mm × 5mm       |

- 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。
- 製品プレビュー。



概略回路図



システム効率



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## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision * (August 2020) to Revision A (February 2021) | Page     |
|---|----------|
| • 「製品情報」表に QFN パッケージ・オプションを追加.....                                  | <b>1</b> |
| • Added QFN package pinout drawing and Pin Functions table.....     | <b>3</b> |

## 5 Pin Configuration and Functions

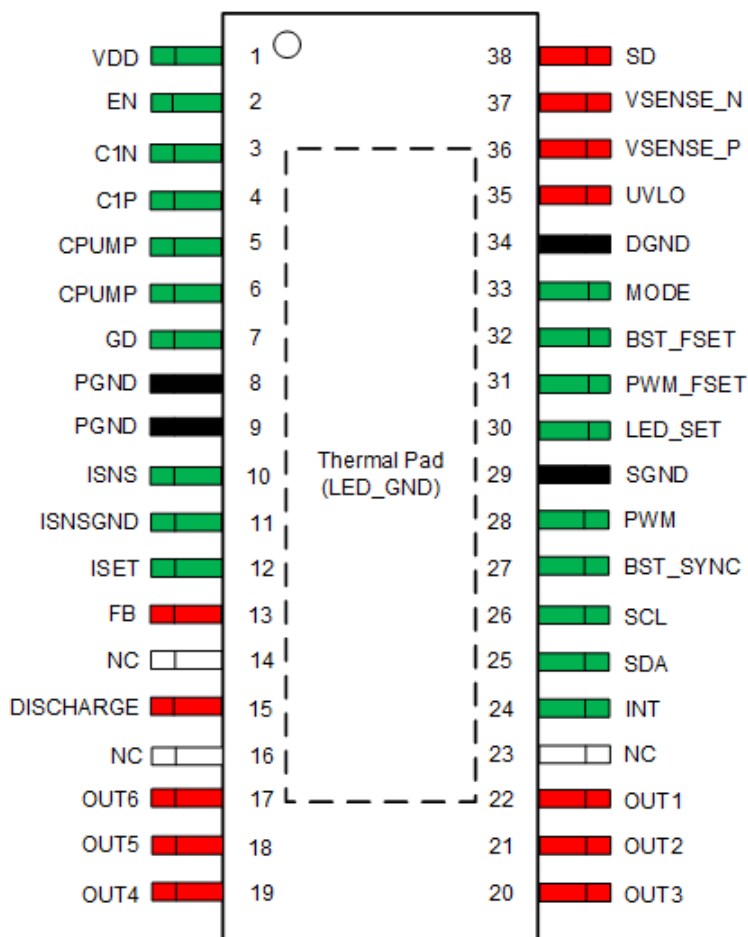
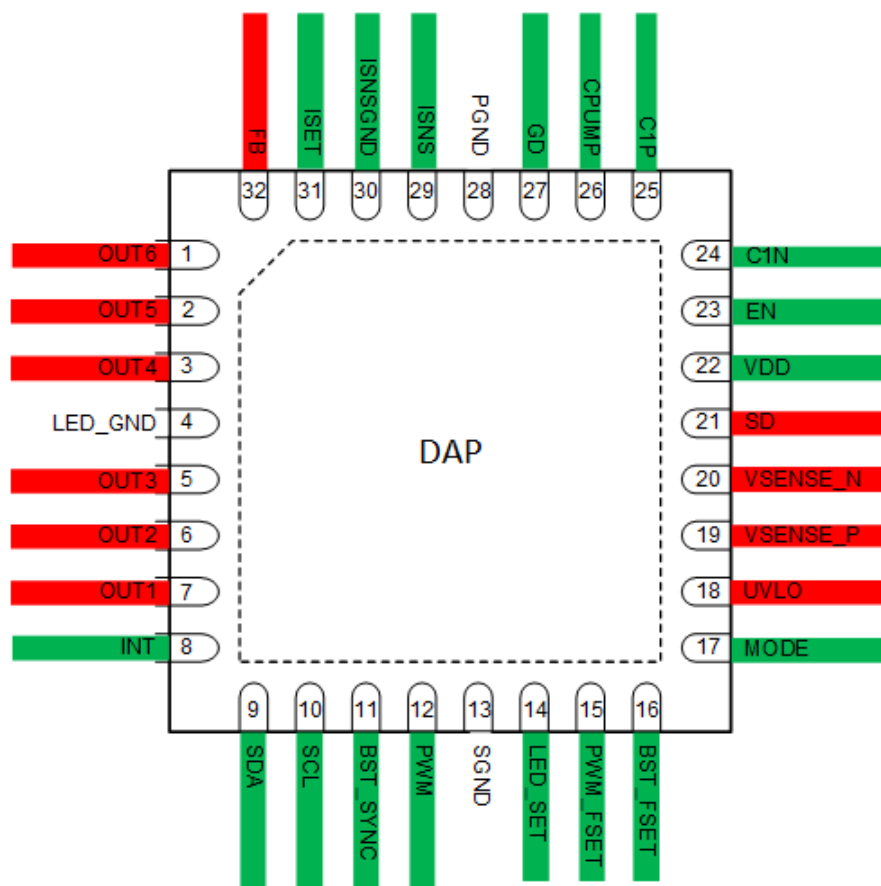


图 5-1. DCP Package 38-Pin HTSSOP Top View



Product preview

**图 5-2. RHB Package 32-PIN QFN Top View**

**表 5-1. HTTSOP Pin Functions**

| PIN |           | TYPE   | DESCRIPTION   |
|-----|-----------|--------|---|
| NO. | NAME      |        |   |
| 1   | VDD       | Power  | Power supply input for internal analog and digital circuit. Connect a 10-uF capacitor between the VDD pin to GND.   |
| 2   | EN        | Analog | Enable input.   |
| 3   | C1N       | Analog | Negative input for charge pump flying capacitor. If feature not used leave this pin floating.   |
| 4   | C1P       | Analog | Positive input for charge pump flying capacitor. If feature not used leave this pin floating.   |
| 5   | CPUMP     | Power  | Charge pump output pin. Connect to VDD if charge pump is not used. A 4.7 $\mu$ F decoupling capacitor is recommended on CPUMP pin.                          |
| 6   | CPUMP     | Power  | Charge pump output pin. Always connects with pin 5.   |
| 7   | GD        | Analog | Gate driver output for external N-FET.  |
| 8   | PGND      | GND    | Power ground.   |
| 9   | PGND      | GND    | Power ground.   |
| 10  | ISNS      | Analog | Boost current sense pin.  |
| 11  | ISNSGND   | GND    | Current sense resistor GND.   |
| 12  | ISET      | Analog | LED full-scale current setup through external resistor.   |
| 13  | FB        | Analog | Boost feedback input.   |
| 14  | NC        | N/A    | No connect - Leave floating.  |
| 15  | DISCHARGE | Analog | Boost output voltage discharge pin. Connect to Boost output.  |
| 16  | NC        | N/A    | No connect - Leave floating.  |
| 17  | OUT6      | Analog | LED current sink output. If unused tie to ground..  |
| 18  | OUT5      | Analog | LED current sink output. If unused tie to ground..  |
| 19  | OUT4      | Analog | LED current sink output. If unused tie to ground.   |
| 20  | OUT3      | Analog | LED current sink output. If unused tie to ground.   |
| 21  | OUT2      | Analog | LED current sink output. If unused tie to ground.   |
| 22  | OUT1      | Analog | LED current sink output. If unused tie to ground.   |
| 23  | NC        | N/A    | No connect - Leave floating.  |
| 24  | INT       | Analog | Device fault interrupt output, open drain. A 10-k $\Omega$ pullup resistor is recommended.  |
| 25  | SDA       | Analog | SDA for I2C interface. A 10-k $\Omega$ pullup resistor is recommended.  |
| 26  | SCL       | Analog | SCL for I2C interface. A 10-k $\Omega$ pullup resistor is recommended.  |
| 27  | BST_SYNC  | Analog | Input for synchronizing boost. When synchronization is not used, connect this pin to ground to disable spread spectrum or to VDD to enable spread spectrum. |
| 28  | PWM       | Analog | PWM input for brightness control. Tie to GND if unused.   |
| 29  | SGND      | GND    | Signal ground.  |
| 30  | LED_SET   | Analog | LED string configuration through external resistor. Do not leave floating.  |
| 31  | PWM_FSET  | Analog | LED dimming frequency setup through external resistor. Do not leave floating.   |
| 32  | BST_FSET  | Analog | Boost switching frequency setup through external resistor. Do not leave floating.   |
| 33  | MODE      | Analog | Dimming mode setup through external resistor. Do not leave floating.  |
| 34  | DGND      | GND    | Digital ground.   |
| 35  | UVLO      | Analog | Input voltage sense for programming input UVLO threshold through external resistor to VIN.  |
| 36  | VSENSE_P  | Analog | Pin for input voltage detection for OVP protection and positive input for input current sense.  |
| 37  | VSENSE_N  | Analog | Negative input for input current sense. If input current sense is not used, please tie to VSENSE_P pin.   |
| 38  | SD        | Analog | Power line FET control. Open Drain output. If unused, leave this pin floating.  |
| DAP | LED_GND   | GND    | LED ground connection.  |

表 5-2. QFN Pin Functions

| PIN |          | TYPE   | DESCRIPTION   |
|-----|----------|--------|---|
| NO. | NAME     |        |   |
| 1   | OUT6     | Analog | LED current sink output. If unused tie to ground..  |
| 2   | OUT5     | Analog | LED current sink output. If unused tie to ground..  |
| 3   | OUT4     | Analog | LED current sink output. If unused tie to ground.   |
| 4   | LED_GND  | GND    | LED ground connection.  |
| 5   | OUT3     | Analog | LED current sink output. If unused tie to ground.   |
| 6   | OUT2     | Analog | LED current sink output. If unused tie to ground.   |
| 7   | OUT1     | Analog | LED current sink output. If unused tie to ground.   |
| 8   | INT      | Analog | Device fault interrupt output, open drain. A 10-k $\Omega$ pullup resistor is recommended.  |
| 9   | SDA      | Analog | SDA for I2C interface. A 10-k $\Omega$ pullup resistor is recommended.  |
| 10  | SCL      | Analog | SCL for I2C interface. A 10-k $\Omega$ pullup resistor is recommended.  |
| 11  | BST_SYNC | Analog | Input for synchronizing boost. When synchronization is not used, connect this pin to ground to disable spread spectrum or to VDD to enable spread spectrum. |
| 12  | PWM      | Analog | PWM input for brightness control. Tie to GND if unused.   |
| 13  | SGND     | GND    | Signal ground.  |
| 14  | LED_SET  | Analog | LED string configuration through external resistor. Do not leave floating.  |
| 15  | PWM_FSET | Analog | LED dimming frequency setup through external resistor. Do not leave floating.   |
| 16  | BST_FSET | Analog | Boost switching frequency setup through external resistor. Do not leave floating.   |
| 17  | MODE     | Analog | Dimming mode setup through external resistor. Do not leave floating.  |
| 18  | UVLO     | Analog | Input voltage sense for programming input UVLO threshold through external resistor to VIN.  |
| 19  | VSENSE_P | Analog | Pin for input voltage detection for OVP protection and positive input for input current sense.  |
| 20  | VSENSE_N | Analog | Negative input for input current sense. If input current sense is not used, please tie to VSENSE_P pin.   |
| 21  | SD       | Analog | Power line FET control. Open Drain output. If unused, leave this pin floating.  |
| 22  | VDD      | Power  | Power supply input for internal analog and digital circuit. Connect a 10-uF capacitor between the VDD pin to GND  |
| 23  | EN       | Analog | Enable input.   |
| 24  | C1N      | Analog | Negative input for charge pump flying capacitor. If feature not used leave this pin floating.   |
| 25  | C1P      | Analog | Positive input for charge pump flying capacitor. If feature not used leave this pin floating.   |
| 26  | CPUMP    | Power  | Charge pump output pin. Connect to VDD if charge pump is not used. A 4.7- $\mu$ F decoupling capacitor is recommended on CPUMP pin.                         |
| 27  | GD       | Analog | Gate driver output for external N-FET.  |
| 28  | PGND     | GND    | Power ground.   |
| 29  | ISNS     | Analog | Boost current sense pin.  |
| 30  | ISNSGND  | GND    | Current sense resistor GND.   |
| 31  | ISET     | Analog | LED full-scale current setup through external resistor.   |
| 32  | FB       | Analog | Boost feedback input.   |
| DAP | LED_GND  | GND    | LED ground connection.  |

## 6 Specifications

### 6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)<sup>(1) (2)</sup>

|                 |   | MIN  | MAX                | UNIT |
|-----------------|---|------|--------------------|------|
| Voltage on pins | VSENSE_N, SD, UVLO  | -0.3 | VSENSE_P + 0.3     | V    |
| Voltage on pins | VSENSE_P, FB, DISCHARGE, OUT1 to OUT6   | -0.3 | 52                 | V    |
|                 | C1N, C1P, VDD, EN, ISNS, ISNS_GND, INT, MODE, PWM_FSET, BST_FSET, LED_SET, ISET, GD and CPUMP | -0.3 | 6                  | V    |
| Voltage on pins | PWM, BST_SYNC, SDA, SCL   | -0.3 | VDD + 0.3          | V    |
|                 | Continuous power dissipation <sup>(3)</sup>   |      | Internally Limited | W    |
| Thermal         | Ambient temperature, T <sub>A</sub> <sup>(4)</sup>  | -40  | 125                |      |
|                 | Junction temperature, T <sub>J</sub> <sup>(4)</sup>   | -40  | 150                | °C   |
|                 | Lead temperature (soldering)  |      | 260                | °C   |
|                 | Storage temperature, T <sub>stg</sub>   | -65  | 150                | °C   |

- (1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to the potential at the GND pins.
- (3) Internal thermal shutdown circuitry protects the device from permanent damage. Thermal shutdown engages at T<sub>J</sub> = 165°C (typical) and disengages at T<sub>J</sub> = 150°C (typical).
- (4) In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature may have to be derated. Maximum ambient temperature (T<sub>A-MAX</sub>) is dependent on the maximum operating junction temperature (T<sub>J-MAX</sub> = 150°C), the power dissipation of the device in the application (P), the junction-to-board thermal resistance and the temperature difference between the system board and the ambient (Δt<sub>BA</sub>), which is given by the following equation: T<sub>A-MAX</sub> = T<sub>J-MAX</sub> - (Θ<sub>JB</sub> × P) - Δt<sub>BA</sub>.

### 6.2 ESD Ratings

|                    |                         |   | VALUE                          | UNIT |
|--------------------|-------------------------|---|--------------------------------|------|
| V <sub>(ESD)</sub> | Electrostatic discharge | Human body model (HBM), per AEC Q100-002 <sup>(1)</sup> | ±2000                          | V    |
|                    |                         | Charged device model (CDM), per AEC Q100-011            | Corner pins (1, 19, 20 and 38) |      |
|                    |                         |   | Other pins                     |      |

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

### 6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)<sup>(1)</sup>

|                 |                                     | MIN | NOM   | MAX | UNIT |
|-----------------|-------------------------------------|-----|-------|-----|------|
| Voltage on pins | VSENSE_P, VSENSE_N, SD, UVLO        | 3   | 12    | 48  | V    |
|                 | FB, OUT1 to OUT6                    | 0   |       | 48  |      |
|                 | ISNS, ISNSGND                       | 0   |       | 5.5 |      |
|                 | EN, PWM, INT, SDA, SCL, BST_SYNC    | 0   | 3.3   | 5.5 |      |
|                 | VDD                                 | 3   | 3.3/5 | 5.5 |      |
|                 | C1N, C1P, CPUMP, GD                 | 0   | 5     | 5.5 |      |
| Thermal         | Ambient temperature, T <sub>A</sub> | -40 |       | 125 | °C   |

- (1) All voltages are with respect to the potential at the GND pins.

## 6.4 Thermal Information

| THERMAL METRIC <sup>(1)</sup> |   | Device | UNIT |
|-------------------------------|---|--------|------|
|                               |   | HTTSOP |      |
|                               |   | 38-PIN |      |
| R <sub>θJA</sub>              | Junction-to-ambient thermal resistance <sup>(2)</sup> | 32.4   | °C/W |
| R <sub>θJC(top)</sub>         | Junction-to-case (top) thermal resistance             | 19.5   |      |
| R <sub>θJB</sub>              | Junction-to-board thermal resistance                  | 8.8    |      |
| Ψ <sub>JT</sub>               | Junction-to-top characterization parameter            | 0.3    |      |
| Ψ <sub>JB</sub>               | Junction-to-board characterization parameter          | 8.9    |      |
| R <sub>θJC(bot)</sub>         | Junction-to-case (bottom) thermal resistance          | 2.7    |      |

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.
- (2) Junction-to-ambient thermal resistance is highly application and board-layout dependent. In applications where high maximum power dissipation exists, special care must be paid to thermal dissipation issues in board design.

## 6.5 Electrical Characteristics

Limits apply over the full operation temperature range  $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ , unless otherwise specified.  $V_{IN} = 12\text{ V}$ ,  $V_{DD} = 3.3\text{ V}$

| PARAMETER                                       |   | TEST CONDITIONS  | MIN   | TYP   | MAX   | UNIT |
|---|---|--|-------|-------|-------|------|
| <b>General Electrical Characteristics</b>       |   |  |       |       |       |      |
| I <sub>Q</sub>                                  | Shutdown mode current, VDD pin              | EN = L   |       | 1     | 5     | μA   |
| I <sub>Q</sub>                                  | Active mode current, VDD pin <sup>(1)</sup> | FSW = 303kHz, PWM = H, BOOST-FET IPD25N06S4L-30, Charge Pump Disabled  |       | 15    | 65    | mA   |
| I <sub>Q</sub>                                  | Active mode current, VDD pin <sup>(1)</sup> | FSW = 2200kHz, PWM = H, BOOST-FET IPD25N06S4L-30, Charge Pump Disabled |       | 40    | 75    | mA   |
| I <sub>Q</sub>                                  | Active mode current, VDD pin <sup>(1)</sup> | FSW = 303kHz, PWM = H, BOOST-FET IPD25N06S4L-30, Charge Pump Enabled   |       | 20    | 91    | mA   |
| I <sub>Q</sub>                                  | Active mode current, VDD pin <sup>(1)</sup> | FSW = 2200kHz, PWM = H, BOOST-FET IPD25N06S4L-30, Charge Pump Enabled  |       | 65    | 104   | mA   |
| <b>CPUMP and LDO Electrical Characteristics</b> |   |  |       |       |       |      |
| V <sub>CPUMP</sub>                              | Voltage accuracy                            | V <sub>DD</sub> = 3.0 to 3.6 V; I <sub>LOAD</sub> = 1 to 50 mA         | 4.8   | 5     | 5.2   | V    |
| f <sub>CP</sub>                                 | CP switching frequency                      |  | 387   | 417   | 447   | kHz  |
| V <sub>CPUMP_UVLO</sub>                         | VCPUMP UVLO threshold                       | V <sub>CPUMP</sub> falling edge  | 3.95  | 4.2   | 4.4   | V    |
| V <sub>CPUMP_UVLO</sub>                         | VCPUMP UVLO threshold                       | V <sub>CPUMP</sub> rising edge   | 4.15  | 4.4   | 4.6   | V    |
| V <sub>CPUMP_HYS</sub>                          | VCPUMP UVLO hysteresis                      |  | 0.1   | 0.2   |       | V    |
| T <sub>START_UP</sub>                           | Charge pump startup time                    | C <sub>CPUMP</sub> = 10 μF   |       | 1000  | 2000  | μs   |
| <b>Protection Electrical Characteristics</b>    |   |  |       |       |       |      |
| V <sub>DD_UVLO_F</sub>                          | V <sub>DD</sub> UVLO threshold              | V <sub>DD</sub> falling  | 2.68  | 2.8   | 2.92  | V    |
| V <sub>DD_UVLO_R</sub>                          | V <sub>DD</sub> UVLO threshold              | V <sub>DD</sub> rising   |       |       | 3.0   | V    |
| V <sub>DD_UVLO_H</sub>                          | V <sub>DD</sub> UVLO hysteresis             |  |       | 0.1   |       | V    |
| V <sub>IN_UVLO_TH</sub>                         | UVLO pin threshold                          | V <sub>UVLO</sub> falling  | 0.753 | 0.777 | 0.801 | V    |
| I <sub>UVLO</sub>                               | UVLO pin bias current                       | V <sub>UVLO</sub> = V <sub>UVLO_TH</sub> + 50 mV                       |       | -5    |       | μA   |



## 6.5 Electrical Characteristics (continued)

Limits apply over the full operation temperature range  $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ , unless otherwise specified.  $V_{IN} = 12\text{ V}$ ,  $V_{DD} = 3.3\text{ V}$

| PARAMETER  |  | TEST CONDITIONS  | MIN  | TYP   | MAX   | UNIT               |
|--|--|--|------|-------|-------|--------------------|
| $V_{IN\_OVP\_TH}$  | OVP threshold                                | $V_{SENSE\_P}$ rising  | 40.8 | 43    | 45.2  | V                  |
| $V_{IN\_OVP\_HYS}$   | OVP hysteresis                               |  |      | 1.7   |       | V                  |
| $V_{IN\_OCP\_TH}$  | Input OCP threshold                          | $R_{ISENSE} = 20\text{ m}\Omega$   | 187  | 220   | 253   | mV                 |
| $T_{SD}$   | Thermal shutdown threshold <sup>(1)</sup>    | Temperature rising   | 150  | 165   | 180   | $^{\circ}\text{C}$ |
| $T_{SD}$   | Thermal shutdown hysteresis <sup>(1)</sup>   |  |      | 20    |       | $^{\circ}\text{C}$ |
| $I_{SD\_LEAKAGE}$  | SD leakage current                           | $V_{SD} = 48\text{ V}$   |      | 1     |       | $\mu\text{A}$      |
| $I_{SD}$   | SD pull down current                         | $R_{SD} = 20\text{ k}\Omega$   | 250  | 325   | 400   | $\mu\text{A}$      |
| $V_{FB\_OVPL}$   | FB pin - Boost OVP low threshold             |  |      | 1.423 |       | V                  |
| $V_{FB\_OVPH}$   | FB pin - Boost OVP high threshold            |  |      | 1.76  |       | V                  |
| $V_{FB\_UVP}$  | FB pin - Boost OCP threshold                 |  |      | 0.886 |       | V                  |
| $V_{BST\_OVPH}$  | Discharge pin - Boost OVP high threshold     |  | 48.5 | 50    | 51.8  | V                  |
| <b>Input PWM Electrical Characteristics</b>                    |  |  |      |       |       |                    |
| $I_{PWM\_LEAKAGE}$   | PWM leakage current                          | $V_{PWM} = 5\text{ V}$   |      | 1     |       | $\mu\text{A}$      |
| $f_{PWM\_IN}$  | PWM input frequency                          |  | 100  |       | 20000 | Hz                 |
| $t_{PWM\_MIN\_ON}$   | PWM input minimum on-time                    | Direct PWM mode  |      |       | 200   | ns                 |
| $t_{PWM\_MIN\_ON}$   | PWM input minimum on-time                    | Phase Shift PWM mode, Hybrid mode, Current Dimming mode                      |      | 200   | 220   | ns                 |
| $PWM\_IN\_RES$   | PWM input resolution                         | $f_{PWM\_IN} = 100\text{ Hz}$  |      | 16    |       | bit                |
| $PWM\_IN\_RES$   | PWM input resolution                         | $f_{PWM\_IN} = 20\text{ kHz}$  |      | 10    |       | bit                |
| <b>LED Current Sink and LED PWM Electrical Characteristics</b> |  |  |      |       |       |                    |
| $I_{LEAKAGE}$  | Leakage current on OUTx                      | $OUTx = V_{OUT} = 45\text{ V}$ , $EN = L$                                    |      | 0.1   | 2.5   | $\mu\text{A}$      |
| $V_{ISET}$   | ISET voltage                                 |  | 1.17 | 1.21  | 1.25  | V                  |
| $I_{MAX}$  | Maximum LED sink current                     | OUTx   |      | 200   |       | mA                 |
| $V_{ISET\_UVLO}$   | ISET pin undervoltage                        |  | 0.97 | 1     | 1.03  | V                  |
| $R_{ISET}$   | ISET Resistor range                          | $I_{OUT} = 30\text{ mA}$ to $200\text{ mA}$                                  | 15.6 |       | 104   | $\text{k}\Omega$   |
| $I_{LED\_LIMIT}$   | LED current limit when ISET pin short to GND |  |      | 280   |       | mA                 |
| $I_{ACC}$  | LED sink current accuracy                    | $R_{ISET} = 15.6\text{ k}\Omega$ , $I_{OUT} = 150\text{ mA}$ , $PWM = 100\%$ | -4   |       | 4     | %                  |
| $I_{MATCH}$  | LED sink current matching                    | $R_{ISET} = 15.6\text{ k}\Omega$ , $I_{OUT} = 150\text{ mA}$ , $PWM = 100\%$ |      | 1     | 3.5   | %                  |

## 6.5 Electrical Characteristics (continued)

Limits apply over the full operation temperature range  $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ , unless otherwise specified.  $V_{IN} = 12\text{ V}$ ,  $V_{DD} = 3.3\text{ V}$

| PARAMETER                  |                               | TEST CONDITIONS                         | MIN     | TYP   | MAX   | UNIT |
|----------------------------|-------------------------------|---|---------|-------|-------|------|
| $f_{\text{DIM}}$           | LED dimming frequency         | PWM_FSET = 3.92 k $\Omega$              | 141     | 152   | 163   | Hz   |
| $f_{\text{DIM}}$           | LED dimming frequency         | PWM_FSET = 4.75 k $\Omega$              | 283     | 305   | 327   |      |
| $f_{\text{DIM}}$           | LED dimming frequency         | PWM_FSET = 5.76 k $\Omega$              | 567     | 610   | 653   |      |
| $f_{\text{DIM}}$           | LED dimming frequency         | PWM_FSET = 7.87 k $\Omega$              | 1135    | 1221  | 1307  |      |
| $f_{\text{DIM}}$           | LED dimming frequency         | PWM_FSET = 11 k $\Omega$                | 2270    | 2441  | 2612  |      |
| $f_{\text{DIM}}$           | LED dimming frequency         | PWM_FSET = 17.8 k $\Omega$              | 4541    | 4883  | 5225  |      |
| $f_{\text{DIM}}$           | LED dimming frequency         | PWM_FSET = 42.4 k $\Omega$              | 9082    | 9766  | 10450 |      |
| $f_{\text{DIM}}$           | LED dimming frequency         | PWM_FSET = 124 k $\Omega$               | 18163   | 19531 | 20899 |      |
| DIM                        | Dimming ratio                 | $f_{\text{PWM\_OUT}} = 152\text{ Hz}$   | 32000:1 |       |       |      |
| DIM                        | Dimming ratio                 | $f_{\text{PWM\_OUT}} = 4.88\text{ kHz}$ | 1000:1  |       |       |      |
| $V_{\text{HEADROOM}}$      | LED sink headroom             |   | 0.7     |       |       | V    |
| $V_{\text{HEADROOM\_HYS}}$ | LED sink headroom hysteresis  |   | 0.8     |       |       | V    |
| $V_{\text{LEDSHORT}}$      | LED internal short threshold  |   | 5.4     |       |       | V    |
| $V_{\text{SHORTGND}}$      | LED short to ground threshold |   | 0.24    |       |       | V    |
| $t_{\text{PWM\_OUT}}$      | LED output minimum pulse      |   | 200     |       |       | ns   |

### Boost Converter Electrical Characteristics

|                       |   |   |      |      |      |               |
|-----------------------|---|---|------|------|------|---------------|
| $f_{\text{SW}}$       | Switching Frequency                                 | BST_FSET = 7.87 k $\Omega$  | 93   | 100  | 107  | kHz           |
| $f_{\text{SW}}$       | Switching Frequency                                 | BST_FSET = 4.75 k $\Omega$  | 186  | 200  | 214  | kHz           |
| $f_{\text{SW}}$       | Switching Frequency                                 | BST_FSET = 5.76 k $\Omega$  | 281  | 303  | 325  | kHz           |
| $f_{\text{SW}}$       | Switching Frequency                                 | BST_FSET = 3.92 k $\Omega$  | 372  | 400  | 428  | kHz           |
| $f_{\text{SW}}$       | Switching Frequency                                 | BST_FSET = 11 k $\Omega$  | 465  | 500  | 535  | kHz           |
| $f_{\text{SW}}$       | Switching Frequency                                 | BST_FSET = 17.8 k $\Omega$  | 1690 | 1818 | 1946 | kHz           |
| $f_{\text{SW}}$       | Switching Frequency                                 | BST_FSET = 42.4 k $\Omega$  | 1860 | 2000 | 2140 | kHz           |
| $f_{\text{SW}}$       | Switching Frequency                                 | BST_FSET = 124 k $\Omega$   | 2066 | 2222 | 2378 | kHz           |
| $V_{\text{ISNS}}$     | External FET current limit                          | $V_{\text{ISNS}}$ threshold, $R_{\text{SENSE}} = 15\text{ to }50\text{ m}\Omega$                                    | 180  | 200  | 220  | mV            |
| $I_{\text{SEL\_MAX}}$ | IDAC maximum current                                | $V_{\text{DD}} = 3.3\text{ V}$  | 36.4 | 38.7 | 40.2 | $\mu\text{A}$ |
| $R_{\text{DS\_ONH}}$  | $R_{\text{DS\_ON}}$ of high-side FET to gate driver | $V_{\text{GD}}/(R_{\text{DS\_ON}} + \text{total resistance to gate input of SW FET})$ must not be higher than 2.5 A | 1.4  |      |      | $\Omega$      |
| $R_{\text{DS\_ONL}}$  | $R_{\text{DS\_ON}}$ of low-side FET to gate driver  | $V_{\text{GD}}/(R_{\text{DS\_ON}} + \text{total resistance to gate input of SW FET})$ must not be higher than 2.5 A | 0.75 |      |      | $\Omega$      |
| $t_{\text{STARUP}}$   | Start-up time                                       | Delay from beginning of boost Soft-start to when LED drivers can begin  | 50   |      |      | ms            |
| $T_{\text{ON}}$       | Minimum switch on-time                              |   | 150  |      |      | ns            |
| $T_{\text{OFF}}$      | Minimum switch off time                             |   | 150  |      |      | ns            |

(1) This specification is not ensured by ATE.

## 6.6 Logic Interface Characteristics

Limits apply over the full operation temperature range  $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ , unless otherwise specified.  $V_{IN} = 12\text{ V}$ ,  $V_{DD} = 5\text{ V}$ ,  $V_{EN} = 3.3\text{ V}$

| PARAMETER             | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|-----------------------|-----------------|-----|-----|-----|------|
| <b>LOGIC INPUT EN</b> |                 |     |     |     |      |

Limits apply over the full operation temperature range  $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ , unless otherwise specified.  $V_{IN} = 12\text{ V}$ ,  $V_{DD} = 5\text{ V}$ ,  $V_{EN} = 3.3\text{ V}$

| PARAMETER                                     |                                      | TEST CONDITIONS                         | MIN | TYP | MAX | UNIT |
|---|--------------------------------------|---|-----|-----|-----|------|
| $V_{EN_{IL}}$                                 | EN logic low threshold               |   |     |     | 0.4 | V    |
| $V_{EN_{IH}}$                                 | EN logic high threshold              |   | 1.2 |     |     | V    |
| $R_{ENPD}$                                    | EN pin internal pull down resistance |   |     | 1   |     | MΩ   |
| <b>LOGIC INPUT SDA, SCL, BST_SYNC and PWM</b> |                                      |   |     |     |     |      |
| $V_{IL}$                                      | Logic low threshold                  | $V_{DD} = 3.3\text{ V and } 5\text{ V}$ |     |     | 0.4 | V    |
| $V_{IH}$                                      | Logic high threshold                 | $V_{DD} = 3.3\text{ V and } 5\text{ V}$ | 1.2 |     |     | V    |
| <b>LOGIC OUTPUT SDA, INT</b>                  |                                      |   |     |     |     |      |
| $V_{OL}$                                      | Output level low                     | $I = 3\text{ mA}$                       |     | 0.2 | 0.4 | V    |
| $I_{LEAKAGE}$                                 | Output leakage current               | $V = 3.3\text{ V}$                      |     |     | 1   | μA   |

## 6.7 Timing Requirements for I2C Interface

Limits apply over the full operation temperature range  $-40^{\circ}\text{C} \leq T_A \leq +125^{\circ}\text{C}$ , unless otherwise specified.  $V_{IN} = 12\text{ V}$ ,  $V_{DD} = 5\text{ V}$ ,  $V_{EN} = 3.3\text{ V}$ .

| PARAMETER  |  | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------|--|-----------------|-----|-----|-----|------|
| $f_{SCLK}$ | Clock frequency                                    |                 |     |     | 400 | kHz  |
| 1          | Hold time (repeated) START condition               |                 | 0.6 |     |     | μs   |
| 2          | Clock low time                                     |                 | 1.3 |     |     | μs   |
| 3          | Clock high time                                    |                 | 600 |     |     | ns   |
| 4          | Set-up time for a repeated START condition         |                 | 600 |     |     | ns   |
| 5          | Data hold time                                     |                 | 50  |     |     | ns   |
| 6          | Data setup time                                    |                 | 100 |     |     | ns   |
| 7          | Rise time of SDA and SCL                           |                 |     |     | 300 | ns   |
| 8          | Fall time of SDA and SCL                           |                 |     |     | 300 | ns   |
| 9          | Set-up time for STOP condition                     |                 | 600 |     |     | ns   |
| 10         | Bus free time between a STOP and a START condition |                 | 1.3 |     |     | μs   |

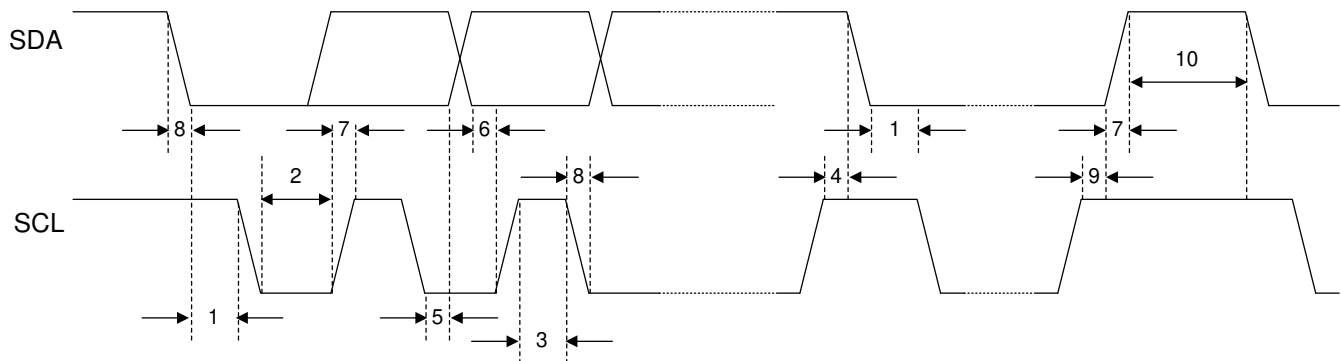
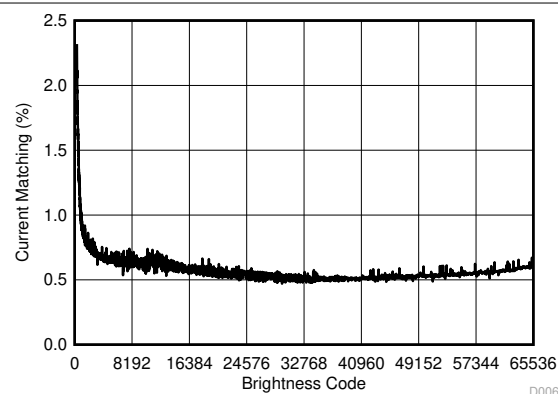
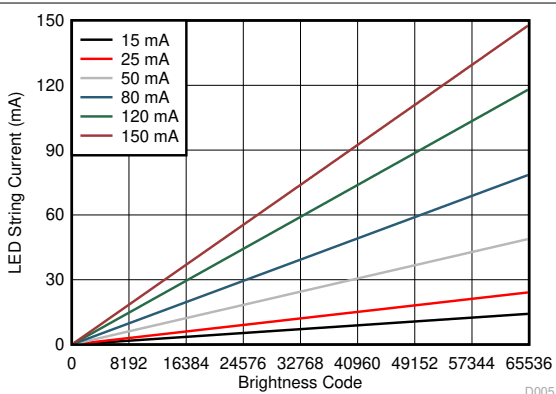
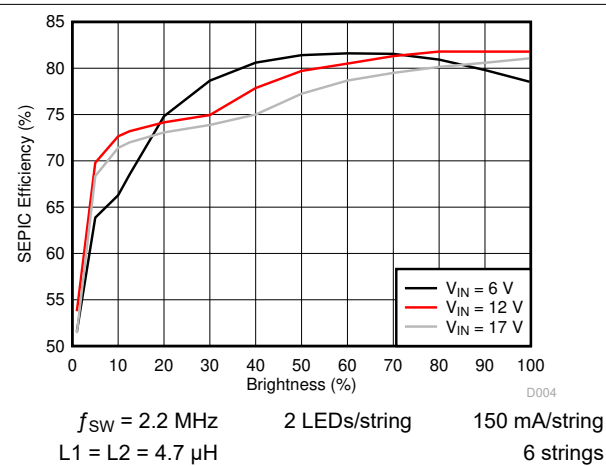
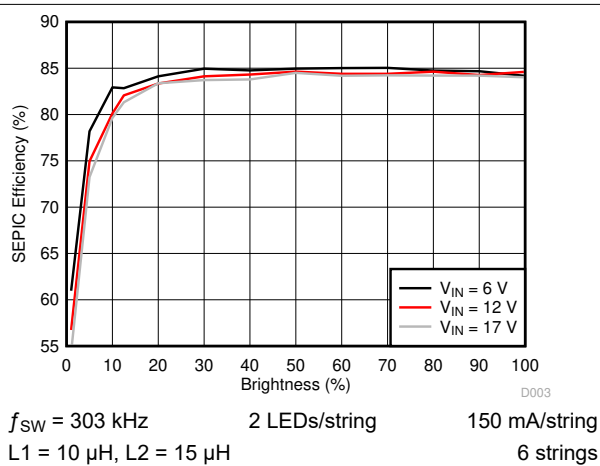
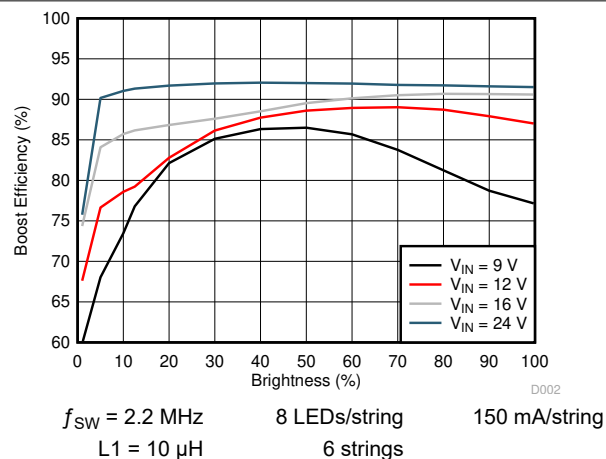
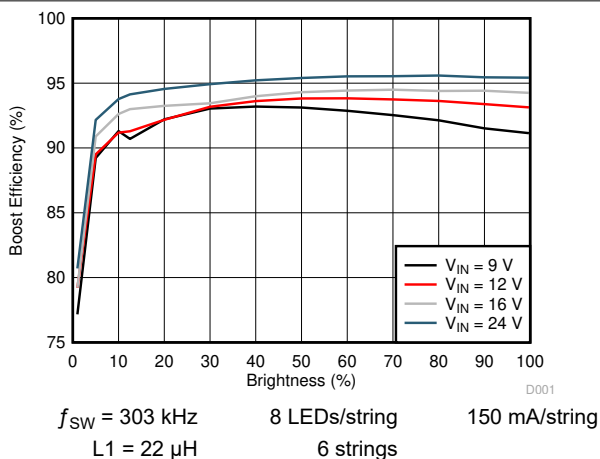


图 6-1. I2C Timing Diagram

## 6.8 Typical Characteristics

Unless otherwise specified:  $C_{IN} = C_{OUT} = 2 \times 10\text{-}\mu\text{F}$  ceramic and  $2 \times 33\text{-}\mu\text{F}$  electrolytic,  $V_{DD} = 3.3\text{ V}$ , charge pump enabled,  $T_A = 25^\circ\text{C}$



## 7 Detailed Description

### 7.1 Overview

The LP8866S-Q1 device is a high-voltage LED driver for automotive infotainment, clusters, HUD and other automotive display LED backlight applications. PWM input is used for brightness control by default. Alternatively, the brightness can also be controlled by I2C Interface.

The boost frequency, LED PWM frequency, and LED string current are configured with external resistors through the BST\_FSET, PWM\_FSET, and ISET pins. The INT pin is used to report faults to the system. Fault interrupt status can be cleared with the I2C interface, or is cleared on the falling edge of the EN pin.

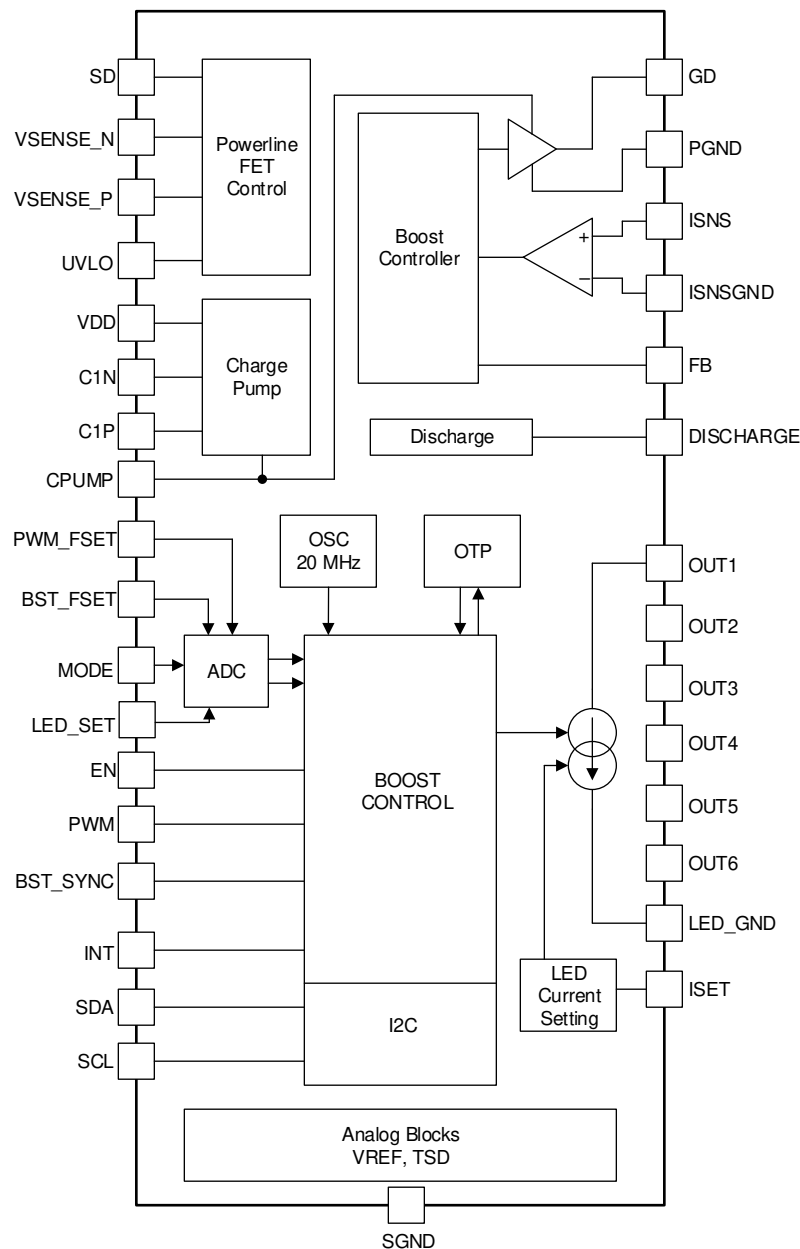
The LP8866S-Q1 supports pure PWM dimming. The six LED current drivers provide up to 150 mA per output and can be tied together to support higher current LEDs. The maximum output current of the LED drivers is set with the ISET resistor and can be optionally scaled by the LEDx\_CURRENT[11:0] register bits with I2C interface. The LED output PWM frequency is set with a PWM\_FSET resistor. The number of connected LED strings is configured by the LED\_SET resistor, and the device automatically selects the corresponding phase shift mode. For example, if the device is set to 4-strings mode, each LED output is phase shifted by 90 degrees with each other(= 360 / 4). Unused outputs, which must be connected to GND, will be disabled and excluded from adaptive voltage and won't generate any LED faults.

A resistor divider connected from V<sub>OUT</sub> to the FB pin sets the maximum voltage of the boost. For best efficiency, the boost voltage is adapted automatically to the minimum necessary level needed to drive the LED strings by monitoring all the LED output voltages continuously. The switching frequency of the boost regulator can be set between 100 kHz and 2.2 MHz by the BST\_FSET resistor. The boost has a start-up feature that reduces the peak current from the power-line during start-up. The LP8866S-Q1 can also control a power-line FET to reduce battery leakage when disabled and provide isolation and protection in the event of a fault.

Fault detection features of LP8866S-Q1 include:

- Open-string and shorted LED detection
  - LED fault detection prevents system overheating in case of open or short in some of the LED strings
- LED short-to-ground detection
- ISET/BST\_FSET/PWM\_FSET/LED\_SET/MODE resistor out-of-range detection
- Boost overcurrent
- Boost overvoltage
- Device undervoltage protection (VDD UVLO)
  - Threshold sensing from VDD pin
- V<sub>IN</sub> input overvoltage protection (V<sub>IN</sub> OVP)
  - Threshold sensing from VSENSE\_P pin
- V<sub>IN</sub> input undervoltage protection (V<sub>IN</sub> UVLO)
  - Threshold sensing from UVLO pin
- V<sub>IN</sub> input overcurrent protection (V<sub>IN</sub> OCP)
  - Threshold sensing across voltage between VSENSE\_P pin and VSENSE\_N pin
- Thermal shutdown in case of die overtemperature

## 7.2 Functional Block Diagram



## 7.3 Feature Description

### 7.3.1 Control Interface

Device control interface includes:

- EN is the enable input for the LP8866S-Q1 device.
- PWM is the default input to control the brightness of all current sinks by duty cycle.
- INT is an open-drain fault output indicating fault condition detection.
- SDA and SCL are data and clock line for I2C interface to control the brightness of all current sinks and read back the fault conditions for diagnosis.
- BST\_SYNC is used to input an external clock for the boost switching frequency and control the internal boost clock mode.
  - The external clock is auto detected at start-up and, if missing, the internal clock is used.
  - Optionally, the BST\_SYNC can be tied to VDD to enable the boost spread spectrum function or tied to GND to disable it.

- ISET pin to set the maximum LED current level per string.

### 7.3.2 Function Setting

Device parameter setting includes:

- BST\_FSET pin is used to set the boost switching frequency through a resistor to signal ground.
- PWM\_FSET pin is used to set the LED output PWM dimming frequency through a resistor to signal ground.
- MODE pin is used to set the dimming mode via an external resistor to signal ground.
- LED\_SET pin is used to set the LED configuration through a resistor to signal ground.
- ISET pin is used to set the maximum LED current level per OUTx pin.

### 7.3.3 Device Supply (VDD)

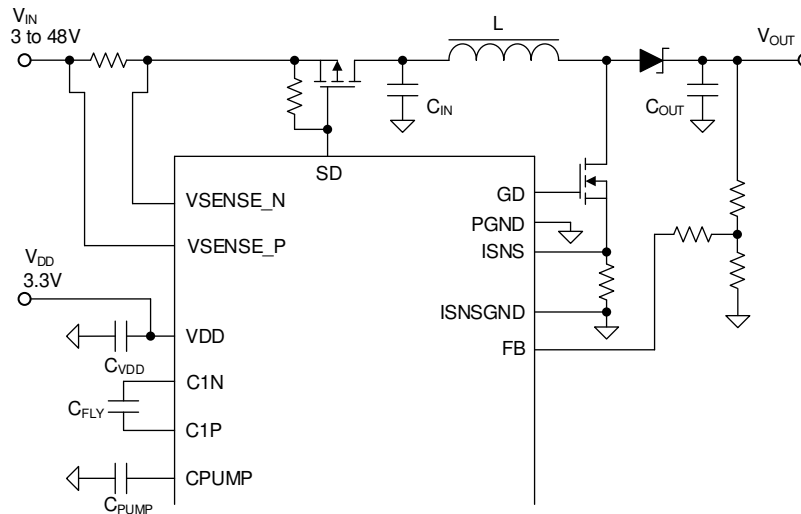
All internal analog and digital blocks of LP8866S-Q1 are biased from external supply from VDD pin. Either a typical 5-V or 3.3-V supply rail is able to supply VDD from previous linear regulator or DC/DC converter with at least 150-mA current capability.

### 7.3.4 Enable (EN)

The LP8866S-Q1 only turns on when the input voltage of EN pin is above the voltage threshold ( $V_{ENIH}$ ) and turns off when the voltage of EN pin is below the threshold ( $V_{ENIL}$ ). All analog and digital blocks start operating once the LP8866S-Q1 is enabled by asserting EN pin. The SD pin is floating, I2C interface and Fault detection are not active if the EN pin is de-asserted.

### 7.3.5 Charge Pump

An integrated regulated charge pump can be used to supply the gate drive for the external FET of the boost controller. The charge pump is enabled or disabled by automatically detecting whether VDD and CPUMP pin are connected together. If VDD is < 4.5 V then use the charge pump to generate a 5-V gate voltage to drive the external boost switching FET. To use the charge pump, a 2.2- $\mu$ F capacitor is placed between C1N and C1P. If the charge pump is not required, C1N and C1P could be left unconnected and CPUMP pins tied to VDD. A 4.7- $\mu$ F CPUMP capacitor is used to store energy for the gate driver. The CPUMP capacitor is required to be used in both charge pump enabled and disabled conditions and must be placed as close as possible to the CPUMP pins. [Figure 7-1](#) and [Figure 7-2](#) show required connections for both use cases.



**Figure 7-1. Charge Pump Enabled Circuit**

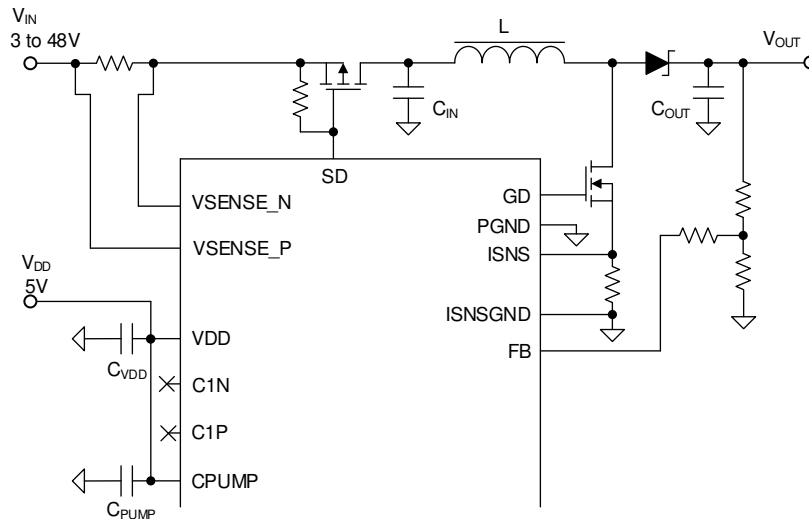


Figure 7-2. Charge Pump Disabled Circuit

If the charge pump is enabled, the CPCAP\_STATUS bit shows whether a fly capacitor was detected and the CP\_STATUS bit shows status of any charge pump faults and generates an INT signal. The CP\_INT\_EN bit can be used to prevent the charge-pump fault from causing an interrupt on the INT pin.

### 7.3.6 Boost Controller

The LP8866S-Q1 current-mode-controlled boost DC/DC controller generates the anode voltage for the LEDs. The boost is a current-mode-controlled topology with a cycle by cycle current limit. The boost converter senses the switch current and across the external sense resistor connected between ISNS and ISNSGND. A 20-mΩ sense resistor results in a 10-A cycle by cycle current limit. The sense resistor value could vary from 15 mΩ to 50 mΩ depending on the application. Maximum boost voltage is configured with external FB-pin resistor divider connected between V\_OUT and FB. The FB-diver equation is described in [セクション 7.3.6.3](#).

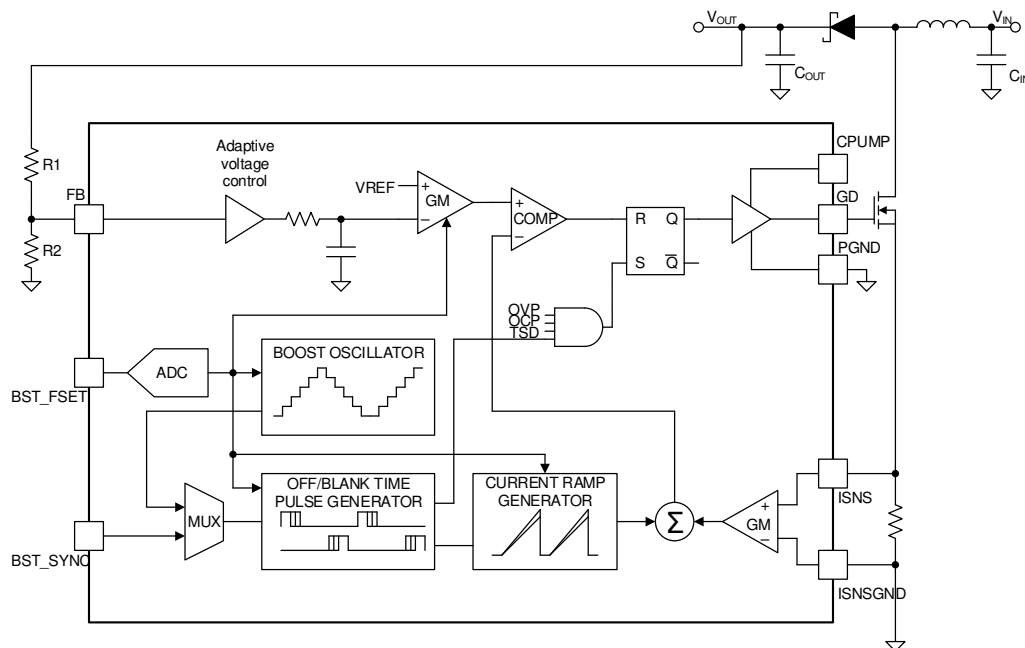


Figure 7-3. Boost Controller Block Diagram

The boost switching frequency is adjustable from 100 kHz to 2.2 MHz via an external resistor at BST\_FSET (see [表 7-1](#)). Resistor with 1% accuracy is needed to ensure proper operation.



**表 7-1. Boost Frequency Selection**

| R_BST_FSET (kΩ) | BOOST FREQUENCY (kHz) |
|-----------------|-----------------------|
| 3.92            | 400                   |
| 4.75            | 200                   |
| 5.76            | 303                   |
| 7.87            | 100                   |
| 11              | 500                   |
| 17.8            | 1818                  |
| 42.2            | 2000                  |
| 124             | 2222                  |

### 7.3.6.1 Boost Cycle-by-Cycle Current Limit

The voltage between ISNS and ISNSGND is used for both boost DC/DC controller's current sensing and cycle-by-cycle current limit settings. When the cycle-by-cycle current limit is reached, the controller will turn off the switching MOSFET immediately and turn on it again in next switching cycle. This cycle-by-cycle current limit could be used as a common protection for all related DC/DC components (inductor, schottky diode and switching MOSFET) to avoid current running over their max limit. Cycle-by-Cycle current limit won't trigger any faults of the device.

$$I_{\text{CYCLE\_LIMIT}} = \frac{V_{\text{ISNS}}}{R_{\text{SENSE}}} \quad (1)$$

where

- $V_{\text{ISNS}} = 200 \text{ mV}$

### 7.3.6.2 Controller Min On/Off Time

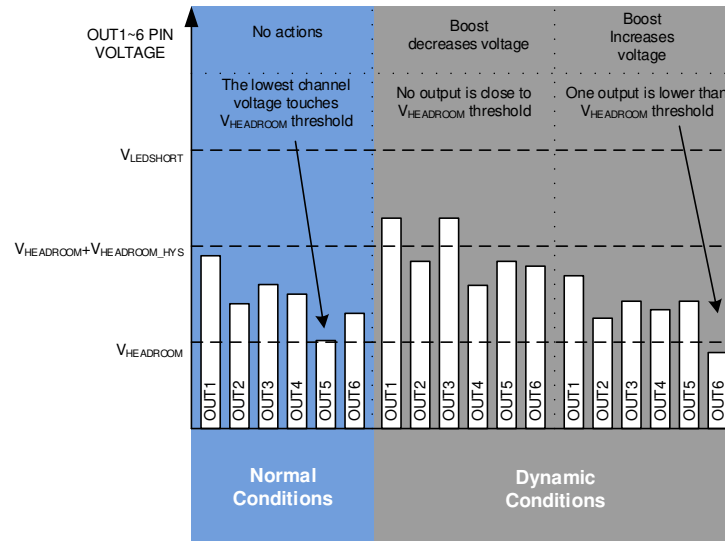
The device boost DC/DC controller has minimum on/off time as below table. Minimum off time should be specially taken care in system design. The SW node rising time plus falling time should be higher than minimum off time to avoid controller not turning off the MOSFET.

**表 7-2. Controller Minimum On/Off Time**

| Frequency (kHz) | Minimum Switch OFF Time (ns) | Minimum Switch ON Time (ns) |
|-----------------|------------------------------|-----------------------------|
| 100 to 500      | 150                          | 150                         |
| 1818 to 2222    | 40                           | 110                         |

### 7.3.6.3 Boost Adaptive Voltage Control

The LP8866S-Q1 boost DC/DC converter generates the anode voltage for the LEDs. During normal operation, boost output voltage is adjusted automatically based on the LED current sink headroom voltages. This is called adaptive boost control. The number of used LED outputs is set by LED\_SET pin and only the active LED outputs are monitored to control the adaptive boost voltage. Any LED strings with open or short faults are also removed from the adaptive voltage control loop. The LED driver pin voltages are periodically monitored by the control loop and the boost voltage is raised if any of the LED outputs falls below the  $V_{\text{HEADROOM}}$  threshold. The boost voltage is lowered until any of the LED outputs touch the  $V_{\text{HEADROOM}}$  threshold. See [图 7-4](#) for how the boost voltage automatically scales based on the OUTx-pin voltage,  $V_{\text{HEADROOM}}$  and  $V_{\text{HEADROOM\_HYS}}$ .

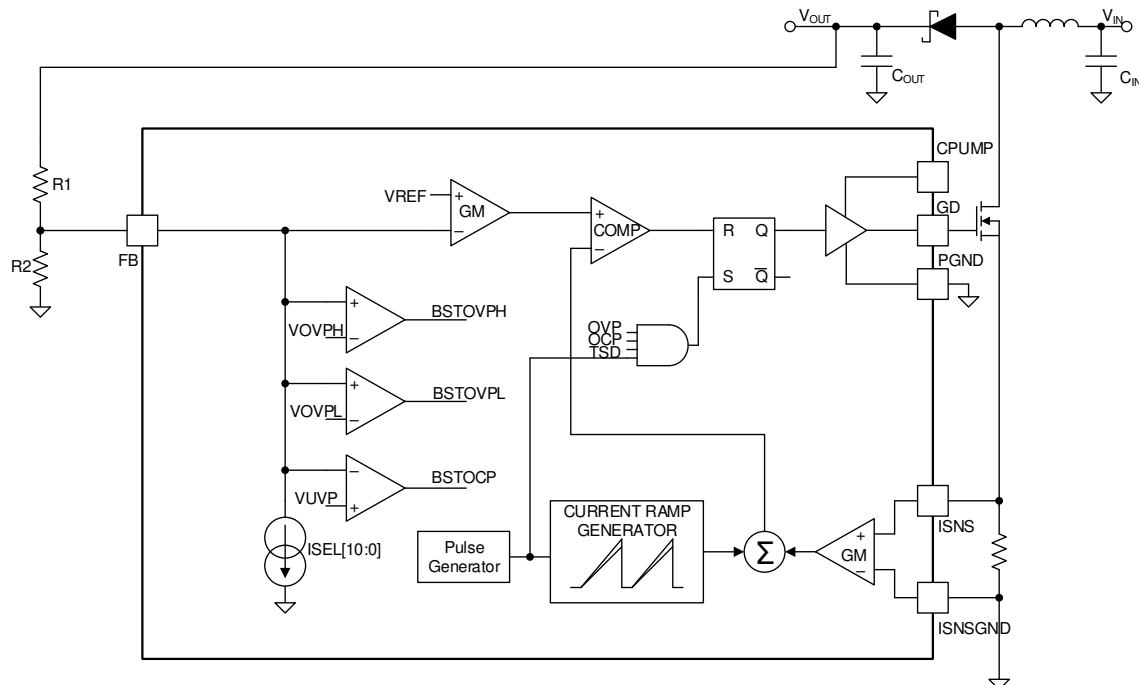


**Figure 7-4. Adaptive Boost Voltage Control Loop Function**

The resistive divider ( $R_1$ ,  $R_2$ ) defines both the minimum and maximum adaptive boost voltage levels. The feedback circuit operates the same in boost and SEPIC topologies. Choose maximum boost voltage based on the maximum LED string voltage specification. Before the LED drivers are active, the boost starts up to the initial boost level. The initial boost voltage is approximately in the 88% point of minimum to maximum boost voltage. Once the LED driver channels are active, the boost output voltage is adjusted automatically based on OUTx pin voltages. The FB pin resistor divider also scales the boost OVP, OCP levels and the LED short level in HUD application.

#### 7.3.6.3.1 FB Divider Using Two-Resistor Method

A typical FB-pin circuit uses a two-resistor divider circuit between the boost output voltage and ground.



**Figure 7-5. Two-Resistor FB Divider Circuit**

Maximum boost voltage can be calculated with [Equation 2](#). The maximum boost voltage can be reached during OPEN string detection or if all LED strings are left disconnected.

$$V_{\text{BOOST\_MAX}} = I_{\text{SEL\_MAX}} \times R_1 + \left( \frac{R_1}{R_2} + 1 \right) \times V_{\text{REF}} \quad (2)$$

where

- $V_{\text{REF}} = 1.21 \text{ V}$
- $I_{\text{SEL\_MAX}} = 38.7 \mu\text{A}$
- $R_1 / R_2$  normal recommended range is 7~15

The minimum boost voltage must be less than the minimum LED string voltage. Minimum boost voltage is calculated with [Equation 3](#):

$$V_{\text{BOOST\_MIN}} = \left( \frac{R_1}{R_2} + 1 \right) \times V_{\text{REF}} \quad (3)$$

where

- $V_{\text{REF}} = 1.21 \text{ V}$

When the boost OVP\_LOW level is reached, the boost controller stops switching the boost FET and the BSTOVPL\_STATUS bit is set. The LED drivers are still active during this condition, and the boost resumes normal switching operation once the boost output level falls. The boost OVP low voltage threshold changes dynamically with current boost voltage. It is calculated in [Equation 4](#):

$$V_{\text{BOOST\_OVPL}} = V_{\text{BOOST}} + \left( \frac{R_1}{R_2} + 1 \right) \times (V_{\text{FB\_OVPL}} - V_{\text{REF}}) \quad (4)$$

where

- $V_{\text{FB\_OVPL}} = 1.423 \text{ V}$
- $V_{\text{REF}} = 1.21 \text{ V}$

When the boost OVP\_HIGH level is reached the boost controller enters fault recovery mode, and the BSTOVPH\_STATUS bit is set. The boost OVP high-voltage threshold also changes dynamically with current boost voltage and is calculated in [Equation 5](#):

$$V_{\text{BOOST\_OVPH}} = V_{\text{BOOST}} + \left( \frac{R_1}{R_2} + 1 \right) \times (V_{\text{FB\_OVPH}} - V_{\text{REF}}) \quad (5)$$

where

- $V_{\text{FB\_OVPH}} = 1.76 \text{ V}$
- $V_{\text{REF}} = 1.21 \text{ V}$

When the boost UVP level is reached the boost controller starts a 110-ms OCP counter. The LP8866S-Q1 device enters the fault recovery mode and sets the BSTOCP\_STATUS bit if the boost voltage does not rise above the UVP threshold before the timer expires. The boost UVP voltage threshold also changes dynamically with current boost voltage and is calculated in [Equation 6](#):

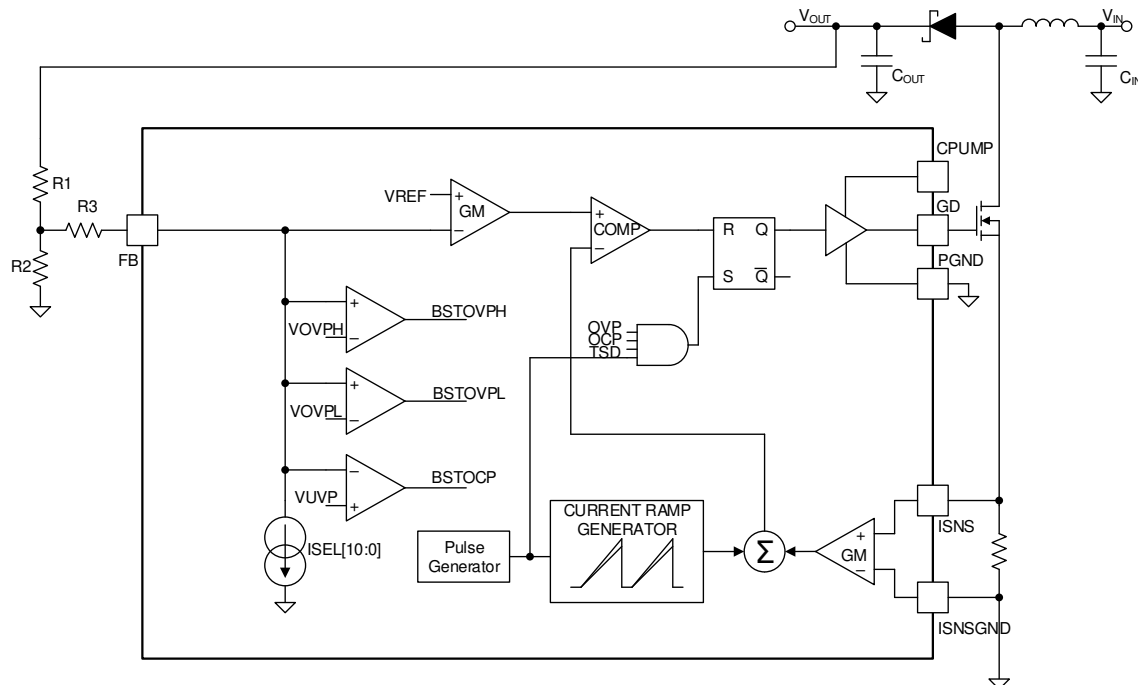
$$V_{\text{BOOST\_UVP}} = V_{\text{BOOST}} - \left( \frac{R_1}{R_2} + 1 \right) \times (V_{\text{REF}} - V_{\text{UVP}}) \quad (6)$$

where

- $V_{\text{UVP}} = 0.886 \text{ V}$
- $V_{\text{REF}} = 1.21 \text{ V}$

#### 7.3.6.3.2 FB Divider Using Three-Resistor Method

A FB-pin circuit using a three-resistor divider circuit can be used for applications where less than 200-k $\Omega$  resistors are required.



### 7-6. Three-Resistor FB Divider Circuit

Maximum boost voltage can be calculated with [Equation 7](#). The maximum boost voltage can be reached during OPEN string detection or if all LED strings are left disconnected.

$$V_{\text{BOOST\_MAX}} = \left( \frac{R_1 \times R_3}{R_2} + R_1 + R_3 \right) \times I_{\text{SEL\_MAX}} + \left( \frac{R_1}{R_2} + 1 \right) \times V_{\text{REF}} \quad (7)$$

where

- $V_{REF} = 1.21\text{ V}$
- $I_{SEL\_MAX} = 38.7\text{ }\mu\text{A}$
- $R_1 / R_2$  normal recommended range is 7 to 15

The minimum boost voltage must be less than the minimum LED string voltage. Minimum boost voltage is calculated in [Equation 8](#):

$$V_{\text{BOOST\_MIN}} = \left( \frac{R_1}{R_2} + 1 \right) \times V_{\text{REF}} \quad (8)$$

When the boost OVP\_LOW level is reached the boost controller stops switching the boost FET, and the BSTOVPL\_STATUS bit is set. The LED drivers are still active during this condition, and the boost resumes normal switching operation once the boost output level falls. The boost OVP low voltage threshold changes dynamically with current boost voltage. It is calculated in [Equation 9](#):

$$V_{\text{BOOST\_OVPL}} = V_{\text{BOOST}} + \left( \frac{R_1}{R_2} + 1 \right) \times (V_{\text{FB\_OVPL}} - V_{\text{REF}}) \quad (9)$$

where

- $V_{\text{FB\_OVPL}} = 1.423 \text{ V}$
- $V_{\text{REF}} = 1.21 \text{ V}$

When the boost OVP\_LOW level is reached the boost controller enters fault recovery mode, and the BSTOVPH\_STATUS bit is set. The boost OVP high-voltage threshold also changes dynamically with current boost voltage and is calculated in [Equation 10](#):

$$V_{\text{BOOST\_OVPH}} = V_{\text{BOOST}} + \left( \frac{R_1}{R_2} + 1 \right) \times (V_{\text{FB\_OVPH}} - V_{\text{REF}}) \quad (10)$$

where

- $V_{\text{FB\_OVPH}} = 1.76 \text{ V}$
- $V_{\text{REF}} = 1.21 \text{ V}$

When the boost UVP level is reached the boost controller starts a 110-ms OCP counter. The LP8866S-Q1 device enters the fault recovery mode and sets the BSTOCP\_STATUS bit if the boost voltage does not rise above the UVP threshold before the timer expires. The boost UVP voltage threshold also changes dynamically with current boost voltage and is calculated in [Equation 11](#):

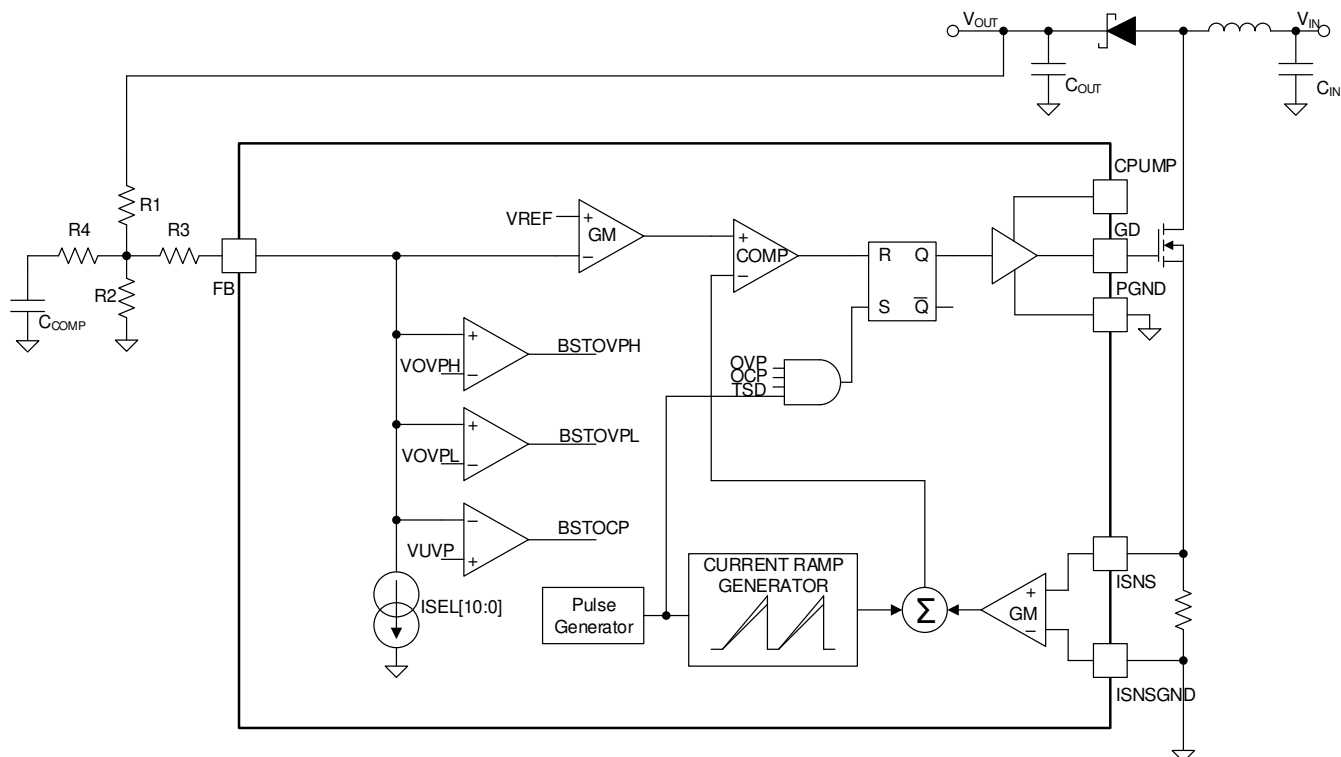
$$V_{\text{BOOST\_UVP}} = V_{\text{BOOST}} - \left( \frac{R_1}{R_2} + 1 \right) \times (V_{\text{REF}} - V_{\text{UVP}}) \quad (11)$$

where

- $V_{\text{UVP}} = 0.886 \text{ V}$
- $V_{\text{REF}} = 1.21 \text{ V}$

#### 7.3.6.3.3 FB Divider Using External Compensation

The device has internal compensation network to keep the DC-DC control loop in good stability in most cases. However, an additional external compensation network could also be added on FB-pin to offer more flexibility in loop design or solving some extreme use-cases.



**图 7-7. External Compensation Network**

This network will create one additional pole and one additional zero in the loop.

$$f_{\text{POLE\_COMP}} = \frac{1}{2\pi[(R_1 \parallel R_2) + R_4]C_{\text{COMP}}} \quad (12)$$

$$f_{\text{ZERO\_COMP}} = \frac{1}{2\pi R_4 C_{\text{COMP}}} \quad (13)$$

It could be noted that  $R_3$  doesn't take part in the compensation. So this external compensation network could be both used in two-divider network and T-divider network with no equation change.

In real application, for example, when DC-DC loop has stability concern, putting the additional pole in 1 kHz and the additional zero in 2 kHz will suppress the loop gain by approximately 6 dB after 2 kHz. This will benefit gain margin and phase margin a lot.

### 7.3.6.4 Boost Sync and Spread Spectrum

Spread spectrum function could be enabled when BST\_SYNC pin is high and disabled when BST\_SYNC pin is low.

If an external CLK signal is on the BST\_SYNC pin, the boost controller can be clocked by this signal. If the clock disappears later, the boost continues operation at the frequency defined by RBST\_FSET resistor, and the spread spectrum function will be enabled or disabled depending on the final pin level of BST\_SYNC.

**表 7-3. Boost Synchronization Mode**

| BST_SYNC PIN LEVEL | BOOST CLOCK MODE         |
|--------------------|--------------------------|
| Low (GND)          | Spread spectrum disabled |
| High (VDDIO)       | Spread spectrum enabled  |

**表 7-3. Boost Synchronization Mode (continued)**

| BST_SYNC PIN LEVEL                  | BOOST CLOCK MODE  |
|-------------------------------------|---|
| 100-kHz to 2222-kHz clock frequency | Spread spectrum disabled, external synchronization mode |

If using the external BST\_SYNC input, the  $R_{BST\_SET}$  resistor should be chosen the closest boost frequency options with the external frequency.

The spread spectrum function helps to reduce EMI noise around the switching frequency and its harmonic frequencies. The internal spread spectrum function modulates the boost frequency  $\pm 3.3\%$  to  $7.2\%$  from the central frequency with a 200-Hz to 1.2-kHz modulation frequency. The switching frequency variation is programmable by SPREAD\_RANGE register, and the modulation frequency is programmable by SPREAD\_MOD\_FREQ register. The spread-spectrum function cannot be used when an external synchronization clock is used.

**表 7-4. Spread Spectrum Frequency Range**

| SPREAD_RANGE (Binary) | SWITCHING FREQUENCY VARIATION |
|-----------------------|-------------------------------|
| 00                    | $\pm 3.3\%$                   |
| 01                    | $\pm 4.3\%$                   |
| 10 (Default)          | $\pm 5.3\%$                   |
| 11                    | $\pm 7.2\%$                   |

**表 7-5. Spread Spectrum Modulation Frequency**

| SPREAD_MOD_FREQ (Binary) | MODULATION FREQUENCY |
|--------------------------|----------------------|
| 00 (Default)             | 200 Hz               |
| 01                       | 500 Hz               |
| 10                       | 800 Hz               |
| 11                       | 1200 Hz              |

### 7.3.6.5 Boost Output Discharge

When the EN pin is pulled low, the device stops the boost controller and LED current sinks, turns off the power-line FET, and starts to discharge the boost output. The discharge pin typically sinks 30-mA current. The discharge duration is 400 ms. After 400 ms, the device shuts down. The DISCHARGE pin must be connected with boost output for normal operation.

There is one internal comparator to monitor the voltage of DISCHARGE pin. As soon as the voltage of DISCHARGE pin is higher than  $V_{BST\_OVPH}$  (typically 50 V), the device enters into fault recovery mode, and BST\_OVPH fault is reported. This provides further protection if boost voltage is out of control because of system failure.

Discharge function is only available in HTSSOP package. It's not available in QFN package.

### 7.3.6.6 Light Load Mode

The DC-DC controller will enter into light load mode in below condition:

- $V_{IN}$  voltage is very close to  $V_{OUT}$
- Loading current is very low
- PWM pulse width is very short

When DC-DC converter enters into light load mode, it stops switching occasionally to make sure output voltage won't rise up too much. It could also be called as PFM mode, since the DC-DC converter switching frequency will change in this mode.

### 7.3.7 LED Current Sinks

#### 7.3.7.1 LED Output Current Setting

The maximum output LED current is set by an external resistor value. For the application only using external resistor  $R_{ISET}$  to set the maximum LED current for each string, the Equation 14 is used to calculate the current setting of all strings:

$$I_{LED} = \frac{1.21V}{R_{ISET}} \times 2580 \quad (14)$$

The LEDx\_CURRENT[11:0] registers can also be used to adjust strings current down from this maximum. The default value for LEDx\_CURRENT[11:0] registers is the maximum 0xFFFF(4095). Equation 15 is used to calculate the current setting of an individual string:

$$I_{LED} = \left( \frac{1.21V}{R_{ISET}} \times 2580 \right) \times \left( \frac{LED\_CURRENT[11:0]}{4095} \right) \quad (15)$$

For high accuracy of LED current, the  $I_{LED}$  current is recommended to set in range from 30 mA to 200 mA. So the  $R_{ISET}$  value is in the range from 15.6 kΩ to 104 kΩ.

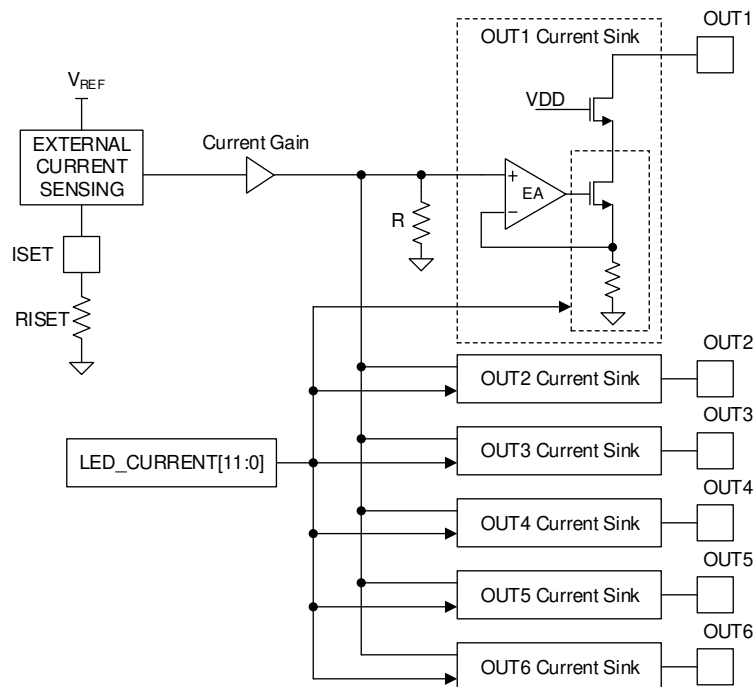


图 7-8. LED Driver Current Setting Circuit

#### 7.3.7.2 LED Output String Configuration

The Six LED driver channels of the LP8866S-Q1 device is configured by the LED\_SET resistor, which supports applications using one to Six LED strings. Resistor with 1% accuracy is needed to ensure proper operation. The driver channels can also be tied together in groups of one, two or three. This allows the LP8866S-Q1 device to drive three 300-mA LED strings, two 450-mA LED strings, or one 900-mA LED string. The LED strings are always appropriately phase shifted for their string configuration. This reduces the ripple seen at the boost output, which allows smaller output capacitors and reduces audible ringing in the capacitors. Phase shift increases



the load frequency, which can move potential capacitor noise above the audible band while still keeping PWM frequency low to support a higher dimming ratio.

When the LP8866S-Q1 device is firstly powered on, the string configuration is configured by the LED\_SET resistor and the phases of each channel are automatically configured. The LED string configuration must not be changed unless the LP8866S-Q1 is powered off in shutdown state. The unused LEDx pins should be tied to ground.

**表 7-6. LED Output String Configuration**

| R_LED_SET (kΩ) | CONFIGURATION | OUT1   | OUT2   | OUT3          | OUT4          | OUT5          | OUT6          | AUTOMATIC<br>PHASE<br>SHIFT |
|----------------|---------------|--------|--------|---------------|---------------|---------------|---------------|-----------------------------|
| 3.92           | 6 Channels    | 150 mA | 150 mA | 150 mA        | 150 mA        | 150 mA        | 150 mA        | 60°                         |
| 4.75           | 5 Channels    | 150 mA | 150 mA | 150 mA        | 150 mA        | 150 mA        | (Tied to GND) | 72°                         |
| 5.76           | 4 Channels    | 150 mA | 150 mA | 150 mA        | 150 mA        | (Tied to GND) | (Tied to GND) | 90°                         |
| 7.87           | 3 Channels    | 150 mA | 150 mA | 150 mA        | (Tied to GND) | (Tied to GND) | (Tied to GND) | 120°                        |
| 11             | 2 Channels    | 150 mA | 150 mA | (Tied to GND) | (Tied to GND) | (Tied to GND) | (Tied to GND) | 180°                        |
| 17.8           | 3 Channels    | 300 mA |        | 300 mA        |               | 300 mA        |               | 120°                        |
| 42.2           | 2 Channels    | 450 mA |        |               | 450 mA        |               |               | 180°                        |
| 124            | 1 Channels    | 900 mA |        |               |               |               |               | None                        |

### 7.3.7.3 LED Output PWM Clock Generation

The LED PWM frequency is asynchronous from the input PWM frequency. The LED PWM frequency is generated from the internal 20-MHz oscillator and can be set to eight discrete frequencies from 152 Hz to 19.531 kHz. The PWM dimming resolution is highest when the lowest PWM frequency is used. The PWM\_FSET resistor determines the LED PWM frequency based on 表 7-8. PWM resolution in Table 7-8 is with PWM dither disabled.

### 7.3.8 Brightness Control

The LP8866S-Q1 supports global brightness control for all LED strings through either duty cycle input on PWM pin or register by I2C bus. An internal 20-MHz clock is used for generating PWM outputs.

#### 7.3.8.1 Brightness Control Signal Path

The BRT\_MODE register selects whether the input to the display brightness path is the PWM input pin or DISP\_BRT register. PWM input control will be the default setup after power on. The brightness control signal path diagram is shown in 図 7-9

The display brightness path has sloper function that can be enabled. By default the sloper function is enabled. The sloper and dither function also can be programmable by I2C control. The sloper function is described in セクション 7.3.8.7, and the dither function is described in セクション 7.3.8.9.

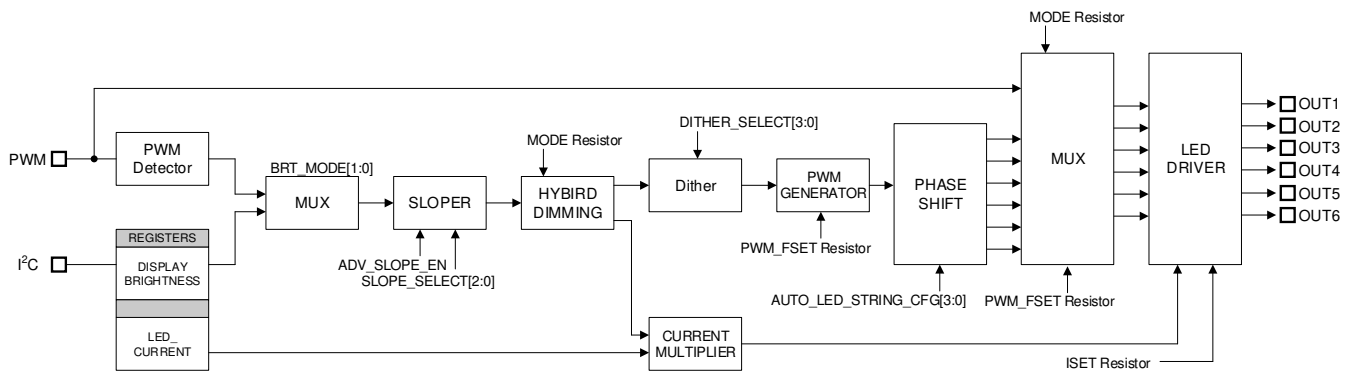


图 7-9. LP8866S-Q1 Brightness Path Diagram

### 7.3.8.2 Dimming Mode

Dimming mode can be adjusted via an external resistor to MODE pin (see 表 7-7). Resistor with 1% accuracy is needed to ensure proper operation.

表 7-7. Dimming Mode Configuration

| R_MODE (kΩ) | MODE                 | I2C Address |
|-------------|----------------------|-------------|
| 3.92        | Phase-shift PWM Mode | 0x2B        |
| 4.75        | Hybrid Mode          | 0x2B        |
| 5.76        | Current Dimming Mode | 0x2B        |
| 7.87        | Direct PWM Mode      | 0x2B        |
| 11          | Phase-shift PWM Mode | 0x2A        |
| 17.8        | Hybrid Mode          | 0x2A        |
| 42.2        | Current Dimming Mode | 0x2A        |
| 124         | Direct PWM Mode      | 0x2A        |

### 7.3.8.3 LED Dimming Frequency

The LED dimming frequency is asynchronous from the input PWM frequency for phase-shift PWM mode and hybrid dimming mode. The LED dimming frequency is generated from the internal 20-MHz oscillator and can be set to eight discrete frequencies from 152 Hz to 19.531 kHz. The PWM dimming resolution is highest when the lowest PWM frequency is used. The PWM\_FSET resistor determines the LED Dimming frequency based on 表 7-8. Resistor with 1% accuracy is needed to ensure proper operation. PWM resolution in 表 7-8 is with PWM dither disabled.

表 7-8. LED PWM Frequency Selection

| R_PWM_FSET (kΩ) | LED PWM FREQUENCY (Hz) | PWM DIMMING RESOLUTION (bits) |
|-----------------|------------------------|-------------------------------|
| 3.92            | 152                    | 16                            |
| 4.75            | 305                    | 16                            |
| 5.76            | 610                    | 15                            |
| 7.87            | 1221                   | 14                            |
| 11              | 2441                   | 13                            |
| 17.8            | 4883                   | 12                            |
| 42.2            | 9766                   | 11                            |
| 124             | 19531                  | 10                            |

### 7.3.8.4 Phase-Shift PWM Mode

In Phase-Shift PWM mode, all current active channels are turned on and off at LED dimming frequency with a constant delay. However, the number of used channels or channel groups determine the phase delay time between two neighboring channels as shown in 图 7-10.

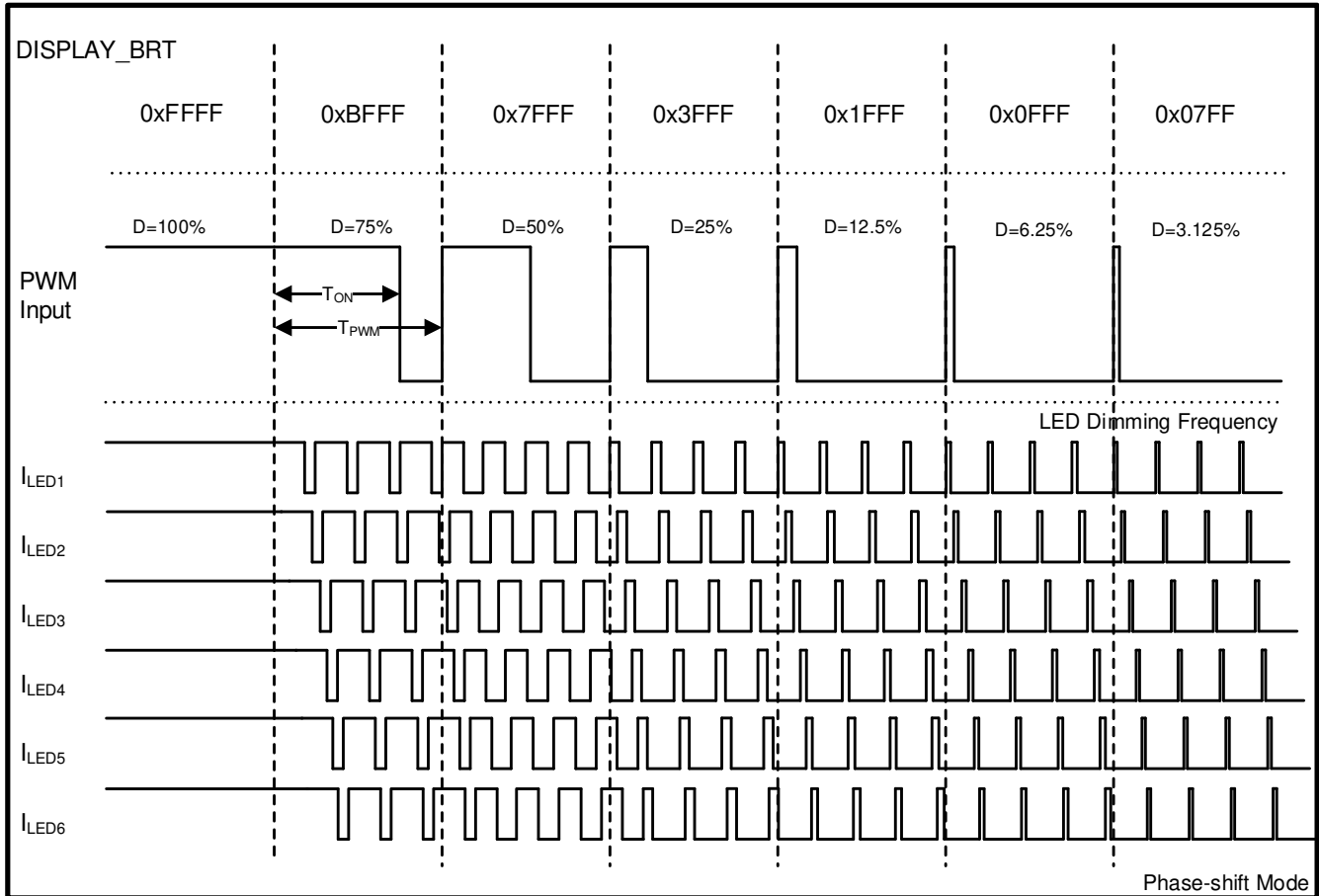


图 7-10. Phase-Shift Dimming Diagram

### 7.3.8.5 Hybrid Mode

In addition to phase-shift PWM dimming, LP8866S-Q1 supports a hybrid-dimming mode. Hybrid dimming combines PWM and current modes for brightness control for the display brightness path. By using hybrid dimming, dimming ratio could be increased by another 8 times. In hybrid mode, PWM dimming is used for low brightness range of brightness, and current dimming is used for high brightness levels as shown in 图 7-11. Current dimming control enables improved optical efficiency due to increased LED efficiency at lower currents. PWM dimming control at low brightness levels ensures linear and accurate control. Hybrid mode can be selected through resistor value at MODE pin as 表 7-7. The PWM and current modes transition threshold can be set at 12.5% or at 0% brightness. The latter selection allows for pure current dimming control mode.

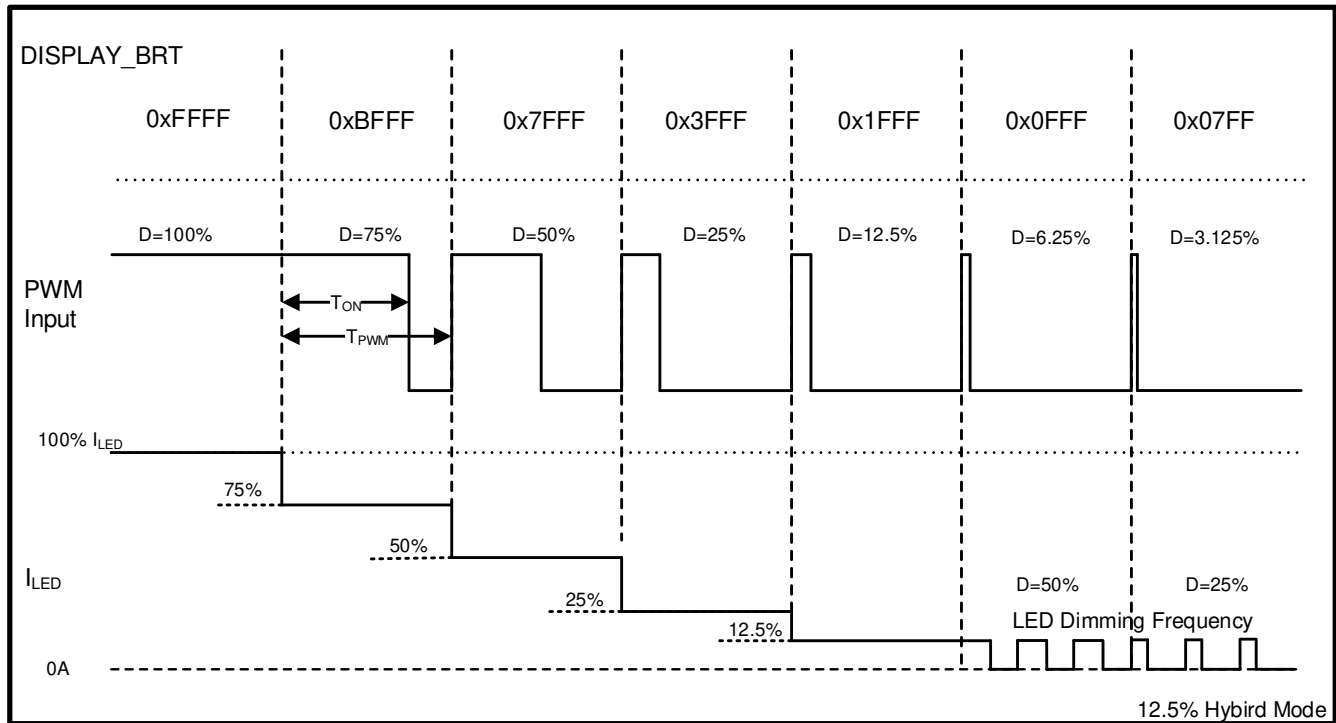


图 7-11. Hybrid Dimming Diagram

#### 7.3.8.6 Direct PWM Mode

In direct PWM mode, all active channels are turned on and off and are synchronized with the input PWM signal.

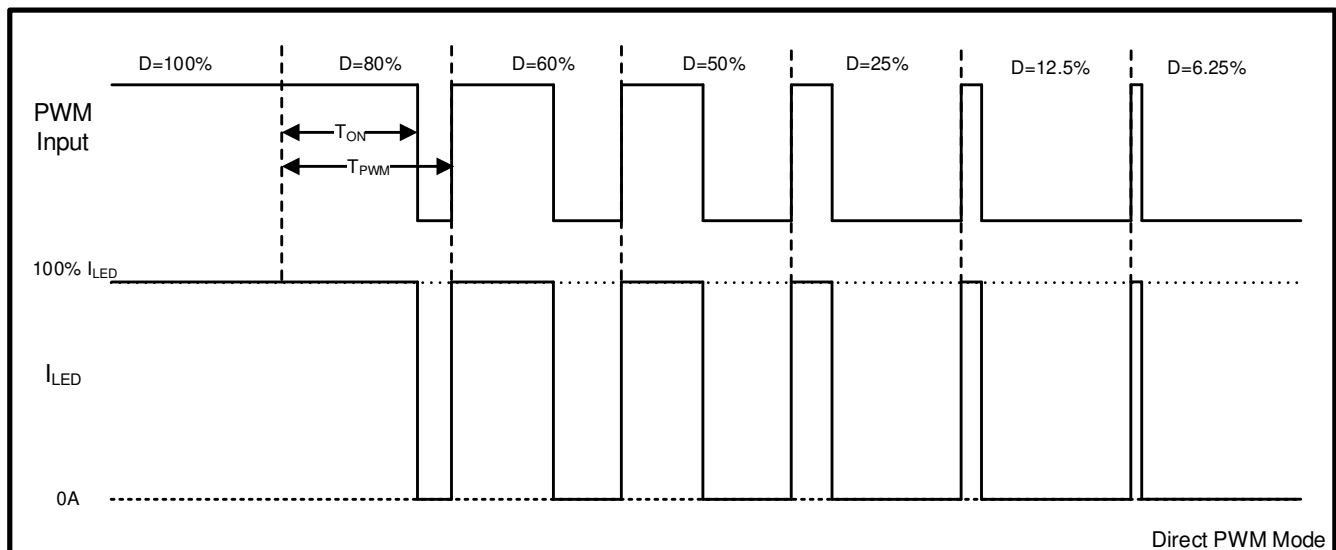
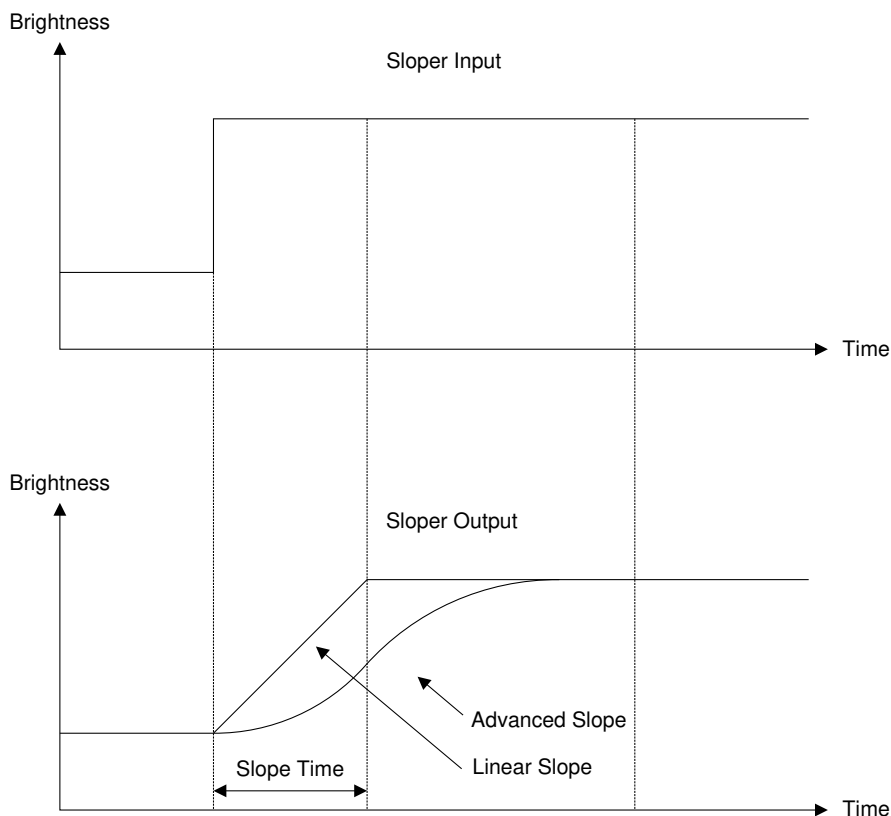


图 7-12. Direct PWM Dimming Diagram

#### 7.3.8.7 Sloper

An optional sloper function makes the transition from one brightness value to another optically smooth. By default the advanced sloper is enabled with a 200-ms linear sloper duration. Transition time between two brightness values is programmed with the SLOPE\_SELECT[2:0] bits (when 000, sloper is disabled). With advanced sloper enabled the brightness changes are further smoothed to be more pleasing to the human eye. Advanced slope is enabled with ADV\_SLOPE\_ENABLE register bit.



**图 7-13. Brightness Sloper**

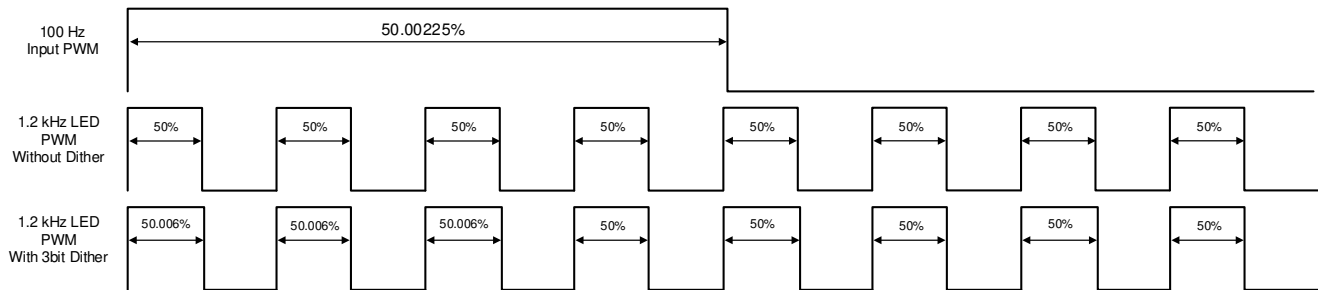
#### 7.3.8.8 PWM Detector Hysteresis

PWM detector has an internal hysteresis function. It means when PWM input is used (except direct PWM mode), PWM output duty cycle will change only when PWM input on-time changes by more than 6.4 $\mu$ s. This is to avoid the PWM duty cycle sampling error due to the onboard PWM signal's rising/falling time.

#### 7.3.8.9 Dither

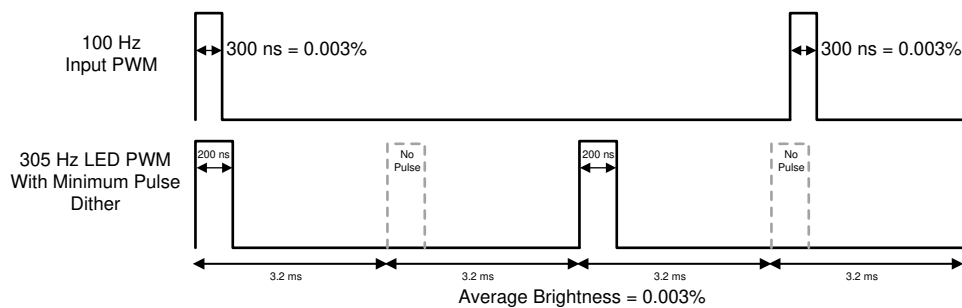
The number of brightness steps when using LED output PWM dimming is equal to the 20-MHz oscillator frequency divided by the LED PWM frequency (set by PWM\_FSET resistor). The PWM duty cycle dither is a function the LP8866S-Q1 uses to increase the number of brightness dimming steps beyond this oscillator clock limitation. The dither function modulates the LED driver output duty cycle over time to create more possible average brightness levels. The DITHER\_SELECT[3:0] register bits control the level of dither, disabled, 1, 2, 3 or 4 bits using the I2C interface. By default the dither is disabled.

When the 1-bit dither is selected, to support higher brightness resolution, the width of every second PWM pulse could be increased by one LSB (one 20-MHz clock period). When the 3-bit dither is selected, within a sequence of 8 PWM periods the number of pulses with increased length varies depending on the dither value: dither value 000 - all 8 pulses at default length; 001 - one of the 8 pulses is longer; 010 - two of the 8 pulses are longer, and so forth, until at 111 - seven of the 8 pulses have increased length. 图 7-14 shows one example of PWM output dither.



**FIG 7-14. PWM Dither Example**

The dither block also helps in low brightness scenario when dimming ratio is limited by LED PWM output frequency and the LED output pulse is less than the minimum pulse width (200 ns). In such scenario, the dither block will skip some of the PWM pulses to reduce the brightness further, enabling high dimming ratio. The end result is that the LED PWM frequency is reduced as more and more minimum pulses are skipped or dithered out. At the same time, dither block will also guarantee that the minimum LED PWM frequency is not less than 152 Hz to ensure no brightness flickering. FIG 7-15 shows how the dither works in low brightness scenario.



**FIG 7-15. Minimum Brightness Dither Example**

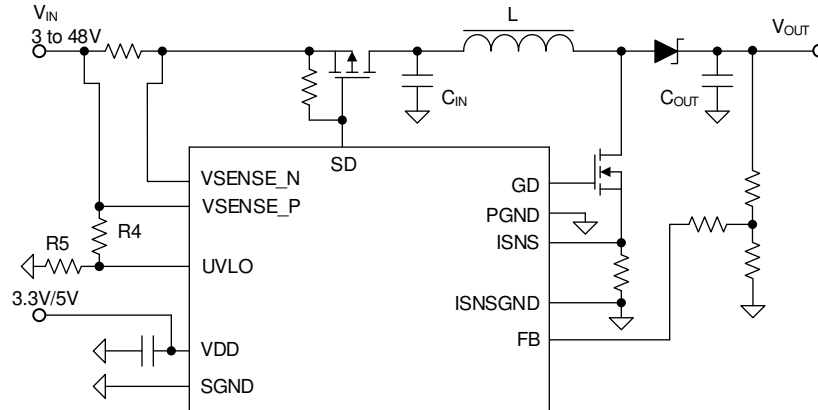
### 7.3.9 Protection and Fault Detections

The LP8866S-Q1 device includes fault detections for LED open, short and short-to-GND conditions, boost input undervoltage, overvoltage and overcurrent, boost output overvoltage and overcurrent, VDD undervoltage, die overtemperature and external components. The host can monitor the status of the faults in registers SUPPLY\_FAULT\_STATUS, BOOST\_FAULT\_STATUS and LED\_STATUS.

#### 7.3.9.1 Supply Faults

##### 7.3.9.1.1 $V_{IN}$ Undervoltage Faults (VINUVLO)

The LP8866S-Q1 device supports  $V_{IN}$  undervoltage and overvoltage protection. The undervoltage threshold is programmable through external resistor divider on UVLO pin. If during operation of the LP8866S-Q1 device, the UVLO pin voltage falls below the UVLO falling level (0.787 V typical), the boost, LED outputs, and power-line FET will be turned off, and the device will enter STANDBY mode. The VINUVLO\_STATUS bit is also set in the SUPPLY\_FAULT\_STATUS register, and the INT pin is triggered. When the UVLO voltage rises above the rising threshold level the LP8866S-Q1 exits STANDBY and begins the start-up sequence.



**图 7-16.  $V_{IN}$  UVLO Setting Circuit**

The following equation is used to calculate the UVLO threshold for VIN rising edge:

$$VIN_{UVLO\_RISING} = \left( \frac{R_4}{R_5} + 1 \right) \times VIN_{UVLO\_TH} \quad (16)$$

where

- $VIN_{UVLO\_TH} = 0.787 \text{ V}$

The hysteresis of UVLO threshold can be designed and calculated with the following equation.

$$VIN_{HYST} = R_4 \times I_{UVLO} \quad (17)$$

where

- $I_{UVLO} = 5 \mu\text{A}$

So the following equation can be used for UVLO threshold for VIN falling edge:

$$VIN_{UVLO\_FALLING} = VIN_{UVLO\_RISING} - VIN_{HYST} \quad (18)$$

The bottom resistors,  $R_5$  of voltage divider is able to be disconnected to the GND through an additional external N-type of FET as 图 7-17. This design is to minimize the current leakage from VIN in shutdown mode to extend the battery life.

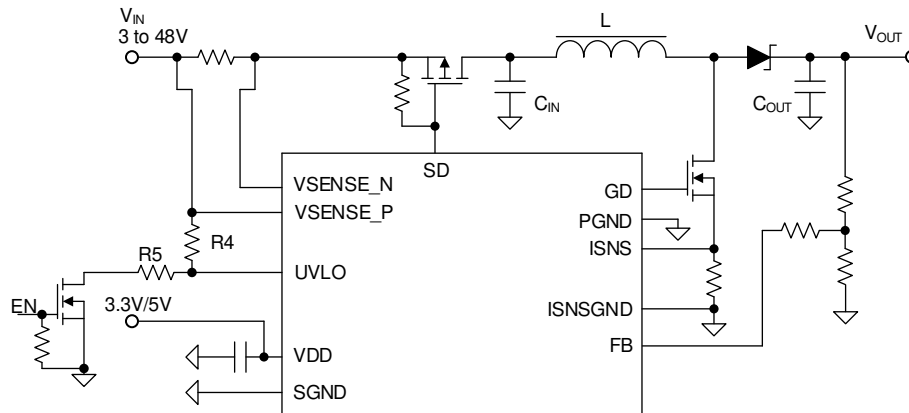


FIG 7-17.  $V_{IN}$  UVLO Setting Circuit Without Current Leakage Path

#### 7.3.9.1.2 $V_{IN}$ Overvoltage Faults (VINOVP)

The overvoltage threshold for  $V_{IN}$  rising edge is internal fixed at typical 43 V. If during LP8866S-Q1 operation, VSENSE\_P pin voltage rises above the OVP rising threshold, boost, LED outputs, and power-line FET will be turned off, and the device will enter STANDBY mode. The VINOVP\_STATUS bit will also be set in the SUPPLY\_FAULT\_STATUS register, and the INT pin will be triggered. When the VSENSE\_P pin voltage falls below the falling threshold level, the LP8866S-Q1 exits STANDBY and begins the start-up sequence.

#### 7.3.9.1.3 $V_{DD}$ Undervoltage Faults (VDDUVLO)

If during LP8866S-Q1 device operation VDD falls below VDDUVLO falling level, boost, power-line FET, and LED outputs are turned off, and the device enters STANDBY mode. The VDDUVLO\_STATUS fault bit will be set in the SUPPLY\_FAULT\_STATUS register, and the INT pin will be triggered. The LP8866S-Q1 restarts automatically to ACTIVE mode when  $V_{DD}$  rises above VDDUVLO rising threshold.

#### 7.3.9.1.4 $V_{IN}$ OCP Faults (VINOCP)

If during LP8866S-Q1 device operation voltage drop on RISENSE resistor rises above 220 mV, boost, power-line FET, and LED outputs are turned off, and the device enters Fault Recovery mode and then attempt to restart 100 ms after fault occurs. The VINOCP\_STATUS fault bit are set in the SUPPLY\_FAULT\_STATUS register, and the INT pin is triggered.

$$I_{VIN\_OCP} = \frac{V_{IN\_OCP\_TH}}{R_{ISENSE}} \quad (19)$$

where

- $V_{IN\_OCP\_TH} = 220 \text{ mV}$

##### 7.3.9.1.4.1 $V_{IN}$ OCP Current Limit vs. Boost Cycle-by-Cycle Current Limit

$V_{IN}$  OCP current limit is totally different from boost cycle-by-cycle current limit.

Boost cycle-by-cycle current limit is to protect the DC/DC components (inductor, schottky diode and switching MOSFET) in normal scenario, avoiding current running over their max limit. The normal scenario means when loading has sharp change or input voltage has sharp change. It won't trigger any device fault.

$V_{IN}$  OCP current limit is to protect system from critical system hazard (e.g, inductor short, switching MOSFET short). It will trigger the device to shutdown all the LED channels and enter into fault recovery state.

$V_{IN}$  OCP current limit should be always greater than boost cycle-by-cycle current limit. This means  $R_{ISENSE}$  should be always no smaller than  $R_{SENSE}$ .



#### 7.3.9.1.5 Charge Pump Faults (CPCAP, CP)

If during LP8866S-Q1 device operation voltage of CPUMP pin falls below typical 4.2-V, boost, power-line FET, and LED outputs are turned off, and the device enters Fault Recovery mode and then attempt to restart 100 ms after fault occurs. The CP\_STATUS fault bit will be set in the SUPPLY\_FAULT\_STATUS register, and the INT pin are triggered.

If during LP8866S-Q1 device initialization, the charge pump fly capacitor is disconnected or shorted, charge pump are turned off. In result, boost, power-line FET, and LED outputs are turned off, and the device enters Fault Recovery mode and then attempt to restart 100 ms after fault occurs. Both CPCAP\_STATUS and CP\_STATUS fault bits are set in the SUPPLY\_FAULT\_STATUS register, and the INT pin are triggered.

#### 7.3.9.1.6 CRC Error Faults (CRCERR)

If during LP8866S-Q1 device initialization, the factory default configuration for registers, options and trim bits are not corrected loaded from memory, LP8866S-Q1 keeps operating normally, unless other fault criteria is triggered. The CRCERR\_STATUS fault bit are set in the SUPPLY\_FAULT\_STATUS register and the INT pin are triggered.

### 7.3.9.2 Boost Faults

#### 7.3.9.2.1 Boost Overvoltage Faults (BSTOVPL, BSTOVPH)

Boost overvoltage is detected if the FB pin voltage exceeds the  $V_{FB\_OVPL}$  threshold. When boost overvoltage is detected, BSTOVPL\_STATUS bit will be set in the BOOST\_FAULT\_STATUS register. The boost FET stops switching, and the output voltage will be automatically limited. If the BSTOVPL\_STATUS bit is continually set (that is, reappears after clearing), it may indicate an loop issue in the application. Boost overvoltage low is monitored during device Boost Softstart and Normal mode.

A second boost overvoltage high fault is detected if the FB pin voltage exceeds the  $V_{FB\_OVPH}$  threshold or the DISCHARGE pin voltage exceeds the  $V_{BST\_OVPH}$ . The LP8866S-Q1 device enters the fault recovery state to protect system damage from a high boost voltage. When boost overvoltage is detected, BSTOVPH\_STATUS bit is set in the BOOST\_FAULT\_STATUS register. A fault interrupt is also generated. The device enters Fault Recovery mode and then attempt to restart after 100 ms. Boost overvoltage high is monitored during Boost Softstart and Normal mode.

#### 7.3.9.2.2 Boost Overcurrent Faults (BSTOCP)

Boost overcurrent is detected if the FB pin voltage drops below the  $V_{UVP}$  threshold for 110 ms. If the boost overcurrent timer expires before the output voltage recovers, the BSTOCP\_STATUS bit is set in the BOOST\_FAULT\_STATUS register. The fault recovery state is entered, and a fault interrupt is generated. The device will enter Fault Recovery mode and then attempt to restart after 100 ms. If the BSTOCP\_STATUS bit is permanently set, it may indicate an issue in the application. Boost overcurrent is monitored from the boost start, and fault may trigger during boost start-up.

#### 7.3.9.2.3 LEDSET Resistor Missing Faults (LEDSET)

The LEDSET resistor missing or invalid is detected if the resistor is not assembled or not valid value as requested during the initialization. The LP8866S-Q1 device defaults to 6-channel/150-mA configuration if the LEDSET resistor is missing or invalid. The LEDSET\_STATUS fault bit is set in the BOOST\_FAULT\_STATUS register. The LEDSET resistor missing or invalid fault will not be monitored after initialization, so that the LP8866S-Q1 is operating in the configuration determined during initialization even though the LEDSET resistor is missing or invalid after initialization.

#### 7.3.9.2.4 MODE Resistor Missing Faults (MODESEL)

The MODE resistor missing or invalid is detected if the resistor is not assembled or not valid value as requested during the initialization. LP8866S-Q1 defaults to phase-shift PWM mode with I2C address 0x2A if the MODE resistor is missing or invalid. The MODESEL\_STATUS fault bit will be set in the BOOST\_FAULT\_STATUS register. The MODE resistor missing or invalid fault is not monitored after initialization, so that the LP8866S-Q1 operates in the mode determined during initialization even though the MODE resistor is missing or invalid after initialization.

### 7.3.9.2.5 FSET Resistor Missing Faults (FSET)

The FSET resistor missing or invalid for both BOOST\_FSET and PWM\_FSET is detected if any one of them is not assembled or not a valid value as requested during the initialization. LP8866S-Q1 defaults the switching frequency of boost to 400 kHz if BOOST\_FSET resistor is missing or invalid, or PWM dimming frequency to 305 Hz if PWM\_FSET resistor is missing or invalid. The FSET\_STATUS fault bit is set in the BOOST\_FAULT\_STATUS register. The FSET resistor missing or invalid fault is not monitored after initialization, so that the LP8866S-Q1 device operates at the boost switching frequency and the PWM dimming frequency determined during initialization even though the FSET resistor is missing or invalid after initialization.

### 7.3.9.2.6 ISET Resistor Out of Range Faults (ISET)

If the ISET pin resistor is shorted to GND during normal operation, the maximum current for each LED channel can be calculated in [Equation 20](#):

$$I_{LED\_ISET\_FAULT} = I_{LED\_LIMIT} \times \left( \frac{LED\_CURRENT[11:0]}{4095} \right) \quad (20)$$

where

- $I_{LED\_LIMIT} = 280 \text{ mA}$

LED\_CURRENT[11:0] register will be automatically modified to 1/4 of latest programmed data. if it is not programmed after device enabling, the default value of LED\_CURRENT[11:0] register is 0xFFFF and automatically modified to 0x3FF after the fault occurs. If ISET pin voltage returns back to above 1.1 V, the LED\_CURRENT[11:0] register data automatically returns to latest programmed data. The ISET\_STATUS fault bit will be set in the BOOST\_FAULT\_STATUS register and the INT pin is triggered.

### 7.3.9.2.7 Thermal Shutdown Faults (TSD)

If the die temperature of LP8866S-Q1 reaches the thermal shutdown threshold  $T_{SD}$ , the boost, power-line FET, and LED outputs on LP8866S-Q1 shuts down to protect the device from damage. Fault status bit TSD\_STATUS bit will be set, and the INT pin will be triggered. The device restarts the power-line FET, the boost, and LED outputs when temperature drops by TSD\_HYS amount.

## 7.3.9.3 LED Faults

### 7.3.9.3.1 Open LED Faults (OPEN\_LED)

During normal boost operation, boost voltage is raised if any of the used LED outputs falls below the LED\_DRV\_HEADROOM threshold level. Open LED fault is detected if boost output voltage has reached the maximum and at least one LED output is still below the threshold. The open string is then disconnected from the boost adaptive control loop and its output is disabled. Any LED fault sets the status bit LED\_STATUS and an interrupt is generated unless LED interrupt is disabled. The detail of open LED faults can be read from bits OPEN\_LED and LEDx\_FAULT (x = 1...6). These bits maintain their value until device power-down. But the LED\_STATUS bit could be cleared by the interrupt clearing procedure. If a new LED fault is detected, LED\_STATUS is set and an interrupt generated again.

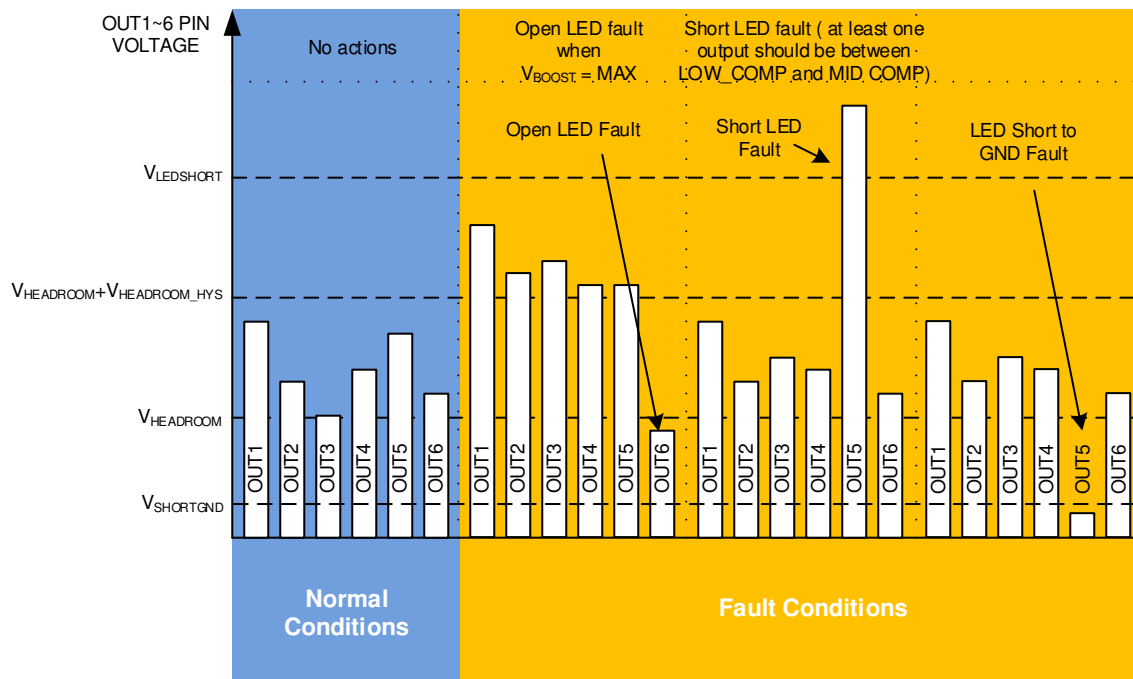


图 7-18. LED Open and Short Detection Logic

#### 7.3.9.3.2 Short LED Faults (SHORT\_LED)

Short LED fault is detected if one or more LED outputs are above the  $V_{LEDSHORT}$  typical 5.4 V and at least one LED output is inside the normal operation window (see 图 7-18). Shorted string is disconnected from the boost adaptive control loop and the LED PWM output is disabled. LED\_STATUS status bit is set and an interrupt generated similarly as in open LED case. Detailed shorted LED fault can be read from bits SHORT\_LED and LEDx\_FAULT ( $x = 1...6$ ), indicating the faulty LED) in LED\_FAULT\_STATUS register.

In HUD application, when output channels are connected as groups and only one or two groups are active, one more special condition will trigger the short LED fault. This is when boost adaptive voltage comes to minimum and one of the LED channels voltage is still higher than  $V_{HEADROOM} + V_{HEADROOM\_HYS}$ .

#### 7.3.9.3.3 LED Short to GND Faults (GND\_LED)

During boost soft start and normal boost operation, if LED output is lower than  $V_{SHORTGND}$  for 20 ms, device turns off the corresponding LED output channel and output a typical 6-mA current for 300-μs period again. After this operation, if output voltage is still lower than  $V_{HEADROOM}$ , LED short to GND fault will be reported.

If LED short to GND is reported, boost, LED outputs and power-line FET is turned off, the device will enter Fault Recovery mode. LED\_STATUS bit is set and an interrupt generated similarly as in open LED case. LED short to GND fault reason can be read from bits LED\_GND and LEDx\_FAULT ( $x = 1...6$ ) in LED\_FAULT\_STATUS register. These bits maintain their value until device powers are down while the LED\_STATUS bit is cleared by the interrupt clearing procedure.

#### 7.3.9.3.4 Invalid LED String Faults (INVSTRING)

During device initialization, any of un-used LED outputs pins are checked whether connected to GND or not. If they are not connected to GND as expected, the LP8866S-Q1 reports invalid string fault and tries to function normally if possible. The INVSTRING\_STATUS fault bit is set in the LED\_FAULT\_STATUS register, and the INT pin is triggered. The LEDSET resistor missing or invalid fault is not detected after initialization, so that the LP8866S-Q1 operates in the configuration determined during initialization even though the LEDSET resistor is missing or invalid after initialization.

#### 7.3.9.3.5 I2C Timeout Faults

If chip receives I2C command without STOP signal for 500 ms, I2C communication block auto resets and waits for the next command. I2C\_ERROR\_STATUS fault bit is set in the LED\_FAULT\_STATUS register, and the INT pin is triggered.

### 7.3.9.4 Overview of the Fault and Protection Schemes

**表 7-9. Fault and Protection Schemes**

| FAULT NAME                     | STATUS BIT     | CONDITION  | TRIGGER FAULT INTERRUPT | ENTER FAULT RECOVERY | ACTION  |
|--------------------------------|----------------|--|-------------------------|----------------------|---|
| V <sub>IN</sub> undervoltage   | VINUVLO_STATUS | UVLO voltage falls below 0.787 V.  | Yes                     | Yes                  | Device goes to standby and then attempts to restart once the input voltage rises above threshold.   |
| V <sub>IN</sub> overvoltage    | VINOVP_STATUS  | V <sub>IN</sub> voltage rises above 43 V.  | Yes                     | Yes                  | Device goes to standby and waits until input voltage falls below threshold before restarting.   |
| V <sub>DD</sub> undervoltage   | VDDUVLO_STATUS | V <sub>DD</sub> level falls below VDDUVLO threshold.   | Yes                     | No                   | Device restarts once VDD level rises above VDDUVLO threshold.   |
| V <sub>IN</sub> overcurrent    | VINOCPP_STATUS | Voltage across R <sub>ISENSE</sub> exceeds 220 mV.   | Yes                     | Yes                  | Device goes to Fault Recovery and then attempts to restart 100 ms after fault occurs.   |
| Charge pump fault              | CP_STATUS      | Charge pump voltage level is abnormal.   | Yes                     | Yes                  | Device goes to Fault Recovery and then attempts to restart 100 ms after fault occurs.   |
| Charge pump components missing | CPCAP_STATUS   | Charge pump is missing components.   | Yes                     | No                   | Charge pump is disabled. Charge pump fault will be reported. Device tries to keep normal operation.   |
| Boost sync clock invalid fault | BSTSYNC_STATUS | Device is enabled while a valid external SYNC clock is running. Then SYNC stops or changes to frequency < 75 kHz.  | Yes                     | No                   | Defaults to internal clock frequency selected by BST_FSET resistor. If BST_SYNC input is held high then spread spectrum is enabled. If BST_SYNC input is held low then spread spectrum is disabled. |
| CRC error                      | CRCERR_STATUS  | Factory default configuration for registers, options and trim bits are not correctly loaded from memory.           | Yes                     | No                   | Device functions normally, if possible.   |
| Boost OVP low                  | BSTOVPL_STATUS | FB pin voltage rises above V <sub>FB_OVPL</sub> level.   | No                      | No                   | Boost stops switching until boost voltage level falls. The device remains in normal mode with LED drivers operational.  |
| Boost OVP high                 | BSTOVPH_STATUS | FB pin voltage rises above V <sub>FB_OVPH</sub> level or DISCHARGE pin voltage rises above V <sub>BST_OVPH</sub> . | Yes                     | Yes                  | Device goes to Fault Recovery and waits until output voltage falls below threshold before restarting.   |
| Boost overcurrent              | BSTOCP_STATUS  | FB pin voltages falls below V <sub>UVF</sub> level for 110 ms.   | Yes                     | Yes                  | Device goes to Fault Recovery and then attempts to start 100 ms after fault occurs.   |
| LEDSET detection fault         | LEDSET_STATUS  | LEDSET resistor missing or invalid.  | No                      | No                   | Defaults to 6-channel / 150-mA configuration.   |
| MODE detection fault           | MODESEL_STATUS | MODE resistor missing or invalid.  | No                      | No                   | Defaults to phase-shift PWM mode, I2C address is 0x2A.  |
| FSET detection fault           | FSET_STATUS    | BST_FSET or PWM_FSET resistor are missing or an invalid value.   | No                      | No                   | Device keeps operating at 400-kHz switching frequency for boost converter and 305 Hz for PWM dimming frequency.   |

表 7-9. Fault and Protection Schemes (continued)

| FAULT NAME                  | STATUS BIT           | CONDITION   | TRIGGER FAULT INTERRUPT | ENTER FAULT RECOVERY | ACTION  |
|-----------------------------|----------------------|---|-------------------------|----------------------|---|
| ISET resistor fault         | ISET_STATUS          | ISET pin voltage is pulled down to below 1V due to ISET pin resistor shorted to GND   | Yes                     | No                   | LED_CURRENT[11:0] is written to 0x3FF. Total LED current limited to 70 mA.  |
| Thermal shutdown            | TSD_STATUS           | Junction temperature rises above $T_{SD}$ threshold.  | Yes                     | Yes                  | Device goes to standby and then attempts to restart once die temperature falls below threshold.                     |
| Open LED string             | LED_STATUS_OPEN_LED  | Headroom voltage on one or more channels is below minimum level and boost has adapted to maximum level.   | Yes                     | No                   | Faulted LED string is disabled and removed from adaptive boost control loop. String is re-enabled next power cycle. |
| LED internal short          | LED_STATUS_SHORT_LED | Headroom voltage on one or more channels is above the SHORTED_LED_THRESHOLD for > 5 ms while the headroom of at least one channel is still below this threshold.  | Yes                     | No                   | Faulted LED string is disabled and removed from adaptive boost control loop. String is re-enabled next power cycle. |
| LED short to GND            | LED_STATUS_GND_LED   | During PL FET SOFT START, voltage of one or more used LED output is below $V_{HEADROOM}$ when small test current is injected.<br>In BOOST_SU and Normal Stage, voltage of one or more used LED output is below $V_{SHORTGND}$ and keeps still when the corresponding channel is off and small test current is injected. | Yes                     | Yes                  | Device goes to Fault Recovery and then attempts to restart 100 ms after fault occurs.                               |
| Invalid LED string detected | INVSTRING_STATUS     | Configured unused LED output is detected not short to GND.  | Yes                     | No                   | Device functions normally, if possible.   |
| I2C timeout                 | I2C_ERROR_STATUS     | Device receives I2C command without STOP signal for 500 ms.   | Yes                     | No                   | Device functions normally and waits for the next I2C command.   |

## 7.4 Device Functional Modes

### 7.4.1 State Diagram

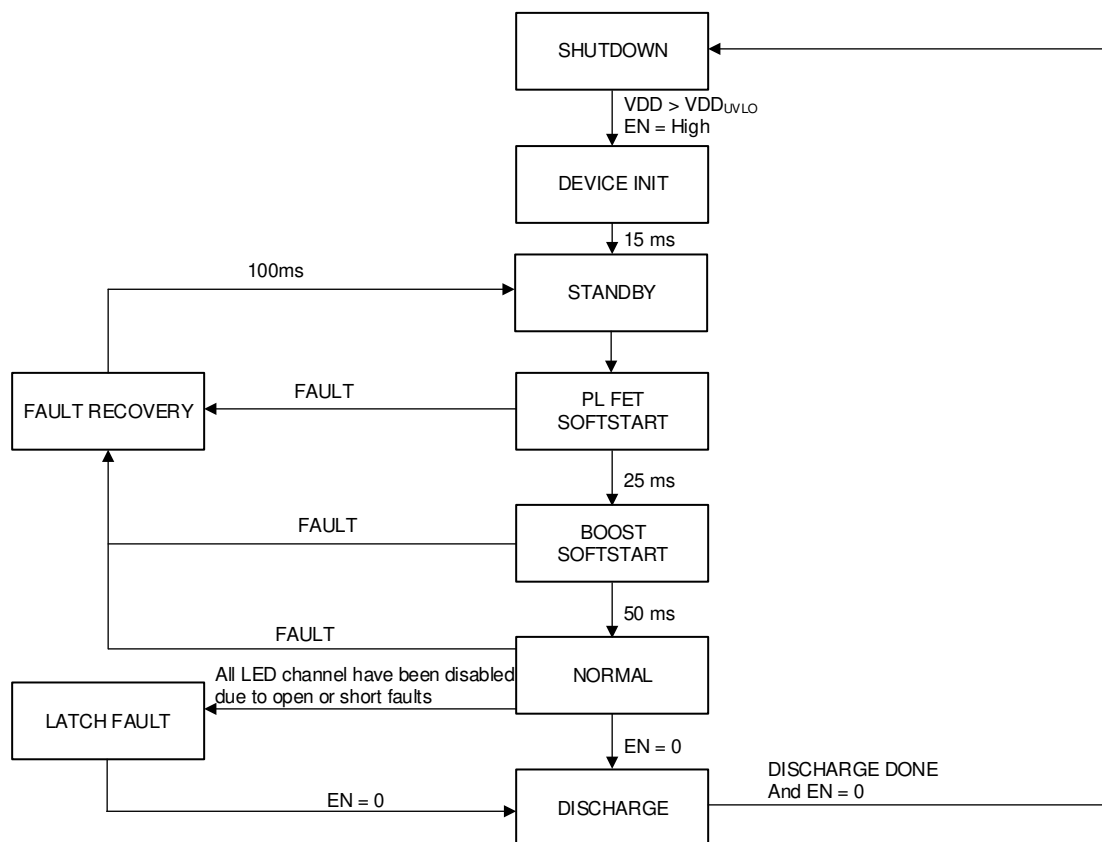


图 7-19. State Machine Diagram

### 7.4.2 Shutdown

When EN is pulled low, boost, power-line FET, and LED outputs are turned off, and the device tries to discharge the boost output for 400 ms. After this, the device is totally turned off.

### 7.4.3 Device Initialization

After POR is released device initialization begins. During this state the LDO is started up, EEPROM default and trim configurations are loaded, LEDSET, MODE, BOOST\_FSET and PWM\_FSET resistors are detected.

### 7.4.4 Standby Mode

Starting from Standby mode, the device can be accessed with I2C to change any configuration registers.

Standby Mode is immediately switched to Power-line FET Soft Start mode if there's no fault.

### 7.4.5 Power-line FET Soft Start

Power-line FET is gradually enabled during this 25-ms long state. Boost input and output capacitors are charged to  $V_{IN}$  level.  $V_{IN}$  faults for OCP, OVP, and UVP and fault for LED short to GND are enabled.

### 7.4.6 Boost Start-Up

Boost voltage is ramped to initial boost voltage level with reduced current limit for 50 ms. All boost faults are now enabled.

### 7.4.7 Normal Mode

LED drivers are enabled when brightness is greater than zero. All LED faults are active.

## 7.4.8 Fault Recovery

Some critical faults can trigger fault recover state. LED drivers, boost converter, and power-line FET are disabled for 100 ms, and the device attempts to restart from standby mode if EN is still high and brightness is greater than zero.

## 7.4.9 Latch Fault

If all LED strings are disabled due to faults then the LP8866S-Q1 enters the latch fault mode. This state can be exited only by pulling the EN pin low.

## 7.4.10 Start-Up Sequence

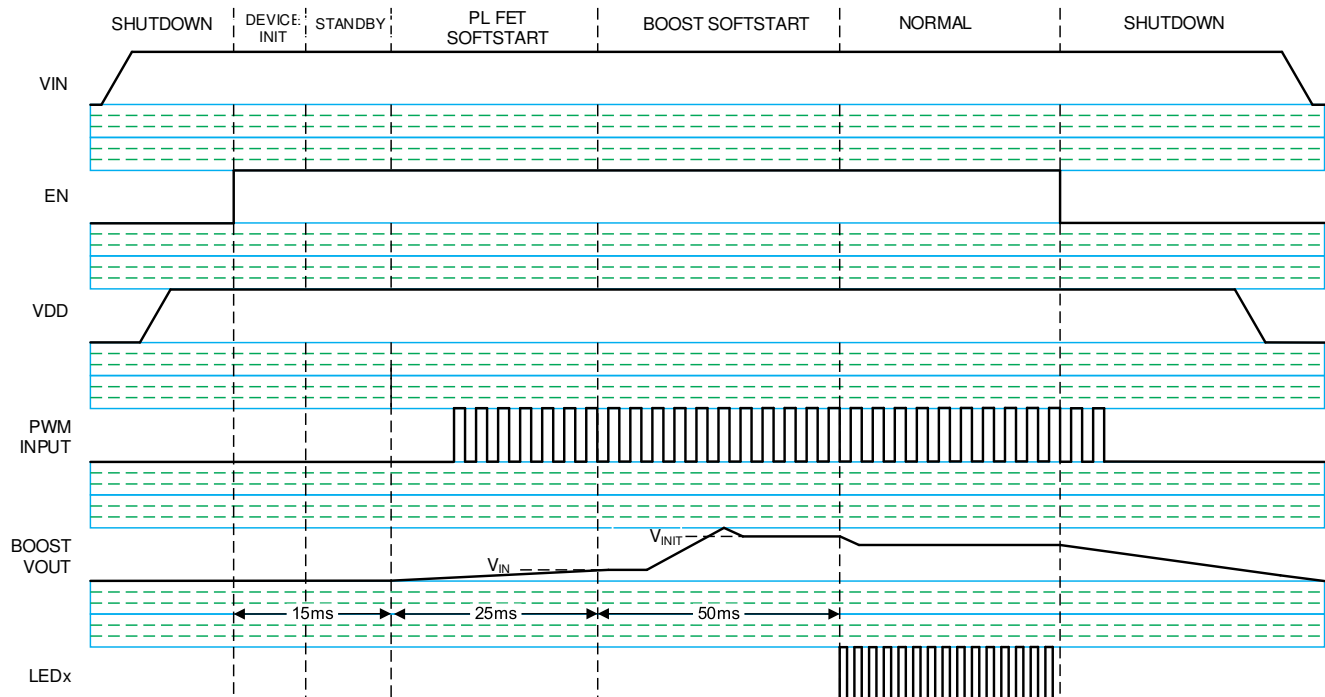


图 7-20. Start-Up Sequence Diagram

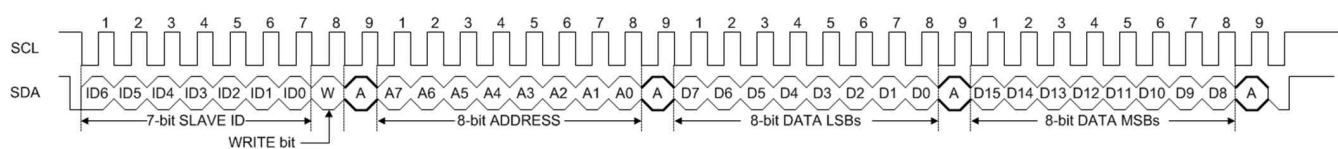
## 7.5 Programming

### 7.5.1 I2C-Compatible Interface

The LP8866S-Q1 device supports I2C interface to access and change the configuration. The 7-bit base slave address is 0x2A or 0x2B. The address could be configured through the resistor settings of MODE pin.

Write I2C transactions are made up of 4 bytes. The first byte includes the 7-bit slave address and Write bit. The 7-bit slave address selects the LP8866S-Q1 slave device. The second byte is eight bits register address. The last two bytes are the 16-bit register value.

Read I2C transactions are made up of 5 bytes. The first byte includes the 7-bit slave address and Write bit. The 7-bit slave address selects the LP8866S-Q1 slave device. The second byte is eight bits register address. The third byte includes the 7-bit slave address and Read bit. The last two bytes are the 16-bit register value returned from the slave.

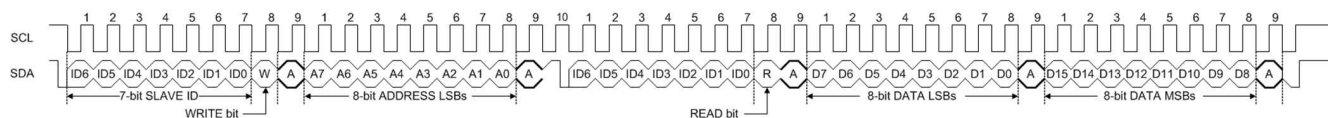


where



- W bit = 1

7-21. I2C Write



where

- R bit = 0
- W bit = 1

7-22. I2C Read

## 7.5.2 Programming Examples

### 7.5.2.1 General Configuration Registers

The LP8866S-Q1 does not require any serial interface configuration. It can be simply controlled with the EN pin and PWM pin. Most of the device configuration is accomplished using external resistor values. If I2C interface is available then extended configuration is possible. The configuration registers can be written from standby state to normal state as shown in 表 7-10.

**表 7-10. Configuration Registers**

| REGISTER NAME    | FUNCTION   |
|------------------|--|
| ADV_SLOPE_ENABLE | Enables advance sloper S-shape smoothing function.                                   |
| DITHER_SELECT    | Selects up to 3 bits of PWM dither for added dimming resolution.                     |
| SLOPE_SELECT     | Selects duration for linear brightness sloper.                                       |
| BRT_MODE         | Selects PWM pin or DISPLAY_BRT register for brightness control.                      |
| SPREAD_RANGE     | Selects up to 2 bits boost switching frequency spread spectrum range.                |
| SPREAD_MOD_FREQ  | Selects up to 2 bits boost switching frequency spread spectrum modulation frequency. |
| SPREAD_PSEUDO_EN | Enables pseudo random modulation for boost switching spread spectrum frequency.      |

### 7.5.2.2 Clearing Fault Interrupts

The LP8866S-Q1 has an INT pin to alert the host when a fault occurs. If I2C interface is available, the Interrupt Fault Status registers can be read back to learn which fault(s) have been detected. These status bits are located in the SUPPLY\_STATUS, BOOST\_STATUS and LED\_STATUS registers. Each interrupt status has a STATUS bit and a CLEAR bit. To clear a fault interrupt status a 1 must be written to both the STATUS bit and CLEAR bit at the same time.

### 7.5.2.3 Disabling Fault Interrupts

By default, most of the LP8866S-Q1 faults trigger the INT pin. Each fault has two INT\_EN bits. These bits are located in the SUPPLY\_INT\_EN, BOOST\_INT\_EN, and LED\_INT\_EN registers. If the INT\_EN bit is read and returns 2b'10, the INT pin is triggered when that fault occurs. The fault interrupt can be disabled by writing 2b'01 to its INT\_EN bits, or it can be enabled by writing 2b'11 to its INT\_EN bits. There is also a GLOBAL fault interrupt that can be disabled to prevent any faults from triggering the INT pin.

### 7.5.2.4 Diagnostic Registers

The LP8866S-Q1 contains several diagnostic registers than can be read with the serial interface for debugging or additional device information. 表 7-11 is a summary of the available registers.

**表 7-11. Diagnostic Registers**

| REGISTER NAME      | FUNCTION  |
|--------------------|---|
| FSM_LIVE_STATUS    | Current state of the functional state machine   |
| PWM_INPUT_STATUS   | Measured 16-bit duty cycle of the PWM pin input   |
| LED_PWM_STATUS     | 16-bit LED PWM duty cycle from state machine  |
| LED_CURRENT_STATUS | 12-bit LED current DAC value from state machine   |
| VBOOST_STATUS      | 10-bit value for adaptive boost voltage target — value is linear between VBOOST_MIN and VBOOST_MAX calculations |
| MODE_SEL_CFG       | Dimming mode configuration from MODE detection  |
| LED_STRING_CFG     | LED string phase configuration from LEDSET detection  |
| BOOST_FREQ_SEL     | Boost switching frequency value from BST_FSET detection   |
| PWM_FREQ_SEL       | LED PWM frequency value from PWM_FSET detection   |

## 7.6 Register Maps

### 7.6.1 FullMap Registers

表 7-12 lists the memory-mapped registers for the FullMap registers. All register offset addresses not listed in 表 7-12 should be considered as reserved locations and the register contents should not be modified.

**表 7-12. FULLMAP Registers**

| Offset | Acronym                 | Register Name              | Section            |
|--------|-------------------------|----------------------------|--------------------|
| 00h    | BRT_CONTROL             | Display Brightness         | <a href="#">Go</a> |
| 02h    | LED_CURR_CONFIG         | LED Current                | <a href="#">Go</a> |
| 04h    | USER_CONFIG1            | User Config 1              | <a href="#">Go</a> |
| 06h    | USER_CONFIG2            | User Config 2              | <a href="#">Go</a> |
| 08h    | SUPPLY_INT_EN           | Supply Interrupt Enable    | <a href="#">Go</a> |
| 0Ah    | BOOST_INT_EN            | Boost Interrupt Enable     | <a href="#">Go</a> |
| 0Ch    | LED_INT_EN              | LED Interrupt Enable       | <a href="#">Go</a> |
| 0Eh    | SUPPLY_STATUS           | Supply Fault Status        | <a href="#">Go</a> |
| 10h    | BOOST_STATUS            | Boost Fault Status         | <a href="#">Go</a> |
| 12h    | LED_STATUS              | LED Fault Status           | <a href="#">Go</a> |
| 14h    | FSM_DIAGNOSTICS         | Device State Diagnostics   | <a href="#">Go</a> |
| 16h    | PWM_INPUT_DIAGNOSTICS   | PWM Input Diagnostics      | <a href="#">Go</a> |
| 18h    | PWM_OUTPUT_DIAGNOSTICS  | PWM Output Diagnostics     | <a href="#">Go</a> |
| 1Ah    | LED_CURR_DIAGNOSTICS    | LED Current Diagnostics    | <a href="#">Go</a> |
| 1Ch    | ADAPT_BOOST_DIAGNOSTICS | Adaptive Boost Diagnostics | <a href="#">Go</a> |
| 1Eh    | AUTO_DETECT_DIAGNOSTICS | Auto Detect Diagnostics    | <a href="#">Go</a> |

Complex bit access types are encoded to fit into small table cells. 表 7-13 shows the codes that are used for access types in this section.

**表 7-13. FullMap Access Type Codes**

| Access Type            | Code | Description                            |
|------------------------|------|--|
| Read Type              |      |  |
| R                      | R    | Read                                   |
| Write Type             |      |  |
| W                      | W    | Write                                  |
| Reset or Default Value |      |  |
| –n                     |      | Value after reset or the default value |

#### 7.6.1.1 BRT\_CONTROL Register (Offset = 00h) [reset = 0h]

BRT\_CONTROL is shown in 图 7-23 and described in 表 7-14.

Return to [Summary Table](#).

**图 7-23. BRT\_CONTROL Register**

|             |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|-------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15          | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| DISPLAY_BRT |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R/W-0h      |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**表 7-14. BRT\_CONTROL Register Field Descriptions**

| Bit  | Field       | Type | Reset | Description                 |
|------|-------------|------|-------|-----------------------------|
| 15-0 | DISPLAY_BRT | R/W  | 0h    | Display Brightness Register |

**7.6.1.2 LED\_CURR\_CONFIG Register (Offset = 02h) [reset = 0FFFh]**

LED\_CURR\_CONFIG is shown in [図 7-24](#) and described in [表 7-15](#).

Return to [Summary Table](#).

**図 7-24. LED\_CURR\_CONFIG Register**

|          |    |    |    |             |    |   |   |   |   |   |   |   |   |   |   |
|----------|----|----|----|-------------|----|---|---|---|---|---|---|---|---|---|---|
| 15       | 14 | 13 | 12 | 11          | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| RESERVED |    |    |    | LED_CURRENT |    |   |   |   |   |   |   |   |   |   |   |
| R/W-0h   |    |    |    | R/W-FFFh    |    |   |   |   |   |   |   |   |   |   |   |

**表 7-15. LED\_CURR\_CONFIG Register Field Descriptions**

| Bit   | Field       | Type | Reset | Description                             |
|-------|-------------|------|-------|---|
| 15-12 | RESERVED    | R/W  | 0h    | These bits are reserved.                |
| 11-0  | LED_CURRENT | R/W  | FFFh  | LED current control for all LED outputs |

**7.6.1.3 USER\_CONFIG1 Register (Offset = 04h) [reset = 8A3h]**

USER\_CONFIG1 is shown in [図 7-25](#) and described in [表 7-16](#).

Return to [Summary Table](#).

**図 7-25. GROUPING1 Register**

|              |                  |                 |               |                  |          |   |   |
|--------------|------------------|-----------------|---------------|------------------|----------|---|---|
| 15           | 14               | 13              | 12            | 11               | 10       | 9 | 8 |
| RESERVED     | SPREAD_PSEUDO_EN | SPREAD_MOD_FREQ | SPREAD_RANGE  | BRT_MODE         |          |   |   |
| R/W-0h       | R/W-0h           | R/W-0h          | R/W-2h        | R/W-0h           |          |   |   |
| 7            | 6                | 5               | 4             | 3                | 2        | 1 | 0 |
| SLOPE_SELECT |                  |                 | DITHER_SELECT | ADV_SLOPE_ENABLE | RESERVED |   |   |
| R/W-5h       |                  |                 | R/W-0h        | R/W-1h           | R/W-1h   |   |   |

**表 7-16. USER\_CONFIG1 Register Field Descriptions**

| Bit   | Field            | Type | Reset | Description   |
|-------|------------------|------|-------|---|
| 15    | RESERVED         | R/W  | 0h    | This bit is reserved.   |
| 14    | SPREAD_PSEUDO_EN | R/W  | 0h    | 0h = Pseudo Random SS disabled<br>1h = Pseudo Random SS enabled   |
| 13-12 | SPREAD_MOD_FREQ  | R/W  | 0h    | Boost spread spectrum modulation frequency<br>0h = 200 Hz<br>1h = 500 Hz<br>2h = 800 Hz<br>3h = 1.2 kHz |
| 11-10 | SPREAD_RANGE     | R/W  | 2h    | OSC_BST spread spectrum range<br>0h = 3.3%<br>1h = 4.3%<br>2h = 5.3%<br>3h = 7.2%                       |

**表 7-16. USER\_CONFIG1 Register Field Descriptions (continued)**

| Bit | Field            | Type | Reset | Description   |
|-----|------------------|------|-------|---|
| 9-8 | BRT_MODE         | R/W  | 0h    | Select PWM pin or DISPLAY_BRT register for brightness controll<br>0h = Brightness controlled by PWM input<br>1h = Reserved<br>2h = Brightness controlled by DISPLAY_BRT register<br>3h = Reserved   |
| 7-5 | SLOPE_SELECT     | R/W  | 5h    | Select duration for linear brightness sloper<br>0h = Disabled<br>1h = 1 ms<br>2h = 2 ms<br>3h = 50 ms<br>4h = 100 ms<br>5h = 200 ms<br>6h = 300 ms<br>7h = 500 ms<br>Times are for linear slope mode. Advanced sloper will increase durations while adding additional smoothing to brightness transitions. 1 ms and 2 ms sloper times are intended to be used only in linear mode. 50 ms to 500 ms sloper durations may be used with or without advanced sloper function. |
| 4-2 | DITHER_SELECT    | R/W  | 0h    | Dither mode select<br>0h = Dither Disabled<br>1h = 1-bit Dither<br>2h = 2-bit Dither<br>3h = 3-bit Dither<br>4h = 4-bit Dither  |
| 1   | ADV_SLOPE_ENABLE | R/W  | 1h    | 0h = Linear Sloping<br>1h = Advanced Sloping  |
| 0   | RESERVED         | R/W  | 1h    | This bit is reserved.   |

#### 7.6.1.4 USER\_CONFIG2 Register (Offset = 06h) [reset = 100h]

USER\_CONFIG2 is shown in [図 7-26](#) and described in [表 7-17](#).

Return to [Summary Table](#).

**図 7-26. USER\_CONFIG2 Register**

|          |                    |                    |                    |                    |                    |                    |                   |
|----------|--------------------|--------------------|--------------------|--------------------|--------------------|--------------------|-------------------|
| 15       | 14                 | 13                 | 12                 | 11                 | 10                 | 9                  | 8                 |
| RESERVED |                    |                    |                    |                    |                    |                    | EN_LED_GND_DETECT |
| R/W-0h   |                    |                    |                    |                    |                    |                    | R/W-1h            |
| 7        | 6                  | 5                  | 4                  | 3                  | 2                  | 1                  | 0                 |
| RESERVED | LED6_SHORT_DISABLE | LED5_SHORT_DISABLE | LED4_SHORT_DISABLE | LED3_SHORT_DISABLE | LED2_SHORT_DISABLE | LED1_SHORT_DISABLE |                   |
| R/W-0h   | R/W-0h             | R/W-0h             | R/W-0h             | R/W-0h             | R/W-0h             | R/W-0h             | R/W-0h            |

**表 7-17. USER\_CONFIG2 Register Field Descriptions**

| Bit  | Field    | Type | Reset | Description              |
|------|----------|------|-------|--------------------------|
| 15-9 | RESERVED | R/W  | 0h    | These bits are reserved. |

**表 7-17. USER\_CONFIG2 Register Field Descriptions (continued)**

| Bit | Field              | Type | Reset | Description  |
|-----|--------------------|------|-------|--|
| 8   | EN_LED_GND_DETECT  | R/W  | 1h    | Enable LED short to ground detection during Boost_SS and normal stage<br>0h = Disable<br>1h = Enable |
| 7-6 | RESERVED           | R/W  | 0h    | These bits must write 0 for normal operation.  |
| 5   | LED6_SHORT_DISABLE | R/W  | 0h    | Disable LED string6 internal short fault.<br>0h = Enable<br>1h = Disable                             |
| 4   | LED5_SHORT_DISABLE | R/W  | 0h    | Disable LED string5 internal short fault.<br>0h = Enable<br>1h = Disable                             |
| 3   | LED4_SHORT_DISABLE | R/W  | 0h    | Disable LED string4 internal short fault.<br>0h = Enable<br>1h = Disable                             |
| 2   | LED3_SHORT_DISABLE | R/W  | 0h    | Disable LED string3 internal short fault.<br>0h = Enable<br>1h = Disable                             |
| 1   | LED2_SHORT_DISABLE | R/W  | 0h    | Disable LED string2 internal short fault.<br>0h = Enable<br>1h = Disable                             |
| 0   | LED1_SHORT_DISABLE | R/W  | 0h    | Disable LED string1 internal short fault.<br>0h = Enable<br>1h = Disable                             |

**7.6.1.5 SUPPLY\_INT\_EN Register (Offset = 08h) [reset = 2AAAh]**SUPPLY\_INT\_EN is shown in [图 7-27](#) and described in [表 7-18](#).Return to [Summary Table](#).**图 7-27. SUPPLY\_INT\_EN Register**

|               |    |                |    |               |    |                |   |
|---------------|----|----------------|----|---------------|----|----------------|---|
| 15            | 14 | 13             | 12 | 11            | 10 | 9              | 8 |
| RESERVED      |    | BSTSYNC_INT_EN |    | CP_INT_EN     |    | CPCAP_INT_EN   |   |
| R/W-0h        |    | R/W-2h         |    | R/W-2h        |    | R/W-2h         |   |
| 7             | 6  | 5              | 4  | 3             | 2  | 1              | 0 |
| VINOCP_INT_EN |    | VDDUVLO_INT_EN |    | VINOVP_INT_EN |    | VINUVLO_INT_EN |   |
| R/W-2h        |    | R/W-2h         |    | R/W-2h        |    | R/W-2h         |   |

**表 7-18. SUPPLY\_INT\_EN Register Field Descriptions**

| Bit   | Field          | Type | Reset | Description  |
|-------|----------------|------|-------|--|
| 15-14 | RESERVED       | R/W  | 0h    | These bits are reserved.   |
| 13-12 | BSTSYNC_INT_EN | R/W  | 2h    | Missing boost sync interrupt enable<br>Read:<br>0h = Interrupt is currently disabled<br>2h = Interrupt is currently enabled<br>Write:<br>1h = Disable interrupt<br>3h = Enable interrupt |

**表 7-18. SUPPLY\_INT\_EN Register Field Descriptions (continued)**

| Bit   | Field           | Type | Reset | Description   |
|-------|-----------------|------|-------|---|
| 11-10 | CP_INT_EN       | R/W  | 2h    | Charge pump interrupt enable<br>Read:<br>0h = Interrupt is currently disabled<br>2h = Interrupt is currently enabled<br>Write:<br>1h = Disable interrupt<br>3h = Enable interrupt                   |
| 9-8   | CPCAP_INT_EN    | R/W  | 2h    | Charge pump cap missing interrupt enable<br>Read:<br>0h = Interrupt is currently disabled<br>2h = Interrupt is currently enabled<br>Write:<br>1h = Disable interrupt<br>3h = Enable interrupt       |
| 7-6   | VINOC_P_INT_EN  | R/W  | 2h    | V <sub>IN</sub> over-current interrupt enable<br>Read:<br>0h = Interrupt is currently disabled<br>2h = Interrupt is currently enabled<br>Write:<br>1h = Disable interrupt<br>3h = Enable interrupt  |
| 5-4   | VDDUVLO_INT_EN  | R/W  | 2h    | V <sub>DD</sub> under-voltage interrupt enable<br>Read:<br>0h = Interrupt is currently disabled<br>2h = Interrupt is currently enabled<br>Write:<br>1h = Disable interrupt<br>3h = Enable interrupt |
| 3-2   | VINOVP_INT_EN   | R/W  | 2h    | V <sub>IN</sub> over-voltage interrupt enable<br>Read:<br>0h = Interrupt is currently disabled<br>2h = Interrupt is currently enabled<br>Write:<br>1h = Disable interrupt<br>3h = Enable interrupt  |
| 1-0   | VINUUVLO_INT_EN | R/W  | 2h    | V <sub>IN</sub> under-voltage interrupt enable<br>Read:<br>0h = Interrupt is currently disabled<br>2h = Interrupt is currently enabled<br>Write:<br>1h = Disable interrupt<br>3h = Enable interrupt |

#### 7.6.1.6 BOOST\_INT\_EN Register (Offset = 0Ah) [reset = A028h]

BOOST\_INT\_EN is shown in [図 7-28](#) and described in [表 7-19](#).

Return to [Summary Table](#).

**図 7-28. BOOST\_INT\_EN Register**

|    |    |    |    |    |    |   |   |
|----|----|----|----|----|----|---|---|
| 15 | 14 | 13 | 12 | 11 | 10 | 9 | 8 |
|----|----|----|----|----|----|---|---|

 **7-28. BOOST\_INT\_EN Register (continued)**

|             |               |                |             |
|-------------|---------------|----------------|-------------|
| TSD_INT_EN  | ISSET_INT_EN  | LEDSET_INT_EN  | MODE_INT_EN |
| R/W-2h      | R/W-2h        | R/W-2h         | R/W-2h      |
| 7           | 6             | 5              | 4           |
| 3           | 2             | 1              | 0           |
| FSET_INT_EN | BSTOCP_INT_EN | BSTOVPH_INT_EN | Reserved    |
| R/W-2h      | R/W-2h        | R/W-2h         | R/W-0h      |

**表 7-19. BOOST\_INT\_EN Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description  |
|-------|---------------|------|-------|--|
| 15-14 | TSD_INT_EN    | R/W  | 2h    | Thermal shutdown interrupt enable<br>Read:<br>0h = Interrupt is currently disabled<br>2h = Interrupt is currently enabled<br>Write:<br>1h = Disable interrupt<br>3h = Enable interrupt               |
| 13-12 | ISSET_INT_EN  | R/W  | 2h    | ISSET resistor short to ground interrupt enable<br>Read:<br>0h = Interrupt is currently disabled<br>2h = Interrupt is currently enabled<br>Write:<br>1h = Disable interrupt<br>3h = Enable interrupt |
| 11-10 | LEDSET_INT_EN | R/W  | 0h    | Missing LEDSET resistor interrupt enable<br>Read:<br>0h = Interrupt is currently disabled<br>2h = Interrupt is currently enabled<br>Write:<br>1h = Disable interrupt<br>3h = Enable interrupt        |
| 9-8   | MODE_INT_EN   | R/W  | 0h    | Missing MODE resistor interrupt enable<br>Read:<br>0h = Interrupt is currently disabled<br>2h = Interrupt is currently enabled<br>Write:<br>1h = Disable interrupt<br>3h = Enable interrupt          |
| 7-6   | FSET_INT_EN   | R/W  | 0h    | Missing FSET resistor interrupt enable<br>Read:<br>0h = Interrupt is currently disabled<br>2h = Interrupt is currently enabled<br>Write:<br>1h = Disable interrupt<br>3h = Enable interrupt          |
| 5-4   | BSTOCP_INT_EN | R/W  | 2h    | Boost over-current interrupt enable<br>Read:<br>0h = Interrupt is currently disabled<br>2h = Interrupt is currently enabled<br>Write:<br>1h = Disable interrupt<br>3h = Enable interrupt             |



**表 7-19. BOOST\_INT\_EN Register Field Descriptions (continued)**

| Bit | Field          | Type | Reset | Description   |
|-----|----------------|------|-------|---|
| 3-2 | BSTOVPH_INT_EN | R/W  | 2h    | Boost over-voltage high interrupt enable<br>Read:<br>0h = Interrupt is currently disabled<br>2h = Interrupt is currently enabled<br>Write:<br>1h = Disable interrupt<br>3h = Enable interrupt |
| 1-0 | Reserved       | R/W  | 0h    | These bits are reserved.  |

#### 7.6.1.7 LED\_INT\_EN Register (Offset = 0Ch) [reset = AAh]

LED\_INT\_EN is shown in [図 7-29](#) and described in [表 7-20](#).

Return to [Summary Table](#).

**図 7-29. LED\_INT\_EN Register**

|               |    |                  |    |                  |    |                |   |
|---------------|----|------------------|----|------------------|----|----------------|---|
| 15            | 14 | 13               | 12 | 11               | 10 | 9              | 8 |
| RESERVED      |    |                  |    |                  |    |                |   |
| R/W-0h        |    |                  |    |                  |    |                |   |
| 7             | 6  | 5                | 4  | 3                | 2  | 1              | 0 |
| GLOBAL_INT_EN |    | I2C_ERROR_INT_EN |    | INVSTRING_INT_EN |    | VINUVVP_INT_EN |   |
| R/W-2h        |    | R/W-2h           |    | R/W-2h           |    | R/W-2h         |   |

**表 7-20. LED\_INT\_EN Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description  |
|------|------------------|------|-------|--|
| 15-8 | RESERVED         | R/W  | 0h    | These bits are reserved.   |
| 7-6  | GLOBAL_INT_EN    | R/W  | 2h    | Global interrupt enable<br>Read:<br>0h = Interrupt is currently disabled<br>2h = Interrupt is currently enabled<br>Write:<br>1h = Disable interrupt<br>3h = Enable interrupt                           |
| 5-4  | I2C_ERROR_INT_EN | R/W  | 2h    | I2C time out interrupt enable<br>Read:<br>0h = Interrupt is currently disabled<br>2h = Interrupt is currently enabled<br>Write:<br>1h = Disable interrupt<br>3h = Enable interrupt                     |
| 3-2  | INVSTRING_INT_EN | R/W  | 2h    | Invalid LED string configuration interrupt enable<br>Read:<br>0h = Interrupt is currently disabled<br>2h = Interrupt is currently enabled<br>Write:<br>1h = Disable interrupt<br>3h = Enable interrupt |

表 7-20. LED\_INT\_EN Register Field Descriptions (continued)

| Bit | Field      | Type | Reset | Description  |
|-----|------------|------|-------|--|
| 1-0 | LED_INT_EN | R/W  | 2h    | LED open/internal short/short to GND interrupt enable<br>Read:<br>0h = Interrupt is currently disabled<br>2h = Interrupt is currently enabled<br>Write:<br>1h = Disable interrupt<br>3h = Enable interrupt |

## 7.6.1.8 SUPPLY\_STATUS Register (Offset = 0Eh) [reset = 0h]

SUPPLY\_STATUS is shown in 图 7-30 and described in 表 7-21.

Return to [Summary Table](#).

图 7-30. SUPPLY\_STATUS Register

|                    |                   |                    |                   |                   |                  |                     |                    |
|--------------------|-------------------|--------------------|-------------------|-------------------|------------------|---------------------|--------------------|
| 15                 | 14                | 13                 | 12                | 11                | 10               | 9                   | 8                  |
| CRCERR_STAT<br>US  | CRCERR_CLE<br>AR  | BSTSYNC_STA<br>TUS | BSTSYNC_CLE<br>AR | CP_STATUS         | CP_CLEAR         | CPCAP_STATU<br>S    | CPCAP_CLEA<br>R    |
| R/W-0h             | R/W-0h            | R/W-0h             | R/W-0h            | R/W-0h            | R/W-0h           | R/W-0h              | R/W-0h             |
| 7                  | 6                 | 5                  | 4                 | 3                 | 2                | 1                   | 0                  |
| VINOC_P_STAT<br>US | VINOC_P_CLEA<br>R | VDDUVLO_ST<br>ATUS | VDDUVLO_CL<br>EAR | VINOVP_STAT<br>US | VINOVP_CLEA<br>R | VINU_VLO_STA<br>TUS | VINU_VLO_CLE<br>AR |
| R/W-0h             | R/W-0h            | R/W-0h             | R/W-0h            | R/W-0h            | R/W-0h           | R/W-0h              | R/W-0h             |

表 7-21. SUPPLY\_STATUS Register Field Descriptions

| Bit | Field          | Type | Reset | Description   |
|-----|----------------|------|-------|---|
| 15  | CRCERR_STATUS  | R/W  | 0h    | CRC error fault status<br>0h = No fault<br>1h = Fault   |
| 14  | CRCERR_CLEAR   | R/W  | 0h    | CRC error fault clear<br>Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status          |
| 13  | BSTSYNC_STATUS | R/W  | 0h    | Missing boost sync fault status<br>0h = No fault<br>1h = Fault  |
| 12  | BSTSYNC_CLEAR  | R/W  | 0h    | Missing boost sync fault clear<br>Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status |
| 11  | CP_STATUS      | R/W  | 0h    | Charge pump fault status<br>0h = No fault<br>1h = Fault   |
| 10  | CP_CLEAR       | R/W  | 0h    | Charge pump fault clear<br>Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status        |
| 9   | CPCAP_STATUS   | R/W  | 0h    | Missing charge pump fault status<br>0h = No fault<br>1h = Fault   |

**表 7-21. SUPPLY\_STATUS Register Field Descriptions (continued)**

| Bit | Field          | Type | Reset | Description  |
|-----|----------------|------|-------|--|
| 8   | CPCAP_CLEAR    | R/W  | 0h    | Missing charge pump fault clear<br>Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status           |
| 7   | VINOCP_STATUS  | R/W  | 0h    | V <sub>IN</sub> over-current fault status<br>0h = No fault<br>1h = Fault   |
| 6   | VINOCP_CLEAR   | R/W  | 0h    | V <sub>IN</sub> over-current fault clear<br>Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status  |
| 5   | VDDUVLO_STATUS | R/W  | 0h    | V <sub>DD</sub> under-voltage fault status<br>0h = No fault<br>1h = Fault  |
| 4   | VDDUVLO_CLEAR  | R/W  | 0h    | V <sub>DD</sub> under-voltage fault clear<br>Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status |
| 3   | VINOVP_STATUS  | R/W  | 0h    | V <sub>IN</sub> over-voltage fault status<br>0h = No fault<br>1h = Fault   |
| 2   | VINOVP_CLEAR   | R/W  | 0h    | V <sub>IN</sub> over-voltage fault clear<br>Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status  |
| 1   | VINUVLO_STATUS | R/W  | 0h    | V <sub>IN</sub> under-voltage fault status<br>0h = No fault<br>1h = Fault  |
| 0   | VINUVLO_CLEAR  | R/W  | 0h    | V <sub>IN</sub> under-voltage fault clear<br>Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status |

#### 7.6.1.9 BOOST\_STATUS Register (Offset = 10h) [reset = 0h]

BOOST\_STATUS is shown in [图 7-31](#) and described in [表 7-22](#).

Return to [Summary Table](#).

**图 7-31. BOOST\_STATUS Register**

|             |            |                   |                  |                    |                   |                    |                   |
|-------------|------------|-------------------|------------------|--------------------|-------------------|--------------------|-------------------|
| 15          | 14         | 13                | 12               | 11                 | 10                | 9                  | 8                 |
| TSD_STATUS  | TSD_CLEAR  | ISSET_STATUS      | ISSET_CLEAR      | LEDSET_STAT<br>US  | LEDSET_CLEA<br>R  | MODESEL_ST<br>ATUS | MODESEL_CL<br>EAR |
| R/W-0h      | R/W-0h     | R/W-0h            | R/W-0h           | R/W-0h             | R/W-0h            | R/W-0h             | R/W-0h            |
| 7           | 6          | 5                 | 4                | 3                  | 2                 | 1                  | 0                 |
| FSET_STATUS | FSET_CLEAR | BSTOCP_STAT<br>US | BSTOCP_CLE<br>AR | BSTOVPH_STA<br>TUS | BSTOVPH_CL<br>EAR | BSTOVPL_STA<br>TUS | BSTOVPL_CLE<br>AR |
| R/W-0h      | R/W-0h     | R/W-0h            | R/W-0h           | R/W-0h             | R/W-0h            | R/W-0h             | R/W-0h            |

**表 7-22. BOOST\_STATUS Register Field Descriptions**

| Bit | Field      | Type | Reset | Description  |
|-----|------------|------|-------|--|
| 15  | TSD_STATUS | R/W  | 0h    | Thermal shutdown fault status<br>0h = No fault<br>1h = Fault |

**表 7-22. BOOST\_STATUS Register Field Descriptions (continued)**

| Bit | Field          | Type | Reset | Description  |
|-----|----------------|------|-------|--|
| 14  | TSD_CLEAR      | R/W  | 0h    | Thermal shutdown fault clear<br>Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status              |
| 13  | ISET_STATUS    | R/W  | 0h    | ISET resistor short to ground fault status<br>0h = No fault<br>1h = Fault  |
| 12  | ISET_CLEAR     | R/W  | 0h    | ISET resistor short to ground fault clear<br>Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status |
| 11  | LEDSET_STATUS  | R/W  | 0h    | Missing LED resistor fault status<br>0h = No fault<br>1h = Fault   |
| 10  | LEDSET_CLEAR   | R/W  | 0h    | Missing LED resistor fault clear<br>Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status          |
| 9   | MODESEL_STATUS | R/W  | 0h    | Missing MODE SEL resistor fault status<br>0h = No fault<br>1h = Fault  |
| 8   | MODESEL_CLEAR  | R/W  | 0h    | Missing MODE SEL resistor fault clear<br>Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status     |
| 7   | FSET_STATUS    | R/W  | 0h    | Missing boost FSET resistor fault status<br>0h = No fault<br>1h = Fault  |
| 6   | FSET_CLEAR     | R/W  | 0h    | Missing boost FSET resistor fault clear<br>Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status   |
| 5   | BSTOCP_STATUS  | R/W  | 0h    | Boost over-current fault status<br>0h = No fault<br>1h = Fault   |
| 4   | BSTOCP_CLEAR   | R/W  | 0h    | Boost over-current fault clear<br>Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status            |
| 3   | BSTOVPH_STATUS | R/W  | 0h    | Boost OVP high fault status<br>0h = No fault<br>1h = Fault   |
| 2   | BSTOVPH_CLEAR  | R/W  | 0h    | Boost OVP high fault clear<br>Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status                |
| 1   | BSTOVPL_STATUS | R/W  | 0h    | Boost OVP low fault status<br>0h = No fault<br>1h = Fault  |
| 0   | BSTOVPL_CLEAR  | R/W  | 0h    | Boost OVP low fault clear<br>Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status  |

### 7.6.1.10 LED\_STATUS Register (Offset = 12h) [reset = 0h]

LED\_STATUS is shown in [Figure 7-32](#) and described in [Table 7-23](#).

Return to [Summary Table](#).

**Figure 7-32. LED\_STATUS Register**

| 15        | 14                   | 13                  | 12                   | 11                  | 10         | 9          | 8          |
|-----------|----------------------|---------------------|----------------------|---------------------|------------|------------|------------|
| RESERVED  | I2C_ERROR_S<br>TATUS | I2C_ERROR_C<br>LEAR | INVSTRING_S<br>TATUS | INVSTRING_C<br>LEAR | LED_STATUS | LED_CLEAR  | GND_LED    |
| R/W-0h    | R/W-0h               | R/W-0h              | R/W-0h               | R/W-0h              | R/W-0h     | R/W-0h     | R-0h       |
| 7         | 6                    | 5                   | 4                    | 3                   | 2          | 1          | 0          |
| SHORT_LED | OPEN_LED             | LED6_FAULT          | LED5_FAULT           | LED4_FAULT          | LED3_FAULT | LED2_FAULT | LED1_FAULT |
| R-0h      | R-0h                 | R-0h                | R-0h                 | R-0h                | R-0h       | R-0h       | R-0h       |

**Table 7-23. LED\_STATUS Register Field Descriptions**

| Bit | Field            | Type | Reset | Description   |
|-----|------------------|------|-------|---|
| 15  | RESERVED         | R/W  | 0h    | This bit is reserved  |
| 14  | I2C_ERROR_STATUS | R/W  | 0h    | I2C time out fault status<br>0h = No fault<br>1h = Fault  |
| 13  | I2C_ERROR_CLEAR  | R/W  | 0h    | I2C time out fault clear<br>Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status                         |
| 12  | INVSTRING_STATUS | R/W  | 0h    | Invalid string configuration fault status<br>0h = No fault<br>1h = Fault  |
| 11  | INVSTRING_CLEAR  | R/W  | 0h    | Invalid string configuration fault clear<br>Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status         |
| 10  | LED_STATUS       | R/W  | 0h    | LED open/internal short/short to GND fault status<br>0h = No fault<br>1h = Fault  |
| 9   | LED_CLEAR        | R/W  | 0h    | LED open/internal short/short to GND fault clear<br>Write "1" to both Status bit and Clear bit at the same time to clear interrupt register status and interrupt pin status |
| 8   | GND_LED          | R    | 0h    | LED short to GND fault status<br>0h = No fault<br>1h = Fault  |
| 7   | SHORT_LED        | R    | 0h    | LED internal short Status<br>0h = No Fault<br>1h = Fault<br>Status is cleared with LED_STATUS bit   |
| 6   | OPEN_LED         | R    | 0h    | LED open fault status<br>0h = No fault<br>1h = Fault<br>Status is cleared with LED_STATUS bit   |
| 5   | LED6_FAULT       | R    | 0h    | LED 6 Status<br>0h = No Fault<br>1h = Fault   |

**表 7-23. LED\_STATUS Register Field Descriptions (continued)**

| Bit | Field      | Type | Reset | Description                                 |
|-----|------------|------|-------|---|
| 4   | LED5_FAULT | R    | 0h    | LED 5 Status<br>0h = No Fault<br>1h = Fault |
| 3   | LED4_FAULT | R    | 0h    | LED 4 Status<br>0h = No Fault<br>1h = Fault |
| 2   | LED3_FAULT | R    | 0h    | LED 3 Status<br>0h = No Fault<br>1h = Fault |
| 1   | LED2_FAULT | R    | 0h    | LED 2 Status<br>0h = No Fault<br>1h = Fault |
| 0   | LED1_FAULT | R    | 0h    | LED 1 Status<br>0h = No Fault<br>1h = Fault |

**7.6.1.11 FSM\_DIAGNOSTICS Register (Offset = 14h) [reset = 0h]**

FSM\_DIAGNOSTICS is shown in [図 7-33](#) and described in [表 7-24](#).

Return to [Summary Table](#).

**図 7-33. FSM\_DIAGNOSTICS Register**

|          |    |    |    |                 |    |   |   |
|----------|----|----|----|-----------------|----|---|---|
| 15       | 14 | 13 | 12 | 11              | 10 | 9 | 8 |
| RESERVED |    |    |    |                 |    |   |   |
| R-0h     |    |    |    |                 |    |   |   |
| 7        | 6  | 5  | 4  | 3               | 2  | 1 | 0 |
| RESERVED |    |    |    | FSM_LIVE_STATUS |    |   |   |
| R-0h     |    |    |    | R-0h            |    |   |   |

**表 7-24. FSM\_DIAGNOSTICS Register Field Descriptions**

| Bit  | Field           | Type | Reset | Description   |
|------|-----------------|------|-------|---|
| 15-5 | RESERVED        | R    | 0h    | These bits are reserved   |
| 4-0  | FSM_LIVE_STATUS | R    | 0h    | Current state of the functional state machine<br>0h = DISABLED<br>1h = LDO_STARTUP<br>2h = OTP_READ<br>3h = STANDBY<br>4h-Fh = BOOST_STARTUP<br>10h = NORMAL<br>11h = SHUTDOWN<br>12h = FAULT_RECOVERY<br>13h = ALL_LED_FAULT |

**7.6.1.12 PWM\_INPUT\_DIAGNOSTICS Register (Offset = 16h) [reset = 0h]**

PWM\_INPUT\_DIAGNOSTICS is shown in [図 7-34](#) and described in [表 7-25](#).

Return to [Summary Table](#).

**图 7-34. PWM\_INPUT\_DIAGNOSTICS Register**

|                  |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15               | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PWM_INPUT_STATUS |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h             |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**表 7-25. PWM\_INPUT\_DIAGNOSTICS Register Field Descriptions**

| Bit  | Field            | Type | Reset | Description   |
|------|------------------|------|-------|---|
| 15-0 | PWM_INPUT_STATUS | R    | 0h    | 16-bit value for detected duty cycle of PWM input signal. |

#### 7.6.1.13 PWM\_OUTPUT\_DIAGNOSTICS Register (Offset = 18h) [reset = 0h]

PWM\_OUTPUT\_DIAGNOSTICS is shown in 图 7-35 and described in 表 7-26.

Return to [Summary Table](#).

**图 7-35. PWM\_OUTPUT\_DIAGNOSTICS Register**

|                   |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
|-------------------|----|----|----|----|----|---|---|---|---|---|---|---|---|---|---|
| 15                | 14 | 13 | 12 | 11 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| PWM_OUTPUT_STATUS |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |
| R-0h              |    |    |    |    |    |   |   |   |   |   |   |   |   |   |   |

**表 7-26. PWM\_OUTPUT\_DIAGNOSTICS Register Field Descriptions**

| Bit  | Field             | Type | Reset | Description  |
|------|-------------------|------|-------|--|
| 15-0 | PWM_OUTPUT_STATUS | R    | 0h    | 16-bit value for configured duty cycle of PWM output signal. |

#### 7.6.1.14 LED\_CURR\_DIAGNOSTICS Register (Offset = 1Ah) [reset = 0h]

LED\_CURR\_DIAGNOSTICS is shown in 图 7-36 and described in 表 7-27.

Return to [Summary Table](#).

**图 7-36. LED\_CURR\_DIAGNOSTICS Register**

|                    |    |    |    |                    |    |   |   |
|--------------------|----|----|----|--------------------|----|---|---|
| 15                 | 14 | 13 | 12 | 11                 | 10 | 9 | 8 |
| RESERVED           |    |    |    | LED_CURRENT_STATUS |    |   |   |
| R-0h               |    |    |    | R-0h               |    |   |   |
| 7                  | 6  | 5  | 4  | 3                  | 2  | 1 | 0 |
| LED_CURRENT_STATUS |    |    |    |                    |    |   |   |
| R-0h               |    |    |    |                    |    |   |   |

**表 7-27. LED\_CURR\_DIAGNOSTICS Register Field Descriptions**

| Bit   | Field              | Type | Reset | Description   |
|-------|--------------------|------|-------|---|
| 15-12 | RESERVED           | R    | 0h    | These bits are reserved.  |
| 11-0  | LED_CURRENT_STATUS | R    | 0h    | 12-bit Current DAC Code that Brightness path is driving to OUT1-6 output. |

#### 7.6.1.15 ADAPT\_BOOST\_DIAGNOSTICS Register (Offset = 1Ch) [reset = 0h]

ADAPT\_BOOST\_DIAGNOSTICS is shown in 图 7-37 and described in 表 7-28.

Return to [Summary Table](#).

**图 7-37. ADAPT\_BOOST\_DIAGNOSTICS Register**

|          |    |    |    |    |    |               |   |
|----------|----|----|----|----|----|---------------|---|
| 15       | 14 | 13 | 12 | 11 | 10 | 9             | 8 |
| RESERVED |    |    |    |    |    | VBOOST_STATUS |   |
| R-0h     |    |    |    |    |    | R-0h          |   |

**图 7-37. ADAPT\_BOOST\_DIAGNOSTICS Register (continued)**

| 7             | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
|---------------|---|---|---|---|---|---|---|
| VBOOST_STATUS |   |   |   |   |   |   |   |
| R-0h          |   |   |   |   |   |   |   |

**表 7-28. ADAPT\_BOOST\_DIAGNOSTICS Register Field Descriptions**

| Bit   | Field         | Type | Reset | Description  |
|-------|---------------|------|-------|--|
| 15-11 | RESERVED      | R    | 0h    | These bits are reserved.   |
| 10-0  | VBOOST_STATUS | R    | 0h    | 11-bit Boost Voltage Code that Adaptive Voltage Control Loop sending to Analog Boost Block.<br>In two-resistor method, Boost Output Voltage = $((1+R1/R2)*1.21V) + (R1*18.9nA*VBOOST\_STATUS)$ |

**7.6.1.16 AUTO\_DETECT\_DIAGNOSTICS Register (Offset = 1Eh) [reset = 0h]**

AUTO\_DETECT\_DIAGNOSTICS is shown in 图 7-38 and described in 表 7-29.

Return to [Summary Table](#).

**图 7-38. AUTO\_DETECT\_DIAGNOSTICS Register**

| 15       | 14                | 13                  | 12 | 11 | 10       | 9                   | 8 |
|----------|-------------------|---------------------|----|----|----------|---------------------|---|
| RESERVED | AUTO_PWM_FREQ_SEL |                     |    |    | RESERVED | AUTO_LED_STRING_CFG |   |
| R-0h     | R-0h              |                     |    |    | R-0h     | R-0h                |   |
| 7        | 6                 | 5                   | 4  | 3  | 2        | 1                   | 0 |
| RESERVED |                   | AUTO_BOOST_FREQ_SEL |    |    |          | MODE_SEL            |   |
| R-0h     |                   | R-0h                |    |    |          | R-0h                |   |

**表 7-29. AUTO\_DETECT\_DIAGNOSTICS Register Field Descriptions**

| Bit   | Field               | Type | Reset | Description  |
|-------|---------------------|------|-------|--|
| 15    | RESERVED            | R    | 0h    | This bit is reserved   |
| 14-12 | AUTO_PWM_FREQ_SEL   | R    | 0h    | LED PWM frequency value from PWM_SEL resistor detection<br>0h = 152 Hz<br>1h = 305 Hz<br>2h = 610 Hz<br>3h = 1221 Hz<br>4h = 2441 Hz<br>5h = 4883 Hz<br>6h = 9766 Hz<br>7h = 19531 Hz  |
| 11    | RESERVED            | R    | 0h    | This bit is reserved   |
| 10-8  | AUTO_LED_STRING_CFG | R    | 0h    | LED string configuration from LED_SET resistor detection<br>0h = 6 separate strings<br>1h = 5 separate strings<br>2h = 4 separate strings<br>3h = 3 separate strings<br>4h = 2 separate strings<br>5h = 6 channel outputs connected in 3 groups to drive 3 strings<br>6h = 6 channel outputs connected in 2 groups to drive 2 strings<br>7h = 6 channel outputs connected together to drive 1 string |
| 7-6   | RESERVED            | R    | 0h    | These bits are reserved  |



**表 7-29. AUTO\_DETECT\_DIAGNOSTICS Register Field Descriptions (continued)**

| Bit | Field               | Type | Reset | Description  |
|-----|---------------------|------|-------|--|
| 5-3 | AUTO_BOOST_FREQ_SEL | R    | 0h    | Boost switching frequency value from PWM_FSET resistor detection<br>0h = 100 kHz<br>1h = 200 kHz<br>2h = 303 kHz<br>3h = 400 kHz<br>4h = 500 kHz<br>5h = 1818 kHz<br>6h = 2000 kHz<br>7h = 2222 kHz  |
| 2-0 | MODE_SEL            | R    | 0h    | LED dimming MODE value from MODE detection<br>0h = PWM mode, I2C address 0x2B<br>1h = 12.5% hybrid dimming mode, I2C address 0x2B<br>2h = Constant current mode, I2C address 0x2B<br>3h = Direct PWM, I2C address 0x2B<br>4h = PWM mode, I2C address 0x2A<br>5h = 12.5% hybrid dimming mode, I2C address 0x2A<br>6h = Constant current mode, I2C address 0x2A<br>7h = Direct PWM, I2C address 0x2A |

## 8 Application and Implementation

## Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

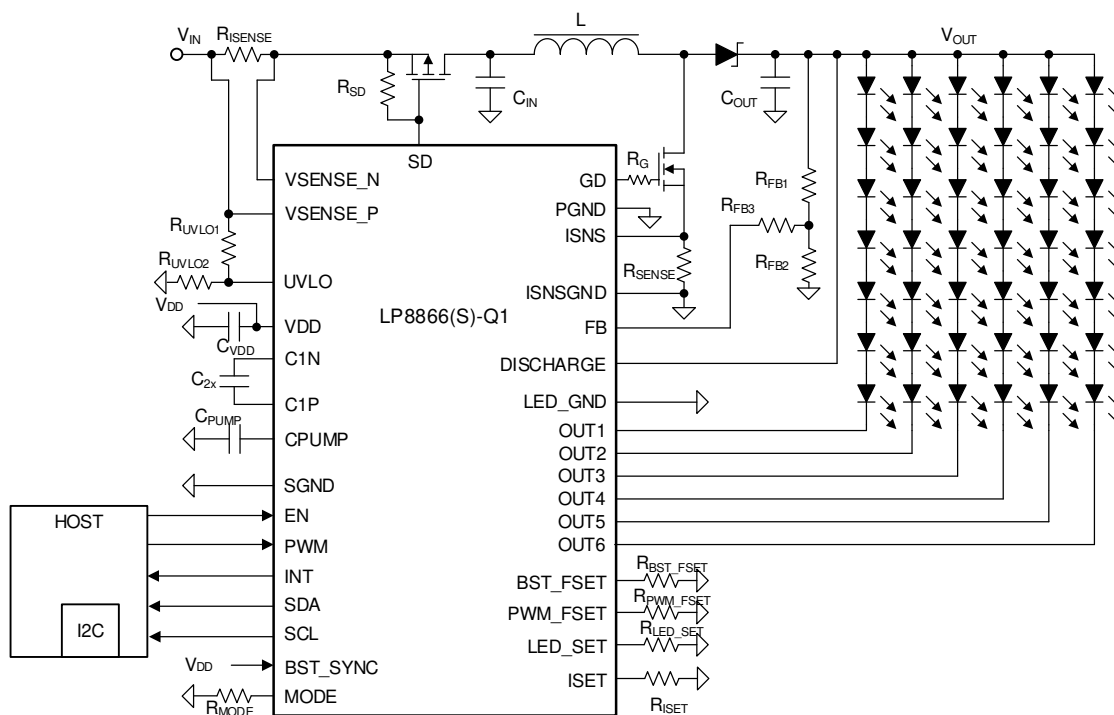
## 8.1 Application Information

The LP8866S-Q1 device is designed for automotive applications, and an input voltage  $V_{IN}$  is intended to be connected to the vehicle battery. Depending on the input voltage, the device may be used in either boost mode or SEPIC mode. The device is internally powered from the VDD pin, and voltage must be in 2.7-V to 5.5-V range. The device has flexible configurability through external components or by an I2C interface. If the VDD voltage is not high enough to drive an external nMOSFET gate, an internal charge pump must be used to power the gate driver (GD pin).

## 8.2 Typical Applications

### 8.2.1 Full Feature Application for Display Backlight

✎ 8-1 shows a full application for the LP8866S-Q1 device in a boost topology. It supports 6 LED strings in display mode, each at 150 mA, with an automatic 60° phase shift. Brightness control register is used for LED dimming method through I2C communication. The charge pump is enabled for a 400-kHz boost switching frequency with spread spectrum.



## ☒ 8-1. Full Feature Application for Display Backlight

### 8.2.1.1 Design Requirements

This typical LED-driver application is designed to meet the parameters listed in 表 8-1:

**表 8-1. LP8866S-Q1 Full-Feature Design Parameters**

| DESIGN PARAMETER          | VALUE   |
|---------------------------|---|
| VIN voltage range         | 5 V to 20 V (Quiescent Voltage)   |
| VDD voltage               | 3.3 V   |
| LED strings configuration | 6 strings, 7 LEDs in series   |
| Charge pump               | Enabled   |
| Brightness control        | I2C   |
| Output configuration      | OUT1 to OUT6 are in phase shift mode (60°)  |
| LED string current        | 150 mA  |
| Boost frequency           | 400 kHz   |
| Inductor                  | 22 µH at 6.5-A saturation current   |
| R <sub>ISENSE</sub>       | 20 mΩ   |
| Power-line FET            | Enabled   |
| R <sub>SENSE</sub>        | 30 mΩ   |
| Input/Output capacitors   | C <sub>IN</sub> and C <sub>OUT</sub> : 1 × 33-µF electrolytic + 1 × 10-µF ceramic |
| Spread spectrum           | Enabled   |
| Discharge function        | Enabled   |

## 8.2.1.2 Detailed Design Procedure

### 8.2.1.2.1 Inductor Selection

There are a few things to consider when choosing an inductor: inductance, current rating, and DC resistance (DCR). 表 8-2 shows recommended inductor values for each operating frequency. The LP8866S-Q1 device automatically sets internal boost compensation controls depending on the selected switching frequency.

**表 8-2. Inductance Values for Boost Switching Frequencies**

| SW FREQUENCY (kHz) | INDUCTANCE (µH) |
|--------------------|-----------------|
| 100                | 47              |
| 200                | 33              |
| 303                | 22              |
| 400                | 22              |
| 500                | 22              |
| 1818               | 10              |
| 2000               | 10              |
| 2222               | 10              |

The current rating of inductor must be at least 25% higher than maximum boost switching current  $I_{SW(max)}$ , which can be calculated with Equation 21. TI recommends to use an inductor with low DCR to achieve good efficiency. Efficiency varies with load condition, switching frequency, and components. 80% can be used as a typical estimation. 65% efficiency needs to take into account in extreme condition.

$$I_{SW(max)} = \frac{\Delta I_L}{2} + \frac{I_{OUT(max)}}{1 - D} \quad (21)$$

where

- $\Delta I_L = V_{IN(min)} \times D / f_{SW} \times L$
- $D = 1 - V_{IN(min)} \times \eta / V_{OUT}$
- $I_{SW(max)}$ : Maximum switching current
- $\Delta I_L$ : Inductor ripple current
- $I_{OUT(max)}$ : Maximum output current
- D: Boost duty cycle

- $V_{IN(min)}$ : Minimum input voltage
- $f_{SW}$ : Minimum switching frequency of the converter
- $L$ : Inductance
- $V_{OUT}$ : Output voltage
- $\eta$ : Efficiency of boost converter

#### 8.2.1.2.2 Output Capacitor Selection

Recommended voltage rating for output capacitors is 50% higher than maximum output voltage level. Capacitance value determines voltage ripple and boost stability. The DC-bias effect can reduce the effective capacitance significantly, by up to 80%, a consideration for capacitance value selection. The conservative target effective capacitance is 50  $\mu$ F to achieve good phase and gain margin levels. A design table in product webpage could be referred for the target effective capacitance in a certain application. TI recommends using 33- $\mu$ F Al-polymer electrolytic capacitor together with 10- $\mu$ F ceramic capacitors in parallel to reduce ripple, increase stability, and reduce ESR effect.

#### 8.2.1.2.3 Input Capacitor Selection

Recommended input capacitance is the same as output capacitance although input capacitors are not as critical to boost operation. Input capacitance can be reduced but must ensure enough filtering for input power.

#### 8.2.1.2.4 Charge Pump Output Capacitor

TI recommends a ceramic capacitor with at least 10-V voltage rating for the output capacitor of the charge pump. A 10- $\mu$ F capacitor can be used for most applications.

#### 8.2.1.2.5 Charge Pump Flying Capacitor

TI recommends a ceramic capacitor with at least 10-V voltage rating for the flying capacitor of the charge pump. One 2.2- $\mu$ F capacitor connecting C1P and C1N pins can be used for most applications.

#### 8.2.1.2.6 Output Diode

A Schottky diode must be used for the boost output diode. Current rating must be at least 25% higher than the maximum output current. Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency. At maximum current, the forward voltage must be as low as possible; less than 0.5 V is recommended. Reverse breakdown voltage of the Schottky diode must be significantly larger than the output voltage, 25% higher voltage rating is recommended. Do not use ordinary rectifier diodes, because slow switching speeds and long recovery times cause efficiency and load regulation to suffer.

#### 8.2.1.2.7 Switching FET

Gate-drive voltage for the FET is 5V. Switching FET is a critical component for determining power efficiency of the boost converter. Several aspects need to be considered when selecting switching FET such as voltage and current rating,  $R_{DS(on)}$ , power dissipation, thermal resistance and rise/fall times. An N type MOSFET with at least 25% higher voltage rating than maximum output voltage must be used. Current rating of switching FET should be same or higher than inductor rating.  $R_{DS(on)}$  must be as low as possible, less than 20 m $\Omega$  is recommended. Thermal resistance ( $R_{\theta JA}$ ) must also be low to dissipate heat from power loss on switching FET. In most cases, a resistance is recommended between GD pin and Switching FET's gate terminal. It could be used to control the rising/falling time of the switching FET. This gate resistance could offer the flexibility of balancing between EMC performance and efficiency.

#### 8.2.1.2.8 Boost Sense Resistor

The  $R_{SENSE}$  resistor determines the boost overcurrent limit and is sensed every boost switching cycle. A high-power 20-m $\Omega$  resistor can be used for sensing the boost SW current and setting maximum current limit at 10 A (typical).  $R_{SENSE}$  can be increased to lower this limit and can be calculated with [Equation 22](#). In typical condition, to avoid too much efficiency loss on  $R_{SENSE}$  resistor, boost overcurrent limit is recommended to be set above 4A, therefore  $R_{SENSE}$  doesn't exceed 50 m $\Omega$ . Power rating can be calculated from the inductor current and sense resistor resistance value.

$$R_{\text{SENSE}} = \frac{200 \text{ mV}}{I_{\text{BOOST\_OCP}}} \quad (22)$$

where

- $R_{\text{SENSE}}$ : boost sense resistor (mΩ)
- $I_{\text{BOOST\_OCP}}$ : boost overcurrent limit

#### 8.2.1.2.9 Power-Line FET

A power line FET can be used to disconnect input power from boost input to protect the LP8866S-Q1 device and boost components in case an overcurrent event occurs. A P type MOSFET is used for the power-line FET. Voltage rating must be at least 25% higher than maximum input voltage level. Low  $R_{\text{DS(on)}}$  is important to reduce power loss on the FET — less than 20 mΩ is recommended. Current rating for the FET must be at least 25% higher than input peak current. Minimum Gate-to-Source voltage ( $V_{\text{GS}}$ ) to turn on transistor fully must be less than minimum input voltage; use a 20-kΩ resistor between the pFET gate and source.

#### 8.2.1.2.10 Input Current Sense Resistor

A high-power resistor can be used for sensing the boost input current. Overcurrent condition is detected when the voltage across  $R_{\text{ISENSE}}$  reaches 220 mV. Typical 20-mΩ sense resistor is used to set 11-A input current limit. Sense resistor value can be increased to lower overcurrent limit for application as needed. Power rating can be calculated from the input current and resistance value.

#### 8.2.1.2.11 Feedback Resistor Divider


Feedback resistors  $R_{\text{FB1}}$  and  $R_{\text{FB2}}$  determine the maximum boost output level. Output voltage can be calculated as in [Equation 23](#):

$$V_{\text{OUT\_MAX}} = \left( \frac{V_{\text{BG}}}{R_{\text{FB2}}} + I_{\text{SEL\_MAX}} \right) \times R_{\text{FB1}} + V_{\text{BG}} \quad (23)$$

where

- $V_{\text{BG}} = 1.21 \text{ V}$
- $I_{\text{SEL\_MAX}} = 38.7 \text{ } \mu\text{A}$
- $R_{\text{FB1}} / R_{\text{FB2}}$  normal recommended range is 7~15

#### 8.2.1.2.12 Critical Components for Design

 [8-2](#) shows the critical part of circuitry: boost components, the LP8866S-Q1 internal charge pump for gate-driver powering, and powering/grounding of LP8866S-Q1. Schematic example is shown in [img 8-2](#).

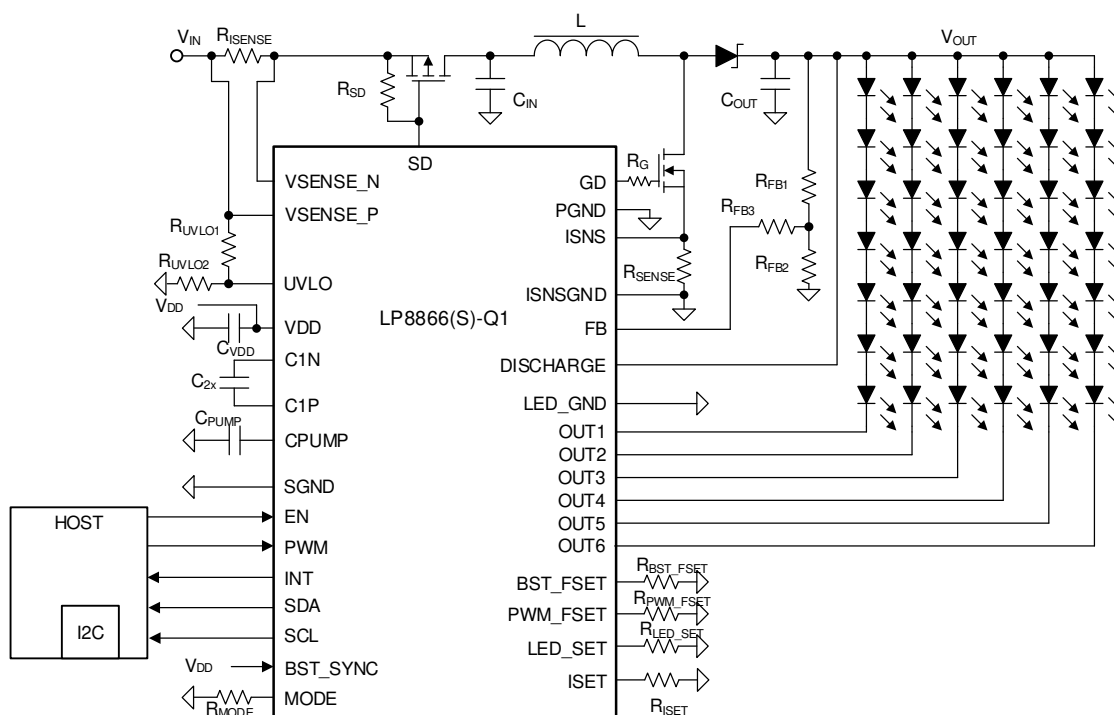
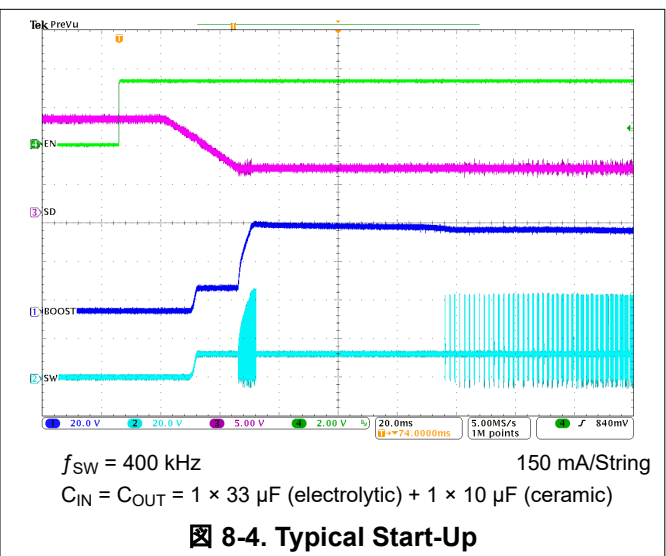
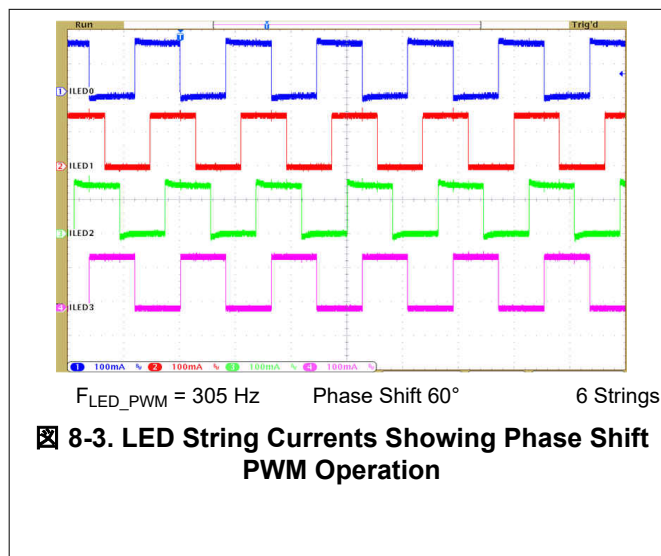


图 8-2. Critical Components for Full Feature Design

**表 8-3. Recommended Component Values for Full Feature Design Example**

| REFERENCE DESIGNATOR  | DESCRIPTION  | NOTE   |
|-----------------------|--|--|
| R <sub>ISENSE</sub>   | 20 mΩ, 3 W   | Input current sensing resistor   |
| R <sub>SD</sub>       | 20 kΩ, 0.1 W   | Power-line FET gate pullup resistor  |
| R <sub>SENSE</sub>    | 30 mΩ, 3 W   | Boost current sensing resistor   |
| R <sub>G</sub>        | 15 Ω, 0.1 W  | Gate resistor to control the rising/falling time of nMOSFET for EMC  |
| R <sub>UVLO1</sub>    | 76.8 kΩ, 0.1 W   | These UVLO resistor settings set the VIN_UVLO rising voltage at 3.75 V, VIN_UVLO falling voltage at 3.35 V |
| R <sub>UVLO2</sub>    | 20.5 kΩ, 0.1 W   |  |
| R <sub>FB3</sub>      | 0 Ω, 0.1 W   | Not needed unless 100-kΩ restrictions on resistors   |
| R <sub>FB2</sub>      | 100 kΩ, 0.1 W  | Bottom feedback divider resistor   |
| R <sub>FB1</sub>      | 910 kΩ, 0.1 W  | Top feedback divider resistor  |
| R <sub>BST_FSET</sub> | 3.92 kΩ, 0.1 W   | Boost frequency set resistor (400 kHz)   |
| R <sub>ISET</sub>     | 20.8 kΩ, 0.1 W   | Current set resistor (150 mA per channel)  |
| R <sub>PWM_FSET</sub> | 17.8 kΩ, 0.1 W   | Output PWM frequency set resistor (4.88kHz PWM frequency to avoid audible noise)                           |
| R <sub>MODE</sub>     | 3.92 kΩ, 0.1 W   | Mode resistor (Phase-Shift PWM mode with 0x2B I2C address)   |
| R <sub>LED_SET</sub>  | 3.92 kΩ, 0.1 W   | LED_SET resistor (6channels configuration)   |
| C <sub>PUMP</sub>     | 10-μF, 10-V ceramic                                    | Charge-pump output capacitor   |
| C <sub>2X</sub>       | 2.2-μF, 10-V ceramic                                   | Flying capacitor   |
| C <sub>VDD</sub>      | 4.7-μF + 0.1-μF, 10-V ceramic                          | VDD bypass capacitor   |
| C <sub>IN</sub>       | 1 × 33-μF, 50-V electrolytic + 1 × 10-μF, 50-V ceramic | Boost input capacitor  |
| C <sub>OUT</sub>      | 1 × 33-μF, 50-V electrolytic + 1 × 10-μF, 50-V ceramic | Boost output capacitor   |
| L1                    | 22-μH saturation current 6.5 A                         | Boost inductor   |
| D1                    | 50 V, 6.5-A Schottky diode                             | Boost Schottky diode   |
| Q1                    | 60-V, 15-A nMOSFET                                     | Boost nMOSFET  |
| Q2                    | 60-V, 15-A pMOSFET                                     | Power-line FET   |

### 8.2.1.3 Application Curves



## 8.2.2 Application with Basic/Minimal Operation

The LP8866S-Q1 needs only a few external components for basic functionality if material cost and PCB area for a solution need to be minimized. In this example LP8866S-Q1 is configured with external components and no I2C communication. The power-line FET is removed, as is input current sensing. Internal charge pump is not used, and all external synchronization functions and special features are disabled. The 33- $\mu$ F Al-polymer electrolytic capacitor is removed for PCB area and height limitation. And boost external compensation is used to compensate the removal of the 33- $\mu$ F Al-polymer electrolytic capacitor.

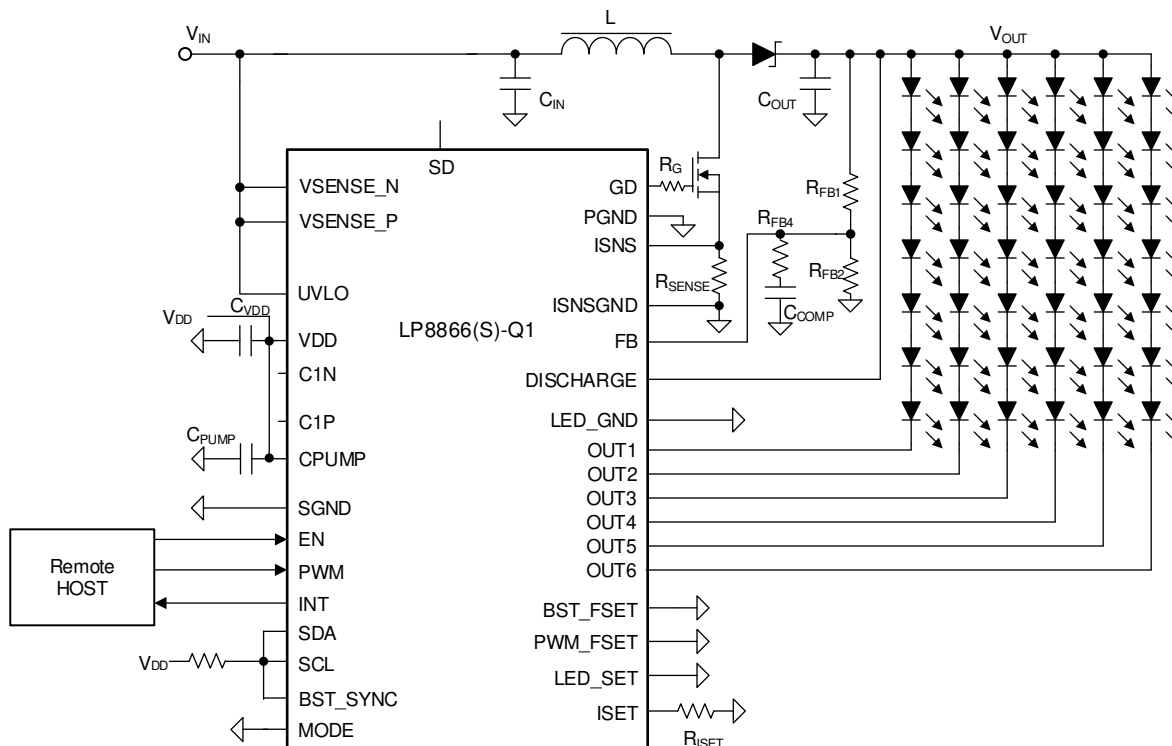


图 8-5. Minimal Solution/Minimum Components Application



### 8.2.2.1 Design Requirements

This typical LED-driver application is designed to meet the parameters listed in [表 8-4](#):

**表 8-4. LP8866S-Q1 Minimal Solution Design Parameters**

| DESIGN PARAMETER          | VALUE  |
|---------------------------|--|
| VIN voltage range         | 3 V to 20 V (Quiescent Voltage)                          |
| VDD voltage               | 5 V  |
| LED strings configuration | 6 strings, 7 LEDs in series                              |
| Charge pump               | Disabled   |
| Brightness control        | PWM  |
| Output configuration      | OUT1 to OUT6 are in phase shift mode (60°)               |
| LED string current        | 120 mA   |
| Boost frequency           | 400 kHz  |
| Inductor                  | 22 µH at 6.5-A saturation current                        |
| R <sub>ISENSE</sub>       | 20 mΩ  |
| Power-line FET            | Enabled  |
| R <sub>SENSE</sub>        | 30 mΩ  |
| Input/Output capacitors   | C <sub>IN</sub> and C <sub>OUT</sub> : 3 × 10-µF ceramic |
| Spread spectrum           | Enabled  |
| Discharge function        | Enabled  |

### 8.2.2.2 Detailed Design Procedure

See [Detailed Design Procedure](#).

### 8.2.2.3 Application Curves

See [Application Curves](#).

### 8.2.3 SEPIC Mode Application

When LED string voltage can be above and below the input voltage level, use the SEPIC configuration. In SEPIC mode, the SW pin detects a maximum voltage equal to the sum of the input and output voltages, a consideration when selecting components.

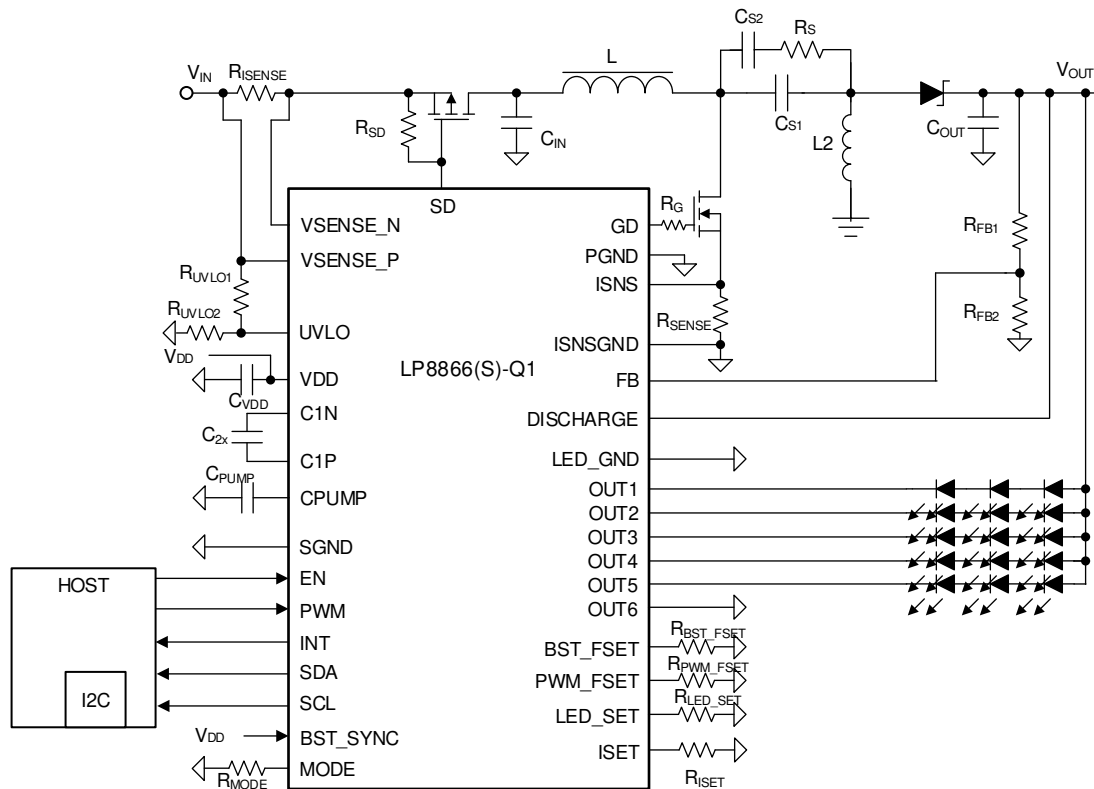


图 8-6. SEPIC Mode with Three LEDs in Series

### 8.2.3.1 Design Requirements

This typical LED-driver application is designed to meet the parameters listed in [表 8-5](#):

**表 8-5. LP8866S-Q1 SEPIC Mode Design Parameters**

| DESIGN PARAMETER              | VALUE   |
|-------------------------------|---|
| V <sub>IN</sub> voltage range | 4.5 V to 20 V (quiescent voltage)   |
| V <sub>DD</sub> voltage       | 3.3 V   |
| LED strings configuration     | 5 strings, 3 LEDs in series   |
| Charge pump                   | Enabled   |
| Brightness control            | I2C   |
| Output configuration          | OUT1 to OUT5 are in phase shift PWM mode  |
| LED string current            | 80 mA   |
| Boost frequency               | 2.2 MHz   |
| Inductor                      | 10 µH at 4-A saturation current   |
| R <sub>ISENSE</sub>           | 20 mΩ   |
| Power-line FET                | Enabled   |
| R <sub>SENSE</sub>            | 50 mΩ   |
| Input/Output capacitors       | C <sub>IN</sub> and C <sub>OUT</sub> : 1 × 33-µF electrolytic + 1 × 10-µF ceramic |
| Spread spectrum               | Enabled   |
| Discharge function            | Enabled   |

### 8.2.3.2 Detailed Design Procedure

#### 8.2.3.2.1 Inductor Selection

Inductance for both inductors can be selected from [表 8-6](#), depending on operating frequency for the application. Current rating is recommended to be at least 25% higher than maximum inductor peak current. Peak-to-peak ripple current can be estimated to be approximately 40% of the maximum input current and inductor peak current can be calculated with [Equation 24](#), [Equation 25](#), and [Equation 26](#):

**表 8-6. Inductance Values for SEPIC Switching Frequencies**

| SW FREQUENCY (kHz) | INDUCTANCE (µH) |
|--------------------|-----------------|
| 100                | 22              |
| 200                | 15              |
| 303                | 10              |
| 400                | 10              |
| 500                | 10              |
| 1818               | 4.7             |
| 2000               | 4.7             |
| 2222               | 4.7             |

$$I_{L1(\text{peak})} = I_{\text{OUT}} \times \frac{V_{\text{OUT}} + V_D}{V_{\text{IN}(\text{min})}} \times \left(1 + \frac{40\%}{2}\right) \quad (24)$$

where

- $I_{L1(\text{peak})}$ : Peak current for inductor 1
- $I_{\text{OUT}}$ : Maximum output current
- $V_{\text{OUT}}$ : Output voltage
- $V_D$ : Diode forward voltage drop
- $V_{\text{IN}(\text{min})}$ : Minimum input voltage

$$I_{L2(\text{peak})} = I_{\text{OUT}} \times \left(1 + \frac{40\%}{2}\right) \quad (25)$$

where

- $I_{L2(\text{peak})}$ : Peak current for inductor 2
- $I_{\text{OUT}}$ : Maximum output current

$$\Delta I_L = I_{\text{IN}} \times 40\% = I_{\text{OUT}} \times \frac{V_{\text{OUT}}}{V_{\text{IN}(\text{min})}} \times 40\% \quad (26)$$

where

- $\Delta I_L$ : Inductor ripple current
- $I_{\text{IN}}$ : Input current
- $V_{\text{OUT}}$ : Output voltage
- $V_{\text{IN}(\text{min})}$ : Minimum input voltage

#### 8.2.3.2.2 Coupling Capacitor Selection

The coupling capacitors  $C_s$  isolate the input from the output and provide protection against a shorted load. The selection of SEPIC capacitors,  $C_s$ , depends mostly on the RMS current, which can be calculated with [Equation 27](#). The capacitors must be rated for a large RMS current relative to the output power; TI recommends at least 25% higher rating for  $I_{\text{RMS}}$ . When using uncoupled inductors, use one 10- $\mu\text{F}$  ceramic capacitor in parallel with one 33- $\mu\text{F}$  electrolytic capacitor and series 2- $\Omega$  resistor. If coupled inductors are used, then use only one 10- $\mu\text{F}$  ceramic capacitor.

$$I_{C_s(\text{rms})} = I_{\text{OUT}} \times \sqrt{\frac{V_{\text{OUT}} + V_D}{V_{\text{IN}(\text{min})}}} \quad (27)$$

where

- $I_{C_s(\text{rms})}$ : RMS current of  $C_s$  capacitor
- $I_{\text{OUT}}$ : Output current
- $V_{\text{OUT}}$ : Output voltage
- $V_D$ : Diode forward voltage drop
- $V_{\text{IN}(\text{min})}$ : Minimum input voltage

#### 8.2.3.2.3 Output Capacitor Selection

See [Detailed Design Procedure](#).

#### 8.2.3.2.4 Input Capacitor Selection

See [Detailed Design Procedure](#).

#### 8.2.3.2.5 Charge Pump Output Capacitor

See [Detailed Design Procedure](#).

#### 8.2.3.2.6 Charge Pump Flying Capacitor

See [Detailed Design Procedure](#).

#### 8.2.3.2.7 Switching FET

Gate-drive voltage for the FET is 5V. Use an N-type MOSFET for the switching FET. The switching FET for SEPIC mode sees a maximum voltage of  $V_{IN(max)} + V_{OUT}$ , 25% higher rating is recommended. Current rating is also recommended to be 25% higher than peak current, which can be calculated with [Equation 28](#).  $R_{DS(on)}$  must be as low as possible — less than 20 mΩ is recommended. Thermal resistance ( $R_{\theta JA}$ ) must also be low to dissipate heat from power loss on switching FET. Typical rise/fall time values recommended are less than 10 ns.

$$I_{Q1(peak)} = I_{L1(peak)} + I_{L2(peak)} \quad (28)$$

where

- $I_{Q1(peak)}$ : Peak current for switching FET
- $I_{L1(peak)}$ : Peak current for inductor 1
- $I_{L2(peak)}$ : Peak current for inductor 2 BOOST\_OCP

#### 8.2.3.2.8 Output Diode

A Schottky diode must be used for the SEPIC output diode. Current rating must be at least 25% higher than the maximum current, which is the same as switch peak current. Schottky diodes with a low forward drop and fast switching speeds are ideal for increasing efficiency. At maximum current, the forward voltage must be as low as possible; TI recommends less than 0.5 V. Reverse breakdown voltage of the Schottky diode must be able to withstand  $V_{IN(max)} + V_{OUT(max)}$ ; at least 25% higher voltage rating is recommended. Do not use ordinary rectifier diodes, because slow switching speeds and long recovery times cause efficiency and load regulation to suffer.

#### 8.2.3.2.9 Switching Sense Resistor

See [Detailed Design Procedure](#).

#### 8.2.3.2.10 Power-Line FET

See [Detailed Design Procedure](#).

#### 8.2.3.2.11 Input Current Sense Resistor

See [Detailed Design Procedure](#).

#### 8.2.3.2.12 Feedback Resistor Divider


Feedback resistors  $R_{FB1}$  and  $R_{FB2}$  determine the maximum boost output level. Output voltage can be calculated as follows:

$$V_{OUT\_MAX} = \left( \frac{V_{BG}}{R_{FB2}} + I_{SEL\_MAX} \right) \times R_{FB1} + V_{BG} \quad (29)$$

where

- $V_{BG} = 1.21$  V
- $I_{SEL\_MAX} = 38.7$  μA
- $R_{FB1} / R_{FB2}$  normal recommended range is 5~15 (recommended for SEPIC Mode)

#### 8.2.3.2.13 Critical Components for Design

 [8-7](#) shows the critical part of circuitry: SEPIC components, the LP8866S-Q1 internal charge pump for gate-driver powering, and powering/grounding of LP8866S-Q1. Schematic example is shown below.

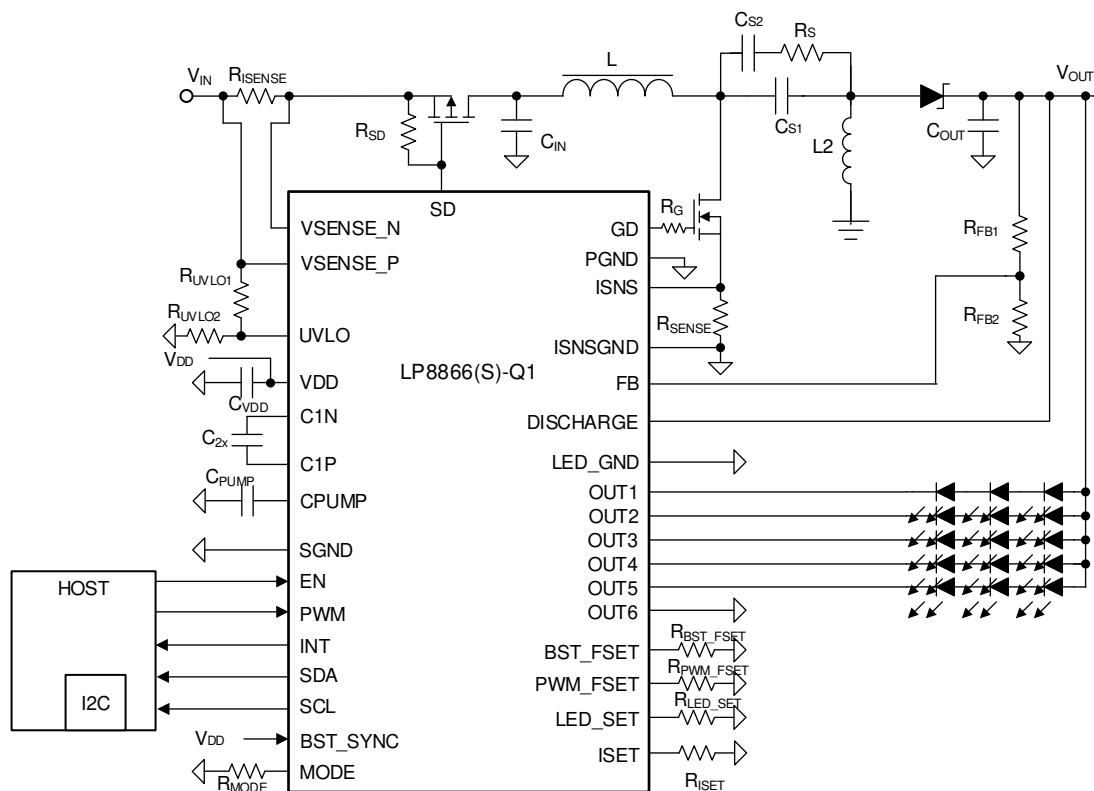


图 8-7. SEPIC Mode with Three LEDs in Series

**表 8-7. Recommended Components for SEPIC Design Example**

| REFERENCE DESIGNATOR  | DESCRIPTION  | NOTE   |
|-----------------------|--|--|
| R <sub>ISENSE</sub>   | 20 mΩ, 1 W   | Input current sensing resistor   |
| R <sub>SD</sub>       | 20 kΩ, 0.1 W   | Power-line FET gate pullup resistor  |
| R <sub>SENSE</sub>    | 50 mΩ, 1 W   | Boost current sensing resistor   |
| R <sub>G</sub>        | 15 Ω, 0.1 W  | Gate resistor to control the rising/falling time of nMOSFET for EMC  |
| R <sub>UVLO1</sub>    | 76.8 kΩ, 0.1 W   | These UVLO resistor settings set the VIN_UVLO rising voltage at 3.75 V, VIN_UVLO falling voltage at 3.35 V |
| R <sub>UVLO2</sub>    | 20.5 kΩ, 0.1 W   |  |
| R <sub>FB2</sub>      | 60 kΩ, 0.1 W   | Bottom feedback divider resistor   |
| R <sub>FB1</sub>      | 330 kΩ, 0.1 W  | Top feedback divider resistor  |
| R <sub>BST_FSET</sub> | 124 kΩ, 0.1 W  | Boost frequency set resistor (2200 kHz)  |
| R <sub>ISET</sub>     | 38.7 kΩ, 0.1 W   | Current set resistor (80 mA per channel)   |
| R <sub>PWM_FSET</sub> | 4.75 kΩ, 0.1 W   | Output PWM frequency set resistor (305-Hz PWM frequency)   |
| R <sub>MODE</sub>     | 3.92 kΩ, 0.1 W   | Mode resistor (Phase-Shift PWM mode with 0x2B I2C address)   |
| R <sub>LED_SET</sub>  | 4.75 kΩ, 0.1 W   | LED_SET resistor (5 channels configuration)  |
| C <sub>PUMP</sub>     | 10-μF, 10-V ceramic                                    | Charge-pump output capacitor   |
| C <sub>2X</sub>       | 2.2-μF, 10-V ceramic                                   | Flying capacitor   |
| C <sub>VDD</sub>      | 4.7-μF + 0.1-μF, 10-V ceramic                          | VDD bypass capacitor   |
| C <sub>IN</sub>       | 1 × 33-μF, 50-V electrolytic + 1 × 10-μF, 50-V ceramic | Boost input capacitor  |
| C <sub>OUT</sub>      | 1 × 33-μF, 50-V electrolytic + 1 × 10-μF, 50-V ceramic | Boost output capacitor   |
| C <sub>S1</sub>       | 10-μF, 50-V ceramic                                    | SEPIC coupling capacitor   |
| C <sub>S2</sub>       | 33-μF, 50-V electrolytic                               | SEPIC coupling capacitor   |
| R <sub>S</sub>        | 2 Ω, 0.125 W   | SEPIC resistor   |
| L1                    | 4.7-μH saturation current 3 A                          | SEPIC inductor   |
| L2                    | 4.7-μH saturation current 3 A                          | SEPIC inductor   |
| D1                    | 50-V 10-A Schottky diode                               | SEPIC Schottky diode   |
| Q1                    | 60-V, 25-A nMOSFET                                     | SEPIC nMOSFET  |
| Q2                    | 60-V, 30-A pMOSFET                                     | Power-line FET   |

### 8.2.3.3 Application Curves

See [Application Curves](#).

## 9 Power Supply Recommendations

The LP8866S-Q1 is designed to operate from a car battery. The V<sub>IN</sub> input must be protected from reverse voltage and voltage dump condition over 48 V. The impedance of the input supply rail must be low enough that the input current transient does not cause drop below VIN UVLO level. If the input supply is connected with long wires, additional bulk capacitance may be required in addition to normal input capacitor.

The voltage range for V<sub>DD</sub> is 3 V to 5.5 V. A ceramic capacitor must be placed as close as possible to the VDD pin. The boost gate driver is powered from the CPUMP pins. A ceramic capacitor must be placed as close to the CPUMP pins as possible.

## 10 Layout

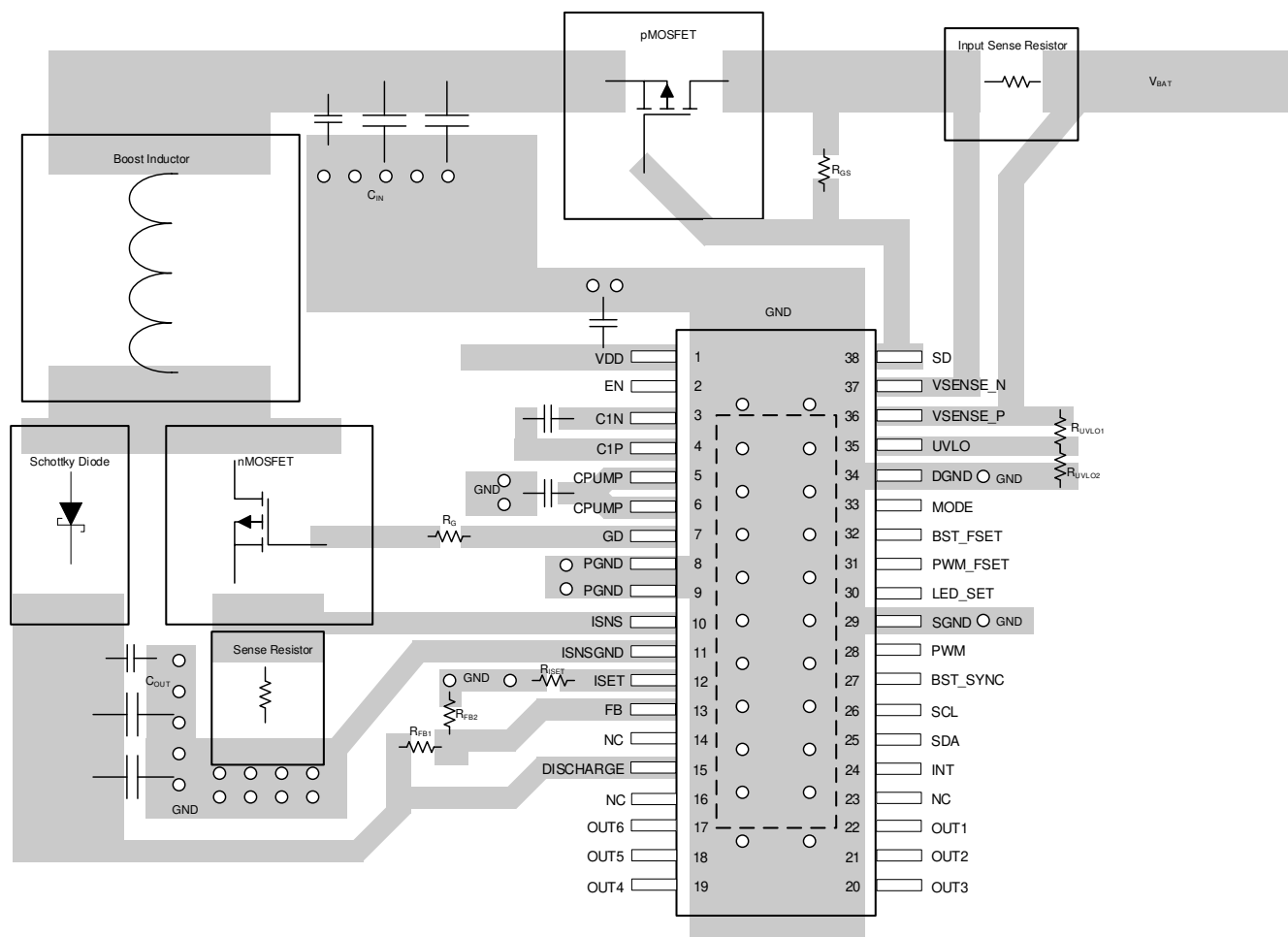
### 10.1 Layout Guidelines

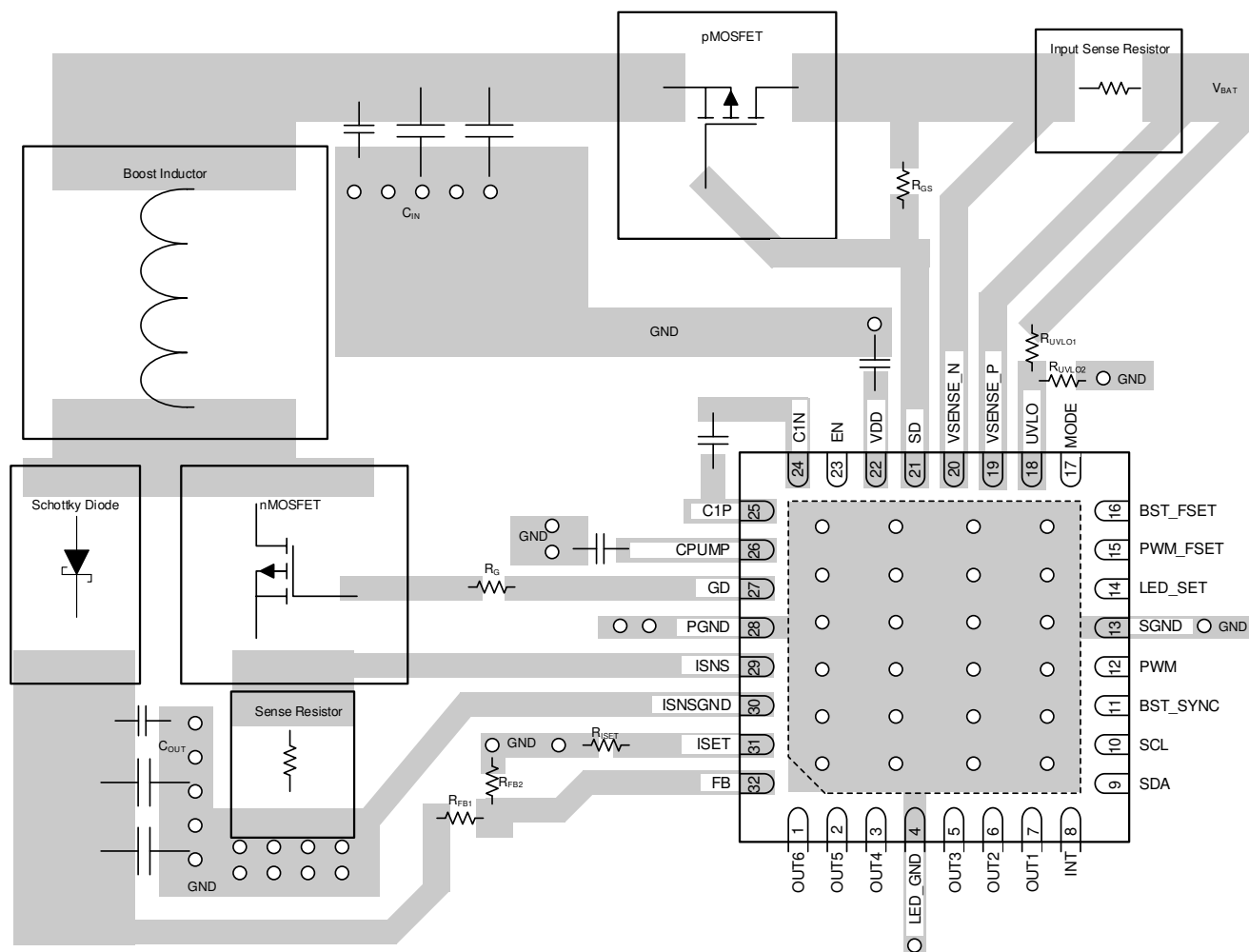
✉ 10-1 shows a layout recommendation for the LP8866S-Q1 used to illustrate the principles of good layout. This layout can be adapted to the actual application layout if and where possible. It is important that all boost components are close to each other and to the chip; the high-current traces must be wide enough. VDD must be as noise-free as possible. Place a VDD bypass capacitor near the VDD and GND pins. A charge-pump capacitor, boost input capacitors, and boost output capacitors must have closest VIAs to GND. Place the charge-pump capacitors close to the device. The main points to guide the PCB layout design:

- Current loops need to be minimized:
  - For low frequency the minimal current loop can be achieved by placing the boost components as close as possible to each other. Input and output capacitor grounds need to be close to each other to minimize current loop size.
  - Minimal current loops for high frequencies can be achieved by making sure that the ground plane is intact under the current traces. High frequency return currents follow the route with minimum impedance, which is the route with minimum loop area, not necessarily the shortest path. Minimum loop area is formed when return current flows just under the *positive* current route in the ground plane, if the ground plane is intact under the route.
  - For high frequency the copper area capacitance must be taken into account. For example, the copper area for the drain of boost N-MOSFET is a tradeoff between capacitance and the cooling capacity of the components.
- GND plane must be intact under the high-current-boost traces to provide shortest possible return path and smallest possible current loops for high frequencies.
- Route boost output voltage (V<sub>OUT</sub>) to LEDs, FB pin & Discharge pin after output capacitors not straight from the diode cathode.
- FB network should be placed as close as possible to the FB pin, not near boost output
- A small bypass capacitor (TI recommends a 39-pF capacitor) could be placed close to the FB pin and GND to suppress high frequency noise
- VDD line must be separated from the high current supply path to the boost converter to prevent high frequency ripple affecting the chip behavior.
- Capacitor connected to charge pump output CPUMP is recommended to have 10-μF capacitance. This capacitor must be as close as possible to CPUMP pin. This capacitor provides a greater peak current for gate driver and must be used even if the charge pump is disabled. If the charge pump is disabled, the VDD and CPUMP pins must be tied together.
- Input and output capacitors need low-impedance grounding (wide traces with many vias to GND plane).
- Input/output ceramic capacitors have DC-bias effect. If the output capacitance is too low, it can cause boost to become unstable under certain load conditions. DC bias characteristics should be obtained from the component manufacturer; DC bias is not taken into account on component tolerance.



## 10.2 Layout Example





10-1. LP8866S-Q1 Layout Guidelines

## 11 Device and Documentation Support

### 11.1 Device Support

#### 11.1.1 Third-Party Products Disclaimer

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#### 11.6 用語集

[TI 用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

## 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status<br>(1) | Package Type | Package<br>Drawing | Pins | Package<br>Qty | Eco Plan<br>(2) | Lead finish/<br>Ball material<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5) | Samples                 |
|------------------|---------------|--------------|--------------------|------|----------------|-----------------|--------------------------------------|----------------------|--------------|-------------------------|-------------------------|
| LP8866SQDCPRQ1   | ACTIVE        | HTSSOP       | DCP                | 38   | 2000           | RoHS & Green    | NIPDAU                               | Level-3-260C-168 HR  | -40 to 125   | LP8866SQ1               | <a href="#">Samples</a> |
| LP8866SQRHBRQ1   | ACTIVE        | VQFN         | RHB                | 32   | 3000           | RoHS & Green    | NIPDAU                               | Level-2-260C-1 YEAR  | -40 to 125   | LP8866S                 | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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## GENERIC PACKAGE VIEW

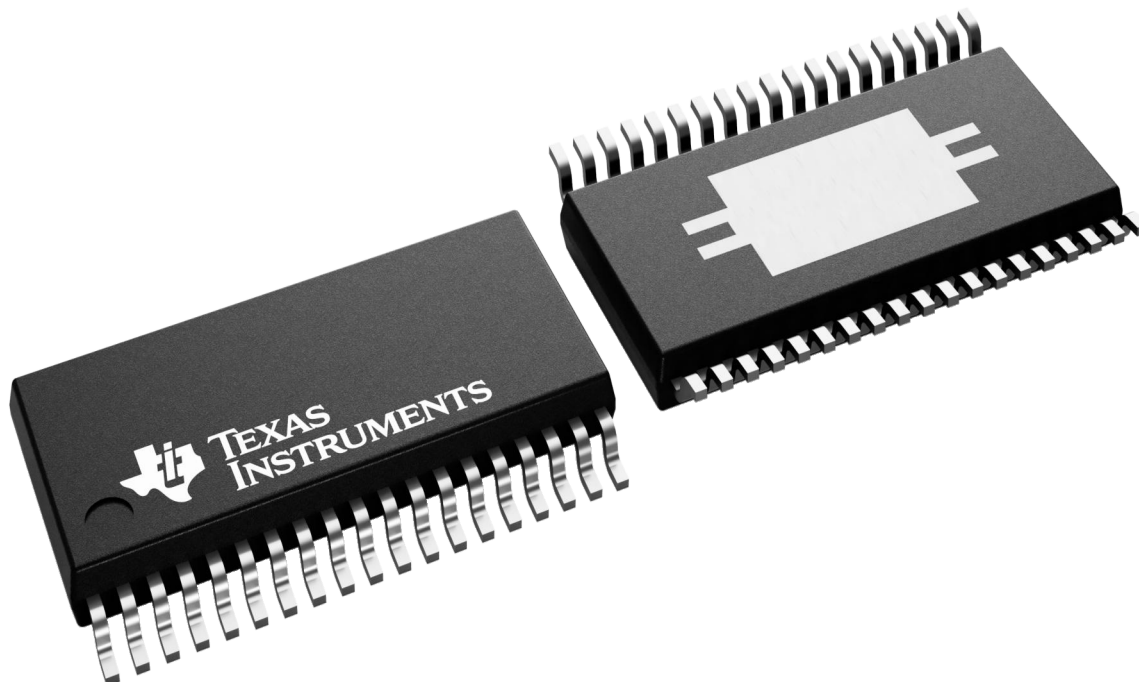
**DCP 38**

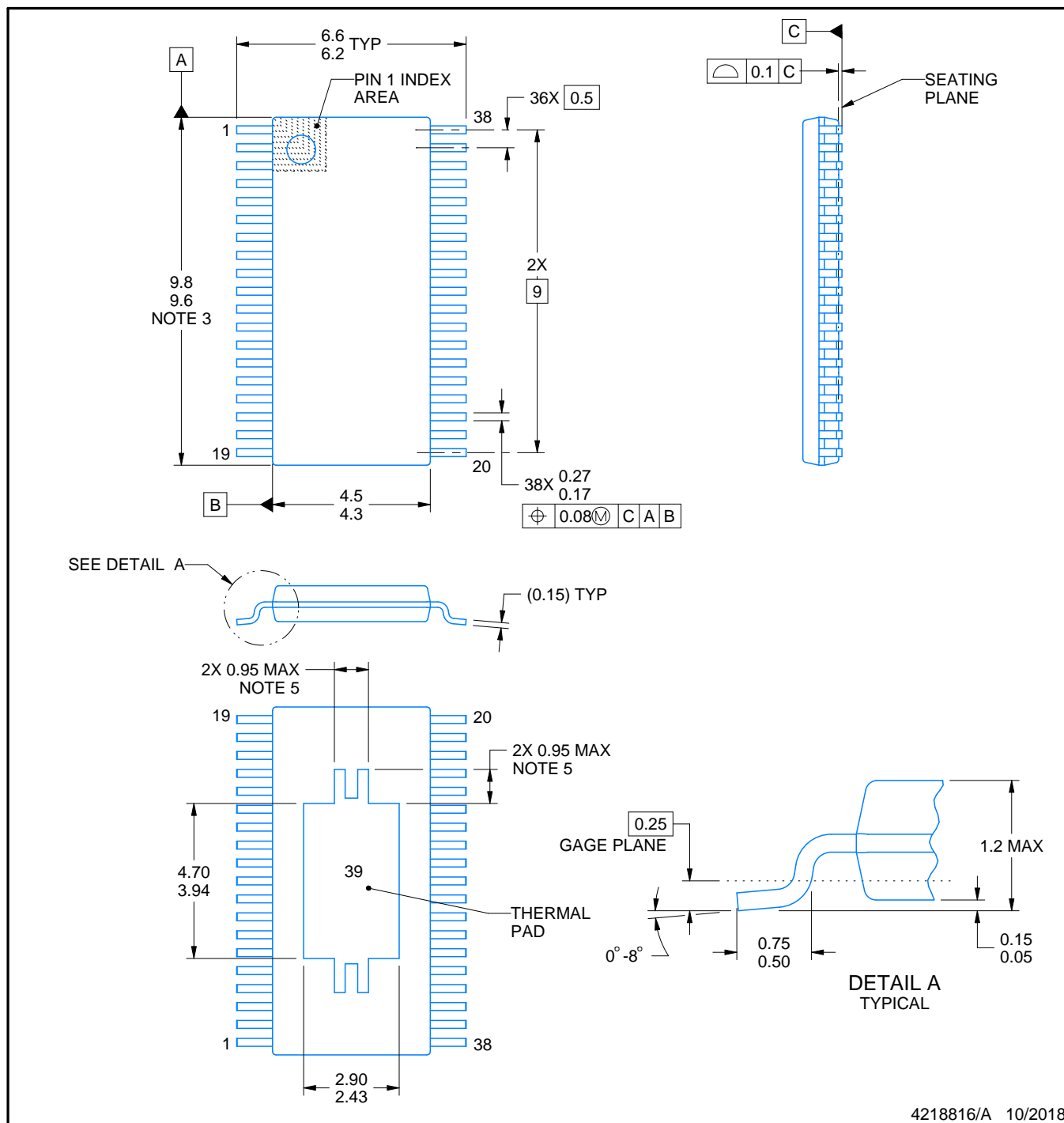
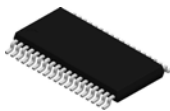
**PowerPAD TSSOP - 1.2 mm max height**

4.4 x 9.7, 0.5 mm pitch

SMALL OUTLINE PACKAGE

This image is a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.





4218816/A 10/2018

**NOTES:**

PowerPAD is a trademark of Texas Instruments.

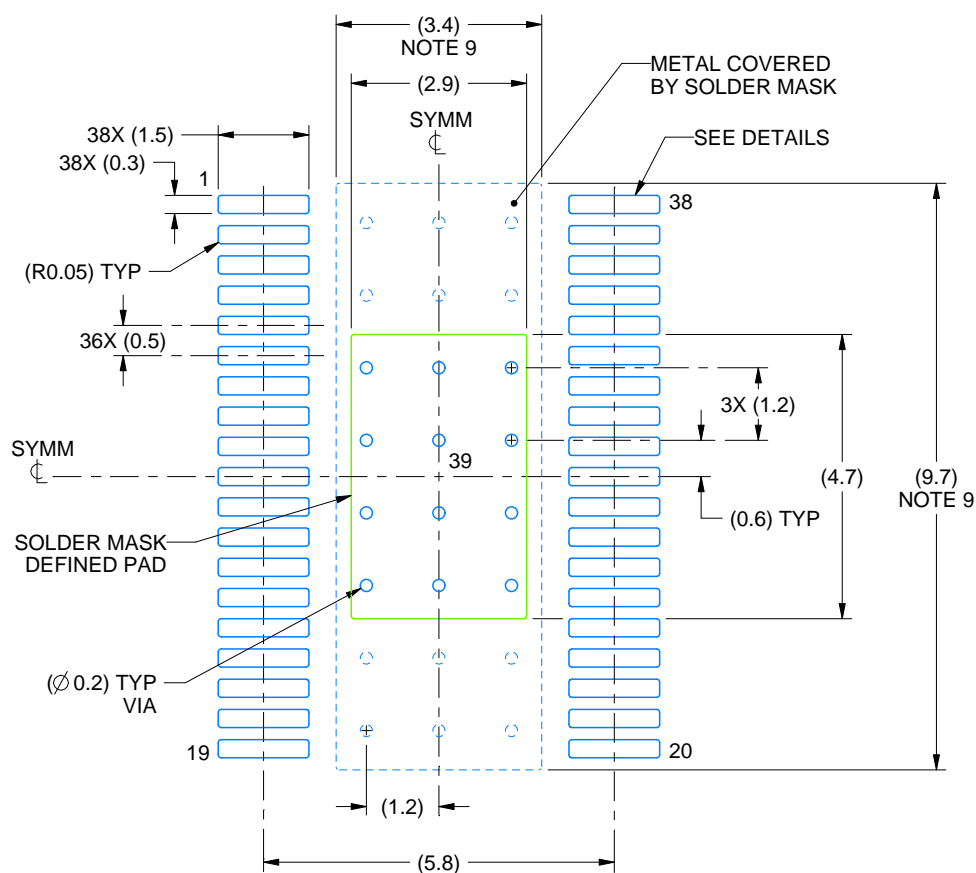
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



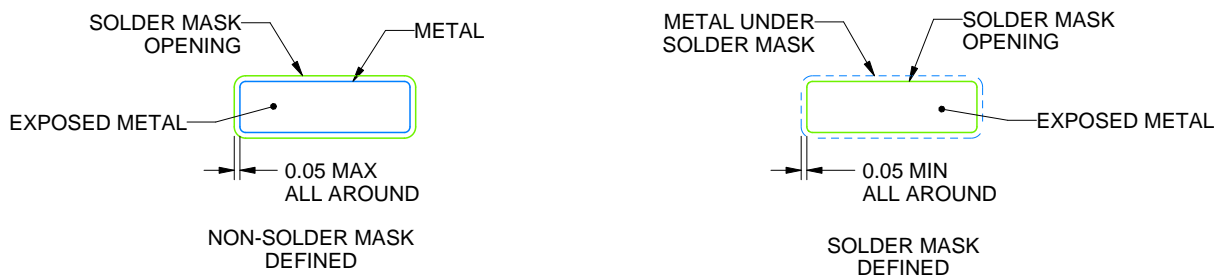
**DCP0038A**

## PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE: 8X



## SOLDER MASK DETAILS

4218816/A 10/2018

NOTES: (continued)

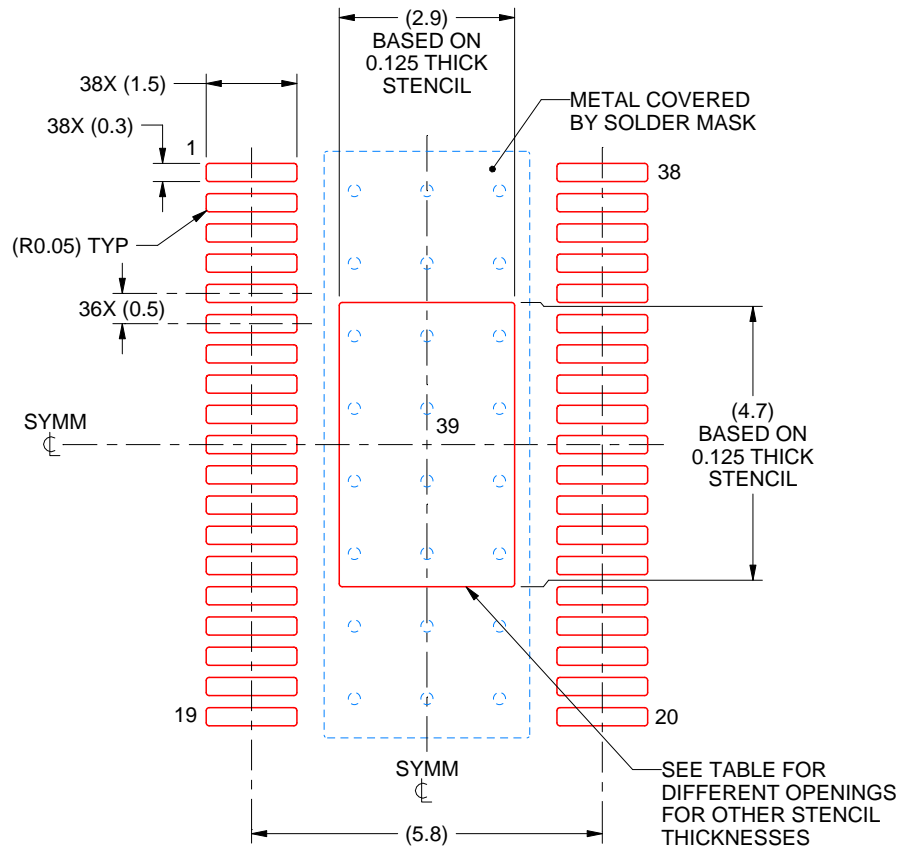
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 ([www.ti.com/lit/slma002](http://www.ti.com/lit/slma002)) and SLMA004 ([www.ti.com/lit/slma004](http://www.ti.com/lit/slma004)).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

DCP0038A

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL  
SCALE: 8X

| STENCIL THICKNESS | SOLDER STENCIL OPENING |
|-------------------|------------------------|
| 0.1               | 3.24 X 5.25            |
| 0.125             | 2.90 X 4.70 (SHOWN)    |
| 0.15              | 2.65 X 4.29            |
| 0.175             | 2.45 X 3.97            |

4218816/A 10/2018

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

## GENERIC PACKAGE VIEW

**RHB 32**

**VQFN - 1 mm max height**

5 x 5, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD



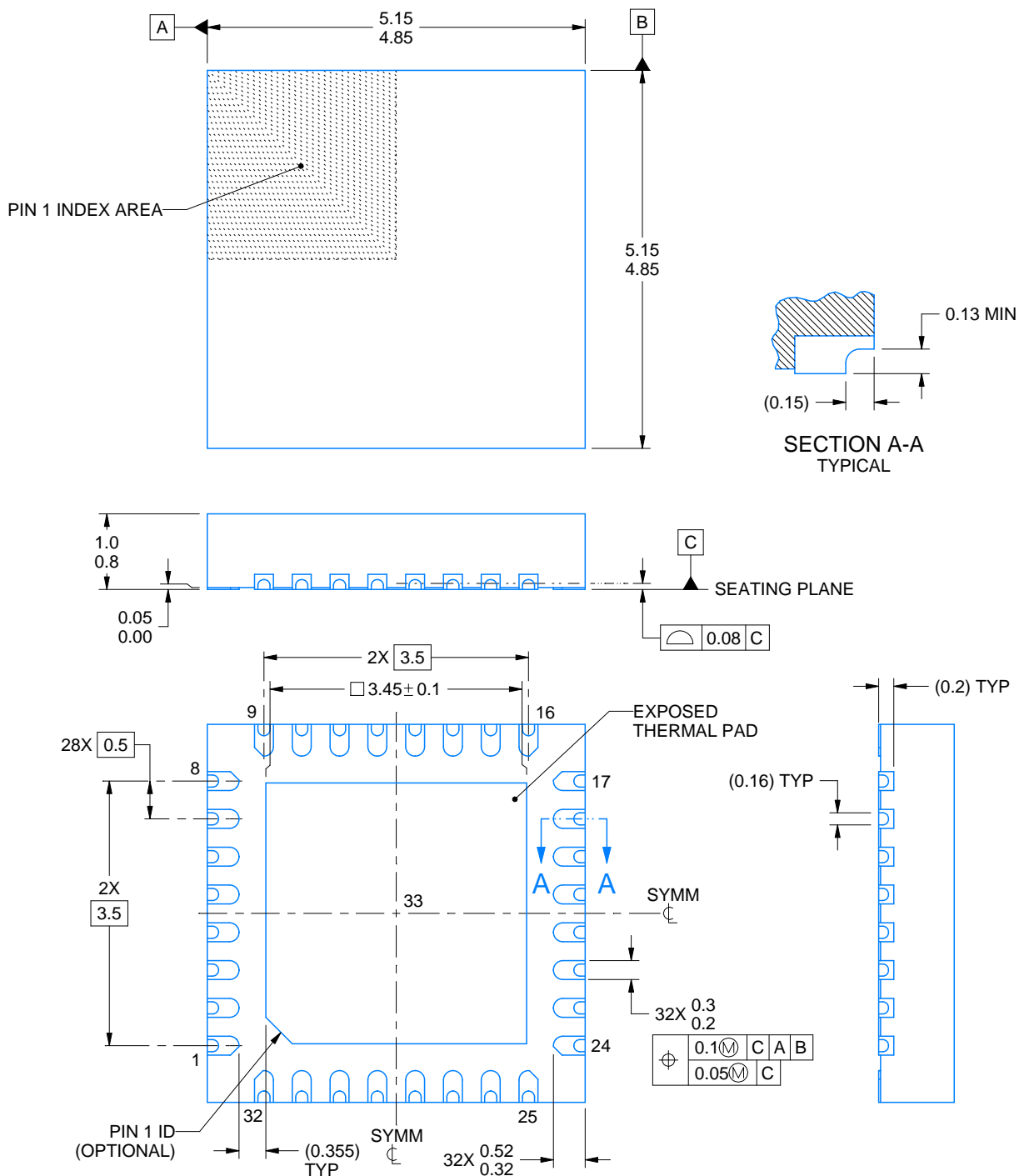
Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4224745/A



### VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4224744/A 01/2019

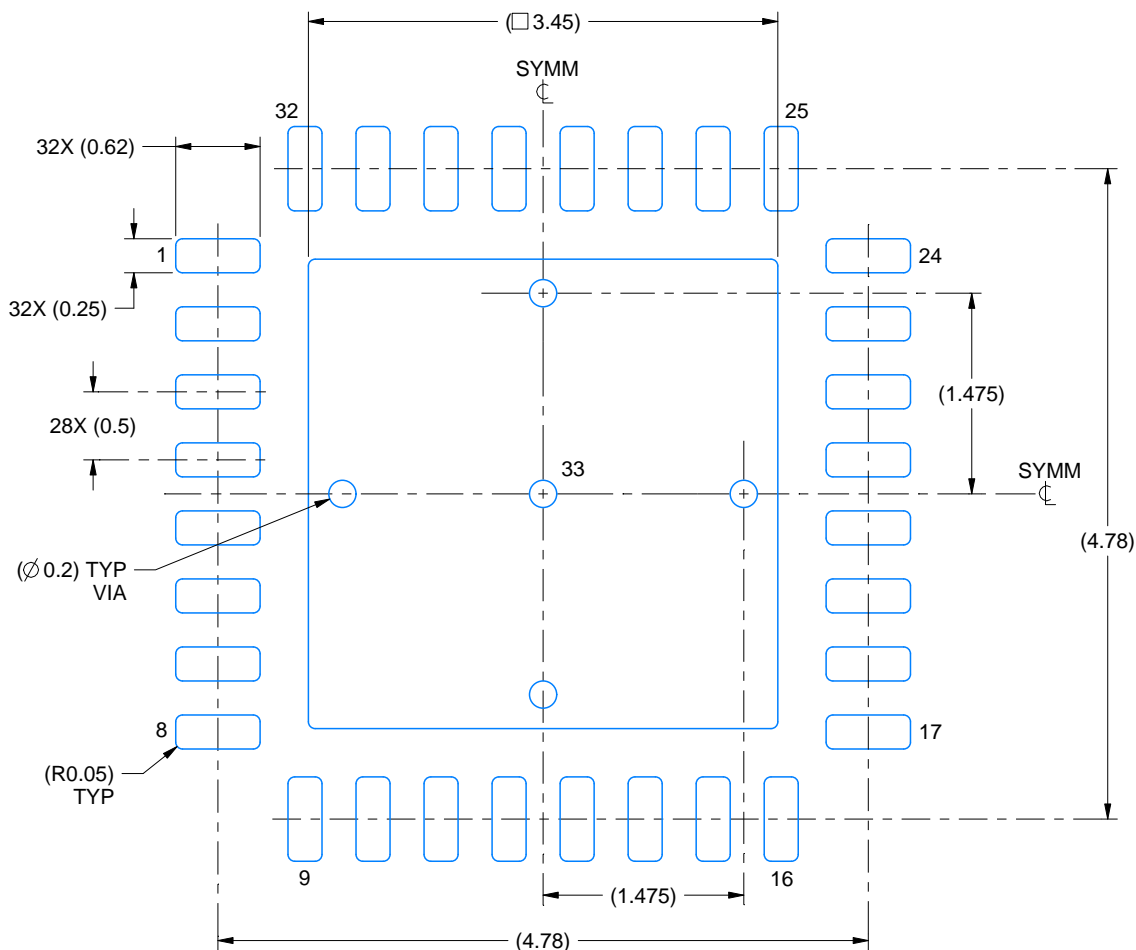
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

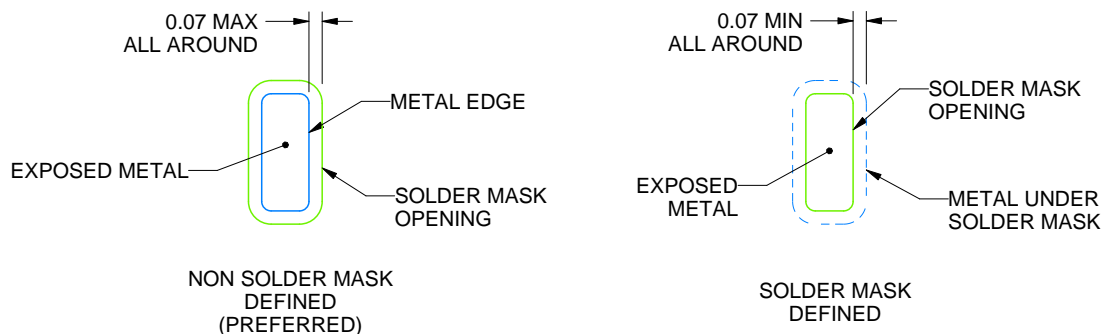
**RHB0032T**

### VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:18X



## SOLDER MASK DETAILS

4224744/A 01/2019

NOTES: (continued)

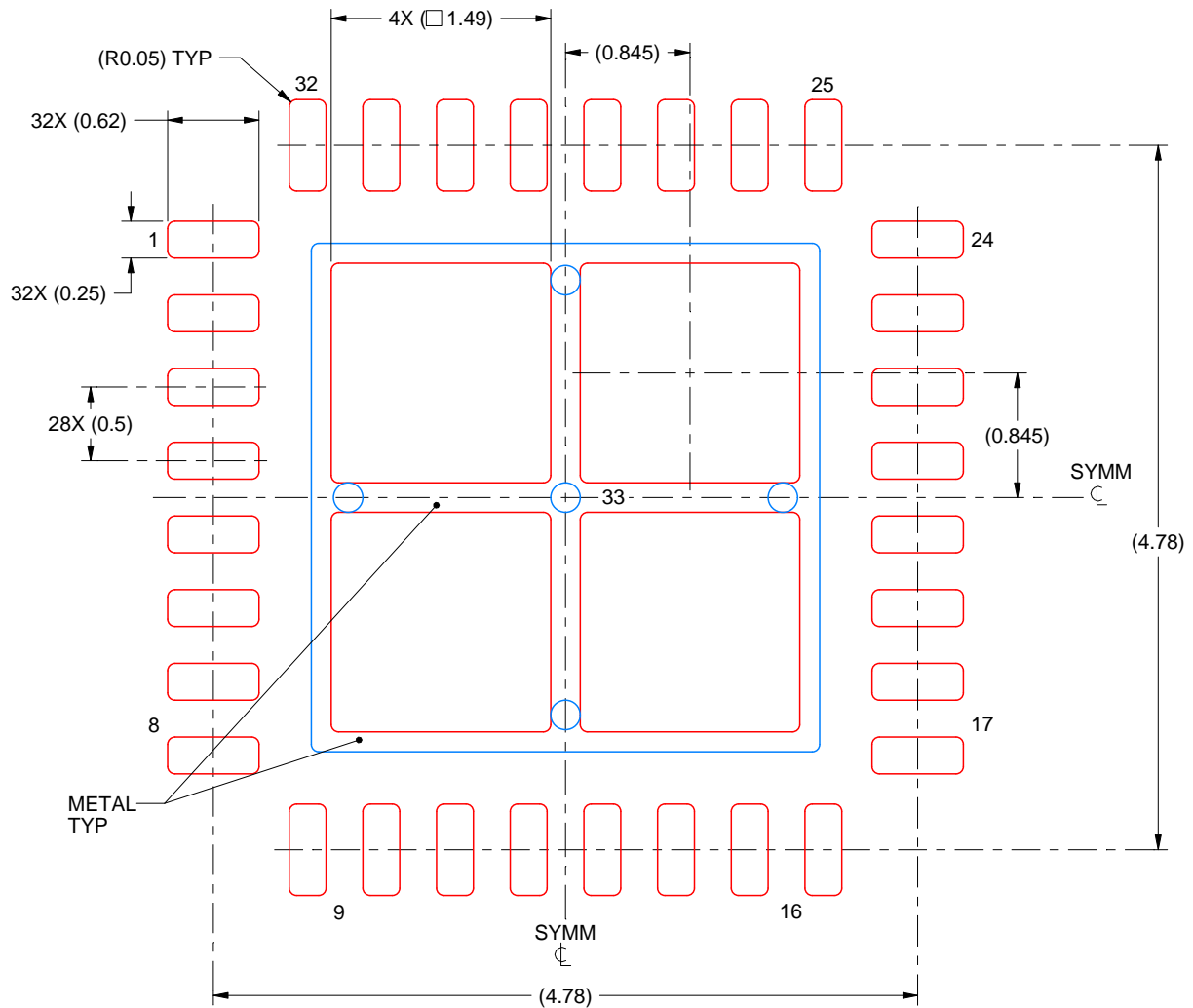
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 ([www.ti.com/lit/sl原因271](http://www.ti.com/lit/sl原因271)).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

# EXAMPLE STENCIL DESIGN

RHB0032T

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



**SOLDER PASTE EXAMPLE**  
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 33:  
75% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE  
SCALE:20X

4224744/A 01/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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