TEXAS INSTRUMENTS
MCT8314Z
JAJSSO4 – DECEMBER 2023

MCT8314Z センサ付き台形制御、統合 FET BLDC モーター ドライバ

ADVANCE INFORMATION

1 特長

- センサ付き台形波制御機能を内蔵した三相 BLDC モーター ドライバ
  - ホール センサを使った台形波 (120°) 整流
  - アナログまたはデジタル ホール入力をサポート
  - 構成可能な PWM 変調:同期 / 非同期
  - サイクル単位の電流制限により位相電流を制限
  - 最大 100kHz の PWM 周波数をサポート
  - 自動同期整流により電力損失を低減
- 動作電圧:5.0V～35V (絶対最大定格 40V)
- 高い出力電流能力:1.5A (ピーク)
- 低い MOSFET オンステート抵抗
  - T_A = 25℃で 575mΩ の $R_{DS(ON)}$ (HS + LS)
- 低消費電力スリープ モード
  - V_{VM} = 24V、T_A = 25℃で 1.5μA
- 電流制限機能内蔵により、外付けの電流センス抵抗が不要
- 柔軟なデバイス構成オプション
  - MCT8314ZS:デバイスの構成とフォルト ステータスのための 5MHz、16 ビット SPI インターフェイス
  - MCT8314ZH:ハードウェア ピンベースの構成
- 1.8V、3.3V、5V のロジック入力をサポート
- 5V (5%)、30mA の LDO レギュレータを内蔵
- 各種保護機能を内蔵
  - 電源低電圧誤動作防止 (UVLO)
  - チャージ ポンプ低電圧 (CPUV)
  - 過電流保護 (OCP)
  - モーター ロック保護
  - 熱警告およびシャットダウン (OTW/OTSD)
  - フォルト状況表示ピン (nFAULT)
  - SPI によるフォルト診断 (オプション)

2 アプリケーション

- ブラシレス DC (BLDC) モーター モジュール
- HVAC モーター
- 小型家電製品
- OA 機器
- ファクトリ オートメーションおよびロボティクス

3 概要

MCT8314Z は、12～24V ブラシレス DC モーターを駆動するための、コード作成不要のセンサ付きシングルチップ台形波整流デバイスを提供します。MCT8314Z は、大電力駆動能力を実現するため、40V の絶対最大定格と 575mΩ (ハイサイドとローサイドを合わせて) の小さい $R_{DS(ON)}$ を持つ 3 つのハーフ H ブリッジを内蔵しています。内蔵された電流制限機能により、起動時または高負荷時のモーター電流が制限され、外付けの検出抵抗が不要になります。内蔵の 5V LDO は、デバイスに必要な電圧レールを生成し、外部回路に電力を供給できます。

MCT8314Z は固定機能のステート マシンでセンサ付き台形波制御を実装しているため、ブラシレス DC モーターを回転させるための外部マイクロコントローラは不要です。MCT8314Z デバイスは、位置をセンスするために 3 個のアナログ ホール コンパレータを内蔵しており、センサ付き台形波 BLDC モーター制御を実現できます。制御方式は、モーター電流制限動作からフォルト応答まで、ハードウェア ピンまたはレジスタ設定を使って詳細に設定できます。速度は、PWM 入力を使って制御できます。

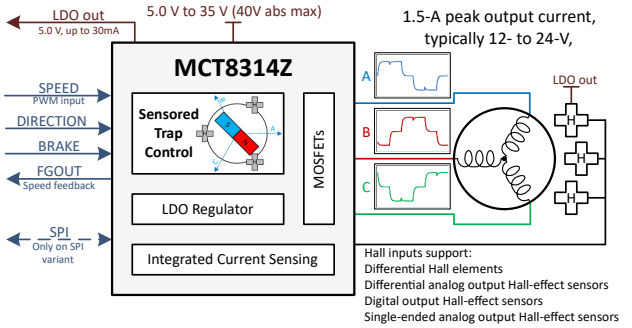
MCT8314Z は、本デバイス自身、モーター、システムをフォルト イベントから保護するために設計された多くの保護機能を内蔵しています。

設計上の考慮事項とデバイス使用上の推奨事項については、Application Information を参照してください。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
MCT8314ZS(2)	WQFN (24)	3.00mm × 3.00mm
MCT8314ZH	WQFN (24)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) このデバイスはプレビューのみで供給されます。



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4 Device Comparison Table

DEVICE	PACKAGES	INTERFACE
MCT8314ZS	24-pin WQFN (3x3 mm)	SPI
MCT8314ZH		Hardware

表 4-1. MCT8314ZS (SPI variant) vs. MCT8314ZH configuration comparison

Parameters	MCT8314ZS (SPI variant)	MCT8314ZH (Hardware variant)
PWM control mode settings	PWM_MODE bits (4 settings)	MODE pin (7 settings)
Direction settings	DIR bit (2 settings)	DIR pin (2 settings)
Current limit threshold	Selectable by resistor to AGND on ILIM pin	
Current limit configuration	ILIM_RECIR bit (2 settings), PWM_100_DUTY_SEL bit	Recirculation fixed to Brake mode and PWM frequency for 100% duty fixed to 20 kHz
Lead angle settings	ADVANCE_LVL bits (8 settings)	ADVANCE pin (7 settings)
FG configuration	FGOUT_SEL bits (4 settings)	3x or 1x commutation frequency depending FGSEL/LOCK_DET_TIME pin configuration
Motor lock configuration: mode, detection and retry timing	MTR_LOCK_MODE bits (4 settings), MTR_LOCK_TDET bits (4 settings), MTR_LOCK_RETRY bit (2 settings)	Enabled with 500-ms automatic retry time, FGSEL/LOCK_DET_TIME pin (3 or 4 detection time settings, depending on configuration)
Automatic synchronous rectification	EN_ASR bit (2 settings)	MODE pin (6 settings)
OCP configuration	OCP_MODE bits (4 settings), $I_{OCP,min}$ = 3 A, OCP_DEG bits (4 settings), and OCP_RETRY bits (2 settings)	Enabled with latched shutdown mode, $I_{OCP,min}$ = 3 A, 0.6 µs deglitch time
Overvoltage protection configuration	OVP_EN bit (2 settings), OVP_SEL bit (2 settings)	Enabled and level is fixed to 34 V (typ)
SDO pin configuration	SDO_MODE bit (2 settings)	NA
SPI fault configuration	SPI_PARITY bit (2 settings), SPI_SCLK_FLT bit (2 settings), SPI_ADDR_FLT bit (2 settings)	NA

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5 Pin Configuration and Functions

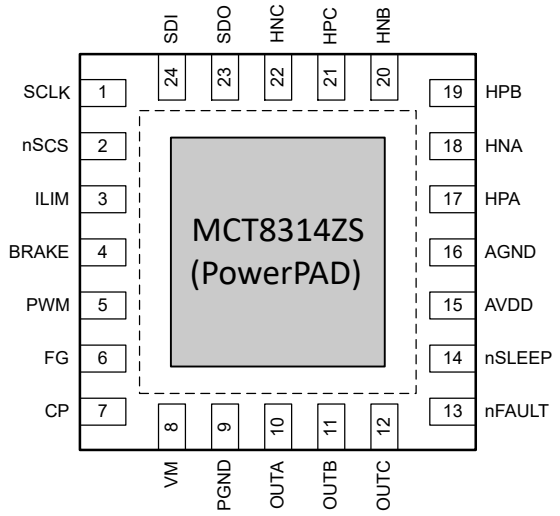

図 5-1. MCT8314ZS 24-Pin VQFN With Exposed Thermal Pad Top View

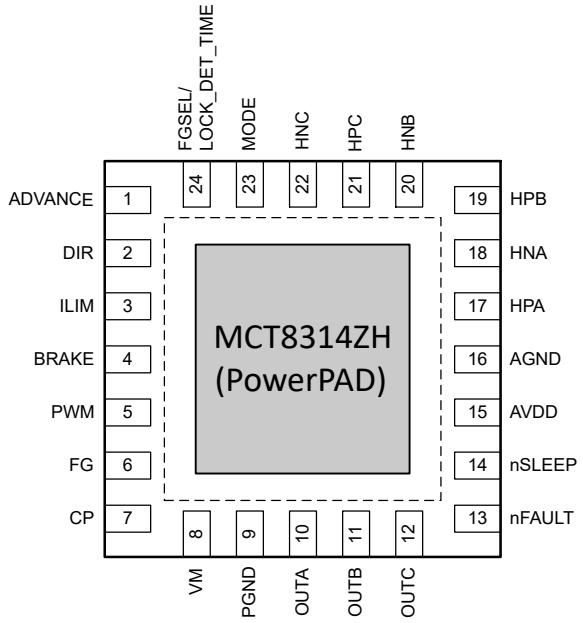

図 5-2. MCT8314ZH 24-Pin VQFN With Exposed Thermal Pad Top View

表 5-1. Pin Functions

PIN	24-pin Package		TYPE[1]	DESCRIPTION
NAME	MCT8314ZS	MCT8314ZH		
ADVANCE	—	1	I	Advance angle level setting. This pin is a 7-level input pin set by an external resistor.
AGND	16	16	GND	Device analog ground. Refer Layout Guidelines for connections recommendation.
AVDD	15	15	PWR O	5.0-V internal regulator output. Connect an X5R or X7R, 2.2-µF, 16-V ceramic capacitor between the AVDD and AGND pins. This regulator can source up to 30 mA externally.
BRAKE	4	4	I	High → Brake the motor when High by turning all low side MOSFETs ON Low → normal operation
CP	7	7	PWR O	Charge pump output. Connect a X5R or X7R, 0.22-µF, 16-V ceramic capacitor between the CP and VM pins.
DIR	—	2	I	Direction pin for setting the direction of the motor rotation to clockwise or counterclockwise.
FG	6	6	O	Motor Speed indicator output. Open-drain output requires an external pull-up resistor to 1.8V to 5.0V. It can be set to different division factor of Hall signals (see FG Signal)
FGSEL/ LOCK_DET_TIME	—	24	I	Electrical frequency generation output mode and Motor lock detection time settings. This pin is a 7-level input pin set by an external resistor.
HNA	18	18	I	Phase A hall element negative input. Noise filter capacitors may be desirable, connected between the positive and negative hall inputs.
HNB	20	20	I	Phase B hall element negative input. Noise filter capacitors may be desirable, connected between the positive and negative hall inputs.
HNC	22	22	I	Phase C hall element negative input. Noise filter capacitors may be desirable, connected between the positive and negative hall inputs.

表 5-1. Pin Functions (続き)

PIN	24-pin Package		TYPE(1)	DESCRIPTION
NAME	MCT8314ZS	MCT8314ZH		
HPA	17	17	I	Phase A hall element positive input. Noise filter capacitors may be desirable, connected between the positive and negative hall inputs.
HPB	19	19	I	Phase B hall element positive input. Noise filter capacitors may be desirable, connected between the positive and negative hall inputs.
HPC	21	21	I	Phase C hall element positive input. Noise filter capacitors may be desirable, connected between the positive and negative hall inputs.
ILIM	3	3	I	Set the threshold for phase current used in cycle by cycle current limit.
MODE	—	23	I	PWM input mode setting. This pin is a 7-level input pin set by an external resistor.
nFAULT	13	13	O	Fault indicator. Pulled logic-low with fault condition; Open-drain output requires an external pull-up resistor to 1.8V to 5.0V. Tie nFAULT to GND if not used.
nSCS	2	—	I	Serial chip select. A logic low on this pin enables serial interface communication.
nSLEEP	14	14	I	Driver nSLEEP. When this pin is logic low, the device goes into a low-power sleep mode. An 20 to 40-µs low pulse can be used to reset fault conditions without entering sleep mode.
OUTA	10	10	PWR O	Half bridge output A
OUTB	11	11	PWR O	Half bridge output B
OUTC	12	12	PWR O	Half bridge output C
PGND	9	9	GND	Device power ground. Refer Layout Guidelines for connections recommendation.
PWM	5	5	I	PWM input for motor control. Set the duty cycle and switching frequency of the phase voltage of the motor.
SCLK	1	—	I	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin (SPI devices).
SDI	24	—	I	Serial data input. Data is captured on the falling edge of the SCLK pin (SPI devices).
SDO	23	—	O	Serial data output. Data is shifted out on the rising edge of the SCLK pin. This pin requires an external pullup resistor (SPI devices).
VM	8	8	PWR I	Power supply. Connect to motor supply voltage; bypass to PGND with two 0.1-µF capacitors (for each pin) plus one bulk capacitor rated for VM. TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device.
Thermal pad			GND	Must be connected to analog ground.

(1) I = input, O = output, GND = ground pin, PWR = power, NC = no connect

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6 Specifications

6.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply pin voltage (VM)	–0.3	40	V
Power supply voltage ramp (VM) from V_{VM} < 4.2 V to V_{VM} = 35 V and from 6 V < V_{VM} to V_{VM} = 35 V		4	V/µs
Power supply voltage ramp (VM) from 4.2 V ≤ V_{VM} ≤ 6 V to V_{VM} = 35 V		1	V/µs
Voltage difference between ground pins (PGND, AGND)	–0.3	0.3	V
Charge pump voltage (CP)	–0.3	V_M + 6	V
Analog regulators pin voltage (AVDD)	–0.3	5.75	V
Hall pin input voltage (HPx, HNx)	–0.3	5.75	V
Configuration pin input voltage (ILIM, ADVANCE, LOCK_DET_TIME, MODE)	–0.3	5.75	V
Logic pin input voltage (PWM, BRAKE, DIR, nSLEEP, nSCS, SCLK, SDI)	–0.3	5.75	V
Logic pin output voltage (nFAULT, SDO)	–0.3	5.75	V
Output pin voltage (OUTA, OUTB, OUTC)	–1	V_{VM} + 1	V
Ambient temperature, T_A	–40	125	°C
Junction temperature, T_J	–40	150	°C
Storage tempertaure, T_{stg}	–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{VM}	Power supply voltage	V_{VM}	5	24	35	V
f_{PWM}	Output PWM frequency	OUTA, OUTB, OUTC			100	kHz
I_{OUT} (1)	Peak output winding current	OUTA, OUTB, OUTC			1.5	A
V_{IN}	Logic input voltage	PWM, BRAKE, DIR, nSLEEP, nSCS, SCLK, SDI	–0.1		5.5	V
	Configuration input voltage	ILIM, ADVANCE, FGSEL/ LOCK_DET_TIME, MODE	–0.1		AVDD	V
V_{OD}	Open drain pullup voltage	nFAULT, SDO	–0.1		5.5	V
V_{SDO}	Push-pull voltage	SDO	2.2		5.5	V
I_{OD}	Open drain output current	nFAULT, SDO			5	mA
T_A	Operating ambient temperature		–40		125	°C
T_J	Operating Junction temperature		–40		150	°C

(1) Power dissipation and thermal limits must be observed

6.4 Thermal Information

THERMAL METRIC(1)		MCT8314Z WQFN (RRM) 24 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	39.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	17.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	17.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	6.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

T_J = –40°C to +150°C, V_{VM} = 5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES						
I_{VMQ}	VM sleep mode current	V_{VM} > 6 V, nSLEEP = 0, T_A = 25 °C		1.5	2.5	µA
		nSLEEP = 0		1.5	5	µA
I_{VMS}	VM standby mode current	nSLEEP = 1, PWM = BRAKE = 0, SPI = 'OFF'		6.8	10	mA
		V_{VM} > 6 V, nSLEEP = 1, PWM = BRAKE = 0, SPI = 'OFF', T_A = 25 °C		6.8	8	mA
I_{VM}	VM operating mode current	V_{VM} > 6 V, nSLEEP = 1, f_{PWM} = 25 kHz, T_A = 25 °C		8	9	mA
		V_{VM} > 6 V, nSLEEP = 1, f_{PWM} = 100 kHz, T_A = 25 °C		9	10	mA
		nSLEEP =1, f_{PWM} = 25 kHz		9	11	mA
		nSLEEP =1, f_{PWM} = 100 kHz		9	11	mA
V_{AVDD}	Analog regulator voltage	V_{VM} > 6 V, 0 mA ≤ I_{AVDD} ≤ 30 mA	4.7	5	5.3	V
I_{AVDD}	External analog regulator load				30	mA
C_{AVDD}	Capacitance for AVDD(1)	External load: 0mA ≤I_{AVDD} ≤ 30 mA	0.7	2.2	2.64	uF
V_{CP}	Charge pump regulator voltage	V_{CP} with respect to VM	3.5	4.7	5.2	V
C_{CP}	Charge pump capacitance (1)	Capacitance between CP and VM	80	220	330	nF
t_{WAKE}	Wakeup time	V_{VM} > V_{UVLO}, nSLEEP = 1 to outputs ready and nFAULT released		3.5	5	ms
t_{SLEEP}	Time to enter sleep mode	nSLEEP = 0 period to enter sleep mode			120	µs
t_{RST}	Reset Pulse time	nSLEEP = 0 period to reset faults	20		40	µs
LOGIC-LEVEL INPUTS (PWM, BRAKE, DIR, nSLEEP, SCLK, SDI, nSCS)						
V_{IL}	Input logic low voltage		0		0.6	V
V_{IH}	Input logic high voltage	Other Pins	1.5		5.5	V
		nSLEEP	1.6		5.5	V
V_{HYS}	Input logic hysteresis	Other Pins	150	250	420	mV
		nSLEEP	95	300	420	mV
I_{IL}	Input logic low current	V_{PIN} (Pin Voltage) = 0 V	–1		1	µA

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T_J = –40°C to +150°C, V_{VM} = 5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	Input logic high current	nSCS, V_{nSCS} (Pin Voltage) = 5 V, VM < 6 V	–1		1	µA
		nSCS, V_{nSCS} (Pin Voltage) = 5 V, VM ≥ 6 V	–1		1	µA
		nSLEEP, V_{nSLEEP} (Pin Voltage) = 5 V	10		30	µA
		Other pins, V_{PIN} (Pin Voltage) = 5 V	25		75	µA
R_{PD}	Input pulldown resistance	nSLEEP	150	225	300	kΩ
		Other pins	70	100	130	kΩ
C_{ID}	Input capacitance			30		pF
SEVEN-LEVEL INPUTS (ADVANCE, MODE, FGSEL/LOCK_DET_TIME)						
V_{L1}	Input mode 1 voltage	Tied to AGND	0		$0.09*V_{AVDD}$	V
V_{L2}	Input mode 2 voltage	22 kΩ ± 5% to AGND	$0.12*V_{AVDD}$	$0.15*V_{AVDD}$	$0.2*V_{AVDD}$	V
V_{L3}	Input mode 3 voltage	100 kΩ ± 5% to AGND	$0.27*V_{AVDD}$	$0.33*V_{AVDD}$	$0.4*V_{AVDD}$	V
V_{L4}	Input mode 4 voltage	Hi-Z	$0.45*V_{AVDD}$	$0.5*V_{AVDD}$	$0.55*V_{AVDD}$	V
V_{L5}	Input mode 5 voltage	100 kΩ ± 5% to AVDD	$0.6*V_{AVDD}$	$0.66*V_{AVDD}$	$0.73*V_{AVDD}$	V
V_{L6}	Input mode 6 voltage	22 kΩ ± 5% to AVDD	$0.77*V_{AVDD}$	$0.85*V_{AVDD}$	$0.9*V_{AVDD}$	V
V_{L7}	Input mode 7 voltage	Tied to AVDD	$0.94*V_{AVDD}$		V_{AVDD}	V
R_{PU}	Input pullup resistance	To AVDD	80	100	120	kΩ
R_{PD}	Input pulldown resistance	To AGND	80	100	120	kΩ
OPEN-DRAIN OUTPUTS (FG, SDO)						
V_{OL}	Output logic low voltage	I_{OD} = 5 mA			0.4	V
I_{OH}	Output logic high current	V_{OD} = 5 V	–1		1	µA
C_{OD}	Output capacitance				30	pF
PUSH-PULL OUTPUTS (SDO)						
V_{OL}	Output logic low voltage	I_{OP} = 5 mA	0		0.4	V
V_{OH}	Output logic high voltage	I_{OP} = 5 mA	2.2		5.5	V
I_{OL}	Output logic low leakage current	V_{OP} = 0 V	–1		1	µA
I_{OH}	Output logic high leakage current	V_{OP} = 5 V	–1		1	µA
C_{OD}	Output capacitance				30	pF
DRIVER OUTPUTS						
$R_{DS(ON)}$	Total MOSFET on resistance (High-side + Low-side)	V_{VM} > 6 V, I_{OUT} = 1 A, T_A = 25°C		575	616	mΩ
		V_{VM} < 6 V, I_{OUT} = 1 A, T_A = 25°C		596	660	mΩ
		V_{VM} > 6 V, I_{OUT} = 1 A, T_J = 150 °C		868	960	mΩ
		V_{VM} < 6 V, I_{OUT} = 1 A, T_J = 150 °C		889	972	mΩ
SR	Phase pin slew rate switching low to high (Rising from 20 % to 80 %)	V_{VM} = 24 V, 50 mA ≤ I_{OUT} ≤ 1.5 A	100	200	320	V/us
	Phase pin slew rate switching high to low (Falling from 80 % to 20 %)	V_{VM} = 24 V, 50 mA ≤ I_{OUT} ≤ 1.5 A	100	200	320	V/us
I_{LEAK}	Leakage current into OUTx	V_{OUTx} = V_{VM}, nSLEEP = 1	-5		0	mA
	Leakage current into OUTx	V_{OUTx} = 0 V, nSLEEP = 1			1	µA

ADVANCE INFORMATION

T_J = –40°C to +150°C, V_{VM} = 5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{DEAD}	Output dead time (high to low / low to high)	V_{VM} = 24 V, HS driver OFF to LS driver ON		500	750	ns
t_{PD}	Propagation delay (high-side / low-side ON/OFF)	V_{VM} = 24 V, 50 mA ≤ I_{OUT} ≤ 1.5 A, PWM pin transition to OUTx transisition		650	1050	ns
t_{MIN_PULSE}	Minimum input pulse width for valid output pulse		600			ns
HALL COMPARATORS						
V_{ICM}	Input Common Mode Voltage (Hall)		0.5		AVDD – 1.2	V
V_{HYS_HALL}	Voltage hysteresis (SPI Device)	HALL_HYS = 0	1.5	5	10	mV
		HALL_HYS = 1	35	50	80	mV
	Voltage hysteresis (HW Device)		1.5	5	10	mV
ΔV_{HYS_HALL}	Hall comparator hysteresis difference	Between Hall A, Hall B and Hall C comparator	–8		8	mV
I_I	Input leakage current	HPx = HNx = 0 V	–1		1	µA
t_{HDG}	Hall deglitch time		0.6	1.15	1.7	µs
t_{HEDG}	Hall Enable deglitch time	During power up		1.4		µs
CYCLE-BY-CYCLE CURRENT LIMIT						
I_{LIMIT}	Current limit	R_{ILIMIT} = 18 kΩ	0.46	0.5	0.59	A
		R_{ILIMIT} = 9 kΩ	0.91	1	1.13	A
		R_{ILIMIT} = 6 kΩ	1.37	1.5	1.66	A
t_{BLANK}	Cycle by cycle current limit blank time			5.0		µs
ADVANCE ANGLE						
θ_{ADV}	Advance Angle Setting (SPI Device)	ADVANCE_LVL = 000 b		0	1	°
		ADVANCE_LVL = 001 b	3	4	5	°
		ADVANCE_LVL = 010 b	6	7	8	°
		ADVANCE_LVL = 011 b	10	11	12	°
		ADVANCE_LVL = 100 b	13.5	15	16.5	°
		ADVANCE_LVL = 101 b	18	20	22	°
		ADVANCE_LVL = 110 b	22.5	25	27.5	°
		ADVANCE_LVL = 111 b	27	30	33	°
θ_{ADV}	Advance Angle Setting (HW Device)	ADVANCE pin tied to AGND		0	1	°
		ADVANCE pin tied to 22 kΩ ± 5% to AGND	3	4	5	°
		ADVANCE pin tied to 100 kΩ ± 5% to AGND	10	11	12	°
		ADVANCE pin tied to Hi-Z	13.5	15	16.5	°
		ADVANCE pin tied to 100 kΩ ± 5% to AVDD	18	20	22	°
		ADVANCE pin tied to 22 kΩ ± 5% to AVDD	22.5	25	27.5	°
		ADVANCE pin tied to Tied to AVDD	27	30	33	°
PROTECTION CIRCUITS						
V_{UVLO}	VM supply undervoltage lockout (UVLO)	VM falling	4.25	4.35	4.48	V
		VM rising	4.42	4.6	4.75	V
V_{UVLO_HYS}	VM supply undervoltage lockout hysteresis	Rising to falling threshold	130	210	260	mV
t_{UVLO}	VM supply undervoltage deglitch time		3	5	7	µs

ADVANCE INFORMATION

T_J = –40°C to +150°C, V_{VM} = 5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OVP}	Supply overvoltage protection (OVP) (SPI Device)	Supply rising, OVP_EN = 1, OVP_SEL = 0	32.5	34	35	V
		Supply falling, OVP_EN = 1, OVP_SEL = 0	31.8	33	34.3	V
		Supply rising, OVP_EN = 1, OVP_SEL = 1	20	22	23	V
		Supply falling, OVP_EN = 1, OVP_SEL = 1	19	21	22	V
V_{OVP_HYS}	Supply overvoltage protection hysteresis (SPI Device)	Rising to falling threshold, OVP_SEL = 1	0.9	1	1.1	V
		Rising to falling threshold, OVP_SEL = 0	0.65	0.8	0.9	V
V_{OVP}	Supply overvoltage protection (OVP) (HW Device)	Supply rising	32.5	34	35	V
		Supply falling	31.8	33	34.3	V
V_{OVP_HYS}	Supply overvoltage protection hysteresis (HW Device)	Rising to falling threshold	0.65	0.8	0.9	V
t_{OVP}	Supply overvoltage deglitch time		2.5	5	7	µs
V_{CPUV}	Charge pump undervoltage lockout (above VM)	Supply rising	2.2	2.5	2.8	V
		Supply falling	2.1	2.4	2.7	V
V_{CPUV_HYS}	Charge pump UVLO hysteresis	Rising to falling threshold	75	100	140	mV
V_{AVDD_UV}	Analog regulator undervoltage lockout	Supply falling	3	3.1	3.3	V
		Supply rising	3.2	3.3	3.47	V
$V_{AVDD\_UV\_HYS}$	Analog regulator undervoltage lockout hysteresis	Rising to falling threshold	150	200	255	mV
I_{OCP}	Overcurrent protection trip point		2.25	3.25	4.25	A
t_{OCP}	Overcurrent protection deglitch time (SPI Device)	OCP_DEG = 00b	0.02	0.2	0.4	µs
		OCP_DEG = 01b	0.2	0.6	1.2	µs
		OCP_DEG = 10b	0.5	1.2	1.8	µs
		OCP_DEG = 11b	0.9	1.6	2.5	µs
	Overcurrent protection deglitch time (HW Device)		0.2	0.6	1.2	µs
t_{RETRY}	Overcurrent protection retry time (SPI Device)	OCP_RETRY = 0	4	5	6	ms
		OCP_RETRY = 1	425	500	575	ms
t_{PWM_LOW}	PWM low time required for motor lock detection			200		ms
t_{MTR_LOCK}	Motor lock detection time (SPI Device)	MOTOR_LOCK_TDET = 00b	270	300	330	ms
		MOTOR_LOCK_TDET = 01b	450	500	550	ms
		MOTOR_LOCK_TDET = 10b	900	1000	1100	ms
		MOTOR_LOCK_TDET = 11b	4500	5000	5500	ms
t_{MTR_LOCK}	Motor lock detection time (HW Device)	FGSEL/LOCK_DET_TIME pin tied to AGND or tied to 100 kΩ ± 5% to AVDD	270	300	330	ms
		FGSEL/LOCK_DET_TIME pin tied to 22 kΩ ± 5% to AGND or tied to 22 kΩ ± 5% to AVDD	450	500	550	ms
		FGSEL/LOCK_DET_TIME pin tied to 100 kΩ ± 5% to AGND or tied to AVDD	900	1000	1100	ms
		FGSEL/LOCK_DET_TIME pin floating (HiZ)	4500	5000	5500	ms
$t_{MTR\_LOCK\_RETRY}$	Motor lock retry time (SPI Device)	MOTOR_LOCK_RETRY = 0b	450	500	550	ms
		MOTOR_LOCK_RETRY = 1b	4500	5000	5500	ms

ADVANCE INFORMATION

T_J = –40°C to +150°C, V_{VM} = 5 to 35 V (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 24 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{MTR\_LOCK\_RETRY}$	Motor lock retry time (HW Device)		450	500	550	ms
T_{OTW_LDO}	Thermal shutdown temperature	Die temperature (T_J)	147	171	184	°C
$T_{OTW\_LDO\_HYS}$	Thermal shutdown hysteresis	Die temperature (T_J)	15	20	25	°C
T_{OTW_FET}	Thermal warning temperature	Die temperature (T_J)	132	145	158	°C
$T_{OTW\_FET\_HYS}$	Thermal warning hysteresis	Die temperature (T_J)	15	20	25	°C
T_{TSD_FET}	Thermal shutdown temperature (FET)	Die temperature (T_J)	150	165	178	°C
$T_{TSD\_FET\_HYS}$	Thermal shutdown hysteresis (FET)	Die temperature (T_J)	17	18	19	°C

(1) Effective capacitance including variations due to DC bias, temperature, manufacturing tolerance, etc.

6.6 SPI Timing Requirements

		MIN	NOM	MAX	UNIT
t_{READY}	SPI ready after power up			1	ms
t_{HI_nSCS}	nSCS minimum high time	300			ns
t_{SU_nSCS}	nSCS input setup time	25			ns
t_{HD_nSCS}	nSCS input hold time	25			ns
t_{SCLK}	SCLK minimum period	100			ns
t_{SCLKH}	SCLK minimum high time	50			ns
t_{SCLKL}	SCLK minimum low time	50			ns
t_{SU_SDI}	SDI input data setup time	25			ns
t_{HD_SDI}	SDI input data hold time	25			ns
t_{DLY_SDO}	SDO output data delay time			30	ns
t_{EN_SDO}	SDO enable delay time			50	ns
t_{DIS_SDO}	SDO disable delay time			50	ns

6.7 SPI Secondary Device Mode Timings

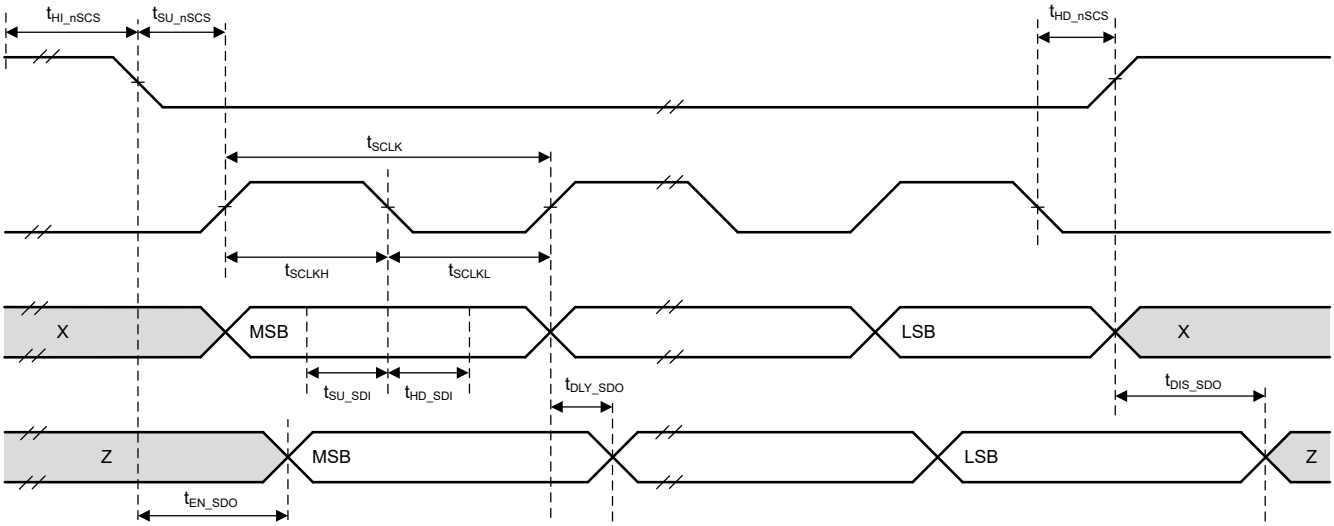

図 6-1. SPI Secondary Device Mode Timing Diagram

ADVANCE INFORMATION

7 Detailed Description

7.1 Overview

The MCT8314Z device is an integrated 575-mΩ (combined high-side and low-side MOSFET's on-state resistance) driver for 3-phase motor-drive applications. The device reduces system component count, cost, and complexity by integrating three half-bridge MOSFETs, gate drivers, a charge pump, and a linear regulator for the external load. A standard serial peripheral interface (SPI) provides a simple method for configuring the various device settings and reading fault diagnostic information through an external controller. Alternatively, a hardware interface (H/W) option allows for configuring the most commonly used settings through fixed external resistors.

The MCT8314Z device architecture uses an internal state machine to protect against short-circuit events, and protect against dv/dt parasitic turnon of the internal power MOSFET. The device also integrates a three-phase sensored trapezoidal commutation state machine using analog or digital hall sensors for position detection.

In addition to the high level of device integration, the MCT8314Z device provides a wide range of integrated protection features. These features include power-supply Undervoltage lockout (UVLO), charge-pump Undervoltage lockout (CPUV), overcurrent protection (OCP), AVDD Undervoltage lockout (AVDD_UV), and overtemperature shutdown (OTW and OTSD). Fault events are indicated by the nFAULT pin with detailed information available in the SPI registers on the SPI device version.

The MCT8314ZZS and MCT8314ZZH devices are available in 0.4-mm pin pitch, WQFN surface-mount packages. The WQFN package size is 3 mm × 3 mm.

7.2 Functional Block Diagram

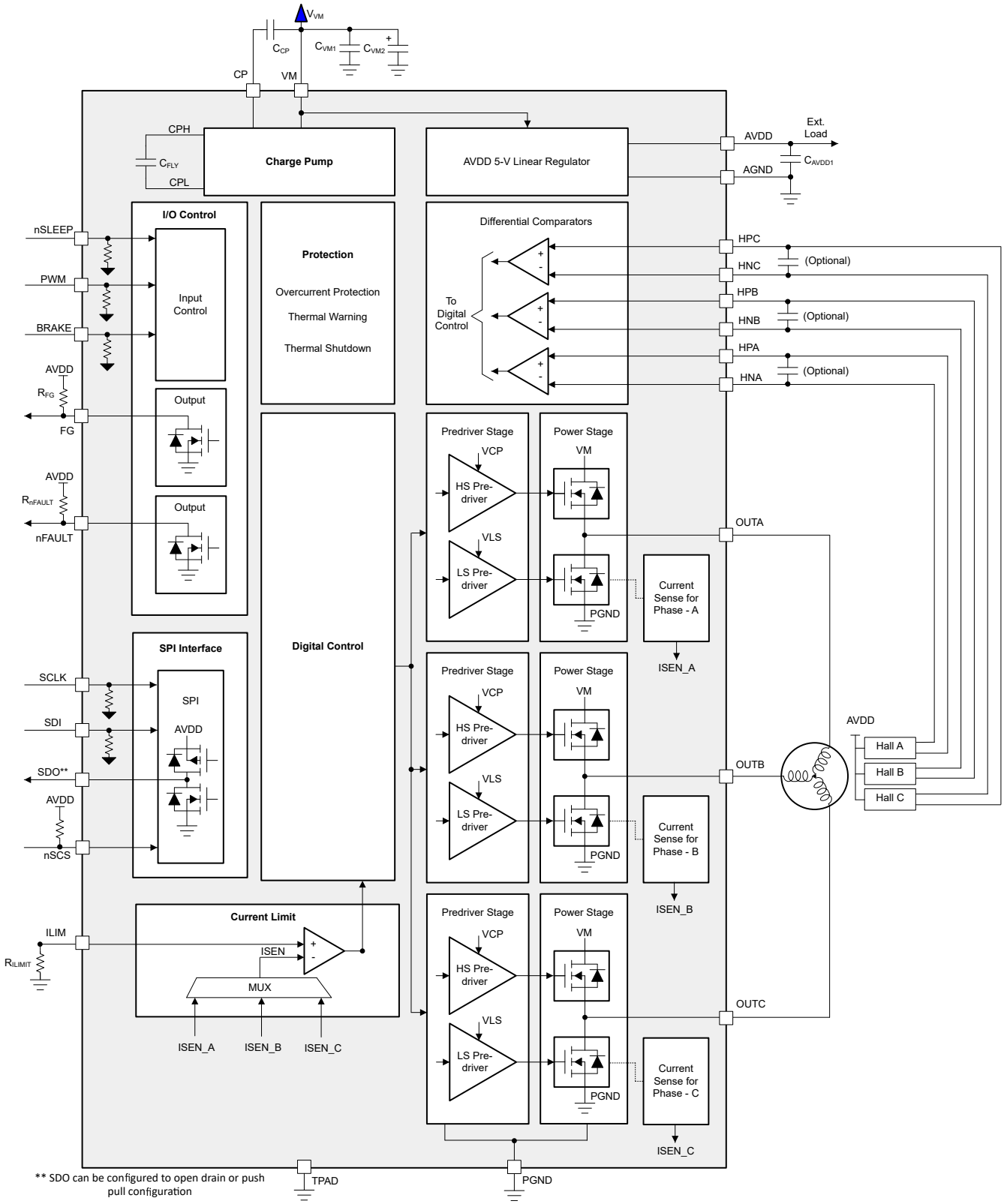

図 7-1. MCT8314ZS Block Diagram

ADVANCE INFORMATION

ADVANCE INFORMATION

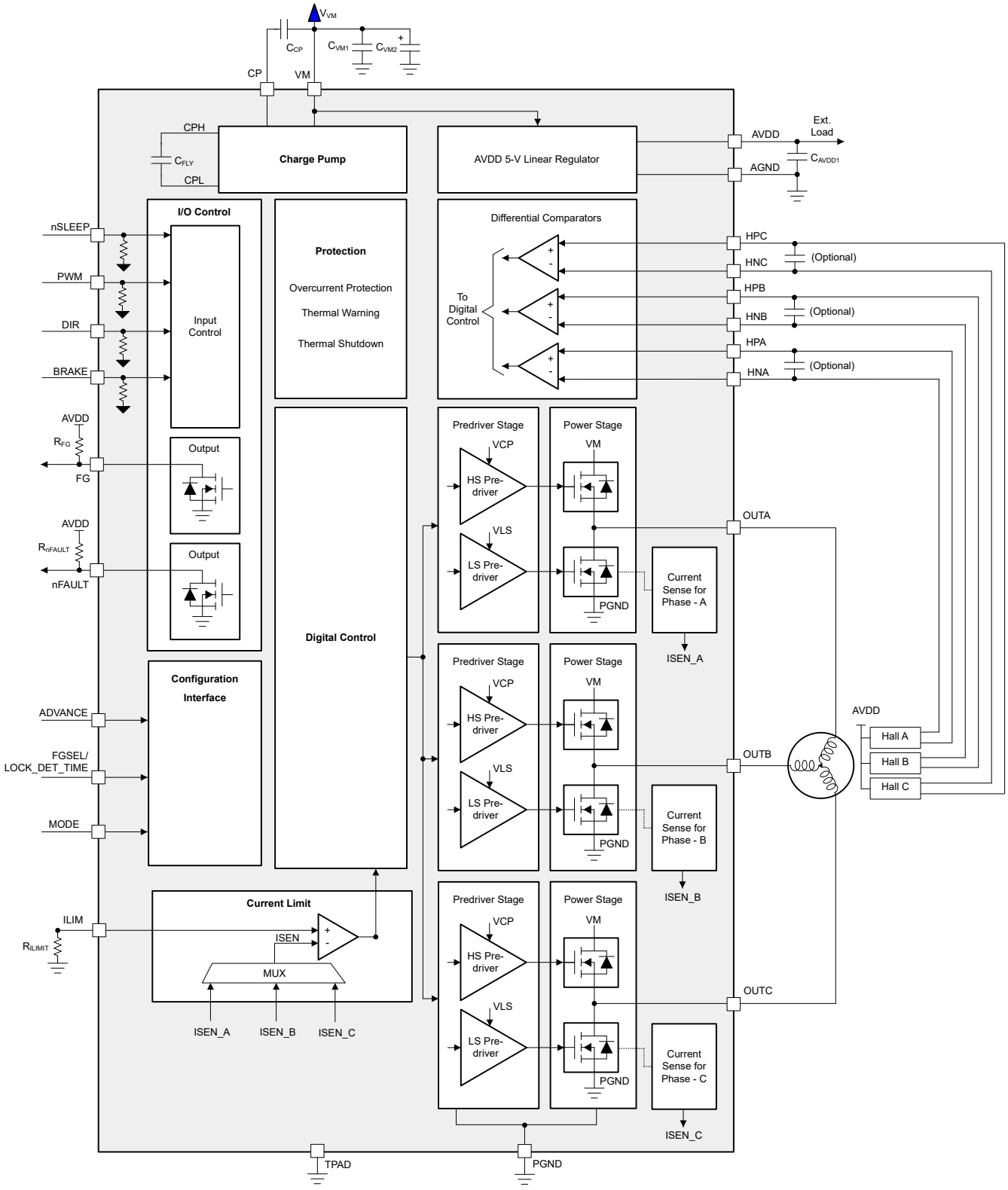

図 7-2. MCT8314ZH Block Diagram

7.3 Feature Description

表 7-1 lists the recommended values of the external components for the driver.

表 7-1. MCT8314Z External Components

COMPONENTS	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	PGND	X5R or X7R, 0.1-µF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device
C_{VM2}	VM	PGND	≥ 10-µF, TI recommends a capacitor voltage rating at least twice the normal operating voltage of the device
C_{CP}	CP	VM	X5R or X7R, ≥16-V, 0.22-µF capacitor
C_{AVDD}	AVDD	AGND	X5R or X7R, 2.2-µF, ≥16-V capacitor. In order for AVDD to accurately regulate output voltage, capacitor should have effective capacitance between 0.7-µF to 2.64-µF at 5 V across operating temperature.
R_{nFAULT}	VCC	nFAULT	5.1-kΩ, Pullup resistor
R_{FG}	VCC	FG	5.1-kΩ, Pullup resistor
R_{SDO}	VCC	SDO	5.1-kΩ, Pullup resistor
R_{MODE}	MODE	AGND or AVDD	MCT8314ZH hardware interface
$R_{ADVANCE}$	ADVANCE	AGND or AVDD	MCT8314ZH hardware interface
R_{LOCK}	FGSEL/LOCK_DET_TIME	AGND	MCT8314ZH hardware interface
R_{ILIMIT}	ILIM	AGND	See セクション 7.3.11

7.3.1 Output Stage

The MCT8314Z device consists of an integrated 575-mΩ (combined high-side and low-side FET's on-state resistance) NMOS FETs connected in a three-phase bridge configuration. A doubler charge pump provides the proper gate-bias voltage to the high-side NMOS FETs across a wide operating voltage range in addition to providing 100% duty-cycle support. An internal linear regulator provides the gate-bias voltage for the low-side MOSFETs. The device has three VM motor power-supply pins which are to be connected to the motor-supply voltage.

7.3.2 PWM Control Mode (1x PWM Mode)

The MCT8314Z family of devices provides seven different control modes to support various commutation and control methods. The MCT8314Z device provides a 1x PWM control mode for driving the BLDC motor in trapezoidal current-control mode. The MCT8314Z device uses 6-step block commutation tables that are stored internally. This feature lets a three-phase BLDC motor be controlled using a single PWM sourced from a simple controller. The PWM is applied on the PWM pin and determines the output frequency and duty cycle of the half-bridges.

The MCT8314Z family of devices supports both analog and digital hall inputs by changing mode input setting. Differential hall inputs should be connected to HPx and HNx pins (see 図 7-3). Digital hall inputs should be connected to the HPx pins while keeping the HNx pins floating (see 図 7-4).

The half-bridge output states are managed by the HPA, HNA, HPB, HNB, HPC and HNC pins in analog mode and HPA, HPB, HPC in digital mode which are used as state logic inputs. The state inputs are the position feedback of the BLDC motor. The 1x PWM mode usually operates with synchronous rectification (low-side MOSFET recirculation); however, the mode can be configured to use asynchronous rectification (MOSFET body diode freewheeling) as shown in 表 7-2.

ADVANCE INFORMATION

表 7-2. PWM mode Configuration

MODE Type	MODE Pin (Hardware Variant)	Hall Configuration	Modulation	ASR configuration	ASR Mode	Comment
Mode 1	Connected to AGND	Analog Hall Input	Asynchronous	EN_ASR = 0	ASR Disabled	TI recommends to operate Pre-Production MCT8314ZH in Mode 3 and Mode 4 only.
Mode 2	Connected to AGND with R_{MODE1}	Digital Hall Input				
Mode 3	Connected to AGND with R_{MODE2}	Analog Hall Input	Synchronous			
Mode 4	Hi-Z	Digital Hall Input				
Mode 5	Connected to AVDD with R_{MODE2}	Analog Hall Input		EN_ASR = 1	ASR Enabled	
Mode 6	Connected to AVDD with R_{MODE1}	Digital Hall Input				
Mode 7	Connected to AVDD					

注

Texas Instruments does not recommend changing the MODE pin or PWM_MODE register during operation of the power MOSFETs. Set PWM to a low level before changing the MODE pin or PWM_MODE register.

7.3.2.1 Analog Hall Input Configuration

図 7-3 shows the connection of analog Hall inputs to the driver. Analog Hall elements are fed to the Hall comparators, which zero crossing is used to generate the commutation logic.

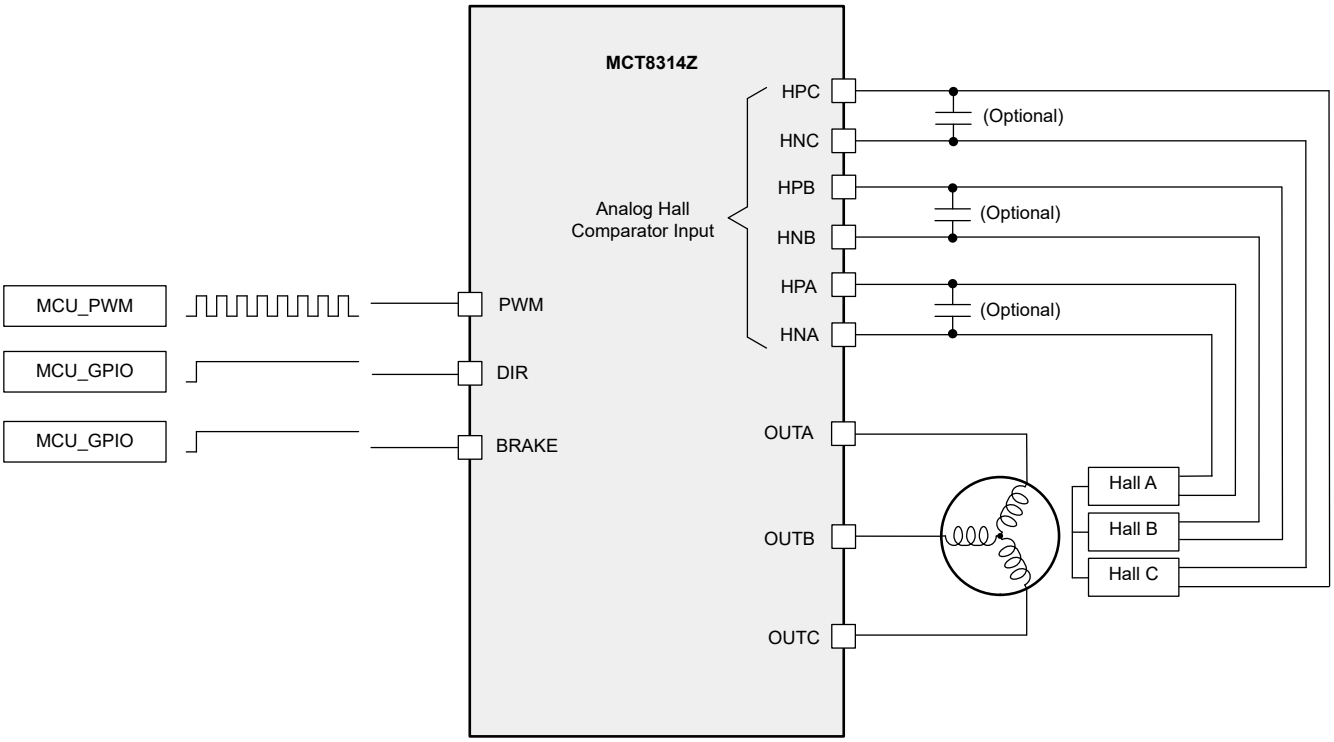

図 7-3. 1x PWM Mode with Analog Hall Input

7.3.2.2 Digital Hall Input Configuration

図 7-4 shows the connection of digital Hall inputs to the driver.

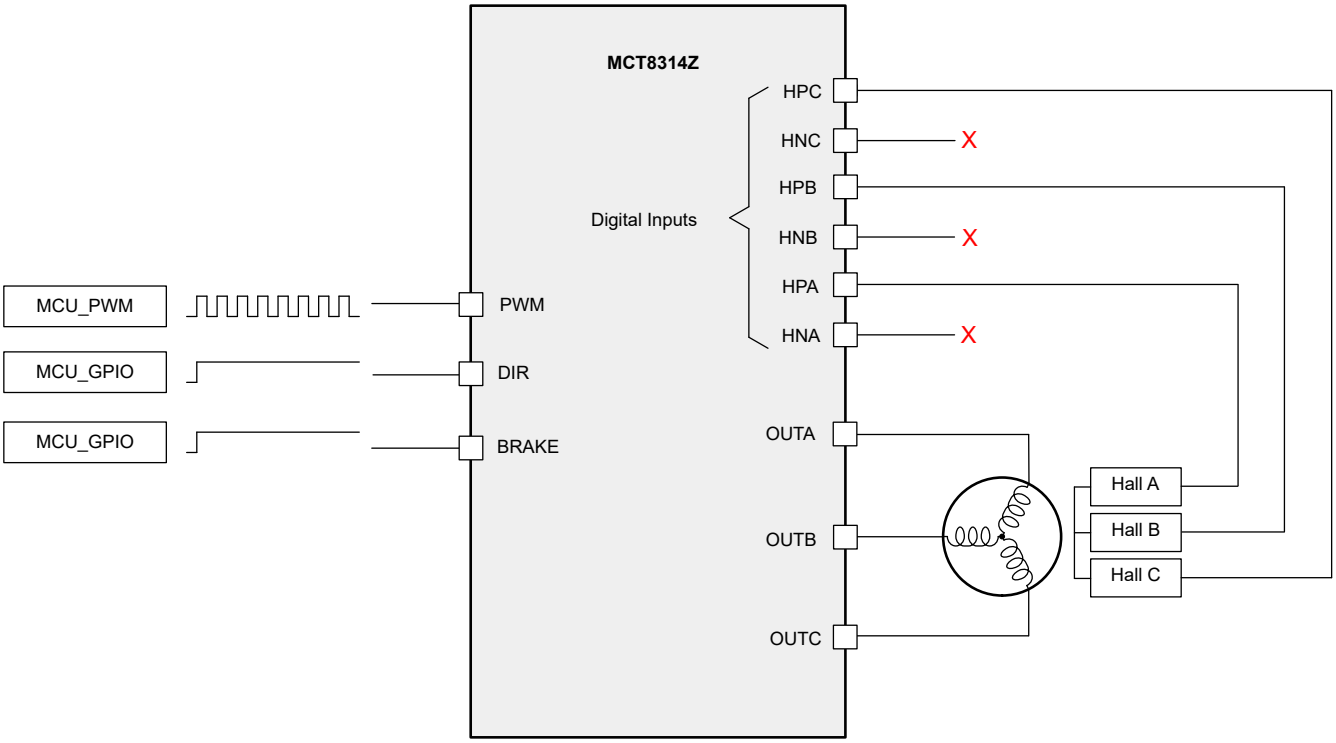

図 7-4. 1x PWM Mode with Digital Hall Input

7.3.2.3 Asynchronous Modulation

The DIR pin controls the direction of BLDC motor in either clockwise or counter-clockwise direction. Tie the DIR pin low if this feature is not required.

The BRAKE input halts the motor by turning off all high-side MOSFETs and turning on all low-side MOSFETs when it is pulled high. This brake is independent of the states of the other input pins. Tie the BRAKE pin low if this feature is not required.

表 7-3 shows the configuration in 1x PWM mode with asynchronous modulation.

表 7-3. Asynchronous Modulation

HALL INPUTS							DRIVER OUTPUTS						
STATE	DIR = 0			DIR = 1			PHASE A		PHASE B		PHASE C		DESCRIPTION
	HALL_A /HPA	HALL_B /HPB	HALL_C /HPC	HALL_A /HPA	HALL_B /HPB	HALL_C /HPC	High Side	Low Side	High Side	Low Side	High Side	Low Side	
Stop	0	0	0	0	0	0	L	L	L	L	L	L	Stop
	1	1	1	1	1	1							
1	1	1	0	0	0	1	L	L	PWM	L	L	H	B → C
2	1	0	0	0	1	1	PWM	L	L	L	L	H	A → C
3	1	0	1	0	1	0	PWM	L	L	H	L	L	A → B
4	0	0	1	1	1	0	L	L	L	H	PWM	L	C → B
5	0	1	1	1	0	0	L	H	L	L	PWM	L	C → A
6	0	1	0	1	0	1	L	H	PWM	L	L	L	B → A

ADVANCE INFORMATION

注

Texas Instruments recommends not to operate the pre-production MCT8314ZH in Asynchronous modulation as this can overstress the device

ADVANCE INFORMATION

7.3.2.4 Synchronous Modulation

表 7-4 shows the configuration in 1x PWM mode with synchronous modulation.

表 7-4. Synchronous Modulation

HALL INPUTS							DRIVER OUTPUTS						
STATE	DIR = 0			DIR = 1			PHASE A		PHASE B		PHASE C		DESCRIPTION
	HALL_A /HPA	HALL_B /HPB	HALL_C /HPC	HALL_A /HPA	HALL_B /HPB	HALL_C /HPC	High Side	Low Side	High Side	Low Side	High Side	Low Side	
Stop	0	0	0	0	0	0	L	L	L	L	L	L	Stop
	1	1	1	1	1	1							
1	1	1	0	0	0	1	L	L	PWM	!PWM	L	H	B → C
2	1	0	0	0	1	1	PWM	!PWM	L	L	L	H	A → C
3	1	0	1	0	1	0	PWM	!PWM	L	H	L	L	A → B
4	0	0	1	1	1	0	L	L	L	H	PWM	!PWM	C → B
5	0	1	1	1	0	0	L	H	L	L	PWM	!PWM	C → A
6	0	1	0	1	0	1	L	H	PWM	!PWM	L	L	B → A

7.3.2.5 Motor Operation

図 7-5 and 図 7-6 shows the BLDC motor commutation with direction setting DIR (bit or pin) as 0 and 1 respectively.

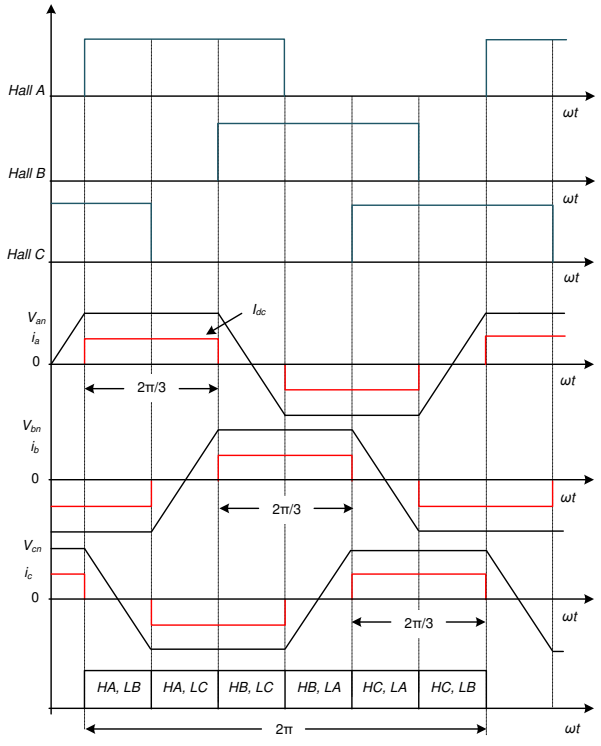

図 7-5. BLDC Motor Commutation with DIR = 0

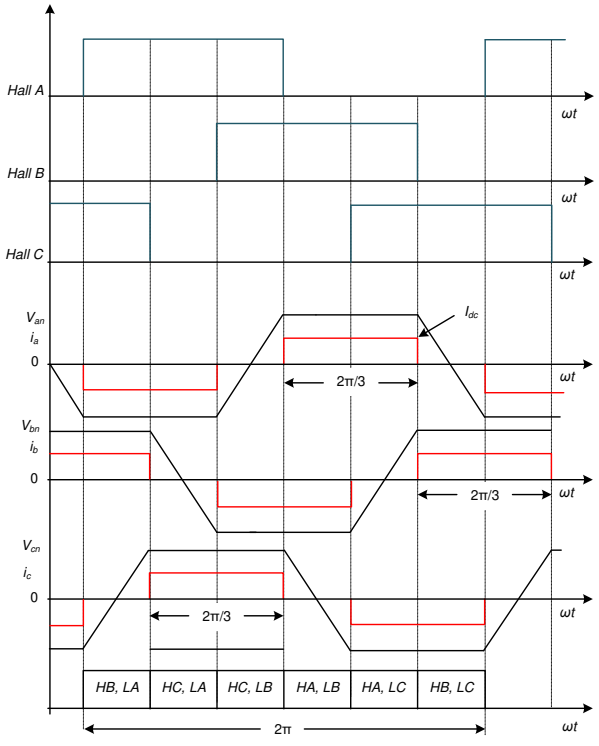

図 7-6. BLDC Motor Commutation with DIR = 1

注

Texas Instruments recommends motor direction (DIR) change when the motor is stationary.

ADVANCE INFORMATION

7.3.3 Device Interface Modes

The MCT8314Z family of devices supports two different interface modes (SPI and hardware) to let the end application design for either flexibility or simplicity (図 7-7 and 図 7-8). The two interface modes share the same four pins, allowing the different versions to be pin-to-pin compatible. This compatibility lets application designers evaluate with one interface version and potentially switch to another with minimal modifications to their design.

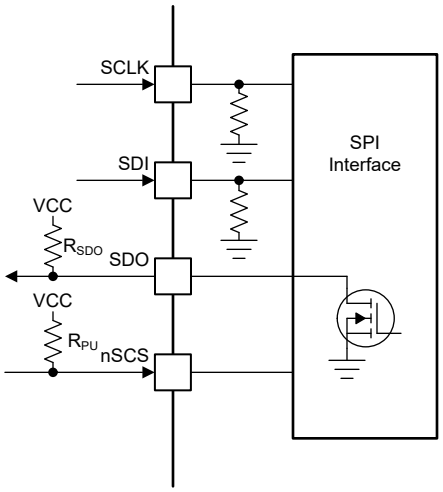

図 7-7. MCT8314ZZS SPI Interface

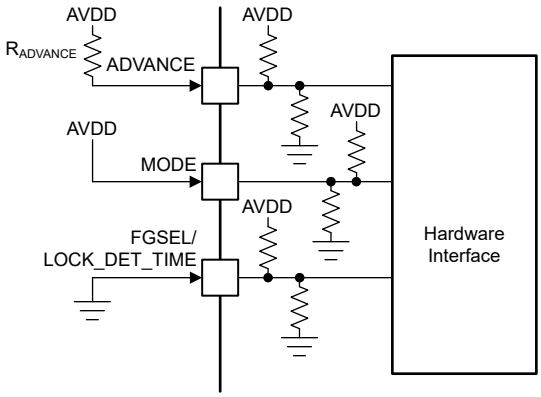

図 7-8. MCT8314ZZH Hardware Interface

7.3.3.1 Serial Peripheral Interface (SPI)

The SPI devices support a serial communication bus that lets an external controller send and receive data with the MCT8314Z. This variant lets the external controller configure device settings and read detailed fault information. The interface is a four wire interface using the SCLK, SDI, SDO, and nSCS pins which are described as follows:

- The SCLK pin is an input that accepts a clock signal to determine when data is captured and propagated on the SDI and SDO pins.
- The SDI pin is the data input.
- The SDO pin is the data output. The SDO pin can be configured to either open-drain or push-pull through SDO_MODE.
- The nSCS pin is the chip select input. A logic low signal on this pin enables SPI communication with the MCT8314Z. Placing an option pull-up resistor on this pin helps to avoid accidental SPI communication during power cycling on the controller or the driver.

For more information on the SPI, see the *セクション 7.5* section.

7.3.3.2 Hardware Interface

Hardware interface devices use three resistor-configurable inputs (in the place of SPI pins) which are ADVANCE, MODE, and FGSEL/LOCK_DET_TIME. This variant lets the application designer configure the most common device settings by tying the pin logic high or logic low, or with a simple pullup or pulldown resistor. This removes the requirement for an SPI bus from the external controller. General fault information can still be obtained through the nFAULT pin.

- The MODE pin configures the PWM control mode.
- The ADVANCE pin configures the lead angle of the output with respect to hall signals.
- The FGSEL/LOCK_DET_TIME pin configures the electrical frequency generation output mode and t_{MTR_LOCK}.

For more information on the hardware interface, see the *セクション 7.3.9* section.

7.3.4 AVDD Linear Voltage Regulator

A 5-V linear regulator is integrated into the MCT8314Z family of devices and is available for use by external circuitry. The AVDD regulator is used for powering up the internal digital circuitry of the device and additionally, this regulator can also provide the supply voltage for a low-power MCU or other circuitry supporting low current (up to 30 mA). The output of the AVDD regulator should be bypassed near the AVDD pin with a X5R or X7R, 2.2-µF, 10-V ceramic capacitor routed directly back to the adjacent AGND ground pin. The AVDD nominal, no-load output voltage is 5 V.

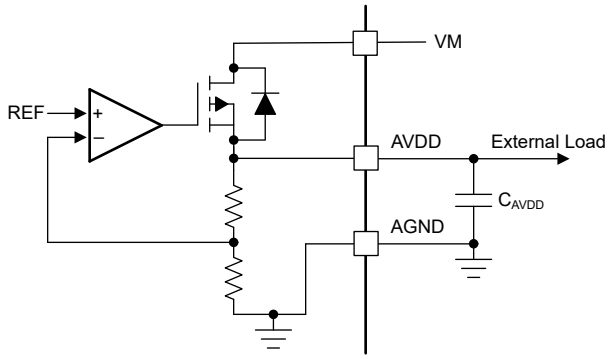

図 7-9. AVDD Linear Regulator Block Diagram

Use 式 1 to calculate the power dissipated in the device by the AVDD linear regulator with VM as supply.

$$P = (V_{VM} - V_{AVDD}) \times I_{AVDD} \quad (1)$$

For example, at a V_{VM} of 24 V, drawing 20 mA out of AVDD results in a power dissipation as shown in 式 2.

$$P = (24\ V - 5\ V) \times 20\ mA = 380\ mW \quad (2)$$

ADVANCE INFORMATION

7.3.5 Charge Pump

Because the output stages use N-channel FETs, the device requires a gate-drive voltage higher than the VM power supply to enhance the high-side FETs fully. The MCT8314Z integrates a charge-pump circuit that generates a voltage above the VM supply for this purpose. The charge pump requires one external capacitor, C_{CP}, for operation. Use a X5R or X7R, 220-nF, 16-V ceramic capacitor for C_{CP} and place it near the VM and CP pins. The charge pump shuts down when nSLEEP is low.

7.3.6 Slew Rate

The slew rate of each half-bridge is 200-V/µs. The slew rate is calculated by the rise time and fall time of the voltage on OUTx pin as shown in 図 7-10.

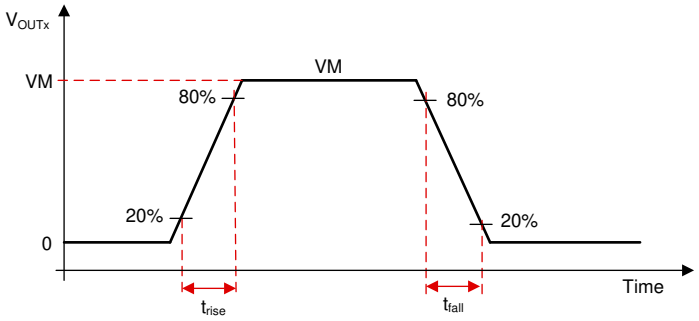

図 7-10. Slew Rate Timings

7.3.7 Cross Conduction (Dead Time)

The device is fully protected for any cross conduction of MOSFETs. In half-bridge configuration, the operation of high-side and low-side MOSFETs are ensured to avoid any shoot-through currents by inserting a dead time (t_{dead}). This is implemented by sensing the gate-source voltage (V_{GS}) of the high-side and low-side MOSFETs and ensuring that V_{GS} of high-side MOSFET has reached below turn-off levels before switching on the low-side MOSFET of same half-bridge as shown in 図 7-11 and 図 7-12.

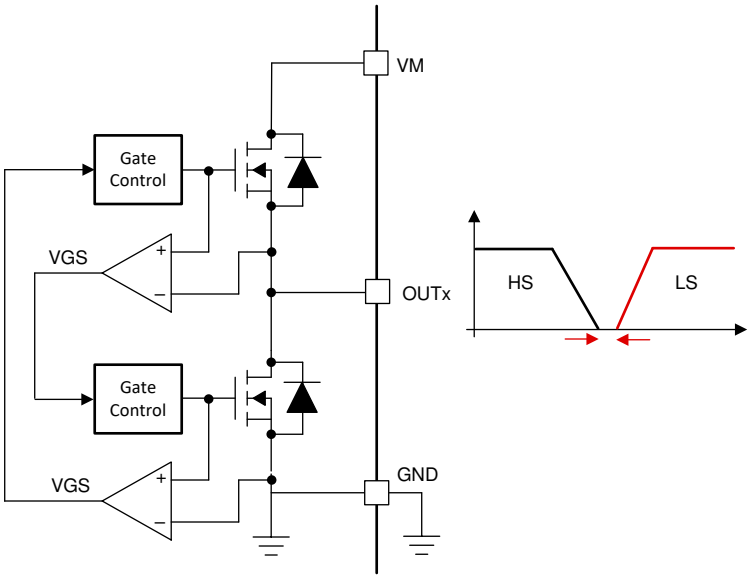

図 7-11. Cross Conduction Protection

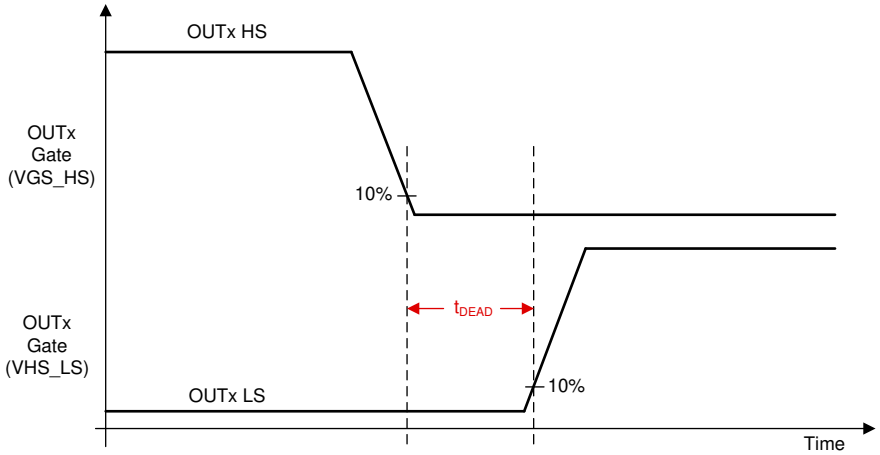

図 7-12. Dead Time

ADVANCE INFORMATION

7.3.8 Propagation Delay

The propagation delay time (t_{pd}) is measured as the time between an input logic edge to change in gate driver voltage. This time has three parts consisting of the digital input deglitcher delay, analog driver, and comparator delay.

The input deglitcher prevents high-frequency noise on the input pins from affecting the output state of the gate drivers. To support multiple control modes, a small digital delay is added as the input command propagates through the device.

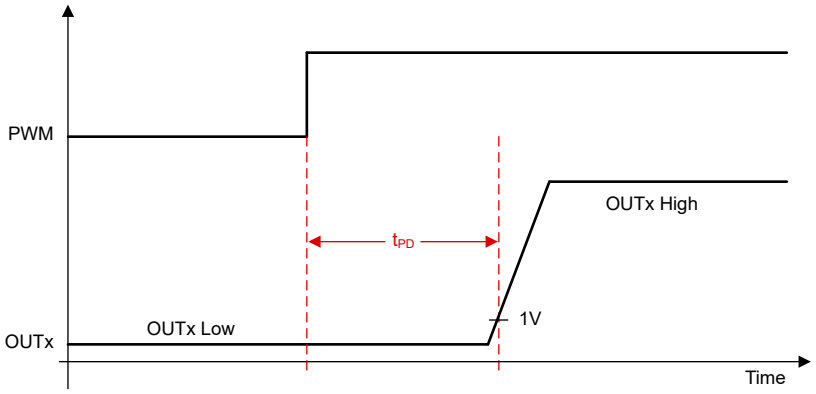

図 7-13. Propagation Delay Timing

7.3.9 Pin Diagrams

This section presents the I/O structure of all digital input and output pins.

7.3.9.1 Logic Level Input Pin (Internal Pulldown)

図 7-14 shows the input structure for the logic level pins: BRAKE, DIR, nSLEEP, PWM, SCLK and SDI. The input can be with a voltage or external resistor. It is recommended to put these pins low in device sleep mode to reduce leakage current through internal pull-down resistors.

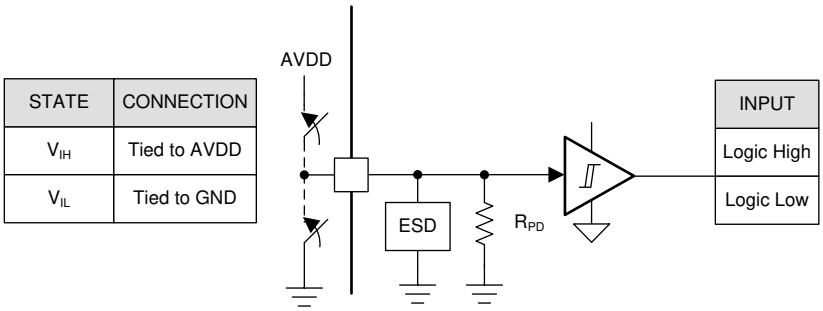

図 7-14. Logic-Level Input Pin Structure

7.3.9.2 Logic Level Input Pin (Internal Pullup)

図 7-15 shows the input structure for the logic level pin, nSCS. The input can be driven with a voltage or external resistor.

ADVANCE INFORMATION

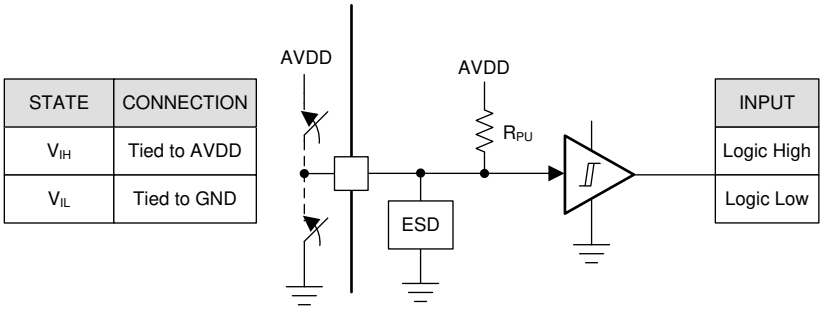

図 7-15. Logic nSCS

7.3.9.3 Open Drain Pin

図 7-16 shows the structure of the open-drain output pins, nFAULT, FG, and SDO in open drain mode. The open-drain output requires an external pullup resistor to function properly.

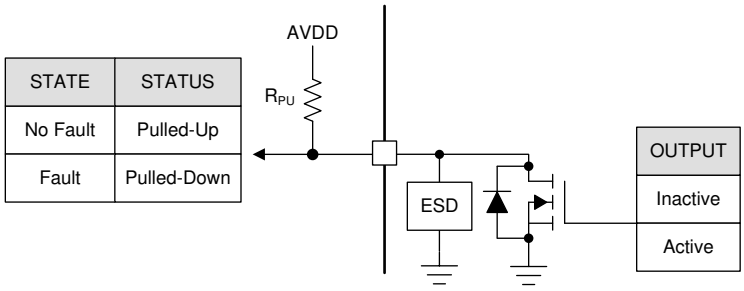

図 7-16. Open Drain

7.3.9.4 Push Pull Pin

図 7-17 shows the structure of SDO in push-pull mode.

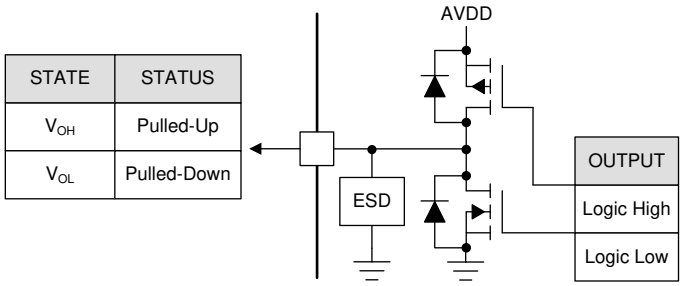

図 7-17. Push Pull

ADVANCE INFORMATION

7.3.9.5 Seven Level Input Pin

図 7-18 shows the structure of the seven level input pins, ADVANCE and MODE, on hardware interface devices. The input can be set with an external resistor.

STATE	RESISTANCE
V_{L1}	Tied to AGND
V_{L2}	22 kΩ ± 5% to AGND
V_{L3}	100 kΩ ± 5% to AGND
V_{L4}	Hi-Z (>2000 kΩ to AGND)
V_{L5}	100 kΩ ± 5% to AVDD
V_{L6}	22 kΩ ±5% to AVDD
V_{L7}	Tied to AVDD

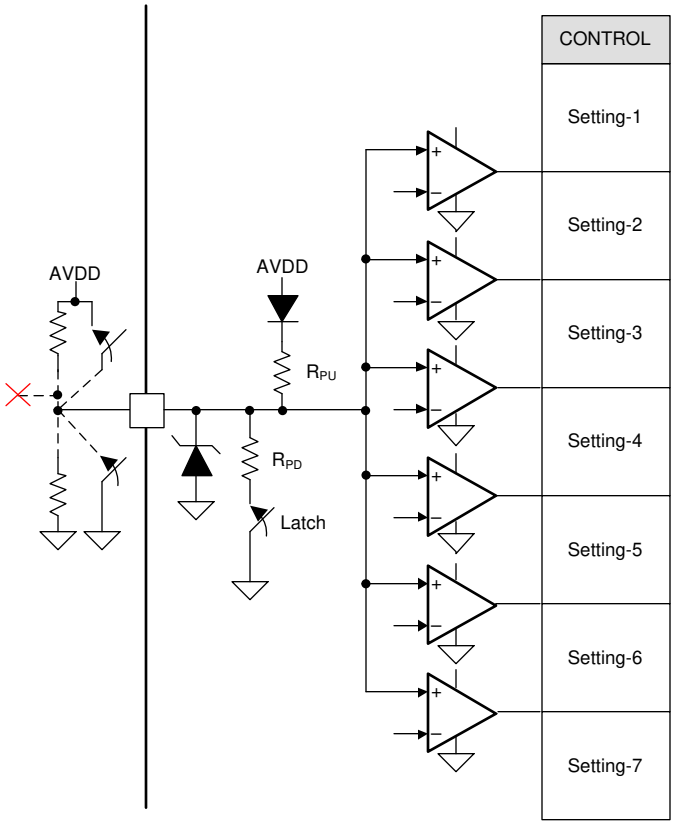

図 7-18. Seven Level Input Pin Structure

7.3.10 Automatic Synchronous Rectification Mode (ASR Mode)

The automatic synchronous rectification (ASR) mode in the MCT8314Z decreases power losses and thermal dissipation by reducing diode conduction losses in the low-side MOSFET. When this feature is enabled, the device automatically turns ON the low-side MOSFET during the PWM OFF time regardless of the device modulation setting. During the PWM OFF time, if the current drops to 0 A, the device automatically disables the MOSFET to avoid back EMF generating negative current in the motor windings. This negative current creates a negative torque on the BLDC motor, and it can reduce performance of low-inductance motors. When ASR mode is enabled, the current during the decay is monitored and the low-side FET is turned off as soon as the current reaches near to zero. This saves the negative current building in the BLDC motor which results in better noise performance and better thermal management. 図 7-19 and 図 7-20 compare asynchronous and synchronous PWM modes with ASR.

ADVANCE INFORMATION

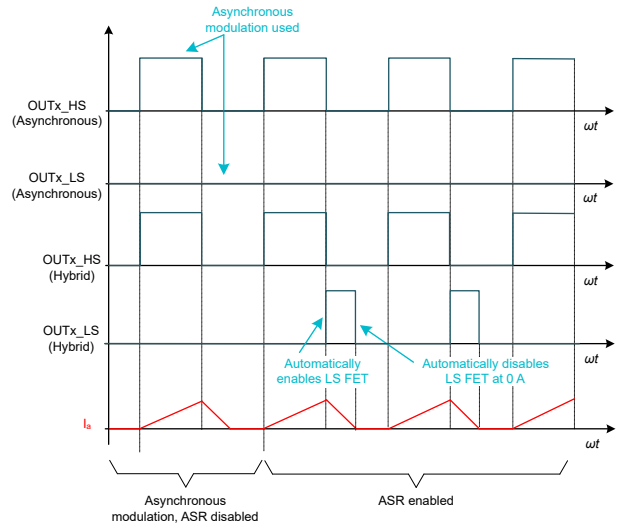

図 7-19. Comparing Asynchronous Modulation and ASR

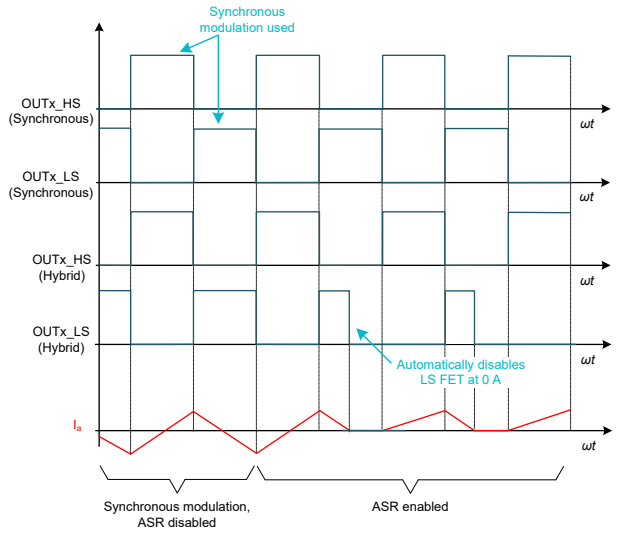

図 7-20. Comparing Synchronous Modulation and ASR

The MCT8314Z device includes a low-side (ASR_LS) comparator which detects the negative flow of current in the device on each low-side MOSFET. The ASR_LS comparator compares the sense-FET output with the ground (0-V) threshold. When the current flows from PGND to OUTx, the ASR_LS comparator trips. This comparator provides a reference point for the operation of the ASR feature.

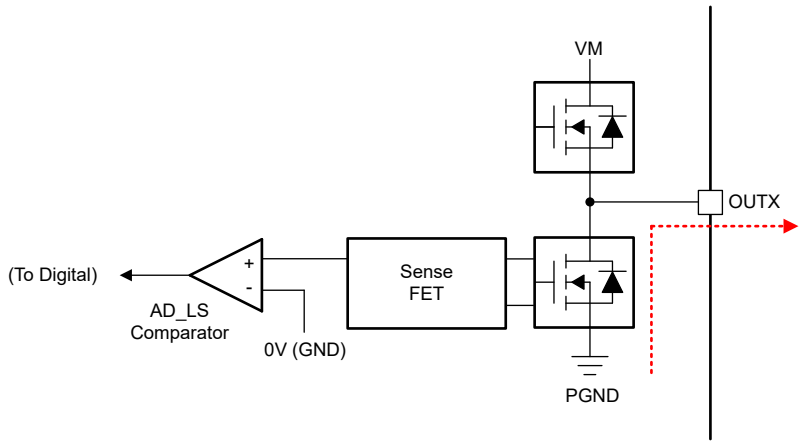

図 7-21. ASR Operation

In the SPI device variant, the EN_ASR bit configures active demagnetization. In the hardware variant, the MODE pin configures active demagnetization as shown in 表 7-5.

表 7-5. PWM_MODE Configuration

MODE Type	MODE Pin (Hardware Variant)	Hall Configuration	Modulation	ASR configuration	ASR Mode	Comment
Mode 1	Connected to AGND	Analog Hall Input	Asynchronous	EN_ASR = 0	ASR Disabled	TI recommends to operate Pre-Production MCT8314ZH in Mode 3 and Mode 4 only.
Mode 2	Connected to AGND with R_{MODE1}	Digital Hall Input				
Mode 3	Connected to AGND with R_{MODE2}	Analog Hall Input	Synchronous			
Mode 4	Hi-Z	Digital Hall Input				
Mode 5	Connected to AVDD with R_{MODE2}	Analog Hall Input		EN_ASR = 1	ASR Enabled	
Mode 6	Connected to AVDD with R_{MODE1}	Digital Hall Input				
Mode 7	Connected to AVDD					

This device does not support smart rectification through the high-side MOSFET. Currents returning to the VM will flow through the high-side body diodes.

注

ASR mode is disabled in pre-production MCT8314ZH devices.

ADVANCE INFORMATION

7.3.11 Cycle-by-Cycle Current Limit

The current-limit circuit activates if the current flowing through the low-side MOSFETs exceeds the I_{LIMIT} current. Large currents may occur during motor start, high torque events, or stall conditions. The current-limit circuitry utilizes the internal sense FETs on the low-side power FETs of the three phases. 図 7-22 shows the implementation of current limit circuitry. The ILIM pin sets the I_{LIMIT} by connecting an R_{LIMIT} from ILIM to AGND. 式 3 calculates the resistor value in Ohms required for a target I_{LIMIT} threshold.

$$R_{LIMIT} = 9000/I_{LIMIT} \quad (3)$$

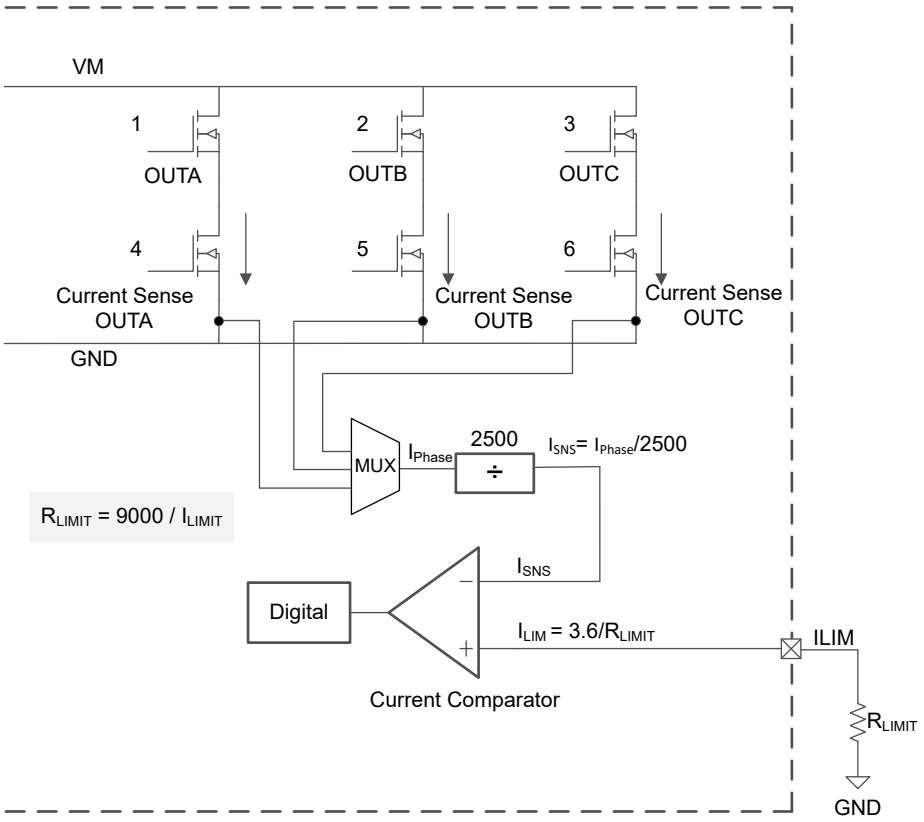

図 7-22. Current Limit Implementation

When the current limit activates, the high-side FETs disable until the beginning of the next PWM cycle as shown in 図 7-23. The low-side FETs can operate in brake mode or coast (high-Z) mode by configuring the ILIM_RECIR bit in the SPI device variant. In the hardware device, the device operates in brake mode when current limiting trips.

ADVANCE INFORMATION

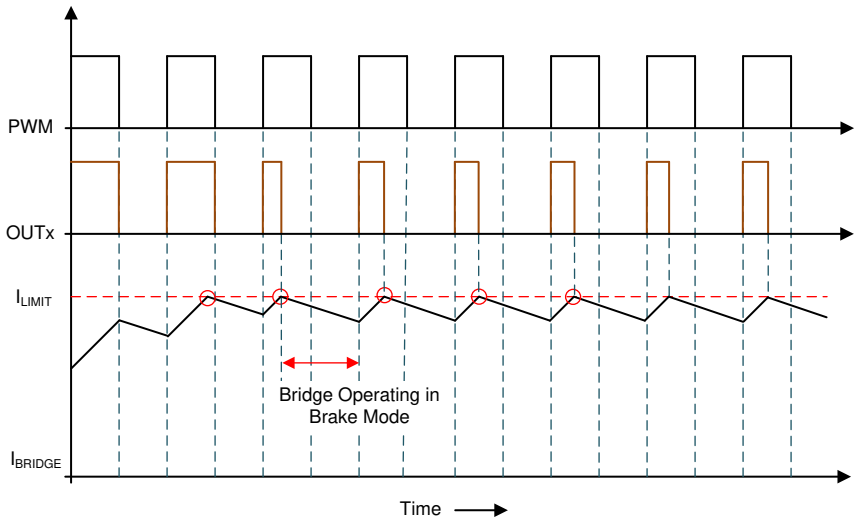

図 7-23. Cycle-by-Cycle Current-Limit Operation

When the current limit activates in synchronous rectification mode, the current recirculates through the low-side FETs while the high-side FETs are disabled as shown in 図 7-24. When the current limit activates in asynchronous rectification mode, the current recirculates through the body diodes of the low-side FETs while the high-side FETs are disabled as shown in 図 7-25

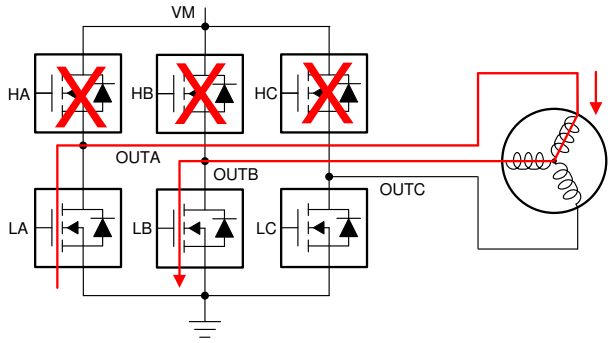

図 7-24. Brake State

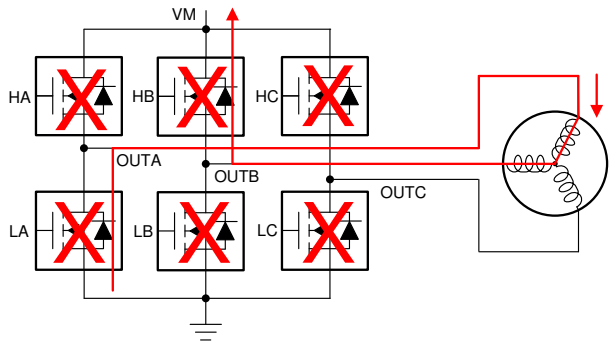

図 7-25. Coast State

注

The current-limit circuit is ignored immediately after the PWM signal goes active for a short blanking time to prevent false trips of the current-limit circuit.

注

During the brake operation, a high-current can flow through the low-side FETs which can eventually trigger the over current protection circuit. This allows the body-diode of the high-side FET to conduct and pump brake energy to the VM supply rail.

ADVANCE INFORMATION

7.3.11.1 Cycle by Cycle Current Limit with 100% Duty Cycle Input

In case of 100% duty cycle applied on PWM input, there is no edge available to turn high-side FET back on. To overcome this problem, MCT8314Z has built in internal PWM clock which is used to turn high-side FET back on once it is disabled after exceeding I_{LIMIT} threshold. In SPI variant MCT8314Z, this internal PWM clock can be configured to either 20 kHz or 40 kHz through PWM_100_DUTY_SEL. In H/W variant MCT8314Z PWM internal clock is set to 20 kHz. 図 7-26 shows operation with 100% duty cycle.

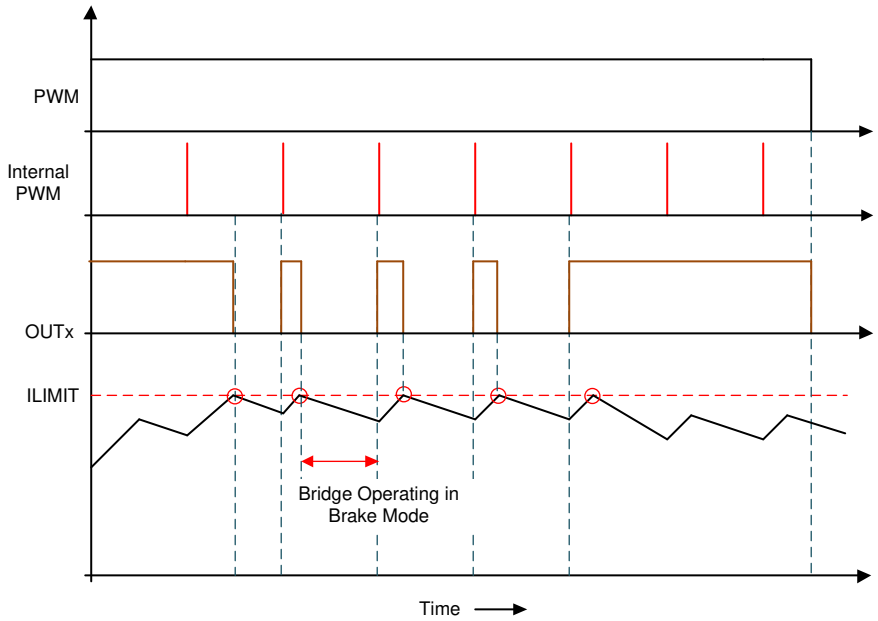

図 7-26. Cycle-by-Cycle Current-Limit Operation with 100% PWM Duty Cycle

7.3.12 Hall Comparators (Analog Hall Inputs)

Three comparators are provided to process the raw signals from the Hall-effect sensors to commutate the motor. The Hall comparators sense the zero crossings of the differential inputs and pass the information to digital logic. The Hall comparators have hysteresis, and their detect threshold is centered at 0 V. The hysteresis is defined as shown in 図 7-27.

In addition to the hysteresis, the Hall inputs are deglitched with a circuit that ignores any extra Hall transitions for a period of t_{HDG} after sensing a valid transition. Ignoring these transitions for the t_{HDG} time prevents PWM noise from being coupled into the Hall inputs, which can result in erroneous commutation.

If excessive noise is still coupled into the Hall comparator inputs, adding capacitors between the positive and negative inputs of the Hall comparators may be required. The ESD protection circuitry on the Hall inputs implements a diode to the AVDD pin. Because of this diode, the voltage on the Hall inputs should not exceed the AVDD voltage.

Because the AVDD pin is disabled in sleep mode (nSLEEP inactive), the Hall inputs should not be driven by external voltages in sleep mode. If the Hall sensors are powered externally, the supply to the Hall sensors should be disabled if the MCT8314Z device is put into sleep mode. In addition, the Hall sensors' power supply should be powered up after enabling the motor otherwise an invalid Hall state may cause a delay in motor operation.

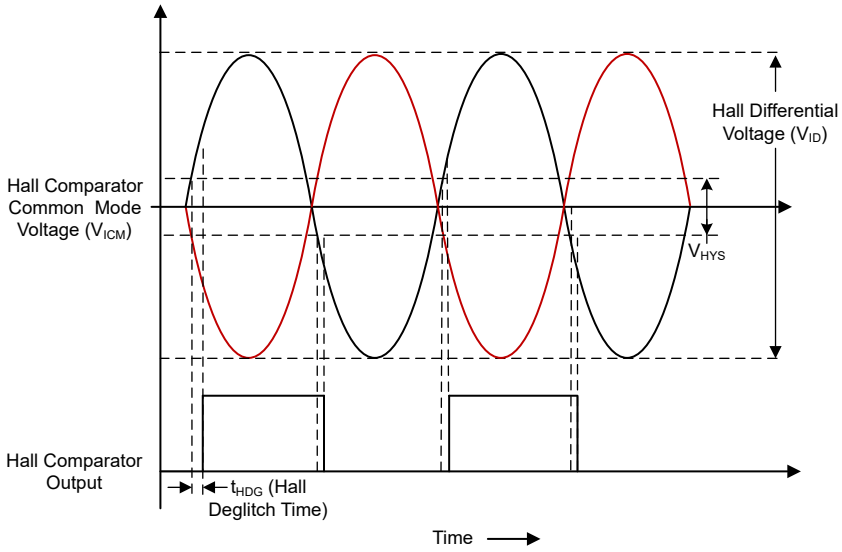

図 7-27. Hall Comparators Operation

ADVANCE INFORMATION

7.3.13 Advance Angle

The MCT8314Z includes device an advance angle feature to advance the commutation by a specified electrical angle based on the voltage on the ADVANCE pin (in H/W device variant) or the ADVANCE bits (in SPI device variant). 図 7-28 shows the operation of advance angle feature.

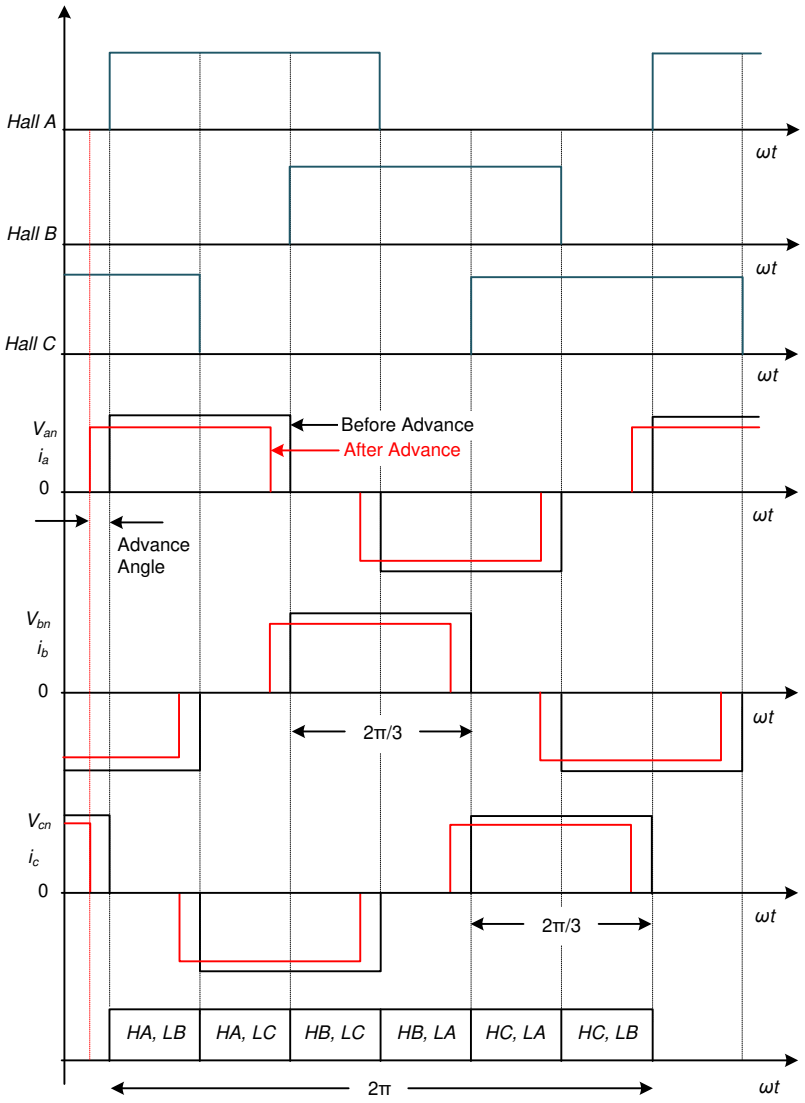

図 7-28. Advance Angle

7.3.14 FG Signal

The MCT8314Z device also has an open-drain FG signal that can be used for closed-loop speed control of a BLDC motor. This signal includes the information of all three Hall-elements inputs as shown in セクション 7.3.14. In the MCT8314ZS (SPI variant), FG can be configured to be a different division factor of Hall signals as shown in セクション 7.3.14. In the MCT8314ZH (Hardware variant), the FGSEL/LOCK_DET_TIME pin selects between 3x (FGOUT_SEL = 00b) or 1x (FGOUT_SEL = 01b) commutation frequencies as shown in 表 7-6.

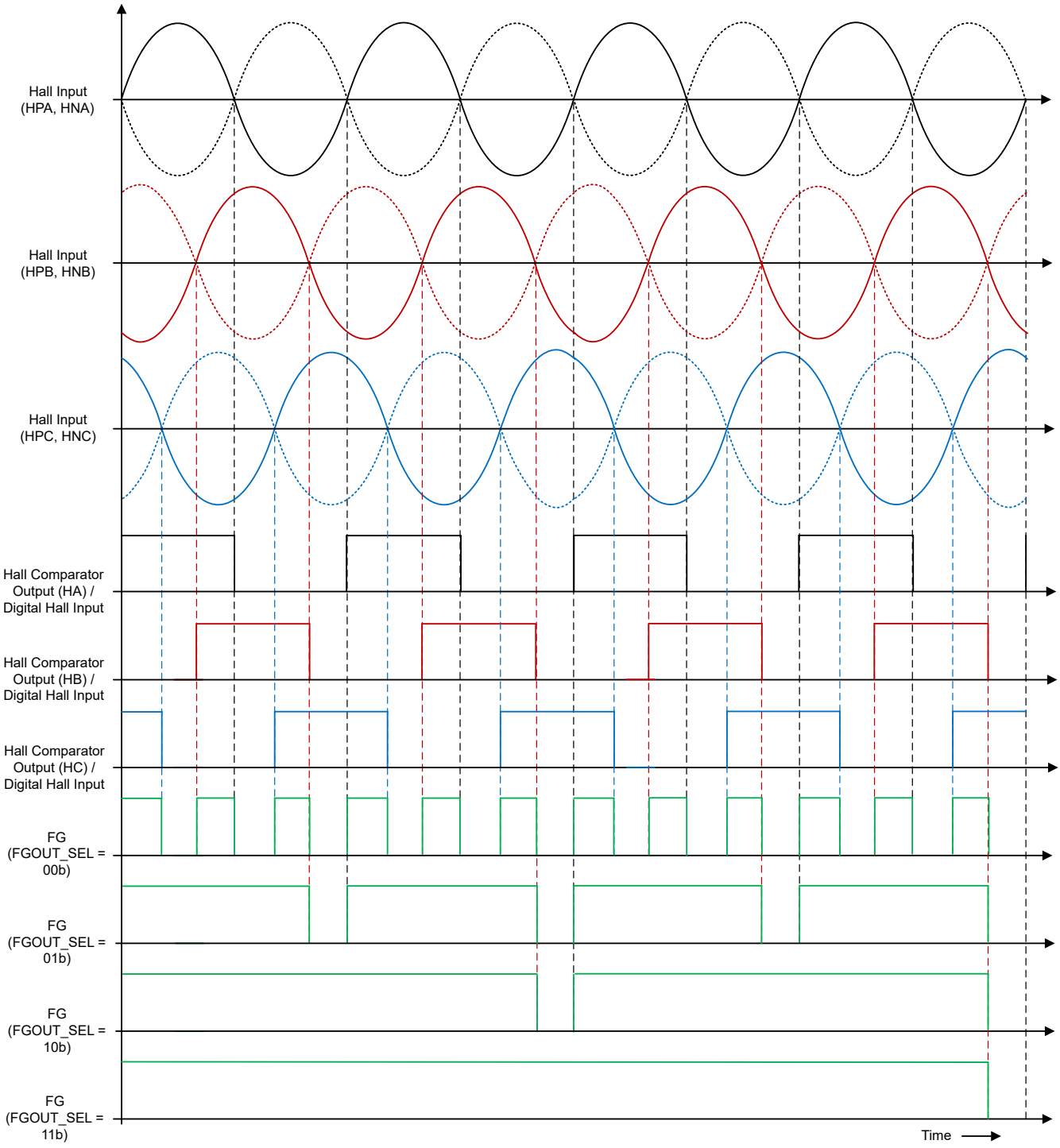

図 7-29. FG Signal

表 7-6. FG_SEL for MCT8314Z

Setting	FGSEL/LOCK_DET_TIME Pin (Hardware Variant)	FG Output Commutation Frequency	t_{MTR_LOCK}
Setting-1	Connected to AGND	3x commutation frequency (FGOUT_SEL = 00b)	300 ms
Setting-2	Connected to AGND with R_{MODE1}		500 ms
Setting-3	Connected to AGND with R_{MODE2}		1000 ms
Setting-4	Hi-Z		5000 ms
Setting-5	Connected to AVDD with R_{MODE2}	1x commutation frequency (FGOUT_SEL = 01b)	300 ms
Setting-6	Connected to AVDD with R_{MODE1}		500 ms
Setting-7	Connected to AVDD		1000 ms

ADVANCE INFORMATION

7.3.15 Protections

The MCT8314Z family of devices is protected against VM undervoltage, charge pump undervoltage, and overcurrent events. 表 7-7 summarizes various faults details.

表 7-7. Fault Action and Response

FAULT	CONDITION	CONFIGURATION	REPORT	H-BRIDGE	LOGIC	RECOVERY
VM undervoltage (NPOR)	$V_{VM} < V_{UVLO}$	Device default	—	Hi-Z	Disabled	Automatic: $V_{VM} > V_{UVLO\_R}$ CLR_FLT, nSLEEP Reset Pulse (NPOR bit)
AVDD undervoltage (NPOR)	$V_{AVDD} < V_{AVDD\_UV}$	Device default	—	Hi-Z	Disabled	Automatic: $V_{AVDD} > V_{AVDD\_UV\_R}$ CLR_FLT, nSLEEP Reset Pulse (NPOR bit)
Charge pump undervoltage (VCP_UV)	$V_{CP} < V_{CPUV}$	Device default	nFAULT	Hi-Z	Active	Automatic: $V_{VCP} > V_{CPUV}$ CLR_FLT, nSLEEP Reset Pulse (VCP_UV bit)
Overvoltage Protection (OVP)	$V_{VM} > V_{OVP}$	OVP_EN = 0b	None	Active	Active	No action (OVP Disabled)
		OVP_EN = 1b, HW device default	FAULT	Hi-Z	Active	Automatic: $V_{VM} < V_{OVP}$ CLR_FLT, nSLEEP Reset Pulse (OVP bit)
Overcurrent Protection (OCP)	$I_{PHASE} > I_{OCP}$	OCP_MODE = 00b, HW device default	nFAULT	Hi-Z	Active	Latched: CLR_FLT, nSLEEP Reset Pulse (OCP bits)
		OCP_MODE = 01b	nFAULT	Hi-Z	Active	Retry: t_{RETRY}
		OCP_MODE = 10b	nFAULT	Active	Active	Automatic: CLR_FLT, nSLEEP Reset Pulse (OCP bits)
		OCP_MODE = 11b	None	Active	Active	No action
SPI Error (SPI_FLT)	SCLK fault and ADDR fault	SPI_FLT_REP = 0b	nFAULT	Active	Active	Automatic: CLR_FLT, nSLEEP Reset Pulse (SPI_FLT bit)
		SPI_FLT_REP = 1b	None	Active	Active	No action
OTP Error (OTP_ERR)	OTP reading is erroneous	Device default	nFAULT	Hi-Z	Active	Latched: Power Cycle, nSLEEP Reset Pulse
Motor Lock (MTR_LOCK)	No Hall Signals > $t_{MTR\_LOCK\_TDET}$	MTR_LOCK_MODE = 00b	nFAULT	Hi-Z	Active	Latched: CLR_FLT, nSLEEP Pulse (MTR_LOCK bit)
		MTR_LOCK_MODE = 01b, HW device default	nFAULT	Hi-Z	Active	Retry: $t_{MTR\_LOCK\_RETRY}$
		MTR_LOCK_MODE = 10b	nFAULT	Active	Active	Automatic: CLR_FLT, nSLEEP Reset Pulse (OCP bits)
		MTR_LOCK_MODE = 11b	None	Active	Active	No action
Thermal warning (OTW)	$T_J > T_{OTW}$	OTW_REP = 0b	None	Active	Active	No action
		OTW_REP = 1b, HW device default	nFAULT	Active	Active	Automatic: $T_J < T_{OTW} - T_{OTW\_HYS}$ CLR_FLT, nSLEEP Pulse (OTW bit)
Thermal shutdown (OTSD_FET)	$T_J > T_{TSD\_FET}$	Device default	nFAULT	Hi-Z	Active	Automatic: $T_J < T_{TSD\_FET} - T_{TSD\_FET\_HYS}$ CLR_FLT, nSLEEP Pulse (OTS bit)

ADVANCE INFORMATION

7.3.15.1 VM Supply Undervoltage Lockout (NPOR)

If at any time the input supply voltage on the VM pin falls lower than the V_{UVLO} threshold (VM UVLO falling threshold), all of the integrated FETs, driver charge-pump and digital logic controller are disabled as shown in 図 7-30. Normal operation resumes (driver operation) when the VM undervoltage condition is removed. The NPOR bit is reset and latched low in the IC status (IC_STAT) register once the device presumes VM. The NPOR bit remains in reset condition until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}).

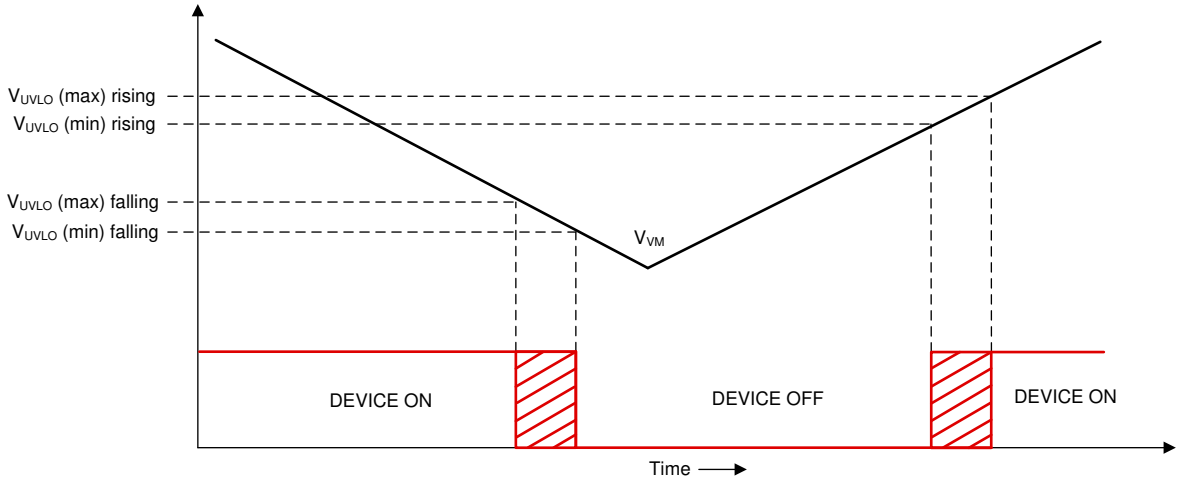

図 7-30. VM Supply Undervoltage Lockout

7.3.15.2 AVDD Undervoltage Lockout (AVDD_UV)

If at any time the voltage on AVDD pin falls lower than the V_{AVDD_UV} threshold, all of the integrated FETs, driver charge-pump and digital logic controller are disabled. Normal operation resumes (driver operation) when the AVDD undervoltage condition is removed. The NPOR bit is reset and latched low in the IC status (IC_STAT) register once the device presumes VM. The NPOR bit remains in reset condition until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}).

7.3.15.3 VCP Charge Pump Undervoltage Lockout (CPUV)

If at any time the voltage on the VCP pin (charge pump) falls lower than the V_{CPUV} threshold voltage of the charge pump, all of the integrated FETs are disabled and the nFAULT pin is driven low. The FAULT and VCP_UV bits are also latched high in the registers on SPI devices. Normal operation starts again (driver operation and the nFAULT pin is released) when the VCP undervoltage condition clears. The CPUV bit stays set until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}). The CPUV protection is always enabled in both hardware and SPI device varaints.

7.3.15.4 Overvoltage Protections (OVP)

If at any time input supply voltage on the VM pins rises higher than the V_{OVP} threshold voltage, all of the integrated FETs are disabled and the nFAULT pin is driven low. The FAULT and OVP bits are also latched high in the registers on SPI devices. Normal operation starts again (driver operation and the nFAULT pin is released) when the OVP condition clears. The OVP bit stays set until cleared through the CLR_FLT bit or an nSLEEP pin reset pulse (t_{RST}). Setting the OVP_EN bit high on the SPI device (MCT8314ZS) enables this protection feature. The OVP threshold is also programmable on the SPI device variant and can be set to 22-V or 34-V based on the OVP_SEL bit. On hardware interface device (MCT8314ZH), the OVP protection is always enabled and set to a 34-V threshold.

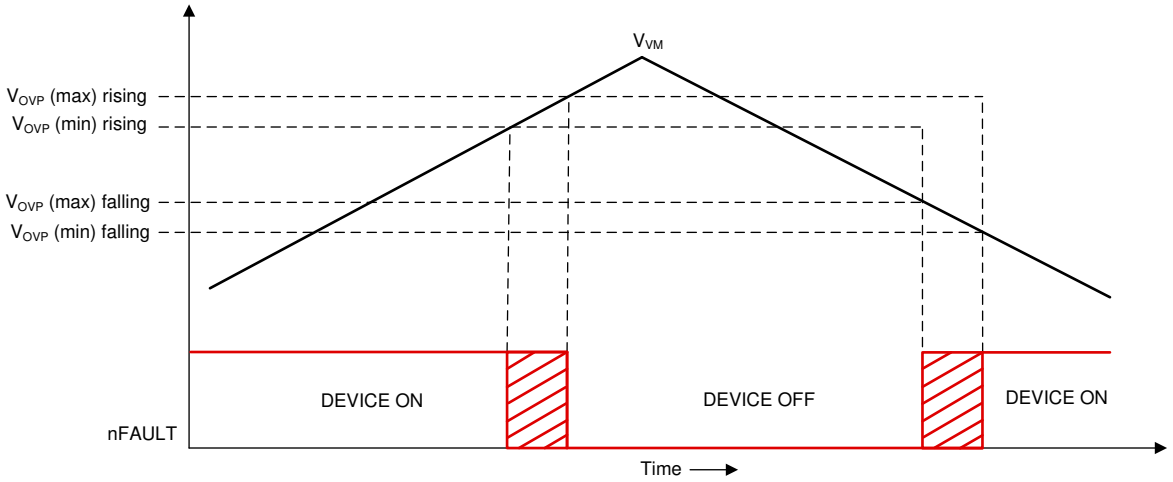

図 7-31. Over Voltage Protection

7.3.15.5 Overcurrent Protection (OCP)

A MOSFET overcurrent event is sensed by monitoring the current flowing through FETs. If the current across a FET exceeds the I_{OCP} threshold for longer than the t_{OCP} deglitch time, an OCP event is recognized and action is done according to the OCP_MODE bit. The I_{OCP} threshold is fixed at 2.25-A threshold. On hardware interface devices, the t_{OCP_DEG} is fixed at 0.6-µs, and the default OCP response is latched shutdown. On SPI devices, the t_{OCP_DEG} is set through the OCP_DEG SPI register, and the OCP_MODE bit can operate in four different modes: OCP latched shutdown, OCP automatic retry, OCP report only, and OCP disabled.

7.3.15.5.1 OCP Latched Shutdown (OCP_MODE = 00b or MCT8314ZH)

After a OCP event in this mode, all MOSFETs are disabled and the nFAULT pin is driven low. The FAULT, OCP, and corresponding FET's OCP bits are latched high in the SPI registers. Normal operation starts again (driver operation and the nFAULT pin is released) when the OCP condition clears and a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}).

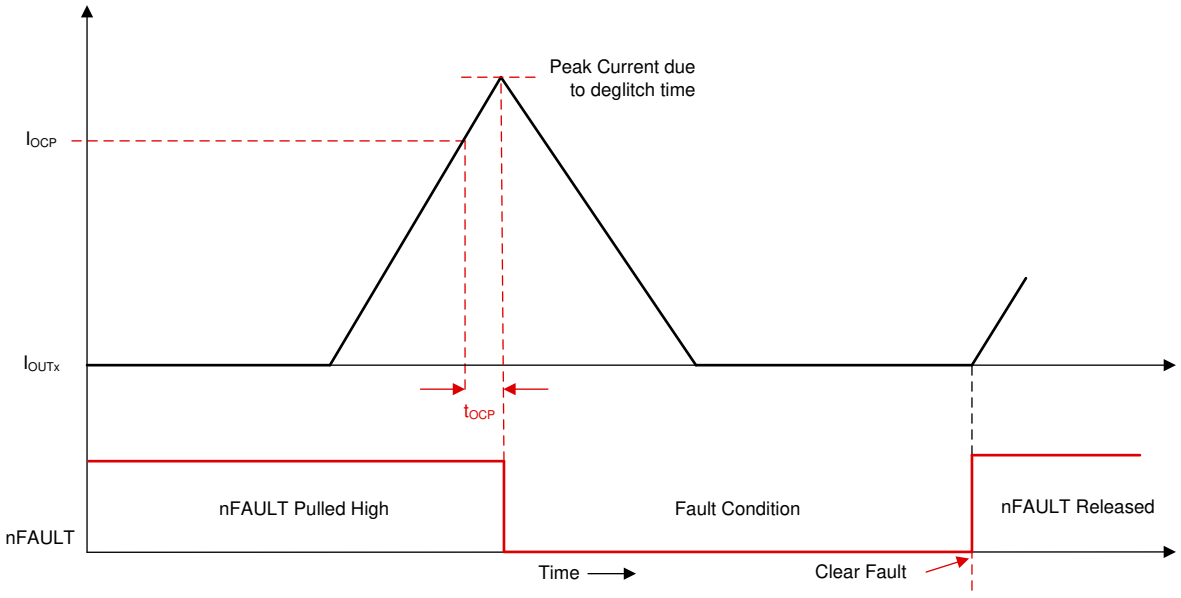

図 7-32. Overcurrent Protection - Latched Shutdown Mode

ADVANCE INFORMATION

7.3.15.5.2 OCP Automatic Retry (OCP_MODE = 01b)

After a OCP event in this mode, all the FETs are disabled and the nFAULT pin is driven low. The FAULT, OCP, and corresponding FET's OCP bits are latched high in the SPI registers. Normal operation starts again automatically (driver operation and the nFAULT pin is released) after the t_{RETRY} time elapses. After the t_{RETRY} time elapses, the FAULT, OCP, and corresponding FET's OCP bits stay latched until a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}).

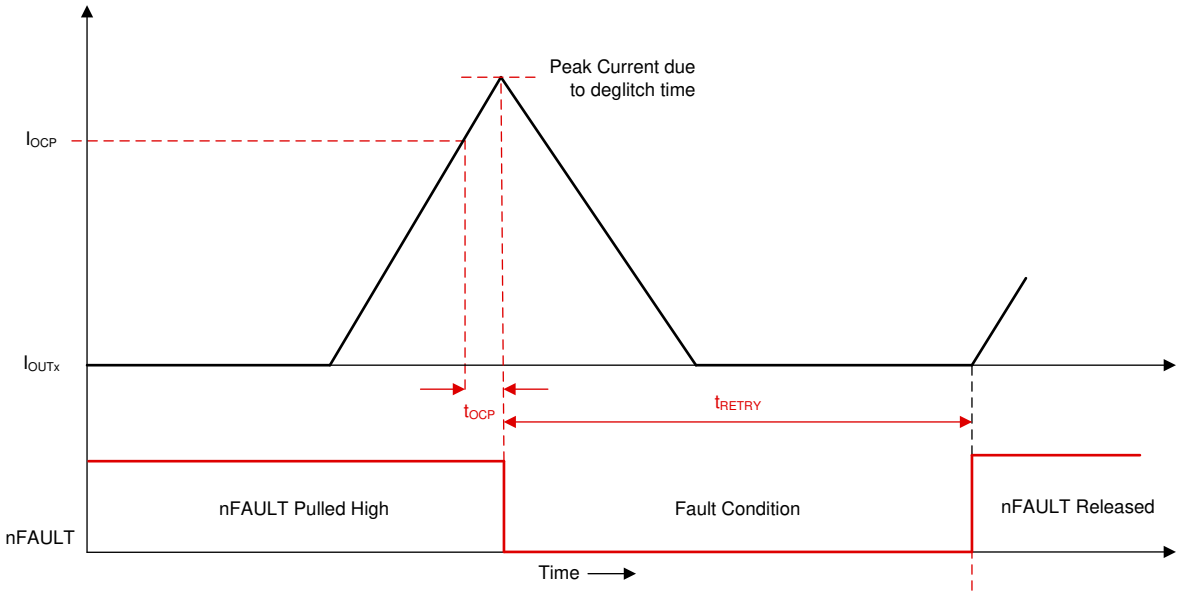

図 7-33. Overcurrent Protection - Automatic Retry Mode

7.3.15.5.3 OCP Report Only (OCP_MODE = 10b)

No protective action occurs after a OCP event in this mode. The overcurrent event is reported by driving the nFAULT pin low and latching the FAULT, OCP, and corresponding FET's OCP bits high in the SPI registers. The MCT8314Z continues to operate as usual. The external controller manages the overcurrent condition by acting appropriately. The reporting clears (nFAULT pin is released) when the OCP condition clears and a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}).

7.3.15.5.4 OCP Disabled (OCP_MODE = 11b)

No action occurs after a OCP event in this mode.

7.3.15.6 Motor Lock (MTR_LOCK)

During motor is in lock condition the hall signals will be not available, so a motor lock event is sensed by monitoring the hall signals. If the Hall signals are not present for for longer than the t_{MTR_LOCK}, the MCT8314Z recognizes a MTR_LCK event and responds according to the MTR_LOCK_MODE bits. On the MCT8314ZH, the FGSEL/LOCK_DET_TIME pin configures t_{MTR_LOCK} detection time, and the device recovers automatically after 500 ms. On SPI devices, the MTR_LOCK_TDET register sets the t_{MTR_LOCK} threshold, and the MTR_LOCK_MODE bit sets four different modes: MTR_LOCK latched shutdown, MTR_LOCK automatic retry, MTR_LOCK report only, and MTR_LOCK disabled.

注

If the PWM pin is held low for longer than t_{PWM_LOW}, then motor lock detection disables.

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7.3.15.6.1 MTR_LOCK Latched Shutdown (MTR_LOCK_MODE = 00b)

After a motor lock event in this mode, all FETs are disabled and the nFAULT pin is driven low. The FAULT and MTR_LOCK bits are latched high in the SPI registers. Normal operation starts again (driver operation and the nFAULT pin is released) after clearing the faults through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}).

7.3.15.6.2 MTR_LOCK Automatic Retry (MTR_LOCK_MODE = 01b or MCT8314ZH)

After a motor lock event in this mode, all the external MOSFETs are disabled and the nFAULT pin is driven low. The FAULT and MTR_LOCK bits are latched high in the SPI registers. Normal operation starts again automatically (driver operation and the nFAULT pin is released) after the $t_{MTR\_LOCK\_RETRY}$ time elapses. The FAULT and MTR_LOCK bits stay latched until the $t_{MTR\_LOCK\_RETRY}$ period expires.

MTR_LOCK automatic retry is the only motor lock response mode available in the hardware interface variant, MCT8314ZH. The retry period, $t_{MTR\_LOCK\_RETRY}$, is set to 500 ms. 表 7-8 shows the options for t_{MTR_LOCK} detection time selectable by external components on the FGSEL/LOCK_DET_TIME pin in the MCT8314ZH hardware variant.

表 7-8. LOCK_DET_TIME Selection for MCT8314Z

Setting	FGSEL/LOCK_DET_TIME Pin (Hardware Variant)	FG Output Commutation Frequency	t_{MTR_LOCK}
Setting-1	Connected to AGND	3x commutation frequency (FGOUT_SEL = 00b)	300 ms
Setting-2	Connected to AGND with R_{MODE1}		500 ms
Setting-3	Connected to AGND with R_{MODE2}		1000 ms
Setting-4	Hi-Z		5000 ms
Setting-5	Connected to AVDD with R_{MODE2}	1x commutation frequency (FGOUT_SEL = 01b)	300 ms
Setting-6	Connected to AVDD with R_{MODE1}		500 ms
Setting-7	Connected to AVDD		1000 ms

7.3.15.6.3 MTR_LOCK Report Only (MTR_LOCK_MODE= 10b)

No protective action occurs after a MTR_LOCK event in this mode. The motor lock event is reported by driving the nFAULT pin low and latching the FAULT and MTR_LOCK bits high in the SPI registers. The MCT8314Z continues to operate as usual. The external controller manages the motor lock condition by acting appropriately. The reporting clears (nFAULT pin is released) when a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}).

7.3.15.6.4 MTR_LOCK Disabled (MTR_LOCK_MODE = 11b)

No action occurs after a MTR_LOCK event in this mode.

7.3.15.7 Thermal Warning (OTW)

MCT8314Z has two die temperature sensor for thermal warning, one of them near FETs and other one near the AVDD LDO. If the die temperature exceeds the trip point of the thermal warning (T_{OTW}), the OT bit in the IC status (IC_STAT) register and OTW bit in the status register is set. The reporting of OTW on the nFAULT pin can be enabled by setting the over-temperature warning reporting (OTW_REP) bit in the configuration control register. The device performs no additional action and continues to function. In this case, the nFAULT pin releases when the die temperature decreases below the hysteresis point of the thermal warning (T_{OTW_HYS}). The OTW bit remains set until cleared through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}) and the die temperature is lower than thermal warning trip (T_{OTW}).

注

Over temperature warning is not reported on nFAULT pin by default.

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7.3.15.8 Thermal Shutdown (OTS)

If the die temperature near FET exceeds the trip point of the thermal shutdown limit (T_{TSD_FET}), all the FETs are disabled and the nFAULT pin is driven low. The AVDD LDO remains active. In addition, the FAULT and OT bit in the IC status (IC_STAT) register and OTS bit in the status register is set. Normal operation starts again (driver operation and the nFAULT pin is released) when the overtemperature condition clears. The OTS bit stays latched high indicating that a thermal event occurred until a clear fault command is issued either through the CLR_FLT bit or an nSLEEP reset pulse (t_{RST}). This protection feature cannot be disabled.

7.4 Device Functional Modes

7.4.1 Functional Modes

7.4.1.1 Sleep Mode

The nSLEEP pin manages the state of the MCT8314Z family of devices. When the nSLEEP pin is low, the device goes to a low-power sleep mode. In sleep mode, all FETs are disabled, sense amplifiers are disabled, the charge pump is disabled, the AVDD regulator is disabled, and the SPI bus is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device goes to sleep mode. The device comes out of sleep mode automatically if the nSLEEP pin is pulled high. The t_{WAKE} time must elapse before the device is ready for inputs.

In sleep mode and when $V_{VM} < V_{UVLO}$, all MOSFETs are disabled.

注

During power up and power down of the device through the nSLEEP pin, the nFAULT pin is held low as the internal regulators are enabled or disabled. After the regulators have enabled or disabled, the nFAULT pin is automatically released. The duration that the nFAULT pin is low does not exceed the t_{SLEEP} or t_{WAKE} time.

7.4.1.2 Operating Mode

When the nSLEEP pin is high and the V_{VM} voltage is greater than the V_{UVLO} voltage, the device goes to operating mode. The t_{WAKE} time must elapse before the device is ready for inputs. In this mode the charge pump, AVDD regulator, and SPI bus are active.

7.4.1.3 Fault Reset (CLR_FLT or nSLEEP Reset Pulse)

In the case of device latched faults, the MCT8314Z family of devices goes to a partial shutdown state to help protect the power MOSFETs and system.

When the fault condition clears, the device can go to the operating state again by either setting the CLR_FLT SPI bit on SPI devices or issuing a reset pulse to the nSLEEP pin on either interface variant. The nSLEEP reset pulse (t_{RST}) consists of a high-to-low-to-high transition on the nSLEEP pin. The low period of the sequence should fall with the t_{RST} time window or else the device will start the complete shutdown sequence. The reset pulse has no effect on any of the regulators, device settings, or other functional blocks.

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7.5 SPI Communication

7.5.1 Programming

On MCT8314Z SPI devices, an SPI bus is used to set device configurations, operating parameters, and read out diagnostic information. The SPI operates in secondary mode and connects to a controller. The SPI input data (SDI) word consists of a 16-bit word, with a 6-bit address and 8 bits of data. The SPI output consists of 16 bit word, with a 8 bits of status information (STAT register) and 8-bit register data.

A valid frame must meet the following conditions:

- The SCLK pin should be low when the nSCS pin transitions from high to low and from low to high.
- The nSCS pin should be pulled high for at least 400 ns between words.
- When the nSCS pin is pulled high, any signals at the SCLK and SDI pins are ignored and the SDO pin is placed in the Hi-Z state.
- Data is captured on the falling edge of the SCLK pin and data is propagated on the rising edge of the SCLK pin.
- The most significant bit (MSB) is shifted in and out first.
- A full 16 SCLK cycles must occur for transaction to be valid.
- If the data word sent to the SDI pin is less than or more than 16 bits, a frame error occurs and the data word is ignored.
- For a write command, the existing data in the register being written to is shifted out on the SDO pin following the 8-bit status data.

The SPI registers are reset to the default settings on power up and when the device is enters sleep mode

7.5.1.1 SPI Format

The SDI input data word is 16 bits long and consists of the following format:

- 1 read or write bit, W (bit B15)
- 6 address bits, A (bits B14 through B9)
- Parity bit, P (bit B8). Parity bit is set such that the SDI input data word has even number of 1s and 0s
- 8 data bits, D (bits B7 through B0)

The SDO output data word is 16 bits long and the first 8 bits are status bits. The data word is the content of the register being accessed.

For a write command (W0 = 0), the response word on the SDO pin is the data currently in the register being written to.

For a read command (W0 = 1), the response word is the data currently in the register being read.

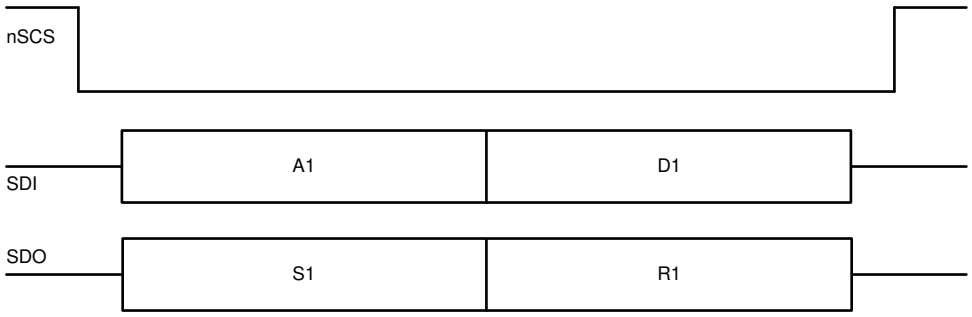

図 7-34.

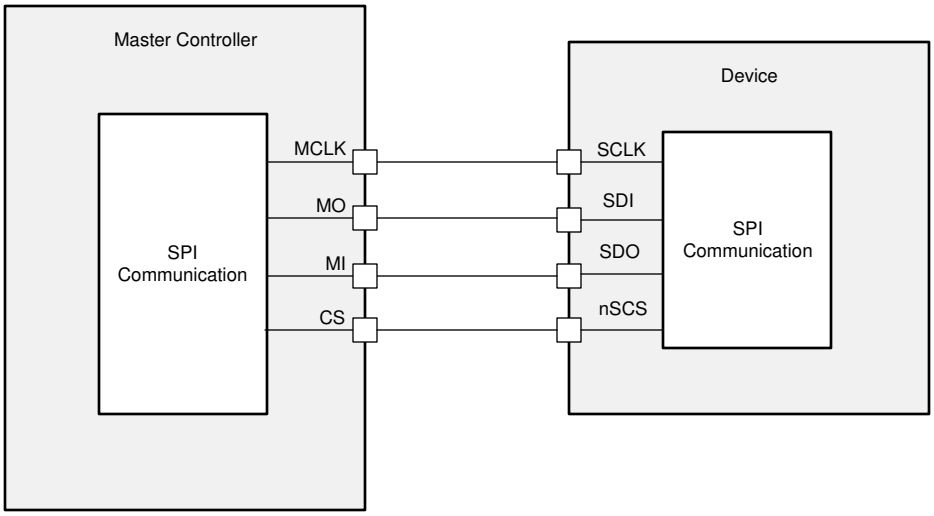

図 7-35.

表 7-9. SDI Input Data Word Format

R/W	ADDRESS						Parity	DATA							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
W0	A5	A4	A3	A2	A1	A0	P	D7	D6	D5	D4	D3	D2	D1	D0

表 7-10. SDO Output Data Word Format

STATUS								DATA							
B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
S7	S6	S5	S4	S3	S2	S1	S0	D7	D6	D5	D4	D3	D2	D1	D0

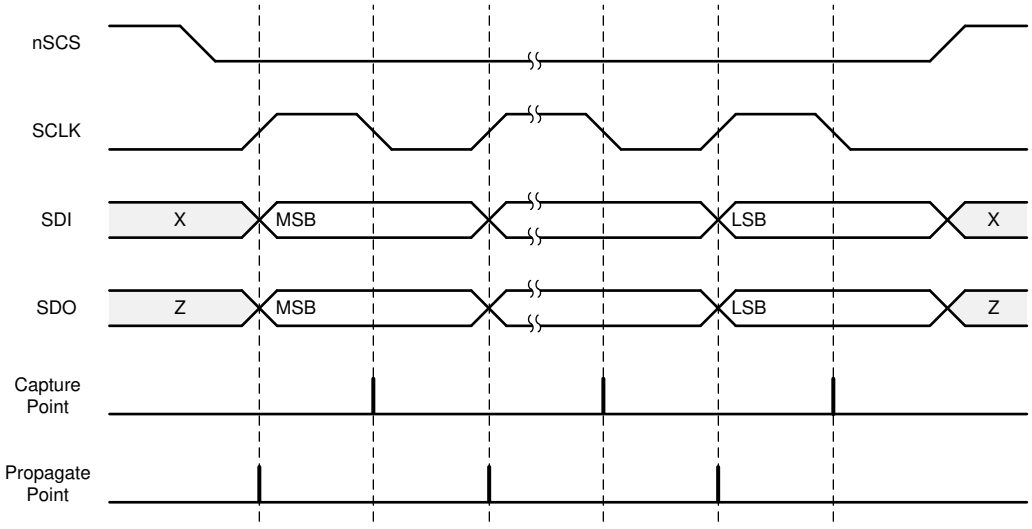

図 7-36. SPI Secondary Timing Diagram

SPI Error Handling

SPI Frame Error (SPI_SCLK_FLT: If the nSCS gets deasserted before the end of 16-bit frame, SPI frame error is detected and SPI_SCLK_FLT bit is set in STAT2. The SPI_SCLK_FLT status bit is latched and can be cleared when a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse

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SPI Address Error (SPI_ADDR_FLT): If an invalid address is provided in the ADDR field of the input SPI data on SDI, SPI address error is detected and SPI_ADDR_FLT bit in STAT2 is set. Invalid address is any address that is not defined in Register Map i.e. address not falling in the range of address 0x0 to 0xC. The SPI_ADDR_FLT status bit is latched and can be cleared when a clear faults command is issued either through the CLR_FLT bit or an nSLEEP reset pulse

7.6 Register Map

7.6.1 STATUS Registers

表 7-11 lists the memory-mapped registers for the STATUS registers. All register offset addresses not listed in 表 7-11 should be considered as reserved locations and the register contents should not be modified.

表 7-11. STATUS Registers

Offset	Acronym	Register Name	Section
0h	IC Status Register	IC Status Register	セクション 7.6.1.1
1h	Status Register 1	Status Register 1	セクション 7.6.1.2
2h	Status Register 2	Status Register 2	セクション 7.6.1.3

Complex bit access types are encoded to fit into small table cells. 表 7-12 shows the codes that are used for access types in this section.

表 7-12. STATUS Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Reset or Default Value		
-n		Value after reset or the default value

7.6.1.1 IC Status Register (Offset = 0h) [Reset = 00h]

IC Status Register is shown in 表 7-13.

Return to the Summary Table.

表 7-13. IC Status Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MTR_LOCK	R	0h	Motor Lock Staus Bit 0h = No motor lock is detected 1h = Motor lock is detected
6	RESERVED	R-0	0h	Reserved
5	SPI_FLT	R	0h	SPI Fault Bit 0h = No SPI fault condition is detected 1h = SPI Fault condition is detected
4	OCP	R	0h	Over Current Protection Status Bit 0h = No overcurrent condition is detected 1h = Overcurrent condition is detected
3	NPOR	R	0h	Supply Power On Reset Bit 0h = Power on reset condition is detected on VM 1h = No power-on-reset condition is detected on VM
2	OVP	R	0h	Supply Overvoltage Protection Status Bit 0h = No overvoltage condition is detected on VM 1h = Overvoltage condition is detected on VM
1	OT	R	0h	Overtemperature Fault Status Bit 0h = No overtemperature warning / shutdown is detected 1h = Overtemperature warning / shutdown is detected
0	FAULT	R	0h	Device Fault Bit 0h = No fault condition is detected 1h = Fault condition is detected

7.6.1.2 Status Register 1 (Offset = 1h) [Reset = 00h]

Status Register 1 is shown in 表 7-14.

Return to the Summary Table.

表 7-14. Status Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
7	OTW	R	0h	Overtemperature Warning Status Bit 0h = No overtemperature warning is detected 1h = Overtemperature warning is detected
6	OTS	R	0h	Overtemperature Shutdown Status Bit 0h = No overtemperature shutdown is detected 1h = Overtemperature shutdown is detected
5	OCP_HC	R	0h	Overcurrent Status on High-side switch of OUTC 0h = No overcurrent detected on high-side switch of OUTC 1h = Overcurrent detected on high-side switch of OUTC
4	OCL_LC	R	0h	Overcurrent Status on Low-side switch of OUTC 0h = No overcurrent detected on low-side switch of OUTC 1h = Overcurrent detected on low-side switch of OUTC
3	OCP_HB	R	0h	Overcurrent Status on High-side switch of OUTB 0h = No overcurrent detected on high-side switch of OUTB 1h = Overcurrent detected on high-side switch of OUTB
2	OCP_LB	R	0h	Overcurrent Status on Low-side switch of OUTB 0h = No overcurrent detected on low-side switch of OUTB 1h = Overcurrent detected on low-side switch of OUTB
1	OCP_HA	R	0h	Overcurrent Status on High-side switch of OUTA 0h = No overcurrent detected on high-side switch of OUTA 1h = Overcurrent detected on high-side switch of OUTA
0	OCP_LA	R	0h	Overcurrent Status on Low-side switch of OUTA 0h = No overcurrent detected on low-side switch of OUTA 1h = Overcurrent detected on low-side switch of OUTA

7.6.1.3 Status Register 2 (Offset = 2h) [Reset = 00h]

Status Register 2 is shown in 表 7-15.

Return to the Summary Table.

表 7-15. Status Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R-0	0h	Reserved
6	OTP_ERR	R	0h	One Time Programmabilty Error 0h = No OTP error is detected 1h = OTP Error is detected
5	RESERVED	R-0	0h	Reserved
4	RESERVED	R	0h	Reserved
3	VCP_UV	R	0h	Charge Pump Undervoltage Status Bit 0h = No charge pump undervoltage is detected 1h = Charge pump undervoltage is detected
2	SPI_PARITY	R-0	0h	SPI Parity Error Bit 0h = No SPI parity error is detected 1h = SPI parity error is detected
1	SPI_SCLK_FLT	R	0h	SPI Clock Framing Error Bit 0h = No SPI clock framing error is detected 1h = SPI clock framing error is detected
0	SPI_ADDR_FLT	R	0h	SPI Address Error Bit 0h = No SPI address fault is detected (due to accessing non-user register) 1h = SPI address fault is detected

ADVANCE INFORMATION

7.6.2 CONTROL Registers

表 7-16 lists the memory-mapped registers for the CONTROL registers. All register offset addresses not listed in 表 7-16 should be considered as reserved locations and the register contents should not be modified.

表 7-16. CONTROL Registers

Offset	Acronym	Register Name	Section
3h	Control Register 1	Control Register 1	セクション 7.6.2.1
4h	Control Register 2	Control Register 2	セクション 7.6.2.2
5h	Control Register 3	Control Register 3	セクション 7.6.2.3
6h	Control Register 4	Control Register 4	セクション 7.6.2.4
7h	Control Register 5	Control Register 5	セクション 7.6.2.5
8h	Control Register 6	Control Register 6	セクション 7.6.2.6
9h	Control Register 7	Control Register 7	セクション 7.6.2.7
Ah	Control Register 8	Control Register 8	セクション 7.6.2.8
Bh	Control Register 9	Control Register 9	セクション 7.6.2.9
Ch	Control Register 10	Control Register 10	セクション 7.6.2.10

Complex bit access types are encoded to fit into small table cells. 表 7-17 shows the codes that are used for access types in this section.

表 7-17. CONTROL Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
R-0	R -0	Read Returns 0s
Write Type		
W	W	Write
W1C	W 1C	Write 1 to clear
WAPU	W APU	Write Atomic write with password unlock
Reset or Default Value		
-n		Value after reset or the default value

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7.6.2.1 Control Register 1 (Offset = 3h) [Reset = 03h]

Control Register 1 is shown in 表 7-18.

Return to the Summary Table.

表 7-18. Control Register 1 Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R-0	0h	Reserved
2-0	REG_LOCK	R/WAPU	3h	Register Lock Bits 0h = No effect unless locked or unlocked 1h = No effect unless locked or unlocked 2h = No effect unless locked or unlocked 3h = Write 011b to this register to unlock all registers 4h = No effect unless locked or unlocked 5h = No effect unless locked or unlocked 6h = Write 110b to lock the settings by ignoring further register writes except to these bits and address 0x03h bits 2-0. 7h = No effect unless locked or unlocked

7.6.2.2 Control Register 2 (Offset = 4h) [Reset = 20h]

Control Register 2 is shown in 表 7-19.

Return to the Summary Table.

表 7-19. Control Register 2 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R-0	0h	Reserved
5	SDO_MODE	R/W	1h	SDO Mode Setting 0h = SDO IO in Open Drain Mode 1h = SDO IO in Push Pull Mode
4-3	RESERVED	R-0	0h	Reserved
2-1	PWM_MODE	R/W	0h	Device Mode Selection 0h = Asynchronous rectification with analog Hall 1h = Asynchronous rectification with digital Hall 2h = Synchronous rectification with analog Hall 3h = Synchronous rectification with digital Hall
0	CLR_FLT	W1C	0h	Clear Fault 0h = No clear fault command is issued 1h = To clear the latched fault bits. This bit automatically resets after being written.

7.6.2.3 Control Register 3 (Offset = 5h) [Reset = 46h]

Control Register 3 is shown in 表 7-20.

Return to the Summary Table.

表 7-20. Control Register 3 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R-0	0h	Reserved
6	RESERVED	R/W	0h	Reserved
5	RESERVED	R/W	0h	Reserved
4	PWM_100_DUTY_SEL	R/W	0h	Freqency of PWM at 100% Duty Cycle 0h = 20KHz 1h = 40KHz
3	OVP_SEL	R/W	0h	Overvoltage Level Setting 0h = VM overvoltage level is 34-V 1h = VM overvoltage level is 22-V
2	OVP_EN	R/W	1h	Overvoltage Enable Bit 0h = Overvoltage protection is disabled 1h = Overvoltage protection is enabled
1	SPI_FLT_REP	R/W	1h	SPI Fault Reporting Disable Bit 0h = SPI fault reporting on nFAULT pin is enabled 1h = SPI fault reporting on nFAULT pin is disabled
0	OTW_REP	R/W	0h	Overtemperature Warning Reporting Bit 0h = Over temperature reporting on nFAULT is disabled 1h = Over temperature reporting on nFAULT is enabled

7.6.2.4 Control Register 4 (Offset = 6h) [Reset = 10h]

Control Register 4 is shown in 表 7-21.

Return to the Summary Table.

表 7-21. Control Register 4 Field Descriptions

Bit	Field	Type	Reset	Description
7	DRV_OFF	R/W	0h	Driver OFF Bit 0h = No Action 1h = Enter Low Power Standby Mode
6	OCP_CBC	R/W	0h	OCP PWM Cycle Operation Bit 0h = OCP clearing in PWM input cycle change is disabled 1h = OCP clearing in PWM input cycle change is enabled
5-4	OCP_DEG	R/W	1h	OCP Deglitch Time Settings 0h = OCP deglitch time is 0.2 µs 1h = OCP deglitch time is 0.6 µs 2h = OCP deglitch time is 1.25 µs 3h = OCP deglitch time is 1.6 µs
3	OCP_RETRY	R/W	0h	OCP Retry Time Settings 0h = OCP retry time is 5 ms 1h = OCP retry time is 500 ms
2	RESERVED	R-0	0h	Reserved
1-0	OCP_MODE	R/W	0h	OCP Fault Options 0h = Overcurrent causes a latched fault 1h = Overcurrent causes an automatic retrying fault 2h = Overcurrent is report only but no action is taken 3h = Overcurrent is not reported and no action is taken

7.6.2.5 Control Register 5 (Offset = 7h) [Reset = 00h]

Control Register 5 is shown in 表 7-22.

Return to the Summary Table.

表 7-22. Control Register 5 Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R/W	0h	Reserved
6	ILIM_RECIR	R/W	0h	Current Limit Recirculation Settings 0h = Current recirculation through FETs (Brake Mode) 1h = Current recirculation through diodes (Coast Mode)
5	RESERVED	R/W	0h	Reserved
4	RESERVED	R/W	0h	Reserved
3	RESERVED	R-0	0h	Reserved
2	EN_ASR	R/W	0h	Active Synchronous Rectification Enable Bit 0h = ASR mode is disabled 1h = ASR mode is enabled
1-0	RESERVED	R-0	0h	Reserved

7.6.2.6 Control Register 6 (Offset = 8h) [Reset = 00h]

Control Register 6 is shown in 表 7-23.

Return to the Summary Table.

表 7-23. Control Register 6 Field Descriptions

Bit	Field	Type	Reset	Description
7-0	RESERVED	R-0	0h	Reserved

7.6.2.7 Control Register 7 (Offset = 9h) [Reset = 00h]

Control Register 7 is shown in 表 7-24.

Return to the Summary Table.

表 7-24. Control Register 7 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R-0	0h	Reserved
4	HALL_HYS	R/W	0h	Hall Comparator Hysteresis Settings 0h = 5 mV 1h = 50 mV
3	BRAKE_MODE	R/W	0h	Brake Mode Setting 0h = Device operation is braking in brake mode 1h = Device operation is coasting in brake mode
2	COAST	R/W	0h	Coast Bit 0h = Device coast mode is disabled 1h = Device coast mode is enabled
1	RESERVED	R-0	0h	Reserved
0	DIR	R/W	0h	Direction Bit 0h = Motor direction is set to clockwise direction 1h = Motor direction is set to anti-clockwise direction

7.6.2.8 Control Register 8 (Offset = Ah) [Reset = 41h]

Control Register 8 is shown in 表 7-25.

Return to the Summary Table.

表 7-25. Control Register 8 Field Descriptions

Bit	Field	Type	Reset	Description
7-6	FGOUT_SEL	R/W	1h	Electrical Frequency Generation Output Mode Bits 0h = FG frequency is 3x commutation frequency 1h = FG frequency is 1x of commutation frequency 2h = FG frequency is 0.5x of commutation frequency 3h = FG frequency is 0.25x of commutation frequency
5	RESERVED	R-0	0h	Reserved
4	MTR_LOCK_RETRY	R/W	0h	Motor Lock Retry Time Settings 0h = 500 ms 1h = 5000 ms
3-2	MTR_LOCK_TDET	R/W	0h	Motor Lock Detection Time Settings 0h = 300 ms 1h = 500 ms 2h = 1000 ms 3h = 5000 ms
1-0	MTR_LOCK_MODE	R/W	1h	Motor Lock Fault Options 0h = Motor lock causes a latched fault 1h = Motor lock causes an automatic retrying fault 2h = Motor lock is report only but no action is taken 3h = Motor lock is not reported and no action is taken

7.6.2.9 Control Register 9 (Offset = Bh) [Reset = 00h]

Control Register 9 is shown in 表 7-26.

Return to the Summary Table.

表 7-26. Control Register 9 Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R-0	0h	Reserved
2-0	ADVANCE_LVL	R/W	0h	Phase Advance Setting 0h = 0° 1h = 4° 2h = 7° 3h = 11° 4h = 15° 5h = 20° 6h = 25° 7h = 30°

7.6.2.10 Control Register 10 (Offset = Ch) [Reset = 00h]

Control Register 10 is shown in 表 7-27.

Return to the Summary Table.

表 7-27. Control Register 10 Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R-0	0h	Reserved
4	RESERVED	R-0	0h	Reserved
3-0	RESERVED	R-0	0h	Reserved

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The MCT8314Z can be used to drive Brushless-DC motors. The following design procedure can be used to configure the MCT8314Z.

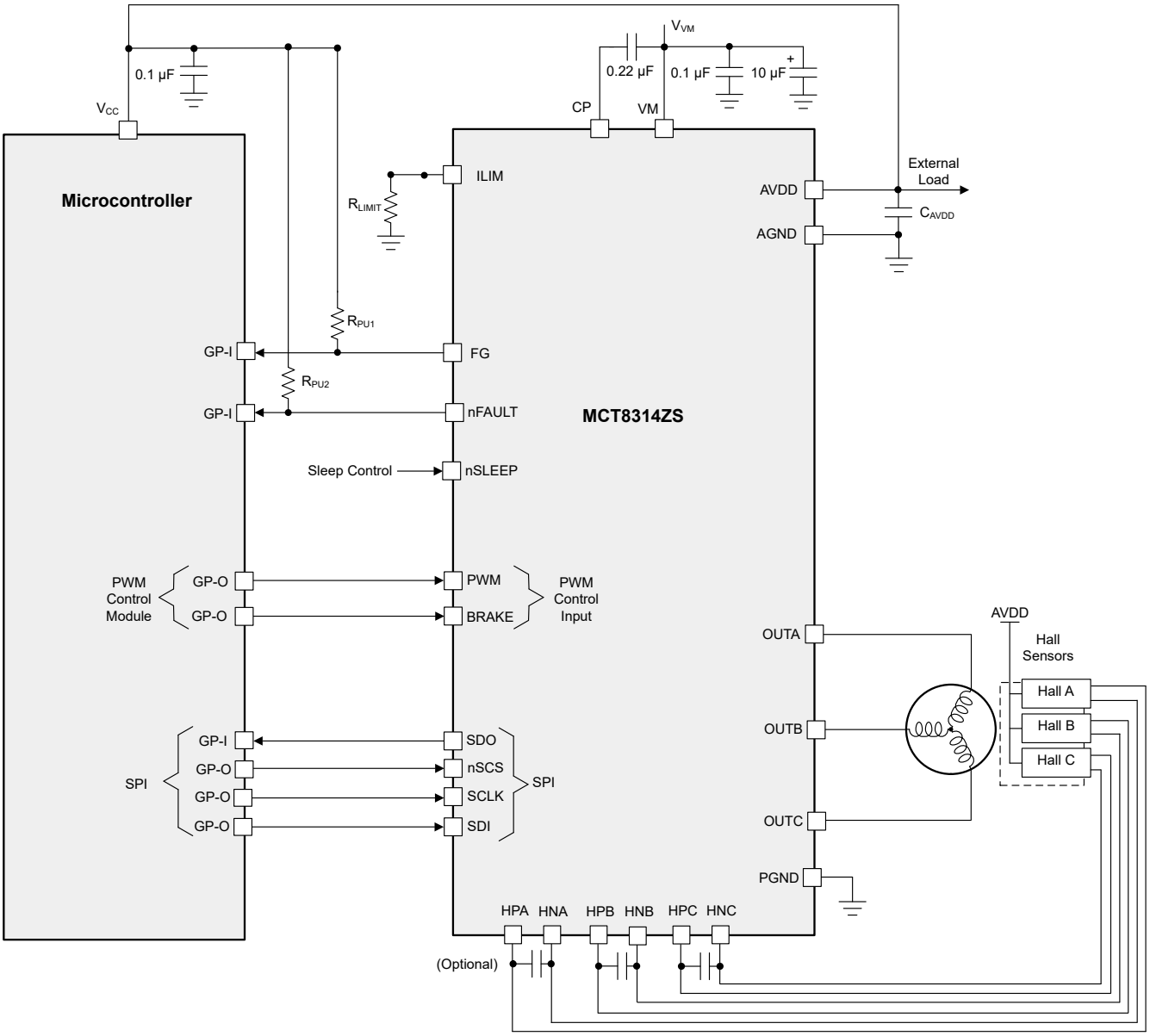


図 8-1. Primary Application Schematics for MCT8314ZS (SPI variant)

ADVANCE INFORMATION

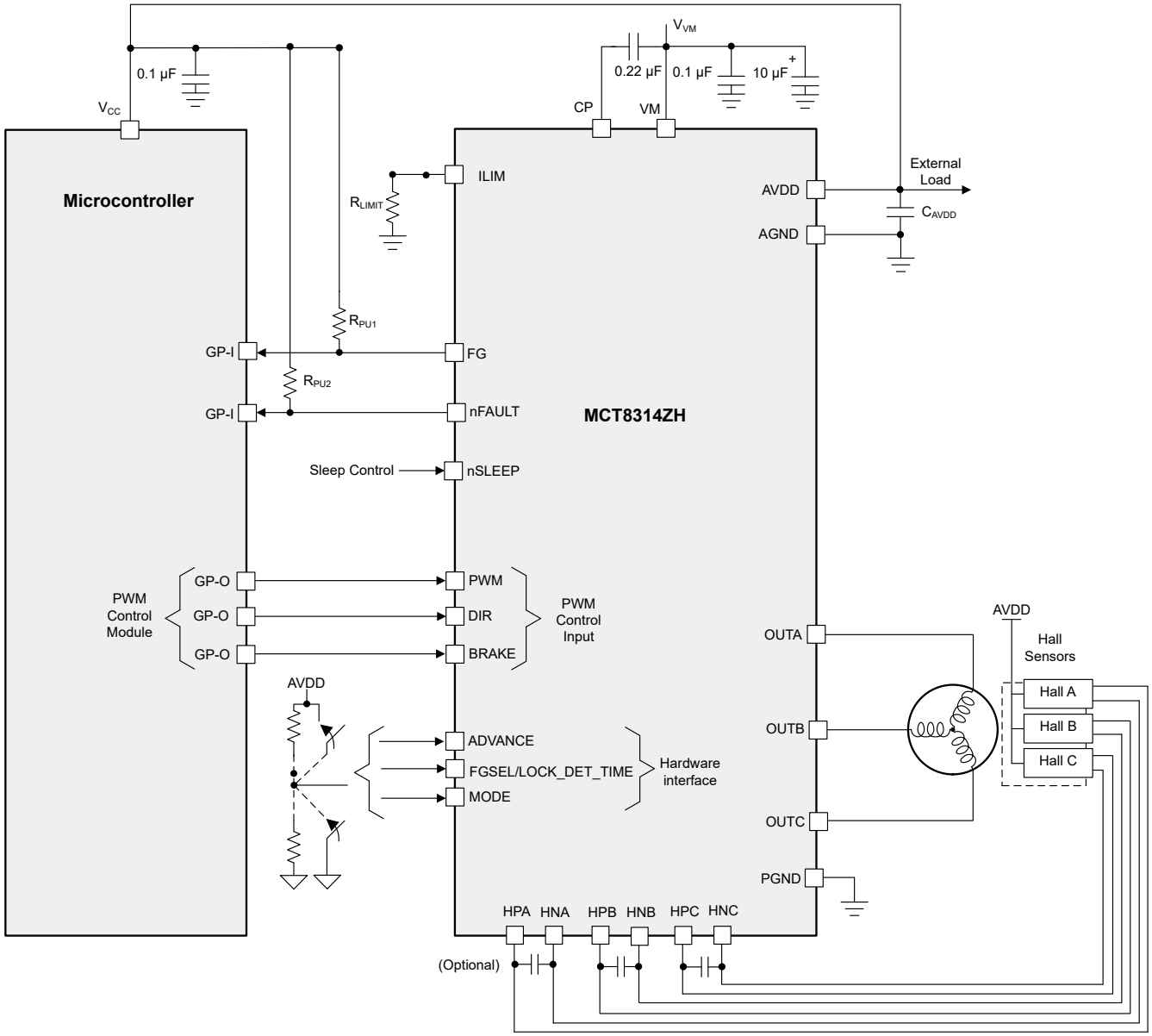


図 8-2. Primary Application Schematics for MCT8314ZH (Hardware variant)

8.2 Hall Sensor Configuration and Connection

The combinations of Hall sensor connections in this section are common connections.

8.2.1 Typical Configuration

The Hall sensor inputs on the MCT8314Z device can interface with a variety of Hall sensors. Typically, a Hall element is used, which outputs a differential signal. To use this type of sensor, the AVDD regulator can be used to power the Hall sensor. 図 8-3 shows the connections.

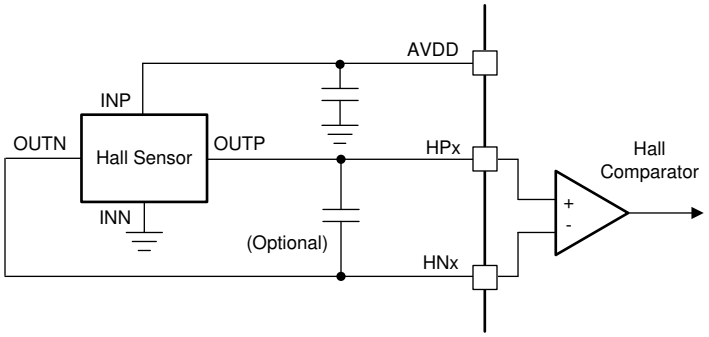


図 8-3. Typical Hall Sensor Configuration

Because the amplitude of the Hall-sensor output signal is very low, capacitors are often placed across the Hall inputs to help reject noise coupled from the motor. Capacitors with a value of 1 nF to 100 nF are typically used.

8.2.2 Open Drain Configuration

Some motors use digital Hall sensors with open-drain outputs. These sensors can also be used with the MCT8314Z device, with the addition of a few resistors as shown in 図 8-4.

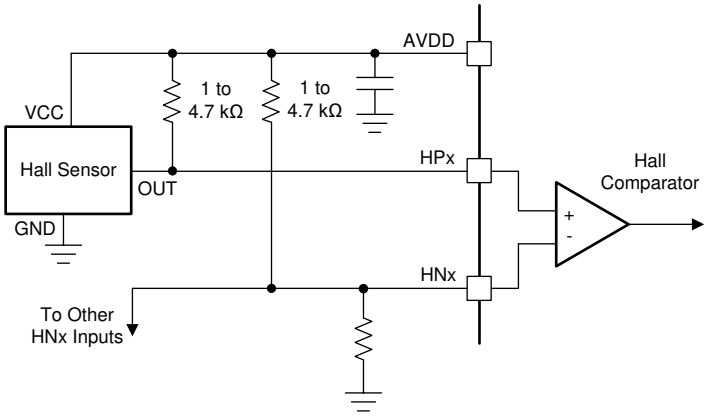


図 8-4. Open-Drain Hall Sensor Configuration

The negative (HNx) inputs are biased to AVDD / 2 by a pair of resistors between the AVDD pin and ground. For open-collector Hall sensors, an additional pullup resistor to the VREG pin is required on the positive (HPx) input. Again, the AVDD output can usually be used to supply power to the Hall sensors.

ADVANCE INFORMATION

8.2.3 Series Configuration

Hall elements are also connected in series or parallel depending upon the Hall sensor current/voltage requirement. 図 8-5 shows the series connection of Hall sensors powered via the MCT8314Z internal LDO (AVDD). This configuration is used if the current requirement per Hall sensor is high (>10 mA)

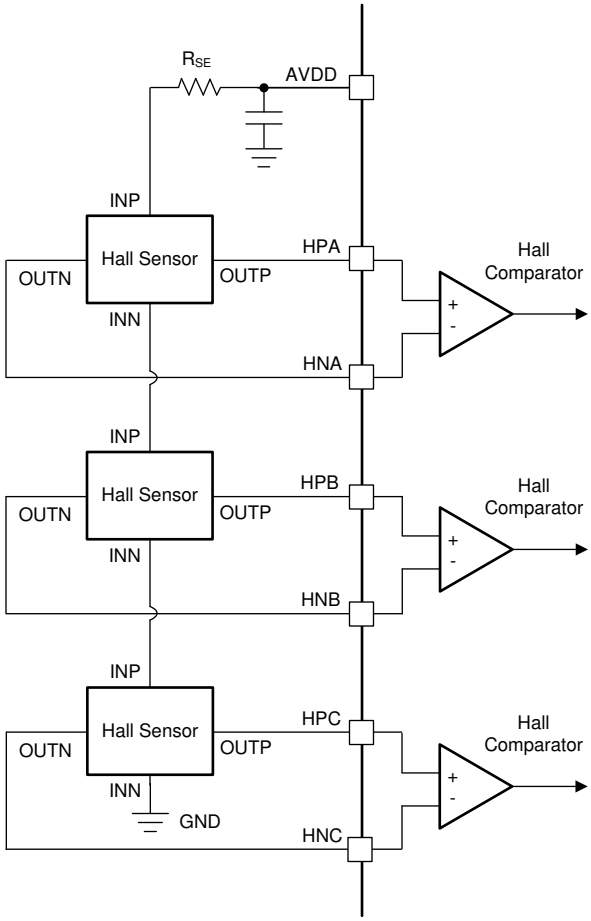


図 8-5. Hall Sensor Connected in Series Configuration

8.2.4 Parallel Configuration

図 8-6 shows the parallel connection of Hall sensors which is powered by the AVDD. This configuration can be used if the current requirement per Hall sensor is low (<10 mA).

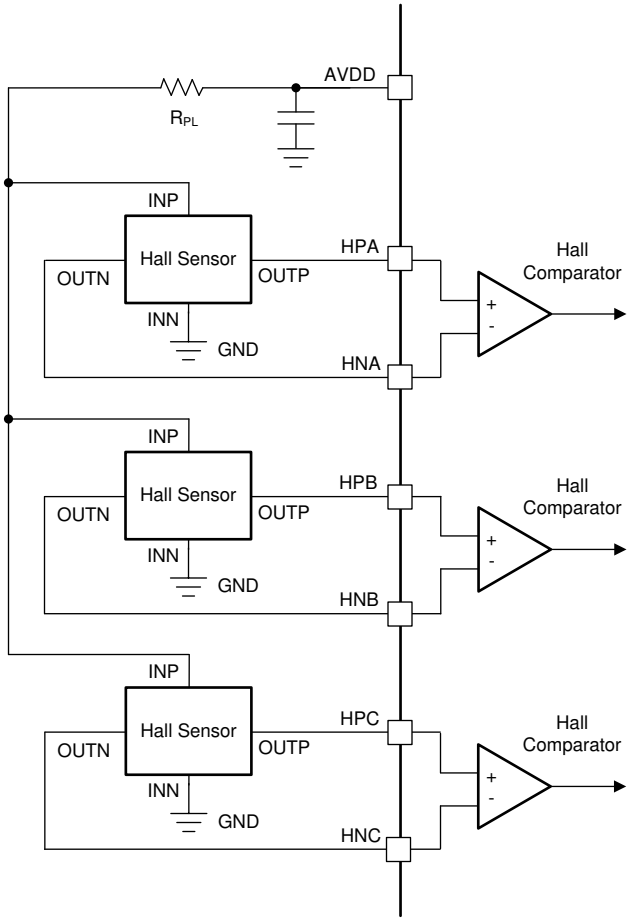


図 8-6. Hall Sensors Connected in Parallel Configuration

ADVANCE INFORMATION

8.3 Typical Applications

8.3.1 Three-Phase Brushless-DC Motor Control With Current Limit

In this application, the MCT8314Z is used to drive a brushless-DC motor with current limit up to 100% duty cycle. The following design procedure can be used to configure the MCT8314Z in current limit mode.

8.3.1.1 Detailed Design Procedure

表 8-1 lists the example input parameters for the system design.

表 8-1. Design Parameters

DESIGN PARAMETERS	REFERENCE	EXAMPLE VALUE
Supply voltage	V_{VM}	24 V
Motor peak current	I_{PEAK}	1.5 A
PWM Frequency	f_{PWM}	50 kHz
Slew Rate Setting	SR	200 V/µs
AVDD output voltage	V_{AVDD}	5.0 V

8.3.1.1.1 Motor Voltage

Brushless-DC motors are typically rated for a certain voltage (for example 12 V or 24 V). Operating a motor at a higher voltage corresponds to a lower drive current to obtain the same motor power. Operating at lower voltages generally allows for more accurate control of phase currents. The MCT8314Z functions down to a supply of 5.0V. A higher operating voltage also corresponds to a higher obtainable rpm. The MCT8314Z allows for a range of possible operating voltages because of a maximum VM rating of 40 V.

8.3.1.1.2 Using Automatic Synchronous Rectification Mode (ASR Mode)

The automatic synchronous rectification (ASR) mode in the MCT8314Z decreases power losses and thermal dissipation by reducing diode conduction losses in the low-side MOSFET. Refer to セクション 7.3.10 for more details.

8.3.1.1.3 Power Dissipation and Junction Temperature Losses

To calculate the junction temperature of the MCT8314Z from power losses, use 式 4. Note that the thermal resistance θ_{JA} depends on PCB configurations such as the ambient temperature, numbers of PCB layers, copper thickness on top and bottom layers, and the PCB area.

$$T_J[℃] = P_{loss}[W] \times \theta_{JA}\left[\frac{℃}{W}\right] + T_A[℃] \quad (4)$$

ADVANCE INFORMATION

9 Power Supply Recommendations

9.1 Bulk Capacitance

Having an appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size.

The amount of local capacitance needed depends on a variety of factors, including:

- The highest current required by the motor system
- The capacitance and current capability of the power supply
- The amount of parasitic inductance between the power supply and motor system
- The acceptable voltage ripple
- The type of motor used (brushed dc, brushless DC, stepper)
- The motor braking method

The inductance between the power supply and the motor drive system limits the rate current can change from the power supply. If the local bulk capacitance is too small, the system responds to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet generally provides a recommended value, but system-level testing is required to determine the appropriate sized bulk capacitor.

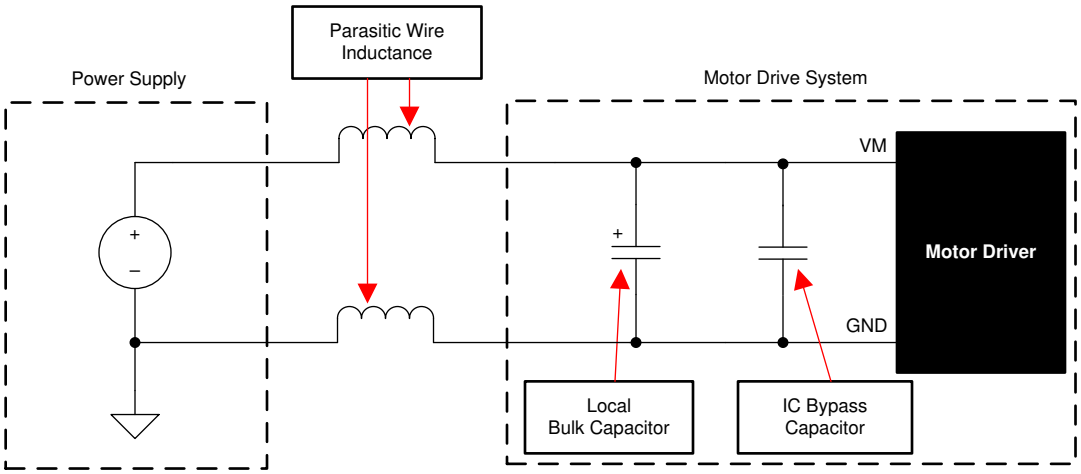


図 9-1. Example Setup of Motor Drive System With External Power Supply

The voltage rating for bulk capacitors should be higher than the operating voltage, to provide margin for cases when the motor transfers energy to the supply.

ADVANCE INFORMATION

10 Layout

10.1 Layout Guidelines

The bulk capacitor should be placed to minimize the distance of the high-current path through the motor driver device. The connecting metal trace widths should be as wide as possible, and numerous vias should be used when connecting PCB layers. These practices minimize inductance and allow the bulk capacitor to deliver high current.

Small-value capacitors such as the charge pump and AVDD capacitors should be ceramic and placed closely to device pins.

The high-current device outputs should use wide metal traces.

To reduce noise coupling and EMI interference from large transient currents into small-current signal paths, grounding should be partitioned between PGND and AGND. TI recommends connecting all non-power stage circuitry (including the thermal pad) to AGND to reduce parasitic effects and improve power dissipation from the device. Ensure grounds are connected through net-ties or wide resistors to reduce voltage offsets and maintain gate driver performance.

The device thermal pad should be soldered to the PCB top-layer ground plane. Multiple vias should be used to connect to a large bottom-layer ground plane. The use of large metal planes and multiple vias helps dissipate the $I^2 \times R_{DS(on)}$ heat that is generated in the device.

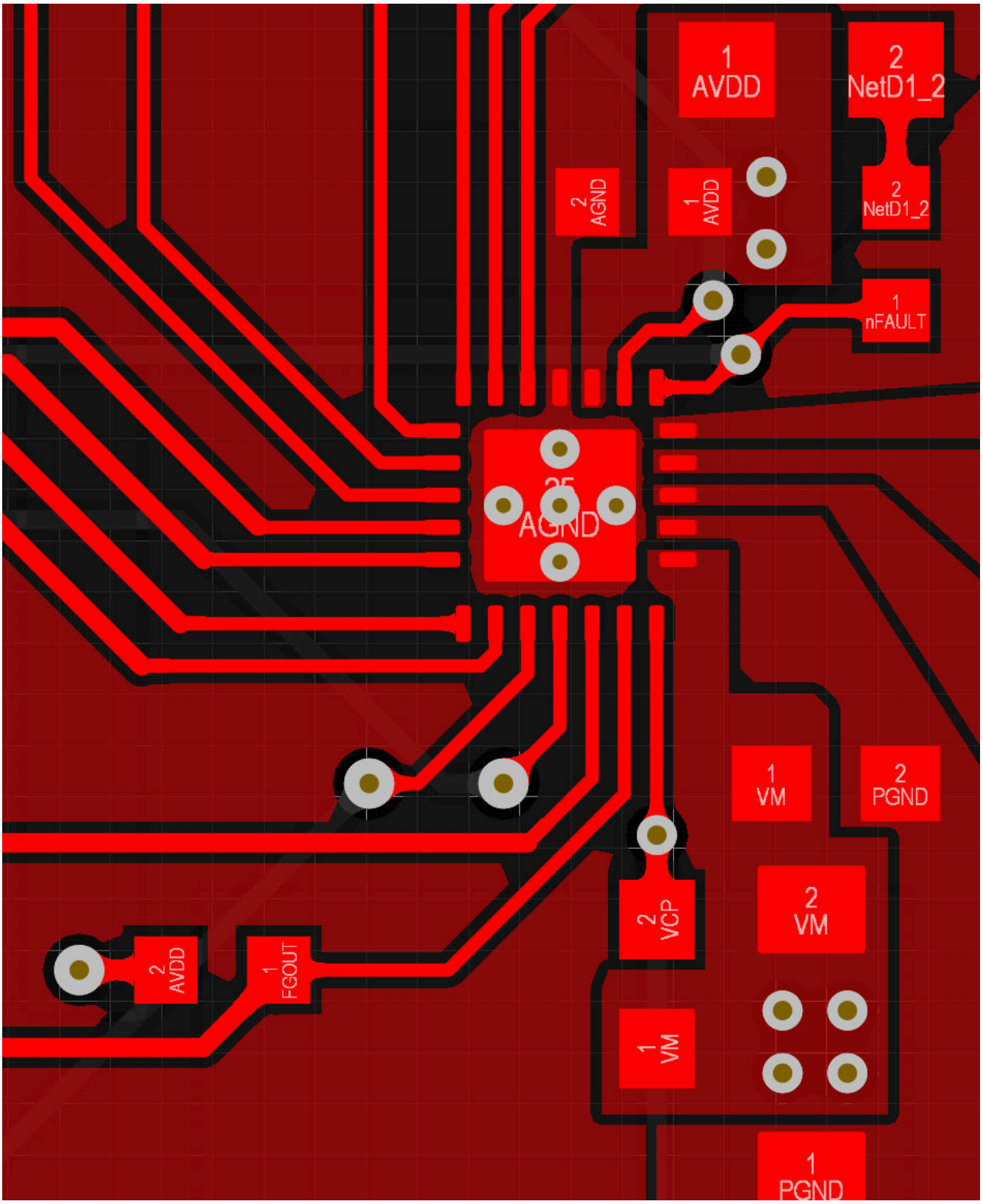
To improve thermal performance, maximize the ground area that is connected to the thermal pad ground across all possible layers of the PCB. Using thick copper pours can lower the junction-to-air thermal resistance and improve thermal dissipation from the die surface.

Recommended Layout Example for VQFN Package shows a layout example for the MCT8314Z.

ADVANCE INFORMATION

10.2 Layout Example

Recommended Layout Example for VQFN Package



ADVANCE INFORMATION

10.3 Thermal Considerations

The MCT8314Z has thermal shutdown (TSD) as previously described. A die temperature in excess of 150°C (minimally) disables the device until the temperature drops to a safe level.

Any tendency of the device to enter thermal shutdown is an indication of excessive power dissipation, insufficient heatsinking, or too high an ambient temperature.

10.3.1 Power Dissipation

The power loss in MCT8314Z include standby power losses, LDO power losses, FET conduction and switching losses, and diode losses. The FET conduction loss dominates the total power dissipation in MCT8314Z. At start-up and fault conditions, the output current is much higher than normal current; remember to take these peak currents and their duration into consideration. The total device dissipation is the power dissipated in each of the three half bridges added together. The maximum amount of power that the device can dissipate depends on ambient temperature and heatsinking. Note that RDS,ON increases with temperature, so as the device heats, the power dissipation increases. Take this into consideration when designing the PCB and heatsinking.

A summary of equations for calculating each loss is shown below for trapezoidal control.

表 10-1. MCT8314Z Power Losses for Trapezoidal Control

Loss type	Trapezoidal
Standby power	$P_{standby} = VM \times I_{VM\_TA}$
LDO (from VM)	$P_{LDO} = (VM - V_{AVDD}) \times I_{AVDD}$
FET conduction	$P_{CON} = 2 \times I_{RMS(trap)} \times R_{ds,on(TA)}$
FET switching	$P_{SW} = I_{PK(trap)} \times V_{PK(trap)} \times t_{rise/fall} \times f_{PWM}$
Diode	$P_{diode} = I_{RMS(trap)} \times V_{diode} \times t_{diode} \times f_{PWM}$

ADVANCE INFORMATION

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation, see the following:

- *Visit the MCT8314ZTEVM Tool Page*
-
- *Download the BLDC Integrated MOSFET Thermal Calculator tool*
- *Calculating Motor Driver Power Dissipation*, SLVA504
- *PowerPAD™ Thermally Enhanced Package*, SLMA002
- *PowerPAD™ Made Easy*, SLMA004
- *Sensored 3-Phase BLDC Motor Control Using MSP430*, SLAA503
- *Understanding Motor Driver Current Ratings*, SLVA505

11.2 サポート・リソース

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リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

11.3 Trademarks

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11.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.5 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

12 Revision History

DATE	REVISION	NOTES
December 2023	*	Initial release.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most-current data available for the designated device. This data is subject to change without notice and without revision of this document. For browser-based versions of this data sheet, see the left-hand navigation pane.

ADVANCE INFORMATION

13.1 Package Option Addendum

Packaging Information

Orderable Device	Status(1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan(2)	Lead/Ball Finish(6)	MSL Peak Temp(3)	Op Temp (°C)	Device Marking(4) (5)
PMCT8314Z0HRRWR	ACTIVE	WQFN	RRW	24	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	8314XP

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material).

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

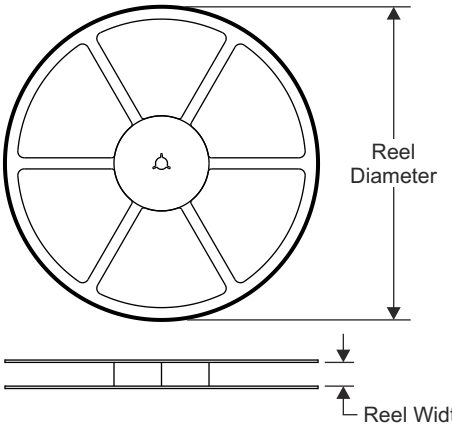
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

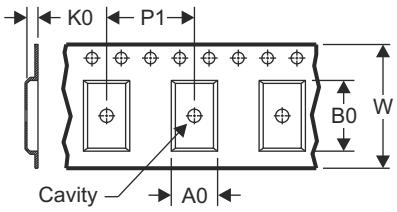
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

13.2 Tape and Reel Information

REEL DIMENSIONS

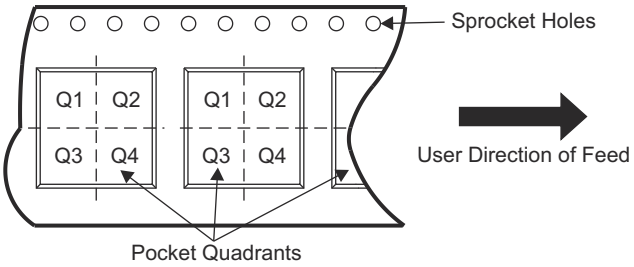


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

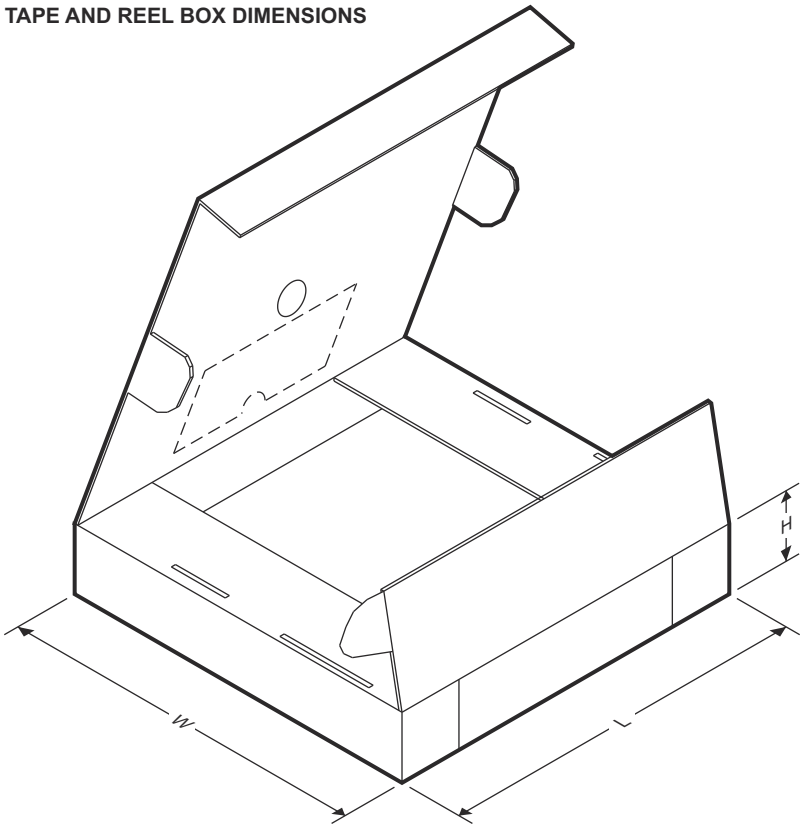


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PMCT8314Z0HRRWR	WQFN	RRW	24	5000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

ADVANCE INFORMATION

ADVANCE INFORMATION

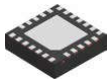
TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PMCT8314Z0HRRWR	WQFN	RRW	24	5000	367.0	367.0	35.0

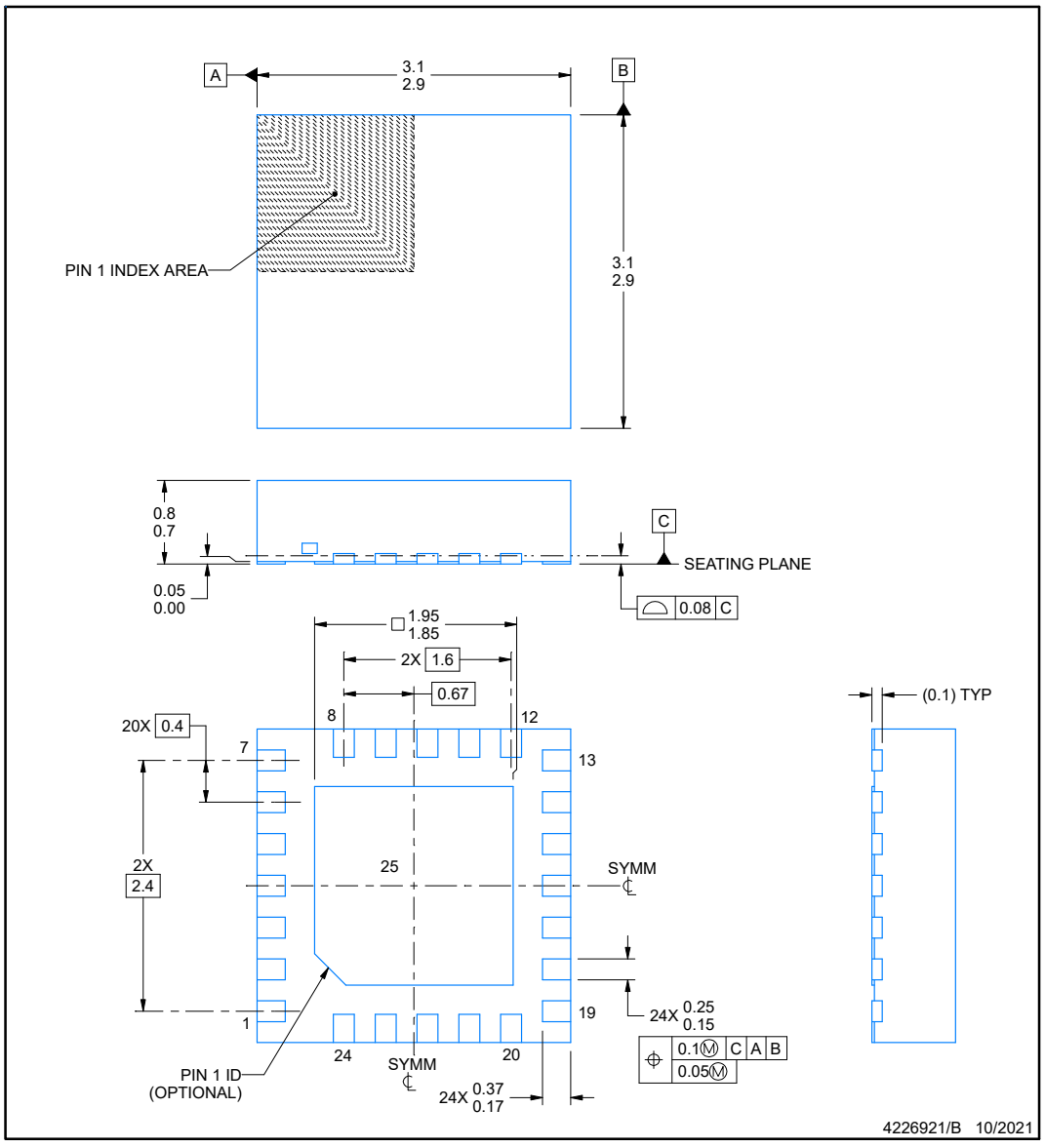
PACKAGE OUTLINE

RRW0024A



WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

www.ti.com

EXAMPLE BOARD LAYOUT

RRW0024A

WQFN - 0.8 mm max height

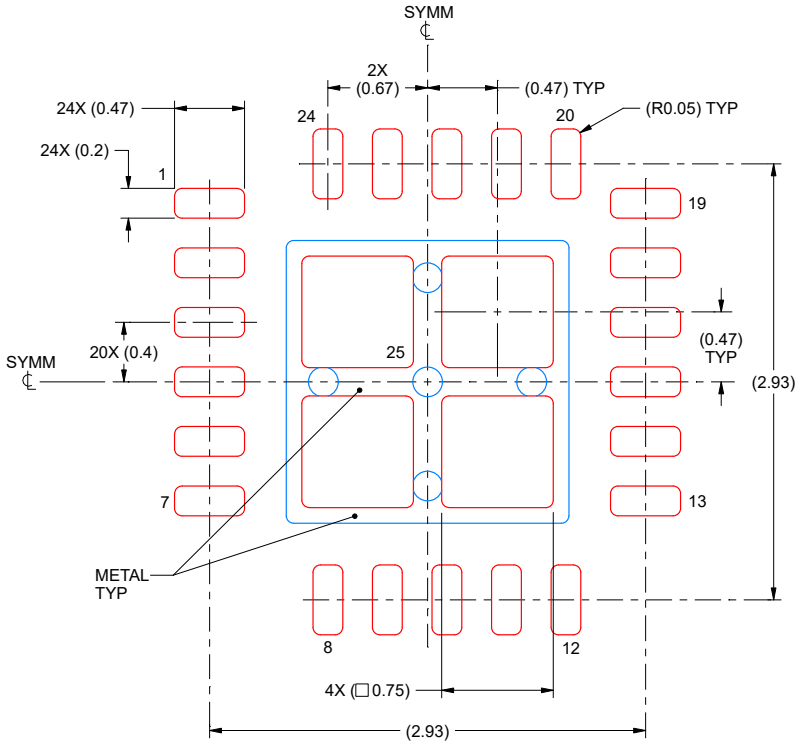
PLASTIC QUAD FLATPACK - NO LEAD

ADVANCE INFORMATION

EXAMPLE STENCIL DESIGN

RRW0024A — **WQFN - 0.8 mm max height**

PLASTIC QUAD FLATPACK - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 25:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PMCT8314Z0HRRWR	ACTIVE	WQFN	RRW	24	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

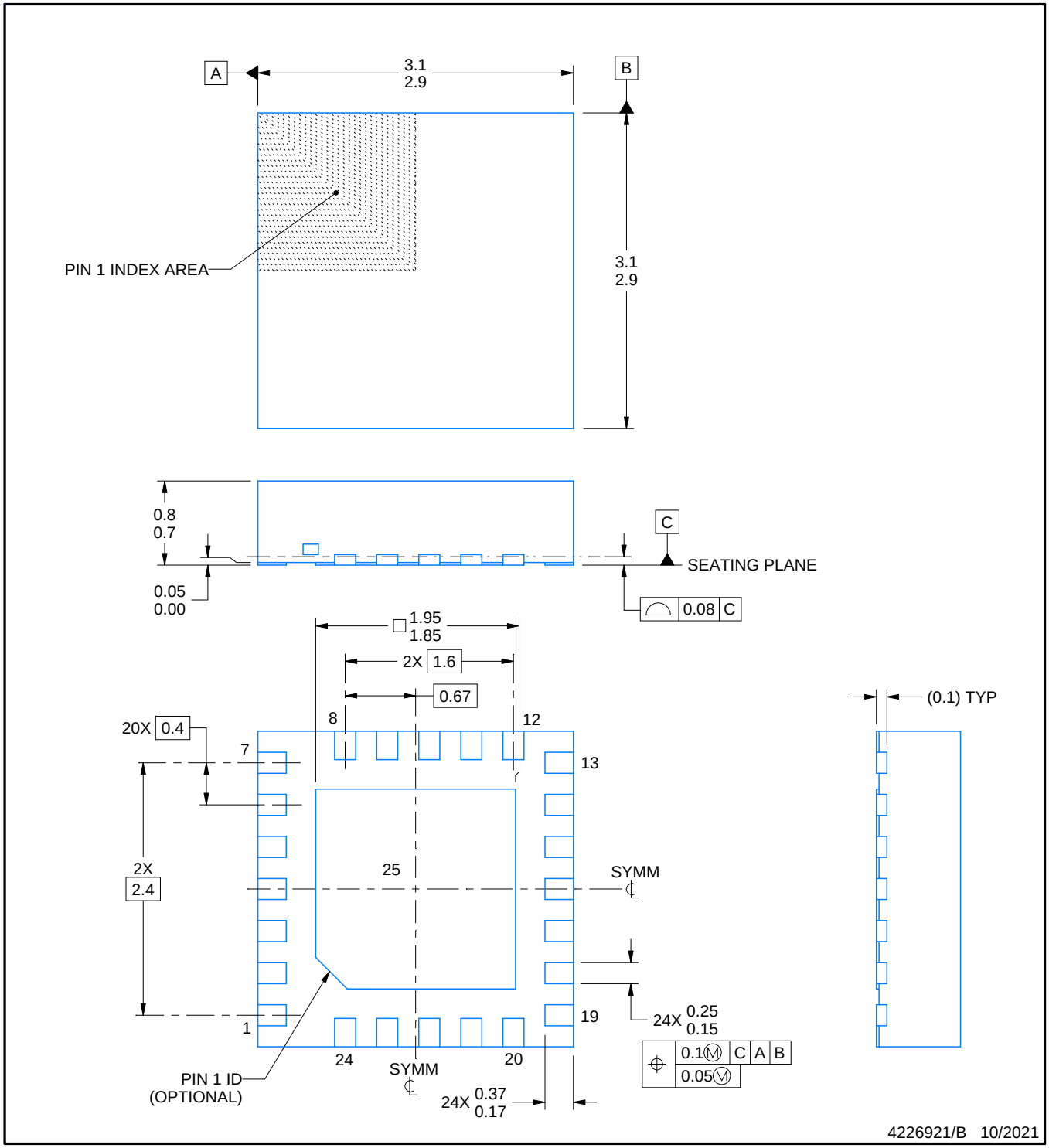
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

RRW0024A

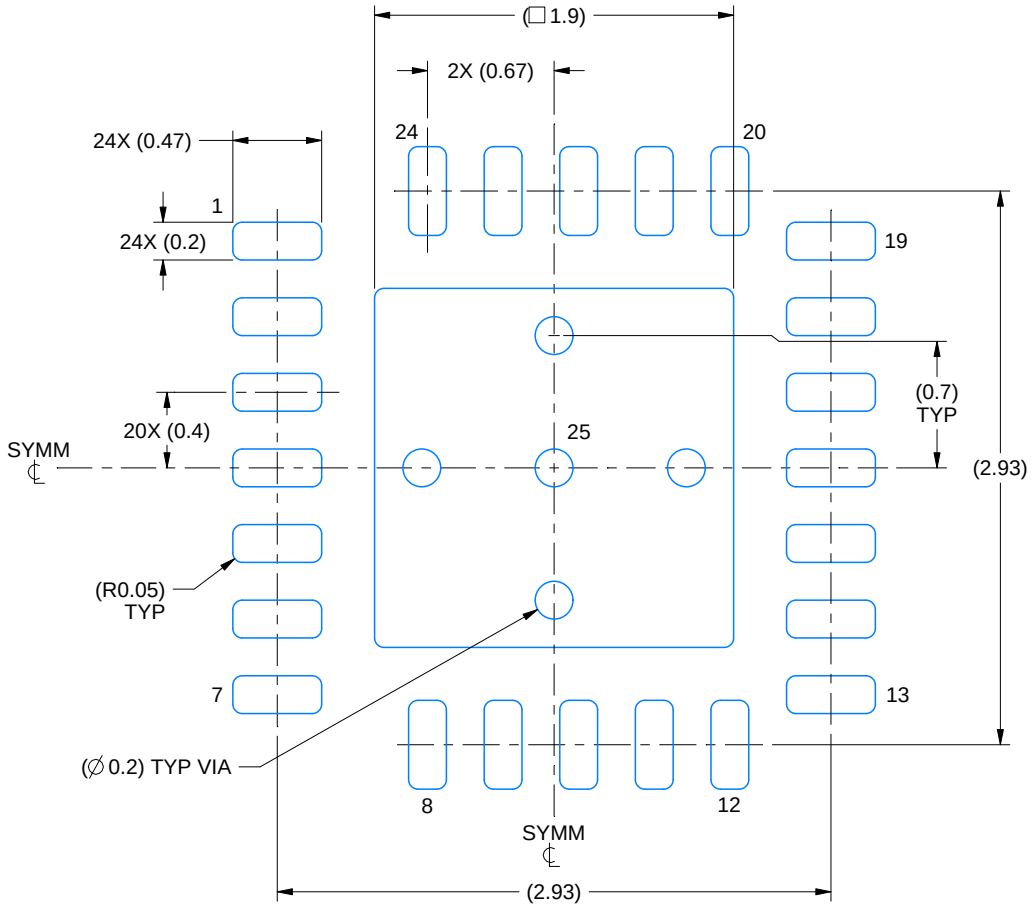
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

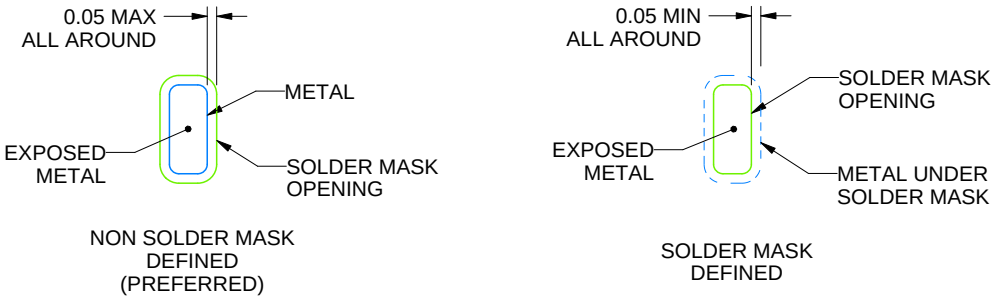


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:25X



SOLDER MASK DETAILS

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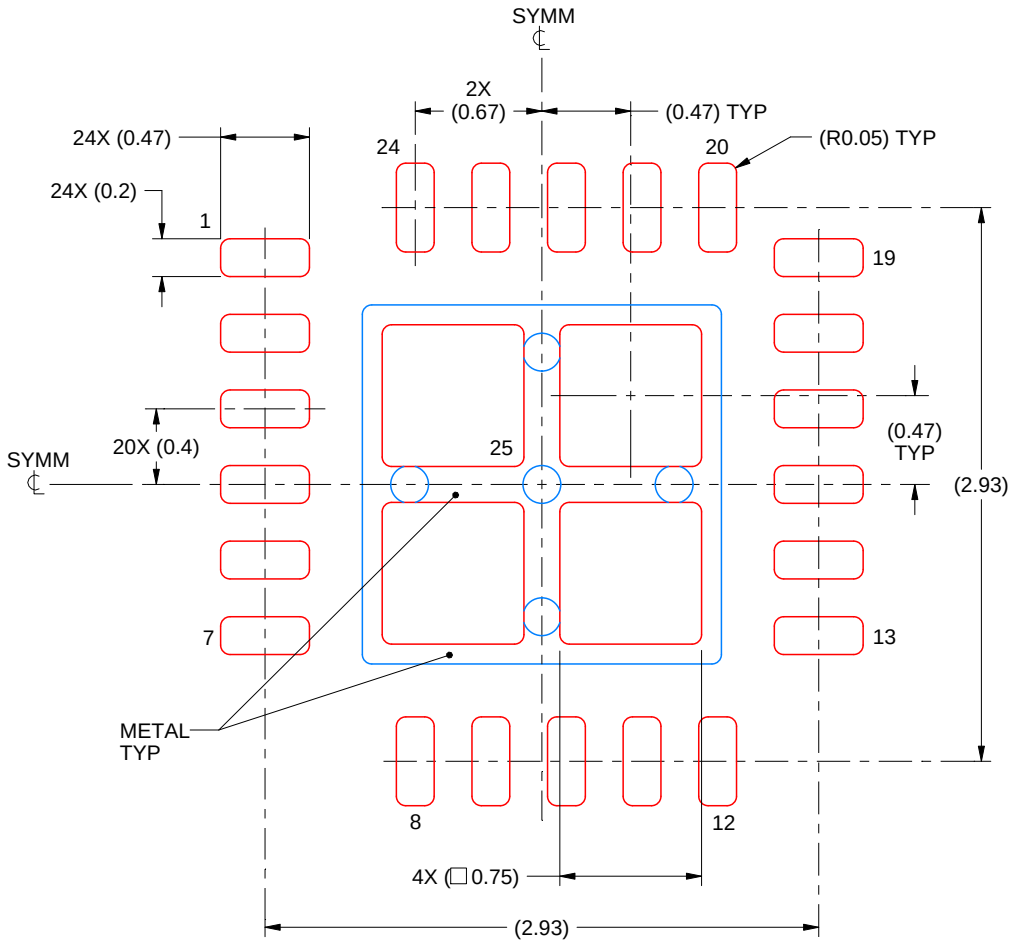
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 25:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4226921/B 10/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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