MSP430F149, MSP430F148, MSP430F147
MSP430F1491, MSP430F1481, MSP430F1471
MSP430F135, MSP430F133
JAJS263H – JULY 2000 – REVISED MAY 2018

MSP430F14x、MSP430F14x1、MSP430F13x ミクスト・シグナル・マイクロコントローラ

1 デバイスの概要

1.1 特長

- 低電源電圧範囲: 1.8V～3.6V
- 超低消費電力
  - アクティブ・モード: 1MHz、2.2Vで280µA
  - スタンバイ・モード: 1.6µA
  - オフ・モード(RAMデータ保持): 0.1µA
- 5つの省電力モード
- スタンバイ・モードから6µs以内にウェークアップ
- 16ビットRISCアーキテクチャ、命令サイクル・タイム 125ns
- 内部リファレンス、サンプル・アンド・ホールド、オートスキャン機能搭載の12ビットのA/Dコンバータ(ADC)
- 16ビットのTimer_B (7個のキャプチャ/コンペア・シャドウ・レジスタ付き)
- 16ビットのTimer_A (3個のキャプチャ/コンペア・レジスタ付き)
- オンチップのコンパレータ
- シリアル・オンボード・プログラミング、外部のプログラミング電圧不要、セキュリティ・ヒューズによるプログラム可能なコード保護
- シリアル通信インターフェイス(USART): 非同期UARTまたは同期SPIインターフェイスとして動作
  - MSP430F14xおよびMSP430F14x1デバイスには2つのUSART (USART0、USART1)を搭載
  - MSP430F13xデバイスには1つのUSART (USART0)を搭載
- ファミリ・メンバー(デバイスの比較も参照)
  - MSP430F133
    - 8KB + 256バイトのフラッシュ・メモリ、256バイトのRAM
  - MSP430F135
    - 16KB + 256バイトのフラッシュ・メモリ、512バイトのRAM
  - MSP430F147、MSP430F1471
    - 32KB + 256バイトのフラッシュ・メモリ、1KBのRAM
  - MSP430F148、MSP430F1481
    - 48KB + 256バイトのフラッシュ・メモリ、2KBのRAM
  - MSP430F149、MSP430F1491
    - 60KB + 256バイトのフラッシュ・メモリ、2KBのRAM

1.2 アプリケーション

- センサ・システム
- 産業用制御
- ハンドヘルド・メータ

1.3 概要

テキサス・インスツルメンツの MSP430™ファミリの超低消費電力マイクロコントローラ(MCU)は、各種アプリケーションを対象に異なるペリフェラルを組み合わせた複数のデバイスで構成されます。このアーキテクチャは5つの低消費電力モードを持ち、携帯用測定器用途でバッテリ駆動時間を延長するよう最適化されています。このデバイスには強力な16ビットRISC CPU、16ビット・レジスタ、および定数ジェネレータが搭載されており、これにより最大のコード効率が得られます。デジタル制御発振回路(DCO)により、低消費電力モードから6µs以内でアクティブ・モードにウェークアップできます。

MSP430F13x、MSP430F14x、MSP430F14x1 MCUには、2つの16ビット・タイマが組み込まれているほか、MSP430F13xおよびMSP430F14xデバイスでは高速な12ビットADC、MSP430F13xデバイスには1つのUSART、MSP430F14xおよびMSP430F14x1デバイスでは2つのUSARTが搭載されており、48本のI/Oピンがあります。ハードウェア乗算器により性能が向上し、コードとハードウェアに互換性を持つ広範なファミリのソリューションが得られます。

モジュールの完全な説明については、『MSP430x1xxファミリ ユーザー・ガイド』を参照してください。

英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

製品情報(1)

型番	パッケージ	本体サイズ(2)
MSP430F149IPM	LQFP (64)	10mm×10mm
MSP430F149IPAG	TQFP (64)	10mm×10mm
MSP430F1491IRTD	VQFN (64)	9mm×9mm

(1) 最新のデバイス、パッケージ、および注文情報については、8の「*付録:パッケージ・オプション*」または、www.ti.comのTI Webサイトを参照してください。
(2) ここに記載されているサイズは概略です。許容公差を含めたパッケージの寸法については、8の「メカニカル・データ」を参照してください。

1.4 機能ブロック図

MSP430F13x MCUの機能ブロック図を、図 1-1に示します。

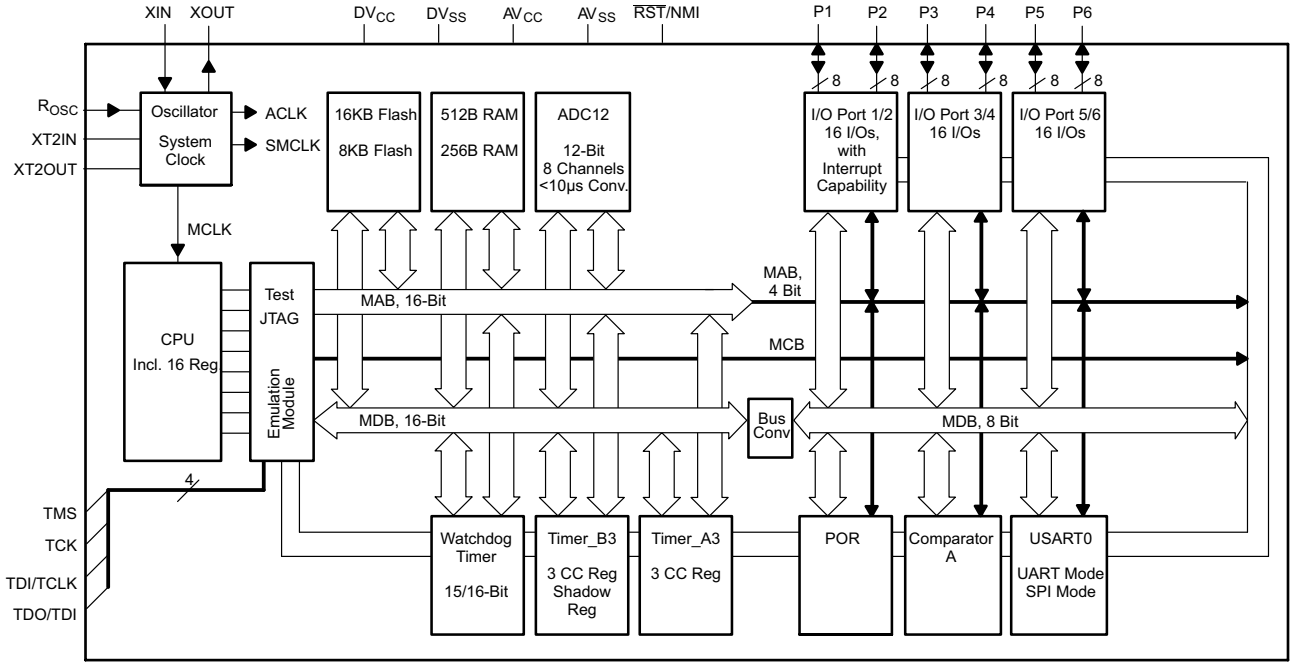


図 1-1. MSP430F13xの機能ブロック図

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MSP430F14x MCUの機能ブロック図を、図 1-2に示します。

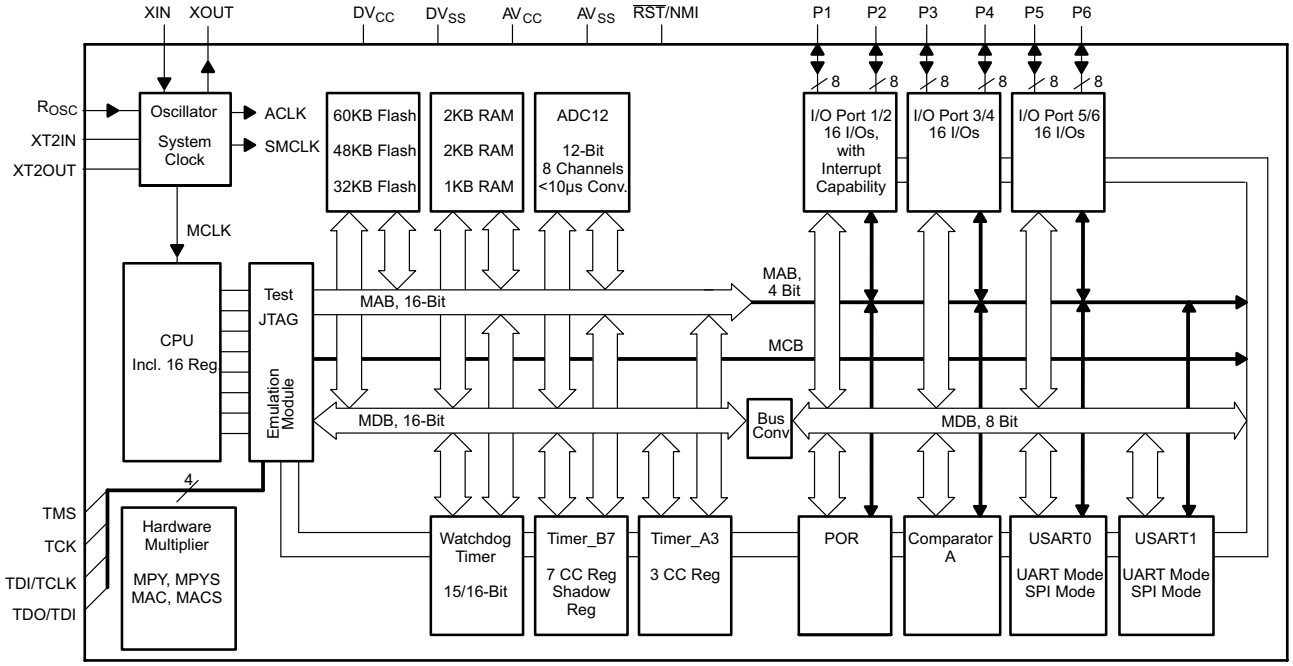


図 1-2. MSP430F14xの機能ブロック図

MSP430F14x1 MCUの機能ブロック図を、図 1-3に示します。

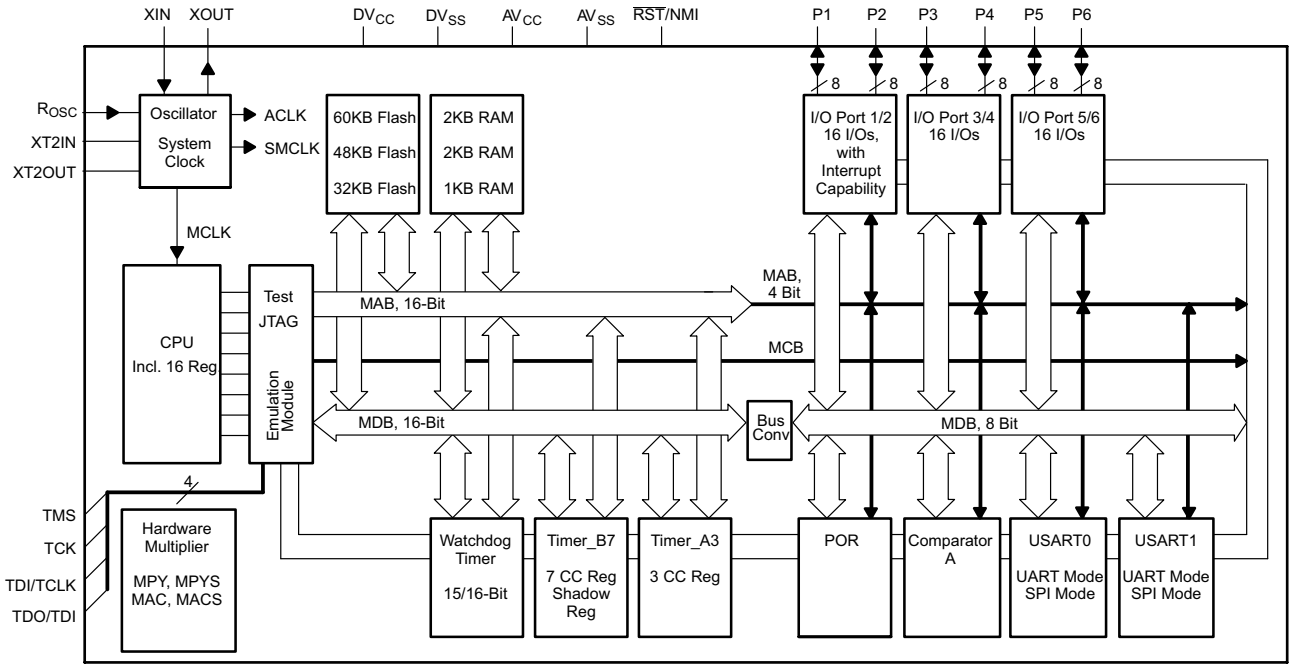


図 1-3. MSP430F14x1の機能ブロック図

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2 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2009年2月12日発行分から2018年05月23日発行分への変更 **Page**

- ドキュメント全体を通してフォーマットと構成を変更 1
- 「 1.2. アプリケーション」を追加 1
- Added Section 3, *Device Comparison* 6
- Added Section 5.2, *ESD Ratings* 16
- Removed note (2) with duplicate information from the f_{LFXT1} parameter in Section 5.3, *Recommended Operating Conditions* 16
- Removed duplicate conditions "XTS = 0, SELM = 0 or 1" from the second row of Test Conditions on the $I_{(AM)}$ parameter in Section 5.4, *Supply Current Into AV_{CC} and DV_{CC} Excluding External Current* 17
- Added Section 5.5, *Thermal Resistance Characteristics* 18
- Removed ADC12DIV from the equation in the TYP value of the $t_{CONVERT}$ parameter (because ADC12CLK is after division) in Section 5.26, *12-Bit ADC, Timing Parameters* 30
- Changed all instances of *bootstrap loader* to *bootloader* throughout document 35
- 7、「デバイスおよびドキュメントのサポート」を追加 59

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3 Device Comparison

Table 3-1 summarizes the features of the device variants in this data sheet.

Table 3-1. Device Comparison(1)(2)

Device	Flash	SRAM	Timer_A(3)	Timer_B(4)	USART	COMP_A	ADC12 (Channels)	I/Os	Package
MSP430F149	60KB	2KB	3	7	2	1	8	48	64-pin PM 64-pin PAG 64-pin RTD
MSP430F1491	60KB	2KB	3	7	2	1	8	48	64-pin PM 64-pin RTD
MSP430F148	48KB	2KB	3	7	2	1	8	48	64-pin PM 64-pin PAG 64-pin RTD
MSP430F1481	48KB	2KB	3	7	2	1	8	48	64-pin PM 64-pin RTD
MSP430F147	32KB	1KB	3	7	2	1	8	48	64-pin PM 64-pin PAG 64-pin RTD
MSP430F1471	32KB	1KB	3	7	2	1	8	48	64-pin PM 64-pin RTD
MSP430F135	16KB	512 bytes	3	3	1	1	8	48	64-pin PM 64-pin PAG 64-pin RTD
MSP430F133	8KB	256 bytes	3	3	1	1	8	48	64-pin PM 64-pin PAG 64-pin RTD

(1) For the most current package and ordering information, see the *Package Option Addendum* in 8, or see the TI website at www.ti.com.
(2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(3) Each number in the sequence represents an instantiation of Timer_A with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_A, the first instantiation having 3 and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.
(4) Each number in the sequence represents an instantiation of Timer_B with its associated number of capture/compare registers and PWM output generators available. For example, a number sequence of 3, 5 would represent two instantiations of Timer_B, the first instantiation having 3 and the second instantiation having 5 capture/compare registers and PWM output generators, respectively.

3.1 Related Products

For information about other devices in this family of products or related products, see the following links.

TI 16-bit and 32-bit microcontrollers High-performance, low-power solutions to enable the autonomous future

Products for MSP430 ultra-low-power microcontrollers One platform. One ecosystem. Endless possibilities.

Products for other MSP430 microcontrollers MCUs for metrology, monitoring, system control, and communications

Companion Products for MSP430F149 Review products that are frequently purchased or used with this product.

Reference Designs The TI Designs Reference Design Library is a robust reference design library that spans analog, embedded processor, and connectivity. Created by TI experts to help you jump start your system design, all TI Designs include schematic or block diagrams, BOMs, and design files to speed your time to market.

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4 Terminal Configuration and Functions

4.1 Pin Diagrams

Figure 4-1 shows the pinout for the MSP430F133 and MSP430F135 MCUs in the 64-pin PM, PAG, and RTD packages.

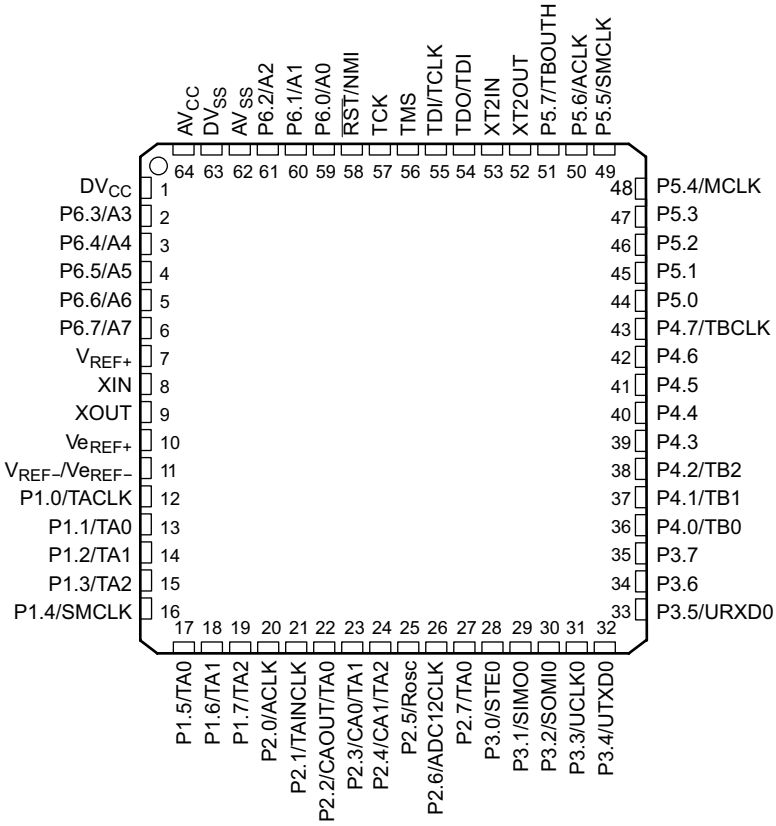


Figure 4-1. 64-Pin PM, PAG, or RTD Package (Top View) for MSP430F133 and MSP430F135

Figure 4-2 shows the pinout for the MSP430F147, MSP430F148, and MSP430F149 MCUs in the 64-pin PM, PAG, and RTD packages.

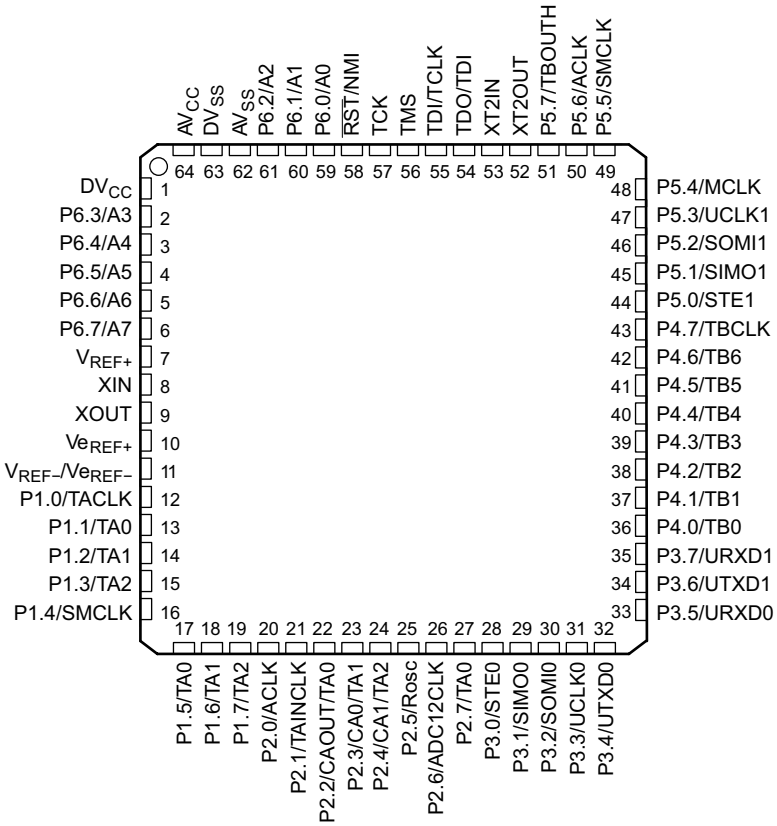


Figure 4-2. 64-Pin PM, PAG, or RTD Package (Top View) for MSP430F147, MSP430F148, and MSP430F149

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Figure 4-3 shows the pinout for the MSP430F1471, MSP430F1481, and MSP430F1491 MCUs in the 64-pin PM and RTD packages.

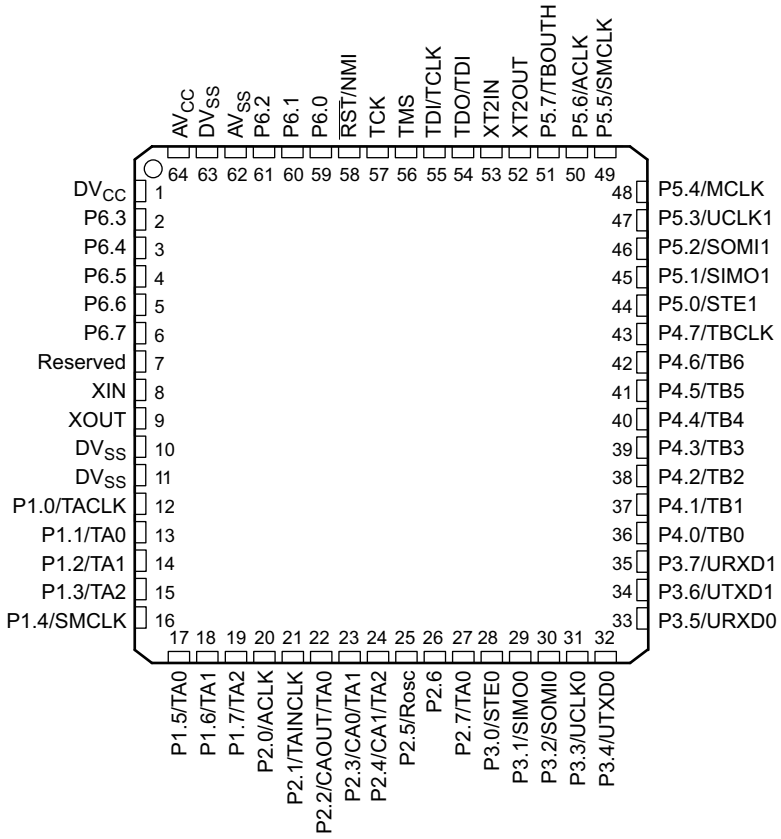


Figure 4-3. 64-Pin PM or RTD Package (Top View) for MSP430F1471, MSP430F1481, and MSP430F1491

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4.2 Signal Descriptions

Table 4-1 describes the signals for the MSP430F13x and MSP430F14x MCUs. See Table 4-2 for the MSP430F14x1 signal descriptions.

Table 4-1. Signal Descriptions for MSP430F13x and MSP430F14x

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
AV_{CC}	64		Analog supply voltage, positive terminal. Supplies the analog portion of the ADC.
AV_{SS}	62		Analog supply voltage, negative terminal. Supplies the analog portion of the ADC.
DV_{CC}	1		Digital supply voltage, positive terminal. Supplies all digital parts.
DV_{SS}	63		Digital supply voltage, negative terminal. Supplies all digital parts.
P1.0/TACLK	12	I/O	General-purpose digital I/O pin Timer_A, clock signal TACLK input
P1.1/TA0	13	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0A input, compare: Out0 output BSL transmit
P1.2/TA1	14	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0A input, compare: Out0 output BSL transmit
P1.3/TA2	15	I/O	General-purpose digital I/O pin Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK	16	I/O	General-purpose digital I/O pin SMCLK signal output
P1.5/TA0	17	I/O	General-purpose digital I/O pin Timer_A, compare: Out0 output
P1.6/TA1	18	I/O	General-purpose digital I/O pin Timer_A, compare: Out1 output
P1.7/TA2	19	I/O	General-purpose digital I/O pin Timer_A, compare: Out2 output/
P2.0/ACLK	20	I/O	General-purpose digital I/O pin ACLK output
P2.1/TAINCLK	21	I/O	General-purpose digital I/O pin Timer_A, clock signal at INCLK
P2.2/CAOUT/TA0	22	I/O	General-purpose digital I/O pin Comparator_A output Timer_A, capture: CCI0B input BSL receive
P2.3/CA0/TA1	23	I/O	General-purpose digital I/O pin Timer_A, compare: Out1 output Comparator_A input
P2.4/CA1/TA2	24	I/O	General-purpose digital I/O pin Timer_A, compare: Out2 output Comparator_A input
P2.5/R_{OSC}	25	I/O	General-purpose digital I/O pin input for external resistor defining the DCO nominal frequency
P2.6/ADC12CLK	26	I/O	General-purpose digital I/O pin Conversion clock for ADC
P2.7/TA0	27	I/O	General-purpose digital I/O pin Timer_A, compare: Out0 output
P3.0/STE0	28	I/O	General-purpose digital I/O pin Slave transmit enable for USART0 in SPI mode
P3.1/SIMO0	29	I/O	General-purpose digital I/O pin Slave in/master out of USART0 in SPI mode
P3.2/SOMI0	30	I/O	General-purpose digital I/O pin Slave out/master in of USART0 in SPI mode
P3.3/UCLK0	31	I/O	General-purpose digital I/O USART0 clock: external input in UART or SPI mode, output in SPI mode
P3.4/UTXD0	32	I/O	General-purpose digital I/O pin Transmit data out for USART0 in UART mode

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Table 4-1. Signal Descriptions for MSP430F13x and MSP430F14x (continued)

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
P3.5/URXD0	33	I/O	General-purpose digital I/O pin Receive data in for USART0 in UART mode
P3.6/UTXD1 (1)	34	I/O	General-purpose digital I/O pin Transmit data out for USART1 in UART mode
P3.7/URXD1 (1)	35	I/O	General-purpose digital I/O pin Receive data in for USART1 in UART mode
P4.0/TB0	.36	I/O	General-purpose digital I/O pin Timer_B, capture: CCI0A or CCI0B input, compare: Out0 output
P4.1/TB1	37	I/O	General-purpose digital I/O pin Timer_B, capture: CCI1A or CCI1B input, compare: Out1 output
P4.2/TB2	38	I/O	General-purpose digital I/O pin Timer_B, capture: CCI2A or CCI2B input, compare: Out2 output
P4.3/TB3 (1)	39	I/O	General-purpose digital I/O pin Timer_B, capture: CCI3A or CCI3B input, compare: Out3 output
P4.4/TB4 (1)	40	I/O	General-purpose digital I/O pin Timer_B, capture: CCI4A or CCI4B input, compare: Out4 output
P4.5/TB5 (1)	41	I/O	General-purpose digital I/O pin Timer_B, capture: CCI5A or CCI5B input, compare: Out5 output
P4.6/TB6 (1)	42	I/O	General-purpose digital I/O pin Timer_B, capture: CCI6A or CCI6B input, compare: Out6 output
P4.7/TBCLK	43	I/O	General-purpose digital I/O pin Timer_B, clock signal TBCLK input
P5.0/STE1 (1)	44	I/O	General-purpose digital I/O pin Slave transmit enable for USART1 in SPI mode
P5.1/SIMO1 (1)	45	I/O	General-purpose digital I/O pin Slave in/master out of USART1 in SPI mode
P5.2/SOMI1 (1)	46	I/O	General-purpose digital I/O pin Slave out/master in of USART1 in SPI mode
P5.3/UCLK1 (1)	47	I/O	General-purpose digital I/O pin USART1 clock: external input in UART or SPI mode, output in SPI mode
P5.4/MCLK	48	I/O	General-purpose digital I/O pin Main system clock MCLK output
P5.5/SMCLK	49	I/O	General-purpose digital I/O pin Submain system clock SMCLK output
P5.6/ACLK	50	I/O	General-purpose digital I/O pin Auxiliary clock ACLK output
P5.7/TBOUTH	51	I/O	General-purpose digital I/O pin Switch all PWM digital output ports to high impedance for Timer_B7 (TB0 to TB6)
P6.0/A0	59	I/O	General-purpose digital I/O pin Analog input A0 for ADC
P6.1/A1	60	I/O	General-purpose digital I/O pin Analog input A1 for ADC
P6.2/A2	61	I/O	General-purpose digital I/O pin Analog input A2 for ADC
P6.3/A3	2	I/O	General-purpose digital I/O pin Analog input A3 for ADC
P6.4/A4	3	I/O	General-purpose digital I/O pin Analog input A4 for ADC
P6.5/A5	4	I/O	General-purpose digital I/O pin Analog input A5 for ADC
P6.6/A6	5	I/O	General-purpose digital I/O pin Analog input A6 for ADC
P6.7/A7	6	I/O	General-purpose digital I/O pin Analog input A7 for ADC

(1) MSP430F14x devices only

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Table 4-1. Signal Descriptions for MSP430F13x and MSP430F14x (continued)

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
$\overline{\text{RST}}$/NMI	58	I	Reset input Nonmaskable interrupt input port Bootloader start
TCK	57	I	Test clock, the clock input port for device programming test and bootloader start
TDI/TCLK	55	I	Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.
TDO/TDI	54	I/O	Test data output or programming data input
TMS	56	I	Test mode select, used as an input port for device programming and test
VeREF+	10	I	Input for an external reference voltage to the ADC
VREF+	7	O	Output of positive terminal of the reference voltage in the ADC
VREF−/VeREF−	11	I	Negative terminal for the ADC reference voltage for both sources, the internal reference voltage or an external applied reference voltage
XIN	8	I	Input port for crystal oscillator XT1, standard or watch crystals can be connected
XOUT	9	O	Output terminal of crystal oscillator XT1
XT2IN	53	I	Input port for crystal oscillator XT2, only standard crystals can be connected
XT2OUT	52	O	Output terminal of crystal oscillator XT2
QFN Pad	NA	NA	QFN package pad, connect to DV_{SS}

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Table 4-2 describes the signals for the MSP430F14x1 MCUs. See Table 4-1 for the MSP430F13x and MSP430F14x signal descriptions.

Table 4-2. Signal Descriptions for MSP430F14x1

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
AV_{CC}	64		Analog supply voltage positive terminal
AV_{SS}	62		Analog supply voltage negative terminal
DV_{CC}	1		Digital supply voltage, positive terminal. Supplies all digital parts.
DV_{SS}	63		Digital supply voltage, negative terminal. Supplies all digital parts.
P1.0/TACLK	12	I/O	General-purpose digital I/O pin Timer_A, clock signal TACLK input
P1.1/TA0	13	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0A input, compare: Out0 output BSL transmit
P1.2/TA1	14	I/O	General-purpose digital I/O pin Timer_A, capture: CCI1A input, compare: Out1 output
P1.3/TA2	15	I/O	General-purpose digital I/O pin Timer_A, capture: CCI2A input, compare: Out2 output
P1.4/SMCLK	16	I/O	General-purpose digital I/O pin SMCLK signal output
P1.5/TA0	17	I/O	General-purpose digital I/O pin Timer_A, compare: Out0 output
P1.6/TA1	18	I/O	General-purpose digital I/O pin Timer_A, compare: Out1 output
P1.7/TA2	19	I/O	General-purpose digital I/O pin Timer_A, compare: Out2 output
P2.0/ACLK	20	I/O	General-purpose digital I/O pin ACLK output
P2.1/TAINCLK	21	I/O	General-purpose digital I/O pin Timer_A, clock signal at INCLK
P2.2/CAOUT/TA0	22	I/O	General-purpose digital I/O pin Timer_A, capture: CCI0B input Comparator_A output BSL receive
P2.3/CA0/TA1	23	I/O	General-purpose digital I/O pin Timer_A, compare: Out1 output Comparator_A input
P2.4/CA1/TA2	24	I/O	General-purpose digital I/O pin Timer_A, compare: Out2 output Comparator_A input
$P2.5/R_{OSC}$	25	I/O	General-purpose digital I/O pin Input for external resistor defining the DCO nominal frequency
P2.6	26	I/O	General-purpose digital I/O pin
P2.7/TA0	27	I/O	General-purpose digital I/O pin Timer_A, compare: Out0 output
P3.0/STE0	28	I/O	General-purpose digital I/O pin Slave transmit enable for USART0 in SPI mode
P3.1/SIMO0	29	I/O	General-purpose digital I/O pin Slave in/master out of USART0 in SPI mode
P3.2/SOMI0	30	I/O	General-purpose digital I/O pin Slave out/master in of USART0 in SPI mode
P3.3/UCLK0	31	I/O	General-purpose digital I/O USART0 clock: external input in UART or SPI mode, output in SPI mode
P3.4/UTXD0	32	I/O	General-purpose digital I/O pin Transmit data out for USART0 in UART mode
P3.5/URXD0	33	I/O	General-purpose digital I/O pin Receive data in for USART0 in UART mode

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Table 4-2. Signal Descriptions for MSP430F14x1 (continued)

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
P3.6/UTXD1	34	I/O	General-purpose digital I/O pin Transmit data out for USART1 in UART mode
P3.7/URXD1	35	I/O	General-purpose digital I/O pin Receive data in for USART1 in UART mode
P4.0/TB0	.36	I/O	General-purpose digital I/O pin Timer_B, capture: CCI0A or CCI0B input, compare: Out0 output
P4.1/TB1	37	I/O	General-purpose digital I/O pin Timer_B, capture: CCI1A or CCI1B input, compare: Out1 output
P4.2/TB2	38	I/O	General-purpose digital I/O pin Timer_B, capture: CCI2A or CCI2B input, compare: Out2 output
P4.3/TB3	39	I/O	General-purpose digital I/O pin Timer_B, capture: CCI3A or CCI3B input, compare: Out3 output
P4.4/TB4	40	I/O	General-purpose digital I/O pin Timer_B, capture: CCI4A or CCI4B input, compare: Out4 output
P4.5/TB5	41	I/O	General-purpose digital I/O pin Timer_B, capture: CCI5A or CCI5B input, compare: Out5 output
P4.6/TB6	42	I/O	General-purpose digital I/O pin Timer_B, capture: CCI6A or CCI6B input, compare: Out6 output
P4.7/TBCLK	43	I/O	General-purpose digital I/O pin Timer_B, clock signal TBCLK input
P5.0/STE1	44	I/O	General-purpose digital I/O pin Slave transmit enable for USART1 in SPI mode
P5.1/SIMO1	45	I/O	General-purpose digital I/O pin Slave in/master out of USART1 in SPI mode
P5.2/SOMI1	46	I/O	General-purpose digital I/O pin Slave out/master in of USART1 in SPI mode
P5.3/UCLK1	47	I/O	General-purpose digital I/O pin USART1 clock: external input in UART or SPI mode, output in SPI mode
P5.4/MCLK	48	I/O	General-purpose digital I/O pin Main system clock MCLK output
P5.5/SMCLK	49	I/O	General-purpose digital I/O pin Submain system clock SMCLK output
P5.6/ACLK	50	I/O	General-purpose digital I/O pin Auxiliary clock ACLK output
P5.7/TBOUTH	51	I/O	General-purpose digital I/O pin Switch all PWM digital output ports to high impedance for Timer_B7 (TB0 to TB6)
P6.0	59	I/O	General-purpose digital I/O pin
P6.1	60	I/O	General-purpose digital I/O pin
P6.2	61	I/O	General-purpose digital I/O pin
P6.3	2	I/O	General-purpose digital I/O pin
P6.4	3	I/O	General-purpose digital I/O pin
P6.5	4	I/O	General-purpose digital I/O pin
P6.6	5	I/O	General-purpose digital I/O pin
P6.7	6	I/O	General-purpose digital I/O pin
$\overline{\text{RST}}$/NMI	58	I	Reset input Nonmaskable interrupt input port Bootloader start
TCK	57	I	Test clock, the clock input port for device programming test and bootloader start
TDI/TCLK	55	I	Test data input or test clock input. The device protection fuse is connected to TDI/TCLK.
TDO/TDI	54	I/O	Test data output or programming data input
TMS	56	I	Test mode select, used as an input port for device programming and test
DV_{SS}	10	I	Connect to DV_{SS}
Reserved	7		Reserved, do not connect externally

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Table 4-2. Signal Descriptions for MSP430F14x1 (continued)

SIGNAL NAME	PIN NO.	I/O	DESCRIPTION
DV_{SS}	11	I	Connect to DV_{SS}
XIN	8	I	Input port for crystal oscillator XT1. Standard or watch crystals can be connected.
XOUT	9	O	Output terminal of crystal oscillator XT1
XT2IN	53	I	Input port for crystal oscillator XT2. Only standard crystals can be connected.
XT2OUT	52	O	Output terminal of crystal oscillator XT2
QFN Pad	NA	NA	QFN package pad, connect to DV_{SS}

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5 Specifications

5.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Voltage applied at V_{CC} to V_{SS}		−0.3	4.1	V
Voltage applied to any pin (2)		−0.3	V_{CC} + 0.3	V
Diode current at any device terminal			±2	mA
Storage temperature	Programmed device	−40	85	°C
	Unprogrammed device	–55	150	

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to V_{SS}, unless otherwise noted. The JTAG fuse-blow voltage, V_{FB}, is allowed to exceed the absolute maximum rating. The voltage is applied to the TDI/TCLK pin when blowing the JTAG fuse.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge ratings	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Pins listed as ±250 V may actually have higher performance.

5.3 Recommended Operating Conditions

Typical values are specified at V_{CC} = 3.3 V and T_A = 25°C (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage (AV_{CC} = DV_{CC} = V_{CC})	During program execution	1.8		3.6	V
		During flash memory programming	2.7		3.6	
V_{SS}	Supply voltage (AV_{SS} = DV_{SS} = V_{SS})		0		0	V
T_A	Operating free-air temperature		–40		85	°C
f_{LFXT1}	LFXT1 crystal frequency(1)	LF selected, XTS = 0, watch crystal		32768		Hz
		XT1 selected, XTS = 1, ceramic resonator	450		8000	kHz
		XT1 selected, XTS = 1, crystal	1000		8000	
f_{XT2}	XT2 crystal frequency(1)	Ceramic resonator	450		8000	kHz
		Crystal	1000		8000	
f_{SYSTEM}	Processor frequency (signal MCLK)	V_{CC} = 1.8 V	DC		4.15	MHz
		V_{CC} = 3.6 V	DC		8	

(1) In LF mode, the LFXT1 oscillator requires a watch crystal. TI recommends a 5.1-MΩ resistor from XOUT to V_{SS} when V_{CC} < 2.5 V.
In XT1 mode, the LFXT1 and XT2 oscillators accept a ceramic resonator or crystal up to 4.15 MHz at V_{CC} ≥ 2.2 V.
In XT1 mode, the LFXT1 and XT2 oscillators accept a ceramic resonator or crystal up to 8 MHz at V_{CC} ≥ 2.8 V.

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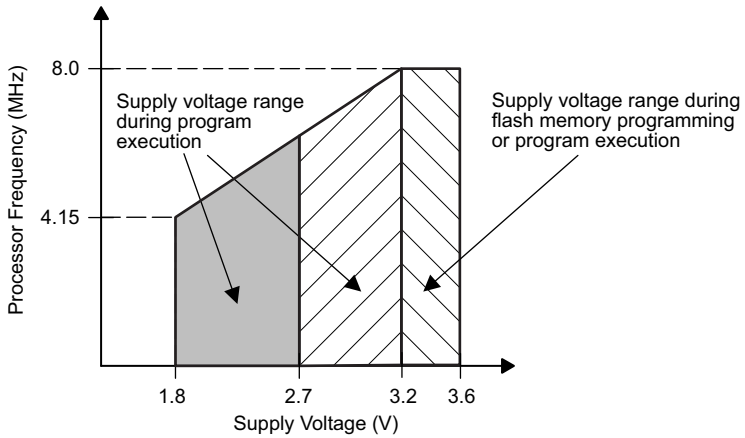


Figure 5-1. Frequency vs Supply Voltage

5.4 Supply Current Into AV_{CC} and DV_{CC} Excluding External Current

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	V_{CC}	MIN	TYP	MAX	UNIT
$I_{(AM)}$	Active mode supply current(1)	$f_{(MCLK)} = f_{(SMCLK)}$ = 1 MHz, $f_{(ACLK)}$ = 32768 Hz, XTS = 0, SELM = 0 or 1	–40°C to 85°C	2.2 V		280	360	µA
				3 V		420	560	
		$f_{(MCLK)} = f_{(SMCLK)} = f_{(ACLK)}$ = 4096 Hz, XTS = 0, SELM = 3	–40°C to 85°C	2.2 V		2.5	7	
				3 V		9	20	
$I_{(LPM0)}$	Low-power mode 0 (LPM0) supply current(1)		–40°C to 85°C	2.2 V		32	45	µA
				3 V		55	70	
$I_{(LPM2)}$	Low-power mode 2 (LPM2) supply current	$f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32768 Hz, SCG0 = 0	–40°C to 85°C	2.2 V		11	14	µA
				3 V		17	22	
$I_{(LPM3)}$	Low-power mode 3 (LPM3) supply current	$f_{(MCLK)} = f_{(SMCLK)}$ = 0 MHz, $f_{(ACLK)}$ = 32768 Hz, SCG0 = 1(2)	–40°C	2.2 V		0.8	1.5	µA
			25°C			0.9	1.5	
			85°C			1.6	2.8	
			−40°C	3 V		1.8	2.2	
			25°C			1.6	1.9	
			85°C			2.3	3.9	
$I_{(LPM4)}$	Low-power mode 4 (LPM4) supply current	$f_{(MCLK)} = f_{(SMCLK)} = f_{(ACLK)}$ = 0 MHz, SCG0 = 1	−40°C	2.2 V		0.1	0.5	µA
			25°C			0.1	0.5	
			85°C			0.8	2.5	
			−40°C	3 V		0.1	0.5	
			25°C			0.1	0.5	
			85°C			0.8	2.5	

(1) Timer_B is clocked by $f_{(DCOCLK)}$ = 1 MHz. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) Timer_B is clocked by $f_{(ACLK)}$ = 32768 Hz. All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current. The current consumption in LPM2 and LPM3 are measured with ACLK selected.

Current consumption of active mode versus system frequency

$I_{(AM)} = I_{(AM)}$ [1 MHz] × $f_{(System)}$ [MHz]

Current consumption of active mode versus supply voltage

$I_{(AM)} = I_{(AM)}$ [3 V] + 175 µA/V × (V_{CC} – 3 V)

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5.5 Thermal Resistance Characteristics

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

THERMAL METRIC[1]		VALUE[2]			UNIT
		64-PIN PM	64-PIN PAG	64-PIN RTD	
$R\theta_{JA}$	Junction-to-ambient thermal resistance, still air	52.0	52.7	25.0	°C/W
$R\theta_{JC(TOP)}$	Junction-to-case (top) thermal resistance	14.4	11.2	14.2	°C/W
$R\theta_{JB}$	Junction-to-board thermal resistance	23.0	23.4	9.6	°C/W
Ψ_{JB}	Junction-to-board thermal characterization parameter	22.7	23.1	9.5	°C/W
Ψ_{JT}	Junction-to-top thermal characterization parameter	0.6	0.3	0.2	°C/W
$R\theta_{JC(BOTTOM)}$	Junction-to-case (bottom) thermal resistance	N/A[3]	N/A[3]	1.3	°C/W

(1) For more information about traditional and new thermal metrics, see Semiconductor and IC Package Thermal Metrics.
(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC ($R\theta_{JC}$) value, which is based on a JEDEC-defined 1S0P system) and will change based on environment and application. For more information, see these EIA/JEDEC standards:
- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

(3) N/A = not applicable

5.6 Schmitt-Trigger Inputs – Ports P1, P2, P3, P4, P5, and P6

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	2.2 V	1.1	1.5	V
		3 V	1.5	1.9	
V_{IT-}	Negative-going input threshold voltage	2.2 V	0.4	0.9	V
		3 V	0.9	1.3	
V_{hys}	Input voltage hysteresis ($V_{IT+} - V_{IT-}$)	2.2 V	0.3	1.1	V
		3 V	0.5	1	

5.7 Standard Inputs – $\overline{RST}$/NMI, JTAG (TCK, TMS, TDI/TCLK, TDO/TDI)

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	MAX	UNIT
V_{IL}	Low-level input voltage	2 2 V, 3 V	V_{SS}	V_{SS} + 0.6	V
V_{IH}	High-level input voltage		0.8 × V_{CC}	V_{CC}	V

5.8 Inputs – Px.y, TAx, TBx

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{(int)}$	External interrupt timing	Port P1.x and P2.x, External trigger pulse duration to set interrupt flag[1]	2.2 V, 3 V	1.5		cycle
			2.2 V	62		ns
			3 V	50		
$t_{(cap)}$	Timer A or Timer B capture timing	TA0, TA1, TA2, TB0, TB1, TB2, TB3, TB4, TB5, TB6[2]	2.2 V	62		ns
			3 V	50		
$f_{(TAext)}$, $f_{(TBext)}$	Timer_A or Timer_B clock frequency externally applied to pin	TACLK, TBCLK, INCLK: $t_{(H)} = t_{(L)}$	2.2 V		8	MHz
			3 V		10	

(1) The external signal sets the interrupt flag every time the minimum $t_{(int)}$ cycle and time parameters are met. It may be set even with trigger signals shorter than $t_{(int)}$. Both the cycle and timing specifications must be met to ensure the flag is set. $t_{(int)}$ is measured in MCLK cycles.
(2) Seven Timer_B capture/compare registers in MSP430F14x and MSP430F14x devices, and three Timer_B capture/compare registers in MSP430F13x devices.

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Inputs – Px.y, TAx, TBx *(continued)*

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$f_{(TAint)}$, $f_{(TBint)}$	Timer_A or Timer_B clock frequency	SMCLK or ACLK signal selected	2.2 V		8	MHz
			3 V		10	

5.9 Leakage Current

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER			TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$I_{lkg(P1.x)}$	Leakage current[1]	Port P1	$V_{(P1.x)}$ [2]	2.2 V, 3 V		±50	nA
$I_{lkg(P2.x)}$		Port P2	$V_{(P2.3)}$, $V_{(P2.4)}$ [2]			±50	
$I_{lkg(P6.x)}$		Port P6	$V_{(P6.x)}$ [2]			±50	

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pin, unless otherwise noted.
(2) The port pin must be set as input, and the optional pullup or pulldown resistor must be disabled.

5.10 Outputs – Ports P1, P2, P3, P4, P5, and P6

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{OH}	High-level output voltage	$I_{(OHmax)}$ = –1 mA[1]	2.2 V	V_{CC} – 0.25	V_{CC}	V
		$I_{(OHmax)}$ = –6 mA[2]		V_{CC} – 0.60	V_{CC}	
		$I_{(OHmax)}$ = 1 mA[1]	3 V	V_{CC} – 0.25	V_{CC}	
		$I_{(OHmax)}$ = –6 mA[2]		V_{CC} – 0.60	V_{CC}	
V_{OL}	Low-level output voltage	$I_{(OLmax)}$ = 1.5 mA[1]	2.2 V	V_{SS}	V_{SS} + 0.25	V
		$I_{(OLmax)}$ = 6 mA[2]		V_{SS}	V_{SS} + 0.6	
		$I_{(OLmax)}$ = 1.5 mA[1]	3 V	V_{SS}	V_{SS} + 0.25	
		$I_{(OLmax)}$ = 6 mA[2]		V_{SS}	V_{SS} + 0.6	

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, must not exceed ±6 mA to hold the maximum voltage drop specified.
(2) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined, must not exceed ±24 mA to hold the maximum voltage drop specified.

5.11 Output Frequency

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{TAx}	Timer_A or Timer_B output frequency	Internal clock source, SMCLK signal applied[1], TA0 to TA2, TB0 to TB6, C_L = 20 pF		DC		f_{SYSTEM}	MHz
f_{ACLK}	Clock output frequency	Measured at P5.6/ACLK	C_L = 20 pF			f_{SYSTEM}	MHz
f_{MCLK}		Measured at P5.4/MCLK				f_{SYSTEM}	
f_{SMCLK}		Measured at P5.5/SMCLK				f_{SYSTEM}	
t_{Xdc}	Duty cycle of output frequency	Measured at P2.0/ACLK, C_L = 20 pF, V_{CC} = 2.2 V or 3 V	$f_{ACLK} = f_{LFXT1} = f_{XT1}$	40%		60%	
			$f_{ACLK} = f_{LFXT1} = f_{LF}$	30%		70%	
			$f_{ACLK} = f_{LFXT1/n}$		50%		
		Measured at P1 4/SMCLK, C_L = 20 pF, V_{CC} = 2.2 V or 3 V	$f_{SMCLK} = f_{LFXT1} = f_{XT1}$	40%		60%	
			$f_{SMCLK} = f_{LFXT1} = f_{LF}$	35%		65%	
			$f_{SMCLK} = f_{LFXT1/n}$	50% – 15 ns	50%	50% + 15 ns	
			$f_{SMCLK} = f_{DCOCLK}$	50% – 15 ns	50%	50% + 15 ns	

(1) The limits of the system clock MCLK must be met; the MCLK frequency must not exceed the limits. MCLK and SMCLK frequencies can be different.

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5.12 Typical Characteristics – Ports P1, P2, P3, P4, P5, and P6 Outputs

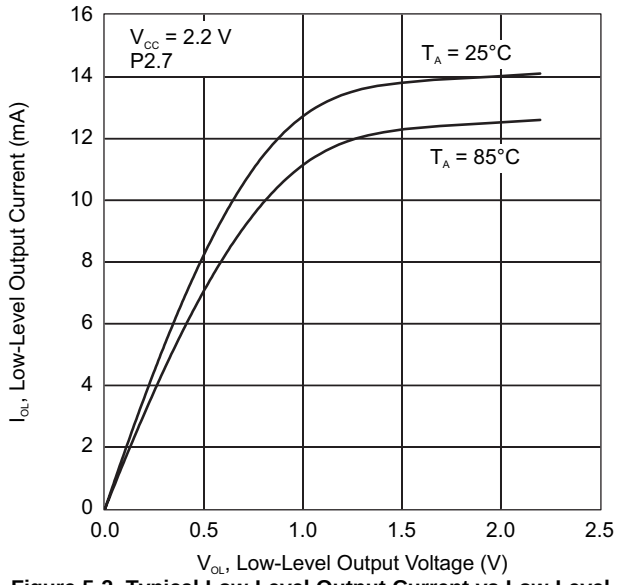


Figure 5-2. Typical Low-Level Output Current vs Low-Level Output Voltage

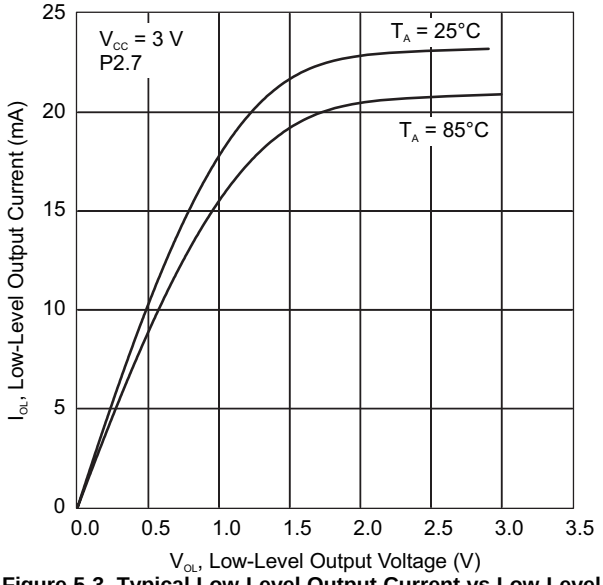


Figure 5-3. Typical Low-Level Output Current vs Low-Level Output Voltage

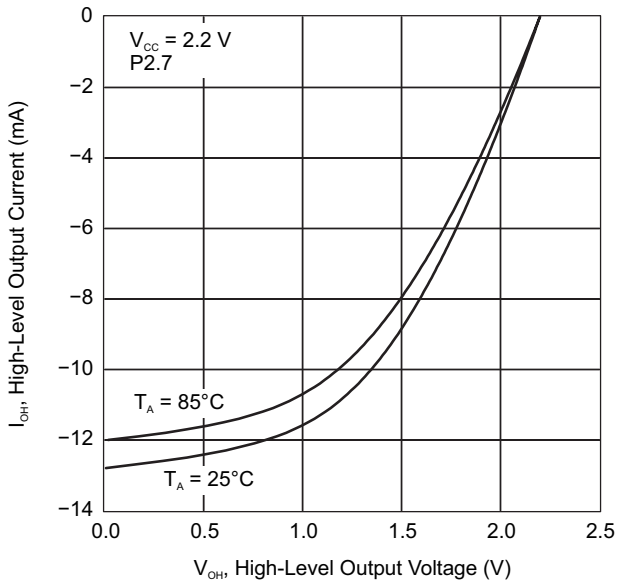


Figure 5-4. Typical High-Level Output Current vs High-Level Output Voltage

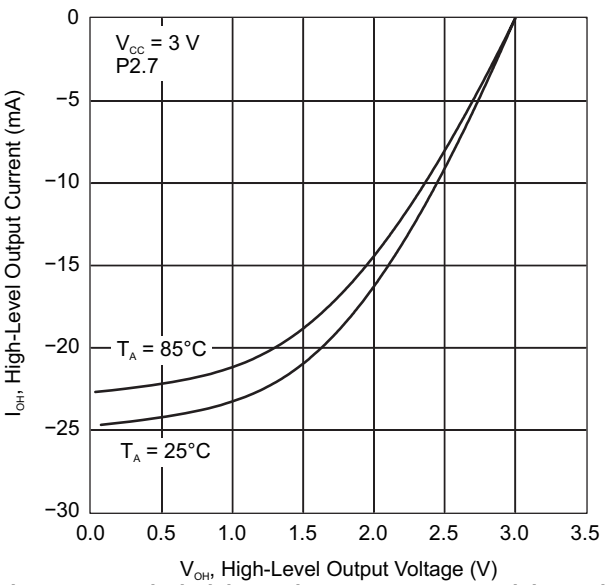


Figure 5-5. Typical High-Level Output Current vs High-Level Output Voltage

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5.13 Wake-up Time From LPM3

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{(LPM3)}$	Wake-up time from LPM3	f = 1 MHz	2.2 V, 3 V		6	µs
		f = 2 MHz			6	
		f = 3 MHz			6	

5.14 RAM

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{RAMh}	Minimum supply voltage[1]	CPU halted	1.6		V

(1) This parameter defines the minimum supply voltage when the data in program memory RAM remain unchanged. No program execution should take place during this supply voltage condition.

5.15 Comparator_A[1]

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$I_{(DD)}$	Supply current	CAON = 1 CARSEL = 0 CAREF = 0	2.2 V		25	40	µA
			3 V		45	60	
$I_{(Refladder/Refdiode)}$	Reference ladder supply current	CAON = 1, CARSEL = 0, CAREF 1, 2, or 3, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V		30	50	µA
			3 V		45	71	
$V_{(IC)}$	Common-mode input voltage	CAON = 1	2.2 V, 3 V	0		V_{CC} – 1	V
$V_{(Ref025)}$	Ratio of (voltage at 0.25 V_{CC} node) / V_{CC}	PCA0 = 1, CARSEL = 1, CAREF = 1, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V, 3 V	0.23	0.24	0.25	
$V_{(Ref050)}$	Ratio of (voltage at 0.5 V_{CC} node) / V_{CC}	PCA0 = 1, CARSEL = 1, CAREF = 2, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2	2.2 V, 3 V	0.47	0.48	0.5	
$V_{(RefVT)}$	Reference voltage (see Figure 5-6 and Figure 5-7)	PCA0 = 1, CARSEL = 1, CAREF = 3, No load at P2.3/CA0/TA1 and P2.4/CA1/TA2, T_A = 85°C	2.2 V	390	480	540	mV
			3 V	400	490	550	
$V_{(offset)}$	Offset voltage[2]		2.2 V, 3 V	–30		30	mV
V_{hys}	Input hysteresis	CAON = 1	2.2 V, 3 V	0	0.7	1.4	mV
$t_{(response\ LH)}$	Low-to-high response time	T_A = 25°C, Overdrive = 10 mV, Without filter: CAF = 0	2.2 V	130	210	300	ns
			3 V	80	150	240	
		T_A = 25°C, Overdrive = 10 mV, Without filter: CAF = 1	2.2 V	1.4	1.9	3.4	µs
			3 V	0.9	1.5	2.6	
$t_{(response\ HL)}$	High-to-low response time	T_A = 25°C, Overdrive = 10 mV, Without filter: CAF = 0	2.2 V	130	210	300	ns
			3 V	80	150	240	
		T_A = 25°C, Overdrive = 10 mV, Without filter: CAF = 1	2.2 V	1.4	1.9	3.4	µs
			3 V	0.9	1.5	2.6	

(1) The leakage current for the Comparator_A terminals is identical to the $I_{lkgPx.x)}$ specification.
(2) The input offset voltage can be cancelled by using the CAEX bit to invert the Comparator_A inputs on successive measurements.The two successive measurements are then summed together.

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5.16 Typical Characteristics – Comparator_A

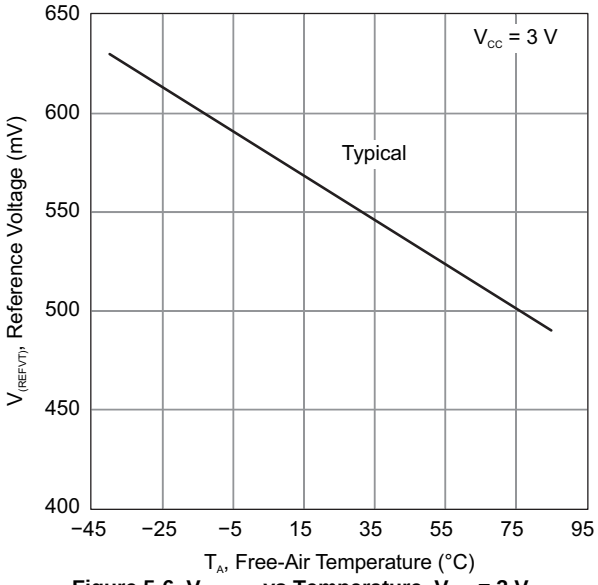


Figure 5-6. $V_{(RefVT)}$ vs Temperature, V_{CC} = 3 V

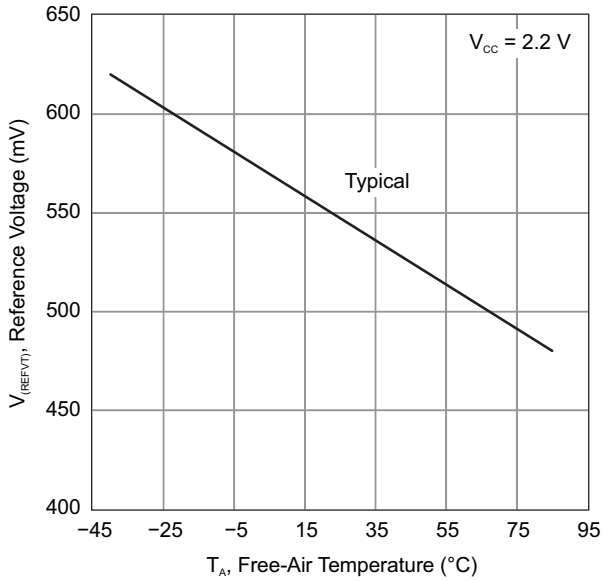


Figure 5-7. $V_{(RefVT)}$ vs Temperature, V_{CC} = 2.2 V

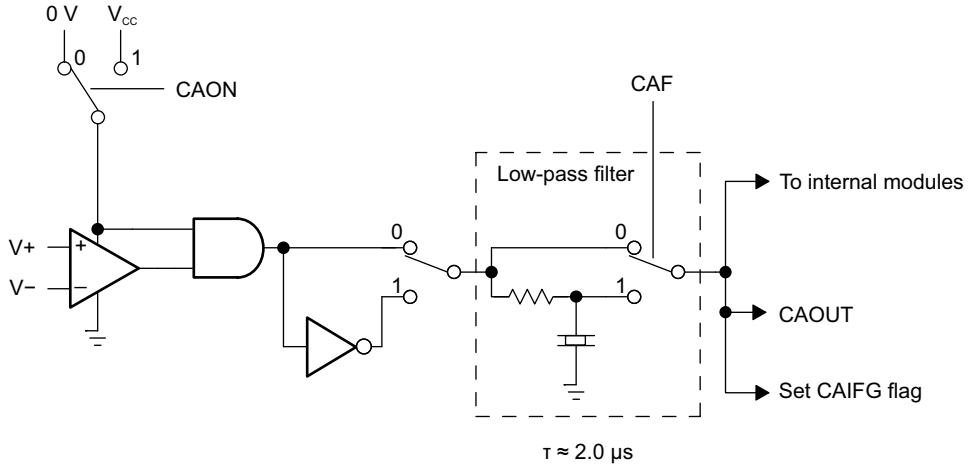


Figure 5-8. Block Diagram of Comparator_A Module

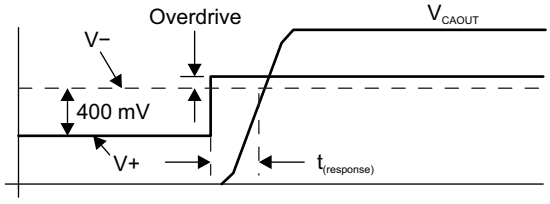


Figure 5-9. Overdrive Definition

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5.17 PUC and POR

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{(POR_Delay)}$	Internal time delay to release POR		2.2 V, 3 V		150	250	µs
V_{POR}	V_{CC} threshold at which POR release delay time begins(1)	T_A = −40°C		1.4		1.8	V
		T_A = 25°C		1.1		1.5	
		T_A = 85°C		0.8		1.2	
$V_{(min)}$	V_{CC} threshold required to generate a POR(2)	V_{CC} |dV/dt| ≥ 1 V/ms	2.2 V, 3 V	0.2			V
$t_{(reset)}$	$\overline{RST}$/NMI low time for PUC or POR	Reset is accepted internally	2.2 V, 3 V	2			µs

(1) V_{CC} rise time dV/dt ≥ 1 V/ms
(2) When driving V_{CC} low to generate a POR condition, drive V_{CC} to 200 mV or lower with a dV/dt equal to or less than −1 V/ms. The corresponding rising V_{CC} must also meet the dV/dt requirement equal to or greater than +1 V/ms.

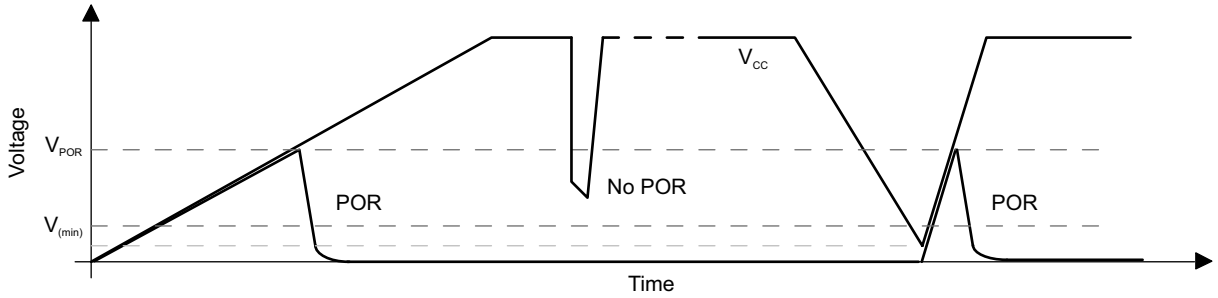


Figure 5-10. V_{POR} vs Supply Voltage

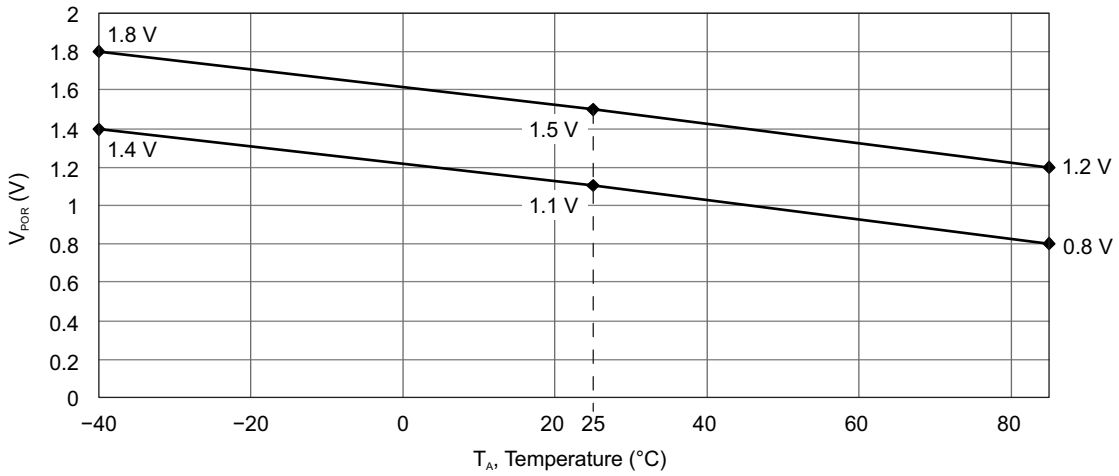


Figure 5-11. V_{POR} vs Temperature

5.18 DCO Frequency(1)

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{DCO(03)}$	Rsel = 0, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V, 3 V	0.08	0.12	0.15	MHz
			0.08	0.13	0.16	
$f_{DCO(13)}$	Rsel = 1, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V, 3 V	0.14	0.19	0.23	MHz
			0.14	0.18	0.22	
$f_{DCO(23)}$	Rsel = 2, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V, 3 V	0.22	0.30	0.36	MHz
			0.22	0.28	0.34	
$f_{DCO(33)}$	Rsel = 3, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V, 3 V	0.37	0.49	0.59	MHz
			0.37	0.47	0.56	
$f_{DCO(43)}$	Rsel = 4, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V, 3 V	0.61	0.77	0.93	MHz
			0.61	0.75	0.90	
$f_{DCO(53)}$	Rsel = 5, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V, 3 V	1	1.2	1.5	MHz
			1	1.3	1.5	
$f_{DCO(63)}$	Rsel = 6, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V, 3 V	1.6	1.9	2.2	MHz
			1.69	2.0	2.29	
$f_{DCO(73)}$	Rsel = 7, DCO = 3, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V, 3 V	2.4	2.9	3.4	MHz
			2.7	3.2	3.65	
$f_{DCO(47)}$	Rsel = 4, DCO = 7, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V, 3 V	f_{DCO40} × 1.7	f_{DCO40} × 2.1	f_{DCO40} × 2.5	MHz
$f_{DCO(77)}$	Rsel = 7, DCO = 7, MOD = 0, DCOR = 0, T_A = 25°C	2.2 V, 3 V	4	4.5	4.9	MHz
			4.4	4.9	5.4	
S_{Rsel}	$S_{Rsel} = f_{Rsel+1} / f_{Rsel}$	2.2 V, 3 V	1.35	1.65	2	
S_{DCO}	$S_{DCO} = f_{DCO+1} / f_{DCO}$	2.2 V, 3 V	1.07	1.12	1.16	
D_t	Temperature drift(2), Rsel = 4, DCO = 3, MOD = 0	2.2 V, 3 V	–0.31	–0.36	–0.40	%/°C
			–0.33	–0.38	–0.43	
D_V	Drift with V_{CC} variation(2), Rsel = 4, DCO = 3, MOD = 0	2.2 V, 3 V	0	5	10	%/V

(1) The DCO frequency may not exceed the maximum system frequency defined by the processor frequency parameter, f_{SYSTEM}.
(2) This parameter is not production tested.

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DCO Characteristics (see Figure 5-12)

- Individual devices have a minimum and maximum operation frequency. The specified parameters for $f_{DCO(x0)}$ to $f_{DCO(x7)}$ are valid for all devices.
- All ranges selected by Rsel(n) overlap with Rsel(n+1); for example, Rsel0 overlaps with Rsel1, and Rsel6 overlaps with Rsel7.
- DCO control bits DCO0, DCO1, and DCO2 have a step size as defined by parameter S_{DCO}.
- Modulation control bits MOD0 to MOD4 select how often f_{DCO+1} is used within the period of 32 DCOCLK cycles. The frequency $f_{(DCO)}$ is used for the remaining cycles. The frequency is an average equal to $f_{(DCO)} \times 2^{MOD/32}$.

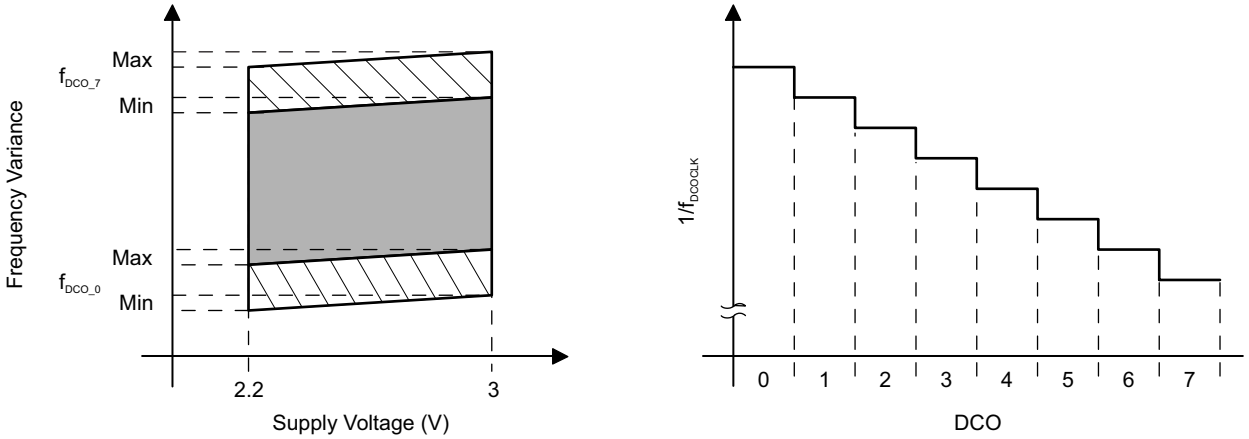


Figure 5-12. DCO Characteristics

5.19 DCO When Using R_{OSC}

over recommended operating supply voltage and free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{DCO}	DCO output frequency	Rsel = 4, DCO = 3, MOD = 0, DCOR = 1, T_A = 25°C	2.2 V		1.8 ±15%		MHz
			3 V		1.95 ±15%		
D_t	Temperature drift	Rsel = 4, DCO = 3, MOD = 0, DCOR = 1	2.2 V, 3 V		±0.1		%/°C
D_v	Drift with V_{CC} variation	Rsel = 4, DCO = 3, MOD = 0, DCOR = 1	2.2 V, 3 V		10		%/°V

(1) R_{OSC} = 100 kΩ, metal film resistor, type 0257, 0.6 W, 1% tolerance, T_K = ±50 ppm/°C

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5.20 Crystal Oscillator, LFXT1

over recommended operating supply voltage and free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
C_{XIN}	Integrated input capacitance	XTS = 0, LF oscillator selected	2.2 V, 3 V		12		pF
		XTS = 1, XT1 oscillator selected			2		
C_{XOUT}	Integrated output capacitance	XTS = 0, LF oscillator selected	2.2 V, 3 V		12		pF
		XTS = 1, XT1 oscillator selected			2		
V_{IL}	Low-level input voltage at XIN(2)		2.2 V, 3 V	V_{SS}		0.2 × V_{CC}	V
V_{IH}	High-level input voltage at XIN(2)		2.2 V, 3 V	0.8 x V_{CC}		V_{CC}	V

(1) The oscillator needs capacitors at both terminals, with values specified by the crystal manufacturer.
(2) Applies only when using an external logic-level clock source. Not applicable when using a crystal or resonator.

5.21 Crystal Oscillator, XT2

over recommended operating supply voltage and free-air temperature (unless otherwise noted)(1)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
C_{XT2IN}	Input capacitance	2.2 V, 3 V		2		pF
C_{XT2OUT}	Output capacitance	2.2 V, 3 V		2		pF
V_{IL}	Low-level input voltage at XT2IN(2)	2.2 V, 3 V	V_{SS}		0.2 × V_{CC}	V
V_{IH}	High-level input voltage at XT2IN(2)	2.2 V, 3 V	0.8 x V_{CC}		V_{CC}	V

(1) The oscillator needs capacitors at both terminals, with values specified by the crystal manufacturer.
(2) Applies only when using an external logic-level clock source. Not applicable when using a crystal or resonator.

5.22 USART0, USART1

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
$t_{(\tau)}$	USART0 or USART1 deglitch time(1)	2.2 V	200	430	800	ns
		3 V	150	280	500	

(1) The signal applied to the USART0 USART1 receive terminal (URXD0 or URXD1) must meet the timing requirements of $t_{(\tau)}$ to ensure that the URXS flip-flop is set. The URXS flip-flop is set with negative pulses meeting the minimum timing condition of $t_{(\tau)}$. The operating conditions to set the flag must be met independently from this timing constraint. The deglitch circuitry is active only on negative transitions on the URXD0 or URXD1 line.

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5.23 12-Bit ADC, Power Supply and Input Range Conditions

over recommended operating supply voltage and free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
AV_{CC}	Analog supply voltage	AV_{CC} and DV_{CC} are connected together, AV_{SS} and DV_{SS} are connected together, $V_{(AVSS)} = V_{(DVSS)} = 0$ V		2.2		3.6	V
$V_{(P6.x/Ax)}$	Analog input voltage (2)	All P6.0/A0 to P6.7/A7 terminals, analog inputs selected in ADC12MCTLx register and P6Sel.x = 1, $0 \le x \le 7$, $V_{(AVSS)} \le V_{(P6.x/Ax)} \le V_{(AVCC)}$		0		V_{AVCC}	V
I_{ADC12}	ADC operating supply current into AV_{CC} terminal(3)	$f_{ADC12CLK}$ = 5.0 MHz, ADC12ON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADC12DIV = 0	2.2 V		0.65	1.3	mA
			3 V		0.8	1.6	
I_{REF+}	REF operating supply current into AV_{CC} terminal(4)	$f_{ADC12CLK}$ = 5.0 MHz, ADC12ON = 0, REFON = 1, REF2_5V = 1	3 V		0.5	0.8	mA
		$f_{ADC12CLK}$ = 5.0 MHz, ADC12ON = 0, REFON = 1, REF2_5V = 0	2.2 V		0.5	0.8	
			3 V		0.5	0.8	
C_I	Input capacitance(5)	Only one P6.x/Ax terminal can be selected at one time	2.2 V			40	pF
R_I	Input MUX ON resistance(5)	$0 \text{ V} \le V_{Ax} \le V_{AVCC}$	3 V			2000	Ω

(1) The leakage current is defined in the leakage current table.
(2) The analog input voltage range must be within the selected reference voltage range V_R+ to V_R- for valid conversion results.
(3) The internal reference supply current is not included in current consumption parameter IADC12.
(4) The internal reference current is supplied through the AV_{CC} terminal. Consumption is independent of the ADC12ON control bit, unless a conversion is active. The REFON bit enables to settle the built-in reference before starting a conversion.
(5) Not production tested, limits verified by design.

5.24 12-Bit ADC, External Reference

over recommended operating supply voltage and free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
V_{VeREF+}	Positive external reference input voltage	$V_{VeREF+} > V_{VREF-/VeREF-}$ (2)		1.4	V_{AVCC}	V
$V_{VREF-/VeREF-}$	Negative external reference input voltage	$V_{VeREF+} > V_{VREF-/VeREF-}$ (3)		0	1.2	V
$V_{VeREF+} - V_{VREF-/VeREF-}$	Differential external reference input voltage	$V_{VeREF+} > V_{VREF-/VeREF-}$ (4)		1.4	V_{AVCC}	V
I_{VeREF+}	Static input current, VeREF+	$0 \text{ V} \le V_{VeREF+} \le V_{AVCC}$	2.2 V, 3 V		±1	μA
$I_{VREF-/VeREF-}$	Static input current, VeREF−	$0 \text{ V} \le V_{VeREF-} \le V_{AVCC}$	2.2 V, 3 V		±1	μA

(1) The external reference is used during conversion to charge and discharge the capacitance array. The input capacitance, C_I, is also the dynamic load for an external reference during conversion. The dynamic impedance of the reference supply should follow the recommendations on analog-source impedance to allow the charge to settle for 12-bit accuracy.
(2) The accuracy requirements limit the minimum positive external reference voltage. Lower reference voltage levels may be applied with reduced accuracy requirements
(3) The accuracy requirements limit the maximum negative external reference voltage. Higher reference voltage levels may be applied with reduced accuracy requirements.
(4) The accuracy requirements limit the minimum external differential reference voltage. Lower differential reference voltage levels may be applied with reduced accuracy requirements.

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5.25 12-Bit ADC, Built-In Reference

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF+}	Positive built-in reference voltage output	REF2_5V = 1 for 2.5 V, $I_{VREF+} \le I_{VREF+}$(max)	3 V	2.4	2.5	2.6	V
		REF2_5V = 0 for 1.5 V, $I_{VREF+} \le I_{VREF+}$(max)	2.2 V, 3 V	1.44	1.5	1.56	
$AV_{CC(min)}$	AV_{CC} minimum voltage, positive built-in reference active	REF2_5V = 0, $I_{VREF+} \le 1$ mA		2.2			V
		REF2_5V = 1, $I_{VREF+} \le 0.5$ mA		V_{REF+} + 0.15			
		REF2_5V = 1, $I_{VREF+} \le 1$ mA		V_{REF+} + 0.15			
I_{VREF+}	Load current out of V_{REF+} terminal		2.2 V	0.01		–0.5	mA
			3 V			–1	
$I_{L(VREF)+}$	Load-current regulation, V_{REF+} terminal(1)	I_{VREF+} = 500 µA ±100 µA, Analog input voltage ≈ 0.75 V, REF2_5V = 0	2.2 V			±2	LSB
			3 V			±2	
		I_{VREF+} = 500 µA ±100 µA, Analog input voltage ≈ 1.25 V, REF2_5V = 1	3 V			±2	LSB
$I_{DL(VREF)+}$	Load-current regulation, VREF+ terminal(2)	I_{VREF+} = 100 µA to 90 µA, C_{VREF+} = 5 µF, V_{Ax} ≈ 0 5 × V_{REF+}, Error of conversion result ≤ 1 LSB	3 V			20	ns
C_{VREF+}	Capacitance at VREF+ terminal(3)	R_{EFON} = 1, 0 mA ≤ $I_{VREF+} \le I_{VREF+}$(max)	2.2 V, 3 V	5	10		µF
T_{REF+}	Temperature coefficient of built-in reference(1)	I_{VREF+} is constant in the range of 0 mA ≤ $I_{VREF+} \le 1$ mA	2.2 V, 3 V			±100	ppm/°C
t_{REFON}	Settling time of reference voltage(4)(1) (see Figure 5-13)	I_{VREF+} = 0.5 mA, C_{VREF+} = 10 µF, V_{VREF+} = 1.5 V, V_{AVCC} = 2.2 V				17	ms

(1) Not production tested, limits characterized
(2) Not production tested, limits verified by design
(3) The internal buffer operational amplifier and the accuracy specifications require an external capacitor. All INL and DNL tests uses two capacitors between pins VREF+ and AV_{SS} and VREF−/VeREF− and AV_{SS}: 10-µF tantalum and 100-nF ceramic.
(4) The condition is that the error in a conversion started after t_{REFON} is less than ±0.5 LSB. The settling time depends on the external capacitive load.

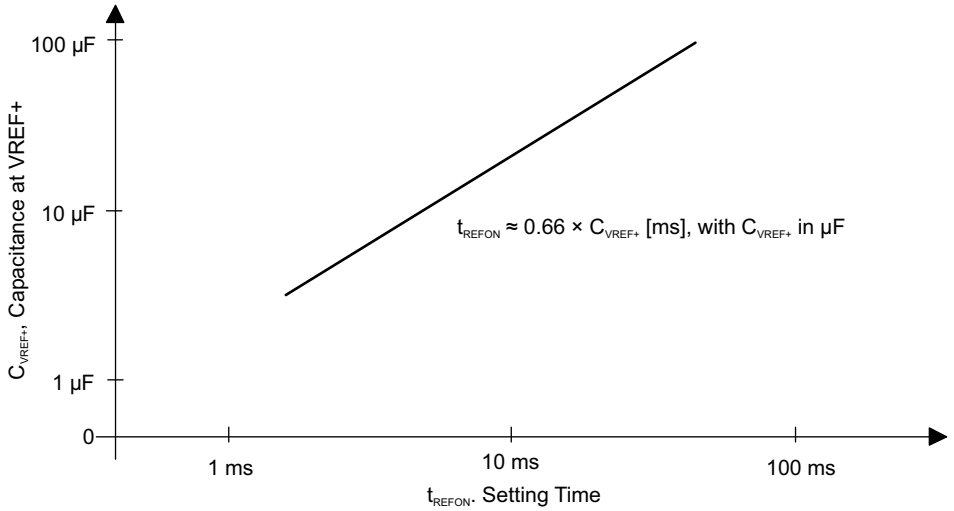


Figure 5-13. Typical Settling Time of Internal Reference (t_{REFON}) vs External Capacitor on VREF+

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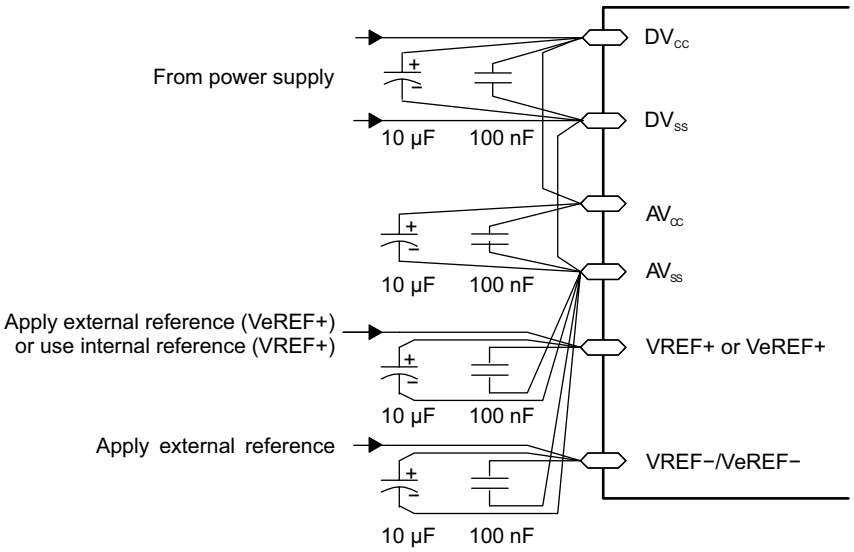


Figure 5-14. Supply Voltage and Reference Voltage Design, V_{REF-}/V_{eREF-} External Supply

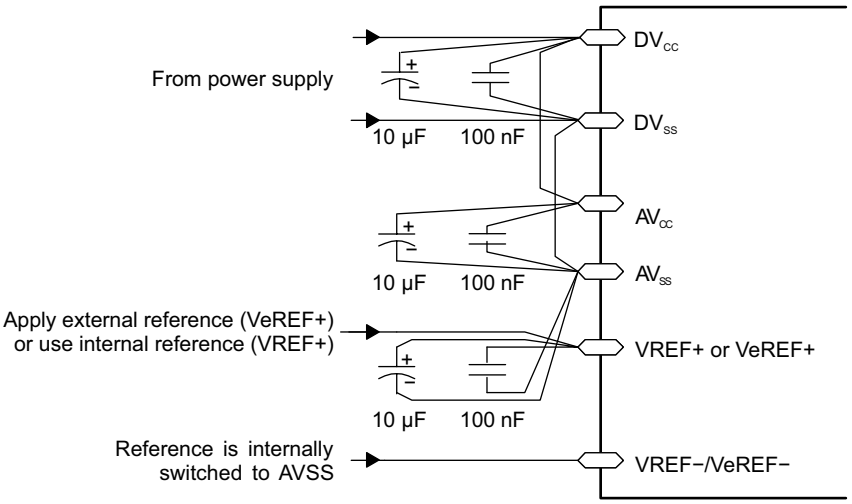


Figure 5-15. Supply Voltage and Reference Voltage Design, VREF-/VeREF- = AVSS, Internally Connected

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5.26 12-Bit ADC, Timing Parameters

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{ADC12CLK}$	ADC clock frequency	For specified performance of ADC12 linearity parameters	2.2 V, 3 V	0.45	5	6.3	MHz
$f_{ADC12OSC}$	Internal ADC12 oscillator	ADC12DIV = 0, $f_{ADC12CLK} = f_{ADC12OSC}$	2.2 V, 3 V	3.7		6.3	MHz
$t_{CONVERT}$	Conversion time	$C_{VREF+} \geq 5$ µF, internal oscillator, $f_{ADC12OSC}$ = 3.7 MHz to 6.3 MHz	2.2 V, 3 V	2.06		3.51	µs
		External $f_{ADC12CLK}$ from ACLK, MCLK or SMCLK, ADC12SSEL ≠ 0			13 × $1/f_{ADC12CLK}$		
$t_{ADC12ON}$	Turn-on settling time of the ADC (1)	See (2)				100	ns
t_{Sample}	Sampling time (1)	R_S = 400 Ω, R_I = 1000 Ω, C_I = 30 pF, $\tau = [R_S + R_I] \times C_I$ (3)	3 V	1220			ns
			2.2 V	1400			

(1) Not production tested, limits verified by design
(2) The condition is that the error in a conversion started after $t_{ADC12ON}$ is less than ±0.5 LSB. The reference and input signal are already settled.
(3) Approximately 10 Tau (τ) are needed to get an error of less than ±0.5 LSB:
$t_{Sample} = \ln(2^{n+1}) \times (R_S + R_I) \times C_I + 800$ ns, where n = ADC resolution = 12, R_S = external source resistance

5.27 12-Bit ADC, Linearity Parameters

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error	1.4 V ≤ $(V_{VeREF+} - V_{VREF-/VeREF-})$min ≤ 1.6 V	2.2 V, 3 V			±2	LSB
		1.6 V < $(V_{VeREF+} - V_{VREF-/VeREF-})$min ≤ V_{AVCC}				±1.7	
E_D	Differential linearity error	$(V_{VeREF+} - V_{VREF-/VeREF-})$min ≤ $(V_{VeREF+} - V_{VREF-/VeREF-})$, C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V, 3 V			±1	LSB
E_O	Offset error	$(V_{VeREF+} - V_{VREF-/VeREF-})$min ≤ $(V_{VeREF+} - V_{VREF-/VeREF-})$, Internal impedance of source R_S < 100 Ω, C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V, 3 V		±2	±4	LSB
E_G	Gain error	$(V_{VeREF+} - V_{VREF-/VeREF-})$min ≤ $(V_{VeREF+} - V_{VREF-/VeREF-})$, C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V, 3 V		±1.1	±2	LSB
E_T	Total unadjusted error	$(V_{VeREF+} - V_{VREF-/VeREF-})$min ≤ $(V_{VeREF+} - V_{VREF-/VeREF-})$, C_{VREF+} = 10 µF (tantalum) and 100 nF (ceramic)	2.2 V, 3 V		±2	±5	LSB

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5.28 12-Bit ADC, Temperature Sensor and Built-In V_{MID}

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{SENSOR}	Operating supply current into AV_{CC} terminal(1)	REFON = 0, INCH = 0Ah, ADC12ON = N/A, T_A = 25°C	2.2 V		40	120	µA
			3 V		60	160	
V_{SENSOR}	Sensor output voltage(2)	ADC12ON = 1, INCH = 0Ah, T_A = 0°C	2.2 V		986	986 ±5%	mV
			3 V		986	986 ±5%	
TC_{SENSOR}	Temperature coefficient of sensor output voltage(2)	ADC12ON = 1, INCH = 0Ah	2.2 V		3.55	3.55 ±3%	mV/°C
			3 V		3.55	3.55 ±3%	
$t_{SENSOR(sample)}$	Sample time required if channel 10 is selected(2)(3)	ADC12ON = 1, INCH = 0Ah, Error of conversion result ≤ 1 LSB	2.2 V	30			µs
			3 V	30			
I_{VMID}	Current into divider at channel 11 (4)	ADC12ON = 1, INCH = 0Bh	2.2 V			N/A(5)	µA
			3 V			N/A	
V_{MID}	AV_{CC} divider at channel 11	ADC12ON = 1, INCH = 0Bh, $V_{MID} \approx 0.5 \times V_{AVCC}$	2.2 V		1.1	1.1 ±0.04	V
			3 V		1.5	1.5 ±0.04	
$t_{VMID(sample)}$	Sample time required if channel 11 is selected(6)	ADC12ON = 1, INCH = 0Bh, Error of conversion result ≤ 1 LSB	2.2 V	1400			ns
			3 V	1220			

(1) The sensor current I_{SENSOR} is consumed if (ADC12ON = 1 and REFON = 1), or (ADC12ON = 1 AND INCH = 0Ah and sample signal is high). Therefore, it includes the constant current through the sensor and the reference.
(2) Not production tested, limits characterized
(3) The typical equivalent impedance of the sensor is 51 kΩ. The sample time required includes the sensor on-time, $t_{SENSOR(on)}$.
(4) No additional current is needed. The V_{MID} is used during sampling.
(5) N/A = Not applicable
(6) The on-time $t_{VMID(on)}$ is included in the sampling time $t_{VMID(sample)}$; no additional on time is needed.

5.29 Flash Memory

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{CC(PGM/ERASE)}$	Program and erase supply voltage		2.7		3.6	V
f_{FTG}	Flash timing generator frequency		257		476	kHz
I_{PGM}	Supply current from DV_{CC} during program	V_{CC} = 2.7 V or 3.6 V		3	5	mA
I_{ERASE}	Supply current from DV_{CC} during erase	V_{CC} = 2.7 V or 3.6 V		3	7	mA
t_{CPT}	Cumulative program time(1)	V_{CC} = 2.7 V or 3.6 V			4	ms
$t_{CMErase}$	Cumulative mass erase time(2)	V_{CC} = 2.7 V or 3.6 V	200			ms
	Program and erase endurance(3)		10^4	10^5		cycles
$t_{Retention}$	Data retention duration(3)	T_J = 25°C	100			years
t_{Word}	Word or byte program time(3)			35		t_{FTG}
$t_{Block, 0}$	Block program time for first byte or word(3)			30		t_{FTG}
$t_{Block, 1-63}$	Block program time for each additional byte or word(3)			21		t_{FTG}
$t_{Block, End}$	Block program end-sequence wait time(3)			6		t_{FTG}
$t_{Mass\ Erase}$	Mass erase time(3)			5297		t_{FTG}
$t_{Seg\ Erase}$	Segment erase time(3)			4819		t_{FTG}

(1) The cumulative program time must not be exceeded when writing to a 64-byte flash block. This parameter applies to all programming methods: individual word or byte write and block write modes.
(2) The mass erase duration generated by the flash timing generator is at least 11.1 ms (= 5297 × $1/f_{FTG}$, maximum = 5297 × 1/476 kHz). To achieve the required cumulative mass erase time the flash controller mass erase operation can be repeated until this time is met. A worst case minimum of 19 cycles are required.
(3) These values are hardwired into the flash controller state machine ($t_{FTG} = 1/f_{FTG}$).

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5.30 JTAG Interface

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{TCK}	TCK input frequency[1]	2.2 V	0		5	MHz
		3 V	0		10	
$R_{internal}$	Internal pullup resistance on TMS, TCK, TDI/TCLK	2.2 V, 3 V	25	60	90	kΩ

(1) f_{TCK} may be restricted to meet the timing requirements of the module selected.

5.31 JTAG Fuse [1]

over recommended operating supply voltage and free-air temperature (unless otherwise noted)

PARAMETER		T_A	MIN	MAX	UNIT
$V_{CC(FB)}$	Supply voltage during fuse blow	25°C	2.5		V
V_{FB}	Voltage level on TDI/TCLK for fuse blow		6	7	V
I_{FB}	Supply current into TDI/TCLK during fuse blow			100	mA
t_{FB}	Time to blow fuse			1	ms

(1) After the fuse is blown, no further access to the MSP430 JTAG/Test and emulation features is possible. The JTAG block is switched to bypass mode.

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6 Detailed Description

6.1 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock. Four of the registers, R0 to R3, are dedicated as program counter, stack pointer, status register, and constant generator, respectively. The remaining registers are general-purpose registers (see Figure 6-1).

Peripherals are connected to the CPU using data, address, and control buses, and can be handled with all instructions.

The instruction set consists of the original 51 instructions with three formats and seven address modes and additional instructions for the expanded address range. Each instruction can operate on word and byte data.

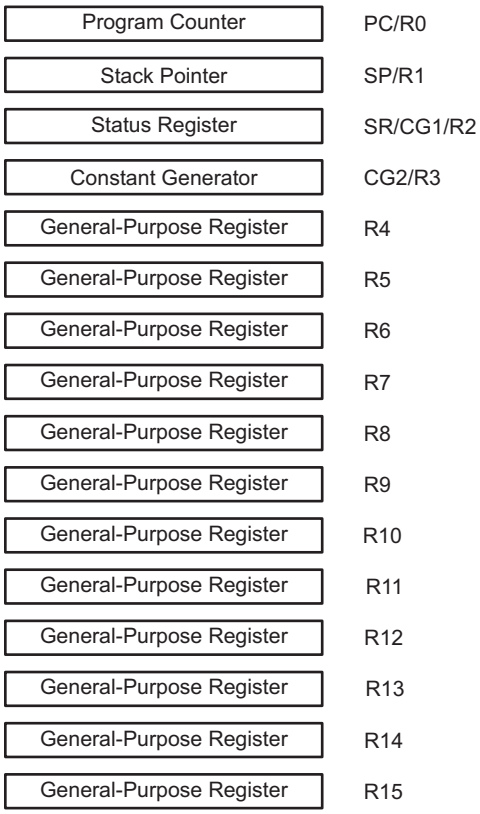


Figure 6-1. CPU Registers

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6.2 Instruction set

The instruction set consists of 51 instructions with three formats and seven address modes. Each instruction can operate on word and byte data. Table 6-1 lists examples of the three types of instruction formats, and Table 6-2 lists the address modes.

Table 6-1. Instruction Word Formats

INSTRUCTION FORMAT	EXAMPLE	OPERATION
Dual operands, source-destination	ADD R4, R5	R4 + R5 → R5
Single operands, destination only	CALL R8	PC → (TOS), R8 → PC
Relative jump, unconditional or conditional	JNE	Jump-on-equal bit = 0

Table 6-2. Address Mode Descriptions

ADDRESS MODE	S(1)	D(1)	SYNTAX	EXAMPLE	OPERATION
Register	✓	✓	MOV Rs, Rd	MOV R10, R11	R10 → R11
Indexed	✓	✓	MOV X(Rn), Y(Rm)	MOV 2(R5), 6(R6)	M(2+R5) → M(6+R6)
Symbolic (PC relative)	✓	✓	MOV EDE, TONI		M(EDE) → M(TONI)
Absolute	✓	✓	MOV &MEM, &TCDAT		M(MEM) → M(TCDAT)
Indirect	✓		MOV @Rn, Y(Rm)	MOV @R10, Tab(R6)	M(R10) → M(Tab+R6)
Indirect autoincrement	✓		MOV @Rn+, Rm	MOV @R10+, R11	M(R10) → R11 R10 + 2 → R10
Immediate	✓		MOV #X, TONI	MOV #45, TONI	#45 → M(TONI)

(1) S = source, D = destination

6.3 Operating Modes

The MSP430F13x, MSP430F14x, and MSP430F14x1 MCUs support one active mode and five software-selectable low-power modes of operation. An interrupt event can wake up the MCU from any of the low-power modes, service the request, and restore back to the low-power mode on return from the interrupt program.

The following operating modes can be configured by software:

- Active mode (AM)
  - All clocks are active
- Low-power mode 0 (LPM0)
  - CPU is disabled
  - ACLK and SMCLK remain active
  - MCLK is disabled
- Low-power mode 1 (LPM1)
  - CPU is disabled
  - ACLK and SMCLK remain active
  - MCLK is disabled
  - DC generator of the DCO is disabled if DCO not used in active mode
- Low-power mode 2 (LPM2)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DC generator of the DCO remains enabled
  - ACLK remains active
- Low-power mode 3 (LPM3)
  - CPU is disabled
  - MCLK and SMCLK are disabled
  - DC generator of the DCO is disabled
  - ACLK remains active
- Low-power mode 4 (LPM4)
  - CPU is disabled
  - ACLK is disabled
  - MCLK and SMCLK are disabled
  - DC generator of the DCO is disabled
  - Crystal oscillator is stopped

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6.4 Interrupt Vector Addresses

The interrupt vectors and the power-up starting address are in the address range 0FFFFh to 0FFE0h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence.

Table 6-3. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
Power up External reset Watchdog Flash memory	WDTIFG KEYV(1)	Reset	0FFFEh	15, highest
NMI Oscillator fault Flash memory access violation	NMIIFG OFIFG ACCVIFG(1)	(Non)maskable(2)	0FFFCh	14
Timer_B7(3)	TBCCR0 CCIFG(4)	Maskable	0FFFAh	13
Timer_B7(3)	TBCCR1 to 6 CCIFGs, TBIFG(1)(4)	Maskable	0FFF8h	12
Comparator_A	CAIFG	Maskable	0FFF9h	11
Watchdog timer	WDTIFG	Maskable	0FFF4h	10
USART0 receive	URXIFG0	Maskable	0FFF2h	9
USART0 transmit	UTXIFG0	Maskable	0FFF0h	8
ADC12(5)	ADC12IFG(1)(4)	Maskable	0FFEEh	7
Timer_A3	TACCR0 CCIFG(4)	Maskable	0FFECh	6
Timer_A3	TACCR1 CCIFG, TACCR2 CCIFG, TAIFG(1)(4)	Maskable	0FFEAh	5
I/O port P1 (eight flags)	P1IFG.0 to P1IFG.7(1)(4)	Maskable	0FFE8h	4
USART1 receive	URXIFG1	Maskable	0FFE6h	3
USART1 transmit	UTXIFG1	Maskable	0FFE4h	2
I/O port P2 (eight flags)	P2IFG.0 to P2IFG.7(1)(4)	Maskable	0FFE2h	1
–	–	–	0FFE0h	0, lowest

(1) Multiple source flags
(2) (Non)maskable: the individual interrupt-enable bit can disable an interrupt event, but the general-interrupt enable can not disable it.
(3) Timer_B7 in the MSP430F14x(1) MCUs has 7 CCRs, and Timer_B3 in the MSP430F13x MCUs has 3 CCRs. In Timer_B3, there are only interrupt flags TBCCR0, TBCCR1, and TBCCR2 CCIFGs and the interrupt-enable bits TBCCTL0, TBCCTL1, and TBCCTL2 CCIEs.
(4) Interrupt flags are located in the module.
(5) ADC12 is not implemented on the MSP430F14x1 devices.

6.5 Bootloader (BSL)

The MSP430 BSL lets users program the flash memory or RAM using a UART serial interface. Access to the MSP430 memory through the BSL is protected by a user-defined password. For complete description of the features of the BSL and its implementation, see the MSP430™ Flash Device Bootloader (BSL) User's Guide. Table 6-4 lists the pin requirements for the BSL.

Table 6-4. BSL Pin Requirements and Functions

BSL FUNCTION	PM, PAG, AND RTD PACKAGE PINS
Data transmit	13 - P1.1
Data receive	22 - P2.2

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6.6 JTAG Fuse Check Mode

MSP430 MCUs that have the fuse on the TDI/TCLK terminal have a fuse check mode that tests the continuity of the fuse the first time the JTAG port is accessed after a power-on reset (POR). When activated, a fuse check current (I_{TF}) of 1 mA at 3 V or 2.5 mA at 5 V can flow from the TDI/TCLK pin to ground if the fuse is not burned. Care must be taken to avoid accidentally activating the fuse check mode and increasing overall system power consumption.

Activation of the fuse check mode occurs with the first negative edge on the TMS pin after power up or if the TMS is being held low during power up. The second positive edge on the TMS pin deactivates the fuse check mode. After deactivation, the fuse check mode remains inactive until another POR occurs. After each POR the fuse check mode has the potential to be activated.

The fuse check current flows only when the fuse check mode is active and the TMS pin is in a low state (see Figure 6-2). Therefore, the additional current flow can be prevented by holding the TMS pin high (default condition).

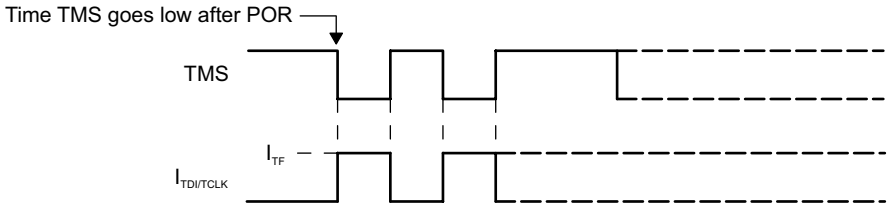


Figure 6-2. Fuse Check Mode Current

6.7 Memory

Table 6-5 summarizes the memory map of all device variants.

Table 6-5. Memory Organization

		MSP430F133	MSP430F135	MSP430F147 MSP430F1471	MSP430F148 MSP430F1481	MSP430F149 MSP430F149
Memory (flash)	Size	8KB	16KB	32KB	48KB	60KB
Main: interrupt vector	Flash	0FFFFh to 0FFE0h	0FFFFh to 0FFE0h	0FFFFh to 0FFE0h	0FFFFh to 0FFE0h	0FFFFh to 0FFE0h
Main: code memory	Flash	0FFFFh to 0E000h	0FFFFh to 0C000h	0FFFFh to 08000h	0FFFFh to 04000h	0FFFFh to 01100h
Information memory	Size	256 bytes	256 bytes	256 bytes	256 bytes	256 bytes
	Flash	010FFh to 01000h	010FFh to 01000h	010FFh to 01000h	010FFh to 01000h	010FFh to 01000h
Boot memory	Size	1KB	1KB	1KB	1KB	1KB
	Flash	0FFFh to 0C00h	0FFFh to 0C00h	0FFFh to 0C00h	0FFFh to 0C00h	0FFFh to 0C00h
RAM	Size	256 bytes	512 bytes	1KB	2KB	2KB
	RAM	02FFh to 0200h	03FFh to 0200h	05FFh to 0200h	09FFh to 0200h	09FFh to 0200h
Peripherals	16-bit	01FFh to 0100h	01FFh to 0100h	01FFh to 0100h	01FFh to 0100h	01FFh to 0100h
	8-bit	0FFh to 010h	0FFh to 010h	0FFh to 010h	0FFh to 010h	0FFh to 010h
	8-bit SFR	0Fh to 00h	0Fh to 00h	0Fh to 00h	0Fh to 00h	0Fh to 00h

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6.7.1 Flash Memory

The flash memory can be programmed through the JTAG port, the bootloader, or in-system by the CPU. The CPU can perform single-byte and single-word writes to the flash memory. Features of the flash memory include:

- Flash memory has n segments of main memory and two segments of information memory (A and B) of 128 bytes each. Each segment in main memory is 512 bytes in size.
- Segments 0 to n may be erased in one step, or each segment may be individually erased.
- Segments A and B can be erased individually, or as a group with segments 0 to n. Segments A and B are also called *information memory*.
- New devices may have some bytes programmed in the information memory (needed for test during manufacturing). The user should perform an erase of the information memory prior to the first use.

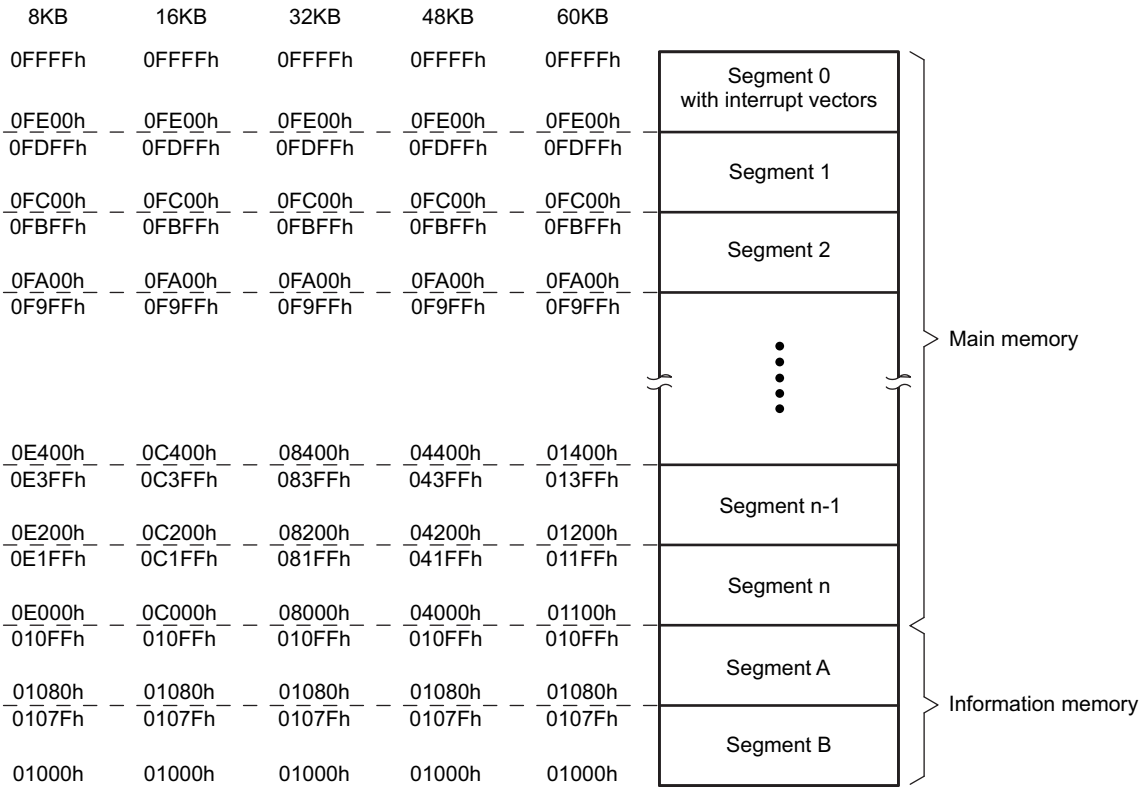


Figure 6-3. Flash Memory

6.7.2 Special Function Registers

Most interrupt and module-enable bits are collected in the lowest address space. Special-function register bits not allocated to a functional purpose are not physically present in the device. This arrangement provides simple software access.

Figure 6-4. Interrupt Enable 1 Bit Register

7	6	5	4	3	2	1	0
UTXIE0	URXIE0	ACCVIE	NMIIE	Reserved		OFIE	WDTIE
R/W-0	R/W-0	R/W-0	R/W-0	R-0		R/W-0	R/W-0

Table 6-6. Interrupt Enable 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	UTXIE0	R/W	0	USART0: UART and SPI transmit interrupt enable
6	URXIE0	R/W	0	USART0: UART and SPI receive interrupt enable
5	ACCVIE	R/W	0	Flash access violation interrupt enable
4	NMIIE	R/W	0	Nonmaskable interrupt enable
3-2	Reserved	R	0	
1	OFIE	R/W	0	Oscillator-fault interrupt enable
0	WDTIE	R/W	0	Watchdog timer interrupt enable. Inactive if watchdog mode is selected. Active if watchdog timer is configured in interval timer mode.

Figure 6-5. Interrupt Enable 2 Bit Register

7	6	5	4	3	2	1	0
Reserved		UTXIE1	URXIE1	Reserved			
R-0		R/W-0	R/W-0	R-0			

Table 6-7. Interrupt Enable 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R	0	
5	UTXIE1	R/W	0	USART1: UART and SPI receive interrupt enable
4	URXIE1	R/W	0	USART1: UART and SPI transmit interrupt enable
3-0	Reserved	R/W	0	

Figure 6-6. Interrupt Flag 1 Bit Register

7	6	5	4	3	2	1	0
UTXIFG0	URXIFG0	Reserved	NMIIFG	Reserved		OFIFG	WDTIFG
R/W-1	R/W-0	R-0	R/W-0	R-0		R/W-1	R/W-(0)

Table 6-8. Interrupt Flag 1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	UTXIFG0	R/W	1	USART0: UART and SPI transmit flag
6	URXIFG0	R/W	0	USART0: UART and SPI receive flag
5	Reserved	R	0	
4	NMIIFG	R/W	0	Set by $\overline{\text{RST}}$/NMI pin
3-2	Reserved	R	0	
1	OFIFG	R/W	1	Flag set on oscillator fault
0	WDTIFG	R/W	(0)	Set on watchdog timer overflow (in watchdog mode) or security key violation. Reset on V_{CC} power up or a reset condition at the $\overline{\text{RST}}$/NMI pin in reset mode.

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Figure 6-7. Interrupt Flag 2 Bit Register

7	6	5	4	3	2	1	0
Reserved		UTXIFG1	URXIFG1	Reserved			
R-0		R/W-1	R/W-0	R-0			

Table 6-9. Interrupt Flag 2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R	0	
5	UTXIFG1	R/W	1	USART1: UART and SPI transmit flag
4	URXIFG1	R/W	0	USART1: UART and SPI receive flag
3-0	Reserved	R	0	

Figure 6-8. Module Enable 1 Bit Register

7	6	5	4	3	2	1	0
UTXE0	URXE0 USPIE0	Reserved					
R/W-0	R/W-0	R-0					

Table 6-10. Module Enable 1 Bit Register Field Descriptions

Bit	Field	Type	Reset	Description
7	UTXE0	R/W	0	USART0: UART transmit enable
6	URXE0 USPIE0	R/W	0	USART0: UART receive enable USART0: SPI (synchronous peripheral interface) transmit and receive enable
5-0	Reserved	R	0	

Figure 6-9. Module Enable 2 Bit Register

7	6	5	4	3	2	1	0
Reserved		UTXE1	URXE1 USPIE1	Reserved			
R-0		R/W-0	R/W-0	R-0			

Table 6-11. Module Enable 2 Bit Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	Reserved	R	0	
5		R/W	0	USART1: UART transmit enable
4	URXE1 USPIE1	R/W	0	USART1: UART receive enable USART1: SPI (synchronous peripheral interface) transmit and receive enable
3-0	Reserved	R	0	

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6.8 Peripherals

Peripherals are connected to the CPU through data, address, and control buses and can be handled using all instructions. For complete module descriptions, see the MSP430x1xx Family User's Guide.

6.8.1 Digital I/O

Six 8-bit I/O ports are implemented: ports P1 to P6:

- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible.
- Edge-selectable interrupt input capability for all the eight bits of ports P1 and P2.
- Read and write access to port-control registers is supported by all instructions.

6.8.2 Oscillator and System Clock

The clock system is supported by the basic clock module that includes support for a 32768-Hz watch crystal oscillator, an internal digitally controlled oscillator (DCO), and a high-frequency crystal oscillator. The basic clock module is designed to meet the requirements of both low system cost and low power consumption. The internal DCO provides a fast turn-on clock source and stabilizes in less than 6 µs. The basic clock module provides the following clock signals:

- Auxiliary clock (ACLK), sourced from a 32768-Hz watch crystal or a high-frequency crystal
- Main clock (MCLK), the system clock used by the CPU
- Sub-Main clock (SMCLK), the subsystem clock used by the peripheral modules

6.8.3 Watchdog Timer (WDT)

The primary function of the WDT module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as an interval timer and can generate interrupts at selected time intervals.

6.8.4 Hardware Multiplier (MSP430F14x and MSP430F14x1 Only)

The multiplication operation is supported by a dedicated peripheral module. The module performs 16 × 16, 16 × 8, 8 × 16, and 8 × 8 bit operations. The module is capable of supporting signed and unsigned multiplication as well as signed and unsigned multiply and accumulate operations. The result of an operation can be accessed immediately after the operands have been loaded into the peripheral registers. No additional clock cycles are required.

6.8.5 USART0

The hardware universal synchronous/asynchronous receive transmit (USART0) peripheral module is used for serial data communication. The USART supports synchronous SPI (3 or 4 pin) and asynchronous UART communication protocols, using double-buffered transmit and receive channels.

6.8.6 USART1 (MSP430F14x and MSP430F14x1 Only)

The MSP430F14x(1) has a second hardware universal synchronous/asynchronous receive transmit (USART1) peripheral module that is used for serial data communication. The USART supports synchronous SPI (3 or 4 pin) and asynchronous UART communication protocols, using double-buffered transmit and receive channels. Operation of USART1 is identical to USART0.

6.8.7 Comparator_A

The primary function of the Comparator_A module is to support precision slope analog-to-digital conversions, battery-voltage supervision, and monitoring of external analog signals.

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6.8.8 ADC12 (MSP430F14x and MSP430F13x Only)

The ADC12 module supports fast 12-bit analog-to-digital conversions. The module implements a 12-bit SAR core, sample select control, reference generator, and a 16-word conversion-and-control buffer. The conversion-and-control buffer allows up to 16 independent ADC samples to be converted and stored without CPU intervention.

6.8.9 Timer_A3

Timer_A3 is a 16-bit timer/counter with three capture/compare registers. Timer_A3 can support multiple capture/compares, PWM outputs, and interval timing (see Table 6-12). Timer_A3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

Table 6-12. Timer_A3 Signal Connections

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER
12 - P1.0	TACLK	TACLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
21 - P2.1	TAINCLK	INCLK			
13 - P1.1	TA0	CCI0A	CCR0	TA0	13 - P1.1
22 - P2.2	TA0	CCI0B			17 - P1.5
	DV_{SS}	GND			27 - P2.7
	DV_{CC}	VCC			
14 - P1.2	TA1	CCI1A	CCR1	TA1	
	CAOUT (internal)	CCI1B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
15 - P1.3	TA2	CCI2A	CCR2	TA2	
	ACLK (internal)	CCI2B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			

6.8.10 Timer_B3 (MSP430F13x Only)

Timer_B3 is a 16-bit timer/counter with three capture/compare registers. Timer_B3 can support multiple capture/compares, PWM outputs, and interval timing (see Table 6-13). Timer_B3 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

6.8.11 Timer_B7 (MSP430F14x and MSP430F14x1 Only)

Timer_B7 is a 16-bit timer/counter with seven capture/compare registers. Timer_B7 can support multiple capture/compares, PWM outputs, and interval timing (see Table 6-13). Timer_B7 also has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers.

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Table 6-13. Timer_B3 and Timer_B7 Signal Connections(1)

INPUT PIN NUMBER	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	OUTPUT PIN NUMBER
43 - P4.7	TBCLK	TBCLK	Timer	NA	
	ACLK	ACLK			
	SMCLK	SMCLK			
43 - P4.7	TBCLK	INCLK			
36 - P4.0	TB0	CCI0A	CCR0	TB0	36 - P4.0
36 - P4.0	TB0	CCI0B			ADC12 (internal)
	DV_{SS}	GND			
	DV_{CC}	VCC			
37 - P4.1	TB1	CCI1A	CCR1	TB1	37 - P4.1
37 - P4.1	TB1	CCI1B			ADC12 (internal)
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
38 - P4.2	TB2	CCI2A	CCR2	TB2	38 - P4.2
38 - P4.2	TB2	CCI2B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
39 - P4.3	TB3	CCI3A	CCR3	TB3	39 - P4.3
39 - P4.3	TB3	CCI3B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
40 - P4.4	TB4	CCI4A	CCR4	TB4	40 - P4.4
40 - P4.4	TB4	CCI4B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
41 - P4.5	TB5	CCI5A	CCR5	TB5	41 - P4.5
41 - P4.5	TB5	CCI5B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			
42 - P4.6	TB6	CCI6A	CCR6	TB6	42 - P4.6
	ACLK (internal)	CCI6B			
	DV_{SS}	GND			
	DV_{CC}	V_{CC}			

(1) Timer_B3 implements three capture/compare blocks (CCR0, CCR1 and CCR2).

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6.8.12 Peripheral File Map

Table 6-14 lists the peripheral register that support word access. See Table 6-15 for the regsiters with byte access.

Table 6-14. Peripherals With Word Access

MODULE	REGISTER NAME	ACRONYM	ADDRESS
Watchdog	Watchdog timer control	WDTCTL	0120h
Timer_B7, Timer_B3	Timer_B interrupt vector	TBIV	011Eh
	Timer_B control	TBCTL	0180h
	Timer_B capture/compare control 0	TBCCTL0	0182h
	Timer_B capture/compare control 1	TBCCTL1	0184h
	Timer_B capture/compare control 2	TBCCTL2	0186h
	Timer_B capture/compare control 3 (1)	TBCCTL3	0188h
	Timer_B capture/compare control 4 (1)	TBCCTL4	018Ah
	Timer_B capture/compare control 5 (1)	TBCCTL5	018Ch
	Timer_B capture/compare control 6 (1)	TBCCTL6	018Eh
	Timer_B counter	TBR	0190h
	Timer_B capture/compare 0	TBCCR0	0192h
	Timer_B capture/compare 1	TBCCR1	0194h
	Timer_B capture/compare 2	TBCCR2	0196h
	Timer_B capture/compare 3 (1)	TBCCR3	0198h
	Timer_B capture/compare 4 (1)	TBCCR4	019Ah
	Timer_B capture/compare 5 (1)	TBCCR5	019Ch
	Timer_B capture/compare 6 (1)	TBCCR6	019Eh
Timer_A3	Timer_A interrupt vector	TAIV	012Eh
	Timer_A control	TACTL	0160h
	Timer_A capture/compare control 0	TACCTL0	0162h
	Timer_A capture/compare control 1	TACCTL1	0164h
	Timer_A capture/compare control 2	TACCTL2	0166h
	Reserved		0168h
	Reserved		016Ah
	Reserved		016Ch
	Reserved		016Eh
	Timer_A counter	TAR	0170h
	Timer_A capture/compare 0	TACCR0	0172h
	Timer_A capture/compare 1	TACCR1	0174h
	Timer_A capture/compare 2	TACCR2	0176h
	Reserved		0178h
	Reserved		017Ah
	Reserved		017Ch
	Reserved		017Eh

(1) Timer_B7 only, reserved for Timer_B3

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Table 6-14. Peripherals With Word Access (continued)

MODULE	REGISTER NAME	ACRONYM	ADDRESS
Hardware multiplier (MSP430F14x and MSP430F14x1 only)	Sum extend	SUMEXT	013Eh
	Result high word	RESHI	013Ch
	Result low word	RESLO	013Ah
	Operand 2	OP2	0138h
	Multiply signed and accumulate operand 1	MACS	0136h
	Multiply and accumulate operand 1	MAC	0134h
	Multiply signed operand 1	MPYS	0132h
	Multiply unsigned operand 1	MPY	0130h
Flash	Flash control 3	FCTL1	012Ch
	Flash control 2	FCTL2	012Ah
	Flash control 1	FCTL1	0128h

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Table 6-14. Peripherals With Word Access (continued)

MODULE	REGISTER NAME	ACRONYM	ADDRESS
ADC12 (not in MSP430F14x1)	Conversion memory 15	ADC12MEM15	015Eh
	Conversion memory 14	ADC12MEM14	015Ch
	Conversion memory 13	ADC12MEM13	015Ah
	Conversion memory 12	ADC12MEM12	0158h
	Conversion memory 11	ADC12MEM11	0156h
	Conversion memory 10	ADC12MEM10	0154h
	Conversion memory 9	ADC12MEM9	0152h
	Conversion memory 8	ADC12MEM8	0150h
	Conversion memory 7	ADC12MEM7	014Eh
	Conversion memory 6	ADC12MEM6	014Ch
	Conversion memory 5	ADC12MEM5	014Ah
	Conversion memory 4	ADC12MEM4	0148h
	Conversion memory 3	ADC12MEM3	0146h
	Conversion memory 2	ADC12MEM2	0144h
	Conversion memory 1	ADC12MEM1	0142h
	Conversion memory 0	ADC12MEM0	0140h
	Interrupt vector word	ADC12IV	01A8h
	Interrupt enable	ADC12IE	01A6h
	Interrupt flag	ADC12IFG	01A4h
	ADC control 1	ADC12CTL1	01A2h
	ADC control 0	ADC12CTL0	01A0h
	ADC memory control 15	ADC12MCTL15	08Fh
	ADC memory control 14	ADC12MCTL14	08Eh
	ADC memory control 13	ADC12MCTL13	08Dh
	ADC memory control 12	ADC12MCTL12	08Ch
	ADC memory control 11	ADC12MCTL11	08Bh
	ADC memory control 10	ADC12MCTL10	08Ah
	ADC memory control 9	ADC12MCTL9	089h
	ADC memory control 8	ADC12MCTL8	088h
	ADC memory control 7	ADC12MCTL7	087h
	ADC memory control 6	ADC12MCTL6	086h
	ADC memory control 5	ADC12MCTL5	085h
	ADC memory control 4	ADC12MCTL4	084h
	ADC memory control 3	ADC12MCTL3	083h
	ADC memory control 2	ADC12MCTL2	082h
	ADC memory control 1	ADC12MCTL1	081h
	ADC memory control 0	ADC12MCTL0	080h

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Table 6-15 lists the peripheral register that support byte access. See Table 6-14 for the regsiters with word access.

Table 6-15. Peripherals With Byte Access

MODULE	REGISTER NAME	ACRONYM	ADDRESS
USART1 (MSP430F14x and MSP430F14x1 only)	Transmit buffer	U1TXBUF	07Fh
	Receive buffer	U1RXBUF	07Eh
	Baud rate 1	U1BR1	07Dh
	Baud rate 0	U1BR0	07Ch
	Modulation control	U1MCTL	07Bh
	Receive control	U1RCTL	07Ah
	Transmit control	U1TCTL	079h
	USART control	U1CTL	078h
USART0	Transmit buffer	U0TXBUF	077h
	Receive buffer	U0RXBUF	076h
	Baud rate 1	U0BR1	075h
	Baud rate 0	U0BR0	074h
	Modulation control	U0MCTL	073h
	Receive control	U0RCTL	072h
	Transmit control	U0TCTL	071h
	USART control	U0CTL	070h
Comparator_A	Comparator_A port disable	CAPD	05Bh
	Comparator_A control 2	CACTL2	05Ah
	Comparator_A control 1	CACTL1	059h
Basic Clock	Basic clock system control 2	BCSCTL2	058h
	Basic clock system control 1	BCSCTL1	057h
	DCO clock frequency control	DCOCTL	056h
Port P6	Port P6 selection	P6SEL	037h
	Port P6 direction	P6DIR	036h
	Port P6 output	P6OUT	035h
	Port P6 input	P6IN	034h
Port P5	Port P5 selection	P5SEL	033h
	Port P5 direction	P5DIR	032h
	Port P5 output	P5OUT	031h
	Port P5 input	P5IN	030h
Port P4	Port P4 selection	P4SEL	01Fh
	Port P4 direction	P4DIR	01Eh
	Port P4 output	P4OUT	01Dh
	Port P4 input	P4IN	01Ch
Port P3	Port P3 selection	P3SEL	01Bh
	Port P3 direction	P3DIR	01Ah
	Port P3 output	P3OUT	019h
	Port P3 input	P3IN	018h

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Table 6-15. Peripherals With Byte Access (continued)

MODULE	REGISTER NAME	ACRONYM	ADDRESS
Port P2	Port P2 selection	P2SEL	02Eh
	Port P2 interrupt enable	P2IE	02Dh
	Port P2 interrupt edge select	P2IES	02Ch
	Port P2 interrupt flag	P2IFG	02Bh
	Port P2 direction	P2DIR	02Ah
	Port P2 output	P2OUT	029h
	Port P2 input	P2IN	028h
Port P1	Port P1 selection	P1SEL	026h
	Port P1 interrupt enable	P1IE	025h
	Port P1 interrupt edge select	P1IES	024h
	Port P1 interrupt flag	P1IFG	023h
	Port P1 direction	P1DIR	022h
	Port P1 output	P1OUT	021h
	Port P1 input	P1IN	020h
Special Functions	SFR module enable 2	ME2	005h
	SFR module enable 1	ME1	004h
	SFR interrupt flag 2	IFG2	003h
	SFR interrupt flag 1	IFG1	002h
	SFR interrupt enable 2	IE2	001h
	SFR interrupt enable 1	IE1	000h

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6.9 Input/Output Diagrams

6.9.1 Port P1, Input/Output With Schmitt Trigger

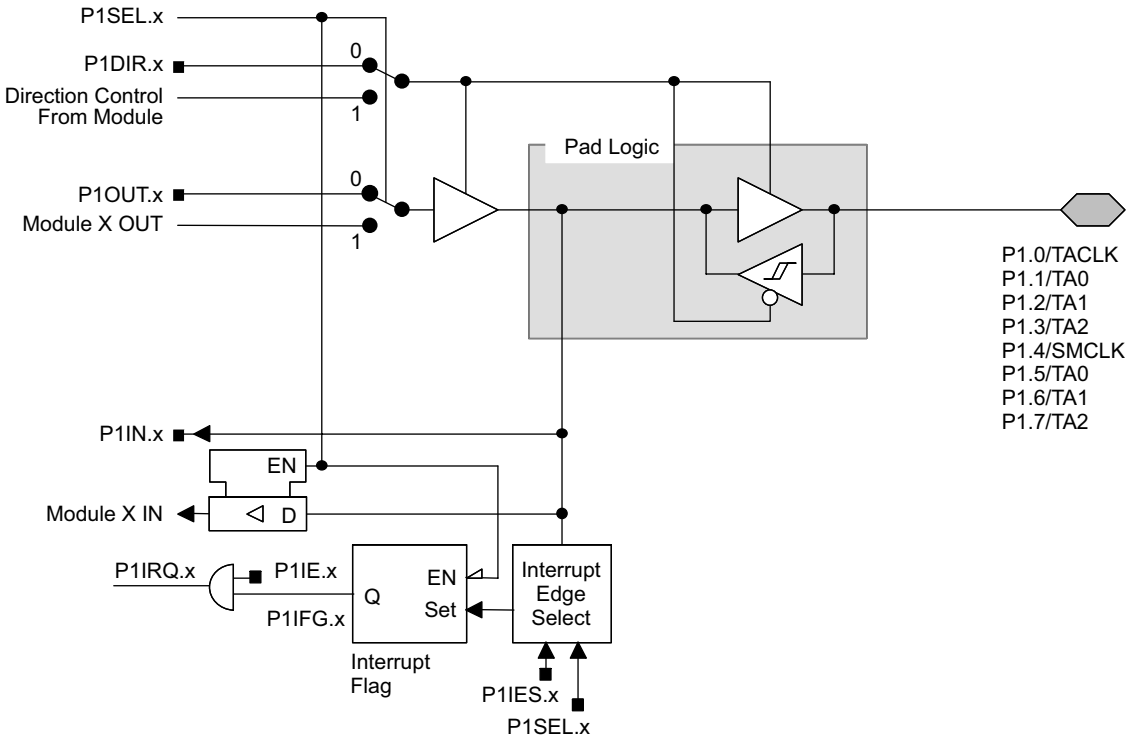


Figure 6-10. Port P1 (P1.0 to P1.7) Diagram

Table 6-16. Port P1 (P1.0 to P1.7) Pin Functions

PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P1Sel.0	P1DIR.0	P1DIR.0	P1OUT.0	DV_{SS}	P1IN.0	TACLK(1)	P1IE.0	P1IFG.0	P1IES.0
P1Sel.1	P1DIR.1	P1DIR.1	P1OUT.1	Out0 signal(1)	P1IN.1	CCI0A(1)	P1IE.1	P1IFG.1	P1IES.1
P1Sel.2	P1DIR.2	P1DIR.2	P1OUT.2	Out1 signal(1)	P1IN.2	CCI1A(1)	P1IE.2	P1IFG.2	P1IES.2
P1Sel.3	P1DIR.3	P1DIR.3	P1OUT.3	Out2 signal(1)	P1IN.3	CCI2A(1)	P1IE.3	P1IFG.3	P1IES.3
P1Sel.4	P1DIR.4	P1DIR.4	P1OUT.4	SMCLK	P1IN.4	unused	P1IE.4	P1IFG.4	P1IES.4
P1Sel.5	P1DIR.5	P1DIR.5	P1OUT.5	Out0 signal(1)	P1IN.5	unused	P1IE.5	P1IFG.5	P1IES.5
P1Sel.6	P1DIR.6	P1DIR.6	P1OUT.6	Out1 signal(1)	P1IN.6	unused	P1IE.6	P1IFG.6	P1IES.6
P1Sel.7	P1DIR.7	P1DIR.7	P1OUT.7	Out2 signal(1)	P1IN.7	unused	P1IE.7	P1IFG.7	P1IES.7

(1) Signal from or to Timer_A

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6.9.2 Port P2, Input/Output With Schmitt Trigger

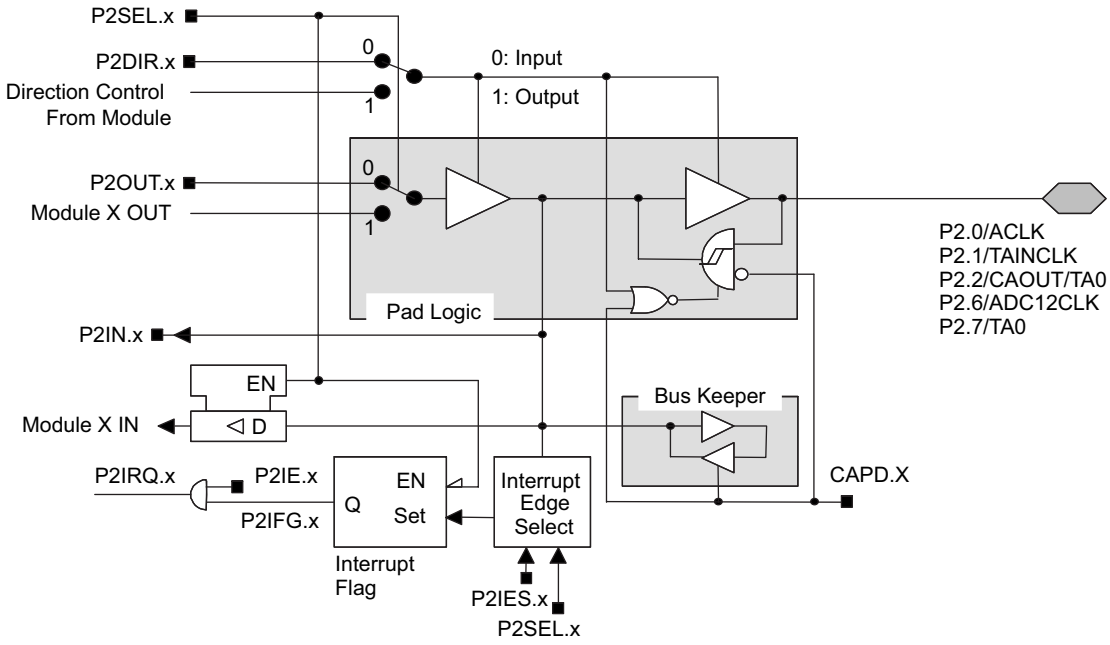


Figure 6-11. Port P2 (P2.0 to P2.2, P2.6, and P2.7) Diagram

Table 6-17. Port P2 (P2.0 to P2.2, P2.6, and P2.7) Pin Functions

PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.0	P2DIR.0	P2DIR.0	P2OUT.0	ACLK	P2IN.0	unused	P2IE.0	P2IFG.0	P2IES.0
P2Sel.1	P2DIR.1	P2DIR.1	P2OUT.1	DV_{SS}	P2IN.1	INCLK(1)	P2IE.1	P2IFG.1	P2IES.1
P2Sel.2	P2DIR.2	P2DIR.2	P2OUT.2	CAOUT(2)	P2IN.2	CCI0B(1)	P2IE.2	P2IFG.2	P2IES.2
P2Sel.6	P2DIR.6	P2DIR.6	P2OUT.6	ADC12CLK(3)	P2IN.6	unused	P2IE.6	P2IFG.6	P2IES.6
P2Sel.7	P2DIR.7	P2DIR.7	P2OUT.7	Out0 signal(4)	P2IN.7	unused	P2IE.7	P2IFG.7	P2IES.7

(1) Signal to Timer_A
(2) Signal from Comparator_A
(3) ADC12CLK signal is output of the 12-bit ADC module
(4) Signal from Timer_A

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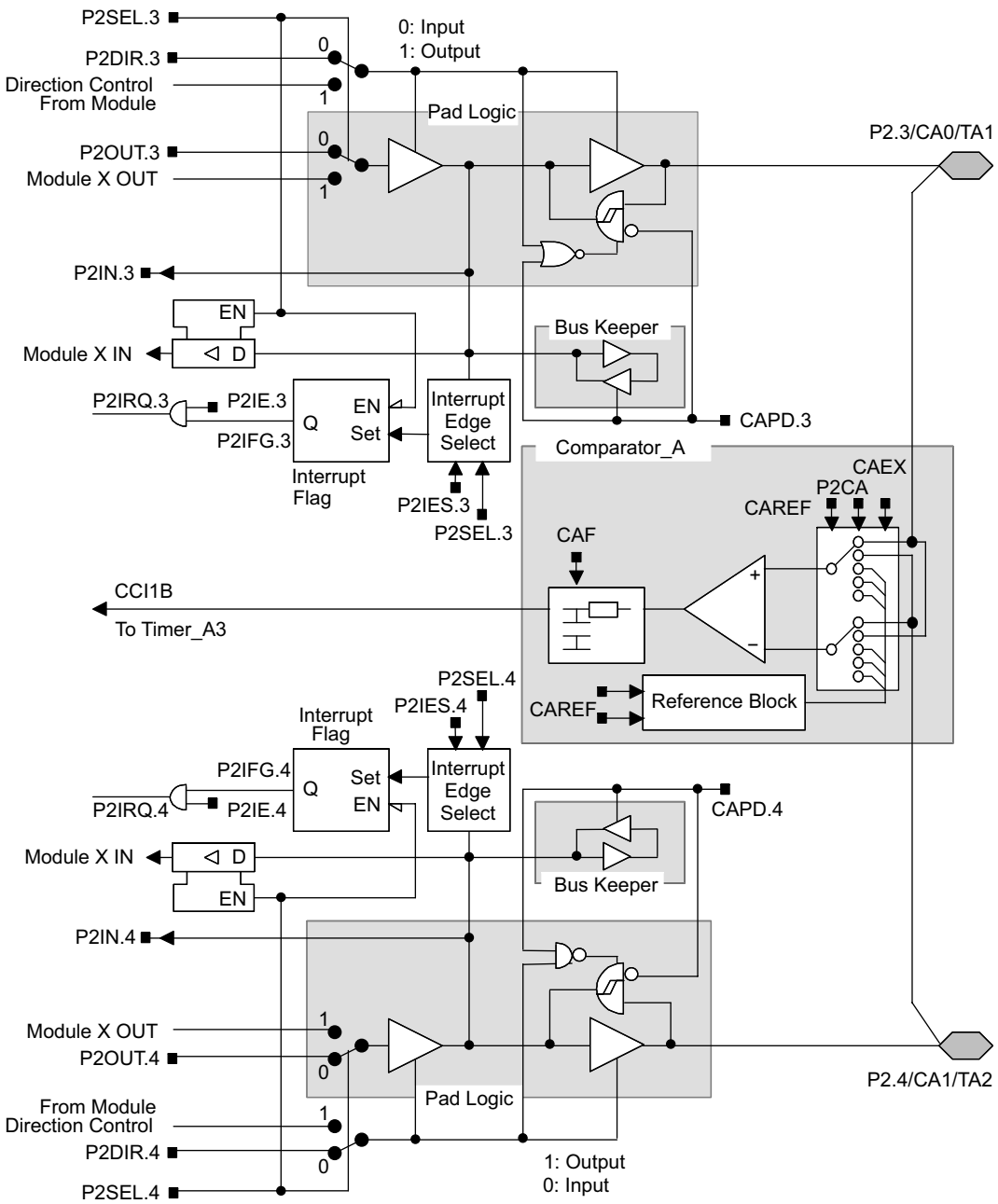


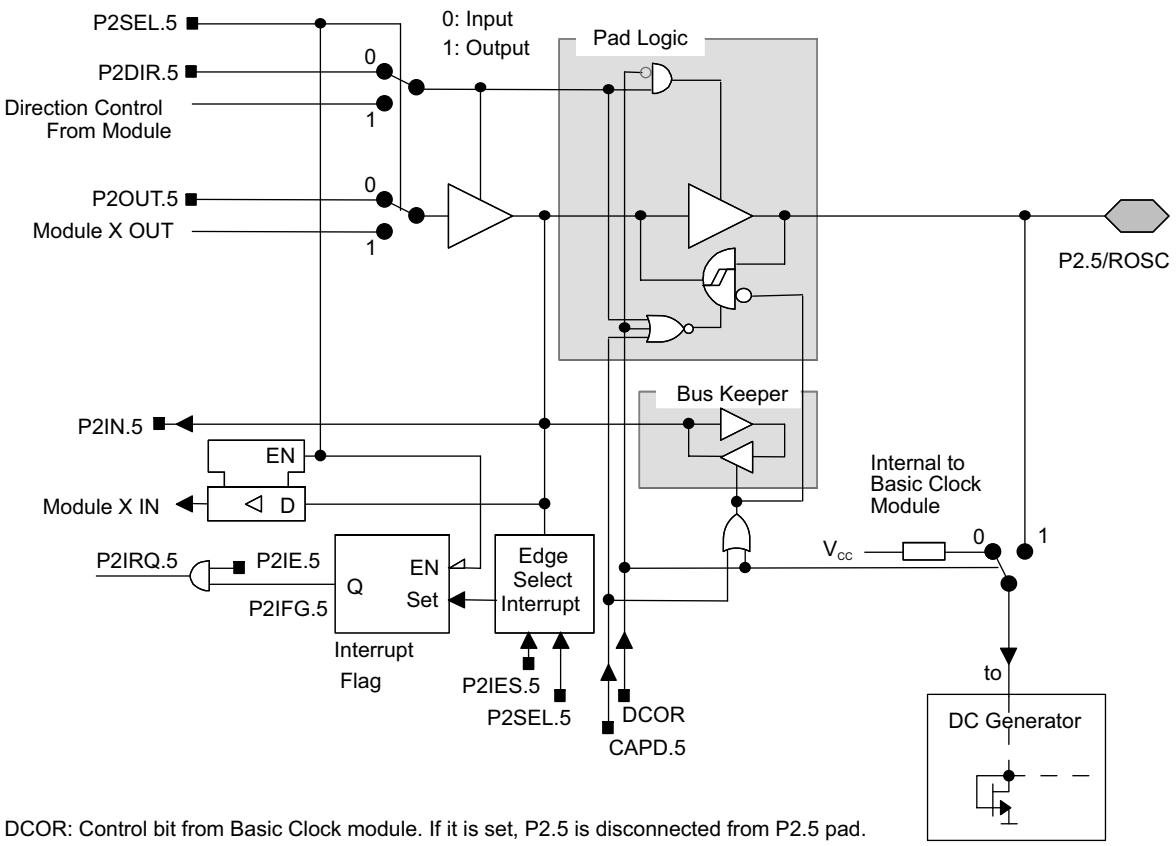
Figure 6-12. Port P2 (P2.3 and P2.4) Diagram

Table 6-18. Port P2 (P2.3 and P2.4) Pin Functions

PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.3	P2DIR.3	P2DIR.3	P2OUT.3	Out1 signal(1)	P2IN.3	unused	P2IE.3	P2IFG.3	P2IES.3
P2Sel.4	P2DIR.4	P2DIR.4	P2OUT.4	Out2 signal(1)	P2IN.4	unused	P2IE.4	P2IFG.4	P2IES.4

(1) Signal from Timer_A

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DCOR: Control bit from Basic Clock module. If it is set, P2.5 is disconnected from P2.5 pad.

Figure 6-13. Port P2 (P2.5) Diagram

Table 6-19. Port P2 (P2.5) Pin Functions

PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN	PnIE.x	PnIFG.x	PnIES.x
P2Sel.5	P2DIR.5	P2DIR.5	P2OUT.5	DV_{SS}	P2IN.5	unused	P2IE.5	P2IFG.5	P2IES.5

6.9.3 Port P3, Input/Output With Schmitt Trigger

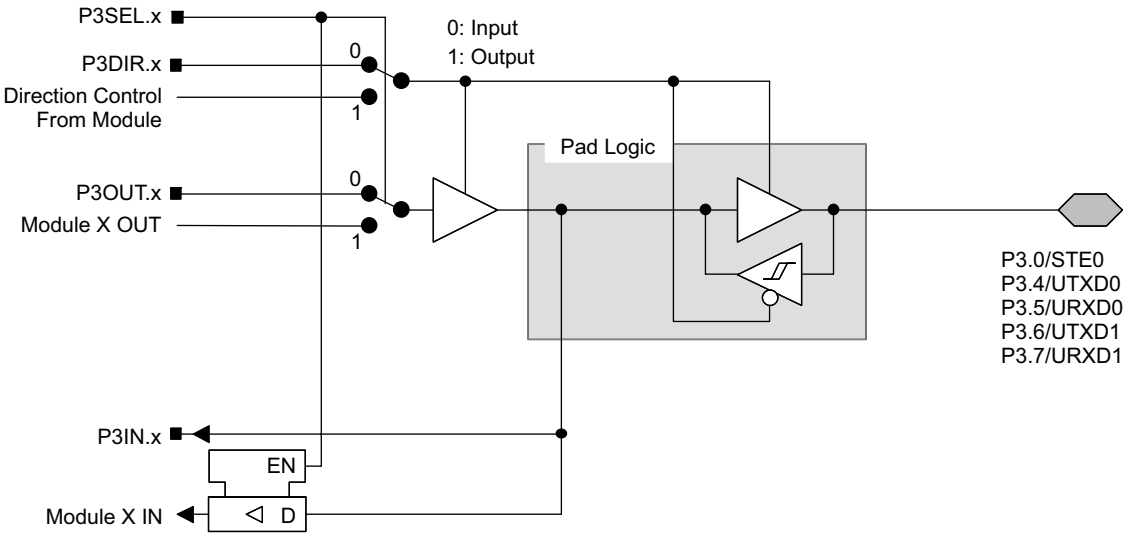


Figure 6-14. Port P3 (P3.0 and 3.4 to 3.7) Diagram

Table 6-20. Port P3 (P3.0 and 3.4 to 3.7) Pin Functions

PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P3Sel.0	P3DIR.0	DV_{SS}	P3OUT.0	DV_{SS}	P3IN.0	STE0
P3Sel.4	P3DIR.4	DV_{CC}	P3OUT.4	UTXD0(1)	P3IN.4	Unused
P3Sel.5	P3DIR.5	DV_{SS}	P3OUT.5	DV_{SS}	P3IN.5	URXD0(2)
P3Sel.6	P3DIR.6	DV_{CC}	P3OUT.6	UTXD1(3)	P3IN.6	unused
P3Sel.7	P3DIR.7	DV_{SS}	P3OUT.7	DV_{SS}	P3IN.7	URXD1(4)

(1) Output from USART0 module
(2) Input to USART0 module
(3) Output from USART1 module in MSP430F14x and MSP430F14x1 devices, DV_{SS} in MSP430F13x devices
(4) Input to USART1 module in MSP430F14x and MSP430F14x1 devices, unused in MSP430F13x devices

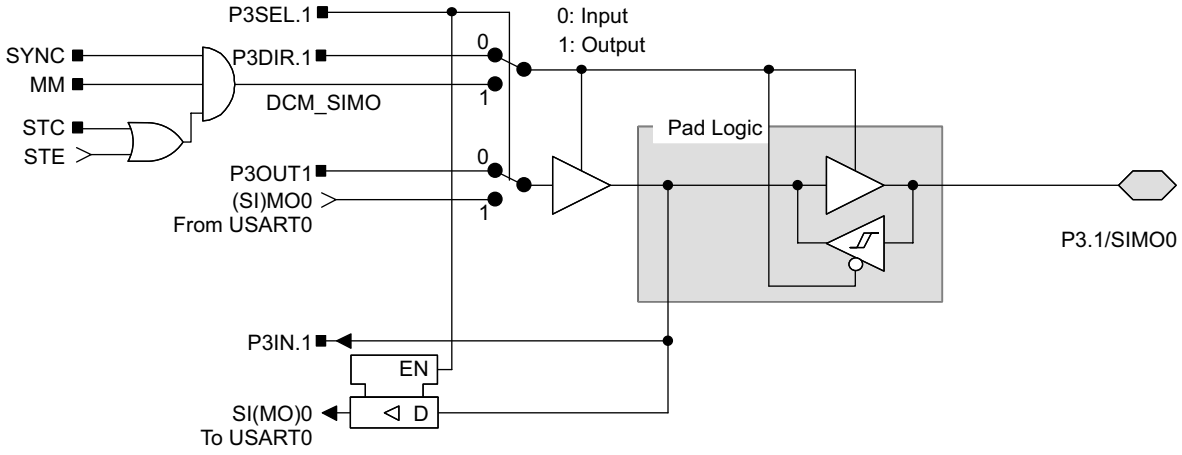


Figure 6-15. Port P3 (P3.1) Diagram

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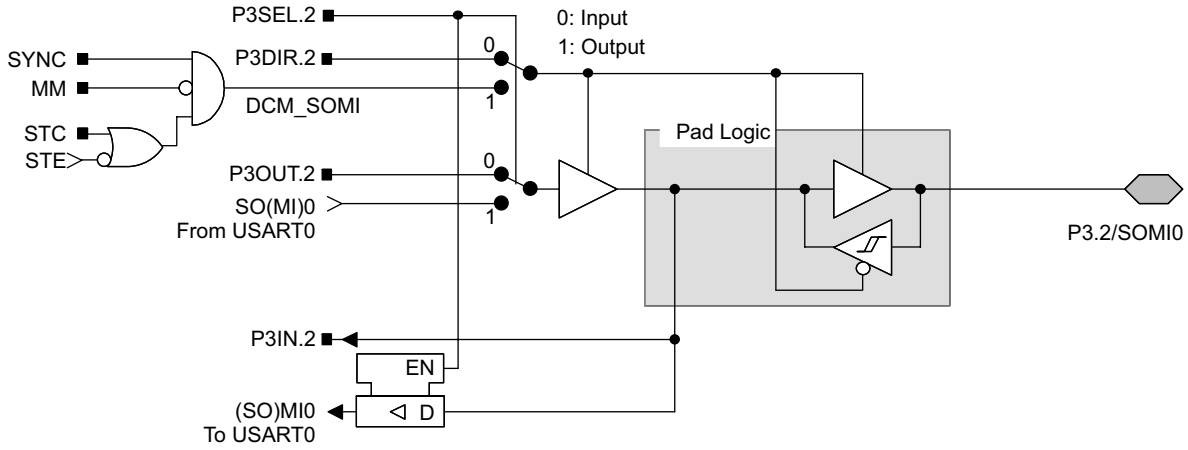
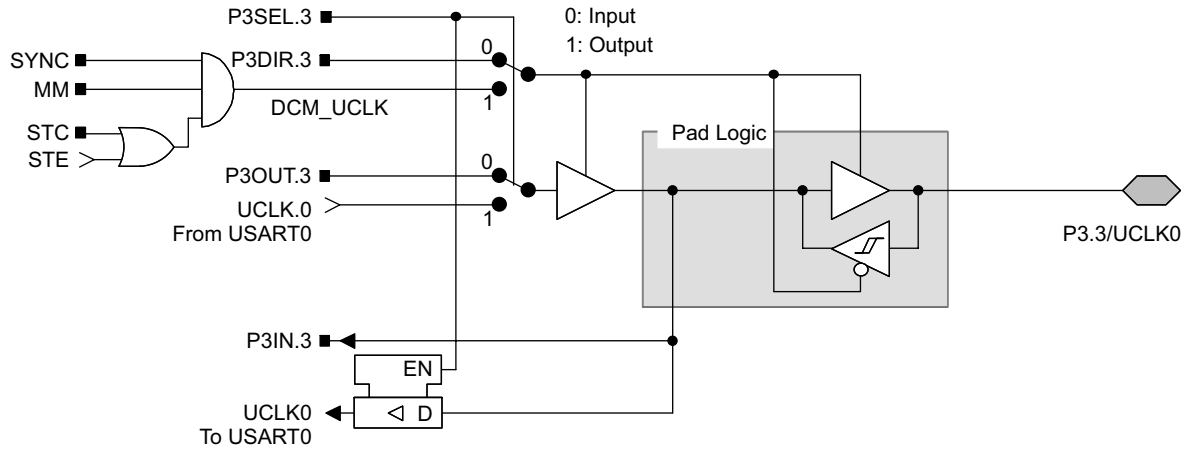


Figure 6-16. Port P3 (P3.2) Diagram



NOTE: UART mode: The UART clock can only be an input. If UART mode and UART function are selected, P3.3/UCLK0 is always an input.
SPI slave mode: The clock applied to UCLK0 is used to shift data in and out.
SPI master mode: The clock to shift data in and out is supplied to connected devices on pin P3.3/UCLK0 (in slave mode).

Figure 6-17. Port P3 (P3.3) Diagram

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6.9.4 Port P4, Input/Output With Schmitt Trigger

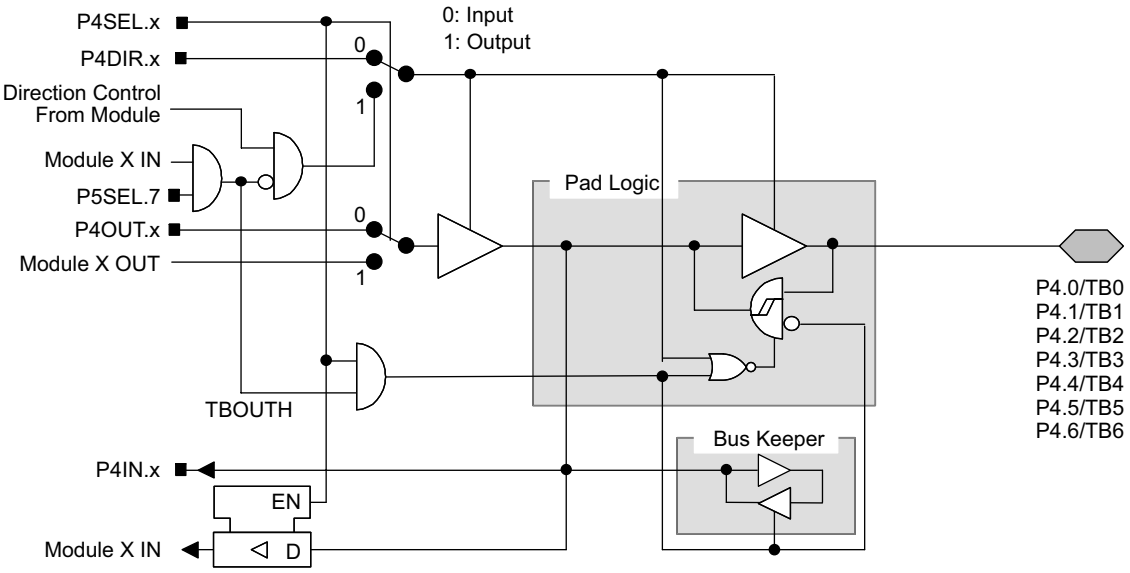


Figure 6-18. Port P4 (P4.0 to P4.6) Diagram

Table 6-21. Port P4 (P4.0 to P4.6) Pin Functions

PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P4Sel.0	P4DIR.0	P4DIR.0	P4OUT.0	Out0 signal(1)	P4IN.0	CCI0A / CCI0B(2)
P4Sel.1	P4DIR.1	P4DIR.1	P4OUT.1	Out1 signal(1)	P4IN.1	CCI1A / CCI1B(2)
P4Sel.2	P4DIR.2	P4DIR.2	P4OUT.2	Out2 signal(1)	P4IN.2	CCI2A / CCI2B(2)
P4Sel.3	P4DIR.3	P4DIR.3	P4OUT.3	Out3 signal(1)	P4IN.3	CCI3A / CCI3B(2)
P4Sel.4	P4DIR.4	P4DIR.4	P4OUT.4	Out4 signal(1)	P4IN.4	CCI4A / CCI4B(2)
P4Sel.5	P4DIR.5	P4DIR.5	P4OUT.5	Out5 signal(1)	P4IN.5	CCI5A / CCI5B(2)
P4Sel.6	P4DIR.6	P4DIR.6	P4OUT.6	Out6 signal(1)	P4IN.6	CCI6A(2)

(1) Signal from Timer_B
(2) Signal to Timer_B

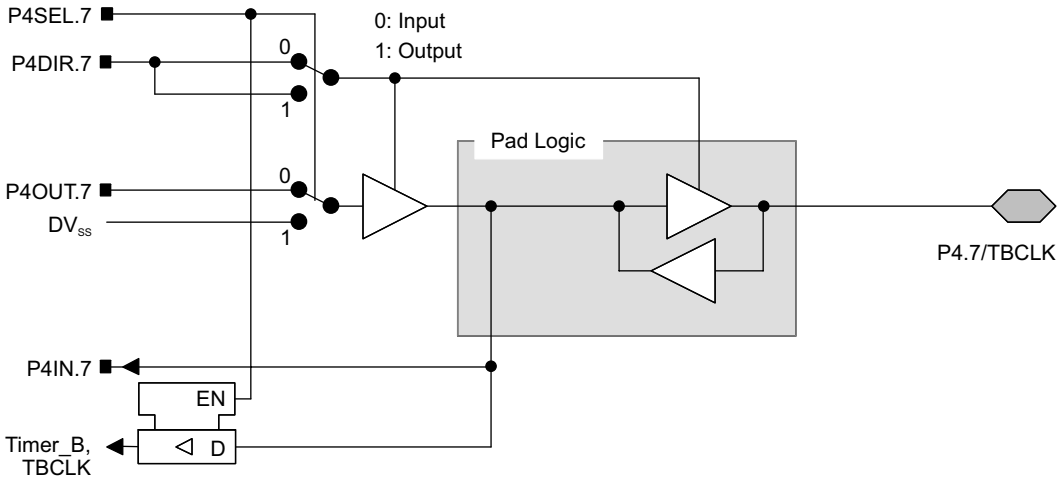


Figure 6-19. Port P4 (P4.7) Diagram

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6.9.5 Port P5, Input/Output With Schmitt Trigger

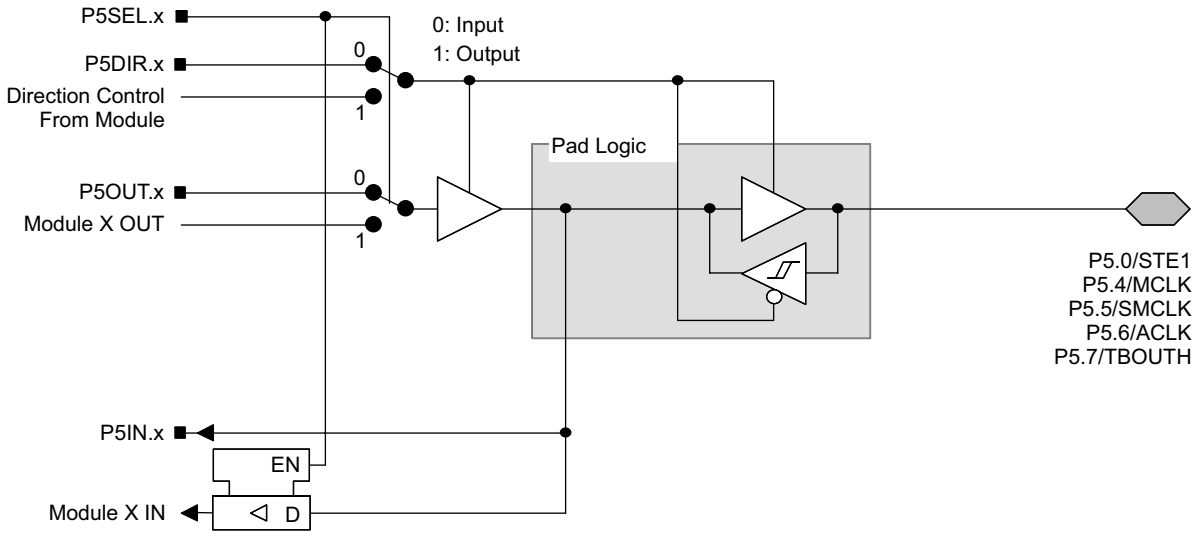


Figure 6-20. Port P5 (P5.0 and P5.4 to P5.7) Diagram

Table 6-22. Port P5 (P5.0 and P5.4 to P5.7) Pin Functions

PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P5Sel.0	P5DIR.0	DV_{SS}	P5OUT.0	DV_{SS}	P5IN.0	STE.1
P5Sel.4	P5DIR.4	DV_{CC}	P5OUT.4	MCLK	P5IN.4	unused
P5Sel.5	P5DIR.5	DV_{CC}	P5OUT.5	SMCLK	P5IN.5	unused
P5Sel.6	P5DIR.6	DV_{CC}	P5OUT.6	ACLK	P5IN.6	unused
P5Sel.7	P5DIR.7	DV_{SS}	P5OUT.7	DV_{SS}	P5IN.7	TBOUTH(1)

(1) The TBOUTH signal is used by port module P4, pins P4.0 to P4.6. The function of TBOUTH is most useful when used with Timer_B7.

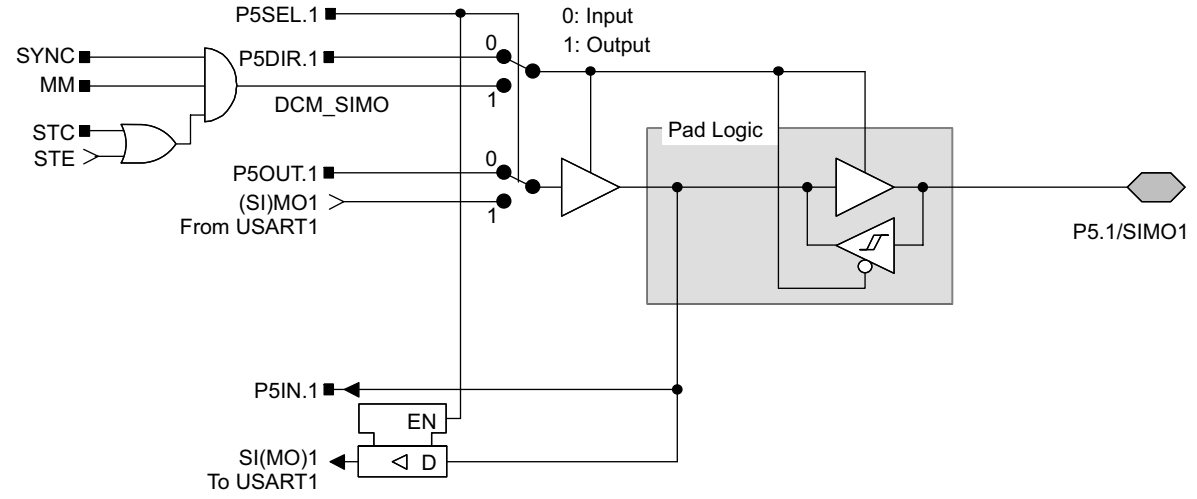


Figure 6-21. Port P5 (P5.1) Diagram

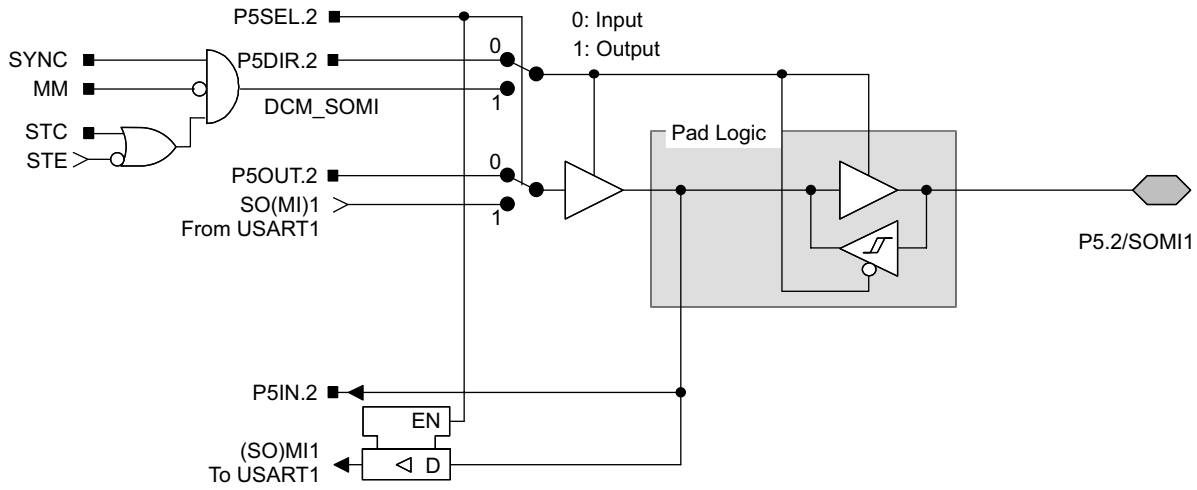
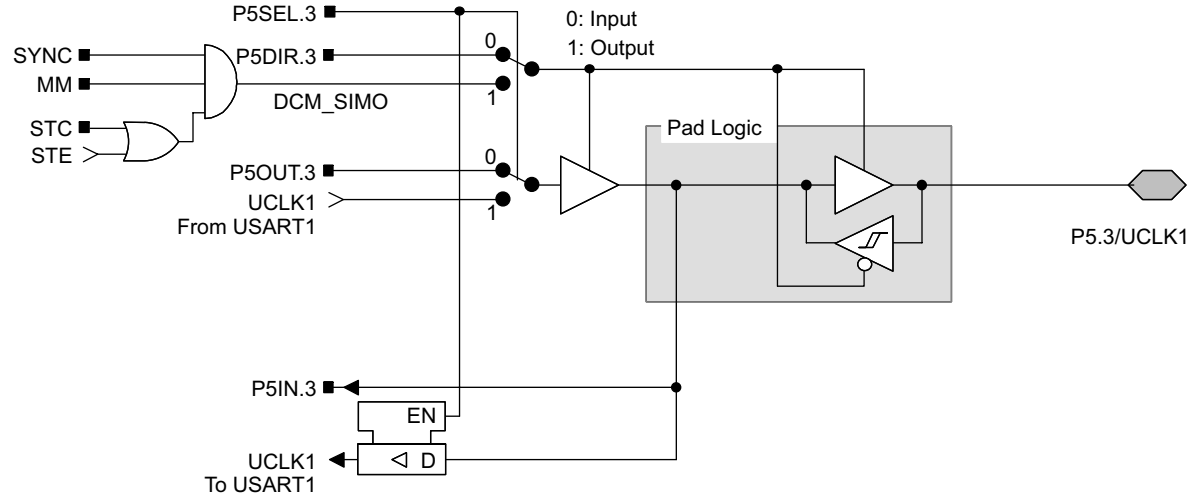


Figure 6-22. Port P5 (P5.2) Diagram

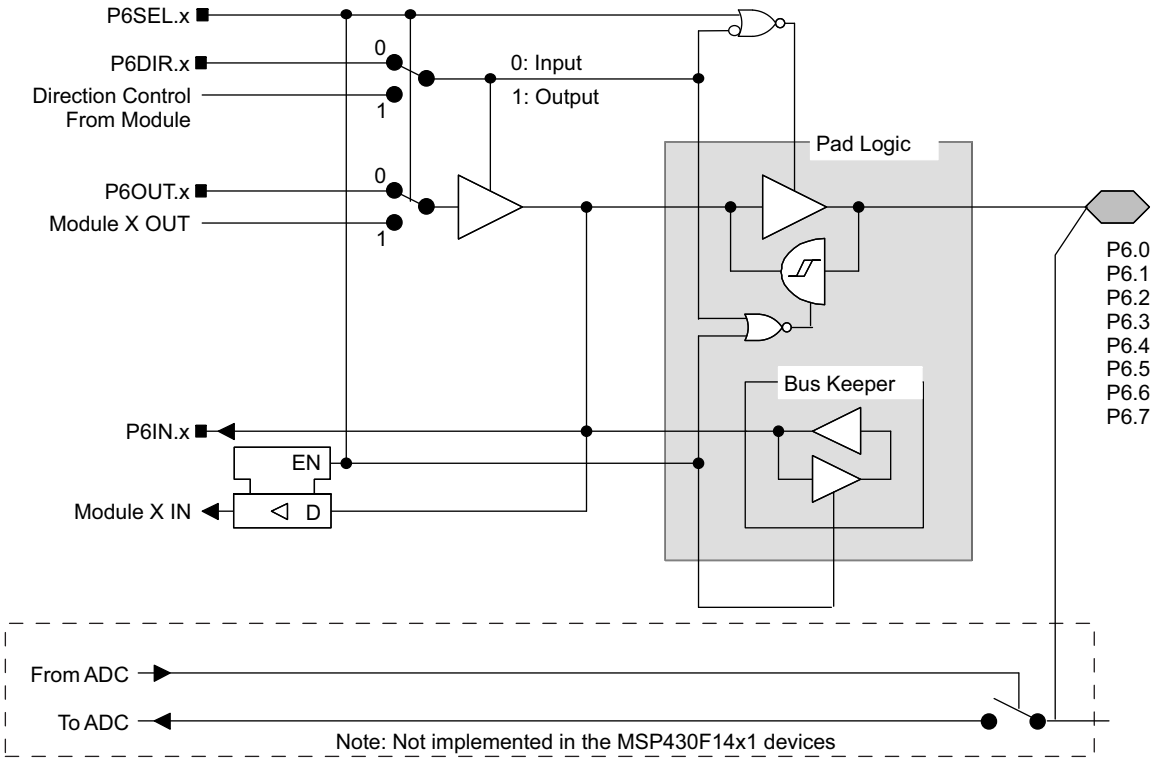


NOTE: UART mode: The UART clock can only be an input. If UART mode and UART function are selected, P5.3/UCLK1 is always an input.
SPI slave mode: The clock applied to UCLK1 is used to shift data in and out.
SPI master mode: The clock to shift data in and out is supplied to connected devices on pin P5.3/UCLK1 (in slave mode).

Figure 6-23. Port P5 (P5.3) Diagram

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6.9.6 Port P6, Input/Output With Schmitt Trigger



NOTE: Analog signals applied to digital gates can cause current flow from the positive to the negative terminal. The throughput current flows if the analog signal is in the range of transitions 0→1 or 1→0. The value of the throughput current depends on the driving capability of the gate. For MSP430 MCUs, the current is approximately 100 µA. Use P6SEL.x = 1 to prevent throughput current. P6SEL.x should be set, even if the signal at the pin is not being used by the ADC12.

Figure 6-24. Port P6 (P6.0 to P6.7) Diagram

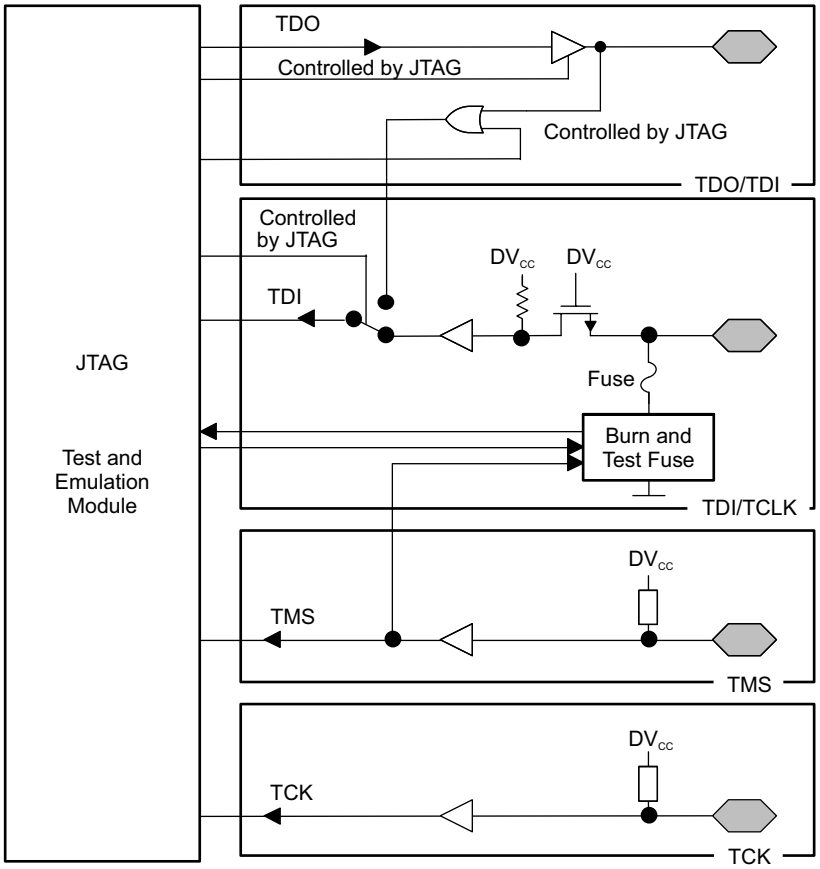
Table 6-23. Port P6 (P6.0 to P6.7) Pin Functions(1)

PnSel.x	PnDIR.x	DIRECTION CONTROL FROM MODULE	PnOUT.x	MODULE X OUT	PnIN.x	MODULE X IN
P6Sel.0	P6DIR.0	P6DIR.0	P6OUT.0	DV_{SS}	P6IN.0	unused
P6Sel.1	P6DIR.1	P6DIR.1	P6OUT.1	DV_{SS}	P6IN.1	unused
P6Sel.2	P6DIR.2	P6DIR.2	P6OUT.2	DV_{SS}	P6IN.2	unused
P6Sel.3	P6DIR.3	P6DIR.3	P6OUT.3	DV_{SS}	P6IN.3	unused
P6Sel.4	P6DIR.4	P6DIR.4	P6OUT.4	DV_{SS}	P6IN.4	unused
P6Sel.5	P6DIR.5	P6DIR.5	P6OUT.5	DV_{SS}	P6IN.5	unused
P6Sel.6	P6DIR.6	P6DIR.6	P6OUT.6	DV_{SS}	P6IN.6	unused
P6Sel.7	P6DIR.7	P6DIR.7	P6OUT.7	DV_{SS}	P6IN.7	unused

(1) The signal at pins P6.x/Ax is used by the 12-bit ADC module.

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6.9.7 Port JTAG (TMS, TCK, TDI/TCLK, TDO/TDI), Input/Output With Schmitt Trigger



During programming activity and during blowing of the fuse, the TDO/TDI pin is used to apply the test input data for JTAG circuitry.

Figure 6-25. JTAG (TMS, TCK, TDI/TCLK, TDO/TDI) Diagram

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7 デバイスおよびドキュメントのサポート

7.1 使い始めと次の手順

MSP430ファミリのデバイス、および開発に役立つツールやライブラリの詳細については、「Getting Started」ページを参照してください。

7.2 デバイスの項目表記

製品開発サイクルの段階を示すために、TIではMSP　MCUデバイスのすべての型番に接頭辞が割り当てられています。MSP MCU商用ファミリの各番号には、MSP、XMSのいずれかの接頭辞があります。これらの接頭辞は、製品開発の進展段階を表します。段階には、エンジニアリング・プロトタイプ(XMS)から、完全認定済みの量産デバイス(MSP)までがあります。

XMS - 実験段階のデバイスで、最終的なデバイスの電気的仕様を表しているとは限りません。

MSP - 完全に認定済みの量産版デバイスです。

XMSデバイスは、次の免責事項付きで出荷されます。

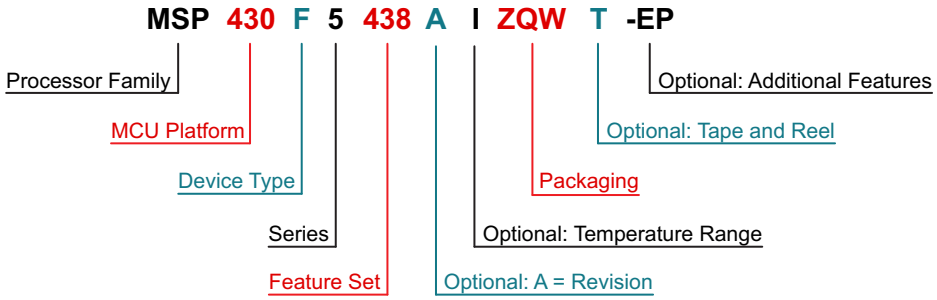
「開発中の製品は、社内での評価用です。」

MSPデバイスの特性は完全に明確化されており、デバイスの品質と信頼性が十分に示されています。TIの標準保証が適用されます。

プロトタイプ・デバイス(XMS)は標準の量産デバイスよりも故障率が高いことが予想されます。これらのデバイスは、予測される最終使用時の故障率が未定義であるため、TIはそれらのデバイスを量産システムで使用しないよう推奨しています。認定された量産デバイスのみを使用する必要があります。

TIデバイスの項目表記には、デバイス・ファミリ名の接尾辞も含まれます。この接尾辞は、温度範囲、パッケージ・タイプ、配布形式を示しています。デバイス名の各部の読み方を図 7-1に示します。

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Processor Family	CC = Embedded RF Radio MSP = Mixed-Signal Processor XMS = Experimental Silicon PMS = Prototype Device	
MCU Platform	430 = MSP430 low-power microcontroller platform	
Device Type	**Memory Type** C = ROM F = Flash FR = FRAM G = Flash or FRAM (Value Line) L = No Nonvolatile Memory	**Specialized Application** AFE = Analog Front End BQ = Contactless Power CG = ROM Medical FE = Flash Energy Meter FG = Flash Medical FW = Flash Electronic Flow Meter
Series	1 = Up to 8 MHz 2 = Up to 16 MHz 3 = Legacy 4 = Up to 16 MHz with LCD	5 = Up to 25 MHz 6 = Up to 25 MHz with LCD 0 = Low-Voltage Series
Feature Set	Various levels of integration within a series	
Optional: A = Revision	N/A	
Optional: Temperature Range	S = 0°C to 50°C C = 0°C to 70°C I = –40°C to 85°C T = –40°C to 105°C	
Packaging	http://www.ti.com/packaging	
Optional: Tape and Reel	T = Small reel R = Large reel No markings = Tube or tray	
Optional: Additional Features	-EP = Enhanced Product (–40°C to 105°C) -HT = Extreme Temperature Parts (–55°C to 150°C) -Q1 = Automotive Q100 Qualified	

NOTE: この図は、利用可能な機能とオプションの完全なリストではなく、与えられたデバイスまたはファミリについて、これらの機能とオプションのすべてが利用できることを示すものでもありません。

図 7-1. デバイスの項目表記 - 型番の読み方

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7.3 ツールとソフトウェア

MSP430F14x、MSP430F14x1、MSP430F13xマイクロコントローラでサポートされるデバッグ機能を、表 7-1に示します。利用可能な機能の詳細については、『MSP430用Code Composer Studio ユーザー・ガイド』を参照してください。

表 7-1. ハードウェアの特長

MSP430のアーキテクチャ	4線式JTAG	2線式JTAG	ブレーク・ポイント	範囲ブレーク・ポイント	クロック制御	状態シーケンサ	トレース・バッファ	LPMx.5デバッグ・サポート
MSP430	○	×	3	○	×	×	×	×

設計キットと評価モジュール

64ピンのターゲット開発ボードとMSP-FETプログラマのバンドル: MSP430F1x、MSP430F2x、MSP430F4x MCU
MSP-FET430U64 は、強力なフラッシュ・エミュレーション・ツールで、MSP430 MCU 向けのアプリケーション開発をすぐに開始するために必要なハードウェアとソフトウェアが含まれています。この中には、ZIFソケット・ターゲット・ボード(MSP-TS430PM64)とUSBデバッグ・インターフェイス(MSP-FET)が含まれており、JTAGインターフェイスを使用してインシステムでMSP430のプログラムとデバッグを行うために使用できます。フラッシュ・メモリは、数回のキー操作により、数秒で消去およびプログラムできます。また、MSP430のフラッシュは消費電力が非常に低いため、外部電源は不要です。

MSP-TS430PM64 - MSP430F1x、MSP430F2x、MSP430F4x MCUの64ピン・ターゲット開発ボード MSP-TS430PM64はスタンドアロンのZIFソケット・ターゲット・ボードで、JTAGインターフェイスを使用してインシステムでMSP430 MCUのプログラムとデバッグを行うために使用されます。

ソフトウェア

MSP430Ware™ソフトウェア MSP430Wareソフトウェアは、すべてのMSP430デバイス向けのサンプル・コード、データシート、その他の設計リソースを、1つの便利なパッケージとしてまとめたものです。既存のMSP430 MCU 設計リソースの完全なコレクションに加えて、MSP430Ware ソフトウェアには、MSPドライバ・ライブラリという高レベルのAPIも含まれています。このライブラリにより、MSP430ハードウェアを簡単にプログラムできます。MSP430Wareソフトウェアは CCSのコンポーネントとして、またはスタンドアロンのパッケージとして入手できます。

MSP430F13x、MSP430F14x、MSP430F15x、MSP430F16xのコード・サンプル すべてのMSPデバイス用に、内蔵の各ペリフェラルをさまざまなアプリケーションの要求に応じて構成するためのCコード・サンプルが用意されています。

MSP低消費電力マイコン用ブートローダ(BSL) ブートローダ(BSL)は、MSP低消費電力マイコンに組み込まれているアプリケーションです。ユーザーはBSLを使用してデバイスと通信を行い、メモリとの間で読み書きを行えます。この機能は主にデバイスのプログラム、プロトタイプ作成時、最終製品の生産、サービス時に使用されます。必要に応じて、プログラム可能メモリ(フラッシュ・メモリ)とデータ・メモリ(RAM)の両方を変更できます。

MSP用の固定小数点算術ライブラリ MSP IQmathおよびQmathライブラリは、Cプログラマ向けの高度に最適化された高精度の算術関数のコレクションで、浮動小数点アルゴリズムをMSP430およびMSP432デバイスの固定小数点コードへシームレスに移行できます。これらのルーチンは通常、最適な実行速度、高精度、超低消費電力が重視される、演算集中型のリアルタイム・アプリケーションで使用されます。IQmathライブラリとQmathライブラリを使用すると、浮動小数点演算を使用して記述した同等のコードに比べて、実行速度を大幅に高速化するとともに、消費電力の大幅な削減が可能です。

開発ツール

Code Composer Studio™: MSPマイクロコントローラ用の統合開発環境 Code Composer Studio (CCS)は、すべてのMSPマイクロコントローラ・デバイスをサポートする統合開発環境(IDE)です。CCSは、組み込みアプリケーションの開発とデバッグに使用される、組み込み用ソフトウェア・ユーティリティのスイートです。CCSには、最適化C/C++コンパイラ、ソース・コード・エディタ、プロジェクト・ビルド環境、デバッガ、プロファイラなど、多数の機能が含まれています。

コマンドライン・プログラマ MSP Flasher は、FETプログラマまたは eZ430 を経由し、JTAG または Spy-Bi-Wire (SBW) 通信を使用して MSP マイクロコントローラをプログラムするための、オープン・ソースでシェル・ベースのインターフェイスです。MSP Flasher は、IDE を使用せずにバイナリ・ファイル (.txt または .hex) を MSP マイクロコントローラへ直接ダウンロードできます。

MSP MCUプログラマおよびデバッガ MSP-FETは強力なエミュレーション開発ツールで、多くの場合にデバッグ・プローブと呼ばれます。ユーザーはこのツールを使用して、MSP低消費電力MCUのアプリケーショ

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ン開発をすぐに始めることができます。MCUのソフトウェアを作成する場合は通常、結果として得られたバイナリ・プログラムをMSPデバイスにダウンロードし、検証とデバッグを行う必要があります。

MSP-GANG量産プログラマ MSP Gang プログラマは MSP430 または MSP432 用のデバイス・プログラマで、8つまでの同一の MSP430 または MSP432 のフラッシュまたは FRAM デバイスを同時にプログラムできます。MSP Gang プログラマは、標準の RS-232 または USB 接続を使用してホスト PC と接続し、柔軟なプログラミング・オプションが用意されているため、ユーザーはプロセスを完全にカスタマイズ可能です。

7.4 ドキュメントのサポート

以下のドキュメントには、MSP430F14x、MSP430F14x1、MSP430F13x MCUについて記載されています。これらのドキュメントのコピーは、www.ti.comで入手できます。

ドキュメントの更新通知を受け取る方法

ドキュメント更新の通知を、シリコンの正誤表も含めて受け取るには、ti.comでご利用の製品のフォルダへ移動します(製品フォルダへのリンクについては、7.5を参照してください)。右上の隅にある「通知を受け取る」ボタンをクリックします。これによって登録が行われ、変更された製品情報の概要を毎週受け取ることができます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

正誤表

『MSP430F149デバイス正誤表』 には、機能仕様に対する既知の例外が記載されています。

『MSP430F1491デバイス正誤表』 には、機能仕様に対する既知の例外が記載されています。

『MSP430F148デバイス正誤表』 には、機能仕様に対する既知の例外が記載されています。

『MSP430F1481デバイス正誤表』 には、機能仕様に対する既知の例外が記載されています。

『MSP430F147デバイス正誤表』 には、機能仕様に対する既知の例外が記載されています。

『MSP430F1471デバイス正誤表』 には、機能仕様に対する既知の例外が記載されています。

『MSP430F135デバイス正誤表』 には、機能仕様に対する既知の例外が記載されています。

『MSP430F133デバイス正誤表』 には、機能仕様に対する既知の例外が記載されています。

ユーザー・ガイド

『MSP430x1xxファミリ・ユーザー・ガイド』 このデバイス・ファミリで利用可能なすべてのモジュールとペリフェラルについての詳細情報です。

『MSP430 フラッシュ・デバイス・ブートローダ(BSL)ユーザー・ガイド』 MSP430™ブートローダ(BSL)を使用すると、プロトタイプ作成フェーズ、最終的な量産、およびサービス中に、MSP430マイクロコントローラ(MCU)の組み込みメモリと通信を行うことができます。必要に応じて、プログラム可能メモリ(フラッシュ・メモリ)とデータ・メモリ(RAM)の両方を変更できます。

『JTAGインターフェイスによるMSP430のプログラミング』 このドキュメントでは、JTAG通信ポートを使用してMSP430のフラッシュ・ベースおよびFRAMベースのマイクロコントローラ・ファミリのメモリ・モジュールを消去、プログラム、検証するために必要な機能について解説しています。さらに、すべてのMSP430デバイスで利用可能なJTAGアクセス・セキュリティ・ヒューズのプログラム方法についても解説しています。このドキュメントには、標準の4線式JTAGインターフェイスと2線式JTAGインターフェイスの両方を使用してデバイスにアクセスする方法が解説されています。2線式JTAGインターフェイスはSpy-Bi-Wire (SBW)とも呼ばれます。

『MSP430ハードウェア・ツール ユーザー・ガイド』 このマニュアルには、TI MSP-FET430フラッシュ・エミュレーション・ツール(FET)のハードウェアについて解説されています。このFETは、MSP430 超低消費電力マイクロコントローラ用のプログラム開発ツールです。利用可能なインターフェイスとして、パラレル・ポート・インターフェイスとUSBインターフェイスの両方について解説されています。

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アプリケーション・レポート

『MSP430 32kHz水晶発振器』 適切な水晶、正しい負荷回路、および適切な基板レイアウトの選択は、安定した水晶発振器のために重要です。このアプリケーション・レポートでは、水晶発振器の機能について要約し、MSP430の超低消費電力動作用の適切な水晶を選択するためのパラメータについて説明します。また、正しい基板レイアウトについてのヒントや例も紹介しています。このドキュメントには、量産時の安定した発振器の動作を保証するために行うことができる、発振器のテストについての詳細情報も記載されています。

『MSP430™ MCUのソフトウェア・コーディング技法』 このアプリケーション・レポートでは、MSP430 MCUのプログラマにとって有用なソフトウェア技法や関連トピックについて説明します。

『MSP ADCの一般的なオーバーサンプリングによる高分解能の実現』 複数のMSP430超低消費電力マイクロコントローラには、物理的な数量をデジタル数値に変換するためのADCがあり、この機能は多くのアプリケーションで広く使用されています。しかし、顧客の設計によっては、選択したMSPに搭載されているものよりも高分解能のADCが必要な場合があります。このアプリケーション・レポートでは、オーバーサンプリングの手法を組み入れて、現在利用可能なビット数を超えるADC分解能を実現する方法について説明します。

『MSP430 システム・レベルESDの考慮事項』 シリコン・テクノロジがますます低電圧化し、コスト効率に優れ非常に消費電力の低いコンポーネントを設計する必要性が高まっていくにつれ、システム・レベルESDの要求はますます高くなりつつあります。このアプリケーション・レポートでは、基板設計者とOEMが堅牢なシステム・レベルのデザインを理解し設計できるよう、3種類の異なるESDトピックについて扱います。

7.5 関連リンク

表 7-2 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 7-2. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
MSP430F149	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430F1491	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430F148	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430F1481	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430F147	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430F1471	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
MSP430F135	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

7.6 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Community

TI's Engineer-to-Engineer (E2E) Community. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas, and help solve problems with fellow engineers.

TI Embedded Processors Wiki

Texas Instruments Embedded Processors Wiki. Established to help developers get started with embedded processors from Texas Instruments and to foster innovation and growth of general knowledge about the hardware and software surrounding these devices.

7.7 商標

MSP430, MSP430Ware, Code Composer Studio, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

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7.8 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

7.9 Export Control Notice

Recipient agrees to not knowingly export or re-export, directly or indirectly, any product or technical data (as defined by the U.S., EU, and other Export Administration Regulations) including software, or any controlled product restricted by other applicable national regulations, received from disclosing party under nondisclosure obligations (if any), or any direct product of such technology, to any destination to which such export or re-export is restricted or prohibited by U.S. or other applicable laws, without obtaining prior authorization from U.S. Department of Commerce and other competent Government authorities to the extent required by those laws.

7.10 Glossary

TI Glossary This glossary lists and explains terms, acronyms, and definitions.

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8 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F133IPAG	ACTIVE	TQFP	PAG	64	160	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 85	M430F133	Samples
MSP430F133IPM	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F133	Samples
MSP430F133IPMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F133	Samples
MSP430F133IRTDT	ACTIVE	VQFN	RTD	64	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	M430F133	Samples
MSP430F135IPAG	ACTIVE	TQFP	PAG	64	160	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 85	M430F135 REV #	Samples
MSP430F135IPM	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F135 REV #	Samples
MSP430F135IPMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F135 REV #	Samples
MSP430F135IRTDR	ACTIVE	VQFN	RTD	64	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	M430F135	Samples
MSP430F135IRTDT	ACTIVE	VQFN	RTD	64	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	M430F135	Samples
MSP430F1471IPM	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F1471 REV #	Samples
MSP430F1471IPMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F1471 REV #	Samples
MSP430F1471IRTDT	ACTIVE	VQFN	RTD	64	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	M430F1471	Samples
MSP430F147IPAG	ACTIVE	TQFP	PAG	64	160	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 85	M430F147 REV #	Samples
MSP430F147IPM	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F147 REV #	Samples
MSP430F147IPMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F147 REV #	Samples
MSP430F147IPMR-KAM	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F147 REV #	Samples
MSP430F147IPMRG4	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F147 REV #	Samples
MSP430F147IRTDR	ACTIVE	VQFN	RTD	64	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	M430F147	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F147IRTDT	ACTIVE	VQFN	RTD	64	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	M430F147	Samples
MSP430F1481IPM	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F1481	Samples
MSP430F1481IPMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F1481	Samples
MSP430F1481IRTDT	ACTIVE	VQFN	RTD	64	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	M430F1481	Samples
MSP430F148IPAG	ACTIVE	TQFP	PAG	64	160	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 85	M430F148	Samples
MSP430F148IPM	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F148 REV #	Samples
MSP430F148IPMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F148 REV #	Samples
MSP430F148IRTDR	ACTIVE	VQFN	RTD	64	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	M430F148	Samples
MSP430F148IRTDT	ACTIVE	VQFN	RTD	64	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	M430F148	Samples
MSP430F1491IPM	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F1491	Samples
MSP430F1491IPMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F1491	Samples
MSP430F1491IRTDR	ACTIVE	VQFN	RTD	64	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	M430F1491	Samples
MSP430F1491IRTDT	ACTIVE	VQFN	RTD	64	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	M430F1491	Samples
MSP430F149IPAG	ACTIVE	TQFP	PAG	64	160	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 85	M430F149 REV #	Samples
MSP430F149IPAGR	ACTIVE	TQFP	PAG	64	1500	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 85	M430F149 REV #	Samples
MSP430F149IPM	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F149 REV #	Samples
MSP430F149IPMG4	ACTIVE	LQFP	PM	64	160	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F149 REV #	Samples
MSP430F149IPMR	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F149 REV #	Samples
MSP430F149IPMRG4	ACTIVE	LQFP	PM	64	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	M430F149 REV #	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430F149IRTDR	ACTIVE	VQFN	RTD	64	2500	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	M430F149	Samples
MSP430F149IRTDT	ACTIVE	VQFN	RTD	64	250	RoHS & Green	SN	Level-3-260C-168 HR	-40 to 85	M430F149	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

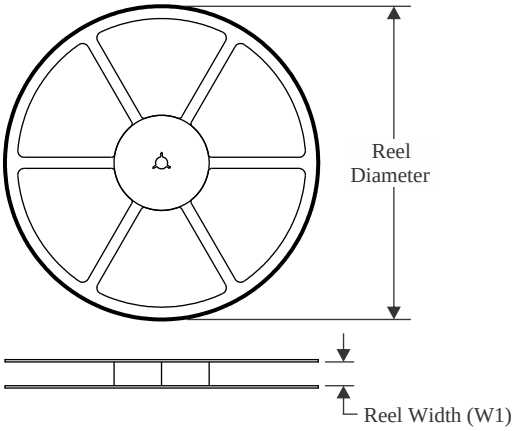
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

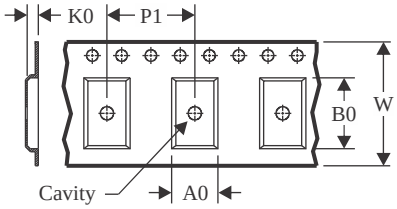
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

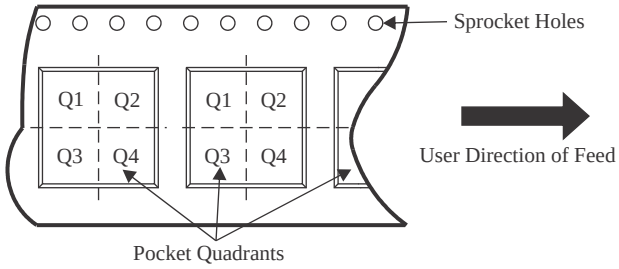


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

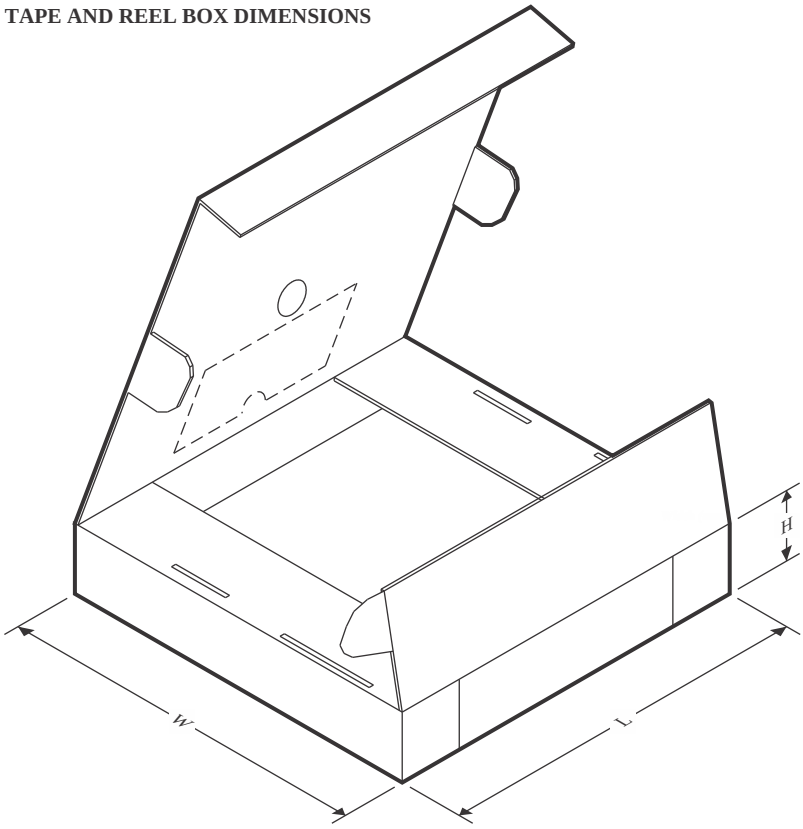


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F133IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F133IRTDT	VQFN	RTD	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F135IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F135IRTDR	VQFN	RTD	64	2500	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F135IRTDT	VQFN	RTD	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F1471IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F1471IRTDT	VQFN	RTD	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F147IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F147IRTDR	VQFN	RTD	64	2500	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F147IRTDT	VQFN	RTD	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F1481IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F1481IRTDT	VQFN	RTD	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F148IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F148IRTDR	VQFN	RTD	64	2500	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F148IRTDT	VQFN	RTD	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F1491IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430F1491IRTDR	VQFN	RTD	64	2500	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F1491IRTDT	VQFN	RTD	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F149IPAGR	TQFP	PAG	64	1500	330.0	24.4	13.0	13.0	1.5	16.0	24.0	Q2
MSP430F149IPMR	LQFP	PM	64	1000	330.0	24.4	13.0	13.0	2.1	16.0	24.0	Q2
MSP430F149IRTDR	VQFN	RTD	64	2500	330.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2
MSP430F149IRTDT	VQFN	RTD	64	250	180.0	16.4	9.3	9.3	1.5	12.0	16.0	Q2

TAPE AND REEL BOX DIMENSIONS

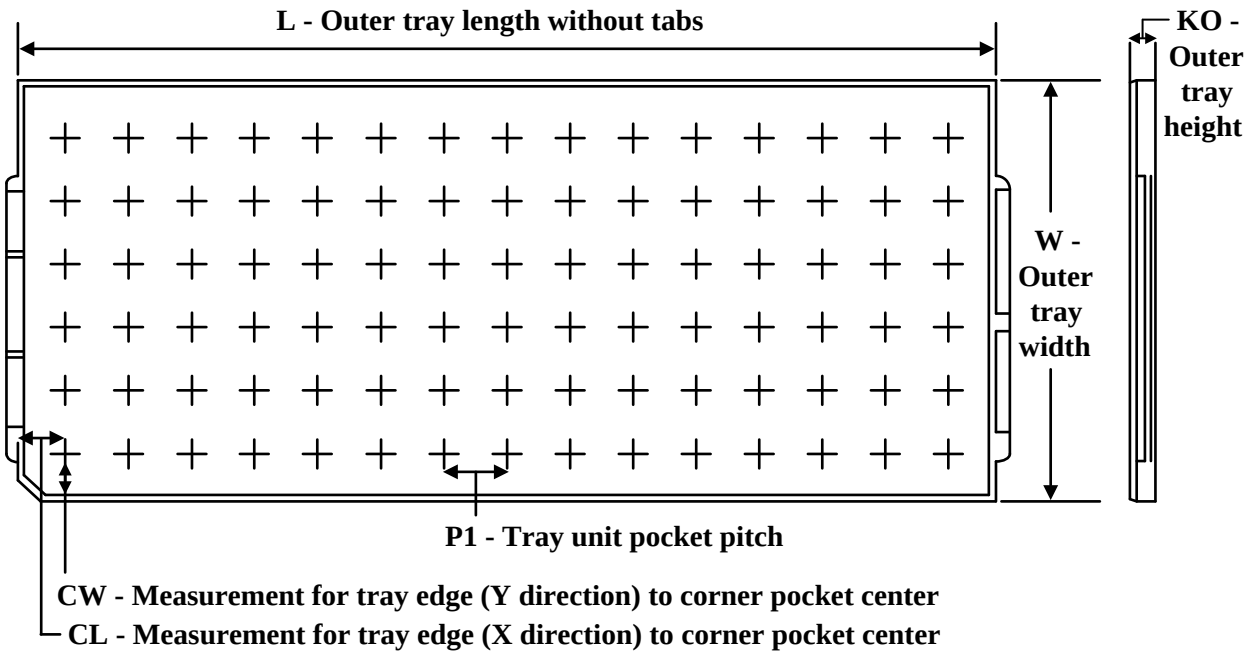


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F133IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F133IRTDT	VQFN	RTD	64	250	210.0	185.0	35.0
MSP430F135IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F135IRTDR	VQFN	RTD	64	2500	356.0	356.0	35.0
MSP430F135IRTDT	VQFN	RTD	64	250	210.0	185.0	35.0
MSP430F1471IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F1471IRTDT	VQFN	RTD	64	250	210.0	185.0	35.0
MSP430F147IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F147IRTDR	VQFN	RTD	64	2500	356.0	356.0	35.0
MSP430F147IRTDT	VQFN	RTD	64	250	210.0	185.0	35.0
MSP430F1481IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F1481IRTDT	VQFN	RTD	64	250	210.0	185.0	35.0
MSP430F148IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F148IRTDR	VQFN	RTD	64	2500	356.0	356.0	35.0
MSP430F148IRTDT	VQFN	RTD	64	250	210.0	185.0	35.0
MSP430F1491IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F1491IRTDR	VQFN	RTD	64	2500	356.0	356.0	35.0
MSP430F1491IRTDT	VQFN	RTD	64	250	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430F149IPAGR	TQFP	PAG	64	1500	350.0	350.0	43.0
MSP430F149IPMR	LQFP	PM	64	1000	336.6	336.6	41.3
MSP430F149IRTDR	VQFN	RTD	64	2500	356.0	356.0	35.0
MSP430F149IRTDT	VQFN	RTD	64	250	210.0	185.0	35.0

TRAY



Chamfer on Tray corner indicates Pin 1 orientation of packed units.

*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
MSP430F133IPAG	PAG	TQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
MSP430F133IPM	PM	LQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
MSP430F133IPM	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
MSP430F135IPAG	PAG	TQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
MSP430F135IPM	PM	LQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
MSP430F135IPM	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
MSP430F1471IPM	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
MSP430F1471IPM	PM	LQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
MSP430F147IPAG	PAG	TQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
MSP430F147IPM	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
MSP430F147IPM	PM	LQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
MSP430F1481IPM	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
MSP430F1481IPM	PM	LQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
MSP430F148IPAG	PAG	TQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
MSP430F148IPM	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
MSP430F148IPM	PM	LQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
MSP430F1491IPM	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13

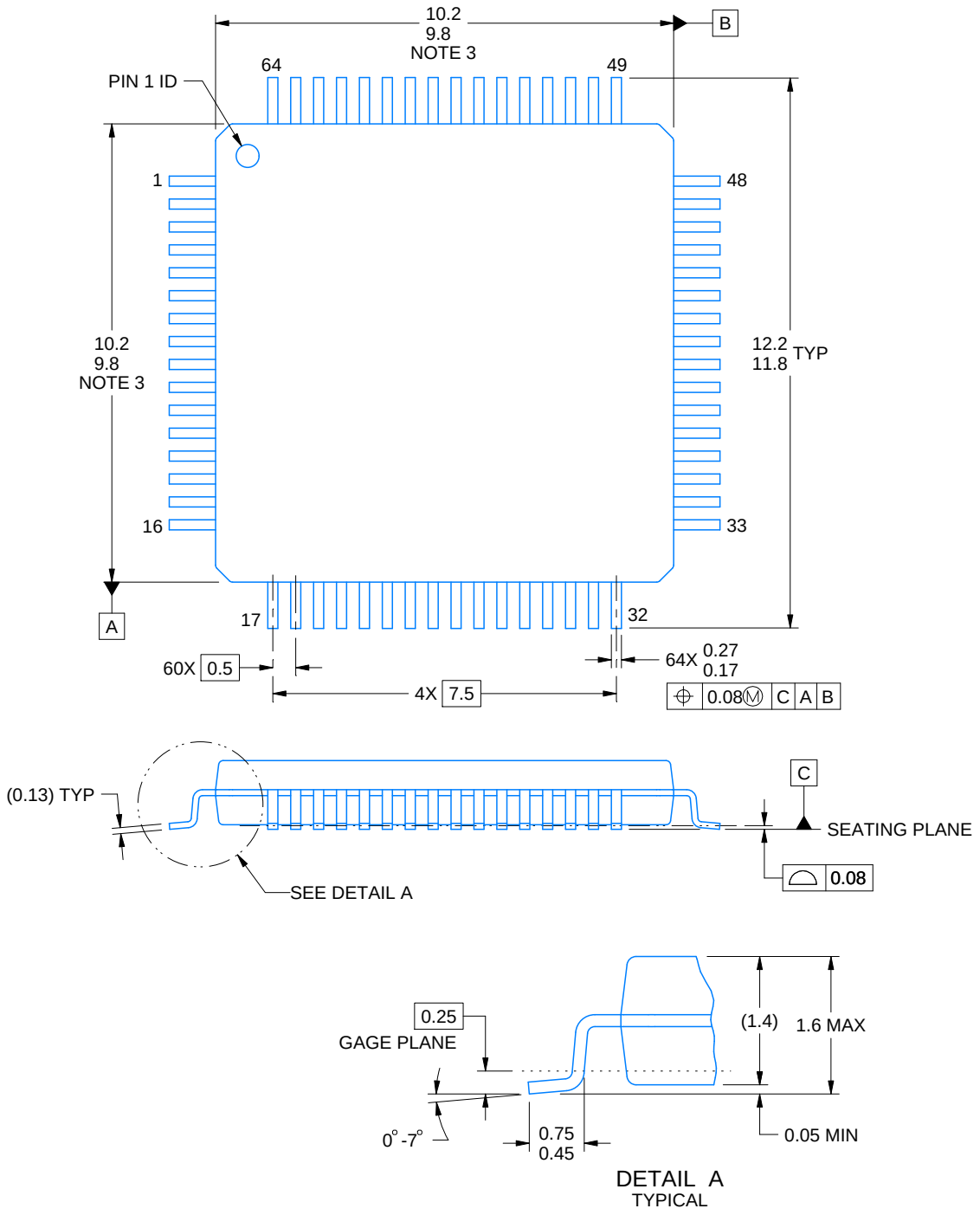
Device	Package Name	Package Type	Pins	SPQ	Unit array matrix	Max temperature (°C)	L (mm)	W (mm)	K0 (µm)	P1 (mm)	CL (mm)	CW (mm)
MSP430F1491IPM	PM	LQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
MSP430F149IPAG	PAG	TQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
MSP430F149IPM	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
MSP430F149IPM	PM	LQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13
MSP430F149IPMG4	PM	LQFP	64	160	8 X 20	150	315	135.9	7620	15.2	13.1	13
MSP430F149IPMG4	PM	LQFP	64	160	8 x 20	150	315	135.9	7620	15.2	13.1	13

PACKAGE OUTLINE

PM0064A

LQFP - 1.6 mm max height

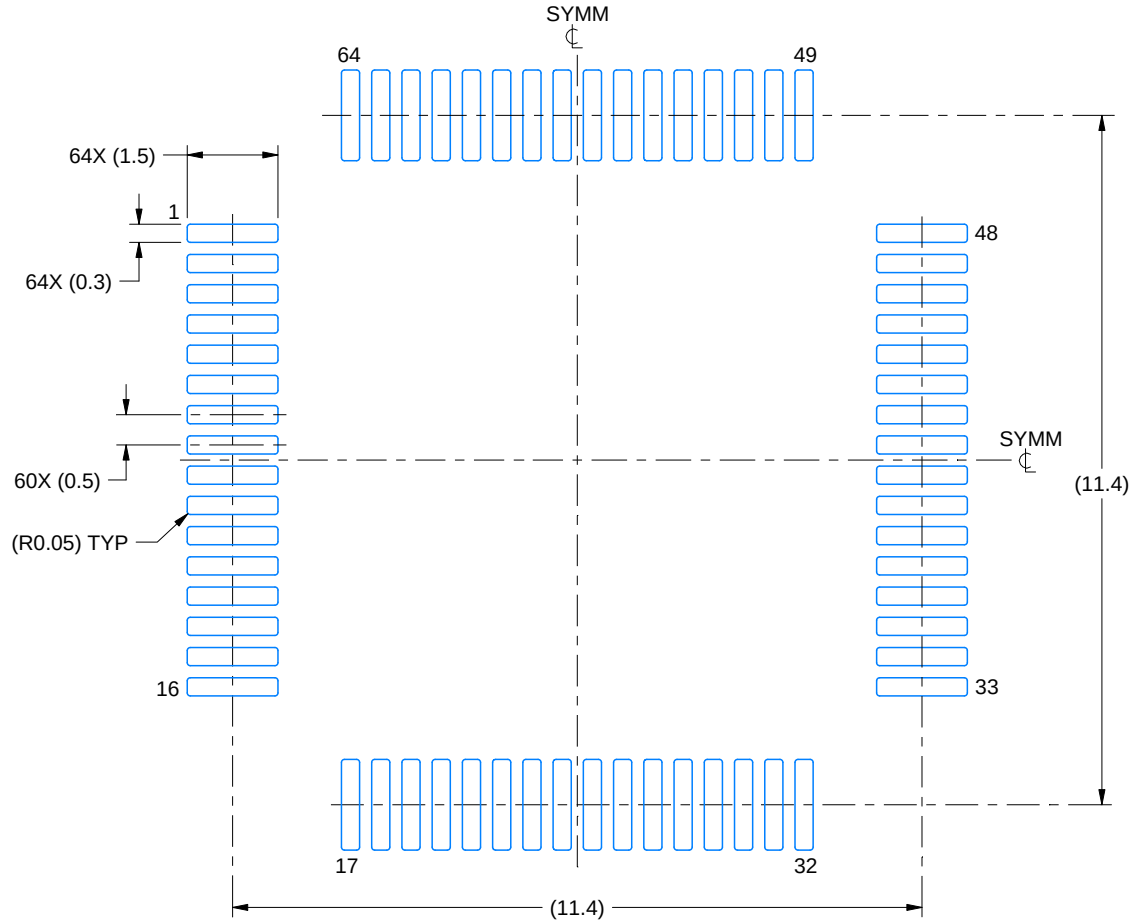
PLASTIC QUAD FLATPACK



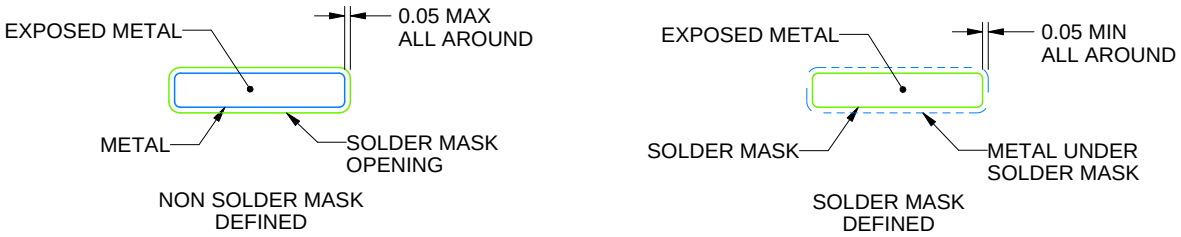
4215162/A 03/2017

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MS-026.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

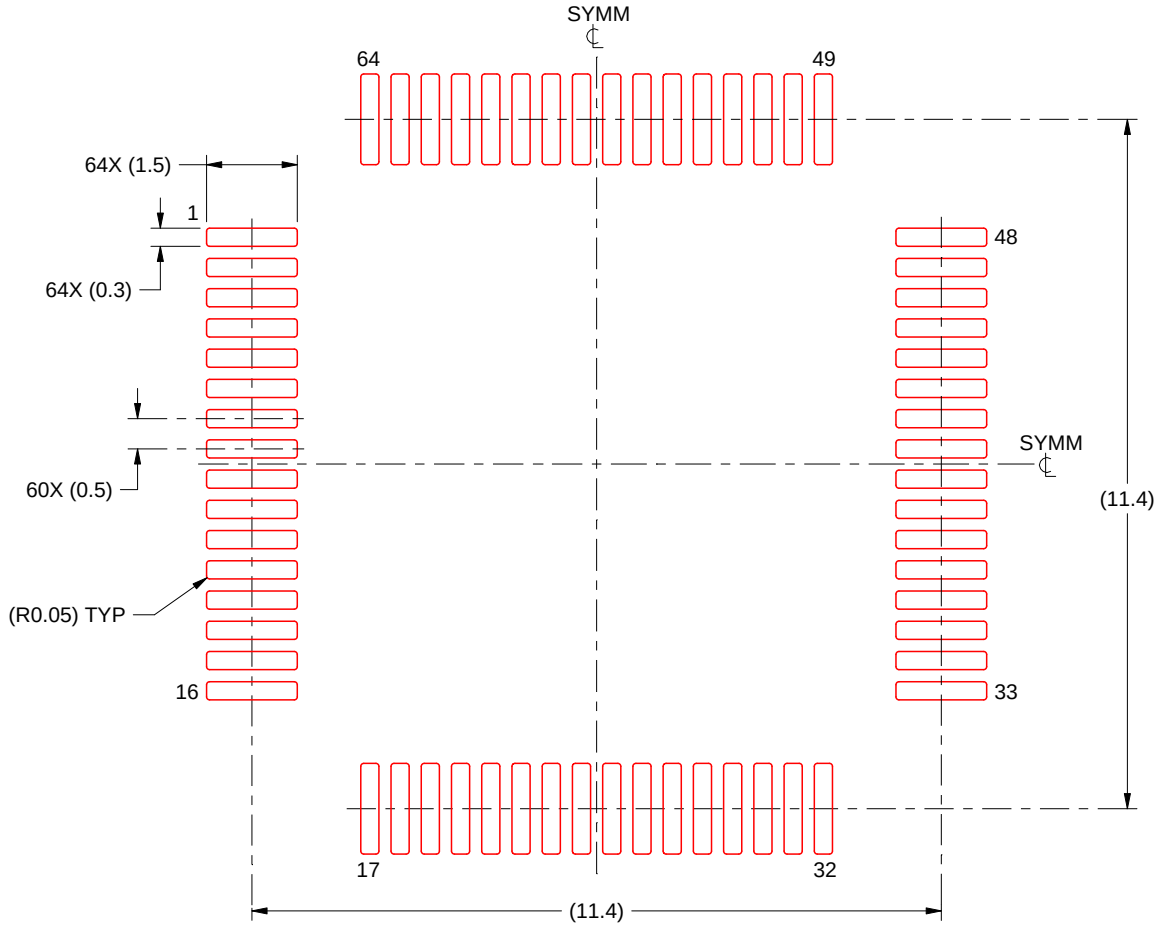


SOLDER MASK DETAILS

4215162/A 03/2017

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. For more information, see Texas Instruments literature number SLMA004 (www.ti.com/lit/slma004).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4215162/A 03/2017

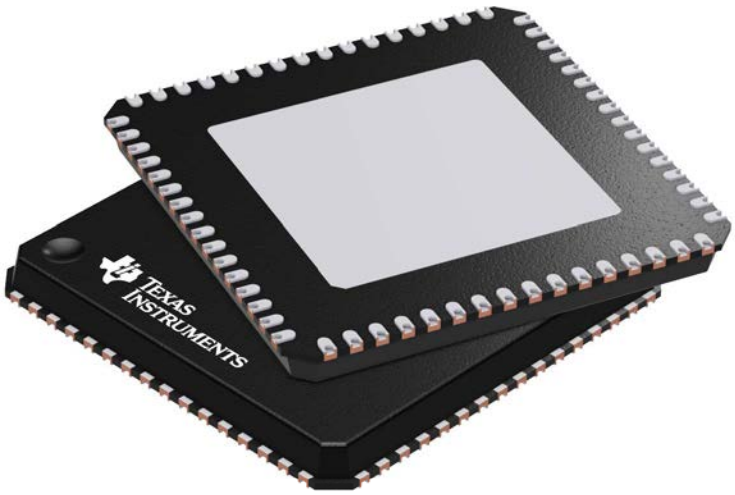
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

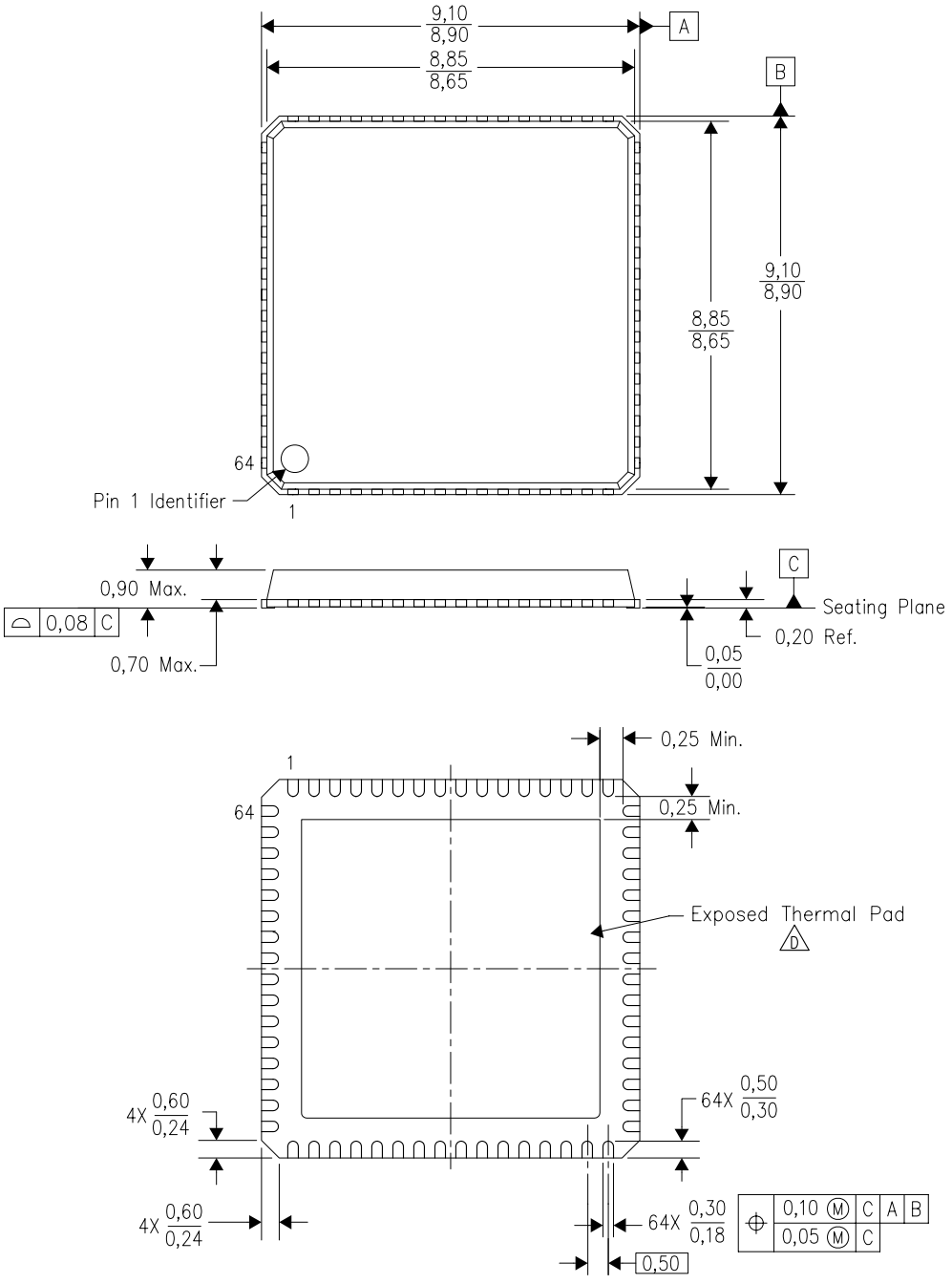
RTD 64 VQFNP - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

RTD (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) Package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.

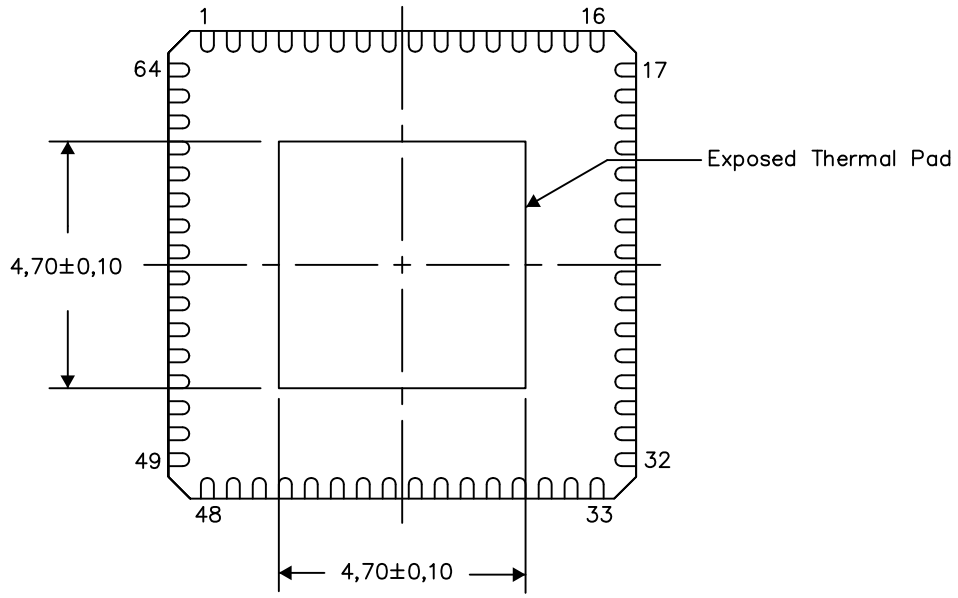
RTD (S–PVQFN–N64) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



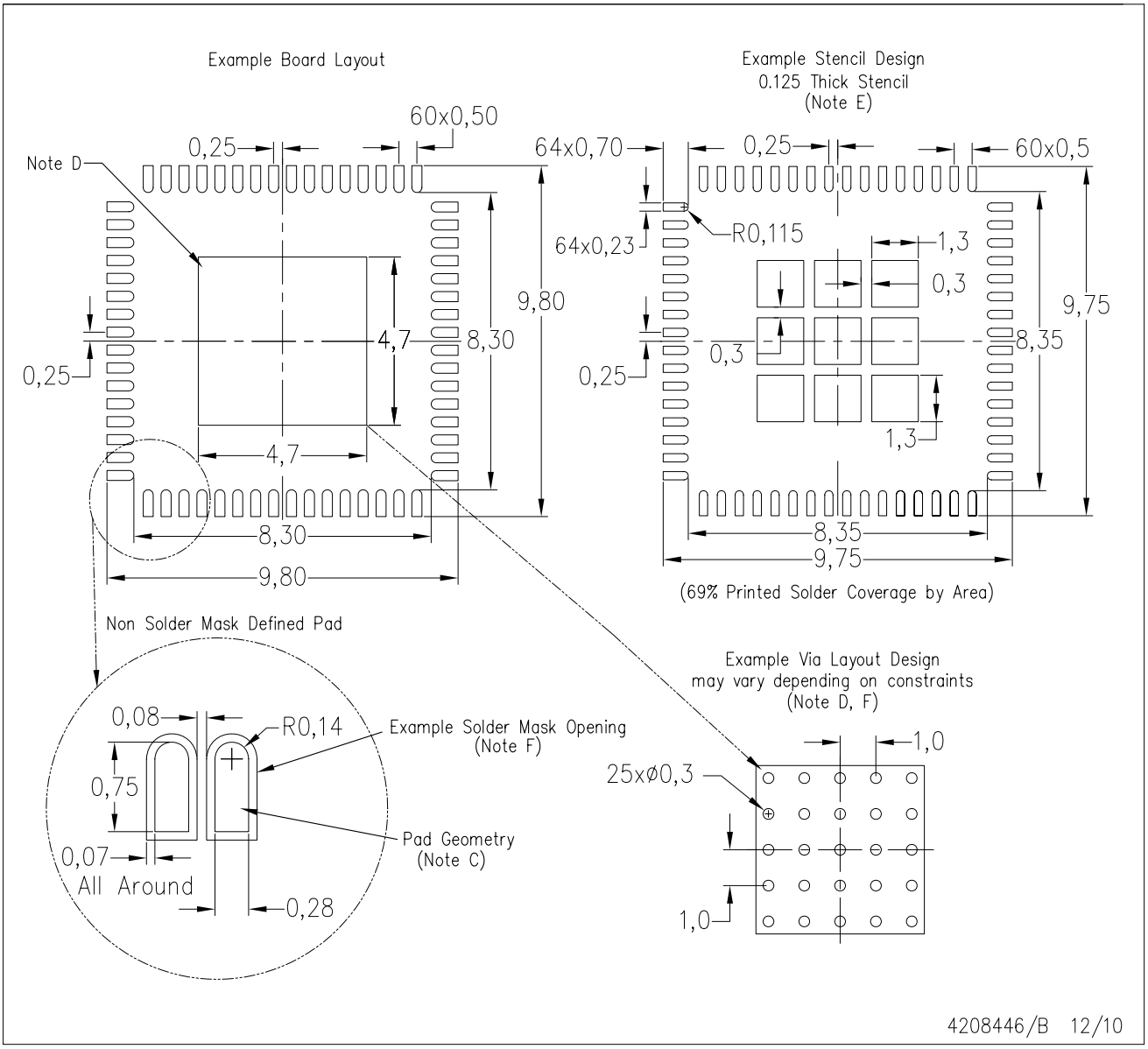
Bottom View

Exposed Thermal Pad Dimensions

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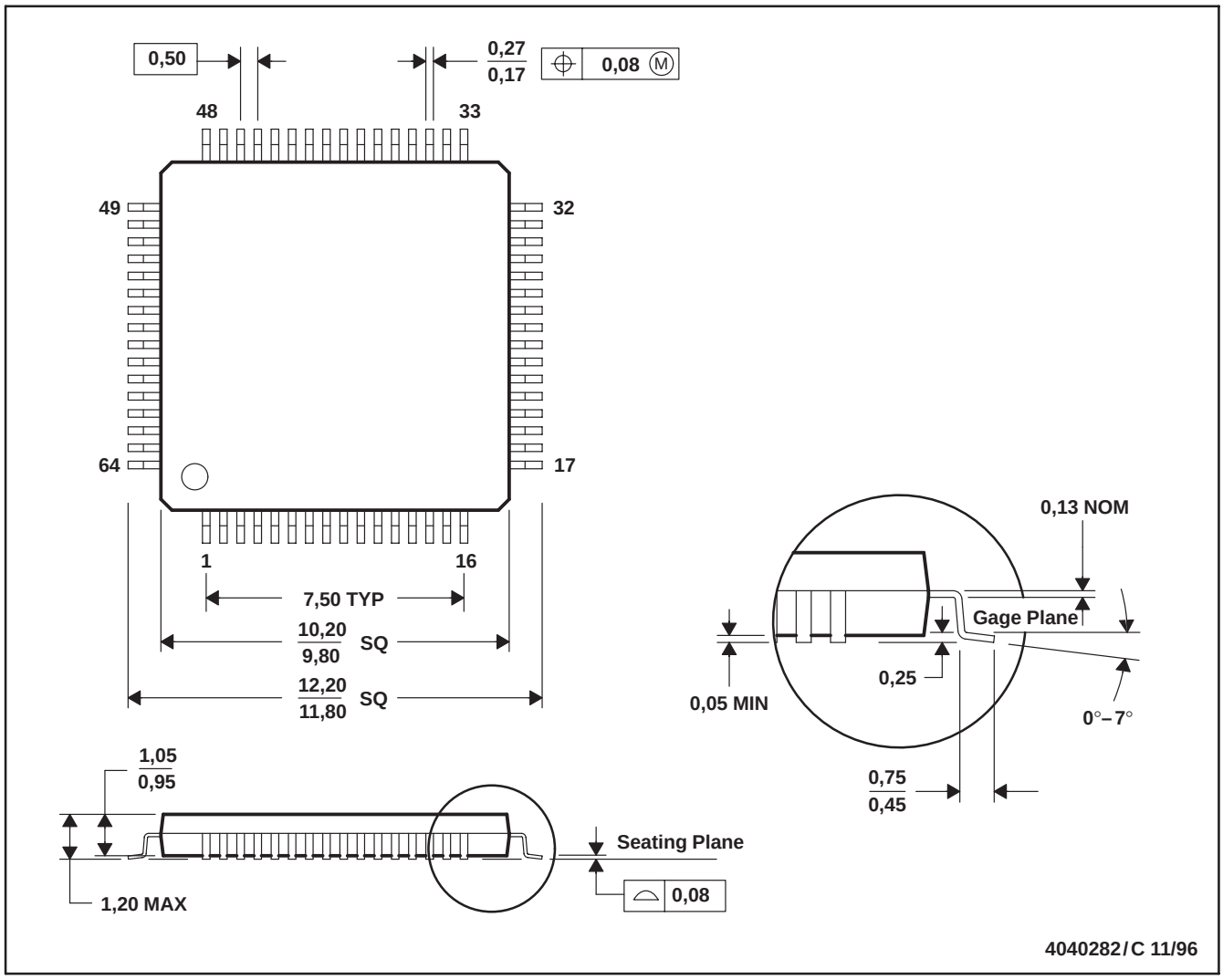
NOTE: A. All linear dimensions are in millimeters

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NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack Package, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http://www.ti.com>.
E. Laser cutting apertures with electropolish and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customer should contact their board fabrication site for recommended solder mask tolerances and vias tenting recommendations for vias placed int the thermal pad.

PAG (S-PQFP-G64) **PLASTIC QUAD FLATPACK**



NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-026

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