TEXAS INSTRUMENTS
MSP430FR2111, MSP430FR2110, MSP430FR2100, MSP430FR2000
JAJSCD6E – AUGUST 2016 – REVISED JUNE 2021

MSP430FR21xx および MSP430FR2000 ミクスト・シグナル・マイクロコントローラ

1 特長

- 組み込みマイクロコントローラ
  - 最高 16MHz の 16 ビット RISC アーキテクチャ
  - 3.6V ~ 1.8V の広い電源電圧範囲 (最小電源電圧は SVS レベルにより制限されます。SVS の仕様を参照)
- 最適化された低消費電力モード (3V 時)
  - アクティブ・モード：120µA/MHz
  - スタンバイ
    - LPM3.5 (VLO 作動)：1µA
    - リアルタイム・クロック (RTC) カウンタ (LPM3.5、32768Hz の水晶発振器を使用)：1µA
  - シャットダウン (LPM4.5)：34nA (SVS なし)
- 高性能アナログ
  - 8 チャネル、10 ビットの A/D コンバータ (ADC)
    - 温度センサ内蔵
    - 内蔵の 1.5V 基準電圧
    - サンプル・アンド・ホールド 200ksps
  - 拡張コンパレータ (eCOMP)
    - 基準電圧として 6 ビット DAC を搭載
    - ヒステリシスをプログラム可能
    - 高消費電力モードと低消費電力モードを構成可能
- 低消費電力の強誘電体 RAM (FRAM)
  - 最大 3.75KB の不揮発性メモリ
  - エラー訂正コード (ECC) 搭載
  - 書き込み保護を構成可能
  - プログラム、定数、ストレージのユニファイド・メモリ
  - 書き込みサイクルの耐久性：10^{15} 回
  - 放射線耐性と非磁性
- インテリジェントなデジタル・ペリフェラル
  - 3 つのキャプチャ / 比較レジスタを搭載した 16 ビット・タイマ (Timer_B3) × 1
  - 16 ビットのカウンタ専用 RTC × 1
  - 16 ビットの巡回冗長性検査 (CRC)
- 拡張シリアル通信
  - 拡張 USCI A (eUSCI_A) により UART、IrDA、SPI をサポート
- クロック・システム (CS)
  - オンチップの 32kHz RC 発振器 (REFO)
  - オンチップの 16MHz デジタル制御発振器 (DCO)、周波数ロック・ループ (FLL) 付き
    - オンチップの基準電圧は室温で ±1% 精度
  - オンチップの超低周波数 10kHz 発振器 (VLO)
  - オンチップの高周波数変調発振器 (MODOSC)
  - 外付けの 32kHz 水晶発振器 (LFXT)
  - 1 ~ 128 にプログラム可能な MCLK プリスケーラ
  - 1、2、4、8 にプログラム可能なプリスケーラを使って MCLK から SMCLK を生成
- 汎用入出力およびピン機能
  - 16 ピンのパッケージに 12 の I/O を搭載
  - 8 本の割り込みピン (P1 に 4 ピン、P2 に 4 ピン) により、MCU を LPM からウェイクアップ可能
  - すべての I/O で静電容量式タッチ機能をサポート
- 開発ツールとソフトウェア (「ツールとソフトウェア」も参照)
  - 無償のプロフェッショナル開発環境
  - 開発キット
    - MSP-TS430PW20
    - MSP-FET430U20
    - MSP-EXP430FR2311
    - MSP-EXP430FR4133
- ファミリ製品 (「デバイスの比較」も参照)
  - MSP430FR2111：プログラム用 FRAM 3.75KB、RAM 1KB
  - MSP430FR2110：プログラム用 FRAM 2KB、RAM 1KB
  - MSP430FR2100：プログラム用 FRAM 1KB、RAM 512 バイト
  - MSP430FR2000：プログラム用 FRAM 0.5KB、RAM 512 バイト
- パッケージ・オプション
  - 16 ピン：TSSOP (PW16)
  - 24 ピン：VQFN (RLL)

2 アプリケーション

- 家電機器用バッテリ・パック
- 煙感知器と熱感知器
- ドアや窓のセンサ
- 照明センサ
- 電力監視
- パーソナルケア家電
- ポータブル・ヘルスケア / フィットネス機器

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

3 概要

MSP430FR2000 および MSP430FR21xx デバイスは、MSP430™ マイクロコントローラ (MCU) バリュー・ライン・センシング・ポートフォリオの一部です。この超低消費電力、低コストの MCU ファミリは、0.5KB ~ 4KB の FRAM ユニファイド・メモリを搭載しており、小型の 3mm × 3mm VQFN パッケージを含む複数のパッケージ・オプションが用意されています。アーキテクチャ、FRAM、内蔵ペリフェラルに多様な低消費電力モードを組み合わせ、携帯型バッテリ駆動センシング・アプリケーションで長いバッテリ駆動時間を実現するように最適化されています。MSP430FR2000 および MSP430FR21xx デバイスでは、8 ビット設計からの移行パスとして、周辺機器の統合による追加機能、データのログ出力、FRAM の低消費電力などの利点を得られます。さらに、MSP430G2x MCU を使用する既存の設計を MSP430FR2000 および MSP430F21xx ファミリへ移行すると、性能が向上し、FRAM を活用できます。

MSP430FR2000 および MSP430FR21xx MCU には強力な 16 ビット RISC CPU、16 ビット・レジスタ、および定数ジェネレータが搭載されているため、最高水準のコード効率を実現できます。また、デジタル制御発振器 (DCO) により、デバイスは低消費電力モードからアクティブ・モードへ、通常は 10µs 以内にウェイクアップできます。この MCU の機能セットは、家電機器用のバッテリ・パックおよびバッテリ監視から、煙感知器やフィットネス・アクセサリまで、幅広いアプリケーションの要求に対応できます。

MSP 超低消費電力 (ULP) FRAM マイクロコントローラ・プラットフォームは、独自の組み込み FRAM と包括的な超低消費電力のシステム・アーキテクチャを組み合わせたものであり、システム設計において性能の向上と消費電力の削減を両立できます。FRAM テクノロジーは、RAM の低消費電力で高速な書き込み、柔軟性、耐久性と、フラッシュの不揮発性動作を併せ持つものです。

MSP430FR2000 および MSP430FR21x MCU は、ハードウェアおよびソフトウェアの大規模なエコシステムによってサポートされており、リファレンス・デザインやサンプル・コードを利用して設計をすぐに開始できます。開発キットには、MSP-EXP430FR2311 および MSP430FR4133 LaunchPad™ 開発キットと MSP-TS430PW20 20 ピン・ターゲット開発ボードがあります。また、テキサス・インスツルメンツは無償の MSP430Ware™ ソフトウェアも提供しており、Code Composer Studio™ IDE デスクトップのコンポーネントとして利用できます。また、TI Resource Explorer ではクラウド・バージョンを利用できます。MSP430 MCU は、テキサス・インスツルメンツのハウスキーピング・サンプル・シリーズ、MSP Academy トレーニング、TI E2E™ サポート・フォーラムによるオンライン・サポートなどの豊富なオンライン資料によってもサポートされています。

モジュールの詳細な説明については、『MSP430FR4xx および MSP430FR2xx ファミリ・ユーザー・ガイド』を参照してください。

デバイス情報

部品番号 (1)	パッケージ	本体サイズ (2)
MSP430FR2111IPW16	TSSOP (16)	5mm × 4.4mm
MSP430FR2110IPW16		
MSP430FR2100IPW16		
MSP430FR2000IPW16		
MSP430FR2111IRLL	VQFN (24)	3mm × 3mm
MSP430FR2110IRLL		
MSP430FR2100IRLL		
MSP430FR2000IRLL		

(1) 最新の製品、パッケージ、および注文情報については、セクション 12 の「*付録 : パッケージ・オプション*」またはテキサス・インスツルメンツ Web サイト (www.tij.co.jp) を参照してください。
(2) ここに記載されているサイズは概略です。許容公差を含めたパッケージの寸法については、セクション 12 の「*メカニカル・データ*」を参照してください。

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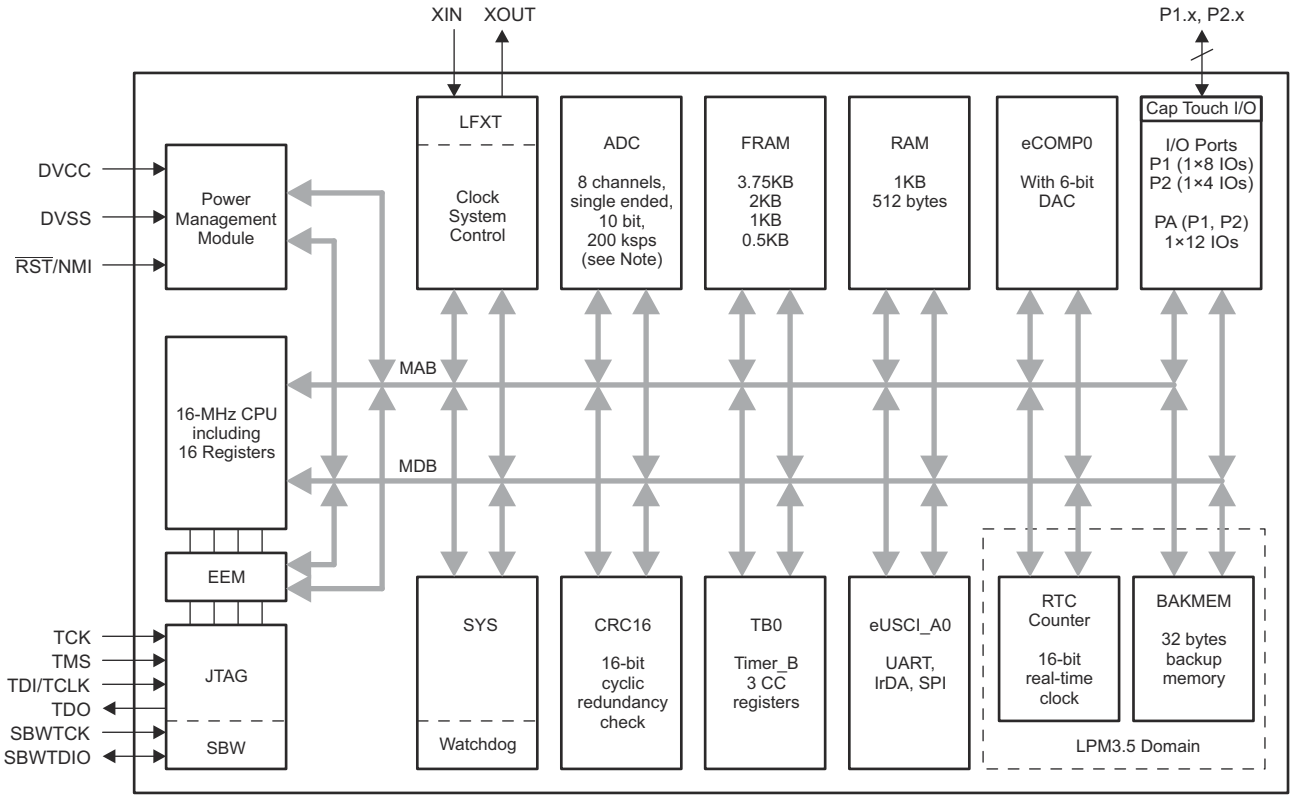
注意

電気的な過剰ストレスや、データやコード・メモリの不安定化を防止するため、デバイス・レベルの ESD 仕様に従って、システム・レベルの ESD 保護を適用する必要があります。詳細については、『MSP430™ のシステム・レベルの ESD に関する考慮事項』を参照してください。

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4 機能ブロック図

機能ブロック図を図 4-1 に示します。



注：MSP430FR2000 デバイスでは、この ADC を利用できません。

図 4-1. 機能ブロック図

- このデバイスには、DVCC および DVSS からなる 1 つの主電源ペアがあり、デジタルとアナログの両方のモジュールへ電力を供給します。バイパスおよびデカップリング・コンデンサとしては、それぞれ 4.7µF ~ 10µF および 0.1µF で、精度 ±5% が推奨されます。
- P1 の 4 本のピンと、P2 の 4 本のピンにはピン割り込み機能があり、LPM4、LPM3.5、LPM4.5 を含むすべての LPM から MCU をウェイクアップできます。
- Timer_B3 には 3 つのキャプチャ / 比較レジスタがあります。外部的に接続されているのは CCR1 および CCR2 のみです。CCR0 レジスタは、内部的な期間のタイミングと割り込みの生成にのみ使用できます。
- LPM3.5 では、RTC カウンタとバックアップ・メモリが動作し、他のペリフェラルはオフです。
- すべての汎用 I/O は、静電容量式タッチ I/O として構成可能です。

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5 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from revision D to revision E

Changes from December 11, 2019 to June 2, 2021	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• セクション 3「概要」を更新	2
• Updated セクション 6.1, *Related Products*	8
• Added a note about the specifications for the 1.5-V internal reference in セクション 8.12.5, *VREF+ Built-in Reference*	28
• Added inverter to Schmitt-trigger enable in 図 9-1	57

Changes from revision C to revision D

Changes from August 30, 2018 to December 10, 2019	Page
• Changed the note that begins "Supply voltage changes faster than 0.2 V/µs can trigger a BOR reset..." in セクション 8.3, *Recommended Operating Conditions*	15
• Added the note that begins "TI recommends that power to the DVCC pin must not exceed the limits..." in セクション 8.3, *Recommended Operating Conditions*	15
• Added the note that begins "A capacitor tolerance of ±20% or better is required..." in セクション 8.3, *Recommended Operating Conditions*	15
• Added the note "See *MSP430 32-kHz Crystal Oscillators* for details on crystal section, layout, and testing" to セクション 8.12.3.1, *XT1 Crystal Oscillator (Low Frequency)*	22
• Changed the note that begins "Requires external capacitors at both terminals..." in セクション 8.12.3.1, *XT1 Crystal Oscillator (Low Frequency)*	22
• Added the $t_{(int)}$ parameter in セクション 8.12.4.1, *Digital Inputs*	26
• Changed the parameter symbol from R_I to $R_{I,MUX}$ in セクション 8.12.8.1, *ADC, Power Supply and Input Range Conditions*	33
• Corrected the test conditions for the $R_{I,MUX}$ parameter in セクション 8.12.8.1, *ADC, Power Supply and Input Range Conditions*	33
• Added $R_{I,Misc}$ TYP value of 34 kΩ in セクション 8.12.8.1, *ADC, Power Supply and Input Range Conditions*	33
• Added $t_{CONVERT}$ for external ADCCLK source in セクション 8.12.8.2, *ADC, 10-Bit Timing Parameters*	33
• Added formula for R_I in セクション 8.12.8.2, *ADC, 10-Bit Timing Parameters*	33
• Added the note that begins "$t_{Sample} = \ln(2^{n+1}) \times \tau$ ..." in セクション 8.12.8.2, *ADC, 10-Bit Timing Parameters*	33
• Removed the description of "±3°C" in table note that starts "The device descriptor structure ..." of セクション 8.12.8.3, *ADC, 10-Bit Linearity Parameters*	34
• Corrected bitfield from IRDSEL to IRDSSEL in セクション 9.11.8, *Timers (Timer0_B3)*, in the description that starts "The interconnection of Timer0_B3 ... "	48
• Corrected the ADCINCHx column heading in 表 9-14, *ADC Channel Connections*	49
• Added P1SELC information in 表 9-26, *Port P1, P2 Registers (Base Address: 0200h)*	52
• Added P2SELC information in 表 9-26, *Port P1, P2 Registers (Base Address: 0200h)*	52

Changes from revision B to revision C

Changes from July 14, 2017 to August 29, 2018	Page
• Added note to V_{SVSH-} and V_{SVSH+} parameters in セクション 8.12.1.1, *PMM, SVS and BOR*	21
• Added the note "Controlled by the RTCCKSEL bit in the SYSCFG2 register" on 表 9-7, *Clock Distribution*	44
• Changed 1 µF capacitor to 10 µF in 図 10-1, *Power Supply Decoupling*	63
• Updated text and figure in セクション 11.2, *Device Nomenclature*	68

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Changes from revision A to revision B

Changes from August 13, 2016 to July 13, 2017	Page
• MSP430FR2100 および MSP430FR2000 デバイスを追加	1
• セクション 1 「*特長*」の項目を再編成	1
• ドキュメント全体で、RLL パッケージのパッケージ・ファミリを訂正 (QFN を VQFN に変更)	1
• 「セクション 2」のアプリケーション一覧を更新	1
• セクション 3「概要」を更新	2
• 図 4-1「*機能ブロック図*」で、*ポート P1 のビット数を訂正*	4
• Updated the note that starts "This is the remapped functionality controlled by the TBRMP bit..." in 表 7-2, *Signal Descriptions*	12
• Updated the note that starts "This is the remapped functionality controlled by the USCIARMP bit..." in 表 7-2, *Signal Descriptions*	12
• Removed former Figure 5-2, *Low-Power Mode 3 Supply Current vs Temperature*	19
• Updated notes on セクション 8.11, *Thermal Resistance Characteristics*	20
• Changed the entry for eUSCI_A in the LPM3 column from Off to Optional in 表 9-1, *Operating Modes*	39
• Updated the note that starts "This is the remapped functionality controlled by the USCIARMP bit..." in 表 9-11, *eUSCI Pin Configurations*	47
• Updated the note that starts "This is the remapped functionality controlled by the TBRMP bit..." in 表 9-12, *Timer0_B3 Signal Connections*	48
• Removed SYSBERRIV register (not supported) from 表 9-21, *SYS Registers*	52
• Updated descriptions of "Design Kits and Evaluation Modules" in セクション 11.3, *Tools and Software*	69

Changes from initial release to revision A

Changes from August 11, 2016 to August 12, 2016	Page
• ドキュメントのステータスを「製品プレビュー」から「量産データ」に変更	1

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6 Device Comparison

表 6-1 summarizes the features of the available family members.

表 6-1. Device Comparison

DEVICE(1) (2)	PROGRAM FRAM (Kbytes)	SRAM (Bytes)	TB0	eUSCI_A	10-BIT ADC CHANNELS	eCOMP0	I/O	PACKAGE
MSP430FR2111IPW16	3.75	1024	3 × CCR(3)	1	8	1	12	16 PW (TSSOP)
MSP430FR2110IPW16	2	1024	3 × CCR(3)	1	8	1	12	16 PW (TSSOP)
MSP430FR2100IPW16	1	512	3 × CCR(3)	1	8	1	12	16 PW (TSSOP)
MSP430FR2000IPW16	0.5	512	3 × CCR(3)	1	–	1	12	16 PW (TSSOP)
MSP430FR2111IRLL	3.75	1024	3 × CCR(3)	1	8	1	12	24 RLL (VQFN)
MSP430FR2110IRLL	2	1024	3 × CCR(3)	1	8	1	12	24 RLL (VQFN)
MSP430FR2100IRLL	1	512	3 × CCR(3)	1	8	1	12	24 RLL (VQFN)
MSP430FR2000IRLL	0.5	512	3 × CCR(3)	1	–	1	12	24 RLL (VQFN)

(1) For the most current device, package, and ordering information, see the *Package Option Addendum* in セクション 12, or see the TI website at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/packaging
(3) A CCR register is a configurable register that provides internal and external capture or compare inputs, or internal and external PWM outputs.

6.1 Related Products

For information about other devices in this family of products or related products, see the following links.

Overview of Microcontrollers (MCUs) & processors

Our diverse portfolio of 16- and 32-bit microcontrollers (MCUs) with real-time control capabilities and high-precision analog integration are optimized for industrial and automotive applications. Backed by decades of expertise and innovative hardware and software solutions, our MCUs can meet the needs of any design and budget.

Overview of MSP430™ microcontrollers (MCUs)

Our 16-bit MSP430™ microcontrollers (MCUs) provide affordable solutions for all applications. Our leadership in integrated precision analog enables designers to enhance system performance and lower system costs. Designers can find a cost-effective MCU within the broad MSP430 portfolio of over 2000 devices for virtually any need. Get started quickly and reduce time to market with our simplified tools, software, and best-in-class support.

Reference designs

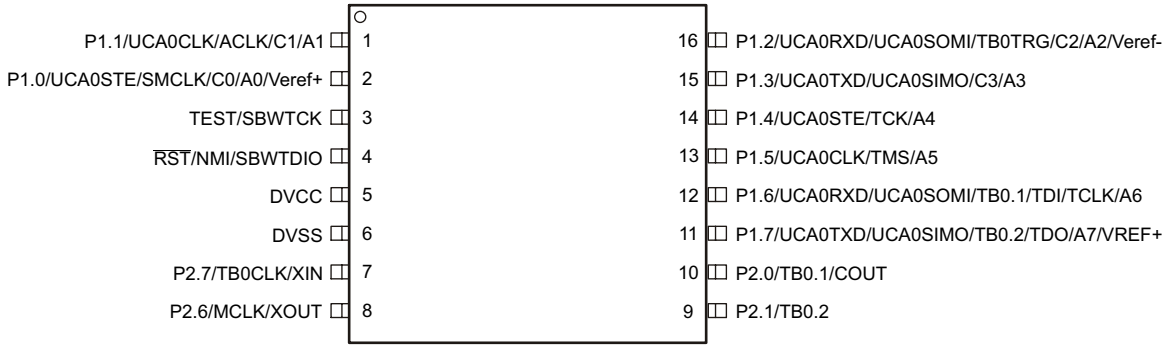
Find reference designs leveraging the best in TI technology – from analog and power management to embedded processors.

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7 Terminal Configuration and Functions

7.1 Pin Diagrams

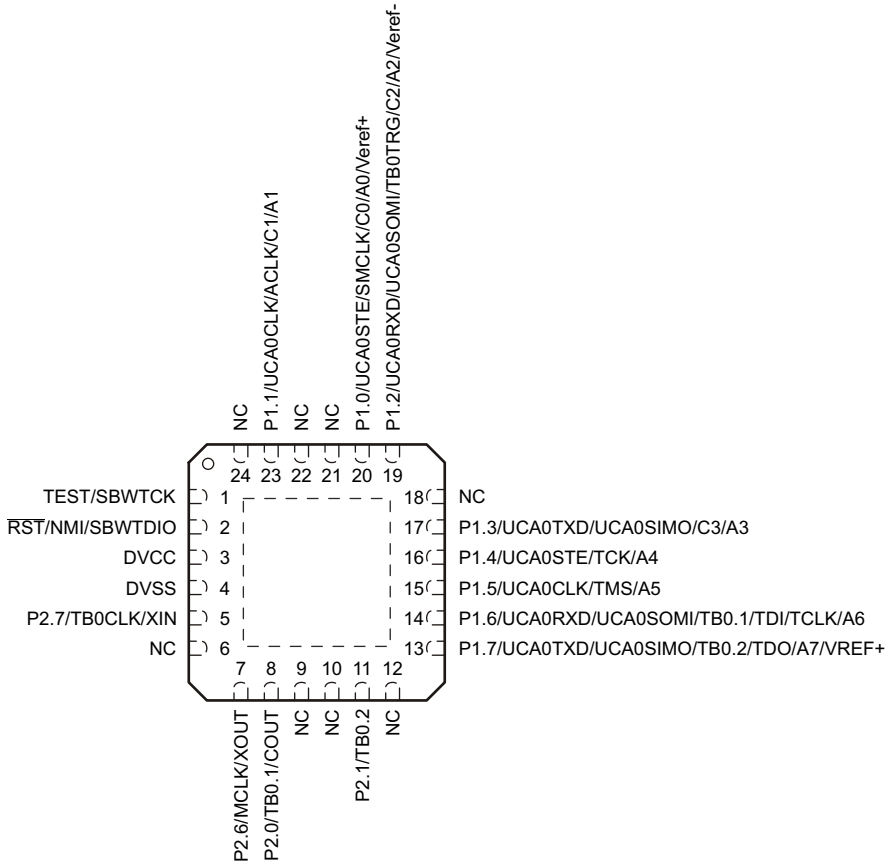
図 7-1 shows the pinout of the 16-pin PW package.



The ADC (signals A0 to A7, Veref+, and Veref-) is not available on the MSP430FR2000 device.

図 7-1. 16-Pin PW (TSSOP) (Top View)

図 7-2 shows the pinout of the 24-pin RLL package.



The ADC (signals A0 to A7, Veref+, and Veref-) is not available on the MSP430FR2000 device.

図 7-2. 24-Pin RLL (VQFN) (Top View)

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7.2 Pin Attributes

表 7-1 lists the attributes of all pins.

表 7-1. Pin Attributes

PIN NUMBER		SIGNAL NAME[1] [2]	SIGNAL TYPE[3]	BUFFER TYPE[4]	POWER SOURCE	RESET STATE AFTER BOR[5]
PW16	RLL					
1	23	P1.1 (RD)	I/O	LVCMOS	DVCC	OFF
		UCA0CLK	I/O	LVCMOS	DVCC	–
		ACLK	O	LVCMOS	DVCC	–
		C1	I	Analog	DVCC	–
		A1[6]	I	Analog	DVCC	–
2	20	P1.0 (RD)	I/O	LVCMOS	DVCC	OFF
		UCA0STE	I/O	LVCMOS	DVCC	–
		SMCLK	O	LVCMOS	DVCC	–
		C0	I	Analog	DVCC	–
		A0[6]	I	Analog	DVCC	–
		Veref+[6]	I	Power	DVCC	–
3	1	TEST (RD)	I	LVCMOS	DVCC	OFF
		SBWTCK	I	LVCMOS	DVCC	–
4	2	$\overline{\text{RST}}$ (RD)	I/O	LVCMOS	DVCC	OFF
		NMI	I	LVCMOS	DVCC	–
		SBWTDIO	I/O	LVCMOS	DVCC	–
5	3	DVCC	P	Power	DVCC	N/A
6	4	DVSS	P	Power	DVCC	N/A
7	5	P2.7 (RD)	I/O	LVCMOS	DVCC	OFF
		TB0CLK	I	LVCMOS	DVCC	–
		XIN	I	LVCMOS	DVCC	–
8	7	P2.6 (RD)	I/O	LVCMOS	DVCC	OFF
		MCLK	O	LVCMOS	DVCC	–
		XOUT	O	LVCMOS	DVCC	–
9	11	P2.1(RD)	I/O	LVCMOS	DVCC	OFF
		TB0.2	I/O	LVCMOS	DVCC	–
10	8	P2.0 (RD)	I/O	LVCMOS	DVCC	OFF
		TB0.1	I/O	LVCMOS	DVCC	–
		COUT	O	LVCMOS	DVCC	–
11	13	P1.7 (RD)	I/O	LVCMOS	DVCC	OFF
		UCA0TXD	O	LVCMOS	DVCC	–
		UCA0SIMO	I/O	LVCMOS	DVCC	–
		TB0.2	I/O	LVCMOS	DVCC	–
		TDO	O	LVCMOS	DVCC	–
		A7[6]	I	Analog	DVCC	–
		VREF+	O	Power	DVCC	–

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表 7-1. Pin Attributes (continued)

PIN NUMBER		SIGNAL NAME[1] [2]	SIGNAL TYPE[3]	BUFFER TYPE[4]	POWER SOURCE	RESET STATE AFTER BOR[5]
PW16	RLL					
12	14	P1.6 (RD)	I/O	LVCMOS	DVCC	OFF
		UCA0RXD	I	LVCMOS	DVCC	–
		UCA0SOMI	I/O	LVCMOS	DVCC	–
		TB0.1	I/O	LVCMOS	DVCC	–
		TDI	I	LVCMOS	DVCC	–
		TCLK	I	LVCMOS	DVCC	–
		A6[6]	I	Analog	DVCC	–
13	15	P1.5 (RD)	I/O	LVCMOS	DVCC	OFF
		UCA0CLK	I/O	LVCMOS	DVCC	–
		TMS	I	LVCMOS	DVCC	–
		A5[6]	I	Analog	DVCC	
14	16	P1.4 (RD)	I/O	LVCMOS	DVCC	OFF
		UCA0STE	I/O	LVCMOS	DVCC	–
		TCK	I	LVCMOS	DVCC	–
		A4[6]	I	Analog	DVCC	–
15	17	P1.3 (RD)	I/O	LVCMOS	DVCC	OFF
		UCA0TXD	O	LVCMOS	DVCC	–
		UCA0SIMO	I/O	LVCMOS	DVCC	–
		C3	I	Analog	DVCC	–
		A3[6]	I	Analog	DVCC	–
16	19	P1.2 (RD)	I/O	LVCMOS	DVCC	OFF
		UCA0RXD	I	LVCMOS	DVCC	–
		UCA0SOMI	I/O	LVCMOS	DVCC	–
		TB0TRG	I	LVCMOS	DVCC	–
		C2	I	Analog	DVCC	–
		A2[6]	I	Analog	DVCC	–
		Veref-[6]	I	Power	DVCC	–
	6, 9, 10, 12, 18, 21, 22, 24	NC[7]	–	–	–	–

(1) Signals names with (RD) denote the reset default pin name.
(2) To determine the pin mux encodings for each pin, see セクション 9.11.15.
(3) Signal Types: I = Input, O = Output, I/O = Input or Output.
(4) Buffer Types: LVCMOS, Analog, or Power (see セクション 7.6)
(5) Reset States:
OFF = High-impedance input with pullup or pulldown disabled (if available)
N/A = Not applicable
(6) The ADC is not available on the MSP430FR2000 device.
(7) NC = Not connected

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7.3 Signal Descriptions

表 7-2 describes the signals for all device variants and package options.

表 7-2. Signal Descriptions

FUNCTION	SIGNAL NAME	PIN NUMBER		PIN TYPE	DESCRIPTION
		PW16	RLL		
ADC(1)	A0	2	20	I	Analog input A0
	A1	1	23	I	Analog input A1
	A2	16	19	I	Analog input A2
	A3	15	17	I	Analog input A3
	A4	14	16	I	Analog input A4
	A5	13	15	I	Analog input A5
	A6	12	14	I	Analog input A6
	A7	11	13	I	Analog input A7
	Veref+	2	20	I	ADC positive reference
	Veref-	16	19	I	ADC negative reference
eCOMP0	C0	2	20	I	Comparator input channel C0
	C1	1	23	I	Comparator input channel C1
	C2	16	19	I	Comparator input channel C2
	C3	15	17	I	Comparator input channel C3
	COUT	10	8	O	Comparator output channel COUT
Clock	ACLK	1	23	O	ACLK output
	MCLK	8	7	O	MCLK output
	SMCLK	2	20	O	SMCLK output
	XIN	7	5	I	Input terminal for crystal oscillator
	XOUT	8	7	O	Output terminal for crystal oscillator
Debug	SBWTCK	3	1	I	Spy-Bi-Wire input clock
	SBWTDIO	4	2	I/O	Spy-Bi-Wire data input/output
	TCK	14	16	I	Test clock
	TCLK	12	14	I	Test clock input
	TDI	12	14	I	Test data input
	TDO	11	13	O	Test data output
	TMS	13	15	I	Test mode select
	TEST	3	1	I	Test mode pin – selected digital I/O on JTAG pins
System	NMI	4	2	I	Nonmaskable interrupt input
	$\overline{\text{RST}}$	4	2	I/O	Reset input, active low
Power	DVCC	5	3	P	Power supply
	DVSS	6	4	P	Power ground
	VREF+	11	13	P	Output of positive reference voltage with ground as reference

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表 7-2. Signal Descriptions (continued)

FUNCTION	SIGNAL NAME	PIN NUMBER		PIN TYPE	DESCRIPTION
		PW16	RLL		
GPIO	P1.0	2	20	I/O	General-purpose I/O
	P1.1	1	23	I/O	General-purpose I/O
	P1.2	16	19	I/O	General-purpose I/O
	P1.3	15	17	I/O	General-purpose I/O
	P1.4	14	16	I/O	General-purpose I/O (2)
	P1.5	13	15	I/O	General-purpose I/O (2)
	P1.6	12	14	I/O	General-purpose I/O(2)
	P1.7	11	13	I/O	General-purpose I/O(2)
	P2.0	10	8	I/O	General-purpose I/O
	P2.1	9	11	I/O	General-purpose I/O
	P2.6	8	7	I/O	General-purpose I/O
	P2.7	7	5	I/O	General-purpose I/O
SPI and UART	UCA0CLK	13	15	I/O	eUSCI_A0 SPI clock input/output
	UCA0RXD	12	14	I	eUSCI_A0 UART receive data
	UCA0SIMO	11	13	I/O	eUSCI_A0 SPI slave in/master out
	UCA0SOMI	12	14	I/O	eUSCI_A0 SPI slave out/master in
	UCA0STE	14	16	I/O	eUSCI_A0 SPI slave transmit enable
	UCA0TXD	11	13	O	eUSCI_A0 UART transmit data
	UCA0CLK(4)	1	23	I/O	eUSCI_A0 SPI clock input/output
	UCA0RXD(4)	16	19	I	eUSCI_A0 UART receive data
	UCA0SIMO(4)	15	17	I/O	eUSCI_A0 SPI slave in/master out
	UCA0SOMI(4)	16	19	I/O	eUSCI_A0 SPI slave out/master in
	UCA0STE(4)	2	20	I/O	eUSCI_A0 SPI slave transmit enable
	UCA0TXD(4)	15	17	O	eUSCI_A0 UART transmit data
Timer_B	TB0.1	12	14	I/O	Timer TB0 CCR1 capture: CCI1A input, compare: Out1 outputs
	TB0.2	11	13	I/O	Timer TB0 CCR2 capture: CCI2A input, compare: Out2 outputs
	TB0CLK	7	5	I	Timer clock input TBCLK for TB0
	TB0TRG	16	19	I	TB0 external trigger input for TB0OUTH
	TB0.1(3)	10	8	I/O	Timer TB0 CCR1 capture: CCI1A input, compare: Out1 outputs
	TB0.2(3)	9	11	I/O	Timer TB0 CCR2 capture: CCI2A input, compare: Out2 outputs
NC pad	NC	–	6, 9, 10, 12, 18, 21, 22, 24	–	Do not connect
VQFN pad	Pad	–	Pad		VQFN package (RLL) exposed thermal pad. Connect to V_{SS}.

(1) The ADC is not available on the MSP430FR2000 device.
(2) Because this pin is multiplexed with the JTAG function, TI recommends disabling the pin interrupt function while in JTAG debug to prevent collisions.
(3) This is the remapped functionality controlled by the TBRMP bit in the SYSCFG3 register. Only one selected port is valid at the same time when TB0 acts as capture input functionality. TB0 PWM outputs regardless of the setting on this remap bit.
(4) This is the remapped functionality controlled by the USCIARMP bit in the SYSCFG3 register. Only one selected port is valid at the same time.

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7.4 Pin Multiplexing

Pin multiplexing for these devices is controlled by both register settings and operating modes (for example, if the device is in test mode). For details of the settings for each pin and schematics of the multiplexed ports, see セクション 9.11.15.

7.5 Connection of Unused Pins

表 7-3 lists the correct termination of unused pins.

表 7-3. Connection of Unused Pins

PIN(1)	POTENTIAL	COMMENT
Px.0 to Px.7	Open	Set to port function, output direction (PxDIR.n = 1)
$\overline{\text{RST}}$/NMI	DVCC	47-kΩ pullup or internal pullup selected with 10-nF (1.1 nF) pulldown(2)
TEST	Open	This pin always has an internal pulldown enabled.

(1) Any unused pin with a secondary function that is shared with general-purpose I/O should follow the Px.0 to Px.7 unused pin connection guidelines.
(2) The pulldown capacitor should not exceed 1.1 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode with TI tools like FET interfaces or GANG programmers.

7.6 Buffer Type

表 7-4 defines the pin buffer types that are listed in 表 7-1.

表 7-4. Buffer Type

BUFFER TYPE (STANDARD)	NOMINAL VOLTAGE	HYSTERESIS	PU OR PD	NOMINAL PU OR PD STRENGTH (µA)	OUTPUT DRIVE STRENGTH (mA)	OTHER CHARACTERISTICS
LVCMOS	3.0 V	Y(1)	Programmable	See セクション 8.12.4	See セクション 8.12.4.3	
Analog	3.0 V	No	No	N/A	N/A	See the analog modules in セクション 8 for details.
Power (DVCC)	3.0 V	No	No	N/A	N/A	SVS enables hysteresis on DVCC.
Power (AVCC)	3.0 V	No	No	N/A	N/A	

(1) Only for input pins

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8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Voltage applied at DVCC pin to V_{SS}	–0.3	4.1	V
Voltage applied to any pin(2)	–0.3	V_{CC} + 0.3 (4.1 V Max)	V
Diode current at any device pin		±2	mA
Maximum junction temperature, T_J		85	°C
Storage temperature range, T_{stg} (3)	–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are referenced to V_{SS}.
(3) Higher temperature may be applied during board soldering according to the current JEDEC J-STD-020 specification with peak reflow temperatures not higher than classified on the device label on the shipping boxes or reels.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±1000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±1000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±250 V may actually have higher performance.

8.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage applied at DVCC pin(1) (2) (3) (4)		1.8		3.6	V
V_{SS}	Supply voltage applied at DVSS pin			0		V
T_A	Operating free-air temperature		–40		85	°C
T_J	Operating junction temperature		–40		85	°C
C_{DVCC}	Recommended capacitor at DVCC(5)		4.7	10		µF
f_{SYSTEM}	Processor frequency (maximum MCLK frequency) (6)	No FRAM wait states (NWAITSx = 0)	0		8	MHz
		With FRAM wait states (NWAITSx = 1)(7)	0		16(8)	
f_{ACLK}	Maximum ACLK frequency				40	kHz
f_{SMCLK}	Maximum SMCLK frequency				16(8)	MHz

(1) Supply voltage changes faster than 0.2 V/µs can trigger a BOR reset even within the recommended supply voltage range. Following the data sheet recommendation for capacitor C_{DVCC} limits the slopes accordingly.
(2) Modules may have a different supply voltage range specification. See the specification of the respective module in this data sheet.
(3) TI recommends that power to the DVCC pin must not exceed the limits specified in *Recommended Operating Conditions*. Exceeding the specified limits can cause malfunction of the device including erroneous writes to RAM and FRAM.
(4) The minimum supply voltage is defined by the SVS levels. See the SVS threshold parameters in セクション 8.12.1.1.
(5) A capacitor tolerance of ±20% or better is required. A low-ESR ceramic capacitor of 100 nF (minimum) should be placed as close as possible (within a few millimeters) to the respective pin pair.
(6) Modules may have a different maximum input clock specification. See the specification of the respective module in this data sheet.
(7) Wait states only occur on actual FRAM accesses (that is, on FRAM cache misses). RAM and peripheral accesses are always executed without wait states.
(8) If clock sources such as HF crystals or the DCO with frequencies >16 MHz are used, the clock must be divided in the clock system to comply with this operating condition.

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8.4 Active Mode Supply Current Into V_{CC} Excluding External Current

V_{CC} = 3.0 V, T_A = 25°C (unless otherwise noted) (1)

PARAMETER	EXECUTION MEMORY	TEST CONDITION	FREQUENCY (f_{MCLK} = f_{SMCLK})						UNIT
			1 MHz 0 WAIT STATES (NWAITSx = 0)		8 MHz 0 WAIT STATES (NWAITSx = 0)		16 MHz 1 WAIT STATE (NWAITSx = 1)		
			TYP	MAX	TYP	MAX	TYP	MAX	
$I_{AM, FRAM (0\%)}$	FRAM 0% cache hit ratio	3.0 V, 25°C	460		2670		2940		µA
		3.0 V, 85°C	475		2730		2980		
$I_{AM, FRAM (100\%)}$	FRAM 100% cache hit ratio	3.0 V, 25°C	191		570		942		µA
		3.0 V, 85°C	199		585		960		
$I_{AM, RAM}$ (2)	RAM	3.0 V, 25°C	213		739		1244		µA

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current. Characterized with program executing typical data processing.
f_{ACLK} = 32768 Hz, f_{MCLK} = f_{SMCLK} = f_{DCO} at specified frequency
Program and data entirely reside in FRAM. All execution is from FRAM.
(2) Program and data reside entirely in RAM. All execution is from RAM. No access to FRAM.

8.5 Active Mode Supply Current Per MHz

V_{CC} = 3.0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	TYP	UNIT
$dI_{AM,FRAM}/df$	Active mode current consumption per MHz, execution from FRAM, no wait states(1)	[(I_{AM} 75% cache hit rate at 8 MHz) – (I_{AM} 75% cache hit rate at 1 MHz)] / 7 MHz	120	µA/MHz

(1) All peripherals are turned on in default settings.

8.6 Low-Power Mode LPM0 Supply Currents Into V_{CC} Excluding External Current

V_{CC} = 3.0 V, T_A = 25°C (unless otherwise noted)(1) (2)

PARAMETER	V_{CC}	FREQUENCY (f_{SMCLK})						UNIT
		1 MHz		8 MHz		16 MHz		
		TYP	MAX	TYP	MAX	TYP	MAX	
I_{LPM0}	2.0 V	148		295		398		µA
	3.0 V	157		304		402		

(1) All inputs are tied to 0 V or to V_{CC}. Outputs do not source or sink any current.
(2) Current for watchdog timer clocked by SMCLK included.
f_{ACLK} = 32768 Hz, f_{MCLK} = 0 MHz, f_{SMCLK} at specified frequency.

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8.7 Low-Power Mode LPM3, LPM4 Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (1) (see 図 8-1)

PARAMETER		V_{CC}	TEMPERATURE						UNIT
			–40°C		25°C		85°C		
			TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM3,XT1}$	Low-power mode 3, includes SVS(2) (3) (4)	3.0 V	0.95		1.07		2.13	6.00	µA
		2.0 V	0.92		1.03		2.09		
$I_{LPM3,VLO}$	Low-power mode 3, VLO, excludes SVS(5)	3.0 V	0.76		0.87		1.94	5.70	µA
		2.0 V	0.74		0.85		1.90		
$I_{LPM3, RTC}$	Low-power mode 3, RTC, excludes SVS(6)	3.0 V	0.88		1.00		2.06		µA
		2.0 V	0.86		0.98		2.02		
$I_{LPM4, SVS}$	Low-power mode 4, includes SVS	3.0 V	0.49		0.58		1.60		µA
		2.0 V	0.46		0.56		1.57		
I_{LPM4}	Low-power mode 4, excludes SVS	3.0 V	0.33		0.42		1.44		µA
		2.0 V	0.32		0.41		1.42		
$I_{LPM4, RTC, VLO}$	Low-power mode 4, RTC is soured from VLO, excludes SVS	3.0 V	0.48		0.59		1.91		µA
		2.0 V	0.48		0.58		1.89		
$I_{LPM4, RTC, XT1}$	Low-power mode 4, RTC is soured from XT1, excludes SVS	3.0 V	0.89		1.04		2.41		µA
		2.0 V	0.88		1.02		2.38		

(1) All inputs are tied to 0 V or to VCC. Outputs do not source or sink any current
(2) Not applicable for devices with HF crystal oscillator only.
(3) Characterized with a Seiko Crystal SC-32S MS1V-T1K crystal with a load capacitance chosen to closely match the required load.
(4) Low-power mode 3, includes SVS test conditions:
Current for watchdog timer clocked by ACLK and RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
f_{XT1} = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(5) Low-power mode 3, VLO, excludes SVS test conditions:
Current for watchdog timer clocked by VLO included. RTC disabled. Current for brownout included. SVS disabled (SVSHE = 0).
CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 0 (LPM3),
f_{XT1} = 32768 Hz, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(6) RTC periodically wakes every second with external 32768-Hz as source.

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8.8 Low-Power Mode LPMx.5 Supply Currents (Into V_{CC}) Excluding External Current

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

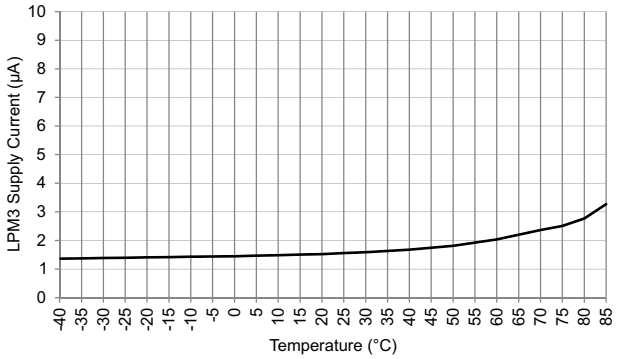
PARAMETER		V_{CC}	TEMPERATURE						UNIT
			–40°C		25°C		85°C		
			TYP	MAX	TYP	MAX	TYP	MAX	
$I_{LPM3.5, XT1}$	Low-power mode 3.5, includes SVS(1) (2) (3) (also see 図 8-2)	3.0 V	0.60		0.66		0.80	2.17	µA
		2.0 V	0.57		0.64		0.75		
$I_{LPM4.5, SVS}$	Low-power mode 4.5, includes SVS(4)	3.0 V	0.23		0.25		0.32	0.43	µA
		2.0 V	0.20		0.23		0.27		
$I_{LPM4.5}$	Low-power mode 4.5, excludes SVS(5) (also see 図 8-3)	3.0 V	0.025		0.034		0.064	0.130	µA
		2.0 V	0.021		0.029		0.055		

(1) Not applicable for devices with HF crystal oscillator only.
(2) Characterized with a Seiko Crystal SC-32S crystal with a load capacitance chosen to closely match the required load.
(3) Low-power mode 3.5, includes SVS test conditions:
Current for RTC clocked by XT1 included. Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
f_{XT1} = 32768 Hz, $f_{ACLK} = f_{XT1}$, $f_{MCLK} = f_{SMCLK}$ = 0 MHz
(4) Low-power mode 4.5, includes SVS test conditions:
Current for brownout and SVS included (SVSHE = 1). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
f_{XT1} = 0 Hz, $f_{ACLK} = f_{MCLK} = f_{SMCLK}$ = 0 MHz
(5) Low-power mode 4.5, excludes SVS test conditions:
Current for brownout included. SVS disabled (SVSHE = 0). Core regulator disabled.
PMMREGOFF = 1, CPUOFF = 1, SCG0 = 1 SCG1 = 1, OSCOFF = 1 (LPMx.5),
f_{XT1} = 0 Hz, $f_{ACLK} = f_{MCLK} = f_{SMCLK}$ = 0 MHz

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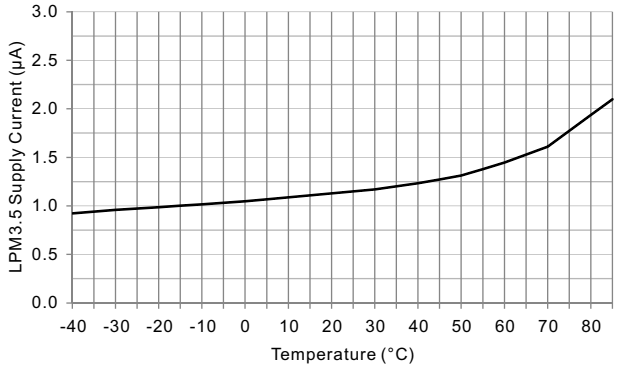
8.9 Typical Characteristics – LPM Supply Currents

3 V at 25°C and 3 V at 85°C



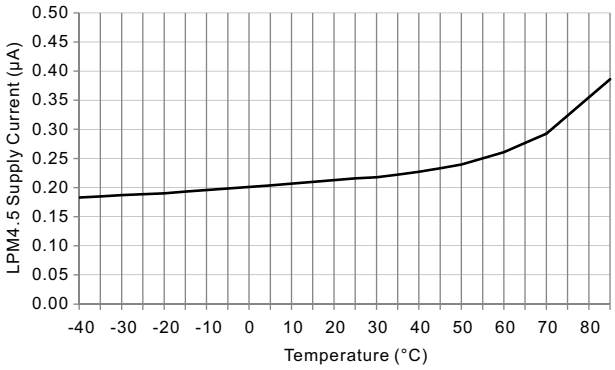
DVCC = 3 V RTC Enabled SVS Disabled

図 8-1. Low-Power Mode 3 Supply Current vs Temperature



DVCC = 3 V XT1, 12.5-pF Crystal SVS Enabled

図 8-2. LPM3.5 Supply Current vs Temperature



DVCC = 3 V SVS Enabled

図 8-3. LPM4.5 Supply Current vs Temperature

8.10 Current Consumption Per Module

MODULE	TEST CONDITIONS	REFERENCE CLOCK	TYP	UNIT
Timer_B	SMCLK = 8 Hz, MC = 10	Module input clock	5	µA/MHz
eUSCI_A	UART mode	Module input clock	7	µA/MHz
eUSCI_A	SPI mode	Module input clock	5	µA/MHz
RTC		32 kHz	85	nA
CRC	From start to end of operation	MCLK	8.5	µA/MHz

8.11 Thermal Resistance Characteristics

THERMAL METRIC(1) (2)			VALUE	UNIT
$R\theta_{JA}$	Junction-to-ambient thermal resistance, still air	VQFN 24 pin (RLL)	38.7	°C/W
		TSSOP 16 pin (PW16)	106.5	
$R\theta_{JC}$	Junction-to-case (top) thermal resistance	VQFN 24 pin (RLL)	39.5	°C/W
		TSSOP 16 pin (PW16)	41.2	
$R\theta_{JB}$	Junction-to-board thermal resistance	VQFN 24 pin (RLL)	8.6	°C/W
		TSSOP 16 pin (PW16)	51.5	

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.
(2) These values are based on a JEDEC-defined 2S2P system (with the exception of the Theta JC [$R\theta_{JC}$] value, which is based on a JEDEC-defined 1S0P system) and will change based on environment and application. For more information, see these EIA/JEDEC standards:

- JESD51-2, *Integrated Circuits Thermal Test Method Environmental Conditions - Natural Convection (Still Air)*
- JESD51-3, *Low Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*
- JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

8.12 Timing and Switching Characteristics

8.12.1 Power Supply Sequencing

図 8-4 shows the power cycle, SVS, and BOR reset conditions.

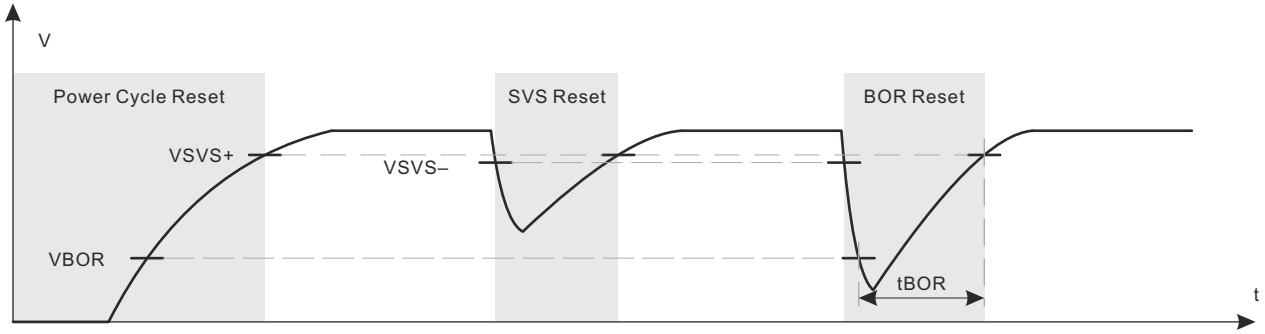


図 8-4. Power Cycle, SVS, and BOR Reset Conditions

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8.12.1.1 PMM, SVS and BOR

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{BOR, safe}$	Safe BOR power-down level(1)		0.1			V
$t_{BOR, safe}$	Safe BOR reset delay(2)		10			ms
$I_{SVSH,AM}$	SVS_H current consumption, active mode	V_{CC} = 3.6 V			1.5	µA
$I_{SVSH,LPM}$	SVS_H current consumption, low-power modes	V_{CC} = 3.6 V		240		nA
V_{SVSH-}	SVS_H power-down level(3)		1.71	1.81	1.86	V
V_{SVSH+}	SVS_H power-up level(3)		1.74	1.88	1.99	V
V_{SVSH_hys}	SVS_H hysteresis			80		mV
$t_{PD,SVSH, AM}$	SVS_H propagation delay, active mode				10	µs
$t_{PD,SVSH, LPM}$	SVS_H propagation delay, low-power modes				100	µs

(1) A safe BOR can be correctly generated only if DVCC drops below this voltage before it rises.
(2) When an BOR occurs, a safe BOR can be correctly generated only if DVCC is kept low longer than this period before it reaches V_{SVSH+}.
(3) For additional information, see the Dynamic Voltage Scaling Power Solution for MSP430 Devices With Single-Channel LDO Reference Design.

8.12.2 Reset Timing

8.12.2.1 Wake-up Times From Low-Power Modes and Reset

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$t_{WAKE-UP\ FRAM}$	(Additional) wake-up time to activate the FRAM in AM if previously disabled through the FRAM controller or from an LPM if immediate activation is selected for wakeup(1)		3 V		10		µs
$t_{WAKE-UP\ LPM0}$	Wake-up time from LPM0 to active mode (1)		3 V			200 + 2.5 / f_{DCO}	ns
$t_{WAKE-UP\ LPM3}$	Wake-up time from LPM3 to active mode (1)		3 V		10		µs
$t_{WAKE-UP\ LPM4}$	Wake-up time from LPM4 to active mode (2)		3 V		10		µs
$t_{WAKE-UP\ LPM3.5}$	Wake-up time from LPM3.5 to active mode (2)		3 V		350		µs
$t_{WAKE-UP\ LPM4.5}$	Wake-up time from LPM4.5 to active mode (2)	SVSHE = 1	3 V		350		µs
		SVSHE = 0			1		ms
$t_{WAKE-UP-RESET}$	Wake-up time from $\overline{RST}$ or BOR event to active mode (2)		3 V		1		ms
t_{RESET}	Pulse duration required at $\overline{RST}$/NMI pin to accept a reset			2			µs

(1) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) to the first externally observable MCLK clock edge.
(2) The wake-up time is measured from the edge of an external wake-up signal (for example, port interrupt or wake-up event) until the first instruction of the user program is executed.

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8.12.3 Clock Specifications

8.12.3.1 XT1 Crystal Oscillator (Low Frequency)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1) (2)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{XT1, LF}$	XT1 oscillator crystal, low frequency	LFXTBYPASS = 0			32768		Hz
$DC_{XT1, LF}$	XT1 oscillator LF duty cycle	Measured at MCLK, f_{LFXT} = 32768 Hz		30%		70%	
$f_{XT1,SW}$	XT1 oscillator logic-level square-wave input frequency	LFXTBYPASS = 1 (3) (4)			32768		Hz
$DC_{XT1, SW}$	LFXT oscillator logic-level square-wave input duty cycle	LFXTBYPASS = 1		40%		60%	
OA_{LFXT}	Oscillation allowance for LF crystals (5)	LFXTBYPASS = 0, LFXTDRIVE = {3}, f_{LFXT} = 32768 Hz, $C_{L,eff}$ = 12.5 pF			200		kΩ
$C_{L,eff}$	Integrated effective load capacitance (6)	See (7)			1		pF
$t_{START,LFXT}$	Start-up time (9)	f_{OSC} = 32768 Hz LFXTBYPASS = 0, LFXTDRIVE = {3}, T_A = 25°C, $C_{L,eff}$ = 12.5 pF			1000		ms
$f_{Fault,LFXT}$	Oscillator fault frequency (10)	XTS = 0(8)		0		3500	Hz

(1) To improve EMI on the LFXT oscillator, observe the following guidelines:
- Keep the trace between the device and the crystal as short as possible.
- Design a good ground plane around the oscillator pins.
- Prevent crosstalk from other clock or data lines into oscillator pins XIN and XOUT.
- Avoid running PCB traces underneath or adjacent to the XIN and XOUT pins.
- Use assembly materials and processes that avoid any parasitic load on the oscillator XIN and XOUT pins.
- If conformal coating is used, make sure that it does not induce capacitive or resistive leakage between the oscillator pins.

(2) See MSP430 32-kHz Crystal Oscillators for details on crystal section, layout, and testing.
(3) When LFXTBYPASS is set, LFXT circuits are automatically powered down. The input signal is a digital square wave with parametrics defined in セクション 8.12.4.1. Duty cycle requirements are defined by $DC_{LFXT, SW}$.
(4) Maximum frequency of operation of the entire device cannot be exceeded.
(5) Oscillation allowance is based on a safety factor of 5 for recommended crystals. The oscillation allowance is a function of the LFXTDRIVE settings and the effective load. In general, comparable oscillator allowance can be achieved based on the following guidelines, but should be evaluated based on the actual crystal selected for the application:
- For LFXTDRIVE = {0}, $C_{L,eff}$ = 3.7 pF
- For LFXTDRIVE = {1}, 6 pF ≤ $C_{L,eff}$ ≤ 9 pF
- For LFXTDRIVE = {2}, 6 pF ≤ $C_{L,eff}$ ≤ 10 pF
- For LFXTDRIVE = {3}, 6 pF ≤ $C_{L,eff}$ ≤ 12 pF

(6) Includes parasitic bond and package capacitance (approximately 2 pF per pin).
(7) Requires external capacitors at both terminals to meet the effective load capacitance specified by crystal manufacturers. Recommended effective load capacitance values supported are 3.7 pF, 6 pF, 9 pF, and 12.5 pF. Maximum shunt capacitance of 1.6 pF. The PCB adds additional capacitance, so it must also be considered in the overall capacitance. Verify that the recommended effective load capacitance of the selected crystal is met.
(8) Measured with logic-level input frequency but also applies to operation with crystals.
(9) Includes start-up counter of 1024 clock cycles.
(10) Frequencies above the MAX specification do not set the fault flag. Frequencies between the MIN and MAX specifications may set the flag. A static condition or stuck at fault condition sets the flag.

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8.12.3.2 DCO FLL, Frequency

over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{DCO, FLL}$	FLL lock frequency, 16 MHz, 25°C	Measured at MCLK, internal trimmed REFO as reference	3.0 V	–1.0%		1.0%	
	FLL lock frequency, 16 MHz, –40°C to 85°C		3.0 V	–2.0%		2.0%	
	FLL lock frequency, 16 MHz, –40°C to 85°C	Measured at MCLK, XT1 crystal as reference	3.0 V	–0.5%		0.5%	
f_{DUTY}	Duty cycle	Measured at MCLK, XT1 crystal as reference	3.0 V	40%	50%	60%	
$Jitter_{cc}$	Cycle-to-cycle jitter, 16 MHz		3.0 V		0.25%		
$Jitter_{long}$	Long term Jitter, 16 MHz		3.0 V		0.022%		
$t_{FLL, lock}$	FLL lock time		3.0 V		245		ms

8.12.3.3 DCO Frequency

over recommended operating free-air temperature (unless otherwise noted) (see 図 8-5)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{DCO, 16 MHz}$ (1)	DCO frequency, 16 MHz	DCORSEL = 101b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 0	3.0 V		7.8		MHz
		DCORSEL = 101b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 511			12.5		
		DCORSEL = 101b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 0			18.0		
		DCORSEL = 101b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 511			30.0		
$f_{DCO, 12 MHz}$ (1)	DCO frequency, 12 MHz	DCORSEL = 100b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 0	3.0 V		6.0		MHz
		DCORSEL = 100b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 511			9.5		
		DCORSEL = 100b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 0			13.5		
		DCORSEL = 100b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 511			22.0		
$f_{DCO, 8 MHz}$ (1)	DCO frequency, 8 MHz	DCORSEL = 011b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 0	3.0 V		3.8		MHz
		DCORSEL = 011b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 511			6.5		
		DCORSEL = 011b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 0			9.5		
		DCORSEL = 011b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 511			16.0		
$f_{DCO, 4 MHz}$ (1)	DCO frequency, 4 MHz	DCORSEL = 010b,, DISMOD = 1b, DCOFTRIM = 000b, DCO = 0	3.0 V		2.0		MHz
		DCORSEL = 010b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 511			3.2		
		DCORSEL = 010b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 0			4.8		
		DCORSEL = 010b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 511			8.0		

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8.12.3.3 DCO Frequency (continued)

over recommended operating free-air temperature (unless otherwise noted) (see 図 8-5)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
$f_{DCO, 2\ MHz}$ (1)	DCO frequency, 2 MHz	DCORSEL = 001b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 0	3.0 V		1.0		MHz
		DCORSEL = 001b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 511			1.7		
		DCORSEL = 001b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 0			2.5		
		DCORSEL = 001b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 511			4.2		
$f_{DCO, 1\ MHz}$ (1)	DCO frequency, 1 MHz	DCORSEL = 000b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 0	3.0 V		0.5		MHz
		DCORSEL = 000b, DISMOD = 1b, DCOFTRIM = 000b, DCO = 511			0.85		
		DCORSEL = 000b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 0			1.2		
		DCORSEL = 000b, DISMOD = 1b, DCOFTRIM = 111b, DCO = 511			2.1		

(1) This frequency reflects the achievable frequency range when FLL is either enabled or disabled.

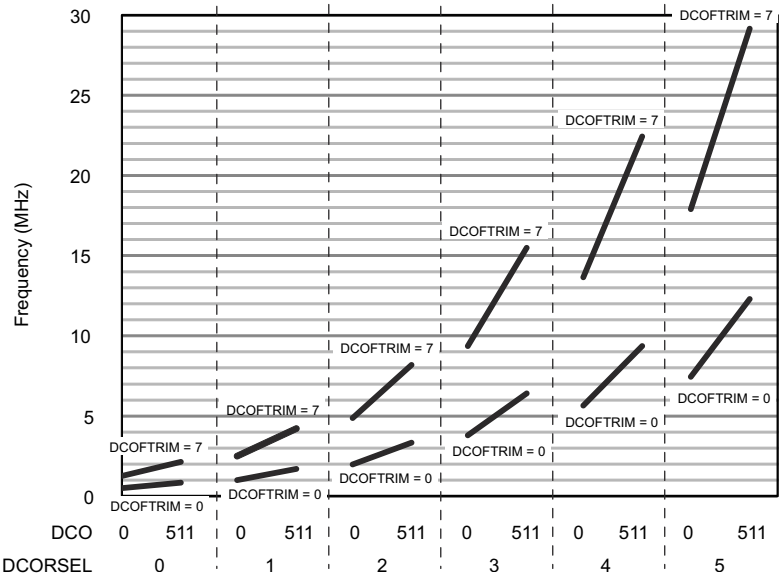


図 8-5. Typical DCO Frequency

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8.12.3.4 REFO

over recommended operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{REFO}	REFO oscillator current consumption	T_A = 25°C	3.0 V		15		µA
f_{REFO}	REFO calibrated frequency	Measured at MCLK	3.0 V		32768		Hz
	REFO absolute calibrated tolerance	–40°C to 85°C	1.8 V to 3.6 V	–3.5%		+3.5%	
df_{REFO}/d_T	REFO frequency temperature drift	Measured at MCLK(1)	3.0 V		0.01		%/°C
df_{REFO}/d_{VCC}	REFO frequency supply voltage drift	Measured at MCLK at 25°C(2)	1.8 V to 3.6 V		1		%/V
f_{DC}	REFO duty cycle	Measured at MCLK	1.8V to 3.6 V	40%	50%	60%	
t_{START}	REFO start-up time	40% to 60% duty cycle			50		µs

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

8.12.3.5 Internal Very-Low-Power Low-Frequency Oscillator (VLO)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{VLO}	VLO frequency	Measured at MCLK	3.0 V		10		kHz
df_{VLO}/d_T	VLO frequency temperature drift	Measured at MCLK(1)	3.0 V		0.5		%/°C
df_{VLO}/dV_{CC}	VLO frequency supply voltage drift	Measured at MCLK(2)	1.8 V to 3.6 V		4		%/V
f	Duty cycle	Measured at MCLK	3.0 V		50%		

(1) Calculated using the box method: (MAX(–40°C to 85°C) – MIN(–40°C to 85°C)) / MIN(–40°C to 85°C) / (85°C – (–40°C))
(2) Calculated using the box method: (MAX(1.8 V to 3.6 V) – MIN(1.8 V to 3.6 V)) / MIN(1.8 V to 3.6 V) / (3.6 V – 1.8 V)

注

The VLO clock frequency is reduced by 15% (typical) when the device switches from active mode to LPM3 or LPM4, because the reference changes. This lower frequency is not a violation of the VLO specifications (see セクション 8.12.3.5).

8.12.3.6 Module Oscillator (MODOSC)

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{MODOSC}	MODOSC frequency	3.0 V	3.8	4.8	5.8	MHz
f_{MODOSC}/dT	MODOSC frequency temperature drift	3.0 V		0.102		%/°C
f_{MODOSC}/dV_{CC}	MODOSC frequency supply voltage drift	1.8 V to 3.6 V		2.29		%/V
$f_{MODOSC,DC}$	Duty cycle	3.0 V	40%	50%	60%	

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8.12.4 Digital I/Os

8.12.4.1 Digital Inputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage		2 V	0.90		1.50	V
			3 V	1.35		2.25	
V_{IT-}	Negative-going input threshold voltage		2 V	0.50		1.10	V
			3 V	0.75		1.65	
V_{hys}	Input voltage hysteresis ($V_{IT+} – V_{IT-}$)		2 V	0.3		0.8	V
			3 V	0.4		1.2	
R_{Pull}	Pullup or pulldown resistor	For pullup: $V_{IN} = V_{SS}$ For pulldown: $V_{IN} = V_{CC}$		20	35	50	kΩ
$C_{I,dig}$	Input capacitance, digital only port pins	$V_{IN} = V_{SS}$ or V_{CC}			3		pF
$C_{I,ana}$	Input capacitance, port pins with shared analog functions	$V_{IN} = V_{SS}$ or V_{CC}			5		pF
$I_{lkg(Px.y)}$	High-impedance leakage current(1) (2)		2 V, 3 V	–20		+20	nA
$t_{(int)}$	External interrupt timing (external trigger pulse duration to set interrupt flag)(3)	Ports with interrupt capability (see block diagram and terminal function descriptions)	2 V, 3 V	50			ns

(1) The leakage current is measured with V_{SS} or V_{CC} applied to the corresponding pins, unless otherwise noted.
(2) The leakage of the digital port pins is measured individually. The port pin is selected for input and the pullup/pulldown resistor is disabled.
(3) An external signal sets the interrupt flag every time the minimum interrupt pulse duration $t_{(int)}$ is met. It may be set by trigger signals shorter than $t_{(int)}$.

8.12.4.2 Digital Outputs

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{OH}	High-level output voltage (also see 図 8-8 and 図 8-9)	$I_{(OHmax)}$ = –3 mA(1)	2.0 V	1.4		2.0	V
		$I_{(OHmax)}$ = –5 mA(1)	3.0 V	2.4		3.0	
V_{OL}	Low-level output voltage (also see 図 8-6 and 図 8-7)	$I_{(OLmax)}$ = 3 mA(1)	2.0 V	0.0		0.60	V
		$I_{(OLmax)}$ = 5 mA(1)	3.0 V	0.0		0.60	
f_{Port_CLK}	Clock output frequency	C_L = 20 pF(2)	2.0 V	16			MHz
			3.0 V	16			
$t_{rise,dig}$	Port output rise time, digital only port pins	C_L = 20 pF	2.0 V		10		ns
			3.0 V		7		
$t_{fall,dig}$	Port output fall time, digital only port pins	C_L = 20 pF	2.0 V		10		ns
			3.0 V		5		

(1) The maximum total current, $I_{(OHmax)}$ and $I_{(OLmax)}$, for all outputs combined should not exceed ±48 mA to hold the maximum voltage drop specified.
(2) The port can output frequencies at least up to the specified limit and might support higher frequencies.

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8.12.4.3 Digital I/O Typical Characteristics

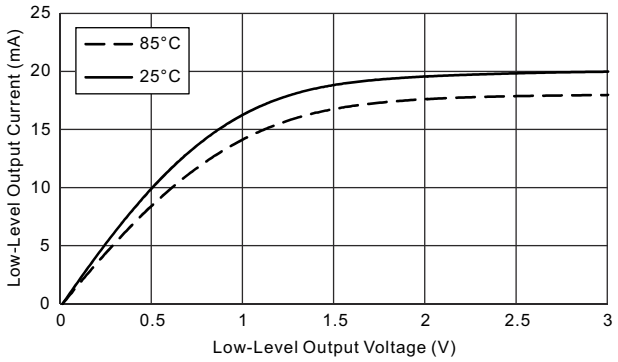


図 8-6. Typical Low-Level Output Current vs Low-Level Output Voltage (DVCC = 3 V)

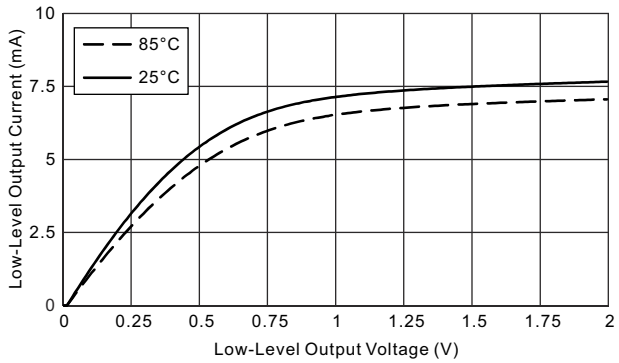


図 8-7. Typical Low-Level Output Current vs Low-Level Output Voltage (DVCC = 2 V)

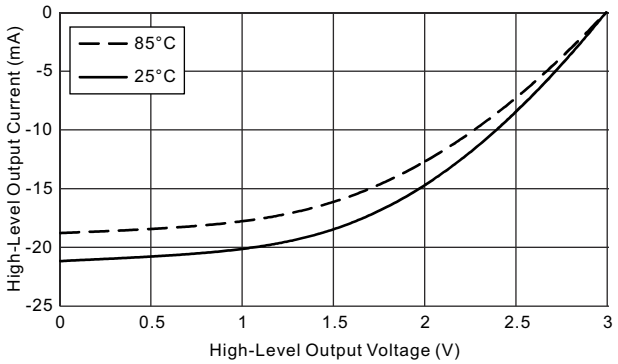


図 8-8. Typical High-Level Output Current vs High-Level Output Voltage (DVCC = 3 V)

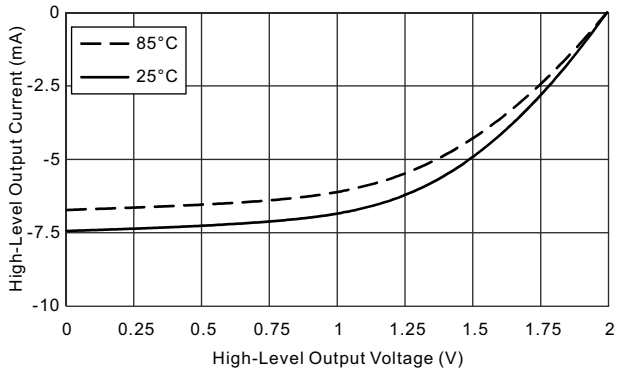


図 8-9. Typical High-Level Output Current vs High-Level Output Voltage (DVCC = 2 V)

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8.12.5 VREF+ Built-in Reference

注

The 1.2-V reference that is available for external use is specified below. The 1.5-V reference is available only for internal use by analog modules. Therefore, the accuracy of the 1.5-V reference is included in the ADC specifications.

8.12.5.1 VREF+ Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{REF+}	Positive built-in reference voltage	EXTREFEN = 1 with 1-mA load current	2.0 V, 3.0 V	1.158	1.2	1.242	V
TC_{REF+}	Temperature coefficient of built-in reference voltage	EXTREFEN = 1 with 1-mA load current			30		µV/°C

8.12.6 Timer_B

8.12.6.1 Timer_B

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{TB}	Timer_B input clock frequency	Internal: SMCLK or ACLK, External: TBCLK, duty cycle = 50% ±10%	2.0 V, 3.0 V		16	MHz
$t_{TB,cap}$	Timer_B capture timing	All capture inputs, minimum pulse duration required for capture	2.0 V, 3.0 V	20		ns

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8.12.7 eUSCI

8.12.7.1 eUSCI (UART Mode) Clock Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK or MODCLK, External: UCLK, duty cycle = 50% ±10%	2.0 V, 3.0 V		16	MHz
f_{BITCLK}	BITCLK clock frequency (equals baud rate in Mbaud)		2.0 V, 3.0 V		5	MHz

8.12.7.2 eUSCI (UART Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
t_t	UART receive deglitch time (1)	UCGLITx = 0	2.0 V, 3.0 V		12		ns
		UCGLITx = 1			40		
		UCGLITx = 2			68		
		UCGLITx = 3			110		

(1) Pulses on the UART receive input (UCxRX) shorter than the UART receive deglitch time are suppressed. To ensure that pulses are correctly recognized their width should exceed the maximum specification of the deglitch time.

8.12.7.3 eUSCI (SPI Master Mode) Clock Frequency

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
f_{eUSCI}	eUSCI input clock frequency	Internal: SMCLK or MODCLK, duty cycle = 50% ±10%		8	MHz

8.12.7.4 eUSCI (SPI Master Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock	UCSTEM = 1, UCMODEx = 01 or 10	3.0 V	1		UCxCLK cycles
$t_{STE,LAG}$	STE lag time, Last clock to STE inactive	UCSTEM = 1, UCMODEx = 01 or 10	3.0 V	1		UCxCLK cycles
$t_{SU,MI}$	SOMI input data setup time		2.0 V	53		ns
			3.0 V	35		
$t_{HD,MI}$	SOMI input data hold time		2.0 V	0		ns
			3.0 V	0		
$t_{VALID,MO}$	SIMO output data valid time(2)	UCLK edge to SIMO valid, C_L = 20 pF	2.0 V		20	ns
			3.0 V		20	
$t_{HD,MO}$	SIMO output data hold time(3)	C_L = 20 pF	2.0 V	0		ns
			3.0 V	0		

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} = \max(t_{VALID,MO(eUSCI)} + t_{SU,SI(Slave)}, t_{SU,MI(eUSCI)} + t_{VALID,SO(Slave)})$
For the slave parameters $t_{SU,SI(Slave)}$ and $t_{VALID,SO(Slave)}$, see the SPI parameters of the attached slave.
(2) Specifies the time to drive the next valid data to the SIMO output after the output changing UCLK clock edge. See the timing diagrams in 図 8-10 and 図 8-11.
(3) Specifies how long data on the SIMO output is valid after the output changing UCLK clock edge. Negative values indicate that the data on the SIMO output can become invalid before the output changing clock edge observed on UCLK. See the timing diagrams in 図 8-10 and 図 8-11.

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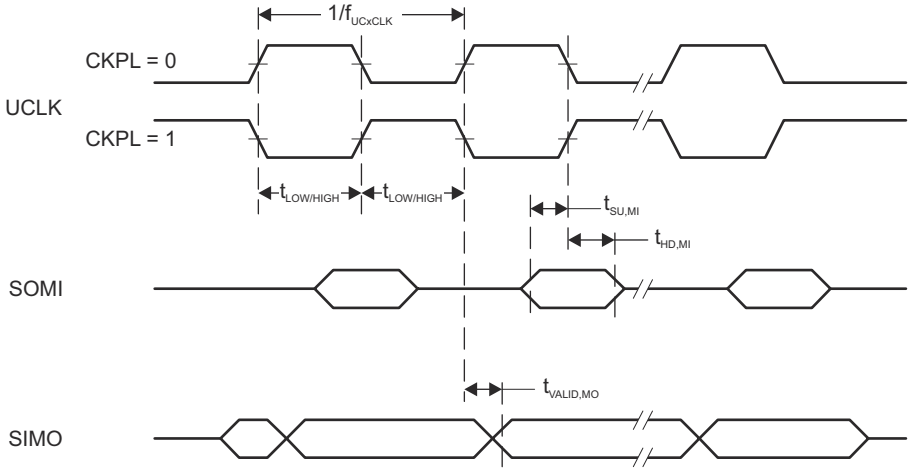


図 8-10. SPI Master Mode, CKPH = 0

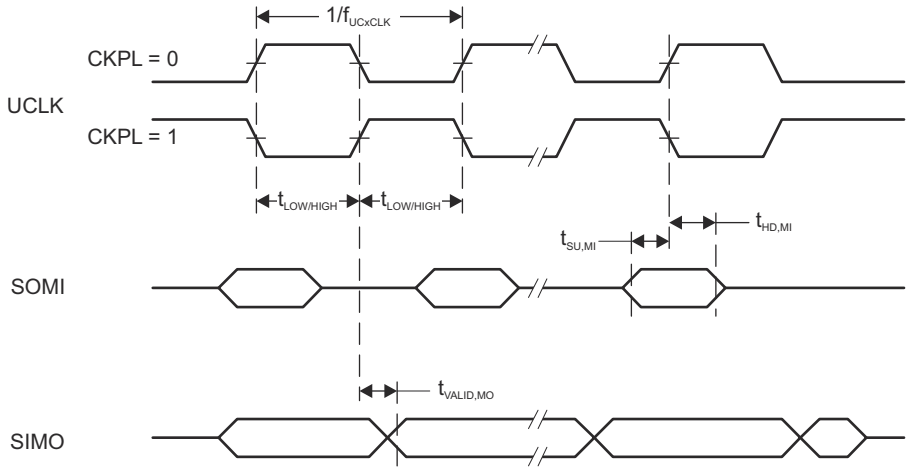


図 8-11. SPI Master Mode, CKPH = 1

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8.12.7.5 eUSCI (SPI Slave Mode) Switching Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)(1)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	MAX	UNIT
$t_{STE,LEAD}$	STE lead time, STE active to clock		2.0 V	55		ns
			3.0 V	45		
$t_{STE,LAG}$	STE lag time, last clock to STE inactive		2.0 V	20		ns
			3.0 V	20		
$t_{STE,ACC}$	STE access time, STE active to SOMI data out		2.0 V		65	ns
			3.0 V		40	
$t_{STE,DIS}$	STE disable time, STE inactive to SOMI high impedance		2.0 V		50	ns
			3.0 V		35	
$t_{SU,SI}$	SIMO input data setup time		2.0 V	10		ns
			3.0 V	8		
$t_{HD,SI}$	SIMO input data hold time		2.0 V	12		ns
			3.0 V	12		
$t_{VALID,SO}$	SOMI output data valid time(2)	UCLK edge to SOMI valid, C_L = 20 pF	2.0 V		68	ns
			3.0 V		42	
$t_{HD,SO}$	SOMI output data hold time (3)	C_L = 20 pF	2.0 V	5		ns
			3.0 V	5		

(1) $f_{UCxCLK} = 1/2t_{LO/HI}$ with $t_{LO/HI} \geq \max(t_{VALID,MO(Master)} + t_{SU,SI(eUSCI)}, t_{SU,MI(Master)} + t_{VALID,SO(eUSCI)})$
For the master parameters $t_{SU,MI(Master)}$ and $t_{VALID,MO(Master)}$, see the SPI parameters of the attached master.

(2) Specifies the time to drive the next valid data to the SOMI output after the output changing UCLK clock edge. See the timing diagrams in 図 8-12 and 図 8-13.

(3) Specifies how long data on the SOMI output is valid after the output changing UCLK clock edge. See the timing diagrams in 図 8-12 and 図 8-13.

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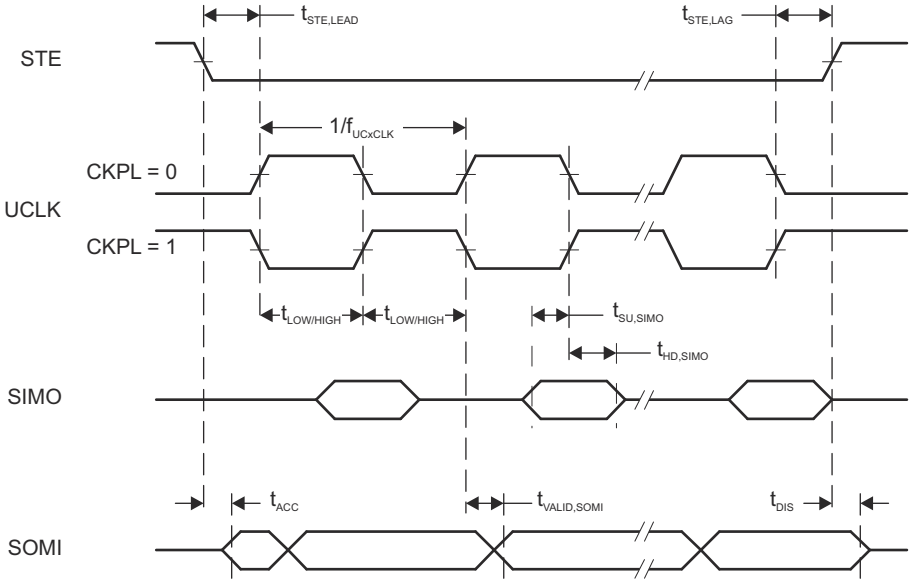


図 8-12. SPI Slave Mode, CKPH = 0

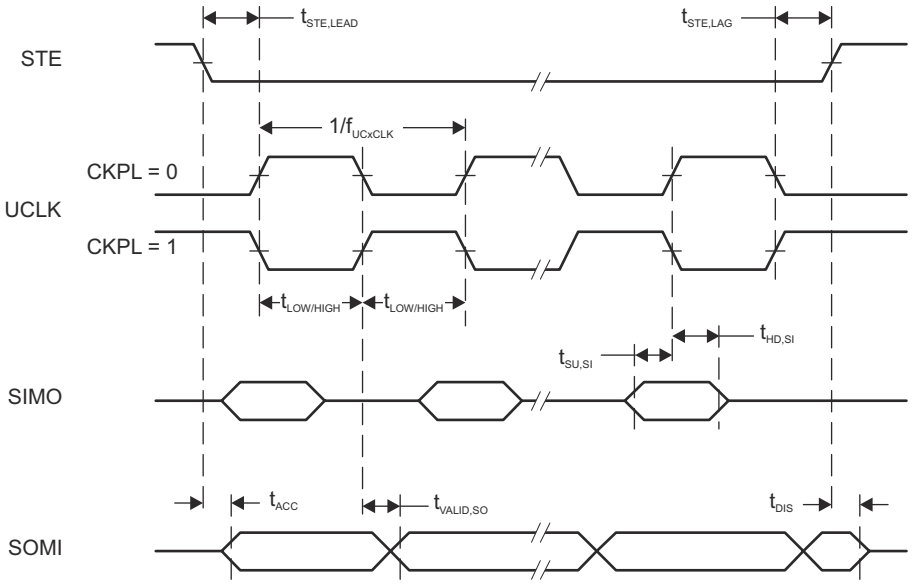


図 8-13. SPI Slave Mode, CKPH = 1

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8.12.8 ADC

注

The ADC is not available on the MSP430FR2000 device.

8.12.8.1 ADC, Power Supply and Input Range Conditions

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
DV_{CC}	ADC supply voltage			2.0		3.6	V
$V_{(Ax)}$	Analog input voltage range	All ADC pins		0		DV_{CC}	V
I_{ADC}	Operating supply current into DVCC terminal, reference current not included, repeat-single-channel mode	f_{ADCCLK} = 5 MHz, ADCON = 1, REFON = 0, SHT0 = 0, SHT1 = 0, ADCDIV = 0, ADCCONSEQx = 10b	2 V		185		µA
			3 V		207		
C_I	Input capacitance	Only one terminal Ax can be selected at one time from the pad to the ADC capacitor array, including wiring and pad	2.2 V		2.5	3.5	pF
$R_{I,MUX}$	Input MUX ON resistance	DV_{CC} = 2 V, 0 V ≤ V_{Ax} ≤ DV_{CC}				2	kΩ
$R_{I,Misc}$	Input miscellaneous resistance				34		kΩ

8.12.8.2 ADC, 10-Bit Timing Parameters

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
f_{ADCCLK}		For specified performance of ADC linearity parameters	2 V to 3.6 V	0.45	5	5.5	MHz
f_{ADCOSC}	Internal ADC oscillator (MODOSC)	ADCDIV = 0, f_{ADCCLK} = f_{ADCOSC}	2 V to 3.6 V	3.8	4.8	5.8	MHz
$t_{CONVERT}$	Conversion time	REFON = 0, Internal oscillator, 10 ADCCLK cycles, 10-bit mode, f_{ADCOSC} = 4.5 MHz to 5.5 MHz	2 V to 3.6 V	2.18		2.67	µs
		External f_{ADCCLK} from ACLK, MCLK or SMCLK, ADCSSEL ≠ 0	2V to 3.6V		12 × 1 / f_{ADCCLK}		
t_{ADCON}	Turn-on settling time of the ADC	The error in a conversion started after t_{ADCON} is less than ±0.5 LSB. Reference and input signal are already settled.				100	ns
t_{Sample}	Sampling time	R_S = 1000 Ω, R_I (1) = 36000 Ω, C_I = 3.5 pF, Approximately 8 Tau (t) are required for an error of less than ±0.5 LSB(2)	2 V	1.5			µs
			3 V	2.0			

(1) $R_I = R_{I,MUX} + R_{I,Misc}$
(2) $t_{Sample} = \ln(2^{n+1}) \times \tau$, where n = ADC resolution, $\tau = (R_I + R_S) \times C_I$

8.12.8.3 ADC, 10-Bit Linearity Parameters

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
E_I	Integral linearity error (10-bit mode)	Veref+ reference	2.4 V to 3.6 V	–2		2	LSB
	Integral linearity error (8-bit mode)		2.0 V to 3.6 V	–2		2	
E_D	Differential linearity error (10-bit mode)	Veref+ reference	2.4 V to 3.6 V	–1		1	LSB
	Differential linearity error (8-bit mode)		2.0 V to 3.6 V	–1		1	
E_O	Offset error (10-bit mode)	Veref+ reference	2.4 V to 3.6 V	–6.5		6.5	mV
	Offset error (8-bit mode)		2.0 V to 3.6 V	–6.5		6.5	
E_G	Gain error (10-bit mode)	Veref+ as reference	2.4 V to 3.6 V	–2.0		2.0	LSB
		Internal 1.5-V reference		–3.0%		3.0%	
	Gain error (8-bit mode)	Veref+ as reference	2.0 V to 3.6 V	–2.0		2.0	LSB
		Internal 1.5-V reference		–3.0%		3.0%	
E_T	Total unadjusted error (10-bit mode)	Veref+ as reference	2.4 V to 3.6 V	–2.0		2.0	LSB
		Internal 1.5-V reference		–3.0%		3.0%	
	Total unadjusted error (8-bit mode)	Veref+ as reference	2.0 V to 3.6 V	–2.0		2.0	LSB
		Internal 1.5-V reference		–3.0%		3.0%	
V_{SENSOR}	See (1)	ADCON = 1, INCH = 0Ch, T_A = 0°C	3.0 V		913		mV
TC_{SENSOR}	See (2)	ADCON = 1, INCH = 0Ch	3.0 V		3.35		mV/°C
t_{SENSOR} (sample)	Sample time required if channel 12 is selected	ADCON = 1, INCH = 0Ch, Error of conversion result ≤1 LSB, AM and all LPMs above LPM3	3.0 V	30			µs
		ADCON = 1, INCH = 0Ch, Error of conversion result ≤1 LSB, LPM3	3.0 V	100			

(1) The temperature sensor offset can vary significantly. TI recommends a single-point calibration to minimize the offset error of the built-in temperature sensor.

(2) The device descriptor structure contains calibration values for 30°C and 85°C for each available reference voltage level. The sensor voltage can be computed as $V_{SENSE} = TC_{SENSOR} \times (\text{Temperature, °C}) + V_{SENSOR}$, where TC_{SENSOR} and V_{SENSOR} can be computed from the calibration values for higher accuracy.

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8.12.9 Enhanced Comparator (eCOMP)

8.12.9.1 eCOMP Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
V_{CC}	Supply voltage			2.0		3.6	V
V_{IC}	Common-mode input range			0		VCC	V
V_{HYS}	DC input hysteresis	CPEN = 1, CPHSEL = 00	2.0 V to 3.6 V		0		mV
		CPEN = 1, CPHSEL = 01			10		
		CPEN = 1, CPHSEL = 10			20		
		CPEN = 1, CPHSEL = 11			30		
V_{OFFSET}	Input offset voltage	CPEN = 1, CPMSEL = 0, CPHSEL = 00	2.0 V to 3.6 V	-40	±5	+40	mV
		CPEN = 1, CPMSEL = 1, CPHSEL = 00			±10		
I_{COMP}	Quiescent current draw from VCC, only comparator	V_{IC} = V_{CC}/2, CPEN = 1, CPMSEL = 0	2.0 V to 3.6 V		22	35	µA
		V_{IC} = V_{CC}/2, CPEN = 1, CPMSEL = 1			1.3	3.5	
I_{DAC}	Quiescent current draw from VCC, only DAC	CPDACREFS = 0, CPEN = 0	2.0 V to 3.6 V		0.5		µA
C_{IN}	Input channel capacitance(1)		2.0 V to 3.6 V		1		pF
R_{IN}	Input channel series resistance	On (switch closed)	2.0 V to 3.6 V		10	20	kΩ
		Off (switch open)		50			MΩ
t_{PD}	Propagation delay, response time	CPMSEL = 0, CPFLT = 0, Overdrive = 20 mV(2)	2.0 V to 3.6 V			1	µs
		CPMSEL = 1, CPFLT = 0, Overdrive = 20 mV(2)			2.4		
t_{EN_CP}	Comparator enable time	CPEN = 0→1, CPMSEL = 0, V+ and V- from pads, Overdrive = 20 mV(2)	2.0 V to 3.6 V		9.3		µs
		CPEN = 0→1, CPMSEL = 1, V+ and V- from pads, Overdrive = 20 mV(2)			12		
$t_{EN_CP_DAC}$	Comparator with reference DAC enable time	CPEN = 0→1, CPDACEN=0→1, CPMSEL = 0, CPDACREFS = 1, CPDACBUF1 = 0F, Overdrive = 20 mV(2)	2.0 V to 3.6 V		9.3		µs
		CPEN = 0→1, CPDACEN=0→1, CPMSEL = 1, CPDACREFS = 1, CPDACBUF1 = 0F, Overdrive = 20 mV (2)			113		
t_{FDLY}	Propagation delay with analog filter active	CPMSEL = 0, CPFLTDY = 00, Overdrive = 20 mV,(2) CPFLT = 1	2.0 V to 3.6 V		0.7		µs
		CPMSEL = 0, CPFLTDY = 01, Overdrive = 20 mV,(2) CPFLT = 1			1.1		
		CPMSEL = 0, CPFLTDY = 10, Overdrive = 20 mV,(2) CPFLT = 1			1.9		
		CPMSEL = 0, CPFLTDY = 11, Overdrive = 20 mV,(2) CPFLT = 1			3.7		
V_{CP_DAC}	Reference voltage for built-in 6-bit DAC	VIN = reference into 6-bit DAC, DAC uses internal REF, n = 0 to 63	2.0 V to 3.6 V		VIN × n / 64		V
		VIN = reference into 6-bit DAC, DAC uses VCC as REF, n = 0 to 63			VIN × n / 64		
INL	Integral nonlinearity		2.0 V to 3.6 V	–0.5		+0.5	LSB
DNL	Differential nonlinearity		2.0 V to 3.6 V	–0.5		+0.5	LSB
	Zero scale		2.0 V to 3.6 V		0		LSB

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8.12.9.1 eCOMP Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	V_{CC}	MIN	TYP	MAX	UNIT
I_{DACOFF}	Leakage current		2.0 V to 3.6 V		5		nA

(1) For the eCOMP C_{IN} model, see 図 8-14.
(2) This is measured over the input offset.

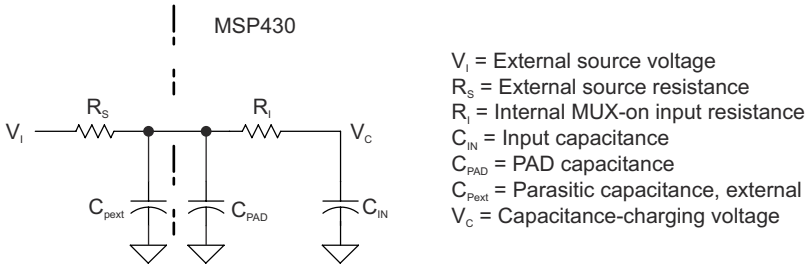


図 8-14. eCOMP Input Circuit

8.12.10 FRAM

8.12.10.1 FRAM Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Read and write endurance		10^{15}			cycles
$t_{Retention}$	Data retention duration	T_J = 25°C	100			years
		T_J= 70°C	40			
		T_J= 85°C	10			
I_{WRITE}	Current to write into FRAM			I_{READ} (1)		nA
I_{ERASE}	Erase current			n/a(2)		
t_{WRITE}	Write time			t_{READ} (3)		ns
I_{READ}	Read time, NWAITSx = 0			1 / f_{SYSTEM} (4)		ns
	Read time, NWAITSx = 1			2 / f_{SYSTEM} (4)		ns

(1) Writing to FRAM does not require a setup sequence or additional power when compared to reading from FRAM. The FRAM read current I_{READ} is included in the active mode current consumption $I_{AM, FRAM}$.
(2) n/a = not applicable. FRAM does not require a special erase sequence.
(3) Writing to FRAM is as fast as reading.
(4) The maximum read (and write) speed is specified by f_{SYSTEM} using the appropriate wait state settings (NWAITSx).

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8.12.11 Emulation and Debug

8.12.11.1 JTAG, Spy-Bi-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 図 8-15)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{SBW}	Spy-Bi-Wire input frequency	2.0 V, 3.0 V	0		8	MHz
$t_{SBW,Low}$	Spy-Bi-Wire low clock pulse duration	2.0 V, 3.0 V	0.028		15	µs
$t_{SU,SBWTDIO}$	SBWTDIO setup time (before falling edge of SBWTCK in TMS and TDI slot Spy-Bi-Wire)	2.0 V, 3.0 V	4			ns
$t_{HD,SBWTDIO}$	SBWTDIO hold time (after rising edge of SBWTCK in TMS and TDI slot Spy-Bi-Wire)	2.0 V, 3.0 V	19			ns
$t_{Valid,SBWTDIO}$	SBWTDIO data valid time (after falling edge of SBWTCK in TDO slot Spy-Bi-Wire)	2.0 V, 3.0 V			31	ns
$t_{SBW,En}$	Spy-Bi-Wire enable time (TEST high to acceptance of first clock edge) (1)	2.0 V, 3.0 V			110	µs
$t_{SBW,Ret}$	Spy-Bi-Wire return to normal operation time(2)	2.0 V, 3.0 V	15		100	µs

(1) Tools that access the Spy-Bi-Wire interface must wait for the $t_{SBW,En}$ time after pulling the TEST/SBWTCK pin high before applying the first SBWTCK clock edge.

(2) Maximum $t_{SBW,Rst}$ time after pulling or releasing the TEST/SBWTCK pin low, the Spy-Bi-Wire pins revert from their Spy-Bi-Wire function to their application function. This time applies only if the Spy-Bi-Wire mode was selected.

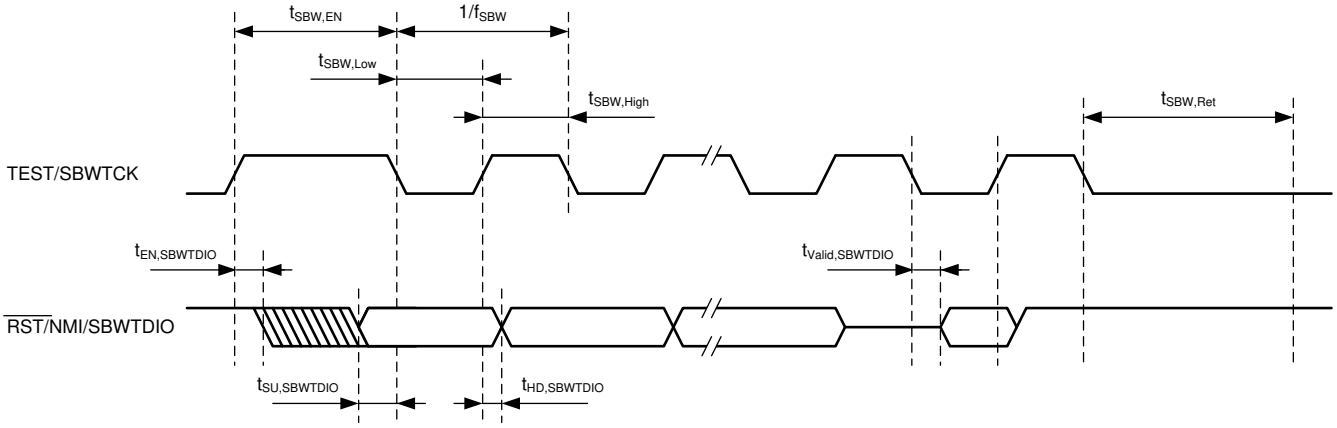


図 8-15. JTAG Spy-Bi-Wire Timing

8.12.11.2 JTAG, 4-Wire Interface

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see 図 8-16)

PARAMETER		V_{CC}	MIN	TYP	MAX	UNIT
f_{TCK}	TCK input frequency(1)	2.0 V, 3.0 V	0		10	MHz
$t_{TCK,Low}$	TCK low clock pulse duration	2.0 V, 3.0 V	15			ns
$t_{TCK,high}$	TCK high clock pulse duration	2.0 V, 3.0 V	15			ns
$t_{SU,TMS}$	TMS setup time (before rising edge of TCK)	2.0 V, 3.0 V	11			ns
$t_{HD,TMS}$	TMS hold time (after rising edge of TCK)	2.0 V, 3.0 V	3			ns
$t_{SU,TDI}$	TDI setup time (before rising edge of TCK)	2.0 V, 3.0 V	13			ns
$t_{HD,TDI}$	TDI hold time (after rising edge of TCK)	2.0 V, 3.0 V	5			ns
$t_{z\text{-}Valid,TDO}$	TDO high impedance to valid output time (after falling edge of TCK)	2.0 V, 3.0 V			26	ns
$t_{Valid,TDO}$	TDO to new valid output time (after falling edge of TCK)	2.0 V, 3.0 V			26	ns
$t_{Valid\text{-}Z,TDO}$	TDO valid to high-impedance output time (after falling edge of TCK)	2.0 V, 3.0 V			26	ns
$t_{JTAG,Ret}$	JTAG return to normal operation time		15		100	µs
$R_{internal}$	Internal pulldown resistance on TEST	2.0 V, 3.0 V	20	35	50	kΩ

(1) f_{TCK} may be restricted to meet the timing requirements of the module selected.

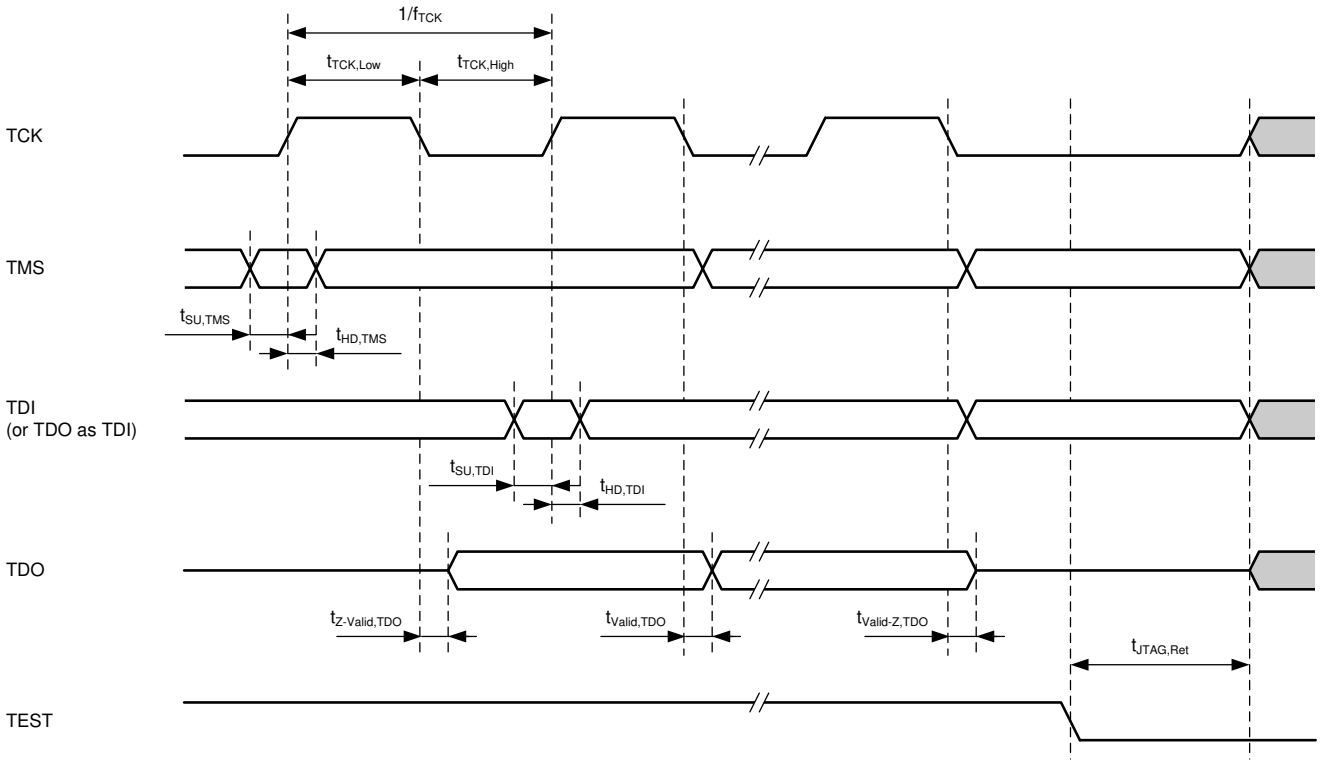


図 8-16. JTAG 4-Wire Timing

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9 Detailed Description

9.1 Overview

The Texas Instruments MSP430FR211x family of ultra-low-power microcontrollers consists of several devices featuring different sets of peripherals. The architecture, combined with five low-power modes, is optimized to achieve extended battery life (for example, in portable measurement applications). The devices feature a powerful 16-bit RISC CPU, 16-bit register, and constant generators that contribute to maximum code efficiency.

The MSP430FR211x devices are microcontroller configurations with one Timer_B, eCOMP with built-in 6-bit DAC as an internal reference voltage, a high-performance 10-bit ADC, an eUSCI that supports UART and SPI, an RTC module with alarm capabilities, and up to 12 I/O pins.

9.2 CPU

The MSP430 CPU has a 16-bit RISC architecture that is highly transparent to the application. All operations, other than program-flow instructions, are performed as register operations in conjunction with seven addressing modes for source operand and four addressing modes for destination operand.

The CPU is integrated with 16 registers that provide reduced instruction execution time. The register-to-register operation execution time is one cycle of the CPU clock.

Four of the registers, R0 to R3, are dedicated as program counter (PC), stack pointer (SP), status register (SR), and constant generator (CG), respectively. The remaining registers are general-purpose registers.

Peripherals are connected to the CPU using data, address, and control buses. Peripherals can be managed with all instructions.

9.3 Operating Modes

The MSP430 has one active mode and several software selectable low-power modes of operation (see 表 9-1). An interrupt event can wake up the device from low-power mode LPM0, LPM3 or LPM4, service the request, and restore back to the low-power mode on return from the interrupt program. Low-power modes LPM3.5 and LPM4.5 disable the core supply to minimize power consumption.

注

XT1CLK and VLOCLK can be active during LPM4 if requested by low-frequency peripherals.

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表 9-1. Operating Modes

MODE		AM	LPM0	LPM3	LPM4	LPM3.5	LPM4.5
		ACTIVE MODE	CPU OFF	STANDBY	OFF	ONLY RTC COUNTER	SHUTDOWN
Maximum system clock		16 MHz	16 MHz	40 kHz	0	40 kHz	0
Power consumption at 25°C, 3 V		120 µA/MHz	40 µA/MHz	1.5 µA	0.42 µA without SVS	0.66 µA	34 nA without SVS
Wake-up time		N/A	instant	10 µs	10 µs	150 µs	150 µs
Wake-up events		N/A	All	All	I/O	RTC Counter I/O	I/O
Power	Regulator	Full Regulation	Full Regulation	Partial Power Down	Partial Power Down	Partial Power Down	Power Down
	SVS	On	On	Optional	Optional	Optional	Optional
	Brownout	On	On	On	On	On	On
Clock[2]	MCLK	Active	Off	Off	Off	Off	Off
	SMCLK	Optional	Optional	Off	Off	Off	Off
	FLL	Optional	Optional	Off	Off	Off	Off
	DCO	Optional	Optional	Off	Off	Off	Off
	MODCLK	Optional	Optional	Off	Off	Off	Off
	REFO	Optional	Optional	Optional	Off	Off	Off
	ACLK	Optional	Optional	Optional	Off	Off	Off
	XT1LFCLK	Optional	Optional	Optional	Off	Optional	Off
	VLOCLK	Optional	Optional	Optional	Off	Optional	Off
Core	CPU	On	Off	Off	Off	Off	Off
	FRAM	On	On	Off	Off	Off	Off
	RAM	On	On	On	On	Off	Off
	Backup Memory[1]	On	On	On	On	On	Off
Peripherals	Timer_B3	Optional	Optional	Optional	Off	Off	Off
	WDT	Optional	Optional	Optional	Off	Off	Off
	eUSCI_A	Optional	Optional	Optional	Off	Off	Off
	CRC	Optional	Optional	Off	Off	Off	Off
	ADC[3]	Optional	Optional	Optional	Off	Off	Off
	eCOMP	Optional	Optional	Optional	Optional	Off	Off
	RTC Counter	Optional	Optional	Optional	Off	Optional	Off
I/O	General Digital Input/Output	On	Optional	State Held	State Held	State Held	State Held
	Capacitive Touch I/O	Optional	Optional	Optional	Off	Off	Off

(1) Backup memory contains 32 bytes of register space in the peripheral memory. See 表 9-18 and 表 9-31 for its memory allocation.
(2) The status shown for LPM4 applies to internal clocks only.
(3) The ADC is not available on the MSP430FR2000 device.

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9.4 Interrupt Vector Addresses

The interrupt vectors and the power-up start address are in the address range 0FFFFh to 0FF80h. The vector contains the 16-bit address of the appropriate interrupt-handler instruction sequence. 表 9-2 summarizes the interrupts sources, flags, and vectors.

表 9-2. Interrupt Sources, Flags, and Vectors

INTERRUPT SOURCE	INTERRUPT FLAG	SYSTEM INTERRUPT	WORD ADDRESS	PRIORITY
System Reset Power up, brownout, supply supervisor External reset $\overline{RST}$ Watchdog time-out, key violation FRAM uncorrectable bit error detection Software POR, BOR FLL unlock error	SVSHIFG PMMRSTIFG WDTIFG PMMPORIFG, PMMBORIFG SYSRSTIV FLLULPUC	Reset	FFFEh	63, Highest
System NMI Vacant memory access JTAG mailbox FRAM access time error FRAM bit error detection	VMAIFG JMBINIFG, JMBOUTIFG CBDIFG, UBDIFG	(Non)maskable	FFFCh	62
User NMI External NMI Oscillator fault	NMIIFG OFIFG	(Non)maskable	FFFAh	61
Timer0_B3	TB0CCR0 CCIFG0	Maskable	FFF8h	60
Timer0_B3	TB0CCR1 CCIFG1, TB0CCR2 CCIFG2, TB0IFG (TB0IV)	Maskable	FFF6h	59
RTC counter	RTCIFG	Maskable	FFF4h	58
Watchdog timer interval mode	WDTIFG	Maskable	FFF2h	57
eUSCI_A0 receive or transmit	UCTXCPTIFG, UCSTTIFG, UCRXIFG, UCTXIFG (UART mode) UCRXIFG, UCTXIFG (SPI mode) (UCA0IV))	Maskable	FFF0h	56
ADC	ADCIFG0, ADCINIFG, ADCLOIFG, ADCHIIFG, ADCTOVIFG, ADCOVIFG (ADCIV)	Maskable	FFEEh	55
P1	P1IFG.0 to P1IFG.3 (P1IV)	Maskable	FFECh	54
P2	P2IFG.0, P2IFG.1, P2IFG.6 and P2IFG.7 (P2IV)	Maskable	FFEAh	53
eCOMP0	CPIIFG, CPIFG (CPIV)	Maskable	FFE8h	52
Reserved	Reserved	Maskable	FFE6h to FF88h	
Signatures	BSL Signature 2		0FF86h	
	BSL Signature 1		0FF84h	
	JTAG Signature 2		0FF82h	
	JTAG Signature 1		0FF80h	

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9.5 Memory Organization

表 9-3 summarizes the memory map of the MSP430FR211x and MSP430FR210x devices.

表 9-3. Memory Organization

MEMORY TYPE	ACCESS	MSP430FR2111	MSP430FR2110	MSP430FR2100	MSP430FR2000
Memory (FRAM) Main: interrupt vectors and signatures Main: code memory	Read/write (optional write protect)(1)	3.75KB FFFFh to FF80h FFFFh to F100h	2KB FFFFh to FF80h FFFFh to F800h	1KB FFFFh to FF80h FFFFh to FC00h	0.5KB FFFFh to FF80h FFFFh to FE00h
RAM	Read/write	1KB 23FFh to 2000h	1KB 23FFh to 2000h	512 bytes 21FFh to 2000h	512 bytes 21FFh to 2000h
Bootloader (BSL) memory (ROM) (TI internal use)	Read only	1KB 13FFh to 1000h	1KB 13FFh to 1000h	1KB 13FFh to 1000h	1KB 13FFh to 1000h
Peripherals	Read/write	4KB 0FFFh to 0000h	4KB 0FFFh to 0000h	4KB 0FFFh to 0000h	4KB 0FFFh to 0000h

(1) The Program FRAM can be write protected by setting the PFWP bit in the SYSCFG0 register. See the SYS chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide* for more details.

9.6 Bootloader (BSL)

The BSL lets users program the FRAM or RAM using a UART interface. Access to the device memory through the BSL is protected by an user-defined password. 表 9-4 lists the BSL pin requirements. BSL entry requires a specific entry sequence on the $\overline{\text{RST}}$/NMI/SBWTDIO and TEST/SBWTCK pins. For a complete description of the features of the BSL and its implementation, see the *MSP430 FRAM Device Bootloader (BSL) User's Guide*.

表 9-4. UART BSL Pin Requirements and Functions

DEVICE SIGNAL	BSL FUNCTION
$\overline{\text{RST}}$/NMI/SBWTDIO	Entry sequence signal
TEST/SBWTCK	Entry sequence signal
P1.7	Data transmit
P1.6	Data receive
DVCC	Power supply
DVSS	Ground supply

9.7 JTAG Standard Interface

The MSP430 family supports the standard JTAG interface, which requires four signals for sending and receiving data. The JTAG signals are shared with general-purpose I/Os. The TEST/SBWTCK pin is used to enable the JTAG signals. The $\overline{\text{RST}}$/NMI/SBWTDIO pin is also is required to interface with MSP430 development tools and device programmers. 表 9-5 lists the JTAG pin requirements. For details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*.

表 9-5. JTAG Pin Requirements and Function

DEVICE SIGNAL	DIRECTION	JTAG FUNCTION
P1.4/UCA0STE/TCK/A4	IN	JTAG clock input
P1.5/UCA0CLK/TMS/A5	IN	JTAG state control
P1.6/UCA0RXD/UCA0SOMI/TB0.1/TDI/TCLK/A6	IN	JTAG data input, TCLK input
P1.7/UCA0TXD/UCA0SIMO/TB0.2/TDO/A7/VREF+	OUT	JTAG data output
TEST/SBWTCK	IN	Enable JTAG pins
RST/NMI/SBWTDIO	IN	External reset
DVCC	–	Power supply
DVSS	–	Ground supply

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9.8 Spy-Bi-Wire Interface (SBW)

The MSP430 family supports the 2-wire Spy-Bi-Wire interface. Spy-Bi-Wire can be used to interface with MSP430 development tools and device programmers. 表 9-6 lists the Spy-Bi-Wire interface pin requirements. For further details on interfacing to development tools and device programmers, see the *MSP430 Hardware Tools User's Guide*.

表 9-6. Spy-Bi-Wire Pin Requirements and Functions

DEVICE SIGNAL	DIRECTION	SBW FUNCTION
TEST/SBWTCK	IN	Spy-Bi-Wire clock input
RST/NMI/SBWTDIO	IN, OUT	Spy-Bi-Wire data input and output
VCC		Power supply
VSS		Ground supply

9.9 FRAM

The FRAM can be programmed using the JTAG port, Spy-Bi-Wire (SBW), the BSL, or in-system by the CPU. Features of the FRAM include:

- Byte and word access capability
- Programmable wait state generation
- Error correction coding (ECC)

9.10 Memory Protection

The device features memory protection of user access authority and write protection include:

- Securing the whole memory map to prevent unauthorized access from JTAG port or BSL, by writing JTAG and BSL signatures using the JTAG port, SBW, the BSL, or in-system by the CPU.
- Write protection enabled to prevent unwanted write operation to FRAM contents by setting the control bits with accordingly password in System Configuration register 0. For more detailed information, see the SYS chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

9.11 Peripherals

Peripherals are connected to the CPU through data, address, and control buses. All peripherals can be handled by using all instructions in the memory map. For complete module description, see the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

9.11.1 Power-Management Module (PMM) and On-Chip Reference Voltages

The PMM includes an integrated voltage regulator that supplies the core voltage to the device. The PMM also includes supply voltage supervisor (SVS) and brownout protection. The brownout reset circuit (BOR) is implemented to provide the proper internal reset signal to the device during power on and power off. The SVS circuitry detects if the supply voltage drops below a user-selectable safe level. SVS circuitry is available on the primary supply.

The device contains two on-chip references: 1.5 V for internal reference and 1.2 V for external reference.

The 1.5-V reference is internally connected to ADC channel 13. DVCC is internally connected to ADC channel 15. When DVCC is set as the reference voltage for ADC conversion, the DVCC can be easily represent as 式 1 by using the ADC sampling the 1.5-V reference without any external components support.

$$DVCC = (1023 \times 1.5\ V) / 1.5\text{-V Reference ADC result} \quad (1)$$

The 1.5-V reference is also internally connected to the comparator built-in DAC as reference voltage. DVCC is internally connected to another source of the DAC reference, and both are controlled by the CPDACREFS bit. For more detailed information, see the Comparator chapter of the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

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A 1.2-V reference voltage can be buffered and output to P1.7/TDO/A7/VREF+, when EXTREFEN = 1 in the PMMCTL2 register. ADC channel 7 can also be selected to monitor this voltage. For more detailed information, see the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

注

The ADC is not available on the MSP430FR2000 device.

9.11.2 Clock System (CS) and Clock Distribution

The clock system includes a 32-kHz low-frequency oscillator (XT1), an internal very-low-power low-frequency oscillator (VLO), an integrated 32-kHz RC oscillator (REFO), an integrated internal digitally controlled oscillator (DCO) that may use frequency-locked loop (FLL) locking with an internal or external 32-kHz reference clock, and on-chip asynchronous high-speed clock (MODOSC). The clock system is designed to target cost-effective designs with minimal external components. A fail-safe mechanism is designed for XT1. The clock system module offers the following clock signals.

- Main Clock (MCLK): the system clock used by the CPU and all relevant peripherals accessed by the bus. All clock sources except MODOSC can be selected as the source with a predivider of 1, 2, 4, 8, 16, 32, 64, or 128.
- Sub-Main Clock (SMCLK): the subsystem clock used by the peripheral modules. SMCLK derives from the MCLK with a predivider of 1, 2, 4, or 8. This means SMCLK is always equal to or less than MCLK.
- Auxiliary Clock (ACLK): this clock is derived from the external XT1 clock or internal REFO clock up to 40 kHz.

All peripherals may have one or several clock sources depending on specific functionality. 表 9-7 and 表 9-8 summarize the clock distribution used in this device.

表 9-7. Clock Distribution

	CLOCK SOURCE SELECT BITS	MCLK	SMCLK	ACLK	MODCLK	VLOCLK	EXTERNAL PIN
Frequency Range		DC to 16 MHz	DC to 16 MHz	DC to 40 kHz	4 MHz	10 kHz	
CPU	N/A	Default					
FRAM	N/A	Default					
RAM	N/A	Default					
CRC	N/A	Default					
I/O	N/A	Default					
TB0	TBSSEL		10b	01b			00b (TB0CLK pin)
eUSCI_A0	UCSSEL		10b or 11b	01b			00b (UCA0CLK pin)
WDT	WDTSSEL		00b	01b		10b	
ADC(1)	ADCSSEL		10b or 11b	01b	00b		
RTC	RTCSS		01b(2)	01b(2)		11b	

(1) The ADC is not available on the MSP430FR2000 device.
(2) Controlled by the RTCCKSEL bit in the SYSCFG2 register.

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表 9-8. XTCLK Distribution

OPERATION MODE	CLOCK SOURCE SELECT BITS	XTLFCLK
		AM TO LPM3.5 (DC to 40 kHz)
MCLK	SELMS	10b
SMCLK	SELMS	10b
REFO	SELREF	0b
ACLK	SELA	0b
RTC	RTCSS	10b

9.11.3 General-Purpose Input/Output Port (I/O)

Up to 12 I/O ports are implemented.

- P1 has 8 bits implemented, and P2 has 4 bits implemented.
- All individual I/O bits are independently programmable.
- Any combination of input, output, and interrupt conditions is possible to P1 and P2.
- Programmable pullup or pulldown on all ports.
- Edge-selectable interrupt, LPM4, LPM3.5 and LPM4.5 wake-up input capability is available for P1.0 to P1.3, P2.0, P2.1, P2.6, and P2.7.
- Read and write access to port-control registers is supported by all instructions.
- Ports can be accessed byte-wise or word-wise in pairs.
- Capacitive Touch I/O functionality is supported on all pins.

注

Configuration of digital I/Os after BOR reset

To prevent any cross currents during start-up of the device, all port pins are high-impedance with Schmitt triggers and module functions disabled. To enable the I/O functions after a BOR reset, the ports must be configured first and then the LOCKLPM5 bit must be cleared. For details, see the *Configuration After Reset* section in the Digital I/O chapter of the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

9.11.4 Watchdog Timer (WDT)

The primary function of the WDT module is to perform a controlled system restart after a software problem occurs. If the selected time interval expires, a system reset is generated. If the watchdog function is not needed in an application, the module can be configured as interval timer and can generate interrupts at selected time intervals.

表 9-9. WDT Clocks

WDTSSEL	NORMAL OPERATION (WATCHDOG AND INTERVAL TIMER MODE)
00	SMCLK
01	ACLK
10	VLOCLK
11	Reserved

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9.11.5 System Module (SYS)

The SYS module handles many of the system functions within the device. These system functions include power-on reset (POR) and power-up clear (PUC) handling, NMI source selection and management, reset interrupt vector generators, bootloader entry mechanisms, and configuration management (device descriptors). SYS also includes a data exchange mechanism through SBW called a JTAG mailbox that can be used in the application. 表 9-10 lists the SYS module interrupt vector registers.

表 9-10. System Module Interrupt Vector Registers

INTERRUPT VECTOR REGISTER	ADDRESS	INTERRUPT EVENT	VALUE	PRIORITY
SYSRSTIV, System Reset	015Eh	No interrupt pending	00h	
		Brownout (BOR)	02h	Highest
		RSTIFG $\overline{\text{RST}}$/NMI (BOR)	04h	
		PMMSWBOR software BOR (BOR)	06h	
		LPMx.5 wakeup (BOR)	08h	
		Security violation (BOR)	0Ah	
		Reserved	0Ch	
		SVSHIFG SVSH event (BOR)	0Eh	
		Reserved	10h	
		Reserved	12h	
		PMMSWPOR software POR (POR)	14h	
		WDTIFG watchdog time-out (PUC)	16h	
		WDTPW password violation (PUC)	18h	
		FRCTLPW password violation (PUC)	1Ah	
		Uncorrectable FRAM bit error detection	1Ch	
		Peripheral area fetch (PUC)	1Eh	
		PMMPW PMM password violation (PUC)	20h	
		Reserved	22h	
		FLL unlock (PUC)	24h	
		Reserved	26h to 3Eh	Lowest
SYSSNIV, System NMI	015Ch	No interrupt pending	00h	
		SVS low-power reset entry	02h	Highest
		Uncorrectable FRAM bit error detection	04h	
		Reserved	06h	
		Reserved	08h	
		Reserved	0Ah	
		Reserved	0Ch	
		Reserved	0Eh	
		Reserved	10h	
		VMAIFG Vacant memory access	12h	
		JMBINIFG JTAG mailbox input	14h	
		JMBOUTIFG JTAG mailbox output	16h	
		Correctable FRAM bit error detection	18h	
		Reserved	1Ah to 1Eh	Lowest
SYSUNIV, User NMI	015Ah	No interrupt pending	00h	
		NMIIFG NMI pin or SVS_H event	02h	Highest
		OFIFG oscillator fault	04h	
		Reserved	06h to 1Eh	Lowest

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9.11.6 Cyclic Redundancy Check (CRC)

The 16-bit CRC module produces a signature based on a sequence of data values and can be used for data checking purposes. The CRC generation polynomial is compliant with CRC-16-CCITT standard of $x^{16} + x^{12} + x^5 + 1$.

9.11.7 Enhanced Universal Serial Communication Interface (eUSCI_A0)

The eUSCI modules are used for serial data communications. The eUSCI_A module supports either UART or SPI communications. Additionally, eUSCI_A supports automatic baud-rate detection and IrDA.

表 9-11. eUSCI Pin Configurations

	PIN (USCIARMP = 0)	UART	SPI
eUSCI_A0	P1.7	TXD	SIMO
	P1.6	RXD	SOMI
	P1.5		SCLK
	P1.4		STE
	PIN (USCIARMP = 1)	**UART**	**SPI**
	P1.3(1)	TXD	SIMO
	P1.2(1)	RXD	SOMI
	P1.1(1)		SCLK
	P1.0(1)		STE

(1) This is the remapped functionality controlled by the USCIARMP bit in the SYSCFG3 register. Only one selected port is valid at the same time.

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9.11.8 Timers (Timer0_B3)

The Timer0_B3 module is 16-bit timer and counter with three capture/compare registers. The timer can support multiple captures or compares, PWM outputs, and interval timing (see 表 9-12). Timer0_B3 has extensive interrupt capabilities. Interrupts may be generated from the counter on overflow conditions and from each of the capture/compare registers. The CCR0 register on Timer0_B3 is not externally connected and can be used only for hardware period timing and interrupt generation. In Up Mode, it can be used to set the overflow value of the counter.

表 9-12. Timer0_B3 Signal Connections

PORT PIN	DEVICE INPUT SIGNAL	MODULE INPUT NAME	MODULE BLOCK	MODULE OUTPUT SIGNAL	DEVICE OUTPUT SIGNAL
P2.7	TB0CLK	TBCLK	Timer	N/A	
	ACLK (internal)	ACLK			
	SMCLK (internal)	SMCLK			
	From Capacitive Touch I/O (internal)	INCLK			
	From RTC (internal)	CCI0A	CCR0	TB0	
	ACLK (internal)	CCI0B			
	DVSS	GND			
	DVCC	VCC			
P1.6 (TBRMP = 0)	TB0.1	CCI1A	CCR1	TB1	TB0.1
P2.0 (TBRMP = 1)(1)					
	From eCOMP (internal)	CCI1B			To ADC trigger(2)
	DVSS	GND			
	DVCC	VCC			
P1.7 (TBRMP = 0)	TB0.2	CCI2A	CCR2	TB2	TB0.2
P2.1 (TBRMP = 1)(1)					
	From Capacitive Touch I/O (internal)	CCI2B			
	DVSS	GND			
	DVCC	VCC			

(1) This is the remapped functionality controlled by the TBRMP bit in the SYSCFG3 register. Only one selected port is valid at the same time when TB0 acts as capture input functionality. TB0 PWM outputs regardless of the setting on this remap bit.
(2) The ADC is not available on the MSP430FR2000 device.

The interconnection of Timer0_B3 can be used to modulate the eUSCI_A pin of UCA0TXD/UCA0SIMO in either ASK or part of FSK mode, with which a user can easily acquire a modulated infrared command for directly driving an external IR diode. The IR functions are fully controlled by SYSCFG1 including IREN (enable), IRPSEL (polarity select), IRMSEL (mode select), IRDSSEL (data select), and IRDATA (data) bits. For more information, see the SYS chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

The Timer_B module can put all Timer_B outputs into a high-impedance state when the selected source is triggered. The source can be selected from external pin or internal of the device, which is controlled by TB0TRG in SYS. For more information, see the SYS chapter in the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

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表 9-13 summarizes the selection of the Timer_B high-impedance trigger.

表 9-13. TBxOUTH

TB0TRGSEL	TB0OUTH TRIGGER SOURCE SELECTION	Timer_B PAD OUTPUT HIGH IMPEDANCE
TB0TRGSEL = 0	eCOMP0 output (internal)	P1.6, P1.7, P2.0, P2.1(1)
TB0TRGSEL= 1	P1.2	

(1) When TB0 is set to PWM output function, both port groups can receive the output, and the output is controlled by only the PxSEL.y bits.

9.11.9 Backup Memory (BAKMEM)

The BAKMEM supports data retention functionality during LPM3.5 mode. This device provides up to 32 bytes that are retained during LPM3.5.

9.11.10 Real-Time Clock (RTC) Counter

The RTC counter is a 16-bit modulo counter that is functional in AM, LPM0, LPM3, LPM4, and LPM3.5. This module may periodically wake up the CPU from LPM0, LPM3, LPM4, or LPM3.5 based on timing from a low-power clock source such as XT1, ACLK, or VLO. In AM, RTC can be driven by SMCLK to generate high-frequency timing events and interrupts. ACLK and SMCLK both can source to the RTC; however, only one of them can be selected at any given time. The RTC overflow events trigger:

- Timer0_B3 CCR0A
- ADC conversion trigger when ADCSHSx bits are set as 01b

9.11.11 10-Bit Analog-to-Digital Converter (ADC)

The 10-bit ADC module supports fast 10-bit analog-to-digital conversions with single-ended input. The module implements a 10-bit SAR core, sample select control, reference generator, and a conversion result buffer. A window comparator with lower and upper limits allows CPU-independent result monitoring with three window comparator interrupt flags.

注

The ADC is not available on the MSP430FR2000 device.

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The ADC supports 10 external inputs and 4 internal inputs (see 表 9-14).

表 9-14. ADC Channel Connections

ADCINCHx	ADC CHANNELS	EXTERNAL PIN OUT
0	A0/Veref+	P1.0
1	A1/	P1.1
2	A2/Veref-	P1.2
3	A3	P1.3
4	A4	P1.4
5	A5	P1.5
6	A6	P1.6
7	A7(1)	P1.7
8	Not used	N/A
9	Not used	N/A
10	Not used	N/A
11	Not used	N/A
12	On-chip temperature sensor	N/A
13	Reference voltage (1.5 V)	N/A
14	DVSS	N/A
15	DVCC	N/A

(1) When A7 is used, the PMM 1.2-V reference voltage can be output to this pin by setting the PMM control register. The 1.2-V voltage can be directly measured by A7 channel.

The conversion can be started by software or a hardware trigger. 表 9-15 lists the trigger sources that are available.

表 9-15. ADC Trigger Signal Connections

ADCSHSx		TRIGGER SOURCE
BINARY	DECIMAL	
00	0	ADCSC bit (software trigger)
01	1	RTC event
10	2	TB0.1B
11	3	eCOMP0 COUT

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9.11.12 eCOMP0

The enhanced comparator is an analog voltage comparator with built-in 6-bit DAC as an internal voltage reference. The integrated 6-bit DAC can be set up to 64 steps for comparator reference voltage. This module has 4-level programmable hysteresis and a configurable power mode: high-power or low-power mode.

The eCOMP0 supports external inputs and internal inputs (see 表 9-16) and outputs (see 表 9-17)

表 9-16. eCOMP0 Input Channel Connections

CPPSEL, CPNSEL BINARY	eCOMP0 CHANNELS	EXTERNAL OR INTERNAL CONNECTION
000	C0	P1.0
001	C1	P1.1
010	C2	P1.2
011	C3	P1.3
100	C4	Not used
101	C5	Not used
110	C6	Built-in 6-bit DAC

表 9-17. eCOMP0 Output Channel Connections

eCOMP0 Out	EXTERNAL PIN OUT, MODULE
1	P2.0
2	TB0.1B ; TB0 (TB0OUTH); ADC

9.11.13 Embedded Emulation Module (EEM)

The EEM supports real-time in-system debugging. The EEM on these devices has the following features:

- Three hardware triggers or breakpoints on memory access
- One hardware trigger or breakpoint on CPU register write access
- Up to four hardware triggers that can be combined to form complex triggers or breakpoints
- One cycle counter
- Clock control on module level

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9.11.14 Peripheral File Map

表 9-18 lists the base address and the memory size of the registers for each peripheral.

表 9-18. Peripherals Summary

MODULE NAME	BASE ADDRESS	SIZE
Special Functions (see 表 9-19)	0100h	0010h
PMM (see 表 9-20)	0120h	0020h
SYS (see 表 9-21)	0140h	0040h
CS (see 表 9-22)	0180h	0020h
FRAM (see 表 9-23)	01A0h	0010h
CRC (see 表 9-24)	01C0h	0008h
WDT (see 表 9-25)	01CCh	0002h
Port P1, P2 (see 表 9-26)	0200h	0020h
Capacitive Touch I/O (see 表 9-27)	02E0h	0010h
RTC (see 表 9-28)	0300h	0010h
Timer0_B3 (see 表 9-29)	0380h	0030h
eUSCI_A0 (see 表 9-30)	0500h	0020h
Backup Memory (see 表 9-31)	0660h	0020h
ADC(1) (see 表 9-32)	0700h	0040h
eCOMP0 (see 表 9-33)	08E0h	0020h

(1) The ADC is not available on the MSP430FR2000 device.

表 9-19. Special Function Registers (Base Address: 0100h)

REGISTER DESCRIPTION	REGISTER	OFFSET
SFR interrupt enable	SFRIE1	00h
SFR interrupt flag	SFRIFG1	02h
SFR reset pin control	SFRRPCR	04h

表 9-20. PMM Registers (Base Address: 0120h)

REGISTER DESCRIPTION	REGISTER	OFFSET
PMM control 0	PMMCTL0	00h
PMM control 1	PMMCTL1	02h
PMM control 2	PMMCTL2	04h
PMM interrupt flags	PMMIFG	0Ah
PM5 control 0	PM5CTL0	10h

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表 9-21. SYS Registers (Base Address: 0140h)

REGISTER DESCRIPTION	REGISTER	OFFSET
System control	SYSCTL	00h
Bootloader configuration area	SYSBSLC	02h
JTAG mailbox control	SYSJMBC	06h
JTAG mailbox input 0	SYSJMBI0	08h
JTAG mailbox input 1	SYSJMBI1	0Ah
JTAG mailbox output 0	SYSJMBO0	0Ch
JTAG mailbox output 1	SYSJMBO1	0Eh
User NMI vector generator	SYSUNIV	1Ah
System NMI vector generator	SYSSNIV	1Ch
Reset vector generator	SYSRSTIV	1Eh
System configuration 0	SYSCFG0	20h
System configuration 1	SYSCFG1	22h
System configuration 2	SYSCFG2	24h
System configuration 3	SYSCFG3	26h

表 9-22. CS Registers (Base Address: 0180h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CS control 0	CSCTL0	00h
CS control 1	CSCTL1	02h
CS control 2	CSCTL2	04h
CS control 3	CSCTL3	06h
CS control 4	CSCTL4	08h
CS control 5	CSCTL5	0Ah
CS control 6	CSCTL6	0Ch
CS control 7	CSCTL7	0Eh
CS control 8	CSCTL8	10h

表 9-23. FRAM Registers (Base Address: 01A0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
FRAM control 0	FRCTL0	00h
General control 0	GCCTL0	04h
General control 1	GCCTL1	06h

表 9-24. CRC Registers (Base Address: 01C0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
CRC data input	CRC16DI	00h
CRC data input reverse byte	CRCDIRB	02h
CRC initialization and result	CRCINIRES	04h
CRC result reverse byte	CRCRESR	06h

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表 9-25. WDT Registers (Base Address: 01CCh)

REGISTER DESCRIPTION	REGISTER	OFFSET
Watchdog timer control	WDTCTL	00h

表 9-26. Port P1, P2 Registers (Base Address: 0200h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Port P1 input	P1IN	00h
Port P1 output	P1OUT	02h
Port P1 direction	P1DIR	04h
Port P1 pulling enable	P1REN	06h
Port P1 selection 0	P1SEL0	0Ah
Port P1 selection 1	P1SEL1	0Ch
Port P1 interrupt vector word	P1IV	0Eh
Port P1 complement selection	P1SELC	16h
Port P1 interrupt edge select	P1IES	18h
Port P1 interrupt enable	P1IE	1Ah
Port P1 interrupt flag	P1IFG	1Ch
Port P2 input	P2IN	01h
Port P2 output	P2OUT	03h
Port P2 direction	P2DIR	05h
Port P2 pulling enable	P2REN	07h
Port P2 selection 0	P2SEL0	0Bh
Port P2 selection 1	P2SEL1	0Dh
Port P2 complement selection	P2SELC	17h
Port P2 interrupt vector word	P2IV	1Eh
Port P2 interrupt edge select	P2IES	19h
Port P2 interrupt enable	P2IE	1Bh
Port P2 interrupt flag	P2IFG	1Dh

表 9-27. Capacitive Touch I/O Registers (Base Address: 02E0h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Capacitive Touch I/O 0 control	CAPIO0CTL	0Eh

表 9-28. RTC Registers (Base Address: 0300h)

REGISTER DESCRIPTION	REGISTER	OFFSET
RTC control	RTCCTL	00h
RTC interrupt vector	RTCIV	04h
RTC modulo	RTCMOD	08h
RTC counter	RTCCNT	0Ch

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表 9-29. Timer0_B3 Registers (Base Address: 0380h)

REGISTER DESCRIPTION	REGISTER	OFFSET
TB0 control	TB0CTL	00h
Capture/compare control 0	TB0CCTL0	02h
Capture/compare control 1	TB0CCTL1	04h
Capture/compare control 2	TB0CCTL2	06h
TB0 counter	TB0R	10h
Capture/compare 0	TB0CCR0	12h
Capture/compare 1	TB0CCR1	14h
Capture/compare 2	TB0CCR2	16h
TB0 expansion 0	TB0EX0	20h
TB0 interrupt vector	TB0IV	2Eh

表 9-30. eUSCI_A0 Registers (Base Address: 0500h)

REGISTER DESCRIPTION	REGISTER	OFFSET
eUSCI_A control word 0	UCA0CTLW0	00h
eUSCI_A control word 1	UCA0CTLW1	02h
eUSCI_A control rate 0	UCA0BR0	06h
eUSCI_A control rate 1	UCA0BR1	07h
eUSCI_A modulation control	UCA0MCTLW	08h
eUSCI_A status	UCA0STAT	0Ah
eUSCI_A receive buffer	UCA0RXBUF	0Ch
eUSCI_A transmit buffer	UCA0TXBUF	0Eh
eUSCI_A LIN control	UCA0ABCTL	10h
eUSCI_A IrDA transmit control	IUCA0IRTCTL	12h
eUSCI_A IrDA receive control	IUCA0IRRCTL	13h
eUSCI_A interrupt enable	UCA0IE	1Ah
eUSCI_A interrupt flags	UCA0IFG	1Ch
eUSCI_A interrupt vector word	UCA0IV	1Eh

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表 9-31. Backup Memory Registers (Base Address: 0660h)

REGISTER DESCRIPTION	REGISTER	OFFSET
Backup memory 0	BAKMEM0	00h
Backup memory 1	BAKMEM1	02h
Backup memory 2	BAKMEM2	04h
Backup memory 3	BAKMEM3	06h
Backup memory 4	BAKMEM4	08h
Backup memory 5	BAKMEM5	0Ah
Backup memory 6	BAKMEM6	0Ch
Backup memory 7	BAKMEM7	0Eh
Backup memory 8	BAKMEM8	10h
Backup memory 9	BAKMEM9	12h
Backup memory 10	BAKMEM10	14h
Backup memory 11	BAKMEM11	16h
Backup memory 12	BAKMEM12	18h
Backup memory 13	BAKMEM13	1Ah
Backup memory 14	BAKMEM14	1Ch
Backup memory 15	BAKMEM15	1Eh

表 9-32. ADC Registers (Base Address: 0700h)

REGISTER DESCRIPTION	REGISTER	OFFSET
ADC control 0	ADCCTL0	00h
ADC control 1	ADCCTL1	02h
ADC control 2	ADCCTL2	04h
ADC window comparator low threshold	ADCLO	06h
ADC window comparator high threshold	ADCHI	08h
ADC memory control 0	ADCMCTL0	0Ah
ADC conversion memory	ADCMEM0	12h
ADC interrupt enable	ADCIE	1Ah
ADC interrupt flags	ADCIFG	1Ch
ADC interrupt vector word	ADCIV	1Eh

表 9-33. eCOMP0 Registers (Base Address: 08E0h)

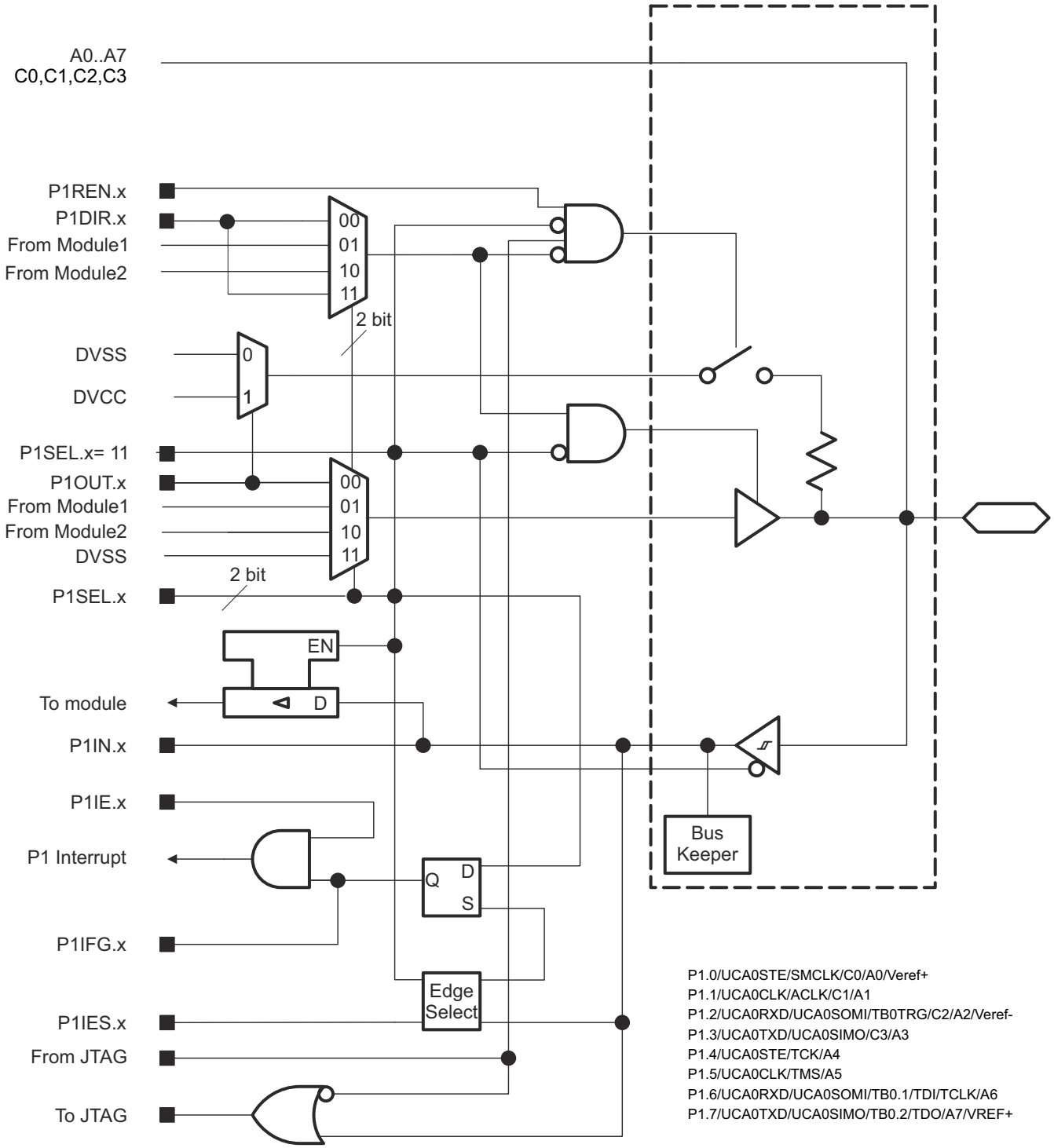
REGISTER DESCRIPTION	REGISTER	OFFSET
Comparator control 0	CPCTL0	00h
Comparator control 1	CPCTL1	02h
Comparator interrupt	CPINT	06h
Comparator interrupt vector	CPIV	08h
Comparator built-in DAC control	CPDACCTL	10h
Comparator built-in DAC data	CPDACDATA	12h

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9.11.15 Input/Output Diagrams

9.11.15.1 Port P1 Input/Output With Schmitt Trigger

図 9-1 shows the port diagram. 表 9-34 summarizes the selection of the pin functions.



Functional representation only.

The ADC (signals A0 to A7, Veref+, and Veref-) is not available on the MSP430FR2000 device.

図 9-1. Port P1 Input/Output With Schmitt Trigger

表 9-34. Port P1 Pin Functions

PIN NAME (P1.x)	x	FUNCTION	CONTROL BITS AND SIGNALS(1)		
			P1DIR.x	P1SELx	JTAG
P1.0/UCA0STE/SMCLK/ C0/A0/Veref+	0	P1.0 (I/O)	I: 0; O: 1	00	N/A
		UCA0STE	X	01	N/A
		SMCLK	1	10	N/A
		VSS	0		
		C0, A0/Veref+(2)	X	11	N/A
P1.1/UCA0CLK/ACLK/ C1/A1	1	P1.1 (I/O)	I: 0; O: 1	0	N/A
		UCA0CLK	X	01	N/A
		ACLK	1	10	N/A
		VSS	0		
		C1, A1(2)	X	11	N/A
P1.2/UCA0RXD/ UCA0SOMI/TB0TRG/ C2/A2/Veref-	2	P1.2 (I/O)	I: 0; O: 1	00	N/A
		UCA0RXD/UCA0SOMI	X	01	N/A
		TB0TRG	0	10	N/A
		C2, A2/Veref-(2)	X	11	N/A
P1.3/UCA0TXD/ UCA0SIMO/C3/A3	3	P1.3 (I/O)	I: 0; O: 1	00	N/A
		UCA0TXD/UCA0SIMO	X	01	N/A
		C3, A3(2)	X	11	N/A
P1.4/UCA0STE/TCK/A4	4	P1.4 (I/O)	I: 0; O: 1	00	Disabled
		UCA0STE	X	01	N/A
		A4(2)	X	11	Disabled
		JTAG TCK	X	X	TCK
P1.5/UCA0CLK/TMS/A5	5	P1.5 (I/O)	I: 0; O: 1	00	Disabled
		UCA0CLK	X	01	N/A
		A5(2)	X	11	Disabled
		JTAG TMS	X	X	TMS
P1.6/UCA0RXD/ UCA0SOMI/TB0.1/ TDI/ TCLK/A6	6	P1.6 (I/O)	I: 0; O: 1	00	Disabled
		UCA0RXD/UCA0SOMI	X	01	N/A
		TB0.CCI1A	0	10	N/A
		TB0.1	1		
		A6(2)	X	11	Disabled
		JTAG TDI/TCLK	X	X	TDI/TCLK
P1.7/UCA0TXD/ UCA0SIMO/TB0.2/ TDO/A7/VREF+	7	P1.7 (I/O)	I: 0; O: 1	00	Disabled
		UCA0TXD/UCA0SIMO	X	01	N/A
		TB0.CCI2A	0	10	N/A
		TB0.2	1		
		A7(2), VREF+	X	11	Disabled
		JTAG TDO	X	X	TDO

(1) X = don't care
(2) The ADC is not available on the MSP430FR2000 device.

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9.11.15.2 Port P2 Input/Output With Schmitt Trigger

図 9-2 shows the port diagram. 表 9-35 summarizes the selection of the pin functions.

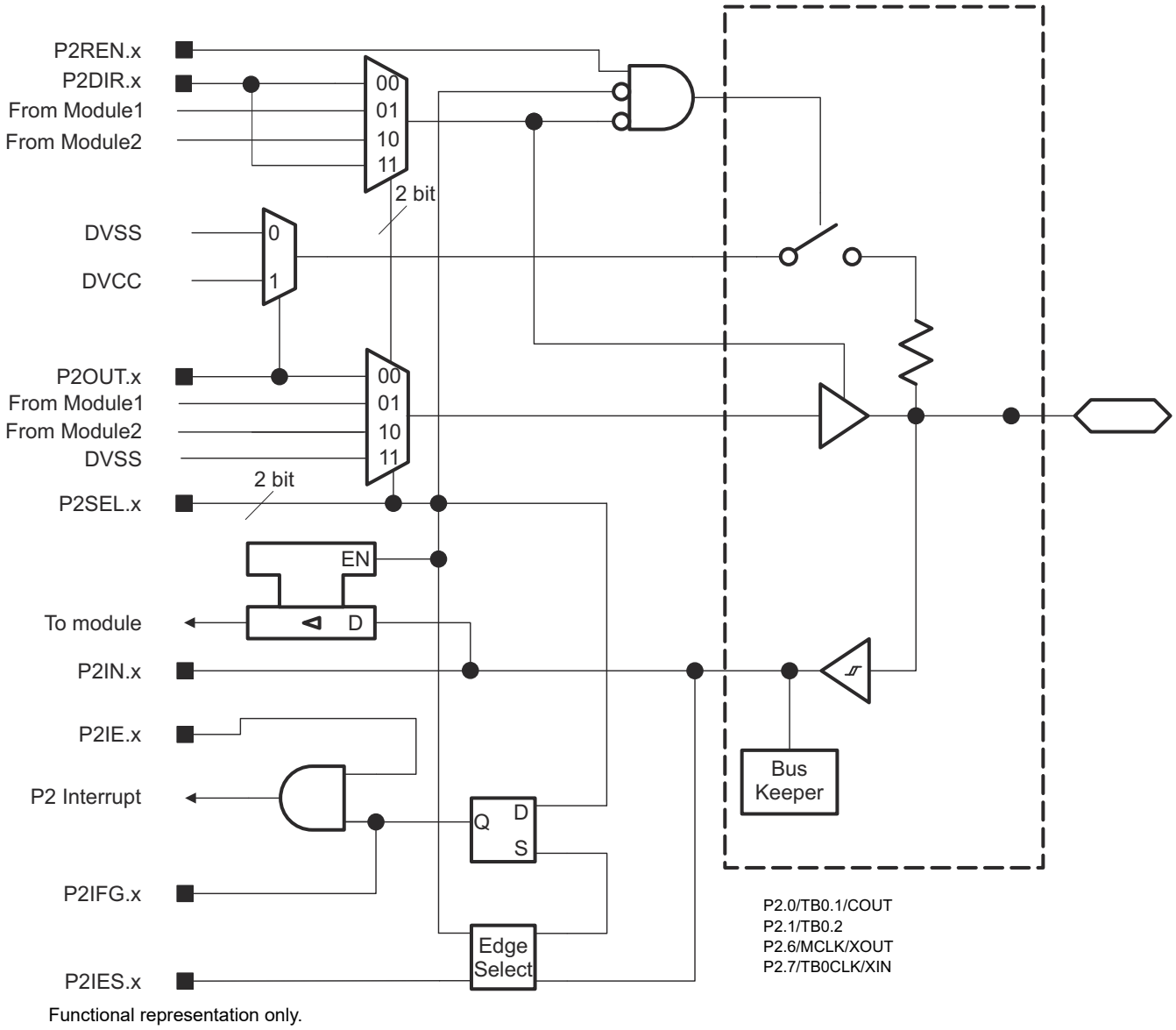


図 9-2. Port P2 Input/Output With Schmitt Trigger

表 9-35. Port P2 Pin Functions

PIN NAME (P2.x)	x	FUNCTION	CONTROL BITS AND SIGNALS[1]	
			P2DIR.x	P2SELx
P2.0/TB0.1/COUT	0	P2.0 (I/O)	I: 0; O: 1	00
		TB0.CCI1A	0	01
		TB0.1	1	
		COUT	1	10
P2.1/TB0.2	1	P2.1 (I/O)0	I: 0; O: 1	00
		TB0.CCI2A	0	01
		TB0.2	1	
P2.6/MCLK/XOUT	6	P2.6 (I/O)	I: 0; O: 1	00
		MCLK	1	01
		VSS	0	
		XOUT	X	10
P2.7/TB0CLK/XIN	7	P2.7 (I/O)	I: 0; O: 1	00
		TB0CLK	0	01
		VSS	1	
		XIN	X	10

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9.12 Device Descriptors (TLV)

表 9-36 lists the Device IDs of the MSP430FR211x MCUs. 表 9-37 lists the contents of the device descriptor tag-length-value (TLV) structure for MSP430FR211x MCUs.

表 9-36. Device IDs

DEVICE	DEVICE ID	
	1A04h	1A05h
MSP430FR2111	FA	82
MSP430FR2110	FB	82
MSP430FR2100	20	83
MSP430FR2000	21	83

表 9-37. Device Descriptors

	DESCRIPTION	MSP430FR211x	
		ADDRESS	VALUE
Info Block	Info length	1A00h	06h
	CRC length	1A01h	06h
	CRC value(1)	1A02h	Per unit
		1A03h	Per unit
	Device ID	1A04h	See 表 9-36
		1A05h	
	Hardware revision	1A06h	Per unit
	Firmware revision	1A07h	Per unit
Die Record	Die record tag	1A08h	08h
	Die record length	1A09h	0Ah
	Lot wafer ID	1A0Ah	Per unit
		1A0Bh	Per unit
		1A0Ch	Per unit
		1A0Dh	Per unit
	Die X position	1A0Eh	Per unit
		1A0Fh	Per unit
	Die Y position	1A10h	Per unit
		1A11h	Per unit
	Test result	1A12h	Per unit
		1A13h	Per unit
ADC Calibration(3)	ADC calibration tag	1A14h	Per unit
	ADC calibration length	1A15h	Per unit
	ADC gain factor	1A16h	Per unit
		1A17h	Per unit
	ADC offset	1A18h	Per unit
		1A19h	Per unit
	ADC 1.5-V reference temperature 30°C	1A1Ah	Per unit
		1A1Bh	Per unit
	ADC 1.5-V reference temperature 85°C	1A1Ch	Per unit
		1A1Dh	Per unit

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表 9-37. Device Descriptors (continued)

	DESCRIPTION	MSP430FR211x	
		ADDRESS	VALUE
Reference and DCO Calibration	Calibration tag	1A1Eh	12h
	Calibration length	1A1Fh	04h
	1.5-V reference factor	1A20h	Per unit
		1A21h	Per unit
	DCO tap settings for 16 MHz, temperature 30°C (2)	1A22h	Per unit
		1A23h	Per unit

(1) The CRC value includes the checksum from 0x1A04h to 0x1A77h, calculated by applying the CRC-CCITT-16 polynomial: $X^{16} + X^{12} + X^5 + 1$
(2) This value can be directly loaded into the DCO bits in the CSCTL0 register to get accurate 16-MHz frequence at room temperature, especially when the MCU exits from LPM3 and below. TI suggests using a predivider to decrease the frequency if the temperature drift might result an overshoot >16 MHz.
(3) The ADC is not available on the MSP430FR2000 device.

9.13 Identification

9.13.1 Revision Identification

The device revision information is shown as part of the top-side marking on the device package. The device-specific errata describes these markings. For links to the errata for the devices in this data sheet, see セクション 11.4.

The hardware revision is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Hardware Revision" entries in セクション 9.12.

9.13.2 Device Identification

The device type can be identified from the top-side marking on the device package. The device-specific errata describes these markings. For links to the errata for the devices in this data sheet, see セクション 11.4.

A device identification value is also stored in the Device Descriptor structure in the Info Block section. For details on this value, see the "Device ID" entries in セクション 9.12.

9.13.3 JTAG Identification

Programming through the JTAG interface, including reading and identifying the JTAG ID, is described in detail in *MSP430 Programming With the JTAG Interface*.

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10 Applications, Implementation, and Layout

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

10.1 Device Connection and Layout Fundamentals

This section describes the recommended guidelines when designing with the MSP430 MCU. These guidelines are to make sure that the device has proper connections for powering, programming, debugging, and optimum analog performance.

10.1.1 Power Supply Decoupling and Bulk Capacitors

TI recommends connecting a combination of a 10-µF capacitor and a 100-nF low-ESR ceramic decoupling capacitor to the DVCC pin. Higher-value capacitors may be used but can affect supply rail ramp-up time. Place decoupling capacitors as close as possible to the pins that they decouple (within a few millimeters).

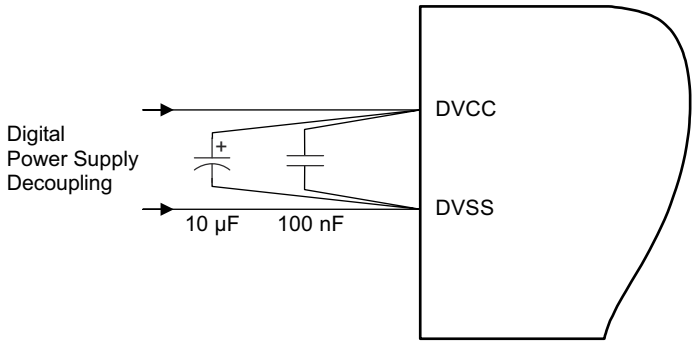


図 10-1. Power Supply Decoupling

10.1.2 External Oscillator

Depending on the device variant (see 表 6-1), the device supports only a low-frequency crystal (32 kHz) on the LFXT pins. External bypass capacitors for the crystal oscillator pins are required.

It is also possible to apply digital clock signals to the LFXIN input pins that meet the specifications of the respective oscillator if the appropriate LFXTBYPASS mode is selected. In this case, the associated LFXOUT pins can be used for other purposes. If the LFXOUT pins are left unused, they must be terminated according to セクション 7.5.

図 10-2 shows a typical connection diagram. See *MSP430 32-kHz Crystal Oscillators* for information on selecting, testing, and designing a crystal oscillator with the MSP430 devices.

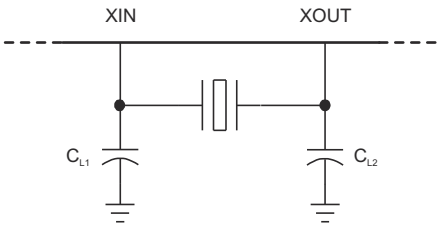


図 10-2. Typical Crystal Connection

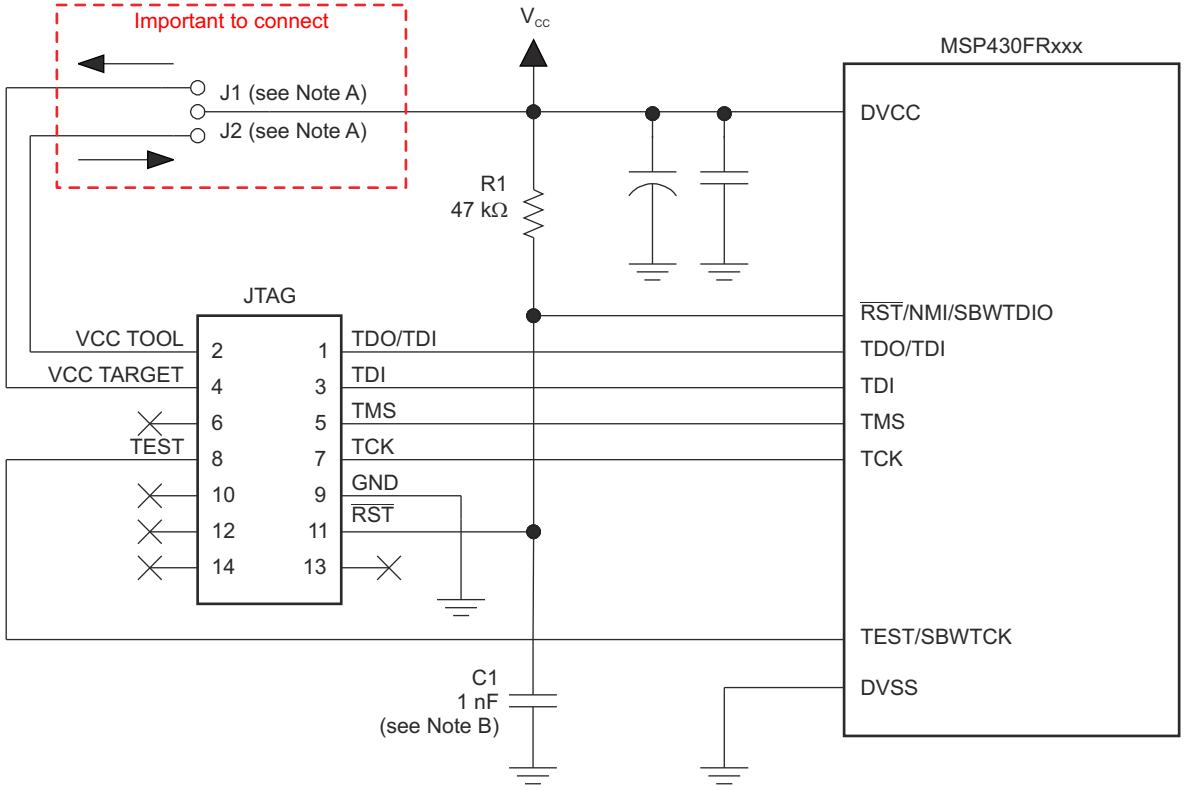
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10.1.3 JTAG

With the proper connections, the debugger and a hardware JTAG interface (such as the MSP-FET or MSP-FET430UIF) can be used to program and debug code on the target board. In addition, the connections also support the MSP-GANG production programmers, thus providing an easy way to program prototype boards, if desired. 図 10-3 shows the connections between the 14-pin JTAG connector and the target device required to support in-system programming and debugging for 4-wire JTAG communication. 図 10-4 shows the connections for 2-wire JTAG mode (Spy-Bi-Wire).

The connections for the MSP-FET and MSP-FET430UIF interface modules and the MSP-GANG are identical. Both can supply V_{CC} to the target board (through pin 2). In addition, the MSP-FET and MSP-FET430UIF interface modules and MSP-GANG have a V_{CC}-sense feature that, if used, requires an alternate connection (pin 4 instead of pin 2). The V_{CC}-sense feature senses the local V_{CC} present on the target board (that is, a battery or other local power supply) and adjusts the output signals accordingly. 図 10-3 and 図 10-4 show a jumper block that supports both scenarios of supplying V_{CC} to the target board. If this flexibility is not required, the desired V_{CC} connections may be hardwired to eliminate the jumper block. Pins 2 and 4 must not be connected at the same time.

For additional design information regarding the JTAG interface, see the *MSP430 Hardware Tools User's Guide*.



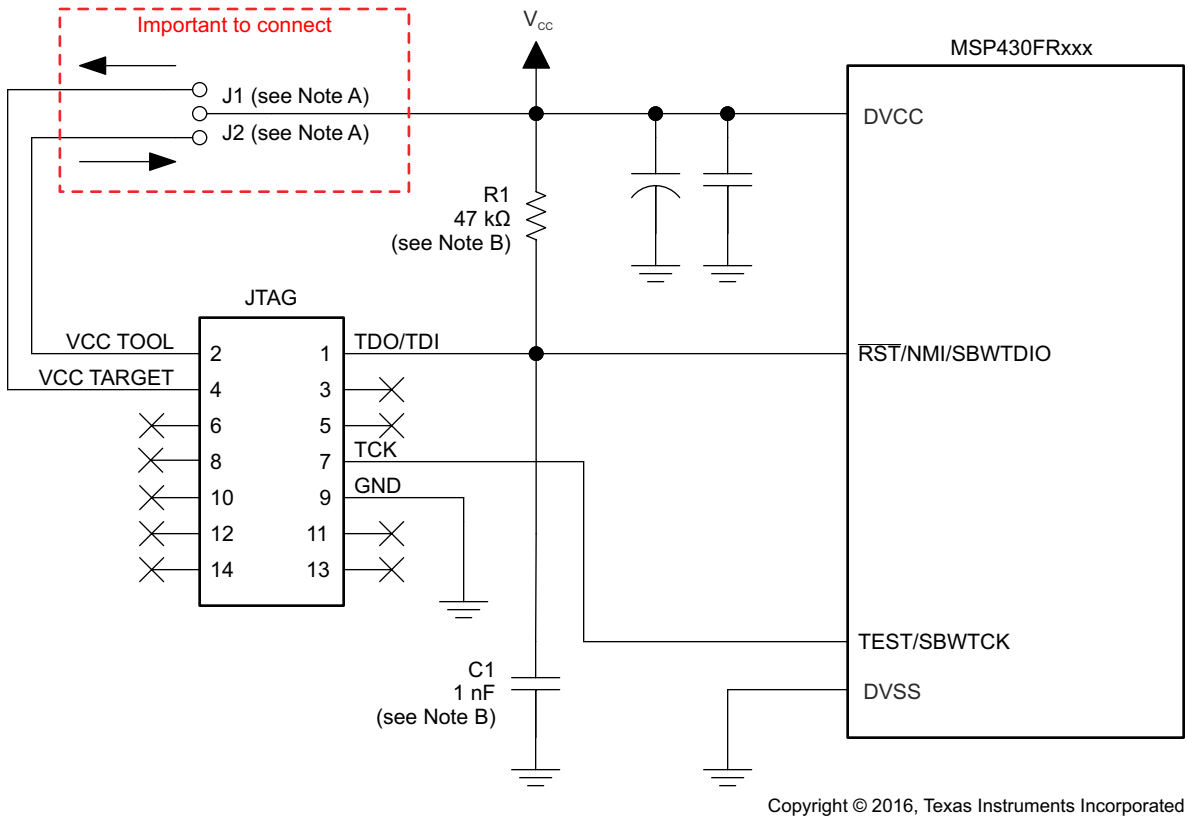
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A. If a local target power supply is used, make connection J1. If power from the debug or programming adapter is used, make connection J2.

B. The upper limit for C1 is 1.1 nF when using current TI tools.

図 10-3. Signal Connections for 4-Wire JTAG Communication

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A. Make connection J1 if a local target power supply is used, or make connection J2 if the target is powered from the debug or programming adapter.

B. The device RST/NMI/SBWTDIO pin is used in 2-wire mode for bidirectional communication with the device during JTAG access, and any capacitance that is attached to this signal may affect the ability to establish a connection with the device. The upper limit for C1 is 1.1 nF when using current TI tools.

図 10-4. Signal Connections for 2-Wire JTAG Communication (Spy-Bi-Wire)

10.1.4 Reset

The reset pin can be configured as a reset function (default) or as an NMI function in the Special Function Register (SFR), SFRRPCR.

In reset mode, the RST/NMI pin is active low, and a pulse applied to this pin that meets the reset timing specifications generates a BOR-type device reset.

Setting SYSNMI causes the RST/NMI pin to be configured as an external NMI source. The external NMI is edge sensitive, and its edge is selectable by SYSNMIIES. Setting the NMIIE enables the interrupt of the external NMI. When an external NMI event occurs, the NMIIFG is set.

The RST/NMI pin can have either a pullup or pulldown that is enabled or not. SYSRSTUP selects either pullup or pulldown, and SYSRSTRE causes the pullup (default) or pulldown to be enabled (default) or not. If the RST/NMI pin is unused, it is required either to select and enable the internal pullup or to connect an external 47-kΩ pullup resistor to the RST/NMI pin with a 10-nF pulldown capacitor. The pulldown capacitor should not exceed 1.1 nF when using devices with Spy-Bi-Wire interface in Spy-Bi-Wire mode or in 4-wire JTAG mode with TI tools like FET interfaces or GANG programmers.

See the *MSP430FR4xx and MSP430FR2xx Family User's Guide* for more information on the referenced control registers and bits.

10.1.5 Unused Pins

For details on the connection of unused pins, see セクション 7.5.

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10.1.6 General Layout Recommendations

- Proper grounding and short traces for external crystal to reduce parasitic capacitance. See *MSP430 32-kHz Crystal Oscillators* for recommended layout guidelines.
- Proper bypass capacitors on DVCC, AVCC, and reference pins if used.
- Avoid routing any high-frequency signal close to an analog signal line. For example, keep digital switching signals such as PWM or JTAG signals away from the oscillator circuit and ADC signals.
- Proper ESD level protection should be considered to protect the device from unintended high-voltage electrostatic discharge. See *MSP430 System-Level ESD Considerations* for guidelines.

10.1.7 Do's and Don'ts

During power up, power down, and device operation, the voltage difference between AVCC and DVCC must not exceed the limits specified in セクション 8.1. Exceeding the specified limits may cause malfunction of the device including erroneous writes to RAM and FRAM.

10.2 Peripheral- and Interface-Specific Design Information

10.2.1 ADC Peripheral

注

The ADC is not available on the MSP430FR2000 device.

10.2.1.1 Partial Schematic

図 10-5 shows the recommended decoupling circuit with either an internal or an external voltage reference.

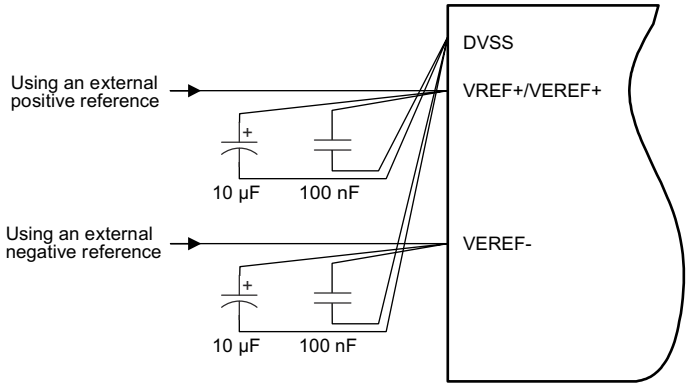


図 10-5. ADC Grounding and Noise Considerations

10.2.1.2 Design Requirements

As with any high-resolution ADC, appropriate printed-circuit-board layout and grounding techniques should be followed to eliminate ground loops, unwanted parasitic effects, and noise.

Ground loops are formed when return current from the ADC flows through paths that are common with other analog or digital circuitry. If care is not taken, this current can generate small unwanted offset voltages that can add to or subtract from the reference or input voltages of the ADC. The general guidelines in セクション 10.1.1 combined with the connections shown in セクション 10.2.1.1 prevent this.

In addition to grounding, ripple and noise spikes on the power-supply lines that are caused by digital switching or switching power supplies can corrupt the conversion result. TI recommends a noise-free design using separate analog and digital ground planes with a single-point connection to achieve high accuracy.

図 10-5 shows the recommended decoupling circuit when an external voltage reference is used. The internal reference module has a maximum drive current as described in the sections *ADC Pin Enable* and *1.2-V Reference Settings* of the *MSP430FR4xx and MSP430FR2xx Family User's Guide*.

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The reference voltage must be a stable voltage for accurate measurements. The capacitor values that are selected in the general guidelines filter out the high- and low-frequency ripple before the reference voltage enters the device. In this case, the 10-µF capacitor buffers the reference pin and filters low-frequency ripple. A 100-nF bypass capacitor filters out high-frequency noise.

10.2.1.3 Layout Guidelines

Components that are shown in the partial schematic (see 図 10-5) should be placed as close as possible to the respective device pins to avoid long traces, because they add additional parasitic capacitance, inductance, and resistance on the signal.

Avoid routing analog input signals close to a high-frequency pin (for example, a high-frequency PWM), because the high-frequency switching can be coupled into the analog signal.

10.3 Typical Applications

表 10-1 lists reference designs that reflect the use of the MSP430FR211x family of devices in different real-world application scenarios. Consult these designs for additional guidance regarding schematic, layout, and software implementation. For the most up-to-date list of available reference designs, see the device-specific product folders or visit TI reference designs.

表 10-1. Reference Designs

DESIGN NAME	LINK
Thermostat Implementation With MSP430FR4xx	TIDM-FRAM-THERMOSTAT
Water Meter Implementation With MSP430FR4xx	TIDM-FRAM-WATERMETER
Remote Controller of Air Conditioner Using Low-Power Microcontroller	TIDM-REMOTE-CONTROLLER-FOR-AC

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11 Device and Documentation Support

11.1 Getting Started

For more information on the MSP430™ family of devices and the tools and libraries that are available to help with your development, visit the MSP430 ultra-low-power sensing & measurement MCUs overview.

11.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of all MSP MCU devices. Each MSP MCU commercial family member has one of two prefixes: MSP or XMS. These prefixes represent evolutionary stages of product development from engineering prototypes (XMS) through fully qualified production devices (MSP).

XMS – Experimental device that is not necessarily representative of the final device's electrical specifications

MSP – Fully qualified production device

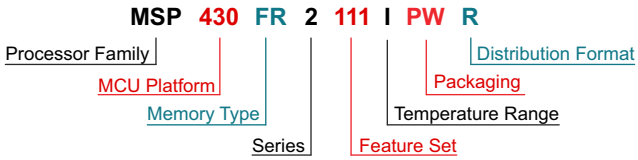
XMS devices are shipped against the following disclaimer:

"Developmental product is intended for internal evaluation purposes."

MSP devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (XMS) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the temperature range, package type, and distribution format. 図 11-1 provides a legend for reading the complete device name.



Processor Family	MSP = Mixed-Signal Processor XMS = Experimental Silicon
MCU Platform	430 = TI's 16-bit MSP430 Low-Power Microcontroller Platform
Memory Type	FR = FRAM
Series	2 = FRAM 2 Series up to 16 MHz without LCD
Feature Set	Variations of the device features; see the Device Comparison section for details
Temperature Range	I = –40°C to 85°C
Packaging	www.ti.com/packaging
Distribution Format	T = Small reel R = Large reel No marking = Tube or tray

図 11-1. Device Nomenclature

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11.3 Tools and Software

All MSP microcontrollers are supported by a wide variety of software and hardware development tools. Tools are available from TI and various third parties. See them all at Development Kits and Software for Low-Power MCUs.

表 11-1 lists the debug features of the MSP430FR211x microcontrollers. See the *Code Composer Studio IDE for MSP430 MCUs User's Guide* for details on the available features.

表 11-1. Hardware Debug Features

MSP430 ARCHITECTURE	4-WIRE JTAG	2-WIRE JTAG	BREAK-POINTS (N)	RANGE BREAK-POINTS	CLOCK CONTROL	STATE SEQUENCER	TRACE BUFFER	LPMx.5 DEBUGGING SUPPORT	EEM VERSION
MSP430Xv2	Yes	Yes	3	Yes	Yes	No	No	No	S

Design Kits and Evaluation Modules

20-pin Target Socket Development Board for MSP430FR23x/21x MCUs

The MSP-TS430PW20 is a stand-alone ZIF socket target board used to program and debug the MSP430 MCU in system through the JTAG interface or the Spy Bi-Wire (2-wire JTAG) protocol. The development board supports all MSP430FR2000, MSP430FR21x, and MSP430FR23x FRAM MCUs in a 20-pin or 16-pin TSSOP package (TI package code: PW).

MSP430FR2311 LaunchPad Development Kit

The MSP-EXP430FR2311 LaunchPad development kit is a microcontroller development board for the MSP430FR2000, MSP430FR21x, and MSP430FR23x MCU families. This kit contains everything needed to evaluate the platform, including onboard emulation for programming, debugging, and energy measurements. The onboard buttons and LEDs allow for integration of simple user interaction.

MSP430FR4133 LaunchPad Development Kit

The MSP-EXP430FR4133 LaunchPad development kit is a microcontroller development board for the MSP430FR2xx and MSP430FR4xx MCU family. This kit contains everything needed to evaluate the MSP430FR2xx and MSP430FR4xx FRAM platform, including onboard emulation for programming, debugging, and energy measurements. The onboard buttons and LEDs allow for integration of simple user interaction, while the 20-pin header for BoosterPack™ plug-in modules allows for the use of BoosterPack modules for quick user experimentation.

MSP-FET and MSP-TS430PW20 FRAM Microcontroller Development Kit Bundle

The MSP-FET430U20 bundle combines two debugging tools that support the 20-pin PW package for the MSP430FR2000, MSP430FR21xx and MSP430FR23xx MCUs (for example, MSP430FR2311IPW20). The included tools are MSP-TS430PW20 and MSP-FET.

Software

MSP430Ware™ Software

MSP430Ware software is a collection of code examples, data sheets, and other design resources for all MSP430 devices, delivered in a convenient package. In addition to providing a complete collection of existing MSP430 design resources, MSP430Ware software also includes a high-level API called MSP Driver Library. This library makes it easy to program MSP430 hardware. MSP430Ware software is available as a component of CCS or as a stand-alone package.

MSP430FR21xx Code Examples

C code examples are available for every MSP device that configures each of the integrated peripherals for various application needs.

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MSP Driver Library

The abstracted API of MSP Driver Library provides easy-to-use function calls that free you from directly manipulating the bits and bytes of the MSP430 hardware. Thorough documentation is delivered through a helpful API Guide, which includes details on each function call and the recognized parameters. Developers can use Driver Library functions to write complete projects with minimal overhead.

ULP (Ultra-Low Power) Advisor

ULP Advisor™ software is a tool for guiding developers to write more efficient code to fully use the unique ultra-low-power features of MSP and MSP432 microcontrollers. Aimed at both experienced and new microcontroller developers, ULP Advisor checks your code against a thorough ULP checklist to help minimize the energy consumption of your application. At build time, ULP Advisor provides notifications and remarks to highlight areas of your code that can be further optimized for lower power.

IEC60730 Software Package

The IEC60730 MSP430 software package was developed to help customers comply with IEC 60730-1:2010 (Automatic Electrical Controls for Household and Similar Use – Part 1: General Requirements) for up to Class B products, which includes home appliances, arc detectors, power converters, power tools, e-bikes, and many others. The IEC60730 MSP430 software package can be embedded in customer applications running on MSP430s to help simplify the customer's certification efforts of functional safety-compliant consumer devices to IEC 60730-1:2010 Class B.

Fixed Point Math Library for MSP

The MSP IQmath and Qmath Libraries are a collection of highly optimized and high-precision mathematical functions for C programmers to seamlessly port a floating-point algorithm into fixed-point code on MSP430 and MSP432 devices. These routines are typically used in computationally intensive real-time applications where optimal execution speed, high accuracy, and ultra-low energy are critical. By using the IQmath and Qmath libraries, it is possible to achieve execution speeds considerably faster and energy consumption considerably lower than equivalent code written using floating-point math.

Floating Point Math Library for MSP430

Continuing to innovate in the low-power and low-cost microcontroller space, TI provides MSPMATHLIB. Leveraging the intelligent peripherals of our devices, this floating-point math library of scalar functions that are up to 26 times faster than the standard MSP430 math functions. Mathlib is easy to integrate into your designs. This library is free and is integrated in both Code Composer Studio IDE and IAR Embedded Workbench IDE.

Development Tools

Code Composer Studio™ Integrated Development Environment for MSP Microcontrollers

Code Composer Studio (CCS) integrated development environment (IDE) supports all MSP microcontroller devices. CCS comprises a suite of embedded software utilities used to develop and debug embedded applications. It includes an optimizing C/C++ compiler, source code editor, project build environment, debugger, profiler, and many other features.

MSP EnergyTrace™ Technology

EnergyTrace technology for MSP430 microcontrollers is an energy-based code analysis tool that measures and displays the energy profile of the application and helps to optimize it for ultra-low-power consumption.

Command-Line Programmer

MSP Flasher is an open-source shell-based interface for programming MSP microcontrollers through a FET programmer or eZ430 using JTAG or Spy-Bi-Wire (SBW) communication. MSP Flasher can download binary files (.txt or .hex) directly to the MSP microcontroller without an IDE.

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MSP MCU Programmer and Debugger

The MSP-FET is a powerful emulation development tool – often called a debug probe – which lets users quickly begin application development on MSP low-power MCUs. Creating MCU software usually requires downloading the resulting binary program to the MSP device for validation and debugging.

MSP-GANG Production Programmer

The MSP Gang Programmer is an MSP430 or MSP432 device programmer that can program up to eight identical MSP430 or MSP432 flash or FRAM devices at the same time. The MSP Gang Programmer connects to a host PC using a standard RS-232 or USB connection and provides flexible programming options that let the user fully customize the process.

11.4 Documentation Support

The following documents describe the MSP430FR211x microcontrollers. Copies of these documents are available on the Internet at www.ti.com.

Receiving Notification of Document Updates

To receive notification of documentation updates—including silicon errata—go to the product folder for your device on ti.com (for example https://www.ti.com/product/MSP430FR2111). In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

Errata

MSP430FR2111 Microcontroller Errata

Describes the known exceptions to the functional specifications.

MSP430FR2110 Microcontroller Errata

Describes the known exceptions to the functional specifications.

MSP430FR2100 Microcontroller Errata

Describes the known exceptions to the functional specifications.

MSP430FR2000 Microcontroller Errata

Describes the known exceptions to the functional specifications.

User's Guides

MSP430FR4xx and MSP430FR2xx Family User's Guide

Detailed information on the modules and peripherals available in this device family.

MSP430 FRAM Device Bootloader (BSL) User's Guide

The bootloader (BSL) on MSP430 MCUs lets users communicate with embedded memory in the MSP430 MCU during the prototyping phase, final production, and in service. Both the programmable memory (FRAM) and the data memory (RAM) can be modified as required.

MSP430 Programming With the JTAG Interface

This document describes the functions that are required to erase, program, and verify the memory module of the MSP430 flash-based and FRAM-based microcontroller families using the JTAG communication port. In addition, it describes how to program the JTAG access security fuse that is available on all MSP430 devices. This document describes device access using both the standard 4-wire JTAG interface and the 2-wire JTAG interface, which is also referred to as Spy-Bi-Wire (SBW).

MSP430 Hardware Tools User's Guide

This manual describes the hardware of the TI MSP-FET430 Flash Emulation Tool (FET). The FET is the program development tool for the MSP430 ultra-low-power microcontroller.

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Application Reports

MSP430 FRAM Technology – How To and Best Practices

FRAM is a nonvolatile memory technology that behaves similar to SRAM while enabling a whole host of new applications, but also changing the way firmware should be designed. This application report outlines the how to and best practices of using FRAM technology in MSP430 from an embedded software development perspective. It discusses how to implement a memory layout according to application-specific code, constant, data space requirements, and the use of FRAM to optimize application energy consumption.

VLO Calibration on the MSP430FR4xx and MSP430FR2xx Family

MSP430FR4xx and MSP430FR2xx (FR4xx/FR2xx) family microcontrollers (MCUs) provide various clock sources, including some high-speed high-accuracy clocks and some low-power low-system-cost clocks. Users can select the best balance of performance, power consumption, and system cost. The on-chip very low-frequency oscillator (VLO) is a clock source with 10-kHz typical frequency included in FR4xx/FR2xx family MCUs. The VLO is widely used in a range of applications because of its ultra-low power consumption.

MSP430 32-kHz Crystal Oscillators

Selection of the right crystal, correct load circuit, and proper board layout are important for a stable crystal oscillator. This application report summarizes crystal oscillator function and explains the parameters to select the correct crystal for MSP430 ultra-low-power operation. In addition, hints and examples for correct board layout are given. The document also contains detailed information on the possible oscillator tests to ensure stable oscillator operation in mass production.

MSP430 System-Level ESD Considerations

System-level ESD has become increasingly demanding with silicon technology scaling towards lower voltages and the need for designing cost-effective and ultra-low-power components. This application report addresses different ESD topics to help board designers and OEMs understand and design robust system-level designs.

11.5 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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11.6 Trademarks

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11.7 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.8 用語集

テキサス・インスツルメンツ用語集　この用語集には、用語や略語の一覧および定義が記載されています。

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
MSP430FR2000IPW16	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FR2000	Samples
MSP430FR2000IPW16R	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FR2000	Samples
MSP430FR2000IRLLR	ACTIVE	VQFN	RLL	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FR2000	Samples
MSP430FR2000IRLLT	ACTIVE	VQFN	RLL	24	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FR2000	Samples
MSP430FR2100IPW16	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FR2100	Samples
MSP430FR2100IPW16R	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FR2100	Samples
MSP430FR2100IRLLR	ACTIVE	VQFN	RLL	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FR2100	Samples
MSP430FR2100IRLLT	ACTIVE	VQFN	RLL	24	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FR2100	Samples
MSP430FR2110IPW16	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FR2110	Samples
MSP430FR2110IPW16R	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FR2110	Samples
MSP430FR2110IRLLR	ACTIVE	VQFN	RLL	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FR2110	Samples
MSP430FR2110IRLLT	ACTIVE	VQFN	RLL	24	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FR2110	Samples
MSP430FR2111IPW16	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FR2111	Samples
MSP430FR2111IPW16R	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	FR2111	Samples
MSP430FR2111IRLLR	ACTIVE	VQFN	RLL	24	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FR2111	Samples
MSP430FR2111IRLLT	ACTIVE	VQFN	RLL	24	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	FR2111	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

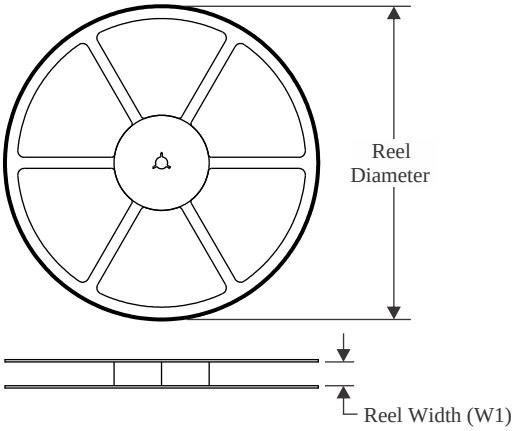
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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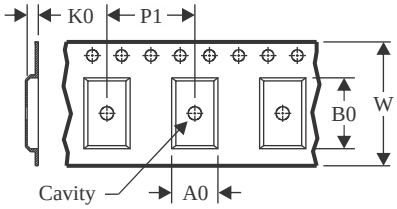
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

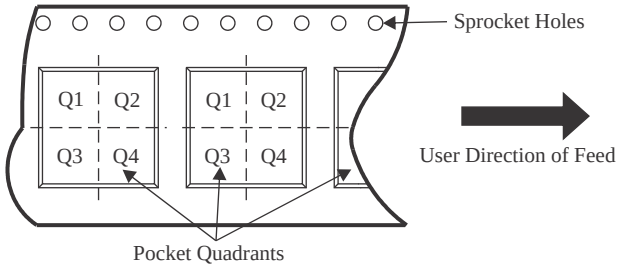


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

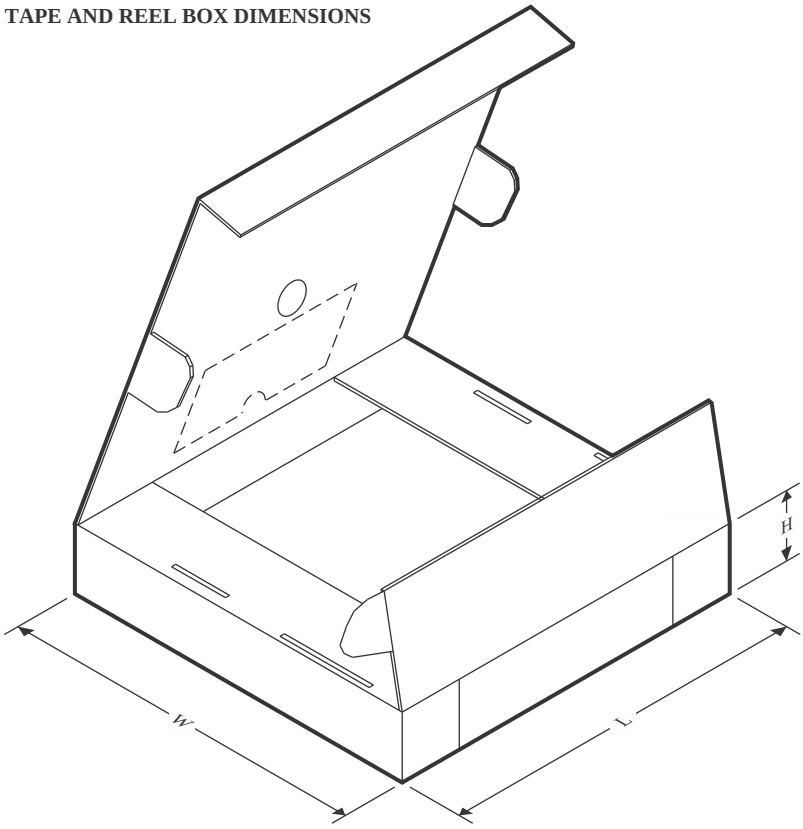
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
MSP430FR2000IPW16R	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430FR2000IRLLR	VQFN	RLL	24	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
MSP430FR2000IRLLT	VQFN	RLL	24	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
MSP430FR2100IPW16R	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430FR2100IRLLR	VQFN	RLL	24	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
MSP430FR2100IRLLT	VQFN	RLL	24	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
MSP430FR2110IPW16R	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430FR2110IRLLR	VQFN	RLL	24	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
MSP430FR2110IRLLT	VQFN	RLL	24	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
MSP430FR2111IPW16R	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
MSP430FR2111IRLLR	VQFN	RLL	24	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
MSP430FR2111IRLLT	VQFN	RLL	24	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

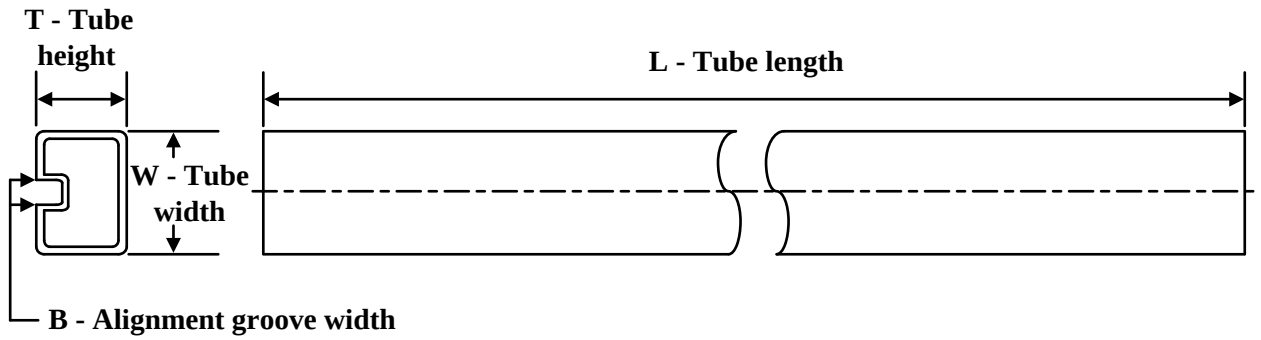
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
MSP430FR2000IPW16R	TSSOP	PW	16	2000	350.0	350.0	43.0
MSP430FR2000IRLLR	VQFN	RLL	24	3000	367.0	367.0	35.0
MSP430FR2000IRLLT	VQFN	RLL	24	250	210.0	185.0	35.0
MSP430FR2100IPW16R	TSSOP	PW	16	2000	350.0	350.0	43.0
MSP430FR2100IRLLR	VQFN	RLL	24	3000	367.0	367.0	35.0
MSP430FR2100IRLLT	VQFN	RLL	24	250	210.0	185.0	35.0
MSP430FR2110IPW16R	TSSOP	PW	16	2000	350.0	350.0	43.0
MSP430FR2110IRLLR	VQFN	RLL	24	3000	367.0	367.0	35.0
MSP430FR2110IRLLT	VQFN	RLL	24	250	210.0	185.0	35.0
MSP430FR2111IPW16R	TSSOP	PW	16	2000	350.0	350.0	43.0
MSP430FR2111IRLLR	VQFN	RLL	24	3000	367.0	367.0	35.0
MSP430FR2111IRLLT	VQFN	RLL	24	250	210.0	185.0	35.0

TUBE



*All dimensions are nominal

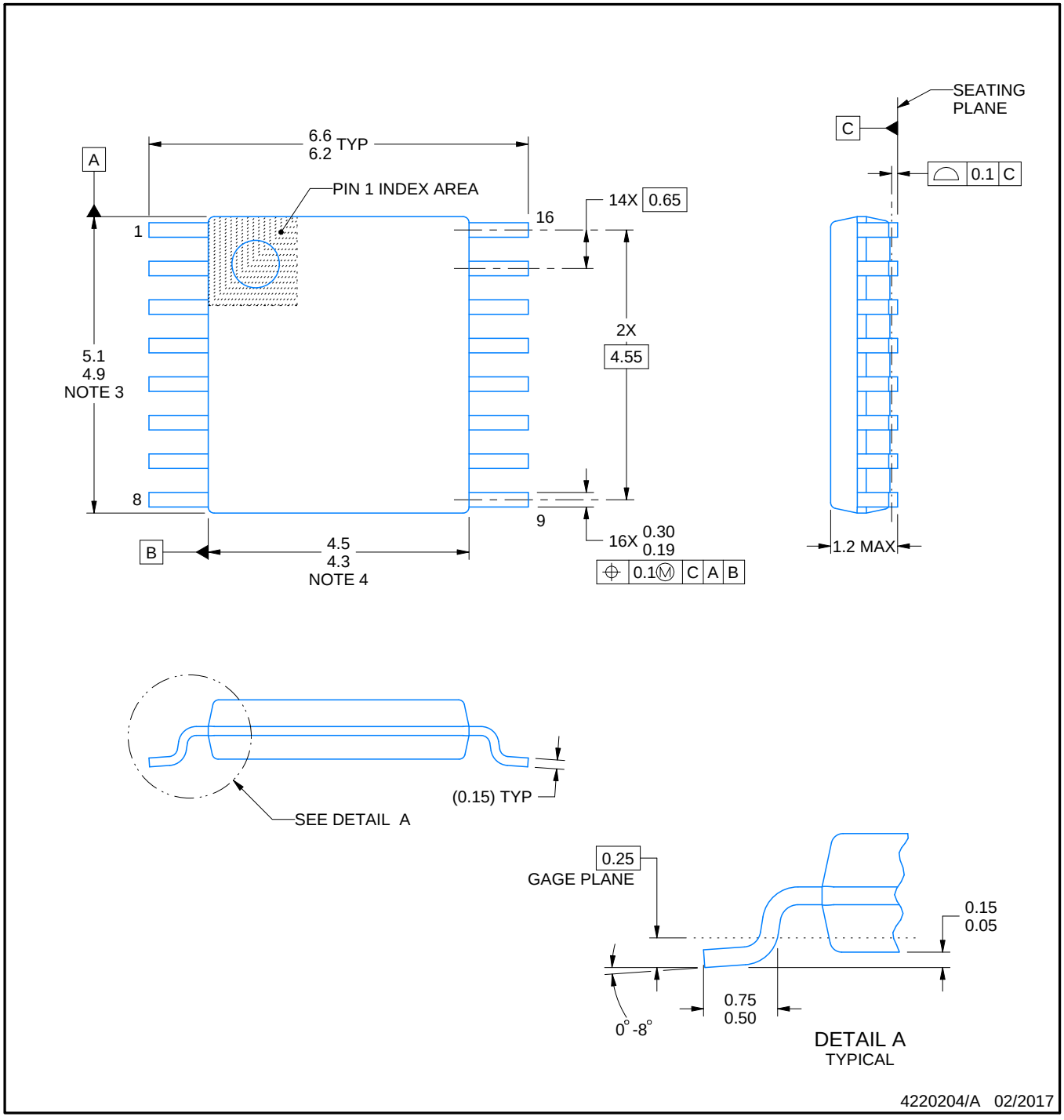
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
MSP430FR2000IPW16	PW	TSSOP	16	90	530	10.2	3600	3.5
MSP430FR2100IPW16	PW	TSSOP	16	90	530	10.2	3600	3.5
MSP430FR2110IPW16	PW	TSSOP	16	90	530	10.2	3600	3.5
MSP430FR2111IPW16	PW	TSSOP	16	90	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0016A

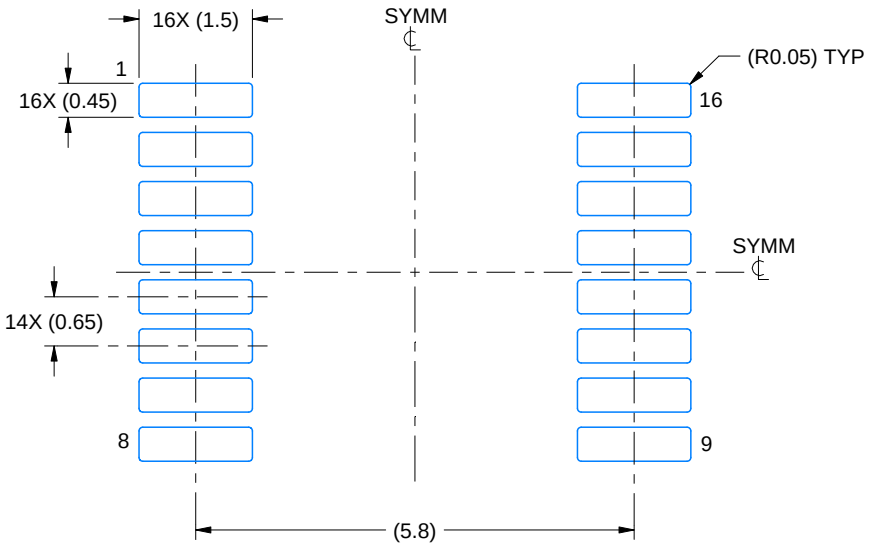
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

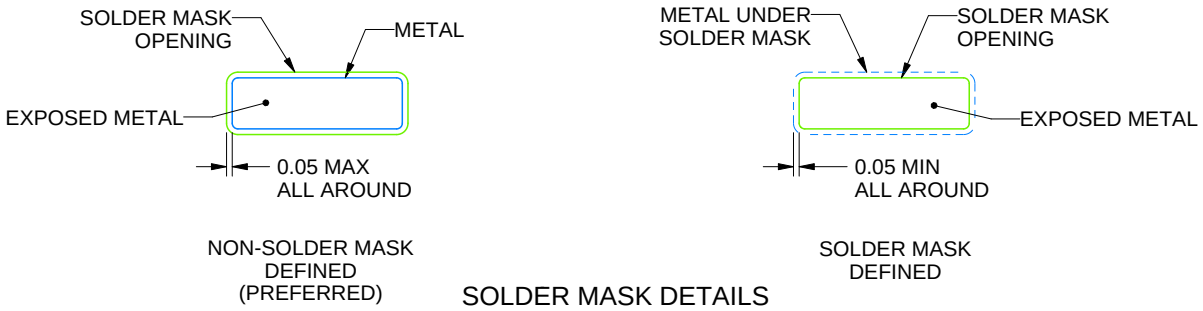


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

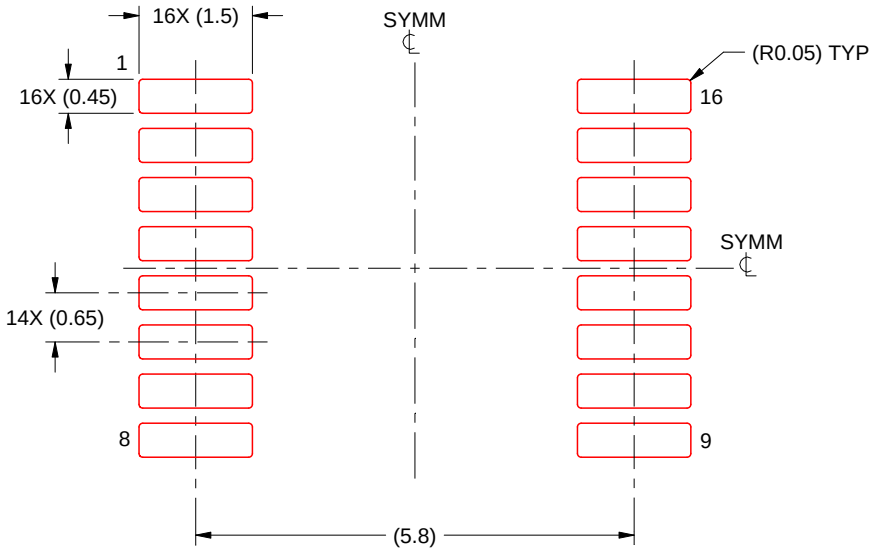


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



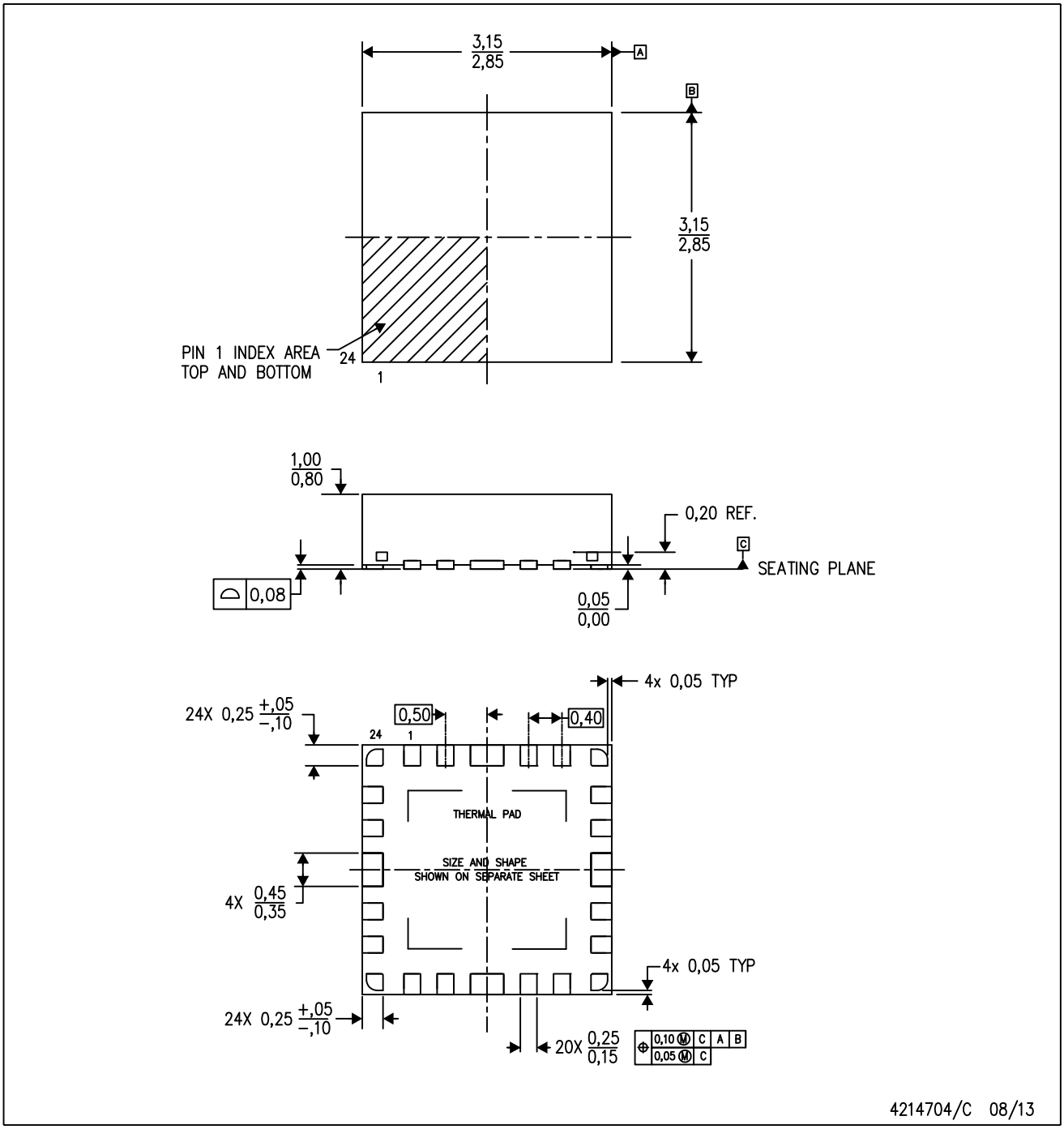
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RLL (S–PVQFN–N24) PLASTIC QUAD FLATPACK NO–LEAD



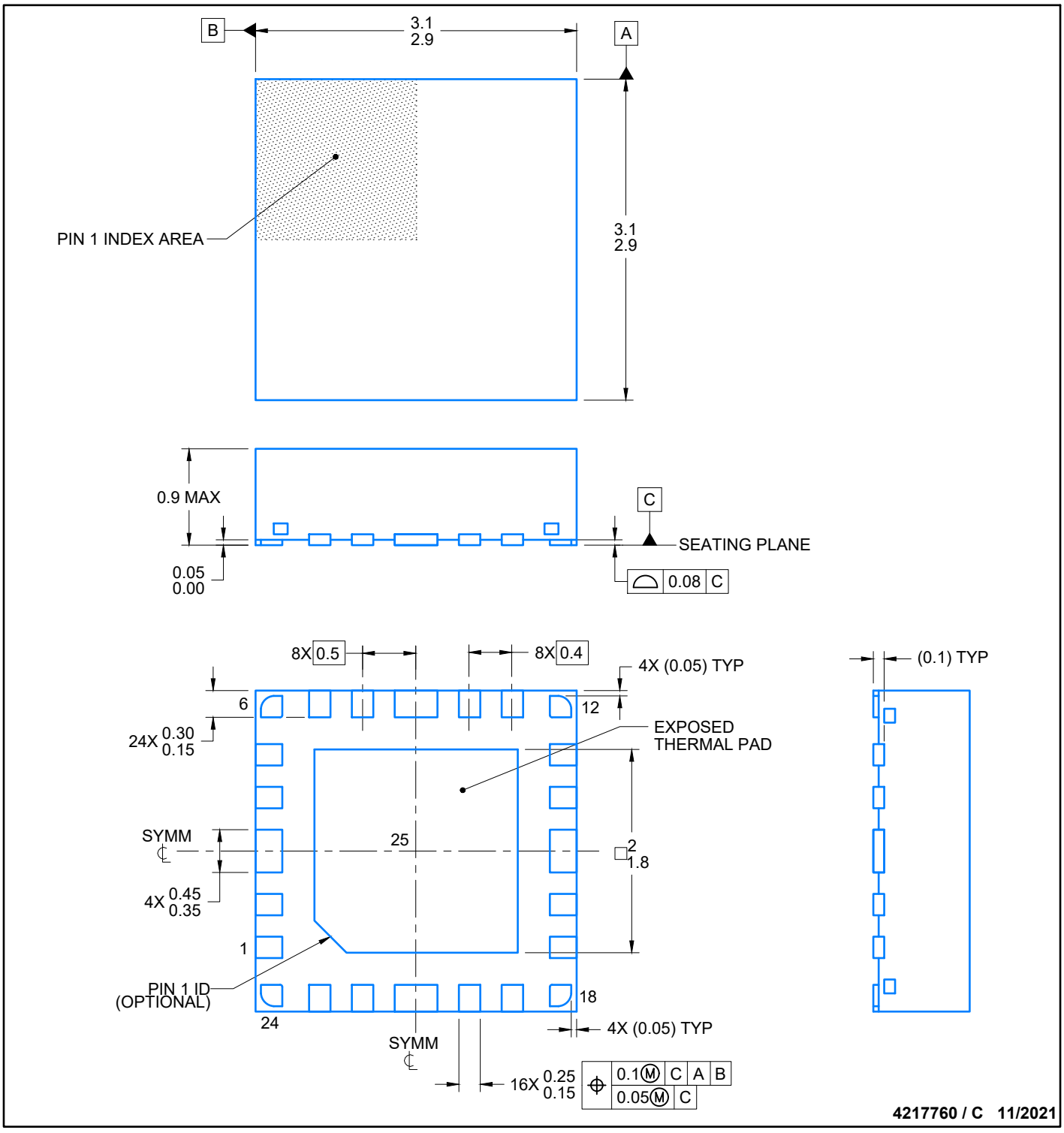
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Quad Flatpack, No–leads (QFN) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

PACKAGE OUTLINE

RLL0024A

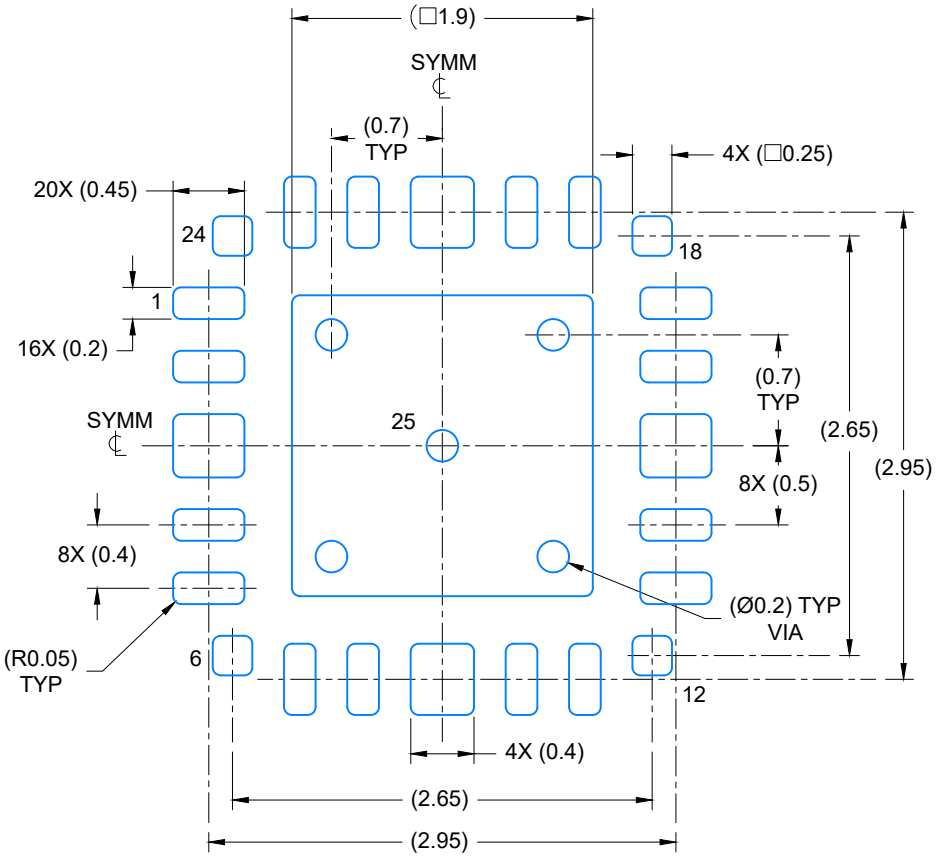
VQFN - 0.9 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



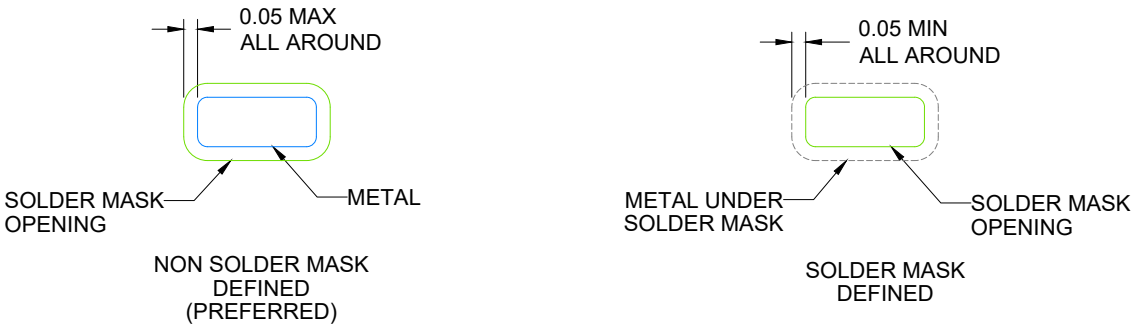
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE

SCALE: 20X

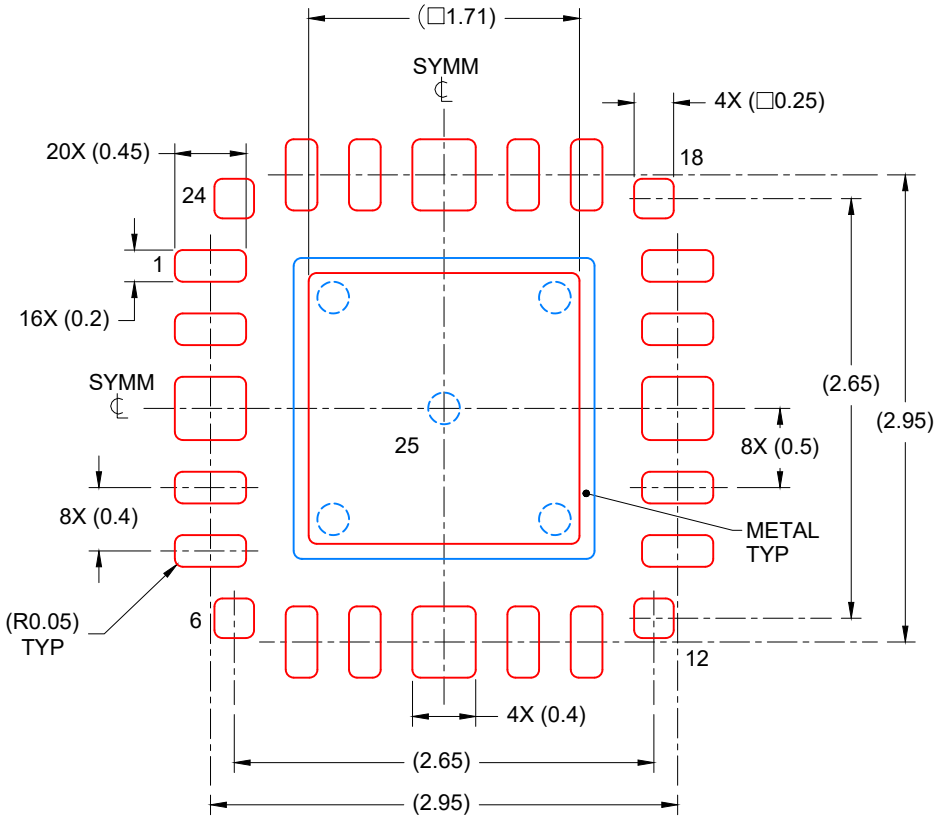


SOLDER MASK DETAILS

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NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD
81% PRINTED COVERAGE BY AREA
SCALE: 20X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations..

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