

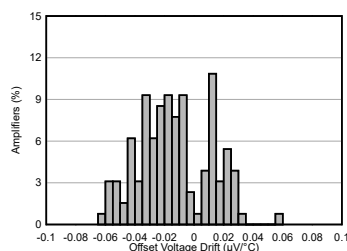
OPAx205 4 μ V、0.08 μ V/°C、低消費電力、スーパー・ベータ、バイポーラ e-trim[™] オペアンプ

1 特長

- e-trim[™] オペアンプの性能
 - 低いオフセット電圧: 25 μ V (最大値)、15 μ V (最大値、高グレード)
 - 低いオフセット電圧ドリフト: $\pm 0.5\mu$ V/°C (標準値)、 $\pm 0.2\mu$ V/°C (最大値、高グレード)
- スーパー・ベータ入力
 - 入力バイアス電流: 500pA (最大値)
 - 入力電流ノイズ: 110fA/ $\sqrt{\text{Hz}}$
- 低ノイズ
 - 0.1~10Hz: 0.2 μ V_{PP}
 - 電圧ノイズ: 7.2nV/ $\sqrt{\text{Hz}}$
- A_{OL}、CMRR、PSRR: 126dB 超 (全温度範囲)
- ゲイン帯域幅積: 3.6MHz
- 低い静止電流: 240 μ A (最大値)
- スルーレート: 4V/ μ s
- 過負荷電力制限
- レール・ツー・レール出力
- EMI および RFI フィルタ入力
- 広い電源範囲: 4.5V~36V
- 温度範囲: -40°C~+125°C
- 標準グレード (OPAx205A) および高グレード (OPA2205、プレビュー) で供給
- OPA206 と OPA2206 は ± 40 V の過電圧保護機能を備えています

2 アプリケーション

- 流量トランスミッタ
- ストリング・インバータ
- データ・アキュイジション (DAQ)
- ソース・メジャー・ユニット (SMU)
- 実験室およびフィールド計測
- バッテリー試験装置
- アナログ入力モジュール
- 圧力トランスミッタ



OPAx205 のオフセット電圧ドリフト

3 概要

OPA205、OPA2205、OPA4205 (OPAx205) は、業界標準の OPAx277 ファミリの次世代製品です。OPA206 および OPA2206 は、同じオペアンプ・コアを持つ関連デバイスですが、電源電圧を ± 40 V 超過する入力過電圧保護の追加機能を備えています。これらのデバイスは、スーパー・ベータ入力を備えた高精度バイポーラ e-trim[™] オペアンプです。テキサス・インスツルメンツ独自のトリミング技術は、 $\pm 4\mu$ V ($\pm 2\mu$ V、高グレード) の標準的な入力オフセット電圧と、 $\pm 0.08\mu$ V ($\pm 0.04\mu$ V、高グレード) の標準的な入力オフセット電圧ドリフトを実現するために使用されています。

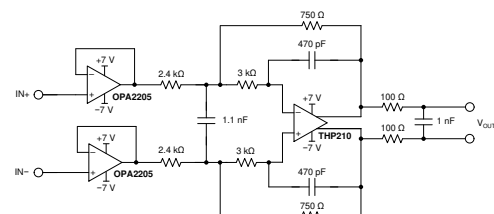
バイポーラ・プロセスで設計された OPAx205 は、わずか 220 μ A の静止電流に対して 3.6MHz のゲイン帯域幅を備えています。このデバイスは、1kHz においてわずか 7.2nV/ $\sqrt{\text{Hz}}$ という低電圧ノイズ密度も達成しています。スーパー・ベータ入力により、OPAx205 は、100pA (標準値) の非常に小さい入力バイアス電流と 110fA/ $\sqrt{\text{Hz}}$ の電流ノイズ密度を実現しています。

高い性能を備えた OPAx205 は、流量および圧力トランスミッタ、携帯型データ・アキュイジション (DAQ) システム、高密度ソース・メジャー・ユニット (SMU) など、高精度と低消費電力を必要とするシステムに最適です。

製品情報

部品番号	チャネル	パッケージ ⁽¹⁾
OPA205	シングル	D (SOIC, 8)
OPA2205 ⁽²⁾	デュアル	D (SOIC, 8)
	デュアル	DGK (VSSOP, 8)
OPA4205	クワッド	D (SOIC, 14)
	クワッド	PW (TSSOP, 14)

- 利用可能なパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。
- 高グレード・バージョンは、プレビューです (量産データではありません)。



OPA2205 の代表的なアプリケーション



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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (December 2022) to Revision F (March 2023)	Page
• 標準グレードのデバイス仕様に合わせてタイトルを変更.....	1
• OPA2205 D (SOIC, 8) パッケージと関連する内容を量産データとして追加.....	1
• OPA4205 D (SOIC, 14) パッケージと関連する内容を量産データとして追加.....	1
• Changed maximum input bias from $\pm 0.4\text{ nA}$ to $\pm 0.5\text{ nA}$	21
• Changed offset and offset drift values to match standard-grade device specifications in <i>Detailed Design Description</i>	26
• Changed Figure 9-6 to show correct V_{S+} connection.....	29

Changes from Revision D (September 2022) to Revision E (December 2022)	Page
• OPA4205 TSSOP パッケージと関連する内容を量産データとして追加.....	1
• Changed typical input offset voltage from $8\text{ }\mu\text{V}$ to $4\text{ }\mu\text{V}$ in <i>Electrical Characteristics</i>	8
• Changed maximum input offset voltage from $50\text{ }\mu\text{V}$ to $25\text{ }\mu\text{V}$ in <i>Electrical Characteristics</i>	8
• Changed maximum input offset voltage over temperature from $80\text{ }\mu\text{V}$ to $55\text{ }\mu\text{V}$ in <i>Electrical Characteristics</i>	8
• Changed typical input offset voltage from $8\text{ }\mu\text{V}$ to $4\text{ }\mu\text{V}$ in <i>Electrical Characteristics</i>	10
• Changed maximum input offset voltage from $50\text{ }\mu\text{V}$ to $25\text{ }\mu\text{V}$ in <i>Electrical Characteristics</i>	10
• Changed maximum input offset voltage over temperature from $80\text{ }\mu\text{V}$ to $55\text{ }\mu\text{V}$ in <i>Electrical Characteristics</i>	10

Changes from Revision C (July 2022) to Revision D (September 2022)	Page
• OPA205 (SOIC) をプレビューから量産データ (アクティブ) に変更.....	1

Changes from Revision B (August 2021) to Revision C (July 2022)	Page
• OPA205 D (SOIC) パッケージを事前情報 (プレビュー) として追加.....	1

Changes from Revision A (May 2021) to Revision B (August 2021)	Page
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- | | |
|---|----|
| <ul style="list-style-type: none"> • Changed Figure 6-22, <i>Voltage Noise Density vs Frequency</i>, to show voltage noise density instead of current noise density..... | 12 |
|---|----|
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Changes from Revision * (April 2020) to Revision A (May 2021)	Page
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- | | |
|--|-------------|
| <ul style="list-style-type: none"> • 文書全体にわたって表、図、相互参照の採番方法を更新..... • OPA2205 を事前情報 (プレビュー) から量産データ (アクティブ) に変更..... • Changed both <i>Electrical Characteristics</i> tables to show differentiated performance between OPA2205 (high grade) and OPA2205A (standard grade)..... | 1
1
8 |
|--|-------------|
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5 Pin Configuration and Functions

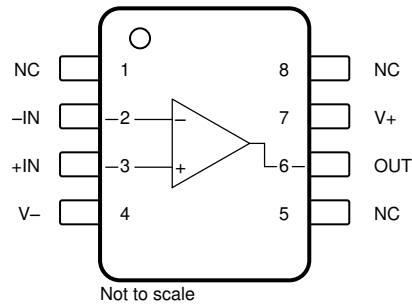


图 5-1. OPA205 D Package, 8-Pin SOIC (Top View)

表 5-1. Pin Functions: OPA205

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN	3	Input	Noninverting input
-IN	2	Input	Inverting input
NC	1, 5, 8	—	No internal connection (can be left floating)
OUT	6	Output	Output
V+	7	—	Positive (highest) power supply
V-	4	—	Negative (lowest) power supply

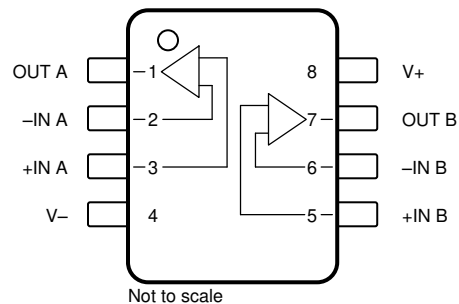
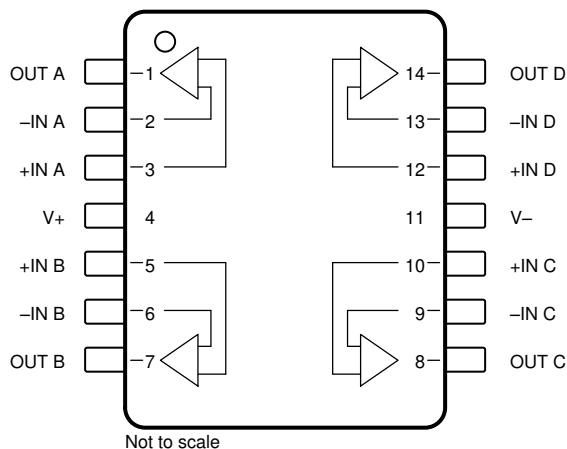


图 5-2. OPA2205 DGK Package, 8-Pin VSSOP and D Package, 8-pin SOIC (Top View)

表 5-2. Pin Functions: OPA2205

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
-IN A	2	Input	Inverting input, channel A
+IN B	5	Input	Noninverting input, channel B
-IN B	6	Input	Inverting input, channel B
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
V+	8	—	Positive (highest) power supply
V-	4	—	Negative (lowest) power supply



✎ 5-3. OPA4205 PW Package, 14-Pin TSSOP and D Package, 14-Pin SOIC (Top View)

Pin Functions: OPA4205

PIN		TYPE	DESCRIPTION
NAME	NO.		
+IN A	3	Input	Noninverting input, channel A
+IN B	5	Input	Noninverting input, channel B
+IN C	10	Input	Noninverting input, channel C
+IN D	12	Input	Noninverting input, channel D
-IN A	2	Input	Inverting input, channel A
-IN B	6	Input	Inverting input, channel B
-IN C	9	Input	Inverting input, channel C
-IN D	13	Input	Inverting input, channel D
OUT A	1	Output	Output, channel A
OUT B	7	Output	Output, channel B
OUT C	8	Output	Output, channel C
OUT D	14	Output	Output, channel D
V+	4	—	Positive (highest) power supply
V-	11	—	Negative (lowest) power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

			MIN	MAX	UNIT
V _S	Supply voltage, V _S = (V ₊) – (V _–)	Single supply		40	V
		Dual supply		±20	
	Signal input pin voltage	Common-mode	(V _–) – 0.5	(V ₊) + 0.5	V
		Differential		±0.5	
	Signal input pin current			±10	mA
	Output short-circuit ⁽²⁾		Continuous		
T _A	Operating temperature		–40	150	°C
T _J	Junction temperature			150	°C
T _{STG}	Storage temperature		–65	150	°C

- (1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
- (2) Short-circuit to ground, one amplifier per package.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
V _S	Supply voltage, V _S = (V ₊) – (V _–)	Single supply	4.5		36	V
		Dual supply	±2.25		±18	
T _A	Operating temperature		–40		125	°C

6.4 Thermal Information: OPA205

THERMAL METRIC ⁽¹⁾		OPA205	UNIT
		D (SOIC)	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	121.5	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	64.3	°C/W
R _{θJB}	Junction-to-board thermal resistance	65.0	°C/W
ψ _{JT}	Junction-to-top characterization parameter	18.2	°C/W
ψ _{JB}	Junction-to-board characterization parameter	64.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Thermal Information: OPA2205

THERMAL METRIC ⁽¹⁾		OPA2205		UNIT
		D (SOIC)	DGK (VSSOP)	
		8 PINS	8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	126.9	175.6	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	67.1	63.1	°C/W
R _{θJB}	Junction-to-board thermal resistance	70.3	97.2	°C/W
ψ _{JT}	Junction-to-top characterization parameter	18.8	7.8	°C/W
ψ _{JB}	Junction-to-board characterization parameter	69.5	95.5	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.6 Thermal Information: OPA4205

THERMAL METRIC ⁽¹⁾		OPA4205		UNIT
		D (SOIC)	PW (TSSOP)	
		14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	86.5	117.1	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	38.5	36.0	°C/W
R _{θJB}	Junction-to-board thermal resistance	43.5	59.3	°C/W
ψ _{JT}	Junction-to-top characterization parameter	7.4	2.6	°C/W
ψ _{JB}	Junction-to-board characterization parameter	42.9	58.3	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.7 Electrical Characteristics: $V_S = \pm 5\text{ V}$

at $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = \text{mid supply}$, and $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V _{OS}	Input offset voltage	OPA2205			±2	±15	μV
			T _A = −40°C to +125°C			±25	
		OPAx205A			±4	±25	
			T _A = −40°C to +125°C			±55	
dV _{OS} /dT	Input offset voltage drift	OPA2205	T _A = −40°C to +125°C		±0.04	±0.2	μV/°C
		OPAx205A	T _A = −40°C to +125°C		±0.08	±0.5	
PSRR	Power supply rejection ratio	OPA2205, V _S = ±2.25 V to ±18 V			±0.05	±0.25	μV/V
			T _A = −40°C to +125°C			±0.5	
		OPAx205A, V _S = ±2.25 V to ±18 V			±0.05	±0.5	
			T _A = −40°C to +125°C			±1	
	Channel separation, (dual, quad)	f = dc			130		dB
		f = 100 kHz			110		
INPUT BIAS CURRENT							
I _B	Input bias current	OPA2205			±0.1	±0.4	nA
			T _A = 0°C to 85°C			±0.6	
			T _A = −40°C to +125°C			±0.9	
		OPAx205A			±0.1	±0.5	
			T _A = 0°C to 85°C			±0.75	
			T _A = −40°C to +125°C			±1	
I _{OS}	Input offset current				±0.1	±0.4	nA
		T _A = 0°C to 85°C				±0.5	
		T _A = −40°C to +125°C				±0.6	
NOISE							
	Input voltage noise	f = 0.1 Hz to 10 Hz			0.2		μV _{PP}
e _n	Input voltage noise density	f = 10 Hz			7.4		nV/√Hz
		f = 100 Hz			7.2		
		f = 1 kHz			7.2		
i _n	Input current noise density	f = 1 kHz			110		fA/√Hz
INPUT VOLTAGE							
V _{CM}	Common-mode voltage			(V−) + 1		(V+) − 1.4	V
CMRR	Common-mode rejection ratio	OPA2205, (V−) + 1 V < V _{CM} < (V+) − 1.4 V, T _A = −40°C to +125°C		124	140		dB
		OPAx205A, (V−) + 1 V < V _{CM} < (V+) − 1.4 V, T _A = −40°C to +125°C		124	140		
INPUT IMPEDANCE							
Z _{ID}	Differential				9 4.4		MΩ pF
Z _{ICM}	Common-mode				300 4.4		GΩ pF

6.7 Electrical Characteristics: $V_S = \pm 5\text{ V}$ (continued)

at $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = \text{mid supply}$, and $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A _{OL}	Open-loop voltage gain	OPA2205, T _A = −40°C to +125°C, (V−) + 200 mV < V _O < (V+) − 200 mV	R _L = 10 kΩ	126	132	dB	
			R _L = 2 kΩ	126	130		
		OPAx205A, T _A = −40°C to +125°C, (V−) + 200 mV < V _O < (V+) − 200 mV	R _L = 10 kΩ	126	132		
			R _L = 2 kΩ	126	130		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product			3.6		MHz	
SR	Slew rate	4-V step, gain = −1		3.2		V/μs	
	Phase margin	R _L = 10 kΩ, C _L = 25 pF		67		degrees	
t _S	Settling time	To 0.024% (12-bit), 4-V step, gain = 1, C _L = 30 pF	Falling	2.2		μs	
			Rising	2.8			
	Overload recovery time	Gain = −10		0.3		μs	
THD+N	Total harmonic distortion + noise	V _O = 5 V _{PP} , gain = +1, f = 1 kHz, R _L = 2 kΩ		0.0004		%	
OUTPUT							
	Voltage output swing from rail	A _{OL} > 126 dB	R _L = 10 kΩ	(V−) + 0.2	(V+) − 0.2	V	
			R _L = 2 kΩ	(V−) + 0.2	(V+) − 0.2		
		T _A = −40°C to +125°C, R _L = 10 kΩ		(V−) + 0.2	(V+) − 0.2		
I _{SC}	Short-circuit current			±25		mA	
C _{LOAD}	Capacitive load drive			See Typical Characteristics			
R _O	Open-loop output impedance			See Typical Characteristics			
POWER SUPPLY							
I _Q	Quiescent current per amplifier	I _O = 0 mA		220	240	μA	
			T _A = −40°C to +125°C		310		

6.8 Electrical Characteristics: $V_S = \pm 15\text{ V}$

at $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = \text{mid supply}$, and $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OFFSET VOLTAGE							
V _{OS}	Input offset voltage	OPA2205			±2	±15	μV
			T _A = −40°C to +125°C			±25	
		OPAx205A			±4	±25	
			T _A = −40°C to +125°C			±55	
dV _{OS} /dT	Input offset voltage drift	OPA2205	T _A = −40°C to +125°C		±0.04	±0.2	μV/°C
		OPAx205A	T _A = −40°C to +125°C		±0.08	±0.5	
PSRR	Power supply rejection ratio	OPA2205, V _S = ±2.25 V to ±18 V			±0.05	±0.25	μV/V
			T _A = −40°C to +125°C			±0.5	
		OPAx205A, V _S = ±2.25 V to ±18 V			±0.05	±0.5	
			T _A = −40°C to +125°C			±1	
	Channel separation, (dual, quad)	f = dc			130		dB
		f = 100 kHz			110		
INPUT BIAS CURRENT							
I _B	Input bias current	OPA2205			±0.1	±0.4	nA
			T _A = 0°C to 85°C			±0.6	
			T _A = −40°C to +125°C			±0.9	
		OPAx205A			±0.1	±0.5	
			T _A = 0°C to 85°C			±1	
			T _A = −40°C to +125°C			±1.2	
I _{OS}	Input offset current				±0.1	±0.4	nA
		T _A = 0°C to 85°C				±0.8	
		T _A = −40°C to +125°C				±0.9	
NOISE							
	Input voltage noise	f = 0.1 Hz to 10 Hz			0.2		μV _{PP}
e _n	Input voltage noise density	f = 10 Hz			7.4		nV/√Hz
		f = 100 Hz			7.2		
		f = 1 kHz			7.2		
i _n	Input current noise density	f = 1 kHz			110		fA/√Hz
INPUT VOLTAGE							
V _{CM}	Common-mode voltage			(V−) + 1		(V+) − 1.4	V
CMRR	Common-mode rejection ratio	OPA2205, (V−) + 1 V < V _{CM} < (V+) − 1.4 V		126	140		dB
			T _A = −40°C to +125°C	124	140		
		OPAx205A, (V−) + 1 V < V _{CM} < (V+) − 1.4 V		126	140		
			T _A = −40°C to +125°C	124	140		
INPUT IMPEDANCE							
Z _{ID}	Differential				9 4.4		MΩ pF
Z _{ICM}	Common-mode				300 4.3		GΩ pF

6.8 Electrical Characteristics: $V_S = \pm 15\text{ V}$ (continued)

at $T_A = 25^\circ\text{C}$, $V_{CM} = V_{OUT} = \text{mid supply}$, and $R_L = 10\text{ k}\Omega$ connected to $V_S / 2$ (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
OPEN-LOOP GAIN							
A _{OL}	Open-loop voltage gain	OPA2205, T _A = −40°C to +125°C	R _L = 10 kΩ, (V−) + 200 mV < V _O < (V+) − 200 mV	132	135	dB	
			R _L = 2 kΩ, (V−) + 350 mV < V _O < (V+) − 350 mV	132	135		
		OPAx205A, T _A = −40°C to +125°C	R _L = 10 kΩ, (V−) + 200 mV < V _O < (V+) − 200 mV	126	132		
			R _L = 2 kΩ, (V−) + 350 mV < V _O < (V+) − 350 mV	126	130		
FREQUENCY RESPONSE							
GBW	Gain-bandwidth product	C _L = 30 pF		3.6		MHz	
SR	Slew rate	10-V step, gain = −1		4		V/μs	
	Phase margin	R _L = 10 kΩ, C _L = 25 pF		58		degrees	
t _s	Settling time	To 0.024% (12-bit), 10-V step, gain = 1, C _L = 30 pF	Falling	2.8		μs	
			Rising	4.5			
	Overload recovery time	Gain = −10		0.2		μs	
THD+N	Total harmonic distortion + noise	V _O = 5 V _{PP} , gain = +1, f = 1 kHz, R _L = 2 kΩ		0.0004		%	
OUTPUT							
	Voltage output swing from rail	A _{OL} > 126 dB	R _L = 10 kΩ	(V−) + 0.2	(V+) − 0.2	V	
			R _L = 2 kΩ	(V−) + 0.35	(V+) − 0.35		
		T _A = −40°C to +125°C, R _L = 10 kΩ		(V−) + 0.2	(V+) − 0.2		
I _{SC}	Short-circuit current			±25		mA	
C _{LOAD}	Capacitive load drive			See Typical Characteristics			
R _O	Open-loop output impedance			See Typical Characteristics			
POWER SUPPLY							
I _Q	Quiescent current per amplifier	I _O = 0 mA		220	240	μA	
			T _A = −40°C to +125°C		310		

6.9 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = V_{OUT} = \text{mid supply}$, and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

表 6-1. Table of Graphs

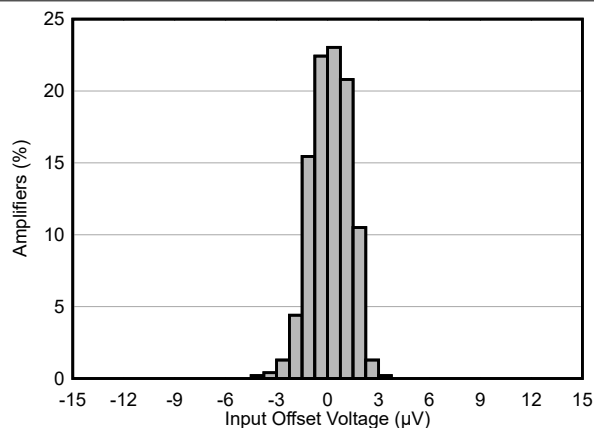
DESCRIPTION	FIGURE
Offset Voltage Production Distribution at 25°C	图 6-1
Offset Voltage at 125°C	图 6-2
Offset Voltage at -40°C	图 6-3
Offset Voltage vs Temperature	图 6-4
Offset Voltage Drift Distribution	图 6-5
Offset Voltage vs Output Voltage	图 6-6
Offset Voltage vs Power Supply Voltage	图 6-7
Power-Supply Rejection Ratio vs Temperature	图 6-8
Power-Supply and Common-Mode Rejection Ratio vs Frequency	图 6-9
Common-Mode Rejection Ratio vs Temperature	图 6-10
Offset Voltage vs Common-Mode Voltage	图 6-11
Offset Voltage vs V_{CM} at Low Supply	图 6-12
Offset Voltage vs V_{CM} at High Supply	图 6-13
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Negative Overload Recovery, Gain = -1	图 6-36
Settling Time	图 6-37
Small-Signal Step Response, Gain = +1	图 6-38
Small-Signal Step Response, Gain = -1	图 6-39
Large-Signal Step Response, Gain = +1	图 6-40
Large-Signal Step Response, Gain = -1	图 6-41
Short-Circuit Current vs Temperature	图 6-42
Electromagnetic Interference Rejection (EMIRR)	图 6-43
Quiescent Current vs Supply Voltage	图 6-44

6.9 Typical Characteristics

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = V_{OUT} = \text{mid supply}$, and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

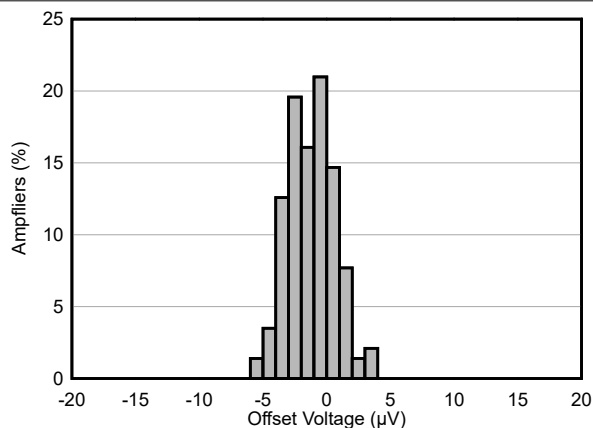
表 6-1. Table of Graphs (continued)

DESCRIPTION	FIGURE
Quiescent Current vs Temperature	图 6-45



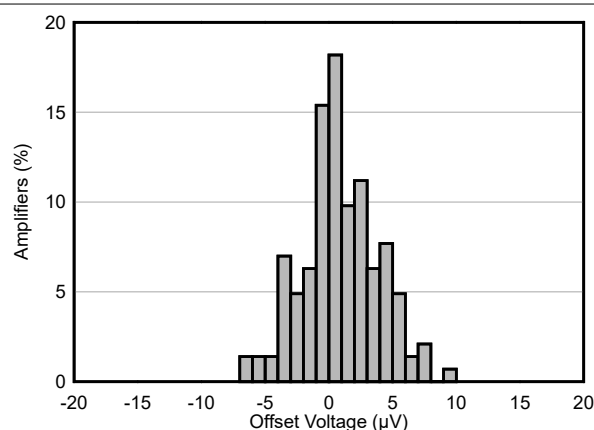
$T_A = 25^\circ\text{C}$

图 6-1. Offset Voltage Production Distribution at 25°C



$T_A = 125^\circ\text{C}$

图 6-2. Offset Voltage Distribution at 125°C



$T_A = -40^\circ\text{C}$

图 6-3. Offset Voltage Distribution at -40°C

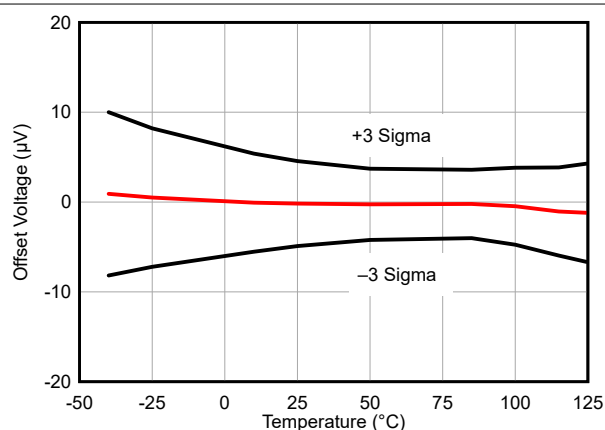


图 6-4. Offset Voltage vs Temperature

6.9 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = V_{OUT} = \text{midsupply}$, and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

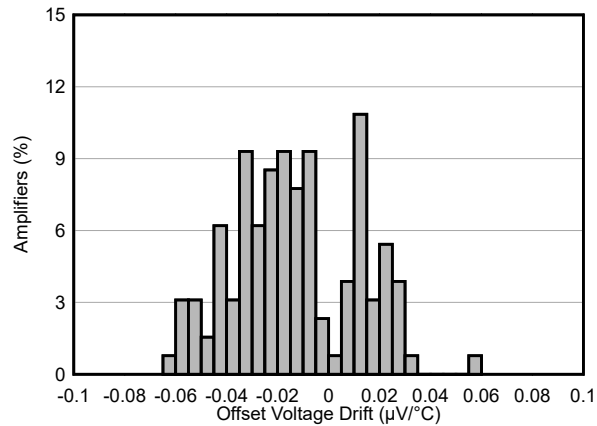


FIG 6-5. Offset Voltage Drift Distribution

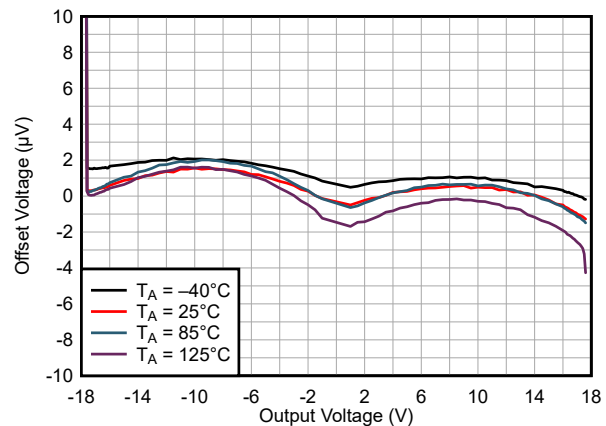


FIG 6-6. Offset Voltage vs Output Voltage

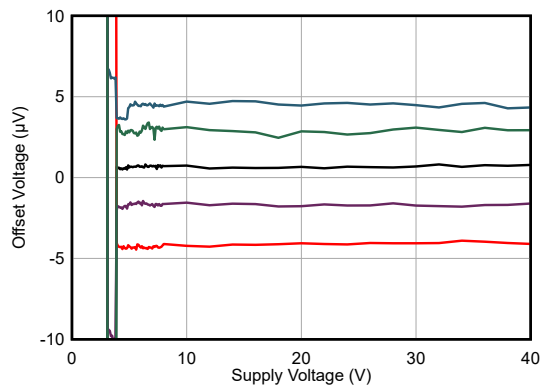


FIG 6-7. Offset Voltage vs Power Supply Voltage

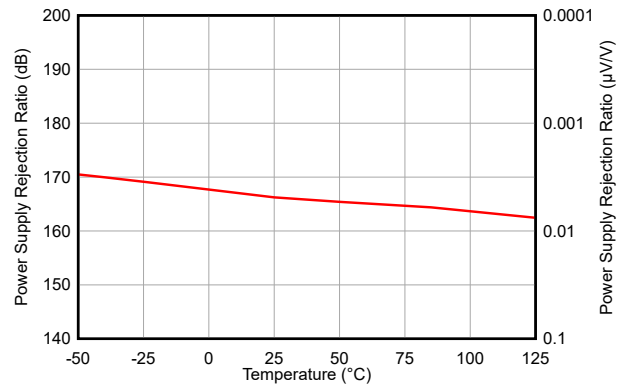


FIG 6-8. Power-Supply Rejection Ratio vs Temperature

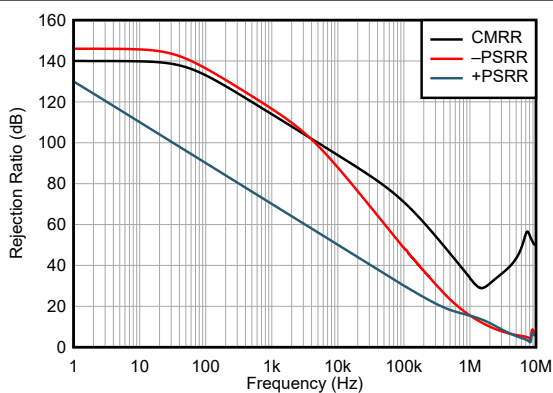


FIG 6-9. Power-Supply and Common-Mode Rejection Ratio vs Frequency

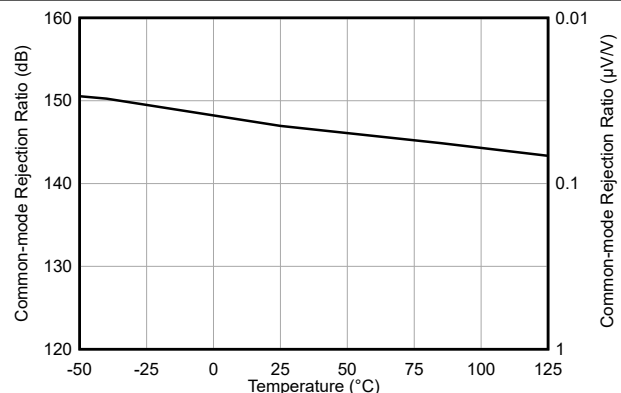


FIG 6-10. Common-Mode Rejection Ratio vs Temperature

6.9 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = V_{OUT} = \text{midsupply}$, and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

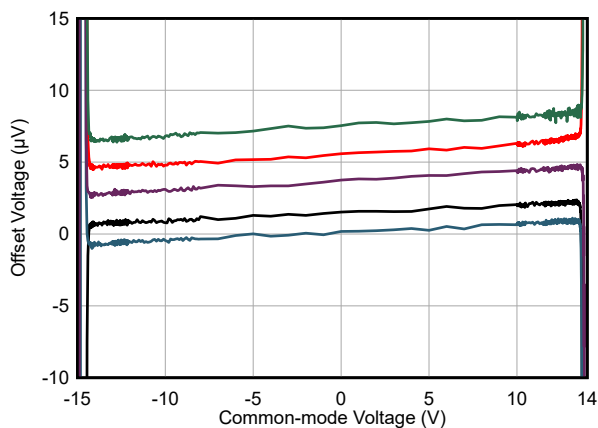


Figure 6-11. Offset Voltage vs Common-Mode Voltage

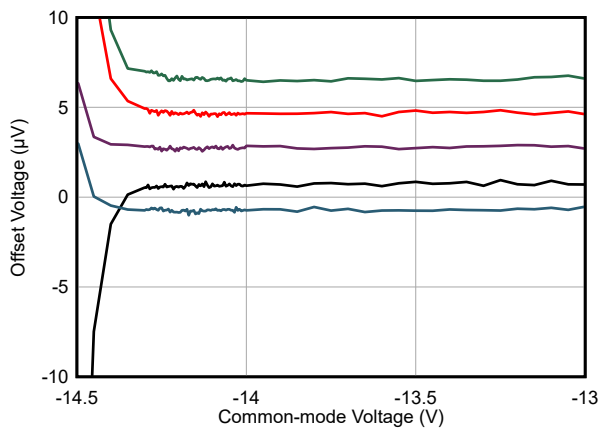


Figure 6-12. Offset Voltage vs V_{CM} at Low Supply

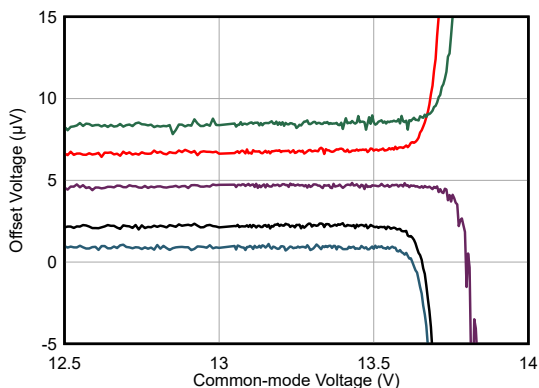


Figure 6-13. Offset Voltage vs V_{CM} at High Supply

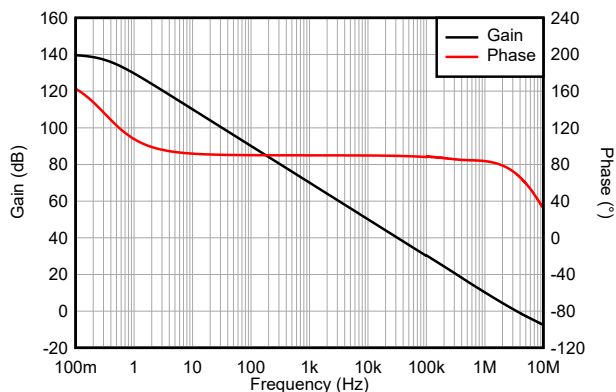


Figure 6-14. Open-Loop Gain and Phase vs Frequency

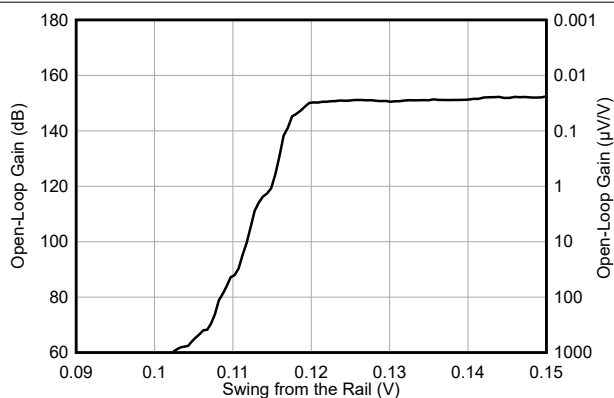


Figure 6-15. Open-Loop Gain vs Swing From the Rail

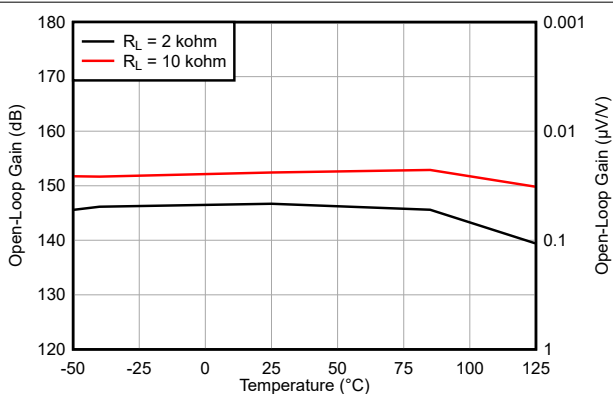


Figure 6-16. Open-Loop Gain vs Temperature

6.9 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = V_{OUT} = \text{mid supply}$, and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

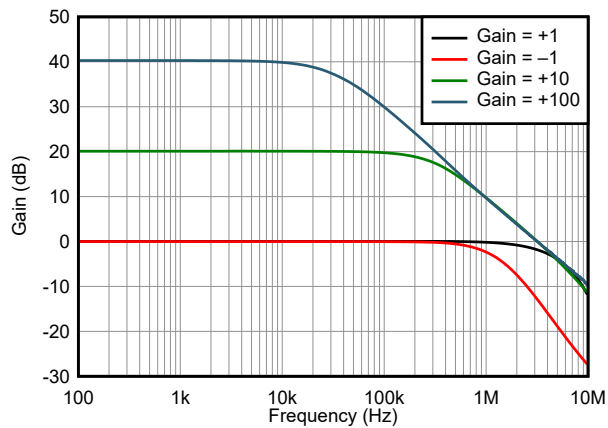


Figure 6-17. Closed-Loop Gain vs Frequency

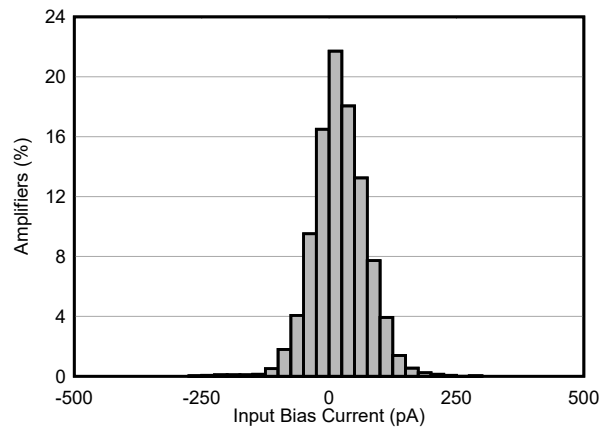


Figure 6-18. Input Bias Production Distribution

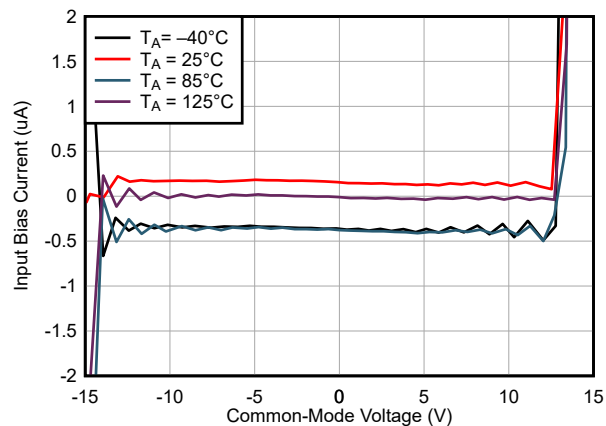


Figure 6-19. Input Bias vs Common-Mode Voltage

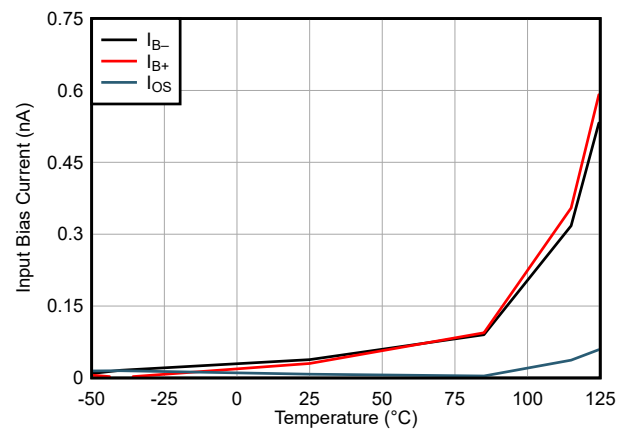


Figure 6-20. Input Bias and Input Offset Current vs Temperature

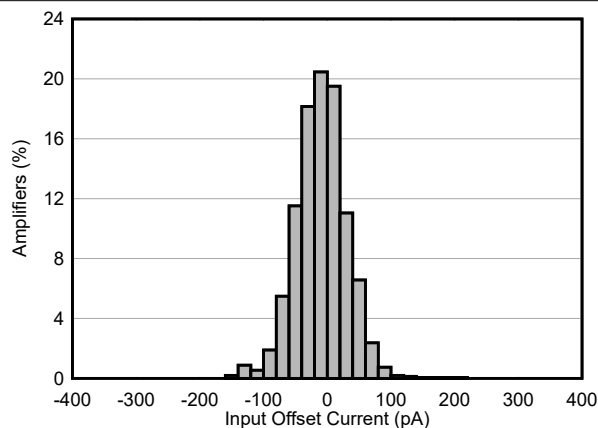


Figure 6-21. Input Offset Current Production Distribution

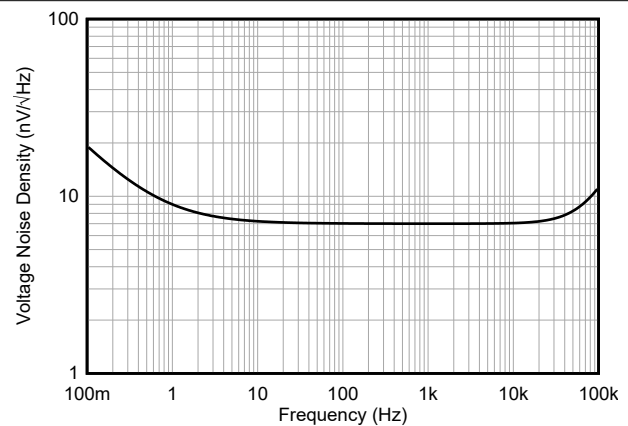
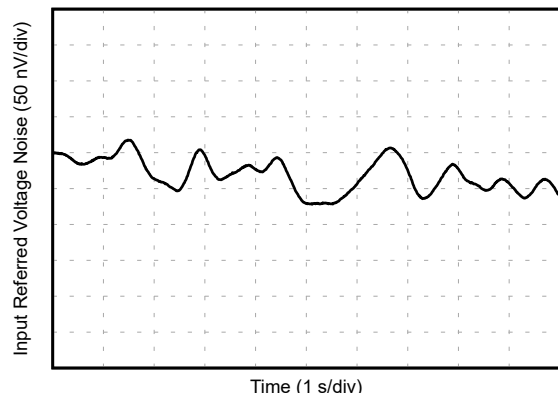


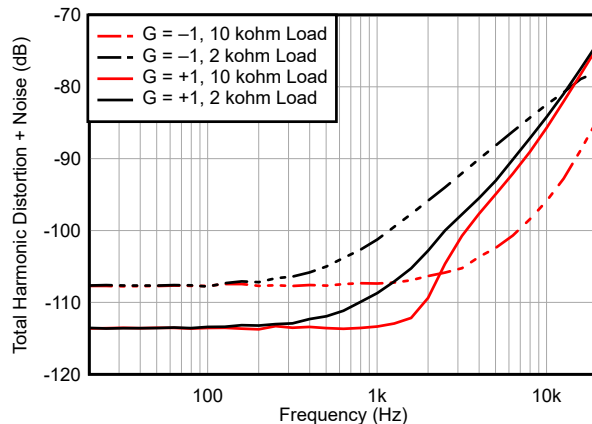
Figure 6-22. Voltage Noise Density vs Frequency

6.9 Typical Characteristics (continued)

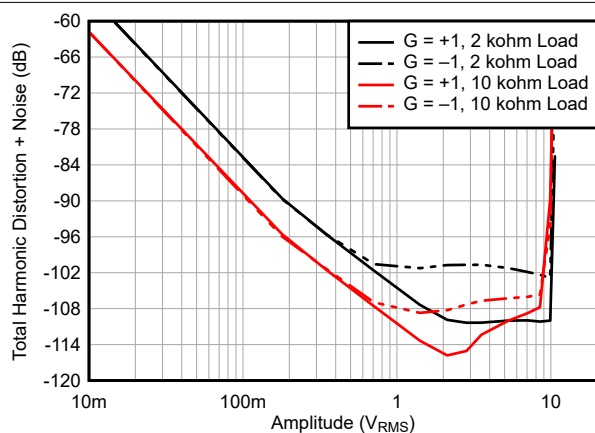
at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = V_{OUT} = \text{midsupply}$, and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)



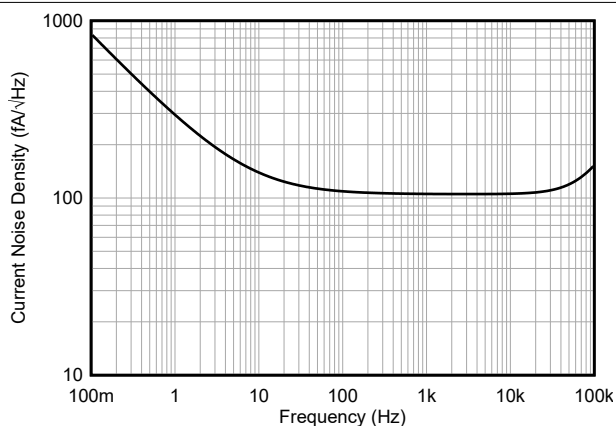
6-23. 0.1-Hz to 10-Hz Noise



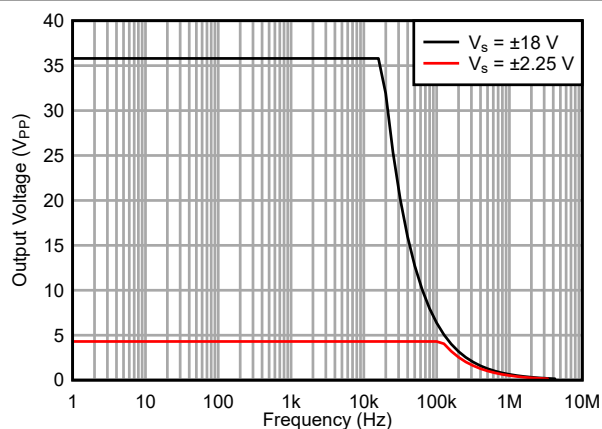
6-24. Total Harmonic Distortion + Noise Ratio vs Frequency



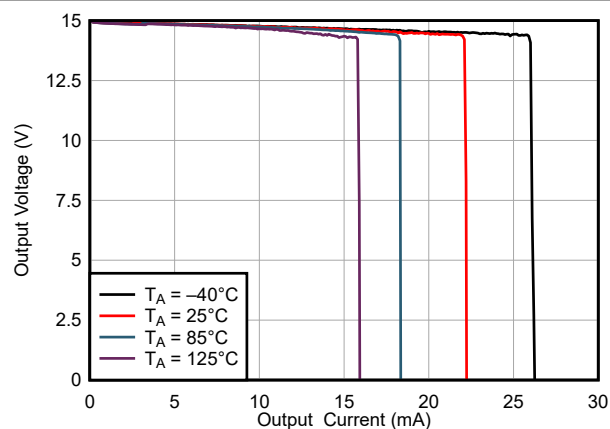
6-25. Total Harmonic Distortion + Noise Ratio vs Output Amplitude



6-26. Current Noise vs Frequency



6-27. Maximum Output Voltage vs Frequency



6-28. Output Voltage Swing vs Output Sourcing Current

6.9 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = V_{OUT} = \text{midsupply}$, and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

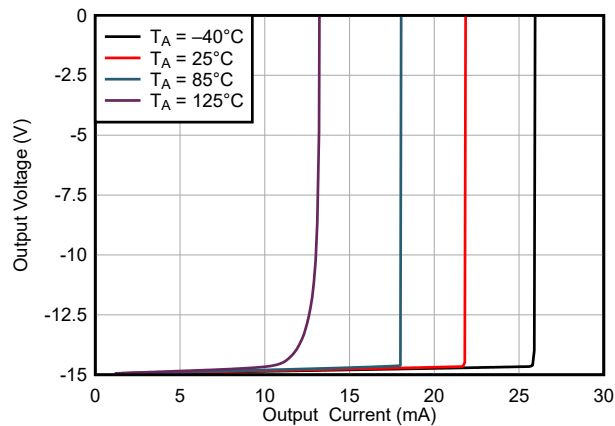


FIG 6-29. Output Voltage Swing vs Output Sinking Current

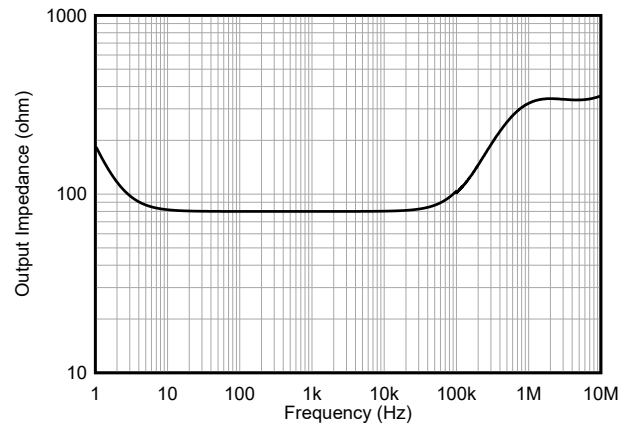


FIG 6-30. Open-Loop Output Impedance vs Frequency

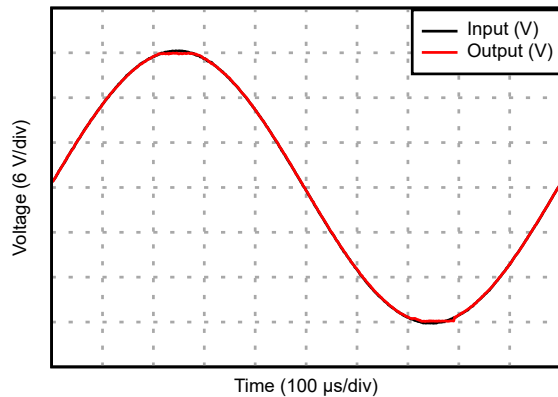


FIG 6-31. No Phase Reversal

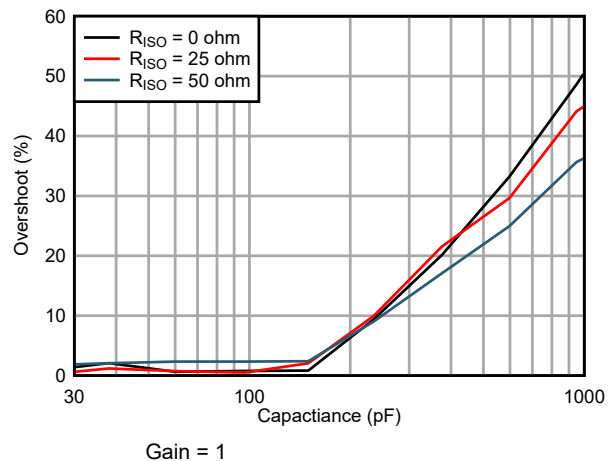


FIG 6-32. Small-Signal Overshoot vs Capacitive Load, Gain = +1

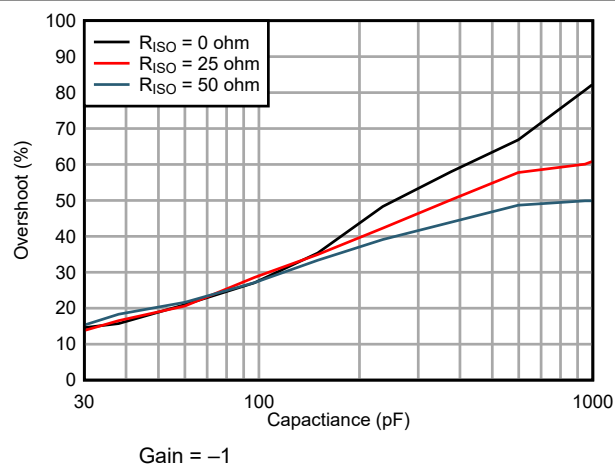


FIG 6-33. Small-Signal Overshoot vs Capacitive Load, Gain = -1

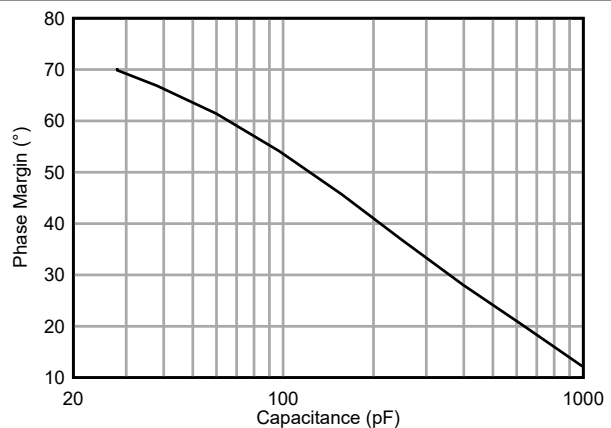
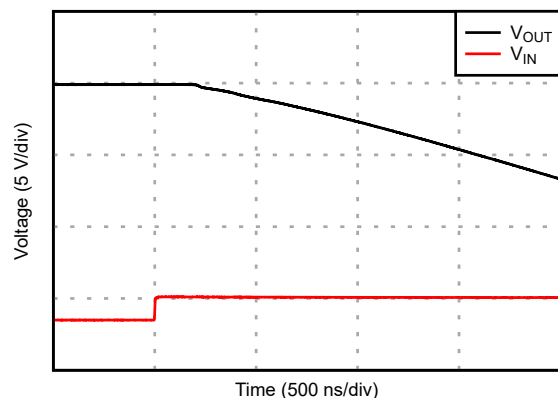


FIG 6-34. Phase Margin vs Capacitive Load

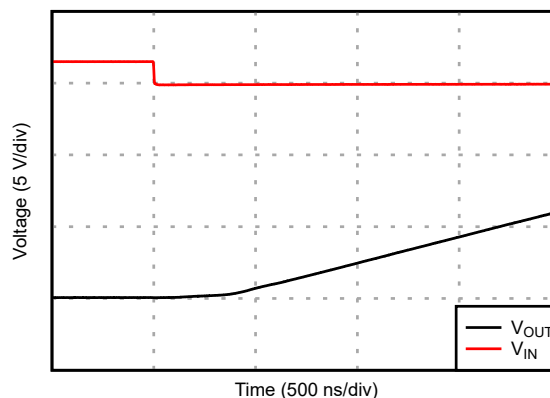
6.9 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = V_{OUT} = \text{midsupply}$, and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)



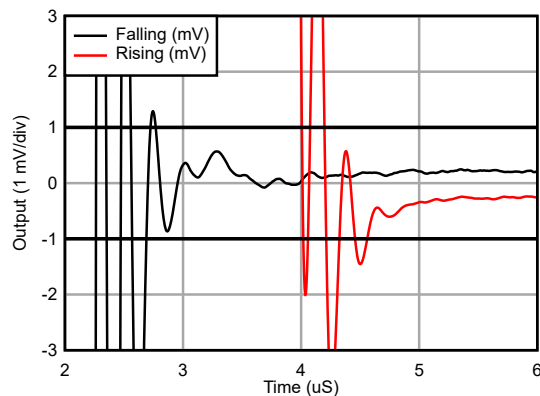
Gain = -1

6-35. Positive Overload Recovery, Gain = -1

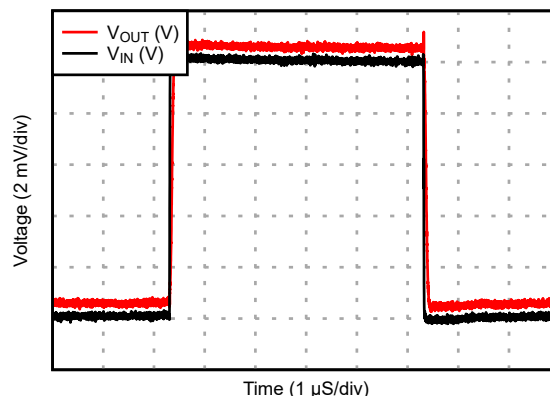


Gain = -1

6-36. Negative Overload Recovery, Gain = -1

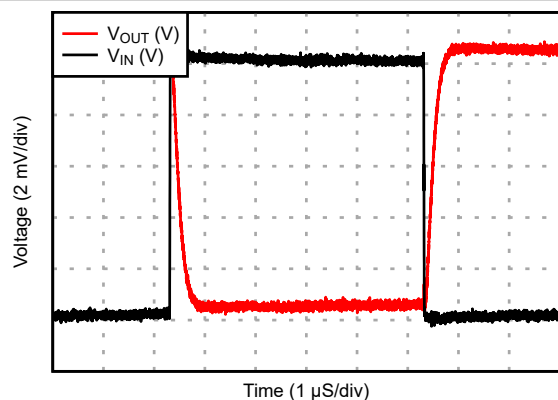


6-37. Settling Time



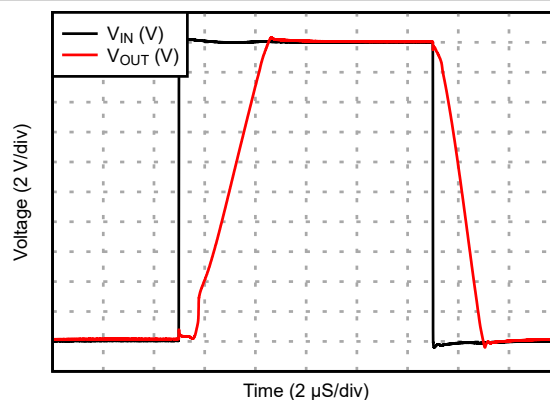
Gain = 1

6-38. Small-Signal Step Response, Gain = +1



Gain = -1

6-39. Small-Signal Step Response, Gain = -1

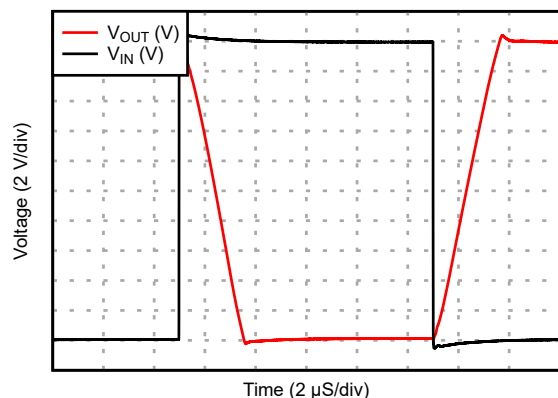


Gain = 1

6-40. Large-Signal Step Response, Gain = +1

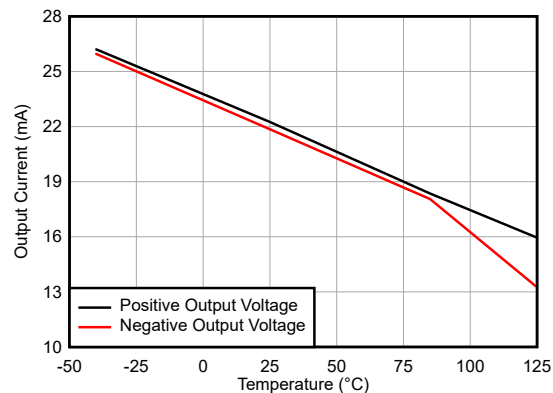
6.9 Typical Characteristics (continued)

at $T_A = 25^\circ\text{C}$, $V_S = \pm 15\text{V}$, $V_{CM} = V_{OUT} = \text{midsupply}$, and $R_L = 10\text{ k}\Omega$ (unless otherwise noted)

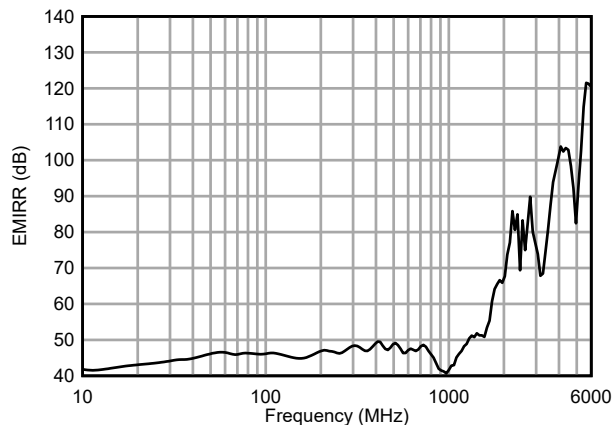


Gain = -1

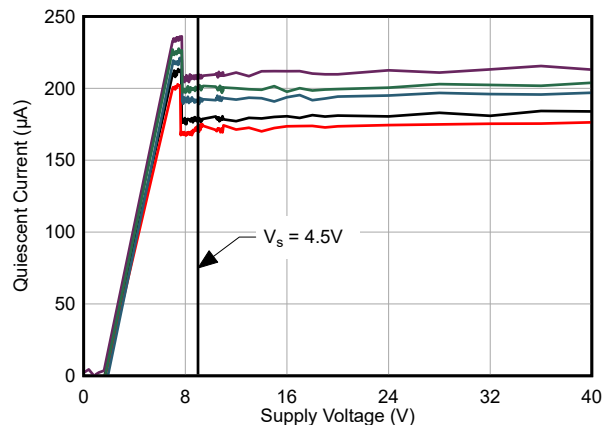
6-41. Large-Signal Step Response, Gain = -1



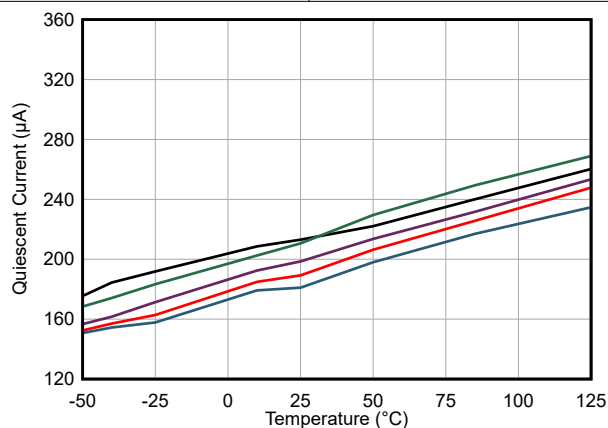
6-42. Short-Circuit Current vs Temperature



6-43. Electromagnetic Interference Rejection



6-44. Quiescent Current vs Supply Voltage



6-45. Quiescent Current vs Temperature

7 Parameter Measurement Information

7.1 Typical Specifications and Distributions

To design a more robust circuit, designers often have questions about a typical specification of an amplifier. As a result of natural variations in process technology and manufacturing procedures, every specification of an amplifier exhibits some amount of deviation from the ideal value, such as the input bias current of an amplifier. These deviations often follow *Gaussian* (bell curve), or *normal* distributions. Circuit designers can leverage this information to guard-band their system, even when there is no minimum or maximum specification in the [Electrical Characteristics](#).

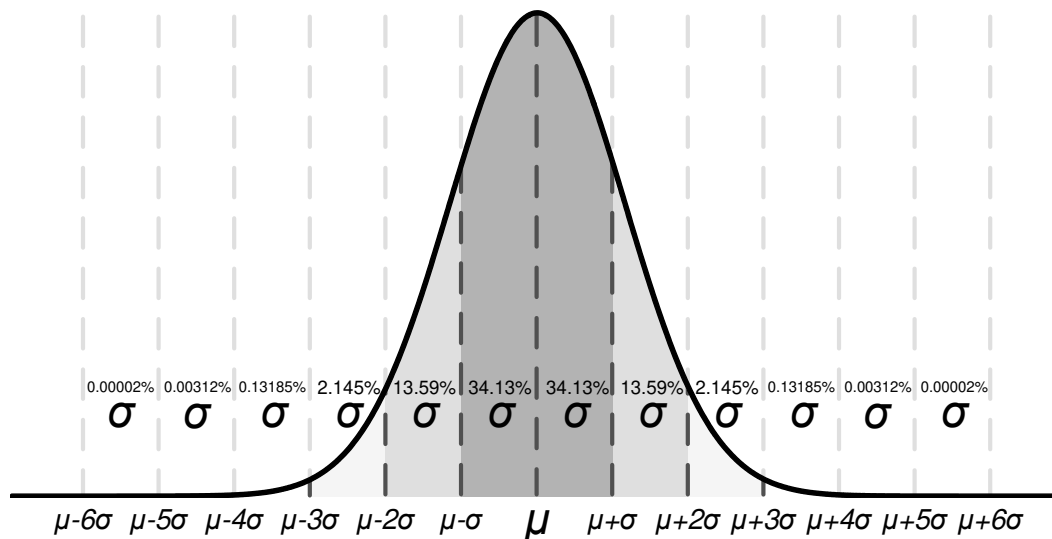


FIG 7-1. Ideal Gaussian Distribution

FIG 7-1 shows an example distribution, where μ , is the mean of the distribution, and where σ , or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from $\mu - \sigma$ to $\mu + \sigma$).

Depending on the specification, values listed in the *typical* column of [Electrical Characteristics](#) are represented in different ways. As a general guideline, if a specification naturally has a nonzero mean (for example, gain bandwidth), then the typical value is equal to the mean (μ). However, if a specification naturally has a mean near zero (for example, input bias current), then the typical value is equal to the mean plus one standard deviation ($\mu + \sigma$) to most accurately represent the typical value.

Use this chart to calculate the approximate probability of a specification in a unit. For example, the OPAx205 typical input bias current is ± 0.1 nA; therefore, 68.2% of all devices are expected to have an input bias from ± 0.1 nA. At 4σ , 99.9937% of the distribution has an input bias less than ± 0.28 nA, which means that 0.0063% of the population is outside of these limits, and corresponds to approximately 1 in 15,873 units.

Units that are found to exceed any tested minimum or maximum specifications are removed from production material. For example, the OPAx205 have a maximum input bias of ± 0.5 nA at 25°C. Although this value corresponds to approximately 6σ (approximately 1 in 500 million units), TI removes any unit with a larger input bias from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guard band for your application, and design worst-case conditions using this value. Use this information to only estimate the performance of a device.

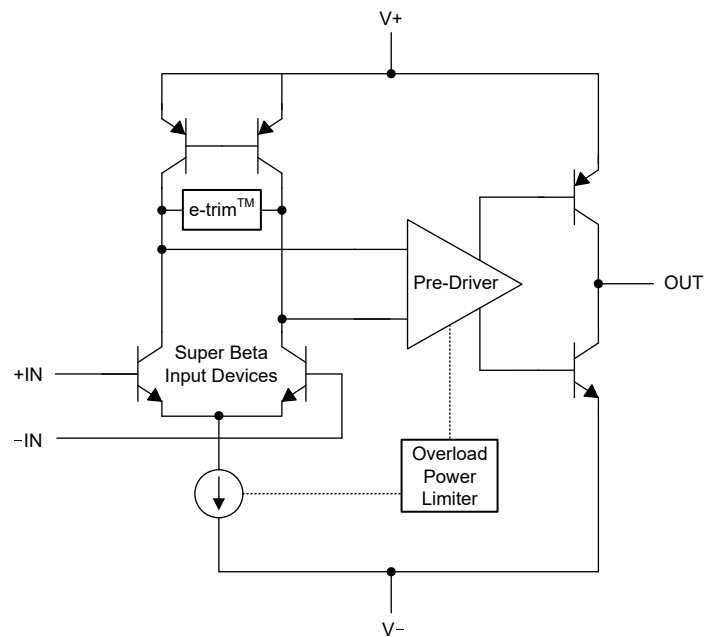
8 Detailed Description

8.1 Overview

The OPAx205 are the first 36-V bipolar, e-trim operational amplifiers that uses a package-level offset trim to minimize the offset voltage and offset voltage drift introduced during the manufacturing process. This trim is performed after the device has been assembled to remove any offset errors introduced throughout the manufacturing process, and trim communication is disabled afterward. These devices also feature super-beta inputs that decrease the input bias current and input current noise.

The following section shows the simplified diagram of the OPAx205.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Input Offset Trimming

The OPAx205 are the industry's first e-trim operational amplifiers built on a bipolar process. The input offset voltage of an amplifier is determined by the inherent mismatch between the input transistors. The offset can be minimized using laser-trimming performed during the manufacturing process while the devices are still in the bare silicon form. However, when the silicon is packaged, the packaging process introduces additional offset due to mechanic stresses. TI's new trimming processes are used to trim the offset after the packaging process is complete to minimize both inherent and package-induced offsets. After trimming, communication is disabled to make sure the amplifiers operate properly in the final system.

A comparison between production offset values for the industry-popular, laser-trimmed [OPA2277](#) and the OPAx205 proprietary trim can be seen in [Figure 8-1](#) and [Figure 8-2](#).

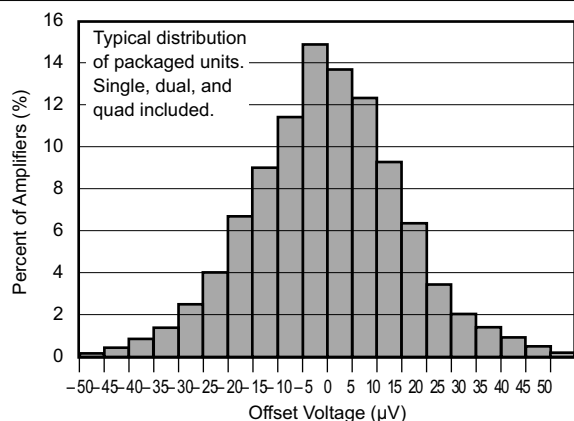


Figure 8-1. OPA2277 Laser-Trimmed Operational Amplifier Offset

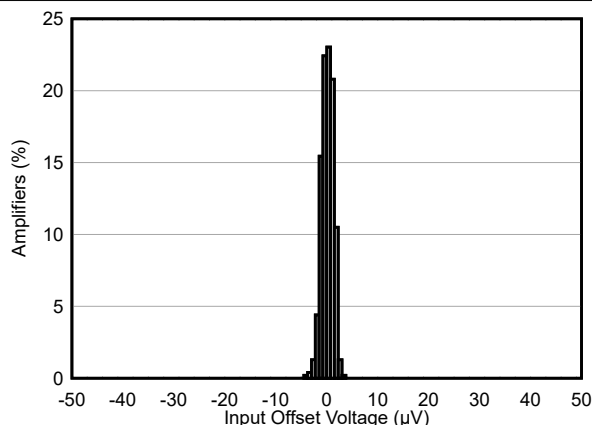


Figure 8-2. OPAx205 e-trim™ Operational Amplifier Offset

The OPAx205 are also trimmed at two temperatures to minimize the input offset voltage drift over temperature. The final performance of the offset drift can be seen in [Figure 8-3](#).

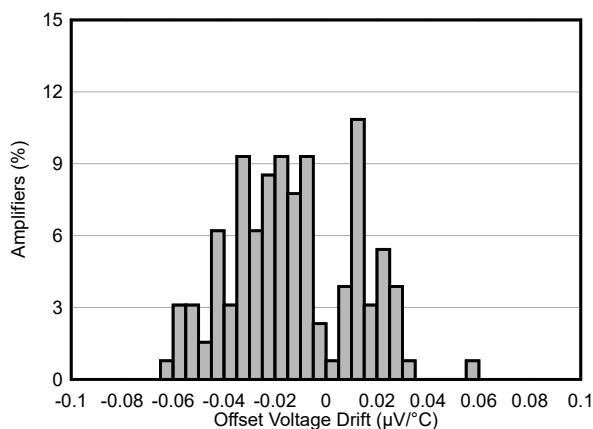


Figure 8-3. OPAx205 e-trim™ Operational Amplifier Drift

8.3.2 Lower Input Bias With Super-Beta Inputs

The OPAx205 have a super-beta input transistor architecture. In a transistor, the beta value is the ratio between the current flowing into the base and the current flowing from the collector to the emitter. A super-beta transistor is one where the beta value has been increased from several hundred to thousands. In a bipolar amplifier, the input bias current is the current flowing into the base of the input transistor pair, as well as a small leakage current that flows through the ESD diodes. A super-beta input reduces the input bias current of the amplifier. In addition, the super-beta inputs lower the input current noise that is directly related to the input bias current of the device. A comparison between the input bias current of the OPA2277 and the OPAx205 super-beta input bias currents can be seen in [Figure 8-4](#) and [Figure 8-5](#).

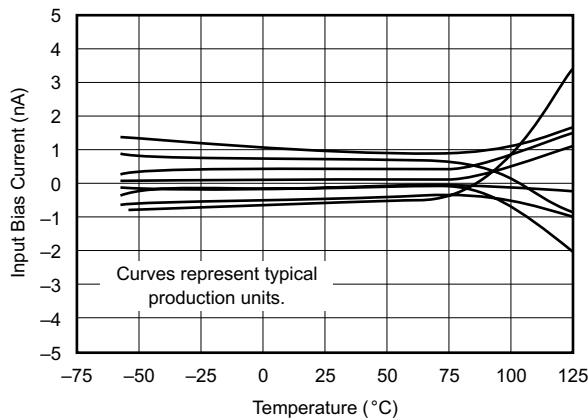


Figure 8-4. OPA2277 Input Bias Current

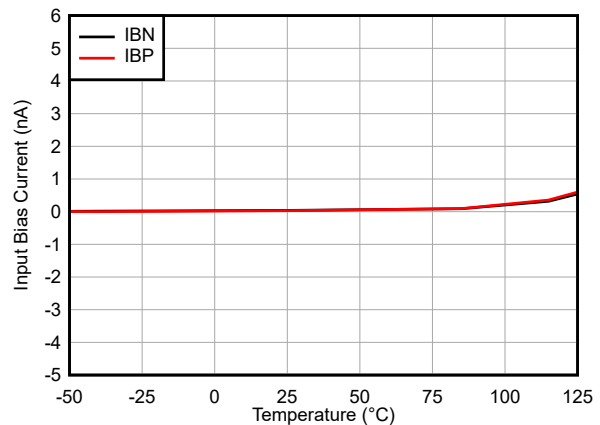


Figure 8-5. OPAx205 Super-Beta Input Bias Current

8.3.3 Overload Power Limiter

In many bipolar-based amplifiers, the output stage of the amplifier can draw significant (several milliamperes) of quiescent current if the output voltage becomes clipped (that is, the output voltage becomes limited by the negative or positive supply voltage). This condition can cause the system to enter a high-power consumption state, and potentially cause oscillations between the power supply and signal chain. The OPAx205 have an advanced output stage design that eliminates this problem. When the output voltage reaches either supply (V_+ or V_-), there is virtually no additional current consumption from the nominal quiescent current. This feature helps eliminate any potential system problems when the signal chain is disrupted by large external transient voltage.

8.3.4 EMI Rejection

The OPAx205 use integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources, such as wireless communications and densely populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved through circuit design techniques that improve the system performance. Additional information can be found in the [EMI Rejection Ratio of Operational Amplifiers application report](#).

8.4 Device Functional Modes

The OPAx205 have a single functional mode and are operational with any supply between 4.5 V (± 2.25 V) and 36 V (± 18 V).

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

The OPAx205 are unity-gain stable operational amplifiers with very low offset voltage, offset voltage drift, voltage noise, current noise and power consumption. These features make this device family a great choice for a variety of space-constrained and power-constrained systems.

9.2 Typical Applications

9.2.1 High-Precision Signal-Chain Input Buffer

A common application for the OPAx205 is an input buffer for the signal chain of a data acquisition (DAQ) or field instrumentation system. This amplifier family is selected because of the low offset and drift that maintain system accuracy across a variety of operating conditions. The low power consumption of the OPAx205 enables the device to be used in battery-operated or high-density applications, where thermal dissipation is difficult. The low 1/f (flicker) noise and broadband noise allow for higher-accuracy signal chains, such as those using a 24-bit delta-sigma analog-to-digital converter (ADC). If a higher sampling rate is needed, the OPAx205 can be paired with a fully differential amplifier, such as the [THP210](#), to drive the ADC inputs. [Figure 9-1](#) shows the OPA2205 configured as an input buffer to a differential ADC driver.

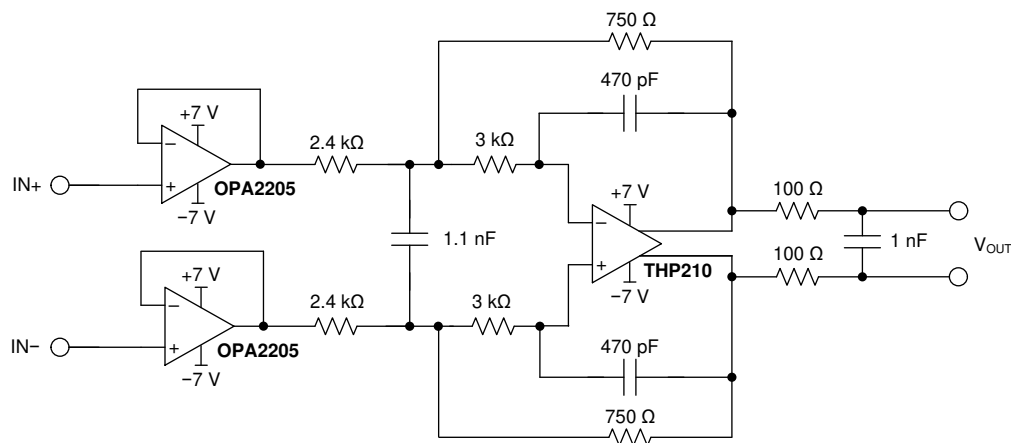


Figure 9-1. OPA2205 Configured as a DAQ Input Buffer

9.2.1.1 Design Requirements

The design requirements for this application are:

- Input range: ± 10 V
- Input frequency: 10 kHz
- Output voltage: ± 3.3 V
- Quiescent current: < 1.5 mA

9.2.1.2 Detailed Design Procedure

In this application, the input signal ranges from -10 V to $+10$ V with a frequency of up to 10 kHz. Because of possible portable-use cases for this data acquisition system (DAQ), low power consumption is required to minimize battery drain and thermal dissipation requirements.

To maintain high system accuracy the OPA2205 is selected as input buffers. This device is selected because of the high dc precision (4 μ V offset and 0.08 μ V/ $^{\circ}$ C offset drift), low flicker noise (0.2 μ Vpp), and low quiescent current (220 μ A). The buffers are followed by a high-precision, fully differential amplifier such as the THP210, which is capable of accurately driving a 24-bit, fully differential ADC such as the [ADS127L01](#).

9.2.1.3 Application Curves

The gain plot for this system can be seen in [Figure 9-2](#). This plot shows proper attenuation of the ± 10 -V signal to the target ± 3.3 -V output, and adequate bandwidth to support the input frequency range.

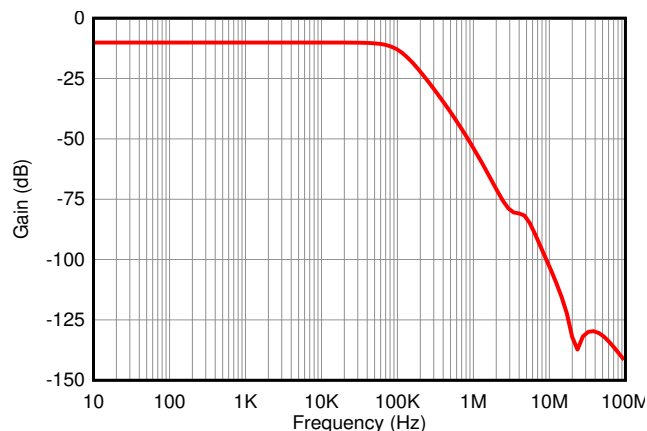


Figure 9-2. Gain Plot of DAQ Front End

9.2.2 Discrete, Two-Op-Amp Instrumentation Amplifier

Figure 9-3 shows the OPA2205 configured as a two-op-amp, discrete instrumentation amplifier. This configuration allows for a differential signal measurement, such as the signal from a load cell, with higher input impedance to the signal chain than most monolithic instrumentation amplifiers. The strong ac and dc performance of the OPA2205 enables high accuracy measurements.

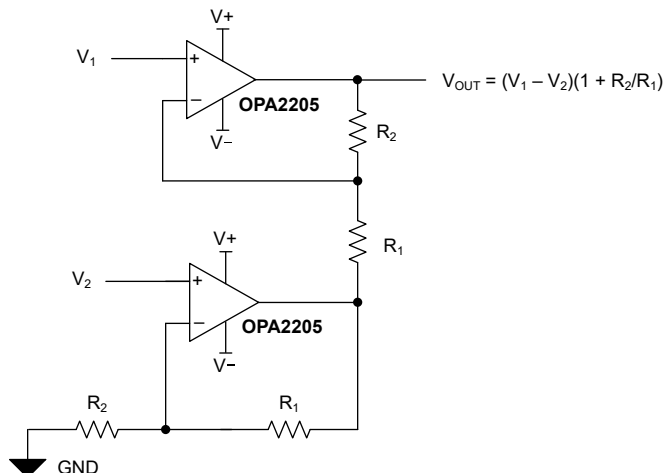


Figure 9-3. OPA2205 Configured as a Two-Op-Amp, Discrete Instrumentation Amplifier

9.2.3 Second-Order Low-Pass Filter

The OPAx205 has a very-low broadband voltage noise of only 7.2 nV/√Hz and flicker noise of 0.2 μV_{PP} given the low power consumption of only 220 μA, making this device an excellent choice for low-power filter applications.

Figure 9-4 is an example of one channel of the OPAx205 configured as a second-order low-pass filter with a cutoff frequency of 50 kHz.

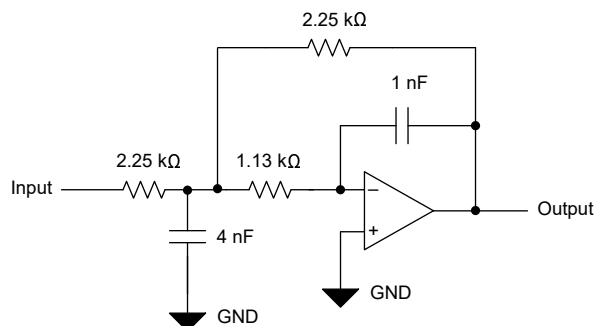


Figure 9-4. Second-Order Low-Pass Filter

9.3 Power Supply Recommendations

The OPAx205 operate with a power supply between 4.5 V to 36 V (± 2.25 V to ± 18 V). Parameters that can exhibit significant variance with regard to operating voltage are presented in [セクション 6.9](#).

Place 0.1- μ F bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see [セクション 9.4.1](#).

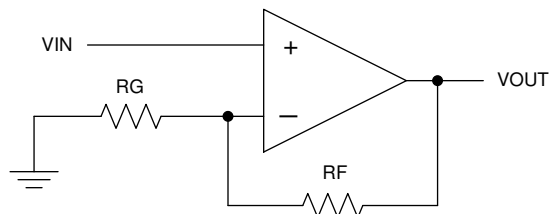
9.4 Layout

9.4.1 Layout Guidelines

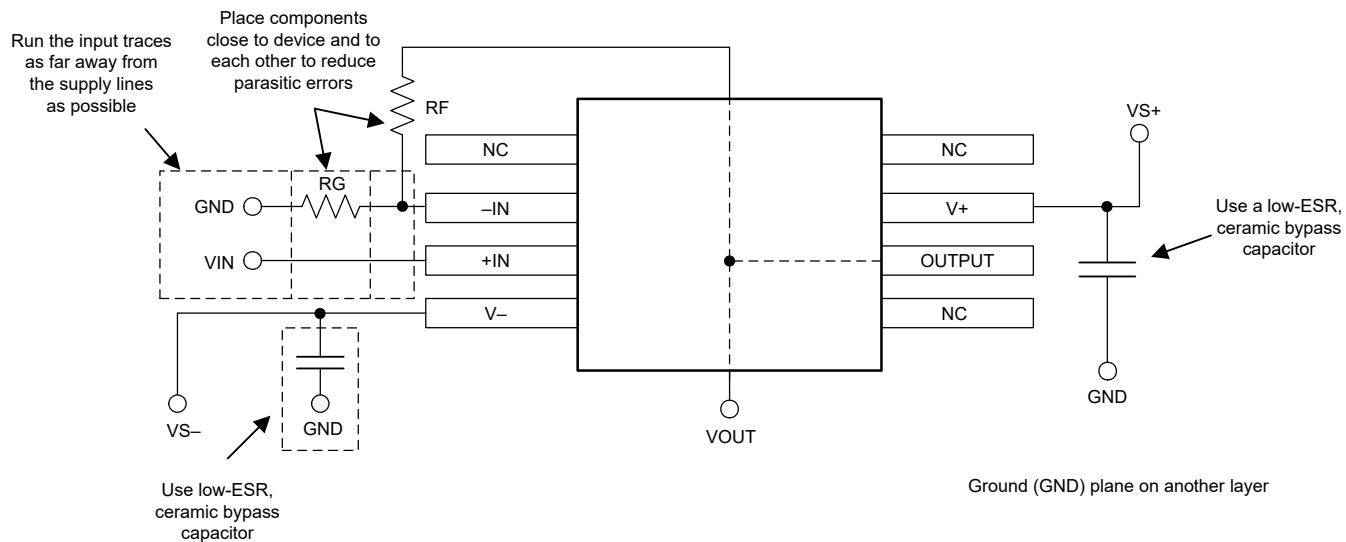
For best operational performance of the device, use good PCB layout practices, including:

- Connect low-ESR, 0.1- μ F ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications. Noise can propagate into analog circuitry through the power pins of the circuit as a whole, as well as through the individual op amp. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
- Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current. Separate grounding for analog and digital portions of circuitry is one of the simplest and most effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in [図 9-5](#), keep RF and RG close to the inverting input to minimize parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Clean the PCB following board assembly for best performance.
- Any precision integrated circuit can experience performance shifts due to moisture ingress into the plastic package. After any aqueous PCB cleaning process, bake the PCB assembly to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

9.4.2 Layout Example



9-5. Schematic Representation



9-6. Operational Amplifier Board Layout for Noninverting Configuration

10 Device and Documentation Support

10.1 Device Support

10.1.1 Development Support

The following evaluation modules are available:

- [DIP-ADAPTER-EVM](#)
- [DIYAMP-EVM](#)

10.1.1.1 PSpice® for TI

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10.2 ドキュメントのサポート

10.2.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、『[DIP-ADAPTER-EVM ユーザー・ガイド](#)』
- テキサス・インスツルメンツ、『[DIYAMP-SOIC-EVM ユーザー・ガイド](#)』

10.3 ドキュメントの更新通知を受け取る方法

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10.4 サポート・リソース

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

10.7 用語集

[テキサス・インスツルメンツ用語集](#) この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA205ADR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP205A	Samples
OPA205ADT	ACTIVE	SOIC	D	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP205A	Samples
OPA2205ADGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	22A5	Samples
OPA2205ADGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	22A5	Samples
OPA2205ADR	ACTIVE	SOIC	D	8	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2205A	Samples
OPA2205ADT	ACTIVE	SOIC	D	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2205A	Samples
OPA4205ADR	ACTIVE	SOIC	D	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4205A	Samples
OPA4205ADT	ACTIVE	SOIC	D	14	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OPA4205A	Samples
OPA4205APWR	ACTIVE	TSSOP	PW	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP4205A	Samples
OPA4205APWT	ACTIVE	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	OP4205A	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA205ADR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA205ADT	SOIC	D	8	250	180.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2205ADGKR	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2205ADGKT	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2205ADR	SOIC	D	8	3000	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA2205ADT	SOIC	D	8	250	180.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4205ADR	SOIC	D	14	3000	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4205ADT	SOIC	D	14	250	180.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
OPA4205APWR	TSSOP	PW	14	3000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4205APWT	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS

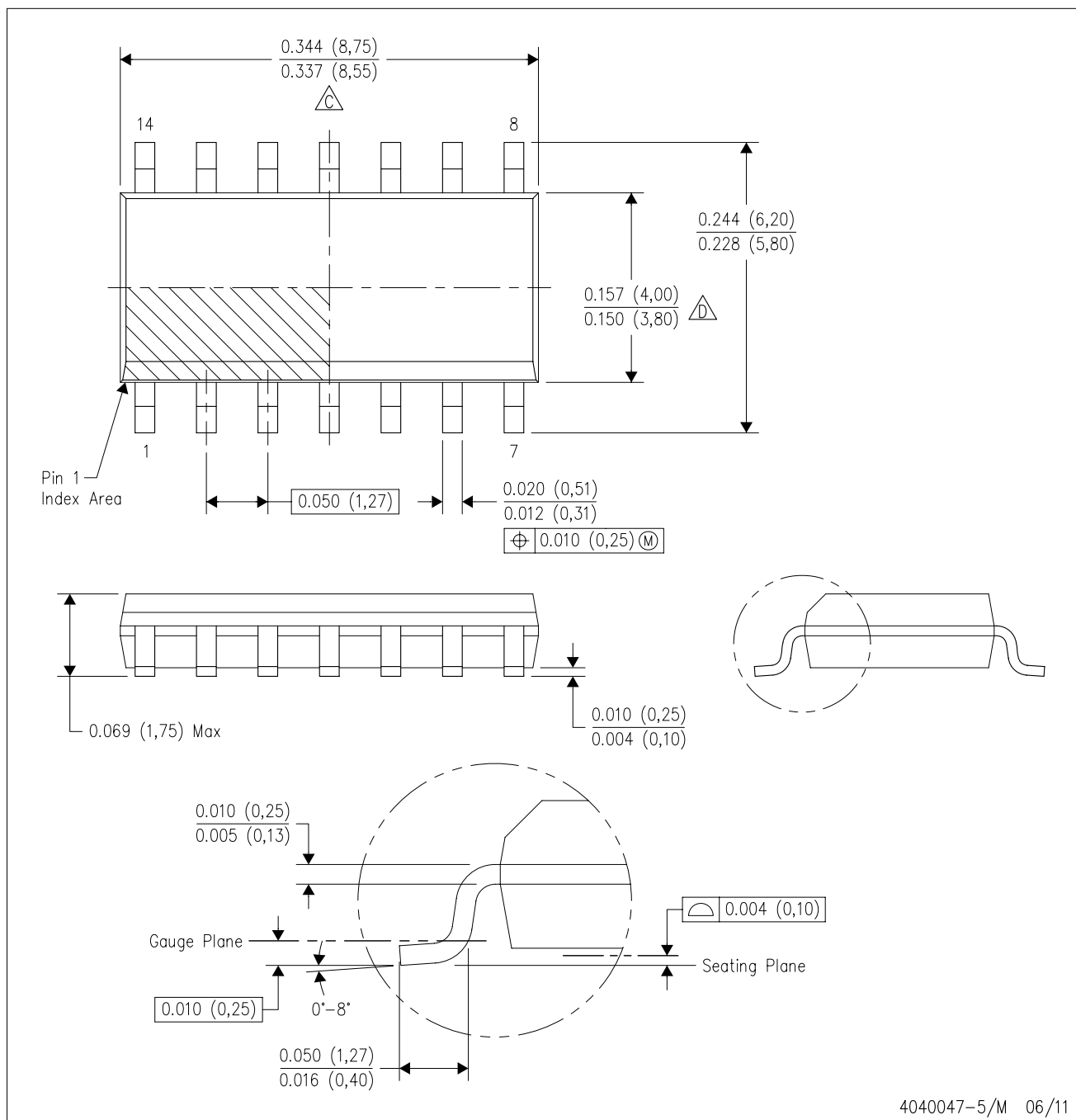


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA205ADR	SOIC	D	8	3000	356.0	356.0	35.0
OPA205ADT	SOIC	D	8	250	210.0	185.0	35.0
OPA2205ADGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
OPA2205ADGKT	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2205ADR	SOIC	D	8	3000	356.0	356.0	35.0
OPA2205ADT	SOIC	D	8	250	210.0	185.0	35.0
OPA4205ADR	SOIC	D	14	3000	356.0	356.0	35.0
OPA4205ADT	SOIC	D	14	250	210.0	185.0	35.0
OPA4205APWR	TSSOP	PW	14	3000	356.0	356.0	35.0
OPA4205APWT	TSSOP	PW	14	250	210.0	185.0	35.0

D (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040047-5/M 06/11

NOTES:

- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
- D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
- E. Reference JEDEC MS-012 variation AB.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



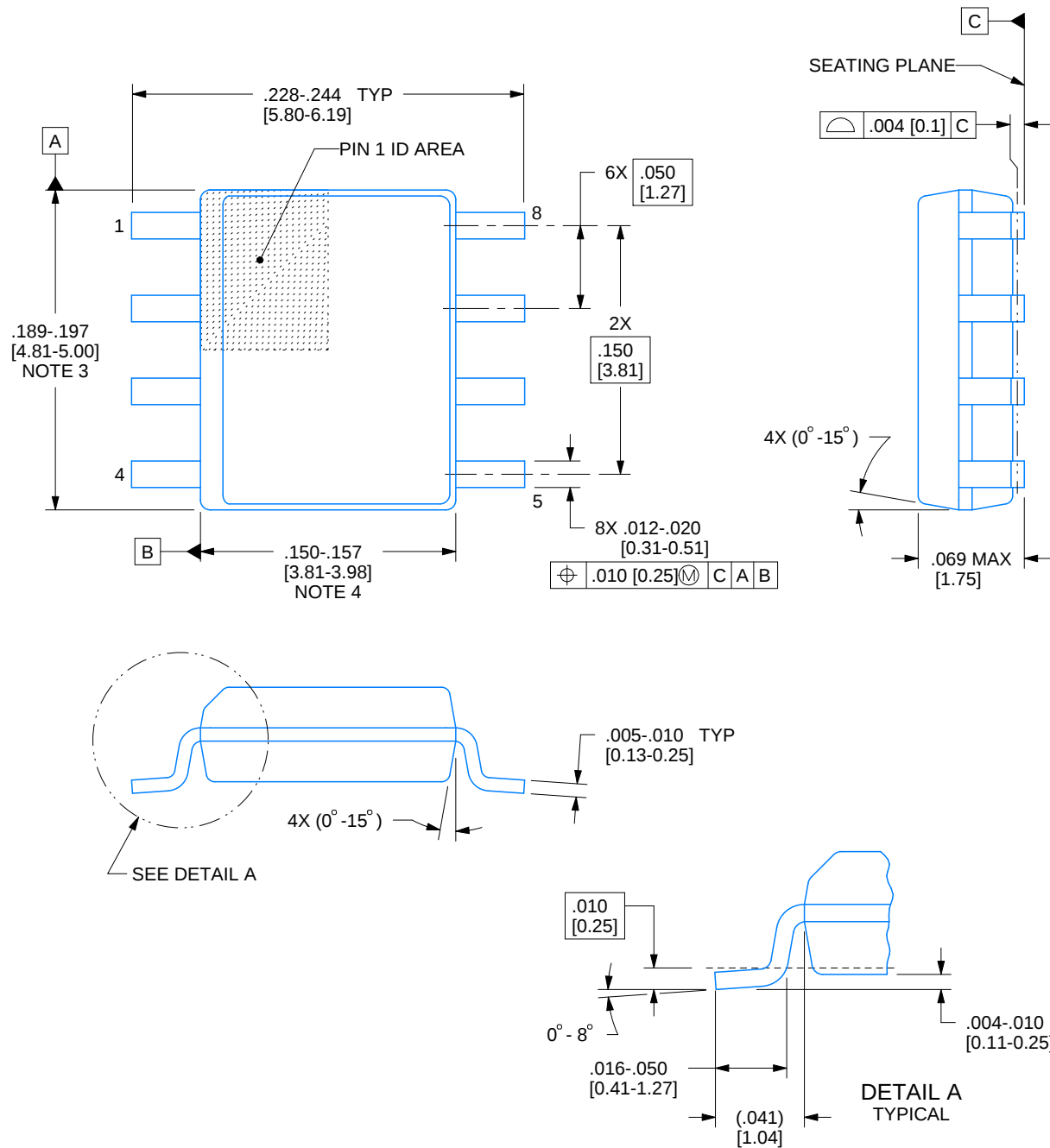
- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate designs.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

D0008A

PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



4214825/C 02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

EXAMPLE BOARD LAYOUT

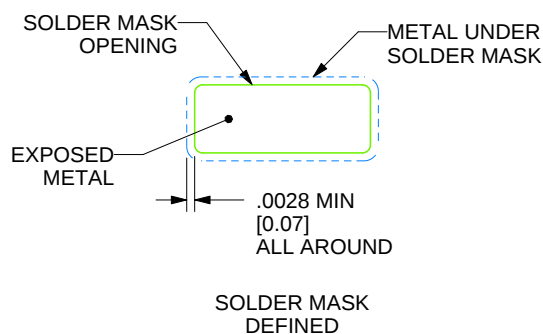
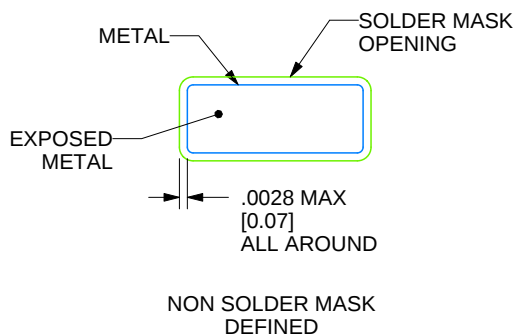
D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DGK (S-PDSO-G8)

PLASTIC SMALL-OUTLINE PACKAGE



4073329/E 05/06

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
 - E. Falls within JEDEC MO-187 variation AA, except interlead flash.

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