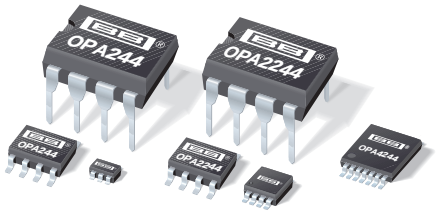
BURR-BROWN®



OPA244
OPA2244
OPA4244

*Micro*Power, Single-Supply OPERATIONAL AMPLIFIERS
*Micro*Amplifier™ Series

FEATURES

- ***Micro*SIZE PACKAGES**
  - **OPA244 (Single): SOT-23-5**
  - **OPA2244 (Dual): MSOP-8**
  - **OPA4244 (Quad): TSSOP-14**
- ***Micro*POWER: I_Q = 50μA/channel**
- **SINGLE SUPPLY OPERATION**
- **WIDE BANDWIDTH: 430kHz**
- **WIDE SUPPLY RANGE:**
  - **Single Supply: 2.2V to 36V**
  - **Dual Supply: ±1.1V to ±18V**

APPLICATIONS

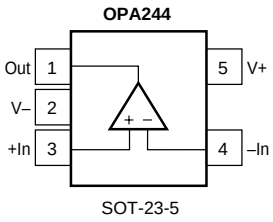
- **BATTERY POWERED SYSTEMS**
- **PORTABLE EQUIPMENT**
- **PCMCIA CARDS**
- **BATTERY PACKS AND POWER SUPPLIES**
- **CONSUMER PRODUCTS**

DESCRIPTION

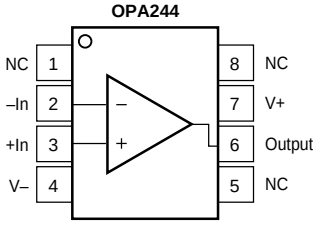
The OPA244 (single), OPA2244 (dual), and OPA4244 (quad) op amps are designed for very low quiescent current (50μA/channel), yet achieve excellent bandwidth. Ideal for battery powered and portable instrumentation, all versions are offered in micro packages for space-limited applications. The dual and quad versions feature completely independent circuitry for lowest crosstalk and freedom from interaction, even when overdriven or overloaded.

The OPA244 series is easy to use and free from phase inversion and overload problems found in some other op amps. These amplifiers are stable in unity gain and excellent performance is maintained as they swing to their specified limits. They can be operated from single (+2.2V to +36V) or dual supplies (±1.1V to ±18V). The input common-mode voltage range includes ground—ideal for many single supply applications. All versions have similar performance. However, there are some differences, such as common-mode rejection. All versions are interchangeable in most applications.

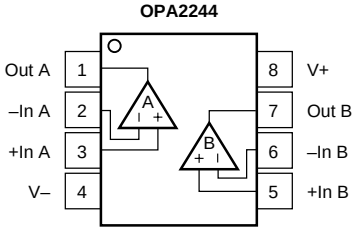
All versions are offered in miniature, surface-mount packages. OPA244 (single version) comes in the tiny 5-lead SOT-23-5 surface mount, SO-8 surface mount, and 8-pin DIP. OPA2244 (dual version) is available in the MSOP-8 surface mount, SO-8 surface-mount, and 8-pin DIP. The OPA4244 (quad) comes in the TSSOP-14 surface mount. They are fully specified from –40°C to +85°C and operate from –55°C to +125°C. A SPICE Macromodel is available for design analysis.



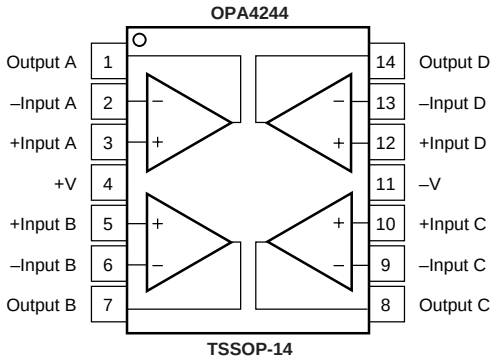
SOT-23-5



8-Pin DIP, SO-8



8-Pin DIP, SO-8, MSOP-8



TSSOP-14

International Airport Industrial Park • Mailing Address: PO Box 11400, Tucson, AZ 85734 • Street Address: 6730 S. Tucson Blvd., Tucson, AZ 85706 • Tel: (520) 746-1111
Twx: 910-952-1111 • Internet: http://www.burr-brown.com/ • Cable: BBRCORP • Telex: 066-6491 • FAX: (520) 889-1510 • Immediate Product Info: (800) 548-6132

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SPECIFICATIONS: V_S = +2.6V to +36V

Boldface limits apply over the specified temperature range, **T_A = –40°C to +85°C**

At T_A = +25°C, R_L = 20kΩ connected to ground, unless otherwise noted.

PARAMETER		CONDITION	OPA244NA, PA, UA MIN	OPA244NA, PA, UA TYP(1)	OPA244NA, PA, UA MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = ±7.5V, V_{CM} = 0		±0.7	±1.5	mV
T_A = –40°C to 85°C					**±2**	mV
vs Temperature	dV_{OS}/dT	**T_A = –40°C to 85°C**		**±4**		µV/°C
vs Power Supply	PSRR	V_S = +2.6V to +36V		5	50	µV/V
T_A = –40°C to 85°C		V_S = +2.6V to +36V			**50**	µV/V
INPUT BIAS CURRENT						
Input Bias Current	I_B	V_{CM} = V_S/2		–10	–25	nA
Input Offset Current	I_{OS}	V_{CM} = V_S/2		±1	±10	nA
NOISE						
Input Voltage Noise, f = 0.1kHz to 10kHz				0.4		µVp-p
Input Voltage Noise Density, f = 1kHz	e_n			22		nV/√Hz
Current Noise Density, f = 1kHz	i_n			40		fA/√Hz
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		0		(V+) – 0.9	V
Common-Mode Rejection	CMRR	V_S = ±18V, V_{CM} = –18V to +17.1V	84	98		dB
T_A = –40°C to 85°C		V_S = ±18V, V_{CM} = –18V to +17.1V	**84**			dB
INPUT IMPEDANCE						
Differential				10^6 || 2		Ω || pF
Common-Mode				10^9 || 2		Ω || pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	V_O = 0.5V to (V+) – 0.9	86	106		dB
T_A = –40°C to 85°C		V_O = 0.5V to (V+) – 0.9	**86**			dB
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW			430		kHz
Slew Rate	SR	G = 1		–0.1/+0.16		V/µs
Settling Time 0.01%		10V Step		150		µs
Overload Recovery Time		V_{IN} • Gain = V_S		8		µs
OUTPUT						
Voltage Output, Positive	V_O	A_{OL} ≥ 80dB, R_L = 20kΩ to V_S/2	(V+) – 0.9	(V+) – 0.75		V
T_A = –40°C to 85°C		A_{OL} ≥ 80dB, R_L = 20kΩ to V_S/2	**(V+) – 0.9**	(V+) – 0.75		V
Voltage Output, Negative		A_{OL} ≥ 80dB, R_L = 20kΩ to V_S/2	0.5	0.2		V
T_A = –40°C to 85°C		A_{OL} ≥ 80dB, R_L = 20kΩ to V_S/2	**0.5**	**0.2**		V
Voltage Output, Positive		A_{OL} ≥ 80dB, R_L = 20kΩ to Ground		(V+) – 0.75		V
T_A = –40°C to 85°C		A_{OL} ≥ 80dB, R_L = 20kΩ to Ground		(V+) – 0.75		V
Voltage Output, Negative		A_{OL} ≥ 80dB, R_L = 20kΩ to Ground		0.1		V
T_A = –40°C to 85°C		A_{OL} ≥ 80dB, R_L = 20kΩ to Ground		**0.1**		V
Short-Circuit Current	I_{SC}			–25/+12		mA
Capacitive Load Drive	C_{LOAD}			See Typical Curve		
POWER SUPPLY						
Specified Voltage Range	V_S	**T_A = –40°C to 85°C**	**+2.6**		**+36**	V
Minimum Operating Voltage				+2.2		V
Quiescent Current	I_Q	I_O = 0		50	60	µA
T_A = –40°C to 85°C		I_O = 0			**70**	µA
TEMPERATURE RANGE						
Specified Range			–40		85	°C
Operating Range			–55		125	°C
Storage Range			–65		150	°C
Thermal Resistance	θ_{JA}					
SOT-23-5 Surface-Mount				200		°C/W
SO-8 Surface-Mount				150		°C/W
8-Pin DIP				100		°C/W

NOTE: (1) V_S = +15V.

The information provided herein is believed to be reliable; however, BURR-BROWN assumes no responsibility for inaccuracies or omissions. BURR-BROWN assumes no responsibility for the use of this information, and all use of such information shall be entirely at the user's own risk. Prices and specifications are subject to change without notice. No patent rights or licenses to any of the circuits described herein are implied or granted to any third party. BURR-BROWN does not authorize or warrant any BURR-BROWN product for use in life support devices and/or systems.

SPECIFICATIONS: V_S = +2.6V to +36V

Boldface limits apply over the specified temperature range, **T_A = –40°C to +85°C**

At T_A = +25°C, R_L = 20kΩ connected to ground, unless otherwise noted.

PARAMETER		CONDITION	OPA2244EA, PA, UA MIN	OPA2244EA, PA, UA TYP(1)	OPA2244EA, PA, UA MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = ±7.5V, V_{CM} = 0		±0.7	±1.5	mV
T_A = –40°C to 85°C					**±2**	mV
vs Temperature	dV_{OS}/dT	**T_A = –40°C to 85°C**		**±4**		µV/°C
vs Power Supply	PSRR	V_S = +2.6V to +36V		5	50	µV/V
T_A = –40°C to 85°C		V_S = +2.6V to +36V			**50**	µV/V
Channel Separation				140		dB
INPUT BIAS CURRENT						
Input Bias Current	I_B	$V_{CM} = V_S/2$		–10	–25	nA
Input Offset Current	I_{OS}	$V_{CM} = V_S/2$		±1	±10	nA
NOISE						
Input Voltage Noise, f = 0.1kHz to 10kHz				0.4		µVp-p
Input Voltage Noise Density, f = 1kHz	e_n			22		nV/√Hz
Current Noise Density, f = 1kHz	i_n			40		fA/√Hz
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		0		(V+) – 0.9	V
Common-Mode Rejection	CMRR	V_S = ±18V, V_{CM} = –18V to +17.1V	72	98		dB
T_A = –40°C to 85°C		V_S = ±18V, V_{CM} = –18V to +17.1V	**72**			dB
INPUT IMPEDANCE						
Differential				10^6 || 2		Ω || pF
Common-Mode				10^9 || 2		Ω || pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	V_O = 0.5V to (V+) – 0.9	86	106		dB
T_A = –40°C to 85°C		V_O = 0.5V to (V+) – 0.9	**86**			dB
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW			430		kHz
Slew Rate	SR	G = 1		–0.1/+0.16		V/µs
Settling Time 0.01%		10V Step		150		µs
Overload Recovery Time		V_{IN} • Gain = V_S		8		µs
OUTPUT						
Voltage Output, Positive	V_O	A_{OL} ≥ 80dB, R_L = 20kΩ to $V_S/2$	(V+) – 0.9	(V+) – 0.75		V
T_A = –40°C to 85°C		A_{OL} ≥ 80dB, R_L = 20kΩ to $V_S/2$	**(V+) – 0.9**	(V+) – 0.75		V
Voltage Output, Negative		A_{OL} ≥ 80dB, R_L = 20kΩ to $V_S/2$	0.5	0.2		V
T_A = –40°C to 85°C		A_{OL} ≥ 80dB, R_L = 20kΩ to $V_S/2$	**0.5**	**0.2**		V
Voltage Output, Positive		A_{OL} ≥ 80dB, R_L = 20kΩ to Ground		(V+) – 0.75		V
T_A = –40°C to 85°C		A_{OL} ≥ 80dB, R_L = 20kΩ to Ground		(V+) – 0.75		V
Voltage Output, Negative		A_{OL} ≥ 80dB, R_L = 20kΩ to Ground		0.1		V
T_A = –40°C to 85°C		A_{OL} ≥ 80dB, R_L = 20kΩ to Ground		**0.1**		V
Short-Circuit Current	I_{SC}			–25/+12		mA
Capacitive Load Drive	C_{LOAD}			See Typical Curve		
POWER SUPPLY						
Specified Voltage Range	V_S	**T_A = –40°C to 85°C**	**+2.6**		**+36**	V
Minimum Operating Voltage				+2.2		V
Quiescent Current (per amplifier)	I_Q	I_O = 0		40	50	µA
T_A = –40°C to 85°C		I_O = 0			**63**	µA
TEMPERATURE RANGE						
Specified Range			–40		85	°C
Operating Range			–55		125	°C
Storage Range			–65		150	°C
Thermal Resistance	θ_{JA}					
MSOP-8 Surface-Mount				200		°C/W
SO-8 Surface-Mount				150		°C/W
8-Pin DIP				100		°C/W

NOTE: (1) V_S = +15V.

SPECIFICATIONS: V_S = +2.6V to +36V

Boldface limits apply over the specified temperature range, **T_A = –40°C to +85°C**

At T_A = +25°C, R_L = 20kΩ connected to ground, unless otherwise noted.

PARAMETER		CONDITION	OPA4244EA MIN	OPA4244EA TYP[1]	OPA4244EA MAX	UNITS
OFFSET VOLTAGE						
Input Offset Voltage	V_{OS}	V_S = ±7.5V, V_{CM} = 0		±0.7	±1.5	mV
T_A = –40°C to 85°C					**±2**	mV
vs Temperature	dV_{OS}/dT	**T_A = –40°C to 85°C**		**±4**		µV/°C
vs Power Supply	PSRR	V_S = +2.6V to +36V		5	50	µV/V
T_A = –40°C to 85°C		V_S = +2.6V to +36V			**50**	µV/V
Channel Separation				140		dB
INPUT BIAS CURRENT						
Input Bias Current	I_B	$V_{CM} = V_S/2$		–10	–25	nA
Input Offset Current	I_{OS}	$V_{CM} = V_S/2$		±1	±10	nA
NOISE						
Input Voltage Noise, f = 0.1kHz to 10kHz				0.4		µVp-p
Input Voltage Noise Density, f = 1kHz	e_n			22		$nV/\sqrt{Hz}$
Current Noise Density, f = 1kHz	i_n			40		$fA/\sqrt{Hz}$
INPUT VOLTAGE RANGE						
Common-Mode Voltage Range	V_{CM}		0		(V+) – 0.9	V
Common-Mode Rejection	CMRR	V_S = ±18V, V_{CM} = –18V to +17.1V	82	104		dB
T_A = –40°C to 85°C		V_S = ±18V, V_{CM} = –18V to +17.1V	**82**			dB
INPUT IMPEDANCE						
Differential				10^6 || 2		Ω || pF
Common-Mode				10^9 || 2		Ω || pF
OPEN-LOOP GAIN						
Open-Loop Voltage Gain	A_{OL}	V_O = 0.5V to (V+) – 0.9	86	106		dB
T_A = –40°C to 85°C		V_O = 0.5V to (V+) – 0.9	**86**			dB
FREQUENCY RESPONSE						
Gain-Bandwidth Product	GBW			430		kHz
Slew Rate	SR	G = 1		–0.1/+0.16		V/µs
Settling Time 0.01%		10V Step		150		µs
Overload Recovery Time		V_{IN} • Gain = V_S		8		µs
OUTPUT						
Voltage Output, Positive	V_O	A_{OL} ≥ 80dB, R_L = 20kΩ to $V_S/2$	(V+) – 0.9	(V+) – 0.75		V
T_A = –40°C to 85°C		A_{OL} ≥ 80dB, R_L = 20kΩ to $V_S/2$	**(V+) – 0.9**	(V+) – 0.75		V
Voltage Output, Negative		A_{OL} ≥ 80dB, R_L = 20kΩ to $V_S/2$	0.5	0.2		V
T_A = –40°C to 85°C		A_{OL} ≥ 80dB, R_L = 20kΩ to $V_S/2$	**0.5**	**0.2**		V
Voltage Output, Positive		A_{OL} ≥ 80dB, R_L = 20kΩ to Ground		(V+) – 0.75		V
T_A = –40°C to 85°C		A_{OL} ≥ 80dB, R_L = 20kΩ to Ground		(V+) – 0.75		V
Voltage Output, Negative		A_{OL} ≥ 80dB, R_L = 20kΩ to Ground		0.1		V
T_A = –40°C to 85°C		A_{OL} ≥ 80dB, R_L = 20kΩ to Ground		**0.1**		V
Short-Circuit Current	I_{SC}			–25/+12		mA
Capacitive Load Drive	C_{LOAD}			See Typical Curve		
POWER SUPPLY						
Specified Voltage Range	V_S	**T_A = –40°C to 85°C**	**+2.6**		**+36**	V
Minimum Operating Voltage				+2.2		V
Quiescent Current (per amplifier)	I_Q	I_O = 0		40	60	µA
T_A = –40°C to 85°C		I_O = 0			**70**	µA
TEMPERATURE RANGE						
Specified Range			–40		85	°C
Operating Range			–55		125	°C
Storage Range			–65		150	°C
Thermal Resistance	θ_{JA}					
TSSOP-14 Surface Mount				100		°C/W

NOTE: (1) V_S = +15V.

ABSOLUTE MAXIMUM RATINGS[1]

Supply Voltage, V+ to V–	36V
Input Voltage Range[2]	(V–) – 0.3V to (V+) + 0.3V
Input Current[2]	10mA
Output Short-Circuit[3]	Continuous
Operating Temperature	–55°C to +125°C
Storage Temperature	–65°C to +150°C
Junction Temperature	150°C
Lead Temperature (soldering, 10s)	300°C
ESD Capability	2000V

NOTES: (1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. (2) Inputs are diode-clamped to the supply rails and should be current-limited to 10mA or less if input voltages can exceed rails by more than 0.3V. (3) Short-circuit to ground, one amplifier per package.



ELECTROSTATIC DISCHARGE SENSITIVITY

This integrated circuit can be damaged by ESD. Burr-Brown recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

PACKAGE/ORDERING INFORMATION

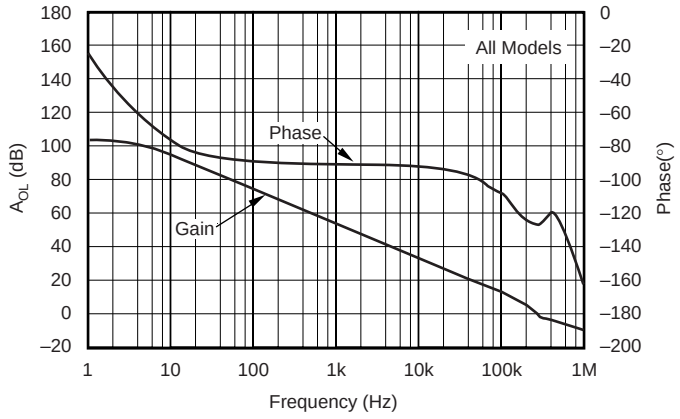
PRODUCT	PACKAGE	PACKAGE DRAWING NUMBER	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER[1]	TRANSPORT MEDIA
Single						
OPA244NA	SOT-23-5 Surface-Mount	331	–40°C to +85°C	A44	OPA244NA/250	Tape and Reel
"	"	"	"	"	OPA244NA/3K	Tape and Reel
OPA244PA	8-Pin DIP	006	–40°C to +85°C	OPA244PA	OPA244PA	Rails
OPA244UA	SO-8 Surface-Mount	182	–40°C to +85°C	OPA244UA	OPA244UA	Rails
"	"	"	"	"	OPA244UA/2K5	Tape and Reel
Dual						
OPA2244EA	MSOP-8 Surface-Mount	337	–40°C to +85°C	A44	OPA2244EA/250	Tape and Reel
"	"	"	"	"	OPA2244EA/2K5	Tape and Reel
OPA2244PA	8-Pin DIP	006	–40°C to +85°C	OPA2244PA	OPA2244PA	Rails
OPA2244UA	SO-8 Surface-Mount	182	–40°C to +85°C	OPA2244UA	OPA2244UA	Rails
"	"	"	"	"	OPA2244UA/2K5	Tape and Reel
Quad						
OPA4244EA	TSSOP-14 Surface-Mount	357	–40°C to +85°C	OPA4244EA	OPA4244EA/250	Tape and Reel
"	"	"	"	"	OPA4244EA/2K5	Tape and Reel

NOTE: (1) Products followed by a slash (/) are only available in Tape and Reel in the quantities indicated (e.g., /250 indicates 250 devices per reel). Ordering 3000 pieces of "OPA244NA/3K" will get a single 3000 piece Tape and Reel.

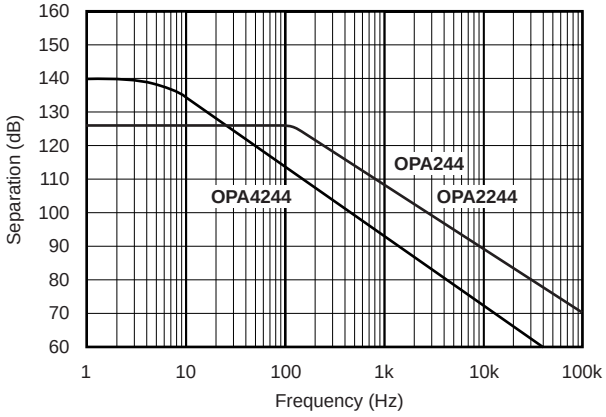
TYPICAL PERFORMANCE CURVES

At T_A = 25°C, V_S = +15V, and R_L = 20kΩ connected to Ground, unless otherwise noted.

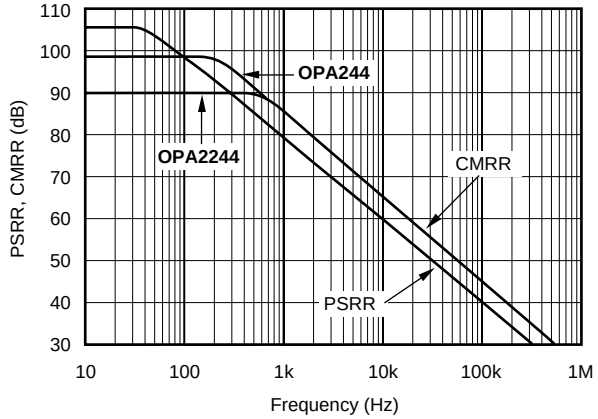
OPEN-LOOP GAIN AND PHASE vs FREQUENCY

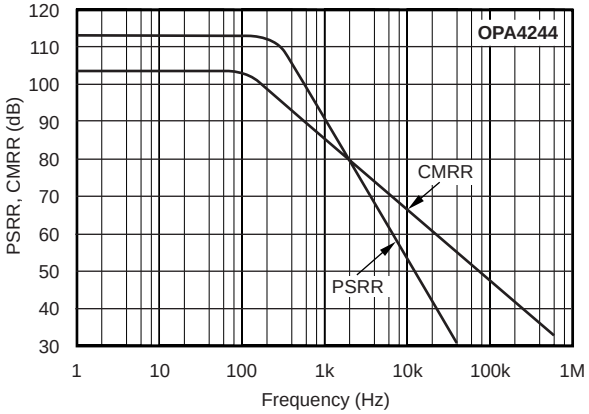


CHANNEL SEPARATION

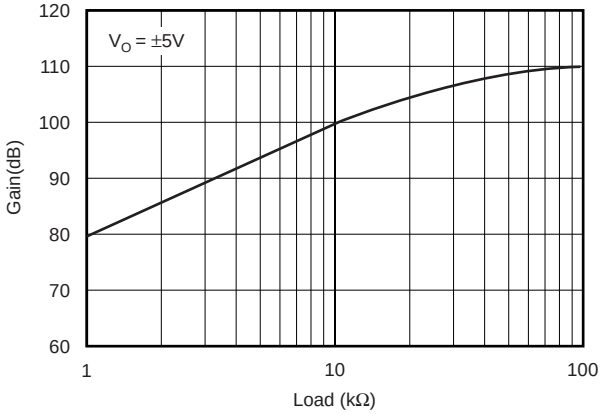


POWER SUPPLY AND COMMON-MODE REJECTION vs FREQUENCY

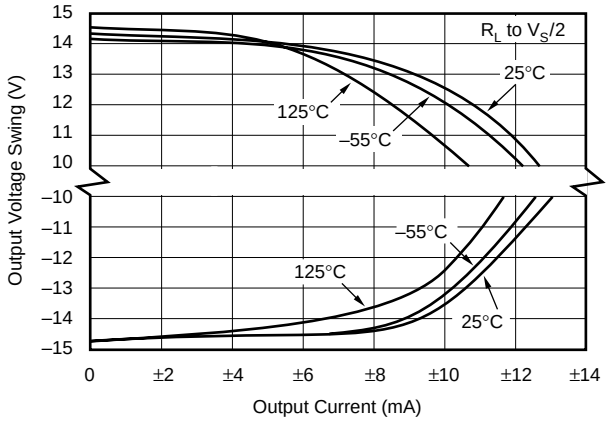




OPEN-LOOP GAIN vs LOAD RESISTANCE



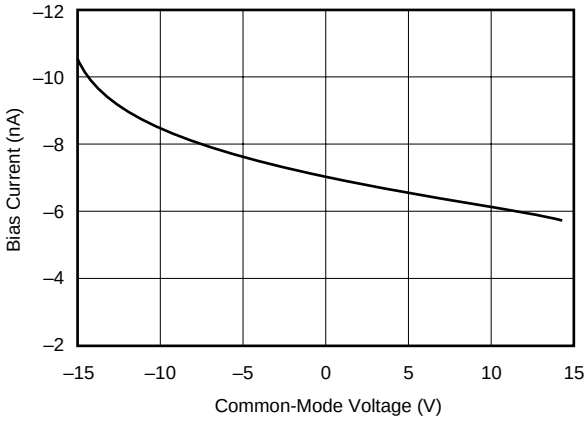
OUTPUT VOLTAGE SWING vs OUTPUT CURRENT



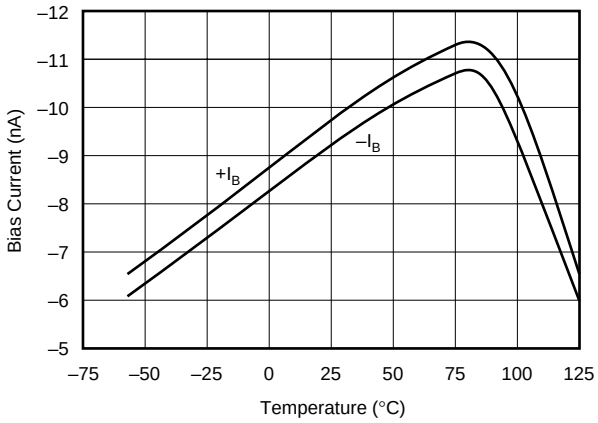
TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = 25°C, V_S = +15V, and R_L = 20kΩ connected to Ground, unless otherwise noted.

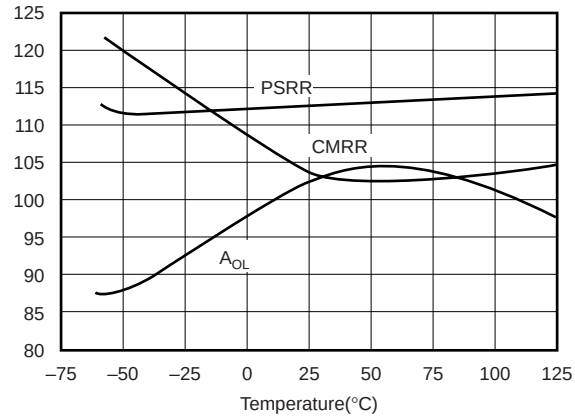
INPUT BIAS CURRENT
vs INPUT COMMON-MODE VOLTAGE



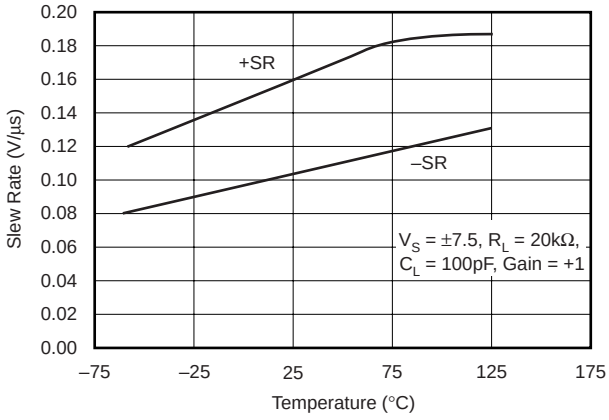
INPUT BIAS CURRENT vs TEMPERATURE



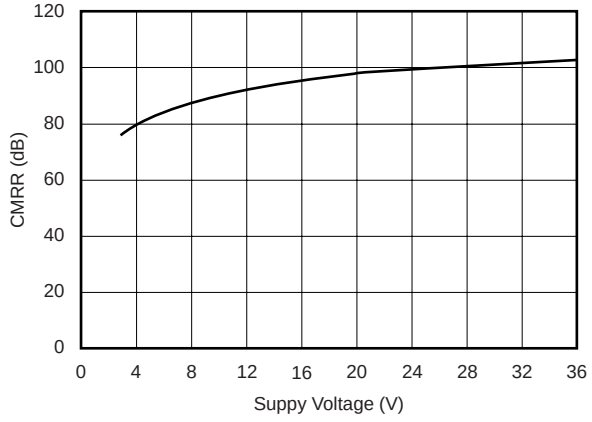
AOL, CMRR, PSRR vs TEMPERATURE



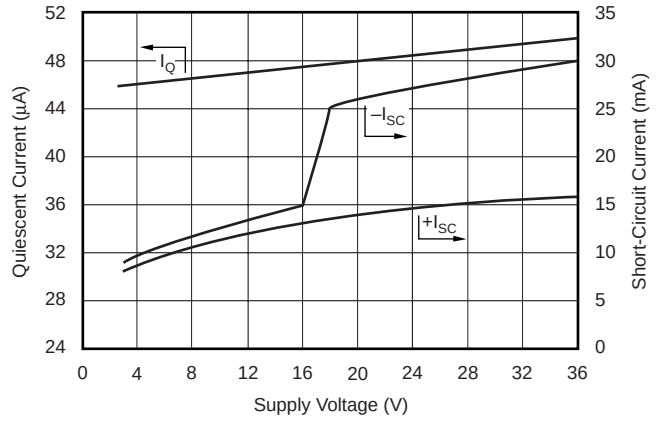
SLEW RATE vs TEMPERATURE



COMMON-MODE REJECTION
vs SUPPY VOLTAGE



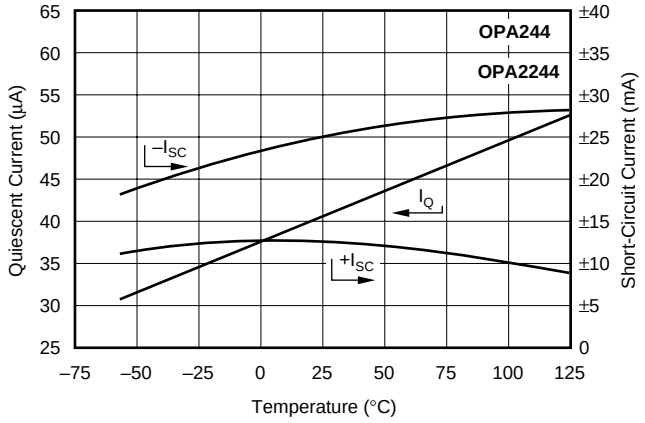
QUIESCENT CURRENT AND SHORT-CIRCUIT
vs SUPPLY VOLTAGE

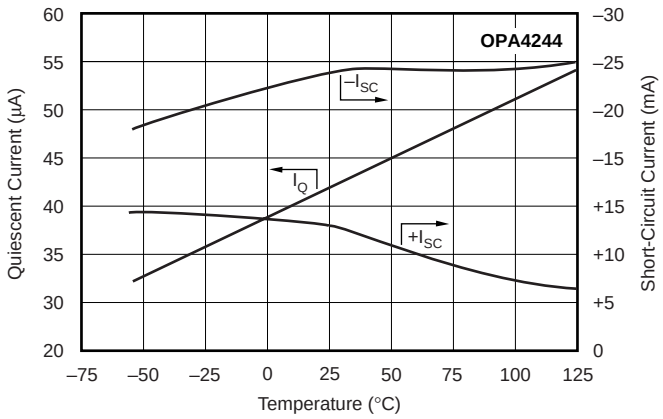


TYPICAL PERFORMANCE CURVES (Cont.)

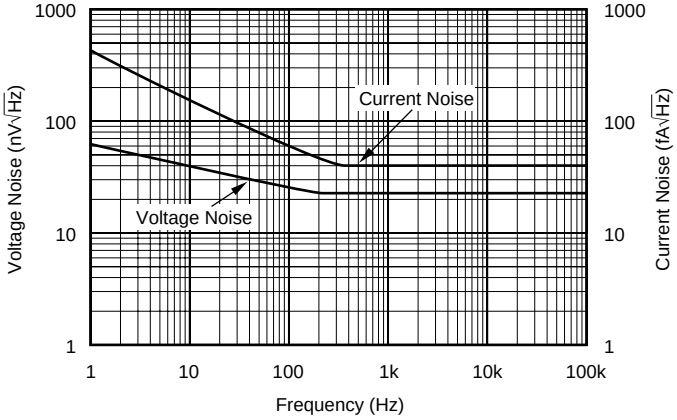
At T_A = 25°C, V_S = +15V, and R_L = 20kΩ connected to Ground, unless otherwise noted.

QUIESCENT AND SHORT-CIRCUIT CURRENT vs TEMPERATURE

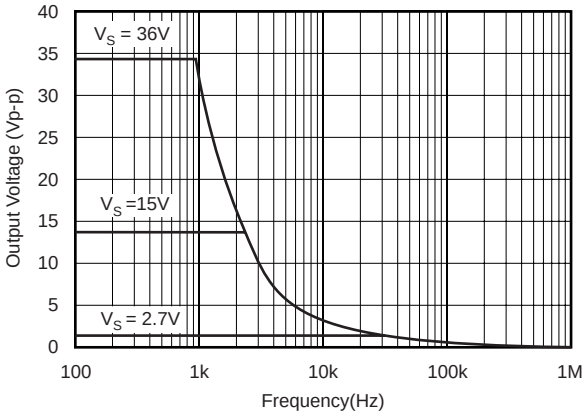




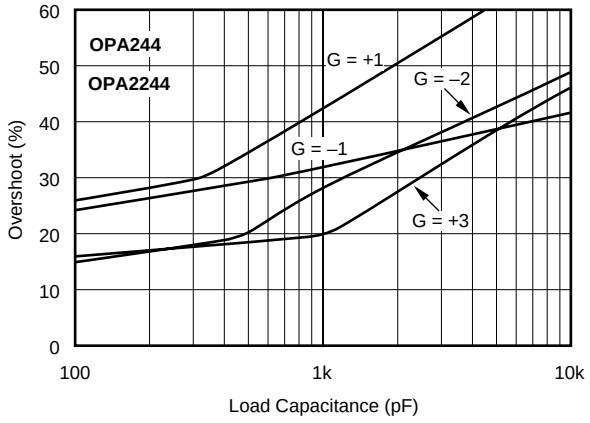
INPUT VOLTAGE AND CURRENT NOISE SPECTRAL DENSITY vs FREQUENCY

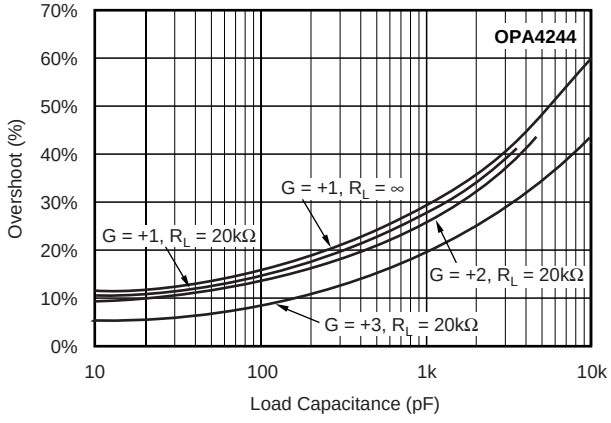


MAXIMUM OUTPUT VOLTAGE vs FREQUENCY



SMALL SIGNAL OVERSHOOT vs LOAD CAPACITANCE

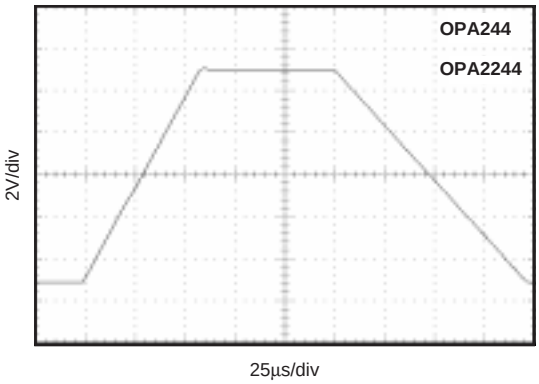


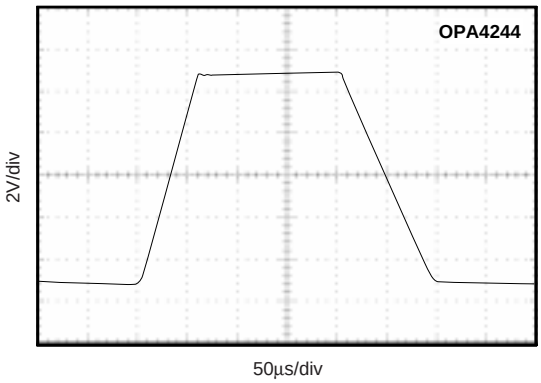


TYPICAL PERFORMANCE CURVES (Cont.)

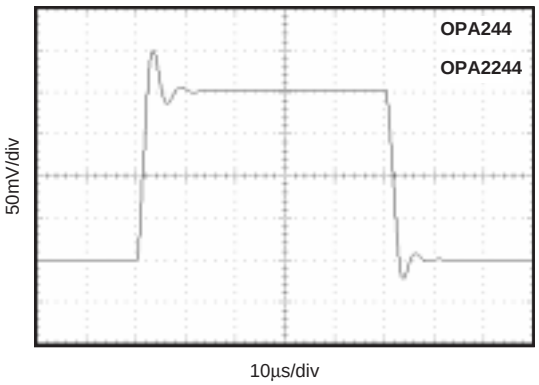
At T_A = 25°C, V_S = +15V, and R_L = 20kΩ connected to Ground, unless otherwise noted.

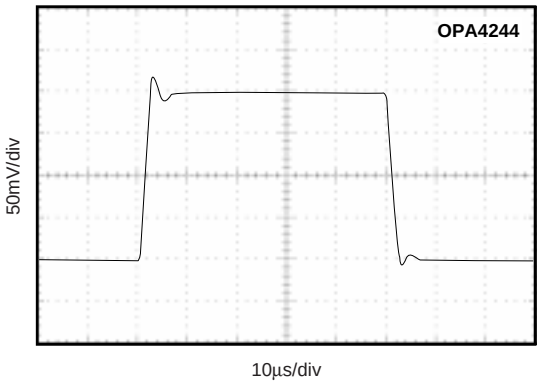
LARGE-SIGNAL STEP RESPONSE, G = 1, C_L = 100pF



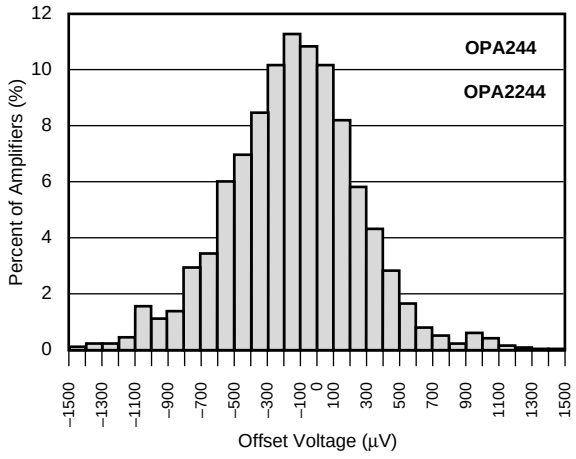


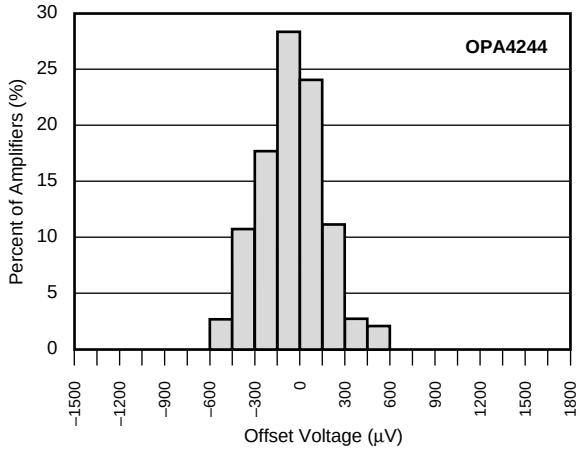
SMALL-SIGNAL STEP RESPONSE, G = 1, C_L = 100pF





OFFSET VOLTAGE PRODUCTION DISTRIBUTION

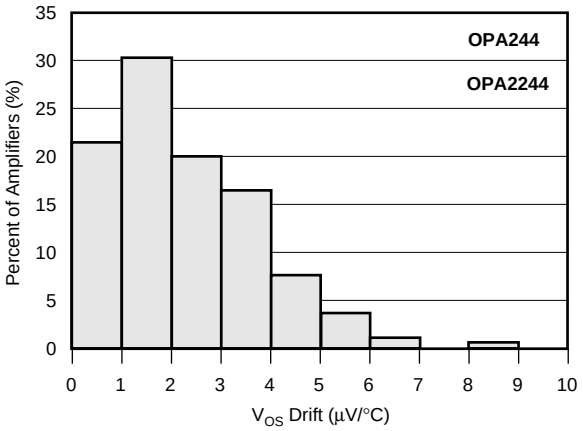


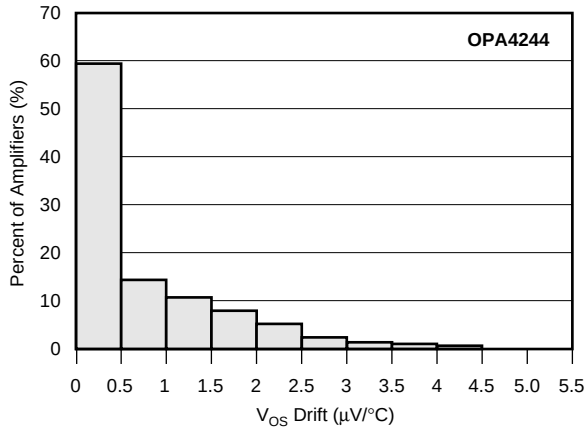


TYPICAL PERFORMANCE CURVES (Cont.)

At T_A = 25°C, V_S = +15V, and R_L = 20kΩ connected to Ground, unless otherwise noted.

OFFSET VOLTAGE PRODUCTION DISTRIBUTION





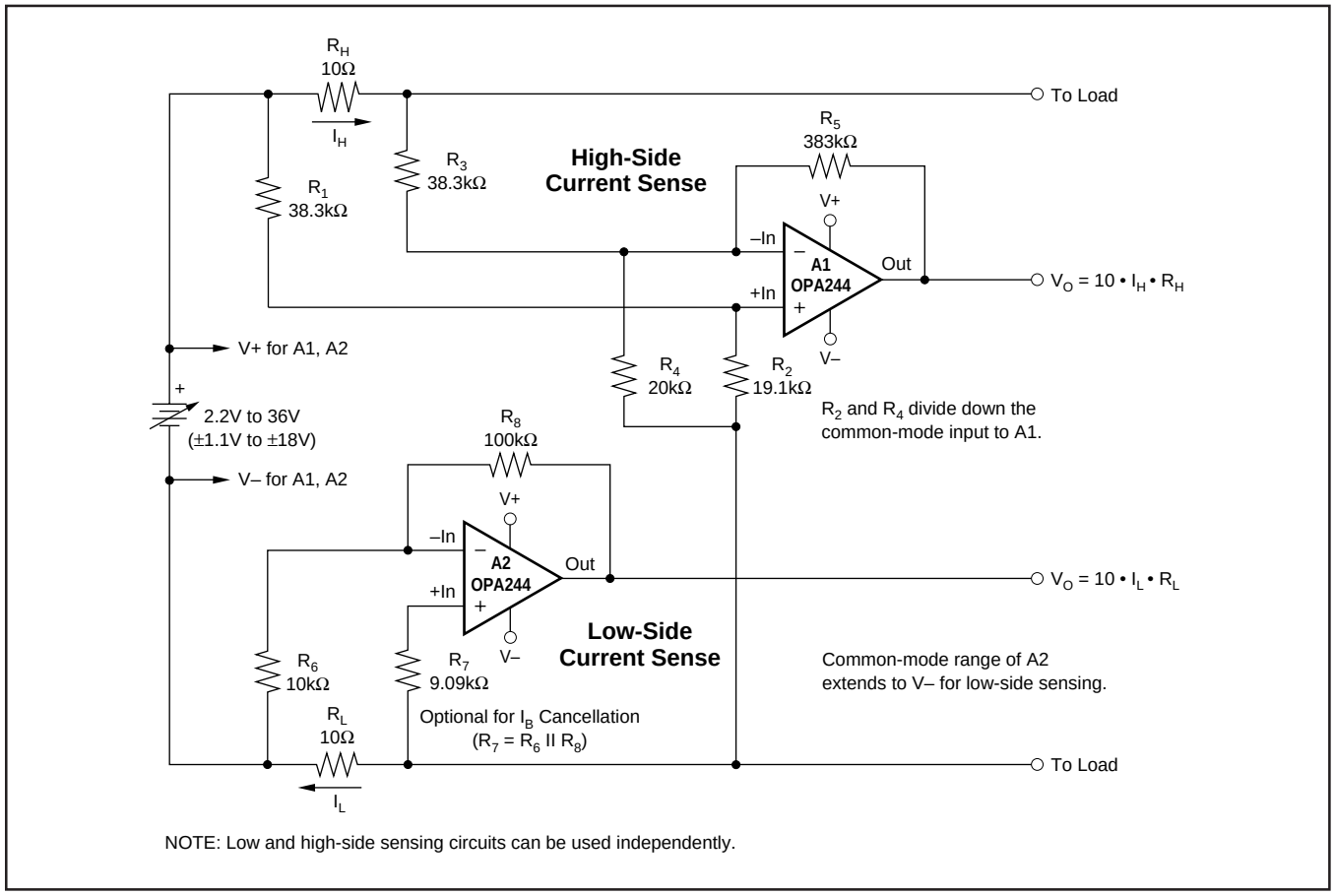
APPLICATIONS INFORMATION

The OPA244 is unity-gain stable and suitable for a wide range of general purpose applications. Power supply pins should be bypassed with 0.01µF ceramic capacitors.

OPERATING VOLTAGE

The OPA244 can operate from single supply (+2.2V to +36V) or dual supplies (±1.1 to ±18V) with excellent performance. Unlike most op amps which are specified at only one supply voltage, the OPA244 is specified for real world applications; a single set of specifications applies throughout the +2.6V to +36V (±1.3 to ±18V) supply range. This allows a designer to have the same assured performance at any supply voltage within this range. In addition, many key parameters are guaranteed over the specified temperature range, –40°C to +85°C. Most behavior remains unchanged throughout the full operating voltage range. Parameters which vary significantly with operating voltage or temperature are shown in typical performance curves.

Useful information on solder pad design for printed circuit boards can be found in Burr-Brown's Application Bulletin AB-132B, “Solder Pad Recommendations for Surface-Mount Devices,” easily found at Burr-Brown's web site (http://www.burr-brown.com).



NOTE: Low and high-side sensing circuits can be used independently.

FIGURE 1. Low and High-Side Battery Current Sensing.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
OPA2244EA/250	LIFEBUY	VSSOP	DGK	8	250	RoHS & Green	NIPDAU | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 85	A44	
OPA2244EA/250G4	LIFEBUY	VSSOP	DGK	8	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A44	
OPA2244EA/2K5	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A44	Samples
OPA2244EA/2K5G4	ACTIVE	VSSOP	DGK	8	2500	TBD	Call TI	Call TI	-40 to 85		Samples
OPA2244PA	LIFEBUY	PDIP	P	8	50	RoHS & Green	NIPDAU	N / A for Pkg Type		OPA2244PA	
OPA2244UA	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR		OPA 2244UA	
OPA2244UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR		OPA 2244UA	Samples
OPA2244UAG4	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR		OPA 2244UA	
OPA244NA/250	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A44	
OPA244NA/250G4	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A44	
OPA244NA/3K	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	A44	Samples
OPA244UA	LIFEBUY	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 244UA	
OPA244UA/2K5	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 244UA	Samples
OPA4244EA/250	LIFEBUY	TSSOP	PW	14	250	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 4244EA	
OPA4244EA/2K5	ACTIVE	TSSOP	PW	14	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	OPA 4244EA	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

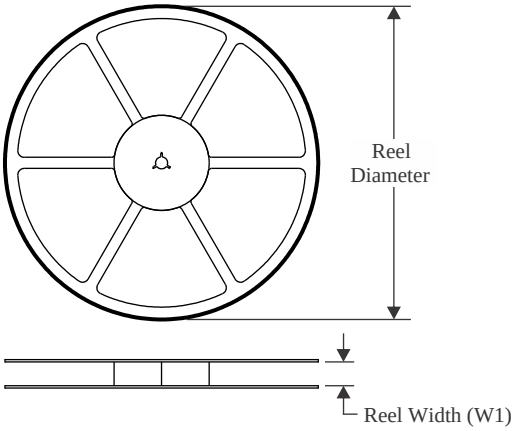
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

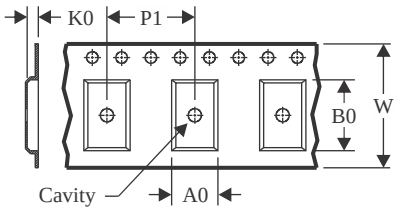
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

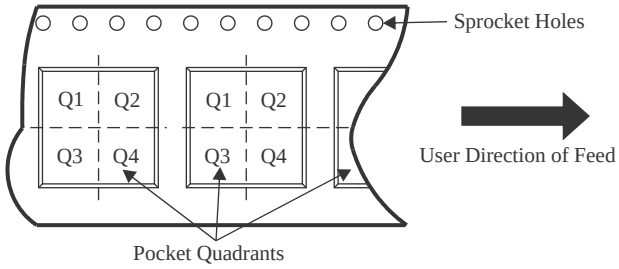


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

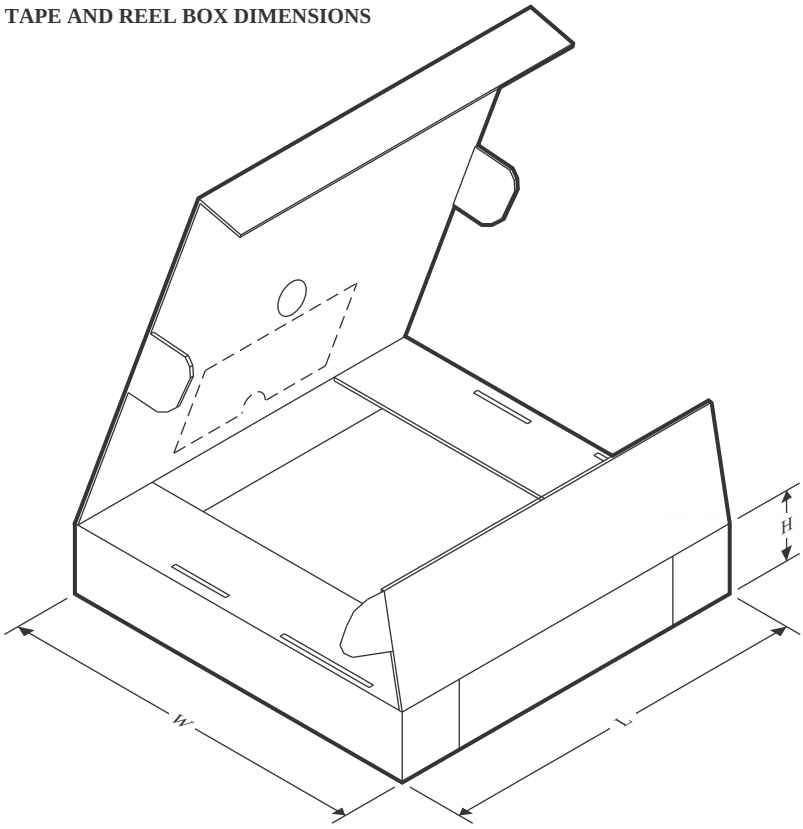
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
OPA2244EA/250	VSSOP	DGK	8	250	180.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2244EA/2K5	VSSOP	DGK	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
OPA2244UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA244NA/250	SOT-23	DBV	5	250	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
OPA244NA/3K	SOT-23	DBV	5	3000	178.0	8.4	3.3	3.2	1.4	4.0	8.0	Q3
OPA244UA/2K5	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
OPA4244EA/250	TSSOP	PW	14	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
OPA4244EA/2K5	TSSOP	PW	14	2500	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

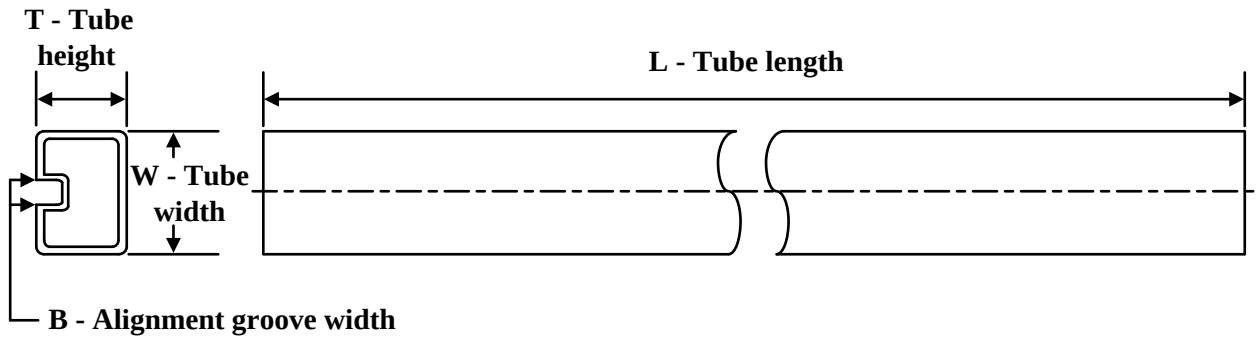
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
OPA2244EA/250	VSSOP	DGK	8	250	210.0	185.0	35.0
OPA2244EA/2K5	VSSOP	DGK	8	2500	356.0	356.0	35.0
OPA2244UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA244NA/250	SOT-23	DBV	5	250	565.0	140.0	75.0
OPA244NA/3K	SOT-23	DBV	5	3000	565.0	140.0	75.0
OPA244UA/2K5	SOIC	D	8	2500	356.0	356.0	35.0
OPA4244EA/250	TSSOP	PW	14	250	210.0	185.0	35.0
OPA4244EA/2K5	TSSOP	PW	14	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

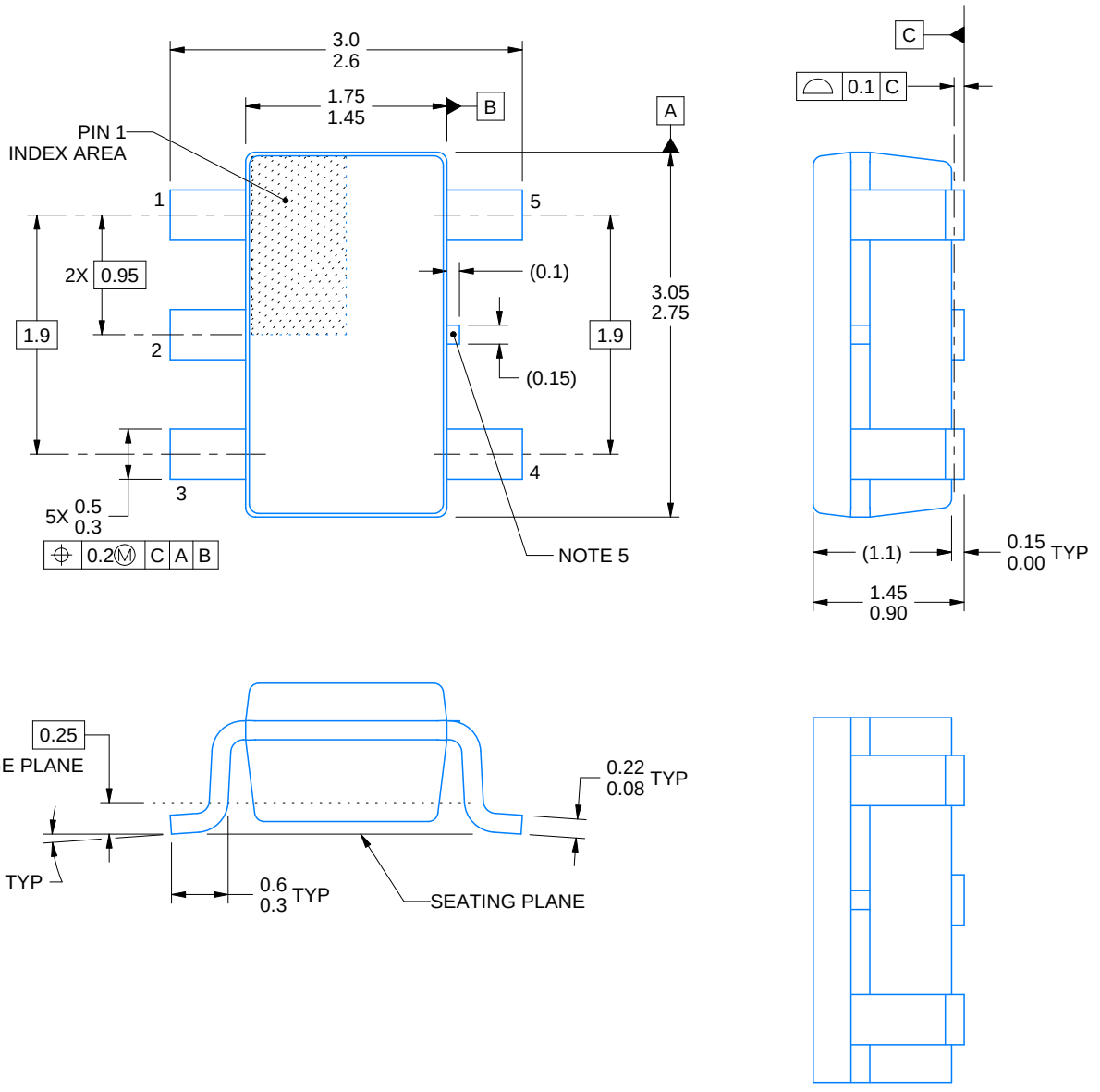
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
OPA2244PA	P	PDIP	8	50	506	13.97	11230	4.32
OPA2244UA	D	SOIC	8	75	506.6	8	3940	4.32
OPA2244UAG4	D	SOIC	8	75	506.6	8	3940	4.32
OPA244UA	D	SOIC	8	75	506.6	8	3940	4.32

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

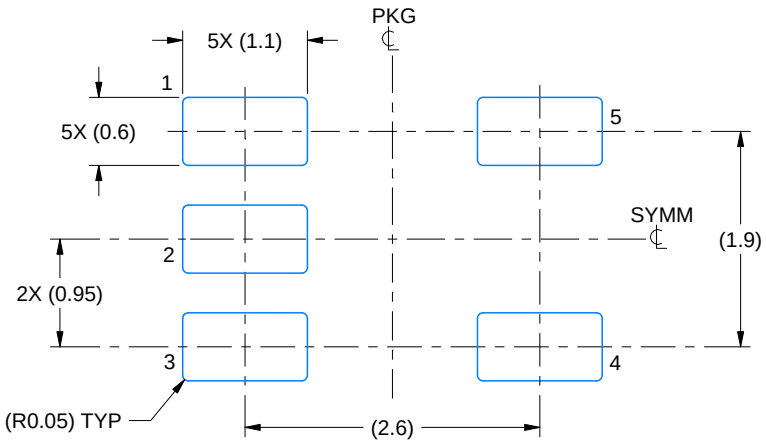


ALTERNATIVE PACKAGE SINGULATION VIEW

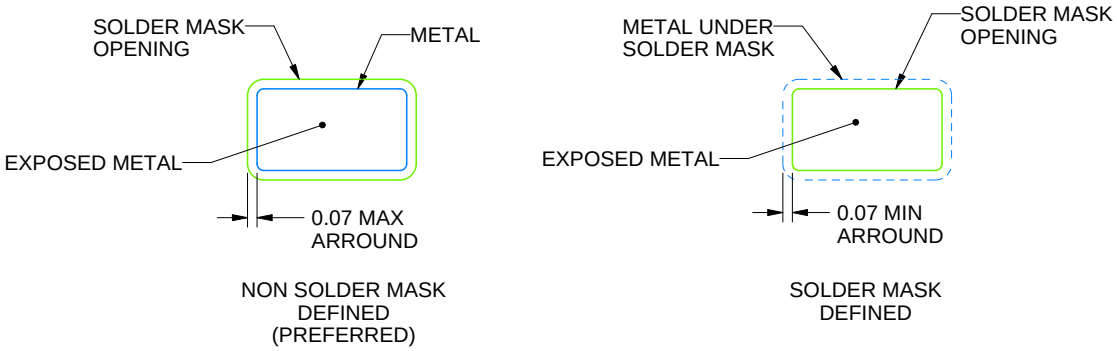
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

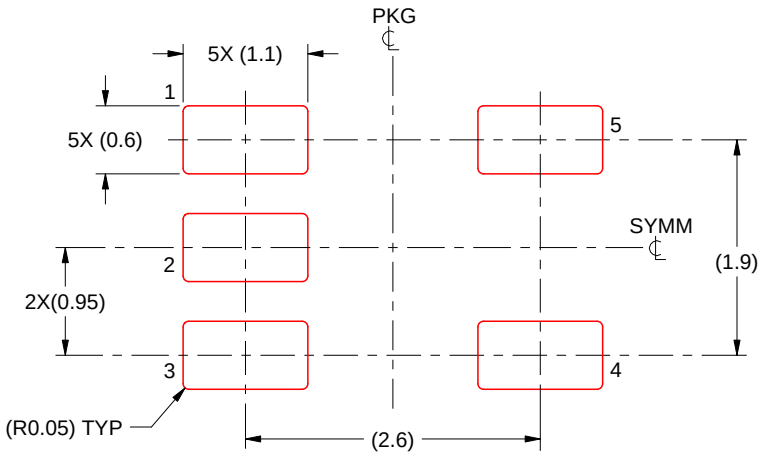


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



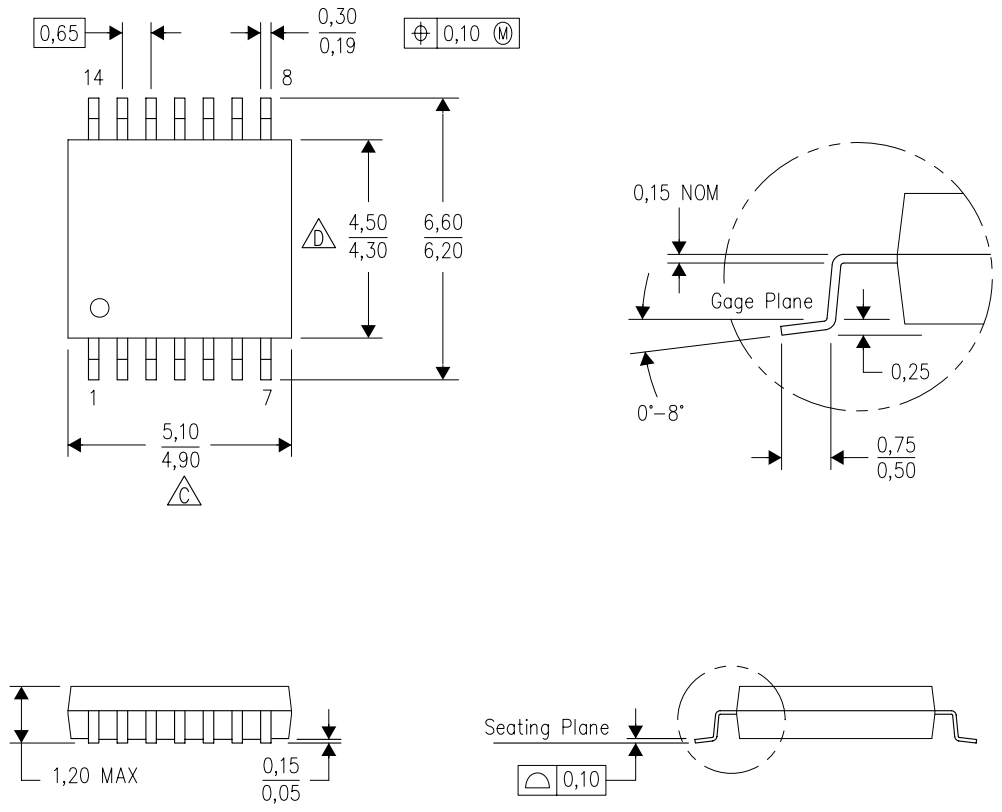
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

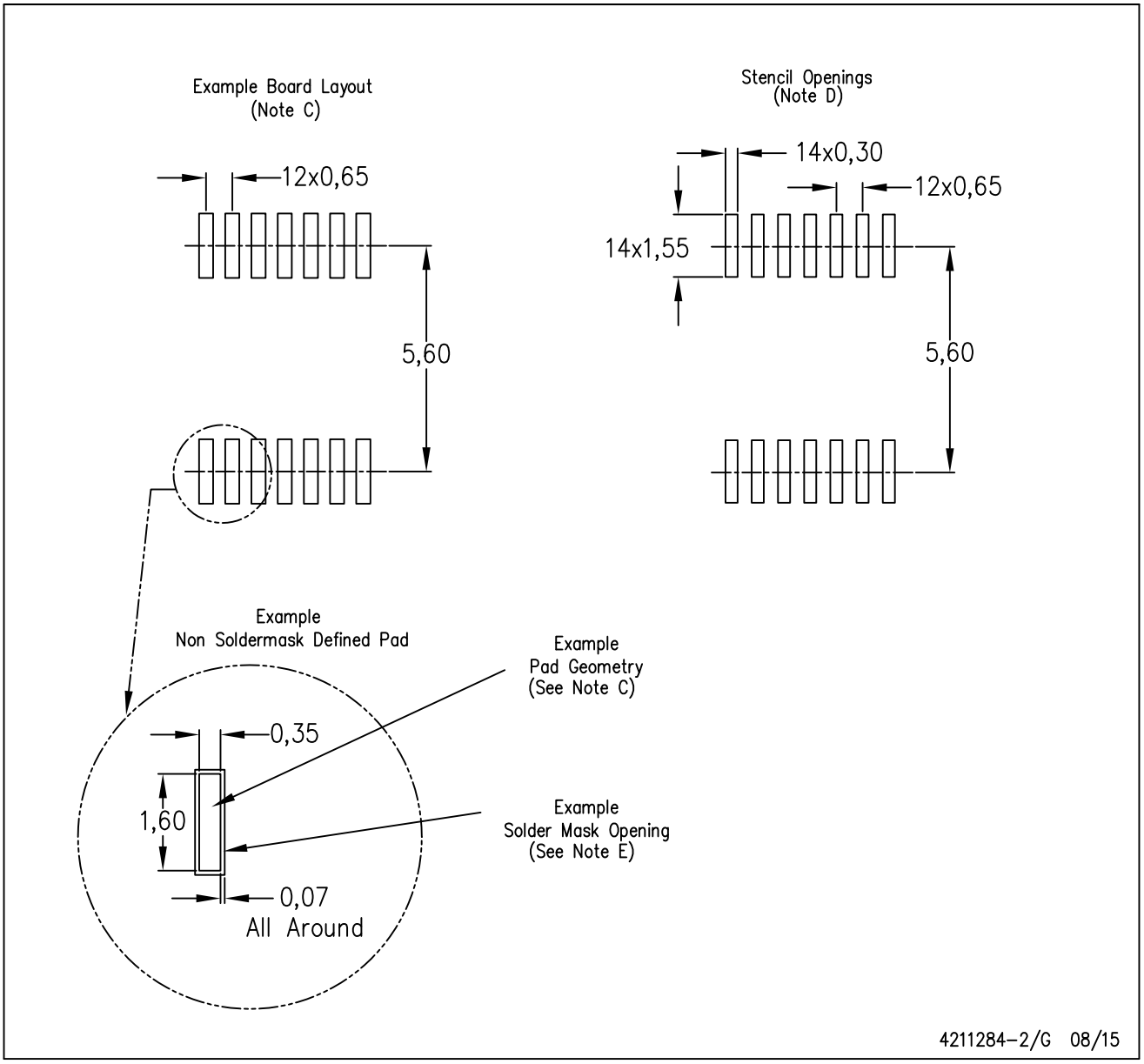
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



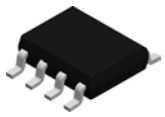
4040064–3/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

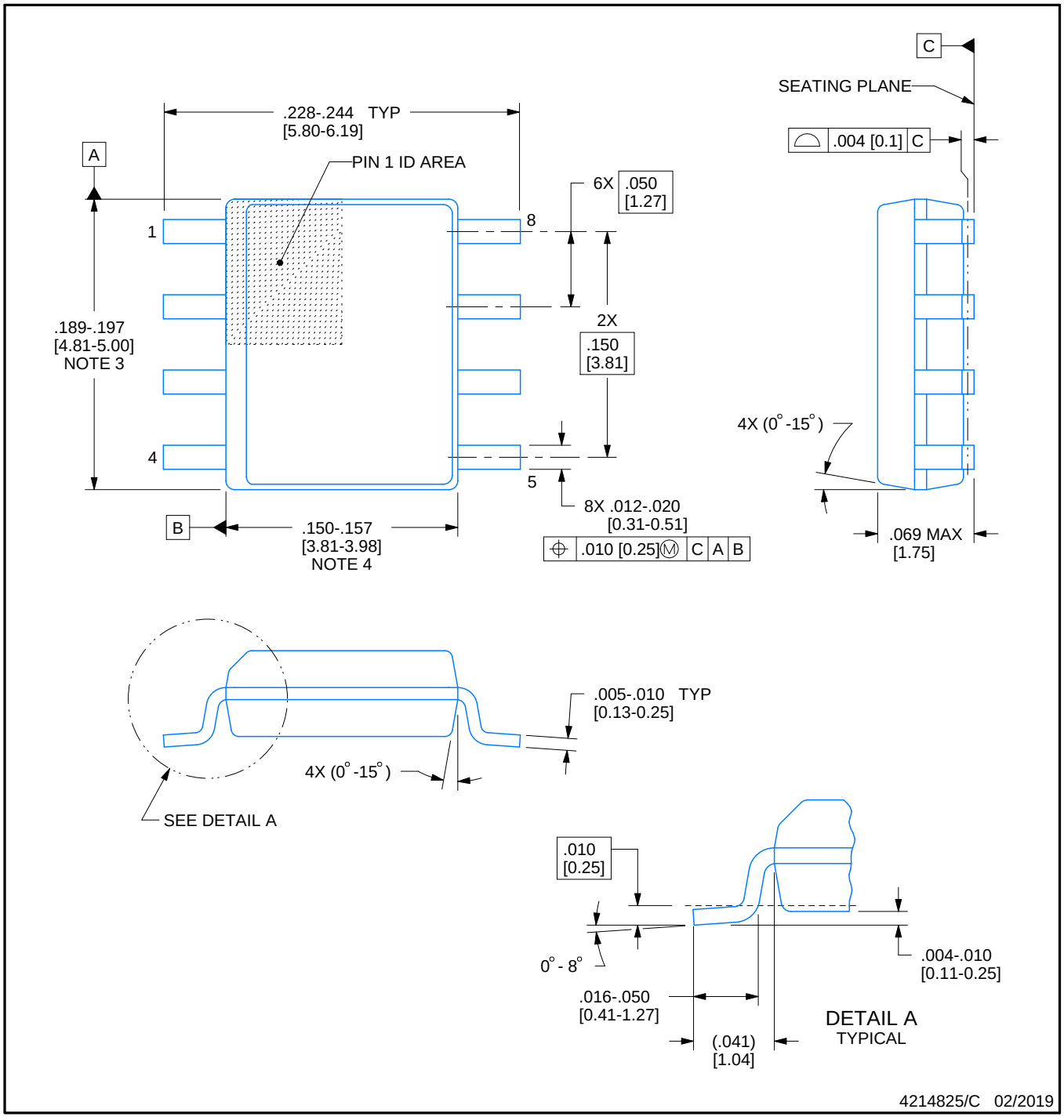


PACKAGE OUTLINE

D0008A

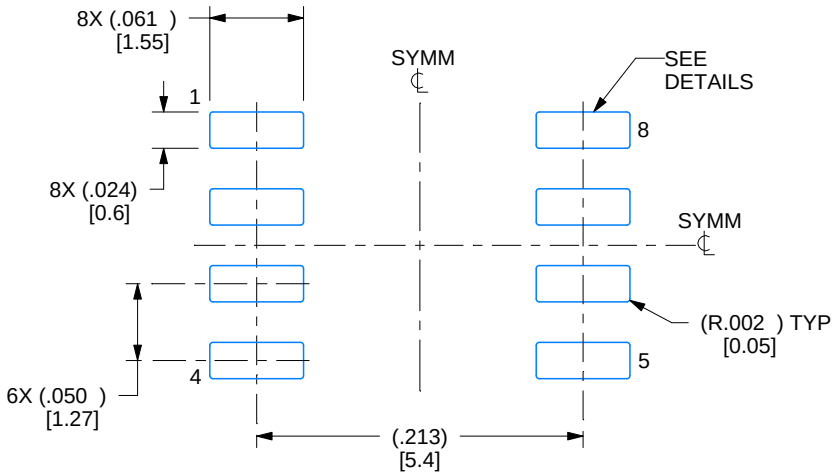
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

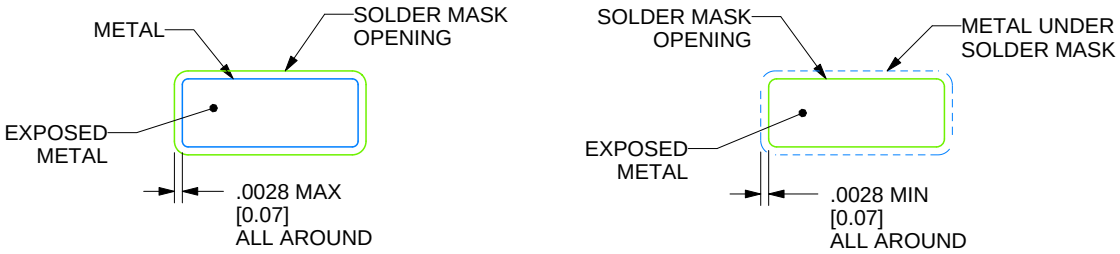


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

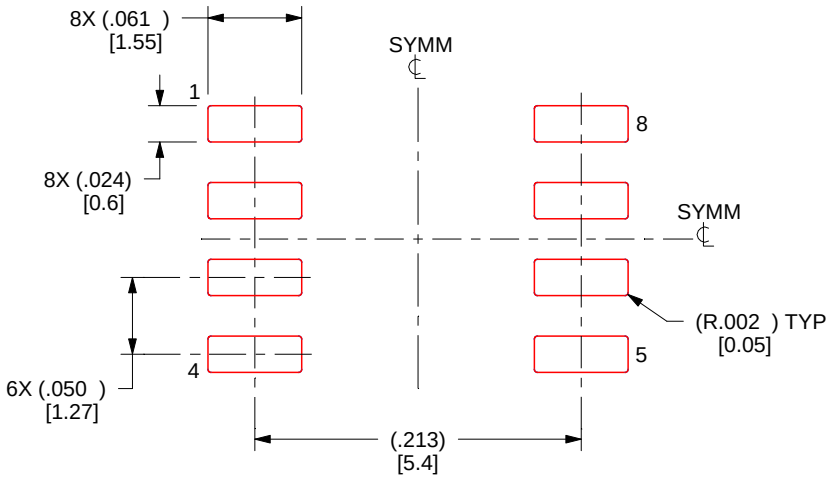
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



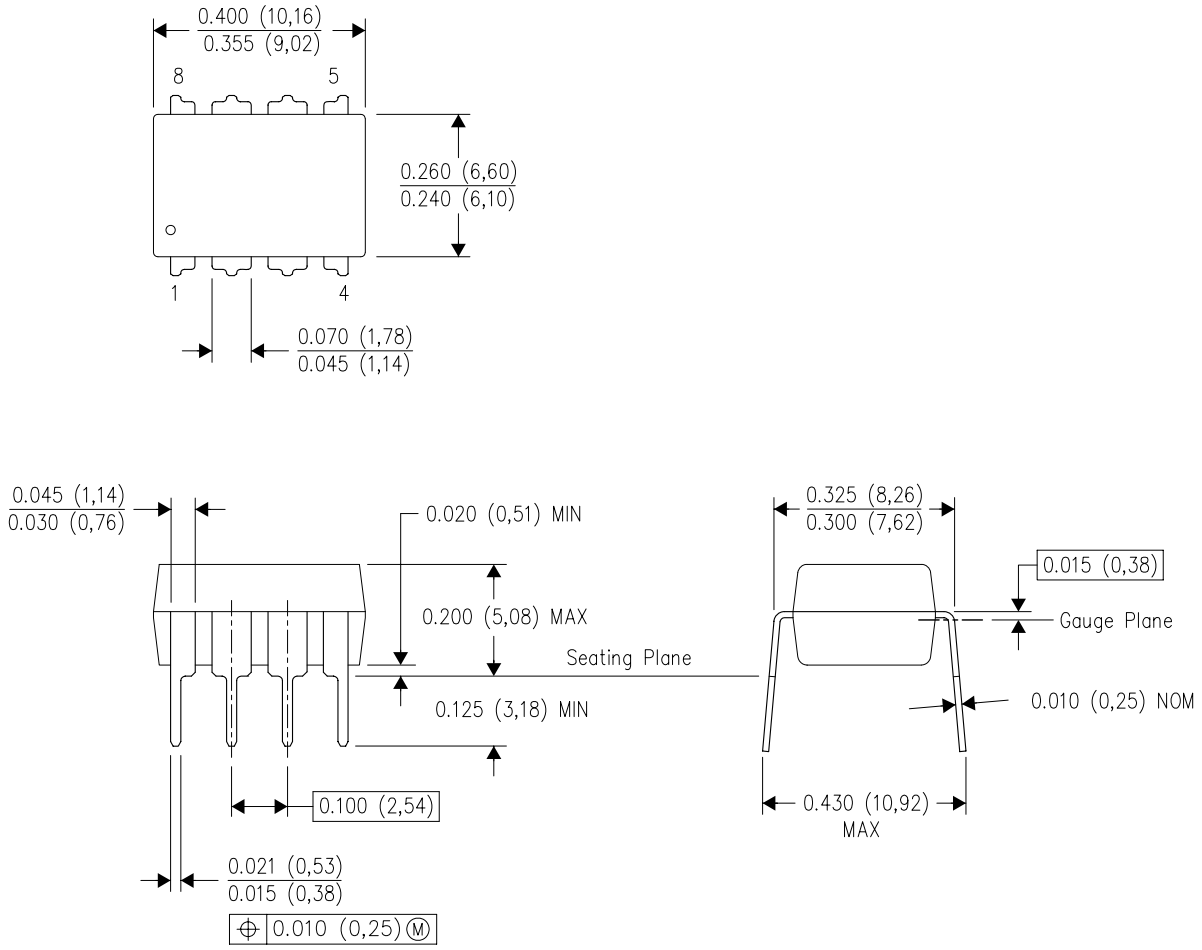
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

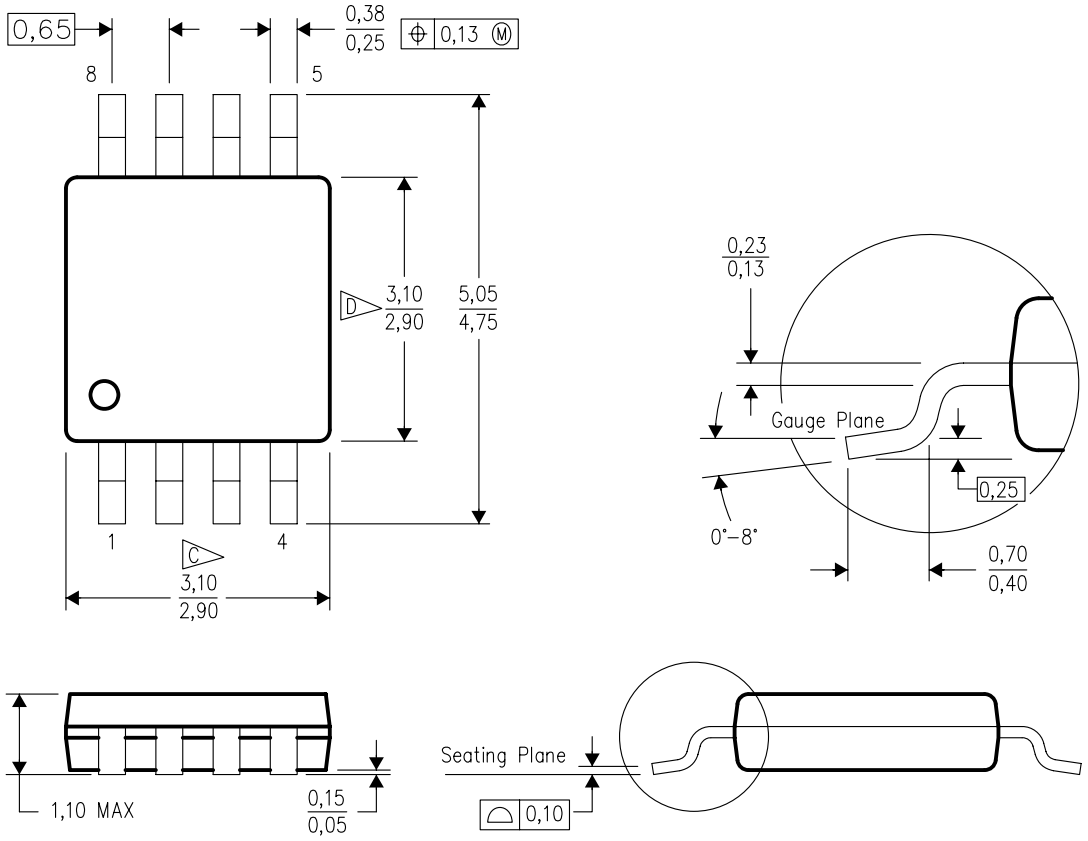
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R–PDIP–T8) PLASTIC DUAL–IN–LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001 variation BA.

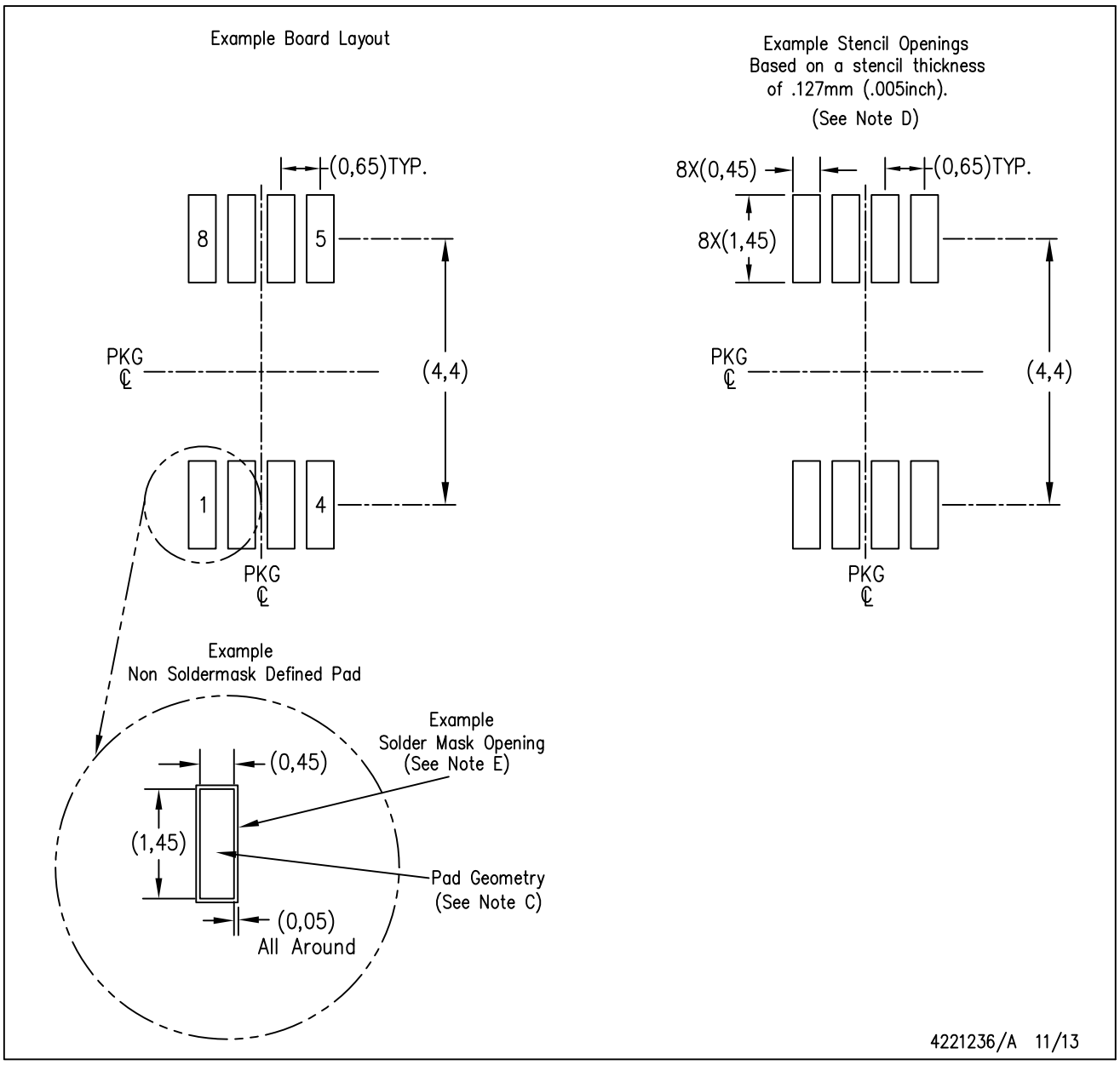
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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