TEXAS INSTRUMENTS
OPT4048
JAJSLS3 – DECEMBER 2022

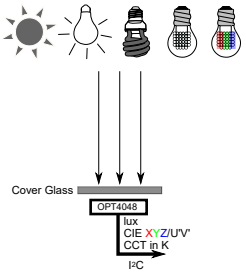
OPT4048 高速、高精度の 三刺激値 XYZ カラー・センサ

1 特長

- 高速 I2C インターフェイスにおける高速、高精度なカラー光 / デジタル変換
- 精度光学フィルタを使用した 4 チャネル検出:
  - 優れた IR 除去機能を備え、CIE 1931 スペクトラムにほぼ一致する XYZ 三刺激値チャネル
  - クリアな広帯域幅チャネル
- CIE XY、LUV 空間、相関色温度 (CCT) における高分解能の色測定と、周囲照度のルクス単位での測定
- 7 つのバイナリ対数フルスケール光レンジによる片対数出力と、各レンジ内における高線形的応答
- 内蔵の自動フルスケール光レンジ選択ロジックにより、入力光条件に基づいて測定レンジを切り替え、レンジ間での優れたゲイン・マッチングを実現
- 26 ビットで 2.15mlux～144klux の実効ダイナミック・レンジ
- 変換時間はチャネルあたり 600µs～800ms の 12 種類を構成でき、さまざまな高速高精度アプリケーションに最適
- ハードウェア同期トリガおよび割り込み用の外部ピン割り込み
- 低動作電流:24µA、超低消費電力待機:2µA
- 動作温度範囲:-40°C～+85°C
- 広い電源電圧範囲:1.6V～3.6V
- 5.5V 対応の I/O
- 選択可能な I^2C アドレス
- 小さいフォームファクタ:
  - 2.1mm x 1.9mm x 0.6mm の SOT-5X3 パッケージ

2 アプリケーション

- ディスプレイの輝度と色の調整
- カメラ画像補正
- 自動ホワイト・バランシング
- ビル・オートメーションおよび制御
- 照明制御システム
- タブレットおよびノート・パソコン



3 概要

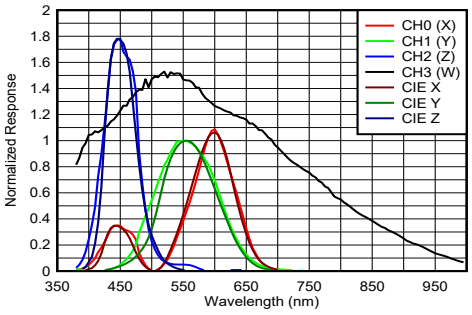
OPT4048 はシングルチップの高分解能カラー・センサです。4 つのチャネルを測定でき、チャネルごとに固有の工学的スペクトル応答があります。4 つのうち 3 つのチャネルは、CIE のスペクトルの三刺激値にほぼ一致し、4 つ目のチャネルには広帯域スペクトル応答があります。これらのチャネルからの測定を通して、(i) 光の強度 (ルクス単位)、(ii) CIE XY、LUV 座標の色、(iii) 相関色温度といった照明環境の重要な特性を抽出できます。OPT4048 は、小型の SOT-5X3 パッケージで供給されます。

OPT4048 の選択可能なアドレッシング方式により、共有 I^2C バスで最大 4 つのデバイスを有効にできます。チャネルのスペクトル応答は、CIE のスペクトルの三刺激値を忠実に模倣するように特別に調整され、それぞれのピーク、特に NIR (850nm および 940nm) 領域から離れた波長を強力に除去しながら最も正確な色検出を実現します。フィルタには高度なフィルタ技術が採用され、高い入射角でも優れたフィルタ性能を発揮します。本デバイスは高精度の色検出機能を備え、周囲光の色や色温度を精密に検出する必要がある複数のアプリケーションに対応できます。

デバイス情報

部品番号	パッケージ(1)	本体サイズ (公称)
OPT4048	SOT-5X3 (8)	2.10mm x 1.90mm x 0.6mm

(1) 利用可能なパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。



正規化されたスペクトル応答

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
December 2022	*	Initial release.

5 概要 (続き)

OPT4048 の光学フィルタには近赤外線除去機能があるため、産業用の製品設計で美観上の理由からよくある要件として、暗色のガラス下にセンサを設置する場合でも、高い精度を維持できます。

OPT4048 は、光レベル検出を必要とするシステム向けに設計され、照明の強度のみでなく色に関する情報を提供することでユーザー体験を向上させます。

OPT4048 デバイスは、チャネルごとに 12 ステップで 600µs～800ms の光変換時間で動作するように構成でき、アプリケーションのニーズに応じたシステムの柔軟性を実現します。変換時間には、光の積分時間と ADC 変換時間が含まれます。測定の分解能は、光の強度と積分時間によって決定され、実質的に最小 2.15 mlux までの光強度を測定できます。

柔軟なデジタル動作により、システムの統合が可能です。連続的な測定も、レジスタ書き込みまたはハードウェアピンによる 1 回のみの測定も可能です。本デバイスは、スレッショルド検出ロジックを備えており、プロセッサがスリープ中であっても、センサが適切なウェイクアップ・イベントの有無を調べて割り込みピンで通知します。

光レベルを表すデジタル出力は、I²C および SMBus 互換の 2 線式シリアル・インターフェイスで通知されます。

OPT4048 は低い消費電力と低い電源電圧で動作するため、バッテリ駆動システムのバッテリ動作時間を延長できます。

6 Pin Configuration and Functions

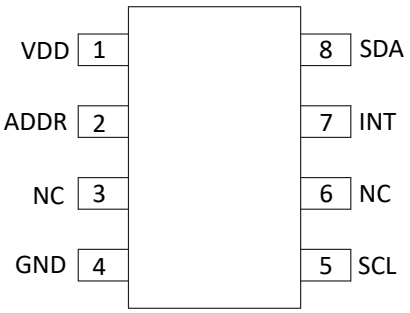


図 6-1. DTS Package, 8-Pin SOT-5X3, Top View

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	VDD	Power	Device power. Connect to a 1.6-V to 3.6-V supply.
2	ADDR	Digital input	Address pin. This pin sets the LSBs of the I²C address.
3	NC	No Connection	No Connection
4	GND	Power	Ground
5	SCL	Digital input	I²C clock. Connect with a 10-kΩ resistor to a 1.6-V to 5.5-V supply.
6	NC	No Connection	No Connection
7	INT	Digital I/O	Interrupt input/output open-drain. Connect with a 10-kΩ resistor to a 1.6-V to 5.5-V supply.
8	SDA	Digital I/O	I²C data. Connect with a 10-kΩ resistor to a 1.6-V to 5.5-V supply.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	VDD to GND	–0.5	6	V
	SDA and SCL to GND	–0.5	6	V
Current in to any pin			10	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–65	150(2)	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) Long exposure to temperatures higher than 105°C can cause package discoloration, spectral distortion, and measurement inaccuracy.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD	Supply voltage	1.6		3.6	V
T_J	Junction temperature	–40		85	°C

7.4 Thermal Information

THERMAL METRIC(1)		OPT4048 DTS 8 Pins	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	112.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	22.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	22	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

All specifications at TA = 25°C, VDD = 3.3 V, 100-ms conversion-time per channel, automatic full-scale range, white LED and normal-angle incidence of light, unless otherwise specified. Spec parameters are preliminary, subject to change.over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Optical						
	Number of Channels			4		
λ_{peak}	Peak irradiance spectral responsivity	CH0 (X)		600		nm
		CH1(Y)		550		nm
		CH2(Z)		460		nm
		CH3(W)		500		nm
	ADC resolution		9		20	bits
	Range determination			3		bits
T_{intg}	Light Integration-time per channel (4)	Conversion-time CT = 0x6		25		ms
		Conversion-time CT = 0xB		800		ms
R_{CH0}	Peak Responsivity	CH0 (X) Lowest auto gain range, 800 ms conversion time per channel		2770		codes per $\mu W/cm^2$
R_{CH1}		CH1 (Y) Lowest auto gain range, 800 ms conversion time per channel		3960		codes per $\mu W/cm^2$
R_{CH2}		CH2 (Z) Lowest auto gain range, 800 ms conversion time per channel		1910		codes per $\mu W/cm^2$
R_{CH3}		CH3 (W) Lowest auto gain range, 800 ms conversion time per channel		6950		codes per $\mu W/cm^2$
ER_{lux}	Equivalent Resolution	Lowest auto gain range, 100 ms conversion-time per channel		17.2		mlux
		Lowest auto gain range, 800 ms conversion-time per channel		2.15		mlux
E_{vFS}	Full-scale equivalent Illuminance			144284		lux
E_v	Measurement output result from lux measurement	2000 lux input(1)	1800	2000	2200	lux
	Relative accuracy between gain ranges (2)	All channels		0.6		%
E_{vIR}	Infrared response(6)	850nm near infra-red, all channels except for CH3 (W)		0.2		%
	Light source variation for lux measurement (incandescent, halogen, fluorescent)	Bare device, no cover glass		4		%
	Linearity	Input illuminance > 2254 lux , 100 ms conversion-time per channel, all channels		2		%
		Input illuminance <= 2254 lux , 100 ms conversion-time per channel, all channels		5		%
	Dark Measurement	All channels		0	10	codes
	Drift across temperature	CH0 (X)		0.02		%/°C
		CH1 (Y)		0.02		%/°C
		CH2 (Z)		0.05		%/°C
		CH3 (W)		0.05		%/°C

7.5 Electrical Characteristics (continued)

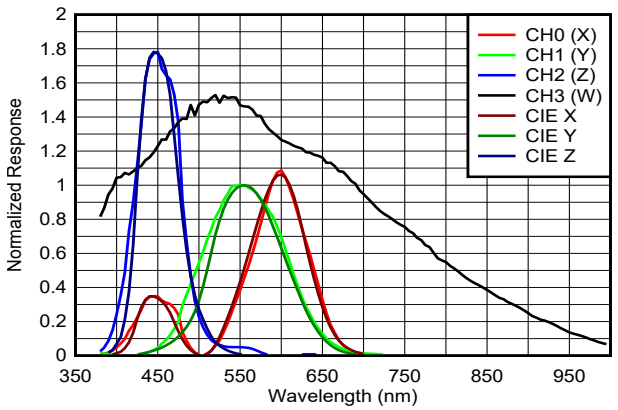
All specifications at TA = 25°C, VDD = 3.3 V, 100-ms conversion-time per channel, automatic full-scale range, white LED and normal-angle incidence of light, unless otherwise specified. Spec parameters are preliminary, subject to change.over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
	Angular response (FWHM)	CH0 (X)		134		°
		CH1 (Y)		121		°
		CH2 (Z)		99		°
		CH3 (W)		128		°
PSRR	Power-supply rejection ratio(3)	VDD at 3.6 V and 1.6 V, 30 different sources, all channels		0.2		%/V
POWER SUPPLY						
V_{DD}	Power supply		1.6		3.6	V
V_{I2C}	Power supply for I^2C pull up resistor	I^2C pullup resistor, $V_{DD} \leq V_{I2C}$	1.6		5.5	V
$I_{QACTIVE}$	Active Current	Dark		24		µA
		Full-scale lux		29		µA
I_Q	Quiescent current	Dark		2		µA
		Full-scale lux		2.6		µA
POR	Power-on-reset threshold			0.8		V
DIGITAL						
C_{IO}	I/O Pin Capacitance			3		pF
V_{IL}	Low-level input voltage (SDA, SCL, and ADDR)		0		0.3 X V_{DD}	V
V_{IH}	High-level input voltage (SDA, SCL, and ADDR)		0.7 X V_{DD}		5.5	V
I_{IL}	Low-level input current (SDA, SCL, and ADDR)			0.01	0.25(5)	µA
V_{OL}	Low-level output voltage (SDA and INT)	I_{OL}=3mA			0.32	V
I_{ZH}	Output logic high, high-Z leakage current (SDA, INT)	Measured with V_{DD} at pin		0.01	0.25(5)	µA
TEMPERATURE						
	Specified temperature range		–40		85	°C

(1) Tested with the white LED calibrated to 2000 lux.
(2) Characterized by measuring fixed near-full-scale light levels on the higher adjacent full-scale range setting.
(3) PSRR is the percent change of the measured lux output from the current value, divided by the change in power supply voltage, as characterized by results from 3.6-V and 1.6-V power supplies.
(4) The conversion-time, from start of conversion until the data are ready to be read, is the integration-time plus analog-to-digital conversion-time.
(5) The specified leakage current is dominated by the production test equipment limitations. Typical values are much smaller.
(6) Tested with a near infrared LED of 850nm wavelength.

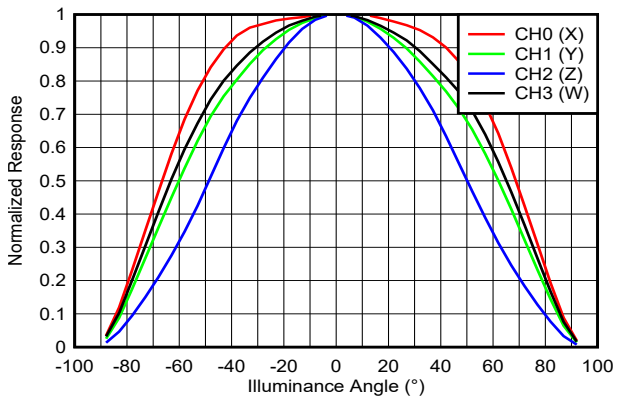
7.6 Typical Characteristics

At T_A = 25°C, V_{DD} = 3.3 V, 800-ms conversion time (CONVERSION_TIME = 0xB), automatic full-scale range (RANGE = 0xC), white LED, and normal-angle incidence of light, unless otherwise specified.



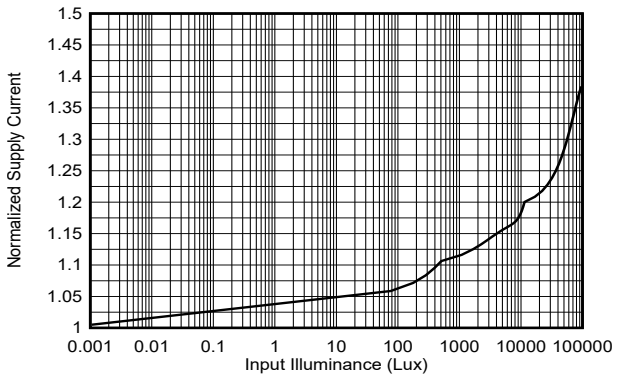
Channels measurements scaled to match CIE curves

図 7-1. Spectral Response vs Wavelength



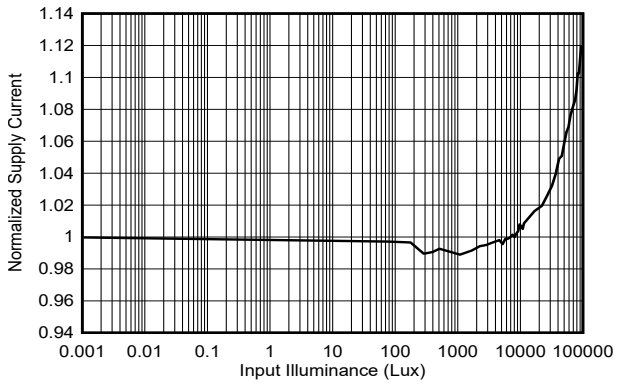
Normalized to 0°

図 7-2. Device Response vs Illuminance Angle



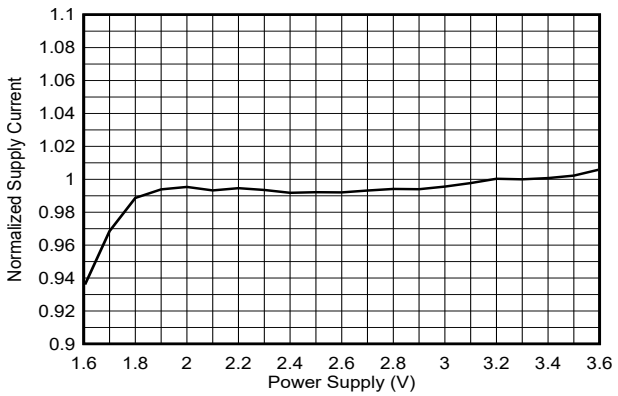
Normalized to dark condition

図 7-3. Active Current vs Input Light Level



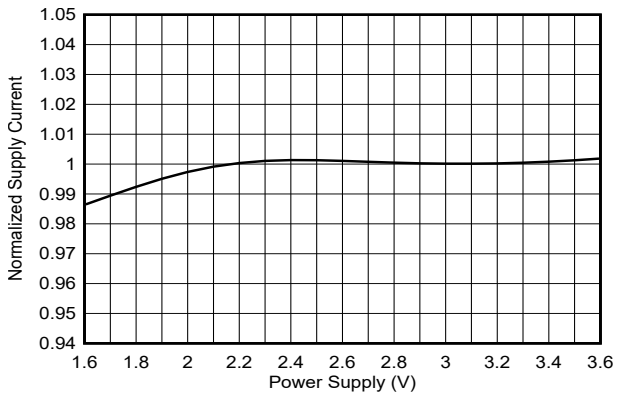
Normalized to dark condition

図 7-4. Standby Current vs Input Light Level



Normalized to 3.3 V

図 7-5. Active Current vs Power Supply

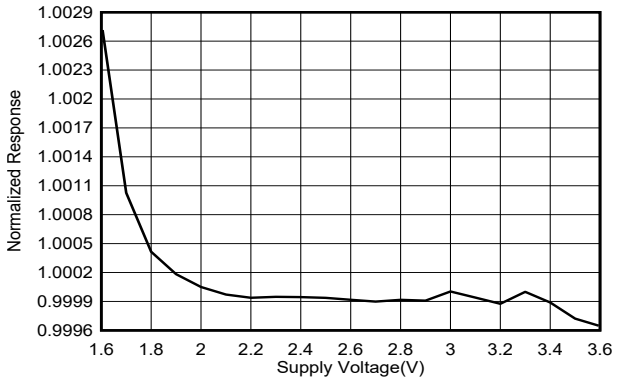


Normalized to 3.3 V

図 7-6. Standby Current vs Power Supply

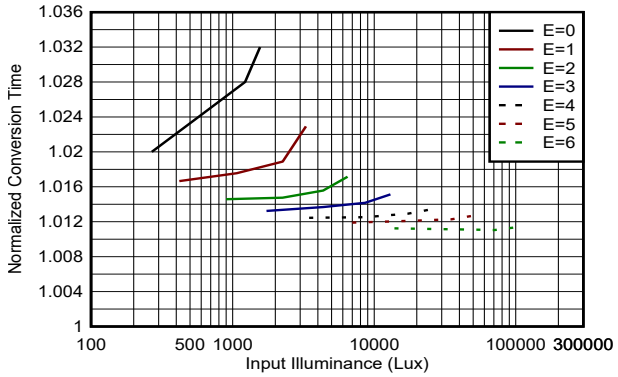
7.6 Typical Characteristics (continued)

At T_A = 25°C, V_{DD} = 3.3 V, 800-ms conversion time (CONVERSION_TIME = 0xB), automatic full-scale range (RANGE = 0xC), white LED, and normal-angle incidence of light, unless otherwise specified.



Normalized to 3.3 V

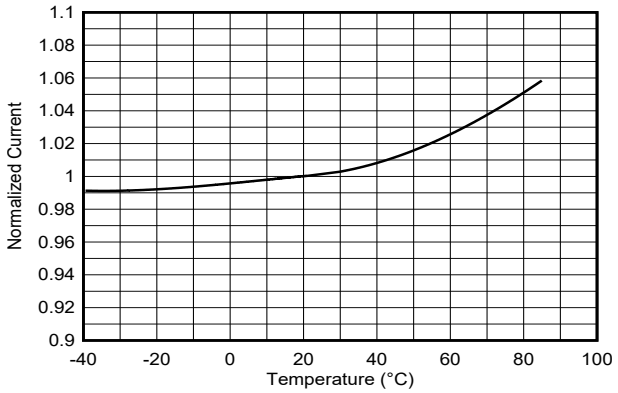
図 7-7. Device Response vs Power Supply



E denotes register EXPONENT_CHx

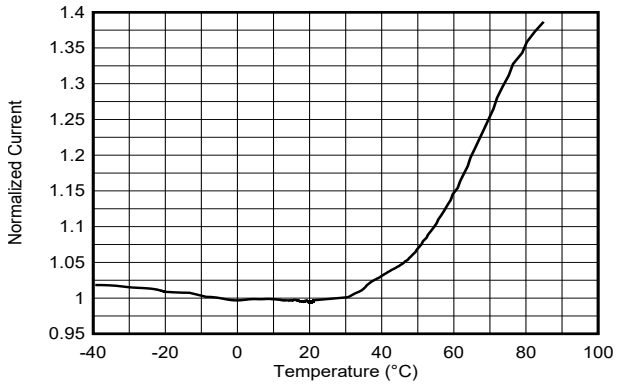
Normalized to 25 ms

図 7-8. Conversion Time at 25 ms per channel vs Input Light Level



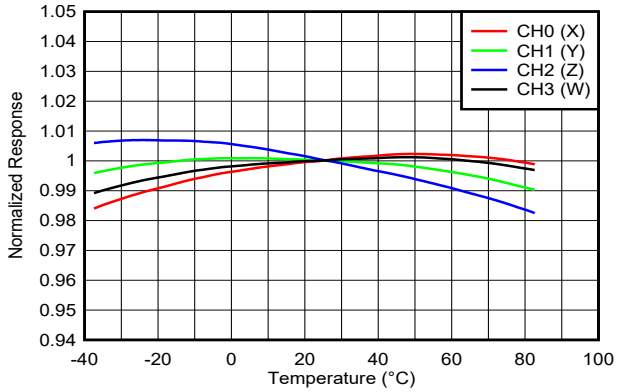
Normalized to 25°C

図 7-9. Active Current vs Temperature



Normalized to 25°C

図 7-10. Standby Current vs Temperature



Normalized to 25°C

図 7-11. Device Response vs Temperature

8 Detailed Description

8.1 Overview

The OPT4048 measures the color properties of the light source that illuminates the device. This device measures four channels (X Channel, Y Channel, Z Channel, W Channel) with special spectral characteristics, which helps extract properties of the light source (i) the CIE XY/U'V' color coordinates (ii) the lux level and (iii) the correlated color temperature. Name of the channels correspond to the respective CIE tristimulus curves with additional W channel being the wide channel response.

With close matching to the CIE tristimulus spectral profiles, OPT4048 measures the true color of any light source or environment. This helps applications where, measuring the precise characteristics of the lighting environment is critical like display brightness, color temperature adjustment, camera color temperature correction, object true color recognition & medical applications.

Since CIE tristimulus curves are devised to mimic human color perception, matching the sensor spectral response to those curves is vital because color sensors are used to measure and help create excellent human lighting experiences. Strong rejection of infrared light, which a human does not see, is a crucial component of this matching. This matching makes the OPT4048 especially good for operation underneath windows that are visibly dark, but infrared transmissive

OPT4048 is fully self-contained to measure the properties of light and report the result in ADC codes digitally over the I^2C bus. The result can also be used to alert a system and interrupt a processor with the INT pin. The result can also be summarized with a programmable threshold comparison with a specified channel and communicated with the INT pin.

OPT4048 is by default configured to operate in automatic full-scale range detection mode that always selects the best full-scale range setting for the given lighting conditions. There are 7 full-scale range settings, one of which can be selected manually as well. Setting the device to operate in automatic full-scale range detection mode frees the user from having to program their software for potential iterative cycles of measurement and readjustment of the full-scale range until good for any given measurement. With device exhibiting excellent linearity over the entire 26 bit dynamic range of measurement no additional linearity calibration is required at system level.

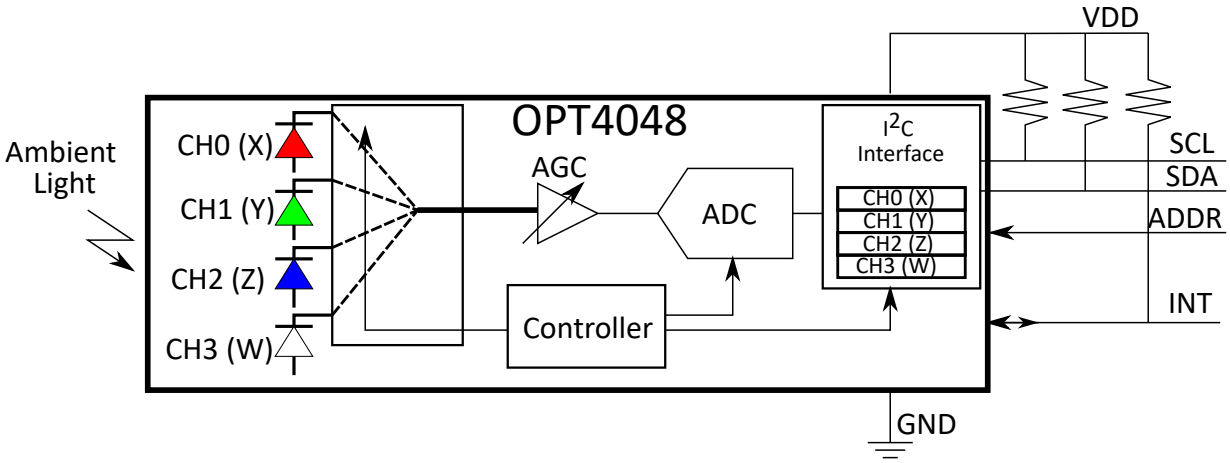
The OPT4048 contains 4 channels, results of which are always available all the time as independent channel registers which can be digitally read over the I^2C bus synchronously or asynchronously.

The device measures light for 4 channels sequentially (X, Y, Z, W) with selectable conversion times from 600 µs per channel to 800 ms per channel in 12 steps. Measurements can be read asynchronously or interrupt pin based which can be configured to generate an interrupt every time a single channel completes conversion or every time all 4 channels complete conversion.

The device starts up in a low-power shutdown state, such that the OPT4048 only consumes active-operation power after being programmed into an active state.

OPT4048 optical filtering system is not excessively sensitive to small particles and micro-shadows on the optical surface. This reduced sensitivity is a result of the relatively minor device dependency on uniform density optical illumination of the sensor area for infrared rejection. Proper optical surface cleanliness is always recommended for best results on all optical devices.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Spectral Matching to CIE

The OPT4048 spectral response closely matches CIE 1931 tristimulus spectra, which is modeled to be a close representation of how an average human perceives light. This is crucial to measure the characteristics of light such an color, intensity as close as possible to how humans perceive.

OPT4048 also has excellent infrared light (IR) rejection. This IR rejection is especially important because many real-world lighting sources have significant infrared content that humans do not see. If the sensor measures infrared light that the human eye does not see, then a true human experience is not accurately represented.

If the application demands hiding OPT4048 underneath dark window (such that the end-product user cannot see the sensor) the infrared rejection of the OPT4048 becomes significantly more important because many dark windows attenuate visible light but transmit infrared light. This attenuation of visible light and lack of attenuation of IR light amplifies the ratio of the infrared light to visible light that illuminates the sensor. Results can still be well matched to the human eye under this condition because of the high infrared rejection of the OPT4048.

8.3.2 Automatic Full-Scale Range Setting

The OPT4048 has an automatic full-scale range setting feature that eliminates the need to predict and set the best range for the device. Each channel has a auto-scaling algorithm and independently tracks light levels. In this mode, the OPT4048 automatically selects the best full-scale range for the given lighting condition. The OPT4048 has a high degree of result matching between the full-scale range settings. This matching eliminates the problem of varying results or the need for range-specific, user-calibrated gain factors when different full-scale ranges are chosen. The device has independent range detection logic making the device operate seamlessly with a wide range of light color and levels.

8.3.3 Output Register CRC and Counter

OPT4048 device features additional bits as part of the output register which helps in improving the reliability of light measurements for the application.

8.3.3.1 Output Sample Counter

The OPT4048 device features registers COUNTER_CHx as part of the output registers which increments for every successful measurement. This register can be read as part of the output registers which helps the application to keep track of measurements. The 4 bit counter starts at 0 on power-up and counts up to 15 after which the counter resets back to 0 and continues to count up. There are independent counters for each channel counting up every successful conversion.

- Host or the controller needs consecutive measurements. Utilizing the COUNTER_CHx registers allow the controller to compare samples and makes sure that the samples are in expected order without missing intermediate counter values.

- As a safety feature where when light level are not changing, the controller can make sure that the measurements from OPT4048 are not stuck by comparing values of registers COUNTER_CHx between measurements. If the COUNTER_CHx values continue to change over samples, the device is updating the output register with the most recent measurement of light levels.

8.3.3.2 Output CRC

CRC_CHx registers consists of Cyclic Redundancy Checker bits part of the output registers calculated within the OPT4048 device and updated on every measurement. This feature helps in detecting communication related bit errors during the output readout from the device. The calculation method for the CRC bits is shown in the 図 8-12, which can be independently verified in the controller or host firmware/software to validate if communication between the controller and the device was successful without bit errors during transmission.

8.3.3.3 Threshold Detection

OPT4048 features a threshold detection logic which can be programmed to indicate and update register flags if measured light levels cross thresholds set by the user. The threshold condition can be programmed to use one of the 4 channels as trigger determined by the THRESHOLD_CH_SEL register. There are independent low and high threshold target registers with independent flag registers to indicate the status of measured light level. Measured light level reaching below low threshold and above the high threshold are called faults. Users can program a fault count register, which counts consecutive number of faults before the flag registers are set. Details on the register and setting up the threshold is available in セクション 8.3.4.2 and セクション 8.3.4.5.

8.3.4 Device Functional Modes

8.3.4.1 Modes of Operation

OPT4048 has output registers which are always available to readout to get measurements, the measurements themselves are updated based on the device mode of operation listed below. The OPT4048 device has the following modes of operation:

- **Power-down mode:** This is power-down or standby mode where the device enters a low power state. There is no active light sensing or conversion in this mode. Device still responds to I^2C transactions which can be utilized to bring the device out of this mode.
- **Continuous mode:** In this mode OPT4048 measures all 4 channels in a round robin fashion continuously and updates their corresponding output registers. The conversion time register CONVERSION_TIME determines the time between each channel conversion and a hardware interrupt on pin INT is generated for every successful conversion on each channel or all 4 channels depending on INT_CFG register value. TI recommends to configure the INT pin in output mode using the INT_DIR register. The device active circuits are continuously kept active to minimize the interval between measurements.
- **One shot mode of operation:** There are several ways in which OPT4048 can be used in one shot mode of operation with one common theme which is that OPT4048 stays in standby mode and a conversion is triggered by a register write either by a register write to configuration register or hardware interrupt on the INT pin. Every trigger generates one measurement for 4 channels, effectively taking four times the time set by the CONVERSION_TIME register

  There are two types of one shot modes.
  - **Force auto-range one shot mode:** Every one shot trigger forces a full reset on auto-ranging control logic and a fresh auto-range detection in initiated ignoring the previous measurements. This is particularly useful in situation where lighting conditions are expected to change a lot and one shot trigger frequency is not very often. There is small penalty on conversion time due for the auto-ranging logic to recover from reset state. The full reset cycle on the auto-ranging control logic takes around 500 µs which needs to be accounted for between measurements when this mode is used.
  - **Regular auto-range one shot mode:** Auto-range selection logic utilizes the information from the previous measurements to decide on range for the current trigger. This mode is recommended only when the device needs time synchronized measurements with frequent triggers from the controller. In other words, this mode can be used as an alternative to continuous mode the key difference being that the interval between measurements in determined by the one shot triggers.

  One Shot can be triggered using by the following:

- **Hardware trigger:** INT pin can be configured to be an input to trigger a measurement using INT_DIR register. Since INT pin is used as input, there is no hardware interrupt to indicate completion of measurement. The controller needs to keep time from the trigger mechanism and read out output registers.
- **Register trigger:** An I^2C write to the M register triggers a measurement. The register value is reset after a successful measurement. INT pin can be configured to indicate measurement completion to read out output registers using the INT_DIR register.

TI highly recommends to set the interval between subsequent triggers to account for all the aspects involved in the trigger mechanism like the I^2C transaction time, device wake-up time, auto-range time (if used) and 4 times the device conversion time.

Since the device enters standby after each one shot trigger, measurement interval on the one shot trigger mechanism needs to account for additional time T_{ss} as specified in the specification table for the circuits to recover from standby state. However setting the quick wake up register QWAKE eliminates the need for this additional T_{ss} at the cost of not powering down the active circuit with device not entering the standby mode between triggers.

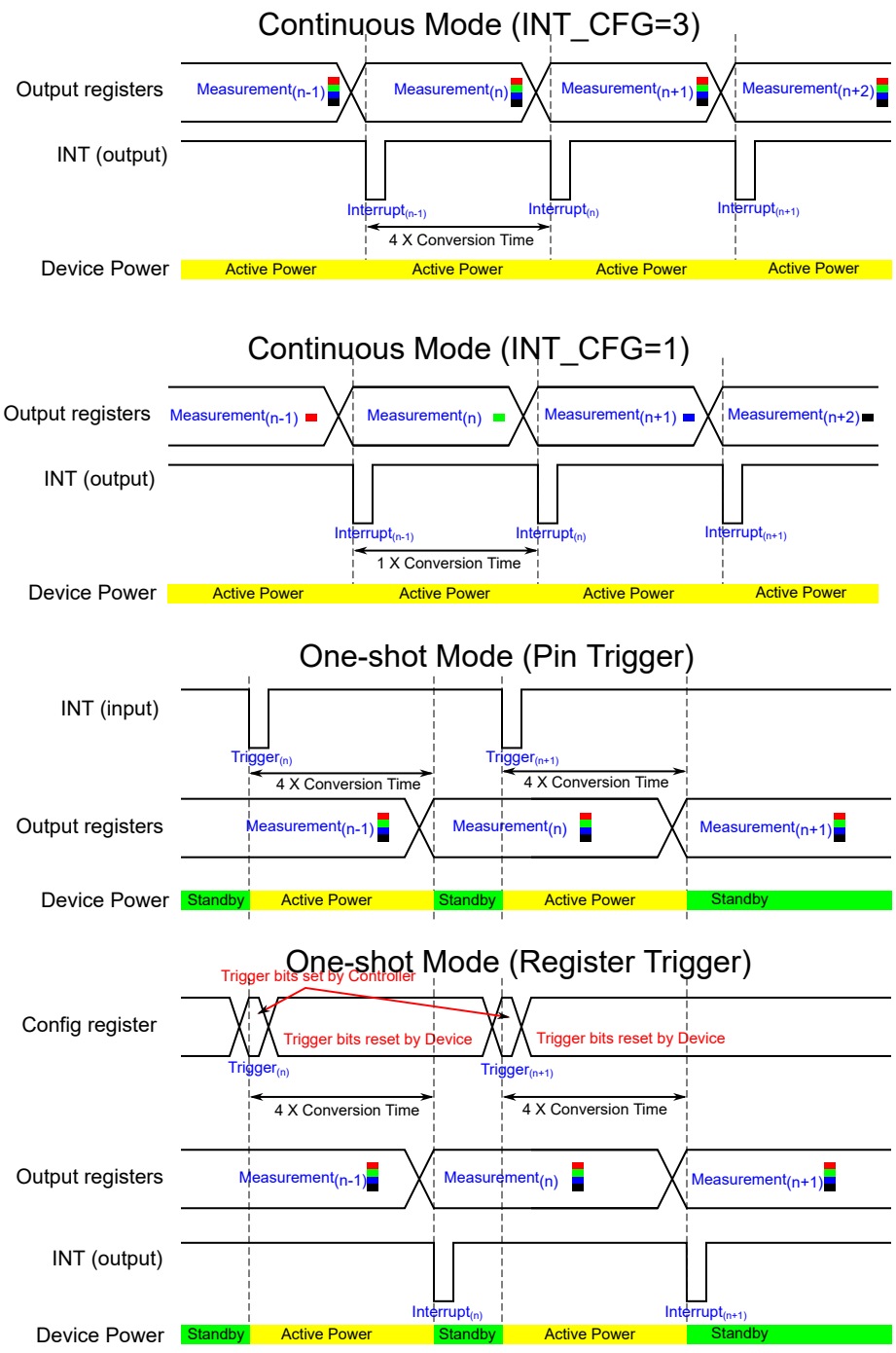


図 8-1. Timing Diagrams for different Operating modes

8.3.4.2 Interrupt Modes of Operation

The device has an interrupt reporting system that allows the processor connected to the I^2C bus to go to sleep, or otherwise ignore the device results, until a user-defined event occurs that requires possible action. Alternatively, this same mechanism can also be used with any system that can take advantage of a single digital signal that indicates whether the light is above or below levels of interest.

Channel on which this behavior can be enabled is set by the register THRESHOLD_CH_SEL.

The INT pin has an open-drain output, which requires the use of a pull-up resistor. This open-drain output allows multiple devices with open-drain INT pins to be connected to the same line, thus creating a logical *NOR* or *AND* function between the devices. The polarity of the INT pin can be controlled by the INT_POL.

There are two major types of interrupt reporting mechanism modes: latched window comparison mode and transparent hysteresis comparison mode. The configuration register LATCH controls which of these two modes is used. 図 8-2 and 表 8-1 summarize the function of these two modes. Additionally, the INT pin can either be used to indicate a fault in one of these modes (INT_CFG=0) or to indicate a conversion completion (INT_CFG >0). This is shown in 表 8-2.

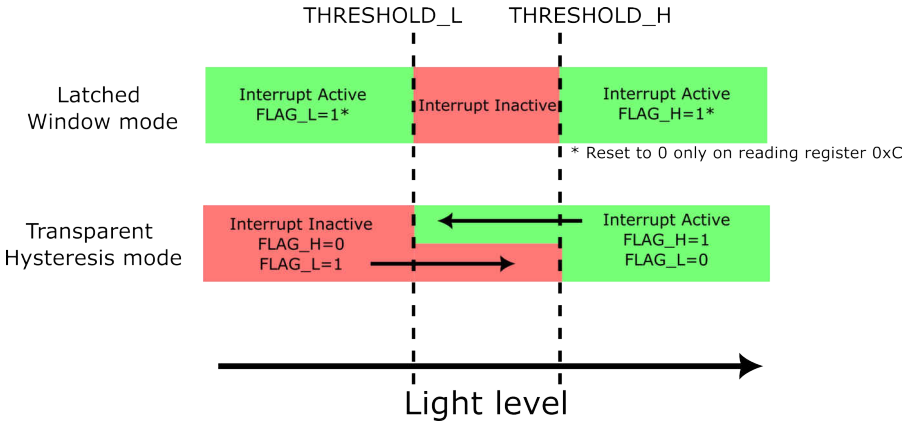


図 8-2. Interrupt Pin Status (for INT_CFG=0 setting) and Register Flag Behavior

表 8-1. Interrupt Pin Status (for INT_CFG=0 setting) and Register Flag Behavior

LATCH Setting	INT Pin State (when INT_CFG=0)	FLAG_H Value	FLAG_L Value	Latching Behavior
0: Transparent hysteresis mode	INT pin indicates if measurement is above (INT active) or below (INT inactive) the threshold. If measurement is between the high and low threshold values then the previous INT value is maintained. This prevents the INT pin from repeated toggling when the measurement values are close to the threshold.	0: If measurement is below the low limit 1: If measurement is above the high limit If measurement is between high and low limits previous value is maintained	0: If measurement is above the high limit 1: If measurement is below the low limit If measurement is between high and low limits previous value is maintained	Not latching: Values are updated after each conversion
1: Latched window mode	INT pin becomes active if the measurement is outside the window (above high threshold or below the low threshold). The INT pin does not reset and return to the inactive state until register 0xC is read.	1: If measurement is above the high limit	1: If measurement is below the low limit	Latching: INT pin, FLAG_H and FLAG_L values do not reset until the register 0x0C is read.

The THRESHOLD_H, THRESHOLD_L, LATCH and FAULT_COUNT registers control the interrupt behavior. The LATCH field setting allows a choice between the latched window mode and transparent hysteresis mode as shown in the table. Interrupt reporting can be observed on INT pin, the FLAG_H, and the FLAG_L registers.

Results from comparing the current sensor measurements with THRESHOLD_H and THRESHOLD_L registers are referred to as *fault events*. The calculations to set these registers can be found in セクション 8.3.4.5. The FAULT_COUNT register dictates the number of continuous *fault events* required to trigger an interrupt event and subsequently change the state of the interrupt reporting mechanisms. For example, with a FAULT_COUNT value

of 2 corresponding to 4 fault counts, the INT pin, FLAG_H and FLAG_L states shown in the table are not realized unless 4 consecutive measurements are taken that satisfy the fault condition.

INT pin function listed in 表 8-1 is valid only when INT_CFG=0. The INT pin function can be changed to indicate an end of conversion as well shown in 表 8-2. The FLAG_H and FLAG_L registers continue to behave as listed in 表 8-1 even while INT_CFG>0. The polarity of the INT pin is controlled by the INT_POL register.

表 8-2. INT_CFG Setting and Resulting INT Pin Behavior

INT_CFG Setting	INT Pin Function
0	As per 表 8-1
1	INT pin asserted with 1us pulse width after conversion of every channel
3	INT pin asserted with 1us pulse width every 4 conversions to indicate all channel measurements are complete

8.3.4.3 Light Range Selection

The OPT4048 has an automatic full-scale-range setting mode that eliminates the need for a user to predict and set the best range for the device. This mode is entered when register RANGE is set to 0xC. The device determines the appropriate full-scale range to take the measurement based on a combination of current lighting conditions and the previous measurement.

If a measurement is towards the low side of full-scale, then the full-scale range is decreased by one or two settings for the next measurement. If a measurement is towards the upper side of full-scale, the full-scale range is increased by one setting for the next measurement.

If the measurement exceeds the full-scale range, resulting from a fast increasing optical transient event, then the current measurement is aborted. This invalid measurement is not reported. If the scale is not at the maximum, then the device increases the scale by one step and a new measurement is retaken with that scale. Therefore, during a fast increasing optical transient in this mode, a measurement can possibly take longer to complete and report than indicated by the configuration register CONVERSION_TIME.

The logic that determines the appropriate range settings for each channel is independent of each other, which verifies a support of a wide range of colors represented with the best accuracy.

TI highly recommends to use this feature, since the device selects the best range setting based on lighting condition. However, there is an option to manually set the range. Setting the range manually turns off the automatic full-scale selection logic and the device operates for a particular range setting.

表 8-3. Range Selection Table

RANGE register setting	Typical Full-scale Light level
0	2254 lux
1	4509 lux
2	9018 lux
3	18036 lux
4	36071 lux
5	72142 lux
6	144284 lux
12	Determined by automatic full-scale range logic

8.3.4.4 Selecting Conversion Time

OPT4048 device offers several conversion times to select from. Conversion Time is defined as the time to take for one measurement to complete for one channel and update the results in output register. Since OPT4048 is 4 channel device the actual time to complete a 4 channel measurement is 4 times the time specified in the CONVERSION_TIME register. Measurement initiation is determined by the mode of operation as specified in セクション 8.3.4.1.

表 8-4. Conversion Time Selection

CONVERSION_TIME Register	Typical Conversion Time Per Channel
0	600 µs
1	1 ms
2	1.8 ms
3	3.4 ms
4	6.5 ms
5	12.7 ms
6	25 ms
7	50 ms
8	100 ms
9	200 ms
10	400 ms
11	800 ms

8.3.4.5 Light and Color Measurement

The OPT4048 device measures light on 4 independent channels and updates output registers with proportional ADC codes. Updated are based on the mode of operation as described in セクション 8.3.4.1. If readout of output registers is performed before a successful completion of a measurement, the previous measurement is what would be read out. Output of the each channel is represented by two parts (i) 4 bits of EXPONENT_CHx and (ii) 20 bits of MANTISSA_CHx. This arrangement of binary logarithmic full-scale range with linear representation with in a range, helps in covering a large dynamic range of measurements. MANTISSA here represents the linear ADC codes proportional to the measured light within a given full-scale range and the EXPONENT_CHx represents the current-full scale range selected. The selected range can be automatically determined by the auto-range selection logic or manually selected as per 表 8-3.

Lux level can be determined using the following equations:

$$MANTISSA\_CHx=(RESULT\_MSB\_CHx<<8) + RESULT\_LSB\_CHx \quad (1)$$

or

$$MANTISSA\_CHx=(RESULT\_MSB\_CHx \times 2^8) + RESULT\_LSB\_CHx \quad (2)$$

where RESULT_MSB_CHx, RESULT_LSB_CHx and EXPONENT_CHx are registers part of the output register for each channel

RESULT_MSB_CHx register carries the most significant 12 bits of the MANTISSA_CHx and RESULT_LSB_CHx register carries the least significant 8 bits of the MANTISSA_CHx. MANTISSA_CHx is then computed using the above equations to get the 20 bit number. EXPONENT_CHx is directly read from the register which is 4 bits.

Once the EXPONENT_CHx and MANTISSA_CHx portions are calculated the linearized ADC_CODES_CHx is calculated using the following equation:

$$ADC\_CODES\_CHx = (MANTISSA\_CHx<<EXPONENT\_CHx) \quad (3)$$

or

$$ADC\_CODES\_CHx = (MANTISSA\_CHx \times 2^{EXPONENT\_CHx}) \quad (4)$$

With maximum value for register EXPONENT_CHx being 8 ADC_CODES is effectively a 28 bit number. The semi-logarithmic numbers have been converted to a linear ADC_CODES_CHx representation making simple to convert to lux and CIE XY color coordinates

Conversion of the raw ADC codes to the CIE colorimetric X, Y and lux are given by the equation below

$$[adc\_codes\_ch0\ adc\_codes\_ch1\ adc\_codes\_ch2\ adc\_codes\_ch3] \cdot \begin{bmatrix} m0x & m0y & m0z & m0l \\ m1x & m1y & m1z & m1l \\ m2x & m2y & m2z & m2l \\ m3x & m3y & m3z & m3l \end{bmatrix} = [x\ y\ z\ lux] \quad (5)$$

$$CIEx = \frac{x}{x + y + z} \quad (6)$$

$$CIEy = \frac{y}{x + y + z} \quad (7)$$

The conversion matrix can be customized based on target application and details for the same can be found in セクション 9.2.4.

Lux Calculations

As listed in the 式 5 lux values can be obtained along with the color information as part of the matrix. However, isolating the lux calculations from the matrix can be useful. In that case, the matrix can be simplified to remove lux calculations as shown below

$$[adc\_codes\_ch0\ adc\_codes\_ch1\ adc\_codes\_ch2\ adc\_codes\_ch3] \cdot \begin{bmatrix} m0x & m0y & m0z \\ m1x & m1y & m1z \\ m2x & m2y & m2z \\ m3x & m3y & m3z \end{bmatrix} = [x\ y\ z] \quad (8)$$

Lux can be simply calculated using the following equation

lux = adc_codes_ch1 x 2.15e-3 (9)

Threshold Detection Calculations

Threshold result registers THRESHOLD_H_RESULT and THRESHOLD_H_RESULT are 12 bit, while threshold exponent registers THRESHOLD_H_EXPONENT and THRESHOLD_L_EXPONENT are 4 bits. Since threshold is compared at linear ADC_CODES_CHx, the threshold registers are padded with zeros internally as shown to compare with the ADC_CODES_CHx

ADC_CODES_TH = THRESHOLD_H_RESULT << (8 + THRESHOLD_H_EXPONENT) (10)

or

ADC_CODES_TH = THRESHOLD_H_RESULT x 2^(8 + THRESHOLD_H_EXPONENT) (11)

and

ADC_CODES_TL = THRESHOLD_L_RESULT << (8 + THRESHOLD_L_EXPONENT) (12)

or

ADC_CODES_TL=THRESHOLD_L_RESULT x 2^(8 + THRESHOLD_L_EXPONENT) (13)

Threshold are then compared as shown to detect Fault events.

If ADC_CODES_CHx < ADC_CODES_TL a Fault Low is detected (14)

and

If ADC_CODES_CHx > ADC_CODES_TH a Fault High is detected (15)

Based on the FAULT_COUNT register setting, with consecutive Fault High or Fault Low events, respective FLAG_H and FLAG_L registers are set. Clearly understanding the difference between THRESHOLD_H_EXPONENT, THRESHOLD_H_RESULT, THRESHOLD_L_EXPONENT, THRESHOLD_L_RESULT and the output registers is important to be able to set appropriate threshold based on application needs. More details can be found in セクション 8.3.4.2.

8.3.4.6 Light Resolution

The OPT4048 device's effective resolution is dependent on both the conversion time setting and the full-scale light range. Although the LSB resolution of the linear ADC_CODES doesn't change, the effective or useful resolution of the device is dependent on the conversion time setting and the full-scale range as per the table below. In conversion times where the effective resolution is lower, the LSBs are padded with 0.

表 8-5. Resolution Table

CONVERSION_TIME register	Conversion Time	MANTESSA effective bits	EXPONENT	0	1	2	3	4	5	6
			Full-scale lux	2254	4509	9018	18036	36071	72142	144284
			Effective Resolution in lux							
0	600 us	9		4.4	8.8	17.6	35.2	70.45	140.9	281.8
1	1 ms	10		2.2	4.4	8.8	17.6	35.2	70.45	140.9
2	1.8 ms	11		1.1	2.2	4.4	8.8	17.6	35.2	70.45
3	3.4 ms	12		550.4 m	1.1	2.2	4.4	8.8	17.6	35.2
4	6.5 ms	13		275.2 m	550.4 m	1.1	2.2	4.4	8.8	17.6
5	12.7 ms	14		137.6 m	275.2 m	550.4 m	1.1	2.2	4.4	8.8
6	25 ms	15		68.8 m	137.6 m	275.2 m	550.4 m	1.1	2.2	4.4
7	50 ms	16		34.4 m	68.8 m	137.6 m	275.2 m	550.4 m	1.1	2.2
8	100 ms	17		17.2 m	34.4 m	68.8 m	137.6 m	275.2 m	550.4 m	1.1
9	200 ms	18		8.6 m	17.2 m	34.4 m	68.8 m	137.6 m	275.2 m	550.4 m
10	400 ms	19		4.30 m	8.6 m	17.2 m	34.4 m	68.8 m	137.6 m	275.2 m
11	800 ms	20		2.15 m	4.30 m	8.6 m	17.2 m	34.4 m	68.8 m	137.6 m

As shown in the table above the resolution of the device is dependent on the CONVERSION_TIME and full-scale range. A similar scaling applies to the peak responsitivity for each channel.

8.3.4.7 Programming

The OPT4048 supports the transmission protocol for standard mode (up to 100 kHz), fast mode (up to 400 kHz), and high-speed mode (up to 2.6 MHz). Fast and standard modes are described as the default protocol, referred to as *F/S*. High-speed mode is described in the セクション 8.3.4.7.2.1.

8.3.4.7.1 I²C Bus Overview

The OPT4048 offers compatibility with both I²C and SMBus interfaces. The I²C and SMBus protocols are essentially compatible with one another. The I²C interface is used throughout this document as the primary example with the SMBus protocol specified only when a difference between the two protocols is discussed.

The device is connected to the bus with two pins: an SCL clock input pin and an SDA open-drain bidirectional data pin. The bus must have a controller device that generates the serial clock (SCL), controls the bus access, and generates start and stop conditions. To address a specific device, the controller initiates a start condition by pulling the data signal line (SDA) from a high logic level to a low logic level while SCL is high. All targets on the bus shift in the target address byte on the SCL rising edge, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the target being addressed responds to the controller by generating an acknowledge bit by pulling SDA low.

Data transfer is then initiated and eight bits of data are sent, followed by an acknowledge bit. During data transfer, SDA must remain stable while SCL is high. Any change in SDA while SCL is high is interpreted as a start or stop condition. When all data are transferred, the controller generates a stop condition, indicated by

pulling SDA from low to high while SCL is high. The device includes a 28-ms timeout on the I²C interface to prevent locking up the bus. If the SCL line is held low for this duration of time, the bus state machine is reset.

8.3.4.7.1.1 Serial Bus Address

To communicate with the OPT4048, the controller must first initiate an I²C start command. Then, the controller must address target devices via a target address byte. The target address byte consists of a seven bit address and a direction bit that indicates whether the action is to be a read or write operation.

Four I²C addresses are possible by connecting the ADDR pin to one of four pins: GND, VDD, SDA, or SCL. Table below summarizes the possible addresses with the corresponding ADDR pin configuration. The state of the ADDR pin is sampled on every bus communication and must be driven or connected to the desired level before any activity on the interface occurs.

ADDR PIN CONNECTION	DEVICE I²C ADDRESS
GND	1000100
VDD	1000101
SDA	1000110
SCL	1000101

8.3.4.7.1.2 Serial Interface

The OPT4048 operates as a target device on both the I²C bus and SMBus. Connections to the bus are made via the SCL clock input line and the SDA open-drain I/O line. The device supports the transmission protocol for standard mode (up to 100 kHz), fast mode (up to 400 kHz), and high-speed mode (up to 2.6 MHz). All data bytes are transmitted most-significant bits first.

The SDA and SCL pins feature integrated spike-suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. See the セクション 9.2.1 for further details of the I²C bus noise immunity.

8.3.4.7.2 Writing and Reading

Accessing a specific register on the OPT4048 is accomplished by writing the appropriate register address during the I²C transaction sequence. Refer to セクション 8.4 for a complete list of registers and their corresponding register addresses. The value for the register address (as shown in セクション 8.4) is the first byte transferred after the target address byte with the R/W bit low.

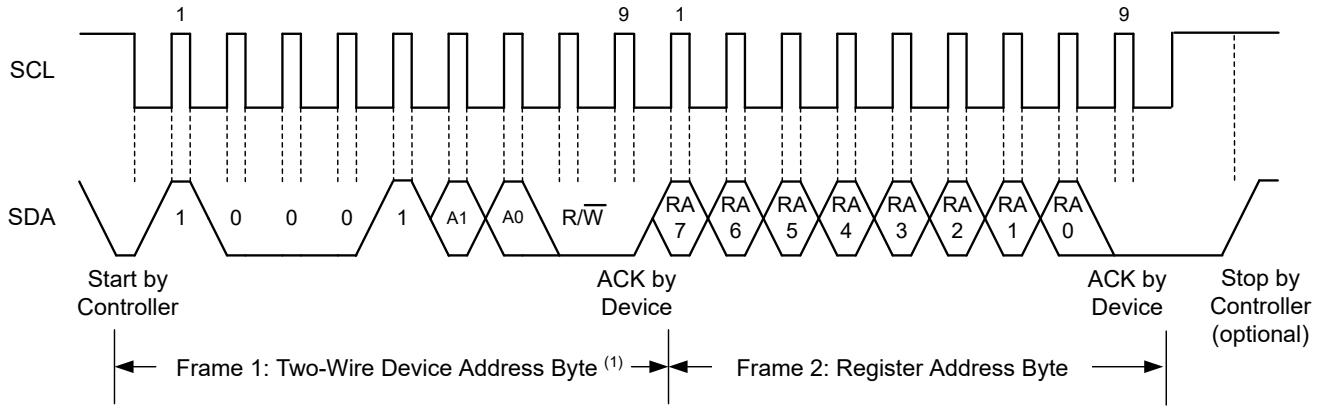


図 8-3. Setting the I²C Register Address

Writing to a register begins with the first byte transmitted by the controller. This byte is the target address with the R/W bit low. The device then acknowledges receipt of a valid address. The next byte transmitted by the controller is the address of the register that data are to be written to. The next two bytes are written to the register addressed by the register address. The device acknowledges receipt of each data byte. The controller can terminate the data transfer by generating a start or stop condition.

When reading from the device, the last value stored in the register address by a write operation determines which register is read during a read operation. To change the register address for a read operation, a new partial I²C write transaction must be initiated. This partial write is accomplished by issuing a target address byte with the R/W bit low, followed by the register address byte and a stop command. The controller then generates a start condition and sends the target address byte with the R/W bit high to initiate the read command. The next byte is transmitted by the target and is the most significant byte of the register indicated by the register address. This byte is followed by an acknowledge from the controller; then the target transmits the least significant byte. The controller acknowledges receipt of the data byte. The controller can terminate the data transfer by generating a not-acknowledge after receiving any data byte, or by generating a start or stop condition. If repeated reads from the same register are desired, continually sending the register address bytes is not necessary; the device retains the register address until that number is changed by the next write operation.

図 8-4and 図 8-5show the write and read operation timing diagrams, respectively. Note that register bytes are sent most significant byte first, followed by the least significant byte.

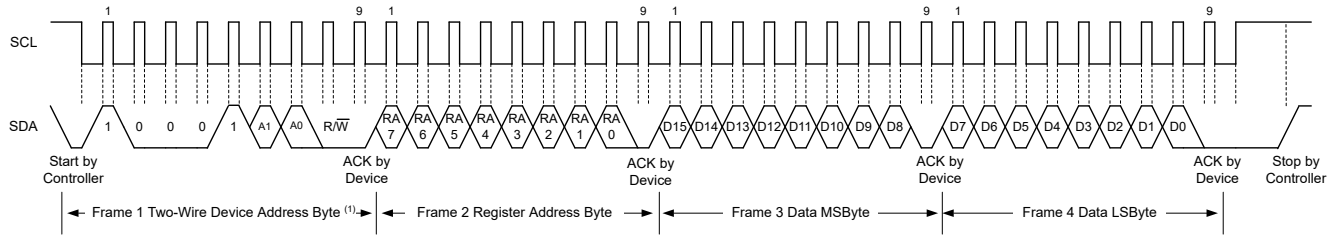
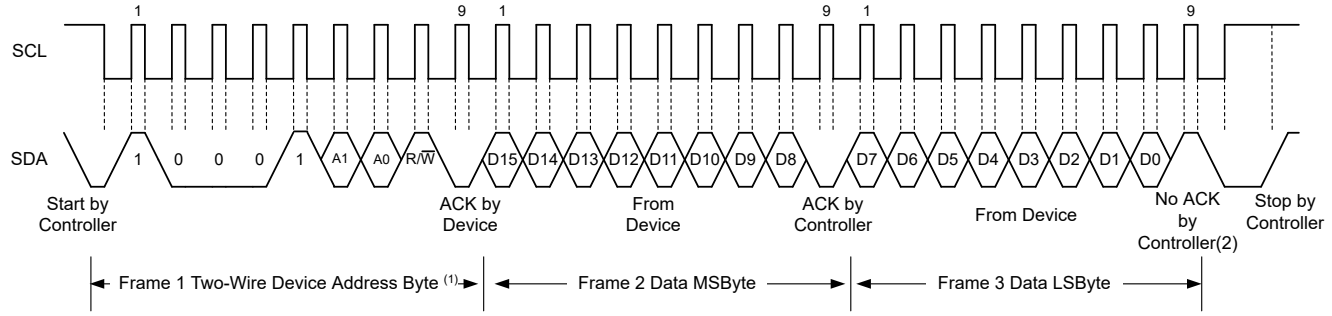


図 8-4. I²C Write Example



A. An ACK by the controller can also be sent.

図 8-5. I²C Read Example

8.3.4.7.2.1 High-Speed I²C Mode

When the bus is idle, both the SDA and SCL lines are pulled high by the pullup resistors or active pullup devices. The controller generates a start condition followed by a valid serial byte containing the high-speed (HS) controller code 0000 1XXXb. This transmission is made in either standard mode or fast mode (up to 400 kHz). The device does not acknowledge the HS controller code but does recognize the code and switches the internal filters to support a 2.6-MHz operation.

The controller then generates a repeated start condition (a repeated start condition has the same timing as the start condition). After this repeated start condition, the protocol is the same as F/S mode, except that transmission speeds up to 2.6 MHz are allowed. Instead of using a stop condition, use repeated start conditions to secure the bus in HS mode. A stop condition ends the HS mode and switches all internal filters of the device to support the F/S mode.

8.3.4.7.2.2 Burst Read Mode

OPT4048 supports I²C burst read mode which helps in minimizing the number of transactions on the bus for efficient data transfer from the device to the controller.

Before considering the burst mode, a regular I²C read transaction involves an I²C write operation to the device read pointer, followed by the actual I²C read operation. With the output registers in continuous locations, writing the register pointer every 2 bytes takes up several clock cycles. With the burst mode enabled, the read pointer address is auto incremented after every register read (2 bytes), eliminating the need write operations to set the pointer for subsequent register reads.

Burst mode can be enabled by setting the register I2C_BURST. When a STOP command is issued the pointer resets to the original register address before the auto-increments.

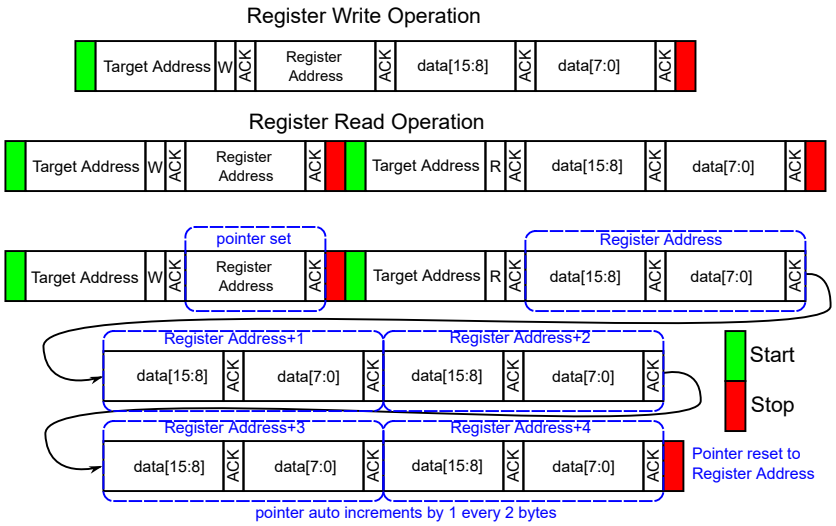


図 8-6. I²C Operations

8.3.4.7.2.3 General-Call Reset Command

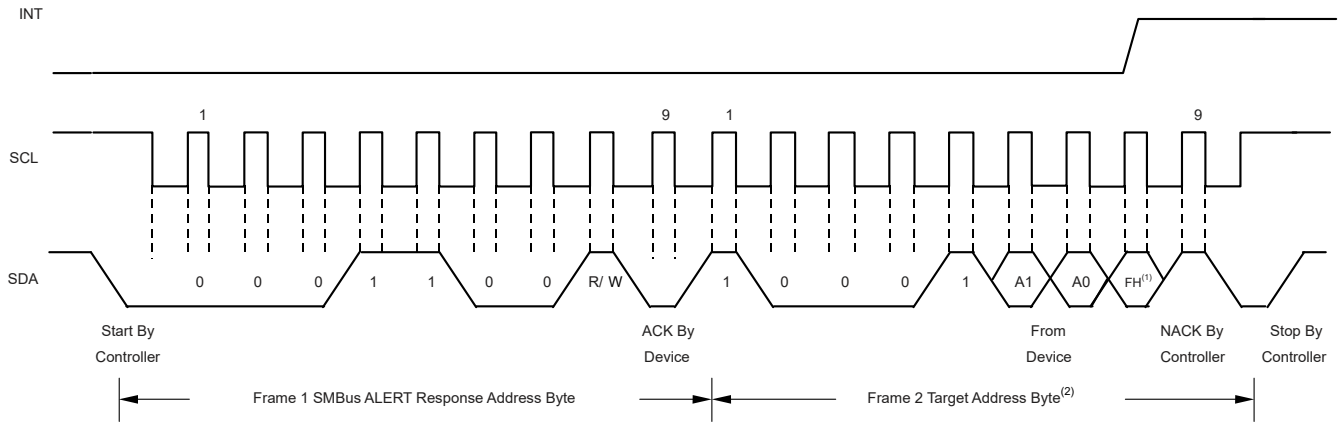
The I²C general-call reset allows the host controller in one command to reset all devices on the bus that respond to the general-call reset command. The general call is initiated by writing to the I²C address 0 (0000 0000b). The reset command is initiated when the subsequent second address byte is 06h (0000 0110b). With this transaction, the device issues an acknowledge bit and sets all registers to the power-on-reset default condition.

8.3.4.7.2.4 SMBus Alert Response

The SMBus alert response provides a quick identification for which device issued the interrupt. Without this alert response capability, the processor does not know which device pulled the interrupt line when there are multiple target devices connected.

OPT4048 is designed to respond to the SMBus alert response address, when in the latched window-style comparison mode. The OPT4048 does not respond to the SMBus alert response when in transparent mode.

The response behavior of the device to the SMBus alert response is shown in 図 8-7. When the interrupt line to the processor is pulled to active, the controller can broadcast the alert response target address. Following this alert response, any target devices that generated an alert identify themselves by acknowledging the alert response and sending respective I²C address on the bus. The alert response can activate several different target devices simultaneously. If more than one target attempts to respond, bus arbitration rules apply. The device with the lowest address wins the arbitration. If the OPT4048 loses the arbitration, the device does not acknowledge the I²C transaction and the INT pin remains in an active state, prompting the I²C controller processor to issue a subsequent SMBus alert response. When the OPT4048 wins the arbitration, the device acknowledges the transaction and sets the INT pin to inactive. The controller can issue that same command again, as many times as necessary to clear the INT pin. See セクション 8.3.4.2 for additional details of how the flags and INT pin are controlled. The controller can obtain information about the source of the OPT4048 interrupt from the address broadcast in the above process. The FLAG_H value is sent as the final LSB of the address to provide the controller additional information about the cause of the OPT4048 interrupt. If the controller requires additional information, the result register or the configuration register can be queried. The FLAG_Hand FLAG_L registers are not cleared upon an SMBus alert response.



A. FH is the FLAG_H register
B. A1 and A0 are determined by the ADDR pin

図 8-7. Timing Diagram for SMBus Alert Response

8.4 Register Maps

図 8-8. ALL Register Map

ADD	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
00h	EXPONENT_CH0				RESULT_MSB_CH0											
01h	RESULT_LSB_CH0								COUNTER_CH0				CRC_CH0			
02h	EXPONENT_CH1				RESULT_MSB_CH1											
03h	RESULT_LSB_CH1								COUNTER_CH1				CRC_CH1			
04h	EXPONENT_CH2				RESULT_MSB_CH2											
05h	RESULT_LSB_CH2								COUNTER_CH2				CRC_CH2			
06h	EXPONENT_CH3				RESULT_MSB_CH3											
07h	RESULT_LSB_CH3								COUNTER_CH3				CRC_CH3			
08h	THRESHOLD_L_EXPONENT				THRESHOLD_L_RESULT											
09h	THRESHOLD_H_EXPONENT				THRESHOLD_H_RESULT											
0Ah	QWAKE	0	RANGE				CONVERSION_TIME				OPERATING_MODE		LATCH	INT_POL	FAULT_COUNT	
0Bh	128									THRESHOLD_CH_SEL		INT_DIR	INT_CFG		0	I2C_BURST
0Ch	0												OVERLOAD_FLAG	CONVERSION_READY_FLAG	FLAG_H	FLAG_L
11h	0		DIDL		DIDH											

8.4.1 ALL Register Map

8.4.1.1 Register 0h (offset = 0h) [reset = 0h]

図 8-9. Register 0h

15	14	13	12	11	10	9	8
EXPONENT_CH0				RESULT_MSB_CH0			
R-0h				R-0h			
7	6	5	4	3	2	1	0
RESULT_MSB_CH0							
R-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

図 8-10. Register 00 Field Descriptions

Bit	Field	Type	Reset	Description
15-12	EXPONENT_CH0	R	0h	EXPONENT output CH0. Determines the full-scale range of the light measurement for the channel.
11-0	RESULT_MSB_CH0	R	0h	Result register MSB (Most significant bits) CH0. Used to calculate the MANTISSA representing light level within a given EXPONENT or full-scale range

8.4.1.2 Register 1h (offset = 1h) [reset = 0h]

図 8-11. Register 1h

15	14	13	12	11	10	9	8
RESULT_LSB_CH0							
R-0h							
7	6	5	4	3	2	1	0
COUNTER_CH0				CRC_CH0			
R-0h				R-0h			

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

図 8-12. Register 01 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESULT_LSB_CH0	R	0h	Result register LSB(Least significant bits) CH0. Used to calculate MANTISSA representing light level within a given EXPONENT or full-scale range
7-4	COUNTER_CH0	R	0h	Sample counter CH0. Rolling counter which increments for every conversion
3-0	CRC_CH0	R	0h	CRC bits CH0. R[19:0]=(RESULT_MSB_CH0[11:0]<<8)+RESULT_LSB_CH0[7:0] X[0]=XOR(EXPONENT_CH0[3:0],R[19:0],CRC_CH0[3:0]) XOR of all bits X[1]=XOR(CRC_CH0[1],CRC_CH0[3],R[1],R[3],R[5],R[7],R[9],R[11],R[13],R[15],R[17],R[19],E[1],E[3]) X[2]=XOR(CRC_CH0[3],R[3],R[7],R[11],R[15],R[19],E[3]) X[3]=XOR(R[3],R[11],R[19])

8.4.1.3 Register 2h (offset = 2h) [reset = 0h]

図 8-13. Register 2h

15	14	13	12	11	10	9	8

図 8-13. Register 2h (continued)

EXPONENT_CH1				RESULT_MSB_CH1			
R-0h				R-0h			
7	6	5	4	3	2	1	0
RESULT_MSB_CH1							
R-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

図 8-14. Register 02 Field Descriptions

Bit	Field	Type	Reset	Description
15-12	EXPONENT_CH1	R	0h	EXPONENT output CH1. Determines the full-scale range of the light measurement for the channel.
11-0	RESULT_MSB_CH1	R	0h	Result register MSB (Most significant bits) CH1. Used to calculate the MANTISSA representing light level within a given EXPONENT or full-scale range

8.4.1.4 Register 3h (offset = 3h) [reset = 0h]

図 8-15. Register 3h

15	14	13	12	11	10	9	8
RESULT_LSB_CH1							
R-0h							
7	6	5	4	3	2	1	0
COUNTER_CH1				CRC_CH1			
R-0h				R-0h			

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

図 8-16. Register 03 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESULT_LSB_CH1	R	0h	Result register LSB(Least significant bits) CH1. Used to calculate MANTISSA representing light level within a given EXPONENT or full-scale range
7-4	COUNTER_CH1	R	0h	Sample counter CH1. Rolling counter which increments for every conversion
3-0	CRC_CH1	R	0h	CRC bits CH1. R[19:0]=(RESULT_MSB_CH1[11:0] <<8)+RESULT_LSB_CH1[7:0] X[0]=XOR(EXPONENT_CH1[3:0],R[19:0],CRC_CH1[3:0]) XOR of all bits X[1]=XOR(CRC_CH1[1],CRC_CH1[3],R[1],R[3],R[5],R[7], R[9],R[11],R[13],R[15],R[17],R[19],E[1],E[3]) X[2]=XOR(CRC_CH1[3],R[3],R[7],R[11],R[15],R[19],E[3]) X[3]=XOR(R[3],R[11],R[19])

8.4.1.5 Register 4h (offset = 4h) [reset = 0h]

図 8-17. Register 4h

15	14	13	12	11	10	9	8
EXPONENT_CH2				RESULT_MSB_CH2			
R-0h				R-0h			
7	6	5	4	3	2	1	0

図 8-17. Register 4h (continued)

RESULT_MSB_CH2
R-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

図 8-18. Register 04 Field Descriptions

Bit	Field	Type	Reset	Description
15-12	EXPONENT_CH2	R	0h	EXPONENT output CH2. Determines the full-scale range of the light measurement for the channel.
11-0	RESULT_MSB_CH2	R	0h	Result register MSB (Most significant bits) CH2. Used to calculate the MANTISSA representing light level within a given EXPONENT or full-scale range

8.4.1.6 Register 5h (offset = 5h) [reset = 0h]

図 8-19. Register 5h

15	14	13	12	11	10	9	8
RESULT_LSB_CH2							
R-0h							
7	6	5	4	3	2	1	0
COUNTER_CH2				CRC_CH2			
R-0h				R-0h			

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

図 8-20. Register 05 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESULT_LSB_CH2	R	0h	Result register LSB(Least significant bits) CH2. Used to calculate MANTISSA representing light level within a given EXPONENT or full-scale range
7-4	COUNTER_CH2	R	0h	Sample counter CH2. Rolling counter which increments for every conversion
3-0	CRC_CH2	R	0h	CRC bits CH2. R[19:0]=(RESULT_MSB_CH2[11:0]<<8)+RESULT_LSB_CH2[7:0] X[0]=XOR(EXPONENT_CH2[3:0],R[19:0],CRC_CH2[3:0]) XOR of all bits X[1]=XOR(CRC_CH2[1],CRC_CH2[3],R[1],R[3],R[5],R[7],R[9],R[11],R[13],R[15],R[17],R[19],E[1],E[3]) X[2]=XOR(CRC_CH2[3],R[3],R[7],R[11],R[15],R[19],E[3]) X[3]=XOR(R[3],R[11],R[19])

8.4.1.7 Register 6h (offset = 6h) [reset = 0h]

図 8-21. Register 6h

15	14	13	12	11	10	9	8
EXPONENT_CH3				RESULT_MSB_CH3			
R-0h				R-0h			
7	6	5	4	3	2	1	0
RESULT_MSB_CH3							
R-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

図 8-22. Register 06 Field Descriptions

Bit	Field	Type	Reset	Description
15-12	EXPONENT_CH3	R	0h	EXPONENT output CH3. Determines the full-scale range of the light measurement for the channel.
11-0	RESULT_MSB_CH3	R	0h	Result register MSB (Most significant bits) CH3. Used to calculate the MANTISSA representing light level within a given EXPONENT or full-scale range

8.4.1.8 Register 7h (offset = 7h) [reset = 0h]

図 8-23. Register 7h

15	14	13	12	11	10	9	8
RESULT_LSB_CH3							
R-0h							
7	6	5	4	3	2	1	0
COUNTER_CH3				CRC_CH3			
R-0h				R-0h			

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

図 8-24. Register 07 Field Descriptions

Bit	Field	Type	Reset	Description
15-8	RESULT_LSB_CH3	R	0h	Result register LSB(Least significant bits) CH3. Used to calculate MANTISSA representing light level within a given EXPONENT or full-scale range
7-4	COUNTER_CH3	R	0h	Sample counter CH3. Rolling counter which increments for every conversion
3-0	CRC_CH3	R	0h	CRC bits CH3. R[19:0]=(RESULT_MSB_CH3[11:0]<<8)+RESULT_LSB_CH3[7:0] X[0]=XOR(EXPONENT_CH3[3:0],R[19:0],CRC_CH3[3:0]) XOR of all bits X[1]=XOR(CRC_CH3[1],CRC_CH3[3],R[1],R[3],R[5],R[7],R[9],R[11],R[13],R[15],R[17],R[19],E[1],E[3]) X[2]=XOR(CRC_CH3[3],R[3],R[7],R[11],R[15],R[19],E[3]) X[3]=XOR(R[3],R[11],R[19])

8.4.1.9 Register 8h (offset = 8h) [reset = 0h]

図 8-25. Register 8h

15	14	13	12	11	10	9	8
THRESHOLD_L_EXPONENT				THRESHOLD_L_RESULT			
R/W-0h				R/W-0h			
7	6	5	4	3	2	1	0
THRESHOLD_L_RESULT							
R/W-0h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

図 8-26. Register 08 Field Descriptions

Bit	Field	Type	Reset	Description
15-12	THRESHOLD_L_EXPONENT	R/W	0h	Threshold low register exponent
11-0	THRESHOLD_L_RESULT	R/W	0h	Threshold low register result

8.4.1.10 Register 9h (offset = 9h) [reset = BFFFh]

図 8-27. Register 9h

15	14	13	12	11	10	9	8
THRESHOLD_H_EXPONENT				THRESHOLD_H_RESULT			
R/W-Bh				R/W-Fh			
7	6	5	4	3	2	1	0
THRESHOLD_H_RESULT							
R/W-FFh							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

図 8-28. Register 09 Field Descriptions

Bit	Field	Type	Reset	Description
15-12	THRESHOLD_H_EXPONENT	R/W	Bh	Threshold high register exponent
11-0	THRESHOLD_H_RESULT	R/W	FFFh	Threshold high register result

8.4.1.11 Register Ah (offset = Ah) [reset = 3208h]

図 8-29. Register Ah

15	14	13	12	11	10	9	8
QWAKE	0	RANGE				CONVERSION_TIME	
R/W-0h	W-0h	R/W-Ch				R/W-2h	
7	6	5	4	3	2	1	0
CONVERSION_TIME		OPERATING_MODE		LATCH	INT_POL	FAULT_COUNT	
R/W-0h		R/W-0h		R/W-1h	R/W-0h	R/W-0h	

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

図 8-30. Register 0A Field Descriptions

Bit	Field	Type	Reset	Description
15-15	QWAKE	R/W	0h	Quick Wake-up from Standby in one shot mode by not powering down all circuits. Applicable only in One-shot mode and helps get out of standby mode faster with penalty in power consumption compared to full standby mode.
14-14	0	W	0h	Must read or write 0

図 8-30. Register 0A Field Descriptions (continued)

Bit	Field	Type	Reset	Description
13-10	RANGE	R/W	Ch	Controls the full-scale light level range of the device. The format of this register is same as the EXPONENT register for all values from 0 to 6. 0 : 2.2klux 1 : 4.5kux 2 : 9klux 3 : 18klux 4 : 36klux 5 : 72klux 6 : 144klux 12 : Auto-Range
9-6	CONVERSION_TIME	R/W	8h	Controls the device conversion time per channel 0 : 600 us 1 : 1 ms 2 : 1.8 ms 3 : 3.4 ms 4 : 6.5 ms 5 : 12.7 ms 6 : 25 ms 7 : 50 ms 8 : 100 ms 9 : 200 ms 10 : 400 ms 11 : 800 ms
5-4	OPERATING_MODE	R/W	0h	Controls device mode of operation 0 : Power-down 1 : Forced auto-range OneShot 2 : OneShot 3 : Continuous
3-3	LATCH	R/W	1h	Controls the functionality of the interrupt reporting mechanisms for INT pin for the threshold detection logic.
2-2	INT_POL	R/W	0h	Controls the polarity or active state of the INT pin. 0 : Active Low 1 : Active High
1-0	FAULT_COUNT	R/W	0h	Fault count register instructs the device as to how many consecutive fault events are required to trigger the threshold mechanisms: the flag high (FLAG_H) and the flag low (FLAG_L) registers. 0 : One fault Count 1 : Two Fault Counts 2 : Four Fault Counts 3 : Eight Fault Counts

8.4.1.12 Register Bh (offset = Bh) [reset = 8011h]

図 8-31. Register Bh

15	14	13	12	11	10	9	8
1	0	0	0	0	0	0	0
R/W-1h	R/W-0h	W-0h	W-0h	W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	THRESHOLD_CH_SEL		INT_DIR	INT_CFG		0	I2C_BURST
R/W-0h	R/W-0h		R/W-1h	R/W-0h		R/W-0h	R/W-1h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

図 8-32. Register 0B Field Descriptions

Bit	Field	Type	Reset	Description
15-7	128	R/W	80h	Must read or write 128
6-5	THRESHOLD_CH_SEL	R/W	0h	Channel select for threshold logic 0 : CH0 Selected 1 : CH1 Selected 2 : CH2 Selected 3 : CH3 Selected
4-4	INT_DIR	R/W	1h	Determines the direction of the INT pin. 0 : Input 1 : Output
3-2	INT_CFG	R/W	0h	Controls the output interrupt mechanism after end of conversion 0 : SMBUS Alert 1 : INT Pin data ready for next channel 3 : INT Pin data ready for all channels
1-1	0	R/W	0h	Must read or write 0
0-0	I2C_BURST	R/W	1h	When set enables I2C burst mode minimizing I2C read cycles by auto incrementing read register point by 1 after every register read

8.4.1.13 Register Ch (offset = Ch) [reset = 0h]

図 8-33. Register Ch

15	14	13	12	11	10	9	8
0	0	0	0	0	0	0	0
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h	R/W-0h
7	6	5	4	3	2	1	0
0	0	0	0	OVERLOAD_FLAG	CONVERSION_READY_FLAG	FLAG_H	FLAG_L
R/W-0h	R/W-0h	R/W-0h	R/W-0h	R-0h	R-0h	R-0h	R-0h

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

図 8-34. Register 0C Field Descriptions

Bit	Field	Type	Reset	Description
15-4	0	R/W	0h	Must read or write 0
3-3	OVERLOAD_FLAG	R	0h	Indicates when an overflow condition occurs in the data conversion process, typically because the light illuminating the device exceeds the full-scale range.
2-2	CONVERSION_READY_FLAG	R	0h	Conversion ready flag indicates when a conversion completes. The flag is set to 1 at the end of a conversion and is cleared (set to 0) when register address 0xA is either read or written with any non-zero value 0 : Conversion in progress 1 : Conversion is complete
1-1	FLAG_H	R	0h	Flag high register identifies that the result of a conversion is measurement than a specified level of interest. FLAG_H is set to 1 when the result is larger than the level in the THRESHOLD_H_EXPONENT and THRESHOLD_H_RESULT registers for a consecutive number of measurements defined by the FAULT_COUNT register.

図 8-34. Register 0C Field Descriptions (continued)

Bit	Field	Type	Reset	Description
0-0	FLAG_L	R	0h	Flag low register identifies that the result of a measurement is smaller than a specified level of interest. FLAG_L is set to 1 when the result is smaller than the level in the THRESHOLD_L_EXPONENT and THRESHOLD_L_RESULT registers for a consecutive number of measurements defined by the FAULT_COUNT register.

8.4.1.14 Register 11h (offset = 11h) [reset = 820h]

図 8-35. Register 11h

15	14	13	12	11	10	9	8
0	0	DIDL		DIDH			
R/W-0h	R/W-0h	R-0h		R-8h			
7	6	5	4	3	2	1	0
DIDH							
R-21h							

LEGEND: R/W = Read/Write; W = Write only; -n = value after reset

図 8-36. Register 11 Field Descriptions

Bit	Field	Type	Reset	Description
15-14	0	R/W	0h	Must read or write 0
13-12	DIDL	R	8h	Device ID L
11-0	DIDH	R	21h	Device ID H

9 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

9.1 Application Information

Color sensors are used in a wide variety of applications that require precise measurement of light as perceived by human eye, since the color sensors have a specialized filter that mimic human eye. The following sections shows crucial information about integrating OPT4048 in applications.

There are two categories of interface to the OPT4048: electrical and optical.

9.2 Typical Application

9.2.1 Electrical Interface

The electrical interface is quite simple, as illustrated in 図 9-1below. Connect the OPT4048 I^2C SDA and SCL pins to the same pins of an applications processor, micro controller, or other digital processor. If that digital processor requires an interrupt resulting from an event of interest from theOPT4048, then connect the INT pin to either an interrupt or general-purpose I/O pin of the processor. There are multiple uses for this INT pin, including triggering a measurement on one-shot mode, signaling the system to wake up from low-power mode, processing other tasks while waiting for an ambient light event of interest, or alerting the processor that a sample is ready to be read. Connect pullup resistors between a power supply appropriate for digital communication and the SDA and SCL pins (because the pins have open-drain output structures). If the INT pin is used, connect a pullup resistor to the INT pin. A typical value for these pullup resistors is 10 kΩ. The resistor choice can be optimized in conjunction to the bus capacitance to balance the system speed, power, noise immunity, and other requirements.

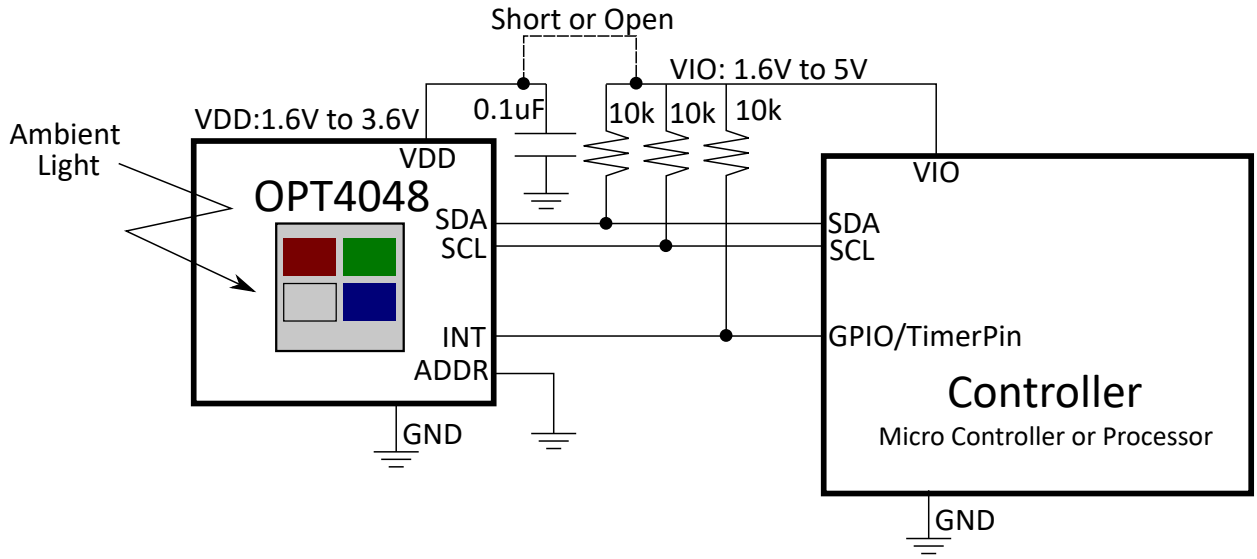


図 9-1. Typical Application Schematic

The power supply and grounding considerations are discussed in the *セクション 9.4*.

Although spike suppression is integrated in the SDA and SCL pin circuits, use proper layout practices to minimize the amount of coupling into the communication lines. One possible introduction of noise occurs from capacitively coupling signal edges between the two communication lines themselves. Another possible noise introduction comes from other switching noise sources present in the system, especially for long communication

lines. In noisy environments, shield communication lines to reduce the possibility of unintended noise coupling into the digital I/O lines that can be incorrectly interpreted.

9.2.2 Design Requirements

9.2.2.1 Optical Interface

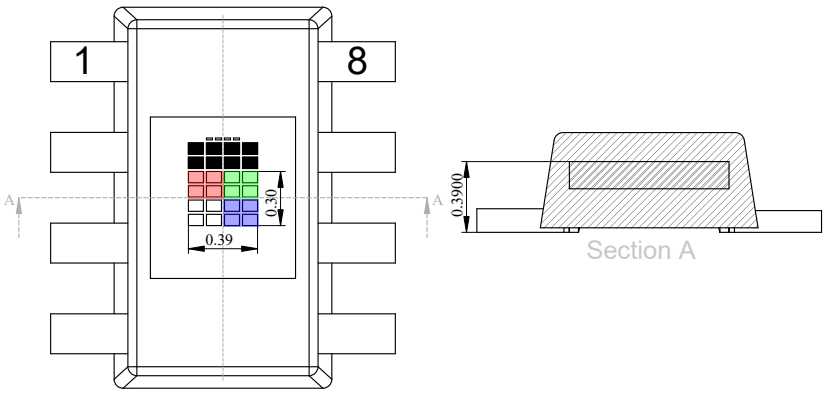


図 9-2. Sensor Position

Any physical component that affects the light which illuminates the sensing area of a light sensor also affects the performance of that light sensor. Therefore, for the best performance, make sure to understand and control the effect of these components. Design a window width and height to permit light from a sufficient field of view to illuminate the sensor. For best performance, use a field of view of at least ±35°, or preferably ±45° or more. Understanding and designing the field of view is discussed further in application report *OPT3001: Ambient Light Sensor Application Guide* (SBEA002)..

9.2.3 Detailed Design Procedure

9.2.3.1 Optomechanical Design

After completing the electrical design, the next task is the optomechanical design. Window sizing and placement is discussed in more rigorous detail in *OPT3001: Ambient Light Sensor Application Guide*.

9.2.4 Application Curves

Matrix values for Color determination

ADC measurements from OPT4048 channels can be used to determine the intensity (lux) and the color (CIE X,Y coordinates) as per specified in セクション 8.3.4.5. Here is an example of such measurements performed an RGB LED source TI LP5036EVM. The intensity of the Red, Green and Blue LEDs were varied independently and the corresponding color coordinates detected by OPT4048 (CIEx,CIEy) are plotted on the CIE XY and CIE UV color space.

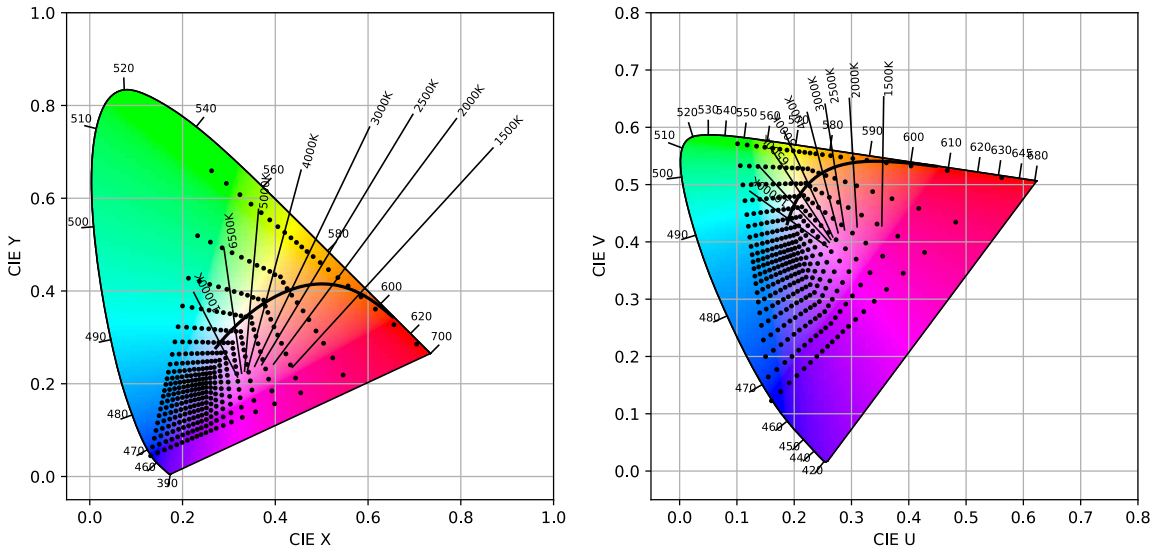


図 9-3. CIE XY and CIE UV space plots of color coordinates

Value of matrix used for this calculation is as shown below

$$\begin{bmatrix} 2.34892992e-04 & -1.89652390e-05 & 1.20811684e-05 & 0 \\ 4.07467441e-05 & 1.98958202e-04 & -1.58848115e-05 & 2.15e-3 \\ 9.28619404e-05 & -1.69739553e-05 & 6.74021520e-04 & 0 \\ 0 & 0 & 0 & 0 \end{bmatrix} \quad (16)$$

Correlated Color Temperature

The CIE XY and CIE UV color spaces shown in 図 9-3 and 図 9-4 has been annotated with the ideal black body curve and intersecting iso-thermal lines. The ideal black body curve represents the color perceived by human eye in CIE YX and CIE UV spaces when an ideal black body of certain Kelvins emit radiation. The intersecting lines with various kelvin markings are iso-thermal lines which represent the same color temperature and is commonly referred to as Correlated Color Temperature (CCT). CCT is a representation of how warm or cool a color source is which is a common terminology used in classifying light bulbs. CCT is often valid only around the ideal black body curve and does not make sense when there is too much deviation. Any color coordinate close to the ideal black body curve can be represented as having a particular CCT by using the formula below:

$$CCT = 437n^3 + 3601n^2 + 6861n + 5517 \quad (17)$$

where n is defined as

$$n = \frac{CIEx - 0.3320}{0.1858 - CIEy} \quad (18)$$

These are highly non-linear functions and the estimation of the CCT is very sensitive to the CIE X and CIE Y coordinates. Small errors due to non-ideality in the system can cause an amplified error in CCT estimation.

Set of off the shelf lamp sources were taken and the CCT values measured by OPT4048 is shown below.

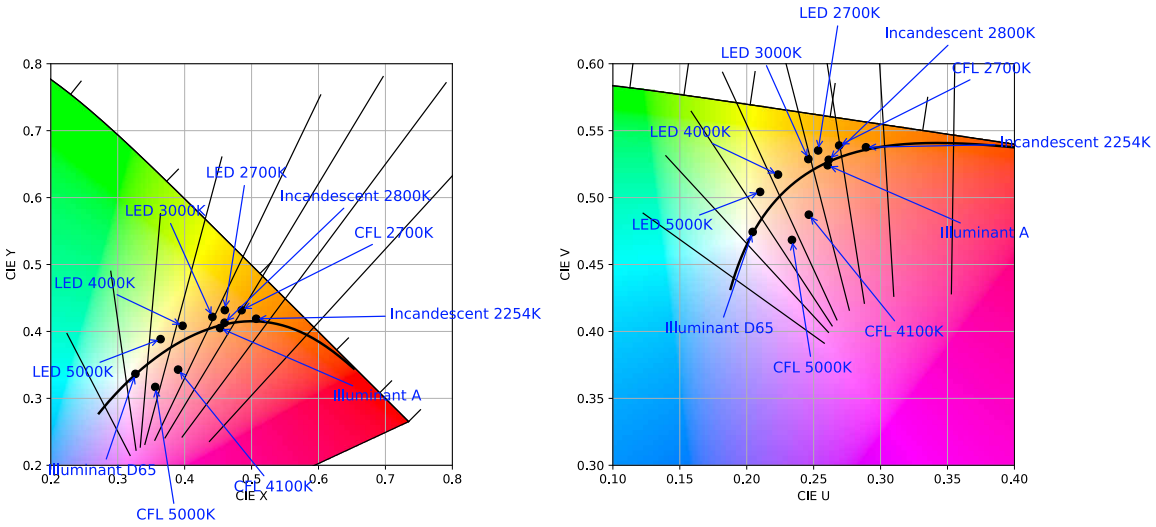


図 9-4. CIE XY and CIE UV Space Plots of Color Coordinates

The CIE color space plots have been zoomed-in to see the points more clearly. The annotation in the plot specify the color temperature of the lamps as specified by the manufacturer. While the lamp manufacturers approximate the CCT in Kelvins to nearest 1000 s, 500 s or 100 s, OPT4048 estimates the CCT high resolution using the equations specified above.

Color accuracy and the CCT accuracy can be further optimized based on the cavity design, cover glass and target application. More information is available at OPT4048.

9.3 Do's and Don'ts

As with any optical product, take special care when handling the OPT4048. The device is a piece of active silicon, without the mechanical protection of an epoxy-like package or other reinforcement. This design allows the device to be as thin as possible. Take extra care to handle the device gently to not crack or break the device. Use a properly-sized vacuum manipulation tool to handle the device.

The optical surface of the device must be kept clean for best performance, both when prototyping with the device, and during mass production manufacturing procedures. Keep the optical surface clean of fingerprints, dust, and other optical-inhibiting contaminants.

If the optical surface of the device requires cleaning, use a few gentle brushes with a soft swab of deionized water or isopropyl alcohol. Avoid potentially abrasive cleaning and manipulating tools and excessive force that can scratch the optical surface.

If the OPT4048 performs less than optimally, then inspect the optical surface for dirt, scratches, or other optical artifacts.

9.4 Power Supply Recommendations

Although the OPT4048 has low sensitivity to power-supply noise, good practices are always recommended. For best performance, the OPT4048 VDD pin must have a stable, low-noise power supply with a 100-nF bypass capacitor close to the device and solid grounding. There are many options for powering the OPT4048 because of the device low current consumption levels.

9.5 Layout

9.5.1 Layout Guidelines

The PCB layout design for the OPT4048 requires a couple of considerations. Bypass the power supply with a capacitor placed close to the device. Note that optically reflective surfaces of components also affect the performance of the design. The three-dimensional geometry of all components and structures around the sensor must be taken into consideration to prevent unexpected results from secondary optical reflections. Placing capacitors and components at a distance of at least twice the height of the component is usually sufficient. The best optical layout is to place all close components on the opposite side of the PCB from the device. However, this approach is not practical for the constraints of every design.

An example PCB layout with the OPT4048 is shown in 図 9-5.

9.5.2 Layout Example

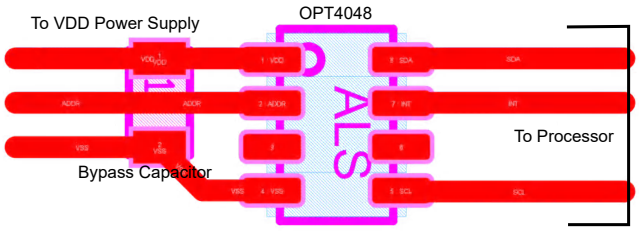


図 9-5. Example PCB Layout with the OPT4048 SOT-5X3 (8) Package

9.5.3 Soldering and Handling Recommendations

Soldering temperature profile and guidelines are published in future revisions of this document.

As with most optical devices, handle the OPT4048 with special care to ensure optical surfaces stay clean and free from damage. See セクション 9.3 for more detailed recommendations. For best optical performance, solder flux and any other possible debris must be cleaned after soldering processes.

注

The bottom side of the device features an angled feature to denote the PIN 1

図 9-6. Identification Feature for PIN 1

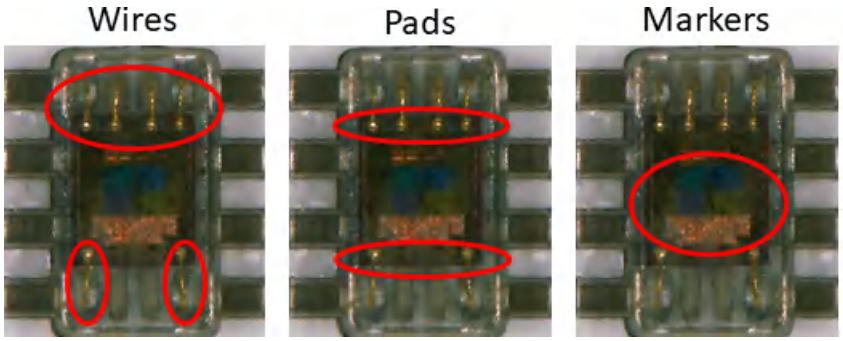


図 9-7. Identification Features for PIN 1 on Package

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

- *OPT4048EVM User's Guide*
- *OPT3001: Ambient Light Sensor Application Guide*

10.2 ドキュメントの更新通知を受け取る方法

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10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
OPT4048DTSR	Active	Production	SOT-5X3 (DTS) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4048
OPT4048DTSR.A	Active	Production	SOT-5X3 (DTS) | 8	3000 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	4048

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

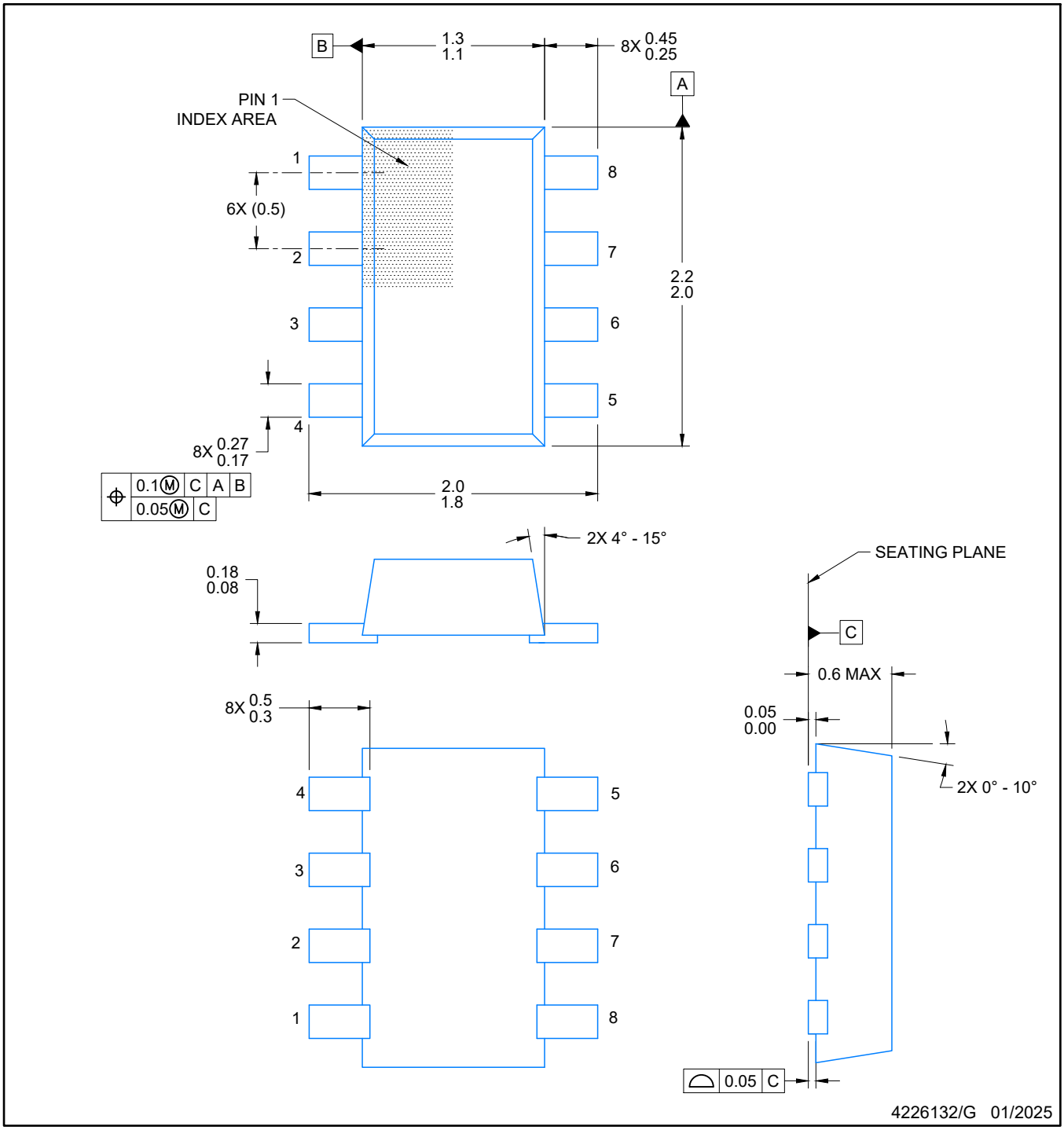
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

PACKAGE OUTLINE

DTS0008A

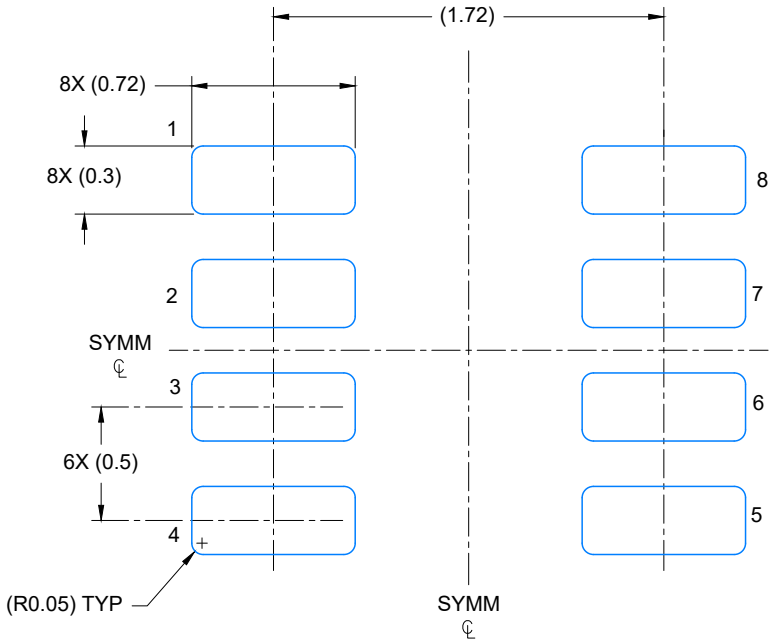
SOT - 0.6 mm max height

SMALL OUTLINE TRANSISTOR

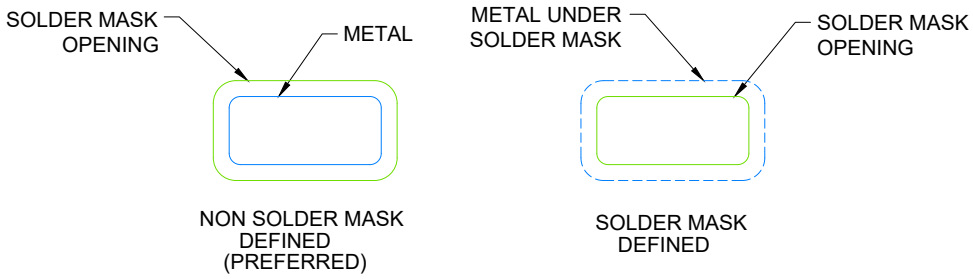


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not incude mold flash, protrusions or gate burrs. Mold flash, interlead flash, protrusions or gate burrs shall not exceed 0.171 per end or side.
4. The side flash along with the stub lead is allowed.
5. Any detached side flash from the stub lead is allowed unless it is touching the bottom side of the lead.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X



SOLDER MASK DETAILS

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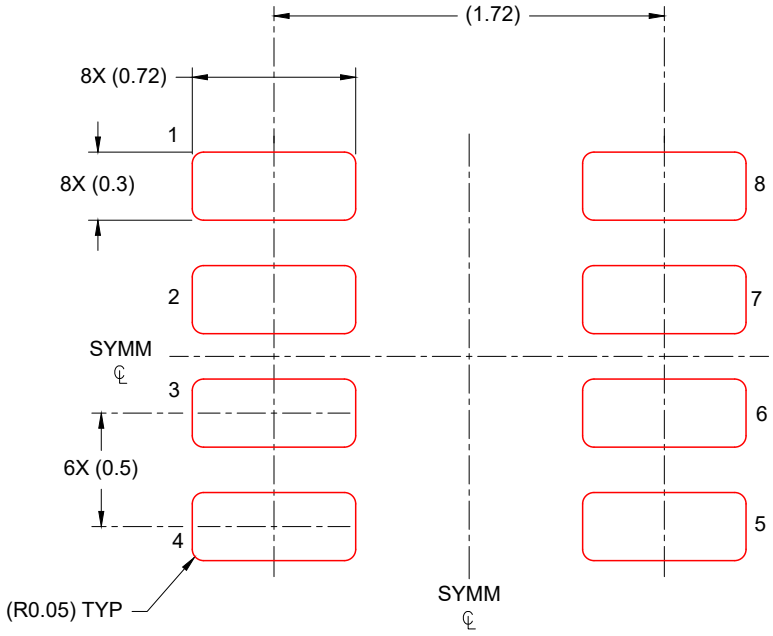
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Land pad design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 30X

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NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
10. Board assembly site may have different recommendations for stencil design.

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