REF35-Q1 超低消費電力、高精度の基準電圧

1 特長

- 以下の結果で AEC-Q100 認定済み:
  - デバイス温度グレード 1:動作時周囲温度範囲:-40℃～125℃
- 非常に小さい静止電流:
  - 650nA (代表値)
- 初期精度:±0.05 % (最大値)
- 温度ドリフト係数:
  - 15ppm/℃ (最大値、-40℃～125℃)
- 出力 1/f ノイズ (0.1Hz～10Hz):3.3ppm$_{P-P}$
- ノイズ低減用に NR ピンを搭載
- シャットダウン時の消費電流の低減用に EN ピンを搭載
- 長期安定性:1000 時間で 30ppm
- 仕様温度範囲:−40℃～+125℃
- 動作温度範囲:−55℃～+125℃
- 出力電流:+10mA、-5mA
- 入力電圧:V_{REF} + V_{DO} ～ 6V
- 出力電圧オプション:
  - 1.2V、1.25V、1.8V、2.048V、2.5V、3.0V、3.3V、4.096V、5.0V
- 小型の 6 ピン SOT-23 パッケージ

2 アプリケーション

- 車載用フロント・カメラ
- ドライバー監視
- バッテリ制御ユニット
- 電動パワー・ステアリング

3 概要

REF35-Q1 は、ナノパワー、低ドリフト、高精度を備えた一連のリファレンス・デバイスのファミリです。REF35-Q1 ファミリは、±0.05 % の初期精度と 650nA (代表値) の消費電力を特長としています。このデバイスの温度ドリフト係数 (15ppm/℃) と長期安定性 (1000 時間で 30ppm) は、システムの安定性と信頼性の向上に役立ちます。低消費電力と高精度の仕様を組み合わせて、広範な低電流アプリケーション向けに設計されています。

REF35-Q1 は、3.3ppm$_{p-p}$ ノイズおよび 20ppm/mA の負荷レギュレーションで、最大 10mA の電流を供給します。この機能セットにより、REF35-Q1 は高精度センサと 12～16 ビット・データ・コンバータ向けの強力な低ノイズで高精度の電源を実現します。

このファミリは -40℃～125℃向けに完全に動作が規定されており、-55℃～125℃で動作します。

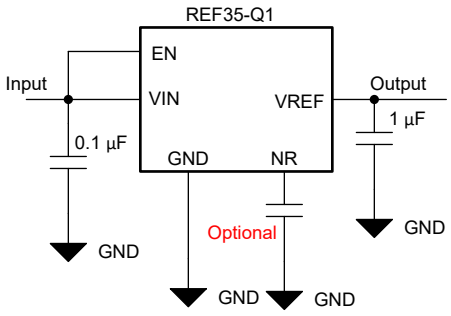
REF35-Q1 は、1.20V～5.0V の幅広い出力電圧範囲のバリアントで利用可能です。このデバイスは、省スペースの SOT23-6 ピン・パッケージで供給されます。使用可能な電圧オプションについては、テキサス・インスツルメンツの営業担当者にお問い合わせください。

製品情報

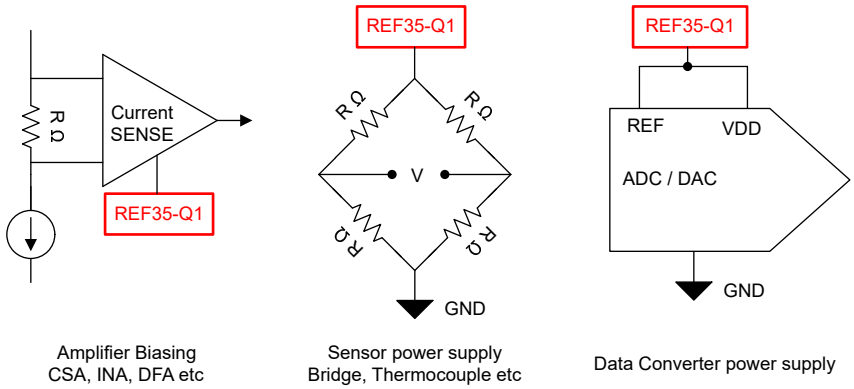
部品番号	パッケージ(1)	本体サイズ (公称)
REF35xxx-Q1	SOT-23 (6)	2.90mm × 1.60mm

(1) 利用可能なすべての電圧バリアントおよびパッケージについては、データシートの末尾にある注文情報を参照してください。

Connection Diagram



Typical Application Use Cases



Amplifier Biasing
CSA, INA, DFA etc

Sensor power supply
Bridge, Thermocouple etc

Data Converter power supply

REF35-Q1 のユースケース

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
August 2023	*	Initial Release

5 Device Comparison

PRODUCT	V_{REF}
REF35120QDBVRQ1 (1)	1.2 V
REF35125QDBVRQ1 (1)	1.25 V
REF35180QDBVRQ1	1.8 V
REF35205QDBVRQ1 (1)	2.048 V
REF35250QDBVRQ1 (1)	2.5 V
REF35300QDBVRQ1	3.0 V
REF35330QDBVRQ1 (1)	3.3 V
REF35409QDBVRQ1 (1)	4.096 V
REF35500QDBVRQ1 (1)	5.0 V

(1) Product preview. Contact local TI support for samples.

6 Pin Configuration and Functions

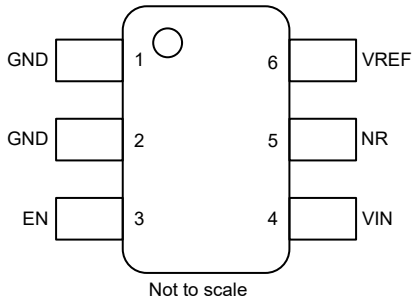


図 6-1. Package
6-Pin DBV
Top View

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	DBV		
GND	1	Ground	Device ground connection
GND	2	Ground	Device ground connection
EN	3	Input	Enable connection. Enables or disables the device.
VIN	4	Power	Input supply voltage connection
NR	5	Output	Noise reduction pin. Connect a capacitor to reduce noise.
VREF	6	Output	Reference voltage output

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN	–0.3	6.5	V
Enable voltage	EN	–0.3	VIN + 0.3 (2)	V
Output voltage	VREF	–0.3	VIN + 0.3 (2)	V
Output short circuit current	I_{SC}		20	mA
Operating temperature range	T_A	–55	125	°C
Storage temperature range	T_{stg}	–65	170	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) IN + 0.3 V or 6.5 V, whichever is lower

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins (2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VIN	Input voltage (1)	VREF+ V_{DO} (2)		6	V
EN	Enable voltage	0		VIN	V
I_L	Output current	–5		10	mA
T_A	Operating temperature	–40	25	125	°C

(1) For V_{REF} = 1.2 V and 1.25 V, minimum V_{IN} = 1.7 V
(2) V_{DO} = Dropout voltage

7.4 Thermal Information

THERMAL METRIC(1)		REF35-Q1 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	164.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	102.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	59.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	44.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	59.4	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

At V_{IN} = V_{REF} + 0.5 V, V_{EN} = V_{IN}, C_L = 10 µF, C_{IN} = 0.1 µF, I_L = 0 mA, minimum and maximum specifications at T_A = –40°C to 125°C, typical specifications T_A = 25°C; unless otherwise noted

PARAMETER		TEST CONDITION		MIN	TYP	MAX	UNIT
ACCURACY AND DRIFT							
	Output voltage accuracy	T_A = 25°C		–0.05		0.05	%
	Output voltage temperature coefficient	–40°C ≤ T_A ≤ 125°C				15	ppm/°C
LINE AND LOAD REGULATION							
$\Delta V_{REF}/\Delta V_{IN}$	Line regulation	V_{REF} < 2.5 V; V_{IN} = V_{REF} + V_{DO} to V_{INMAX}			40	160	ppm/V
		V_{REF} ≥ 2.5 V; V_{IN} = V_{REF} + V_{DO} to V_{INMAX}			40	120	ppm/V
$\Delta V_{REF}/\Delta I_L$	Load regulation	I_L = 0 mA to 10 mA, V_{IN} = V_{REF} + V_{DO}	Source		20	60	ppm/mA
		I_L = 0 mA to 5 mA, V_{IN} = V_{REF} + V_{DO}	Sink		40	350	ppm/mA
POWER SUPPLY							
V_{IN}	Input voltage (1)			V_{REF} + V_{DO}		6	V
I_Q	Quiescent current	Active mode	T_A = 25°C		0.65	0.9	µA
			–40°C ≤ T_A ≤ 125°C			2.6	
		Shutdown mode	T_A = 25°C			0.1	
			–40°C ≤ T_A ≤ 125°C			0.5	
V_{EN}	Enable pin voltage	Active mode (EN = 1 or Float)		0.7 x V_{IN}			V
		Shutdown mode (EN = 0)				0.3 x V_{IN}	
I_{EN}	Enable pin current	V_{EN} = V_{IN}			0.05	0.1	uA
V_{DO}	Dropout voltage	I_L = 5 mA				120	mV
		I_L = 10 mA				250	
I_{SC}	Short circuit current, Sourcing	V_{REF} = 0 V, T_A = 25°C			33		mA
I_{SC}	Short circuit current, Sinking	V_{REF} = V_{IN} V, T_A = 25°C			21		mA
TURN-ON TIME							
t_{ON}	Turn-on time (2)	0.1% settling, C_L = 1 µF, V_{REF} = 2.5 V			2		ms
NOISE							
e_n	Output voltage noise	f = 10 Hz to 1 kHz, C_L = 1 µF			0.7		ppm_{rms}
e_{np-p}	Low-frequency noise	f = 0.1 Hz to 10 Hz, V_{REF} ≥ 2.5 V			3.8		ppm_{p-p}
		f = 0.1 Hz to 10 Hz, V_{REF} < 2.5 V			3.3		ppm_{p-p}
HYSTERESIS AND LONG-TERM STABILITY							
	Long-term stability	0 to 1000h at 35°C			30		ppm
	Output voltage hysteresis	25°C, –40°C, 125°C, 25°C (cycle 1)			90		ppm
	Output voltage hysteresis	25°C, –40°C, 125°C, 25°C (cycle 2)			70		ppm
STABLE CAPACITANCE RANGE							
	Input capacitor range			0.1			µF
	Output capacitor range (3)			0.1		10	µF

(1) For V_{REF} = 1.2 V and 1.25 V, minimum V_{IN} = 1.7 V
(2) Scales linearly with V_{REF}.
(3) ESR for the capacitor <= 400 mΩ

7.6 Typical Characteristics

at T_A = 25°C, V_{IN} = V_{EN} = V_{REF} + 0.3 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

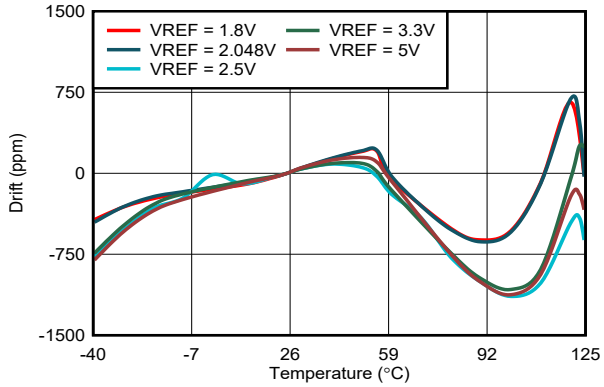


図 7-1. Output Voltage Drift vs Free-Air Temperature

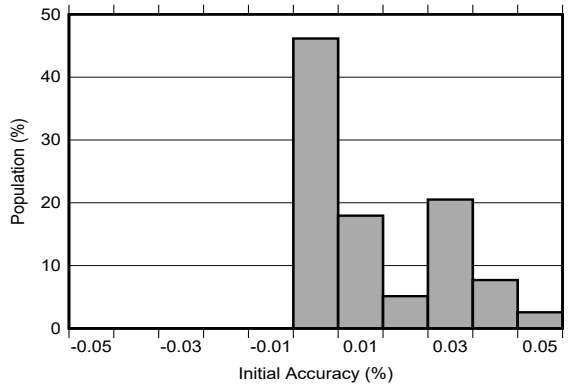


図 7-2. Initial Accuracy Distribution

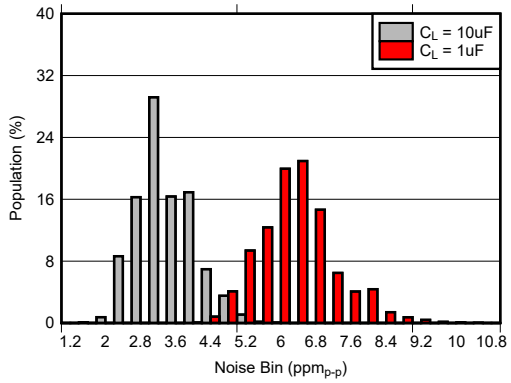


図 7-3. 0.1 Hz to 10 Hz Noise Distribution
(V_{REF} = 1.25 V, C_{NR} = Open, I_L = 0 mA)

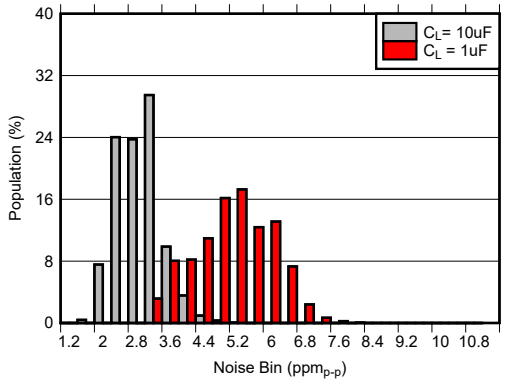


図 7-4. 0.1 Hz to 10 Hz Noise Distribution
(V_{REF} = 2.5 V, C_{NR} = Open, I_L = 0 mA)

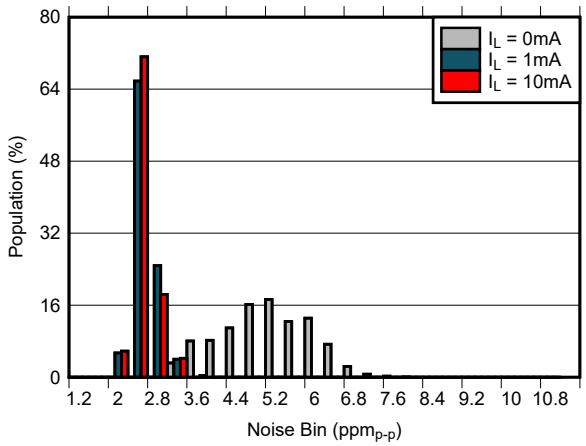


図 7-5. 0.1 Hz to 10 Hz Noise Distribution
(V_{REF} = 2.5 V, C_L = 1 µF, C_{NR} = Open)

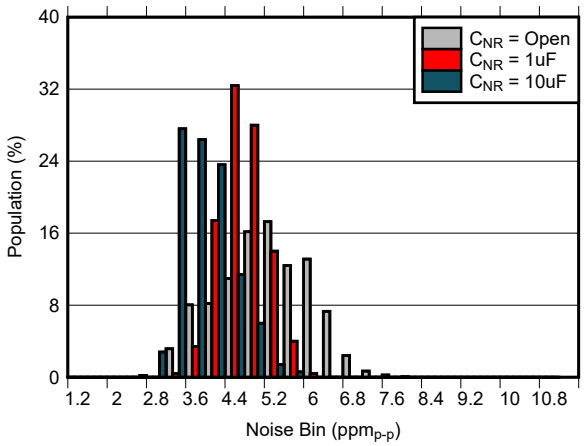


図 7-6. 0.1 Hz to 10 Hz Noise Distribution
(V_{REF} = 2.5 V, C_L = 1 µF, I_L = 0 mA)

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = V_{REF} + 0.3 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

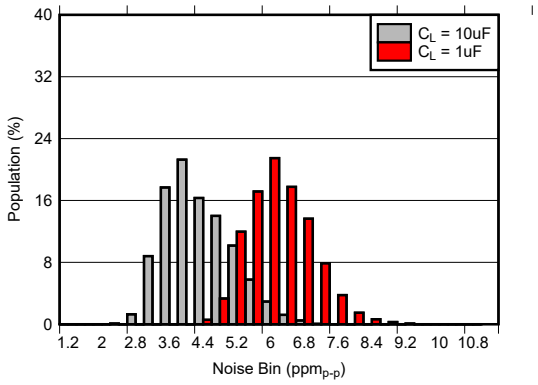


図 7-7. 0.1 Hz to 10 Hz Noise Distribution (V_{REF} = 5 V, C_{NR} = Open, I_L = 0 mA)

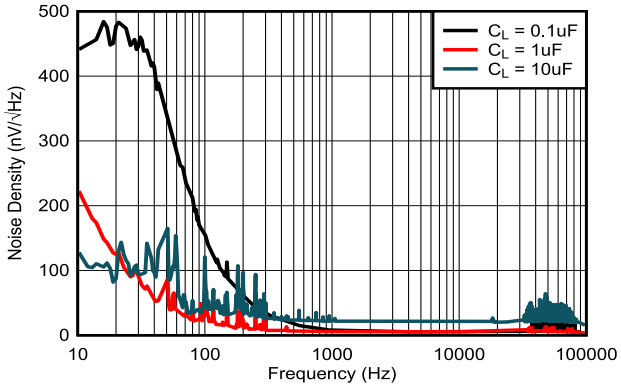


図 7-8. Noise Density vs Frequency (V_{REF} = 1.25 V, I_L = 0 mA)

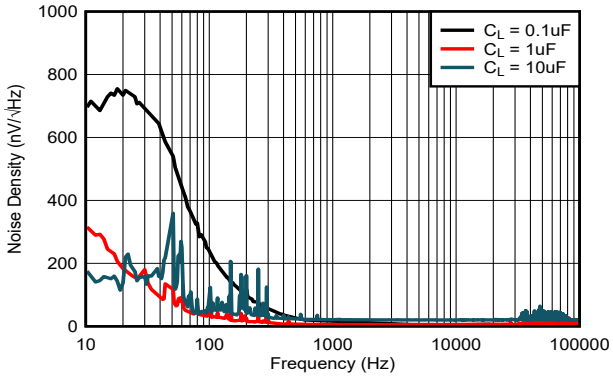


図 7-9. Noise Density vs Frequency (V_{REF} = 2.5 V, I_L = 0 mA)

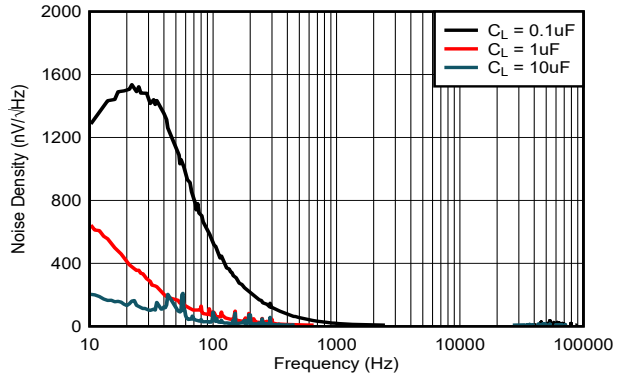


図 7-10. Noise Density vs Frequency (V_{REF} = 5 V, I_L = 0 mA)

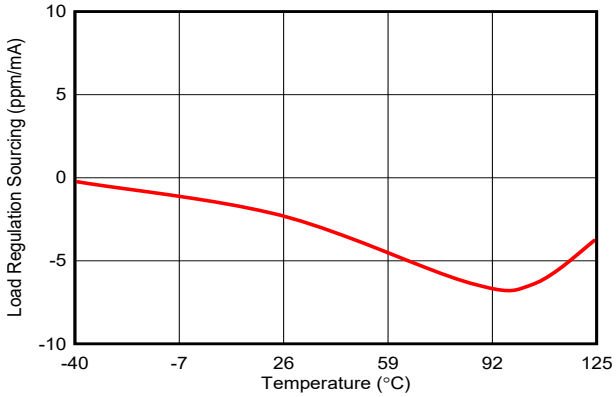


図 7-11. Load Regulation (Sourcing 10 mA) vs Free-Air Temperature

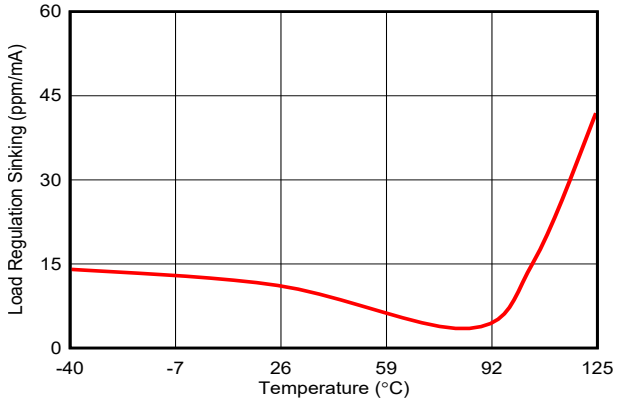


図 7-12. Load Regulation (Sinking 5 mA) vs Free-Air Temperature

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = V_{REF} + 0.3 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

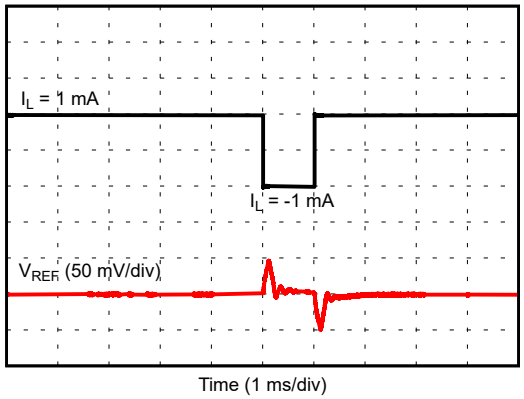


図 7-13. Load Transient Response (V_{REF} = 2.5 V, C_L = 10 µF)

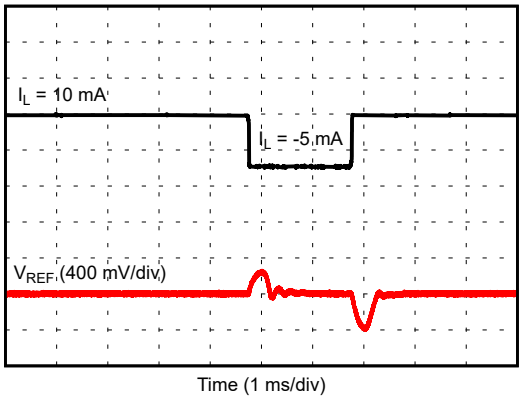


図 7-14. Load Transient Response (V_{REF} = 2.5 V, C_L = 10 µF)

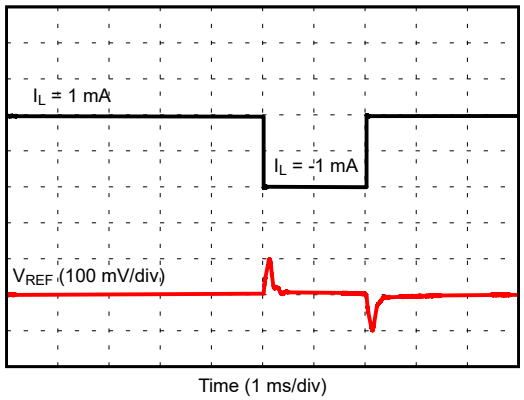


図 7-15. Load Transient Response (V_{REF} = 2.5 V, C_L = 1 µF)

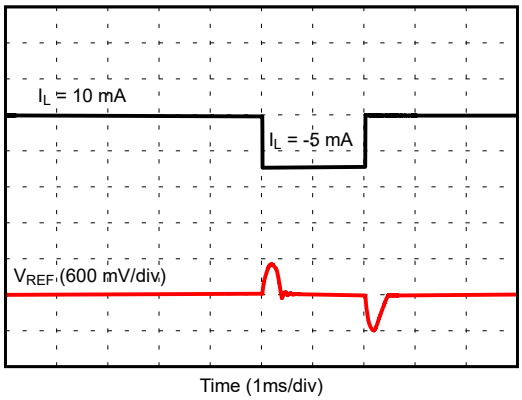


図 7-16. Load Transient Response (V_{REF} = 2.5 V, C_L = 1 µF)

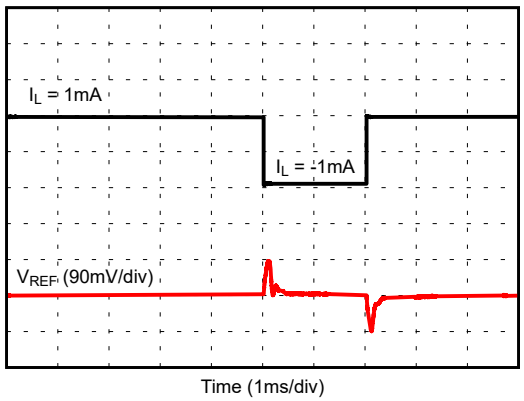


図 7-17. Load Transient Response (V_{REF} = 1.25 V, C_L = 1 µF)

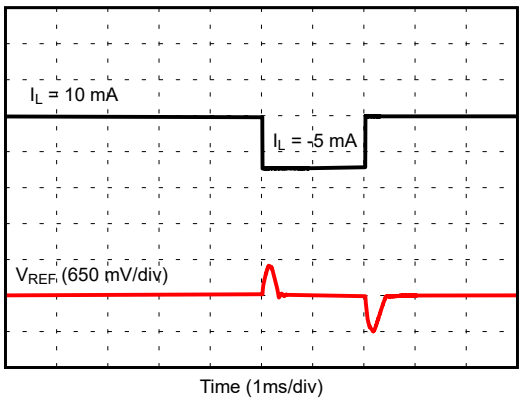


図 7-18. Load Transient Response (V_{REF} = 1.25 V, C_L = 1 µF)

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = V_{REF} + 0.3 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

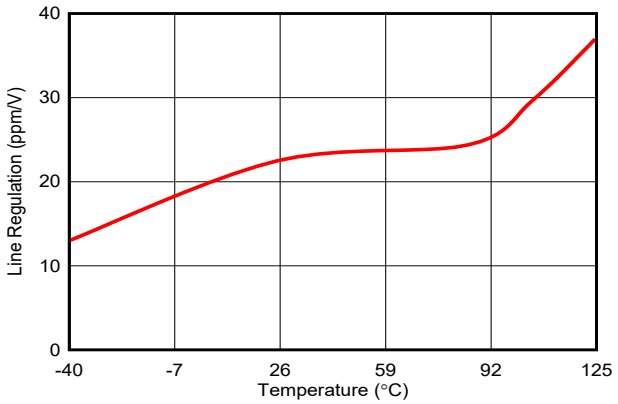


図 7-19. Line Regulation vs Free-Air Temperature

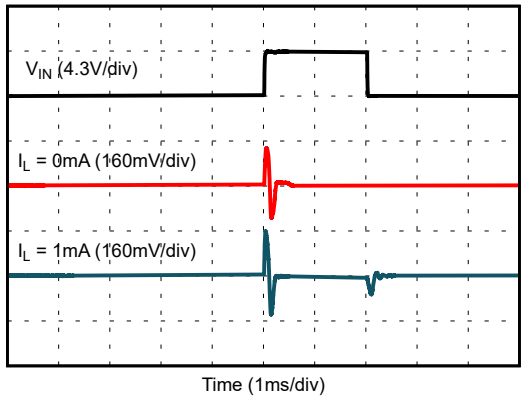


図 7-20. Line Transient Response (V_{REF} = 1.25 V, C_L = 1 µF)

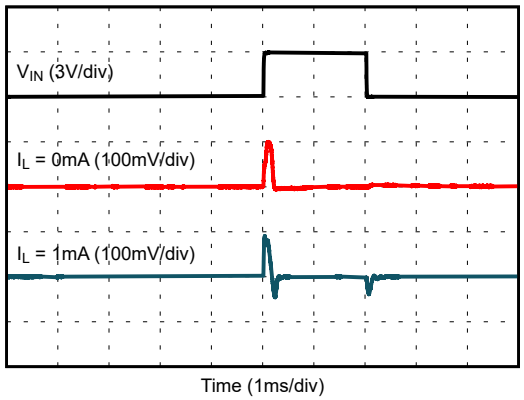


図 7-21. Line Transient Response (V_{REF} = 2.5 V, C_L = 1 µF)

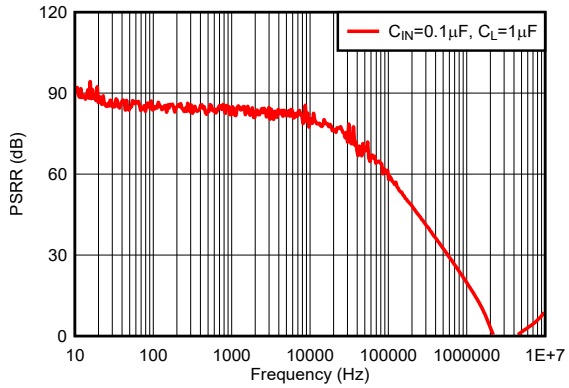


図 7-22. Power Supply Rejection Ratio (V_{REF} = 2.5 V, I_L = 0 mA)

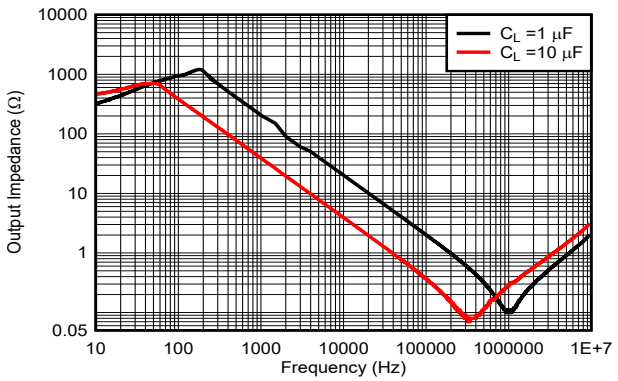


図 7-23. Output Impedance

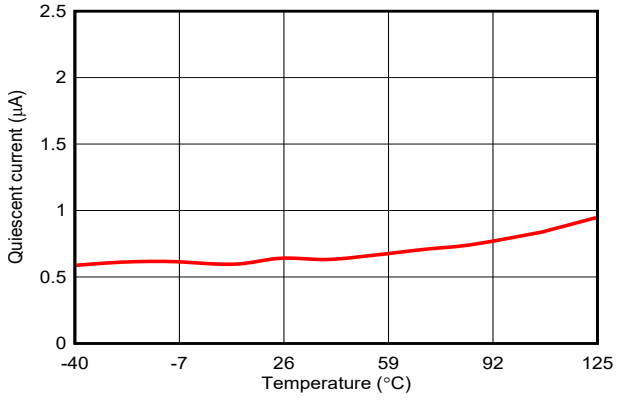


図 7-24. Quiescent Current vs Free-Air Temperature

7.6 Typical Characteristics (continued)

at T_A = 25°C, V_{IN} = V_{EN} = V_{REF} + 0.3 V, I_L = 0 mA, C_L = 10 µF, C_{IN} = 0.1 µF (unless otherwise noted)

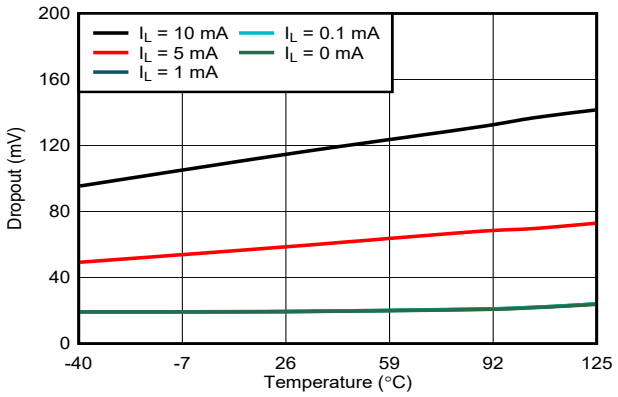


図 7-25. Dropout Voltage vs Free-Air Temperature

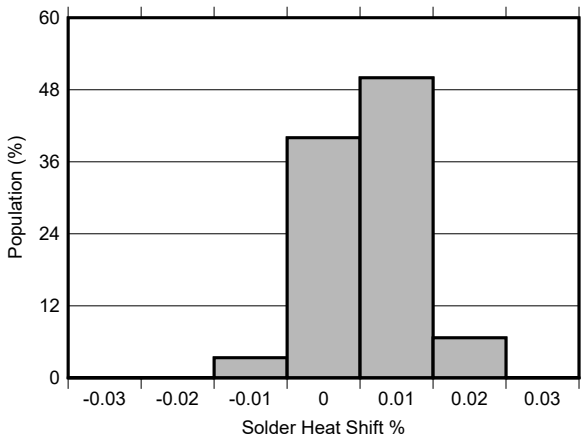


図 7-26. Solder Heat Shift Distribution

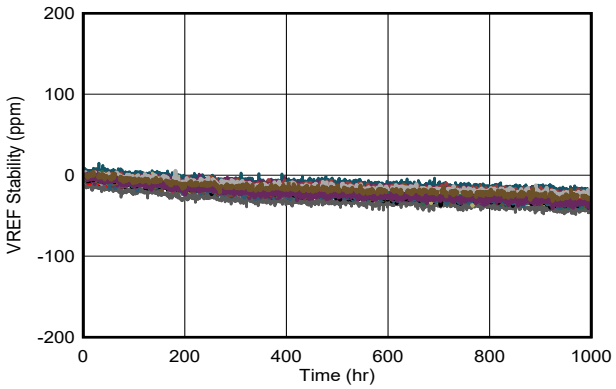


図 7-27. Long Term Stability - 1000 hours (V_{REF})

8 Parameter Measurement Information

8.1 Solder Heat Shift

The materials used in the manufacture of the REF35-Q1 have differing coefficients of thermal expansion, resulting in stress on the device die when the part is heated. Mechanical and thermal stress on the device die can cause the output voltages to shift, degrading the initial accuracy specifications of the product. Reflow soldering is a common cause of this error.

To illustrate this effect, a total of 32 devices were soldered on one printed circuit board using lead-free solder paste and the paste manufacturer suggested reflow profile. 図 8-1 shows the reflow profile. The printed circuit board is comprised of FR4 material. The board thickness is 1.66 mm and the area is 174 mm × 135 mm.

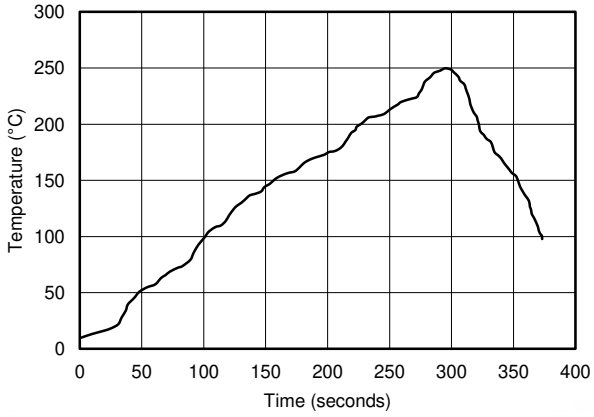


図 8-1. Reflow Profile

The reference output voltage is measured before and after the reflow process; 図 8-2 shows the typical shift. Although all tested units exhibit very low shifts (< 0.03%), higher shifts are also possible depending on the size, thickness, and material of the printed circuit board (PCB). An important note is that the histograms display the typical shift for exposure to a single reflow profile. Exposure to multiple reflows, as is common on PCBs with surface-mount components on both sides, causes additional shifts in the output bias voltage. If the PCB is exposed to multiple reflows, the device must be soldered in the last pass to minimize its exposure to thermal stress.

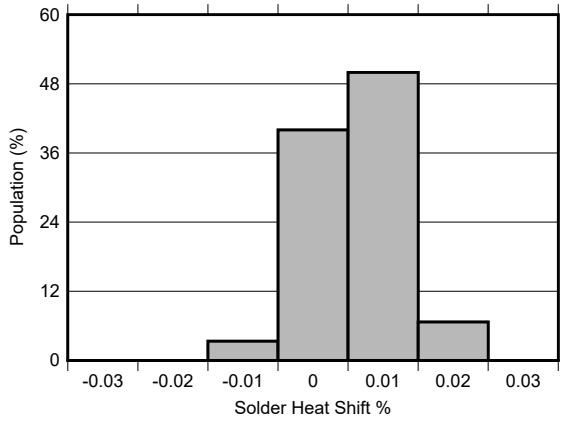


図 8-2. Solder Heat Shift Distribution, V_{REF} (%)

8.2 Temperature Coefficient

The REF35-Q1 is designed and tested for a low output voltage temperature coefficient, which is defined as the change in output voltage over temperature. The temperature coefficient is calculated using the box method in which a box is formed by the minimum/maximum limits for the nominal output voltage over the operating temperature range. REF35-Q1 has a low maximum temperature coefficient of 15 ppm/°C from –40°C to +125°C. The box method specifies limits for the temperature error but does not specify the exact shape and slope of the device under test. Due to temperature curvature correction to achieve low-temperature drift, the temperature drift is expected to be non-linear. See TI's Analog Design Journal, *Precision voltage references*, for more information on the box method. Use 式 1 for the box method.

$$\text{Drift} = \left(\frac{V_{REF(MAX)} - V_{REF(MIN)}}{V_{REF(25°C)} \times \text{Temperature Range}} \right) \times 10^6 \quad (1)$$

図 8-3 shows a typical voltage versus temperature curves for various reference voltages.

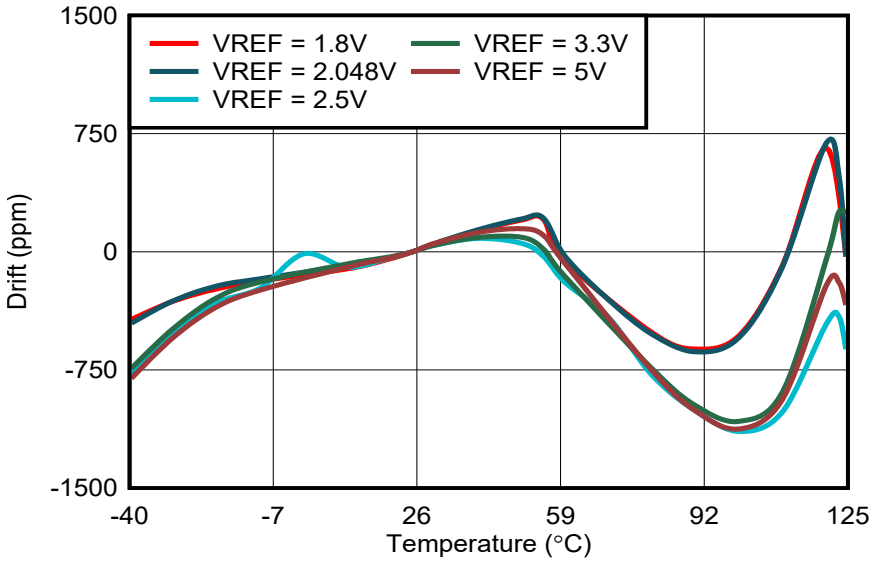


図 8-3. Output Voltage Drift Vs Free-Air Temperature

8.3 Long-Term Stability

One of the key performance parameters of the REF35-Q1 references is long-term stability also known as long-term drift. The long-term stability value is tested in a typical setup that reflects standard PCB board manufacturing practices. The boards are made of standard FR4 material and the board does not have special cuts or grooves around the devices to relieve the mechanical stress of the PCB. The devices and boards in this test do not undergo high temperature burn in post-soldering prior to testing. These conditions reflect a real world use case scenario and common manufacturing techniques.

During the long-term stability testing, precautions are taken to ensure that only the long-term stability drift is being measured. The boards are maintained at 35°C in an oil bath. The oil bath ensures that the temperature is constant across the device over time compared to an air oven. The measurements are captured every 30 minutes with a calibrated 8.5 digit multimeter.

The typical long-term stability characteristic is expressed as a deviation of the reference voltage output over time.

図 8-4 shows the typical drift value for the REF35-Q1 in 6-pin SOT-23 package is 30 ppm from 0 to 1000 hours. It is important to understand that long-term stability is not ensured by design and that the value is typical. The

REF35-Q1 will experience the highest drift in the initial 1000 hr. Subsequent deviation is typically lower than first 1000 hr.

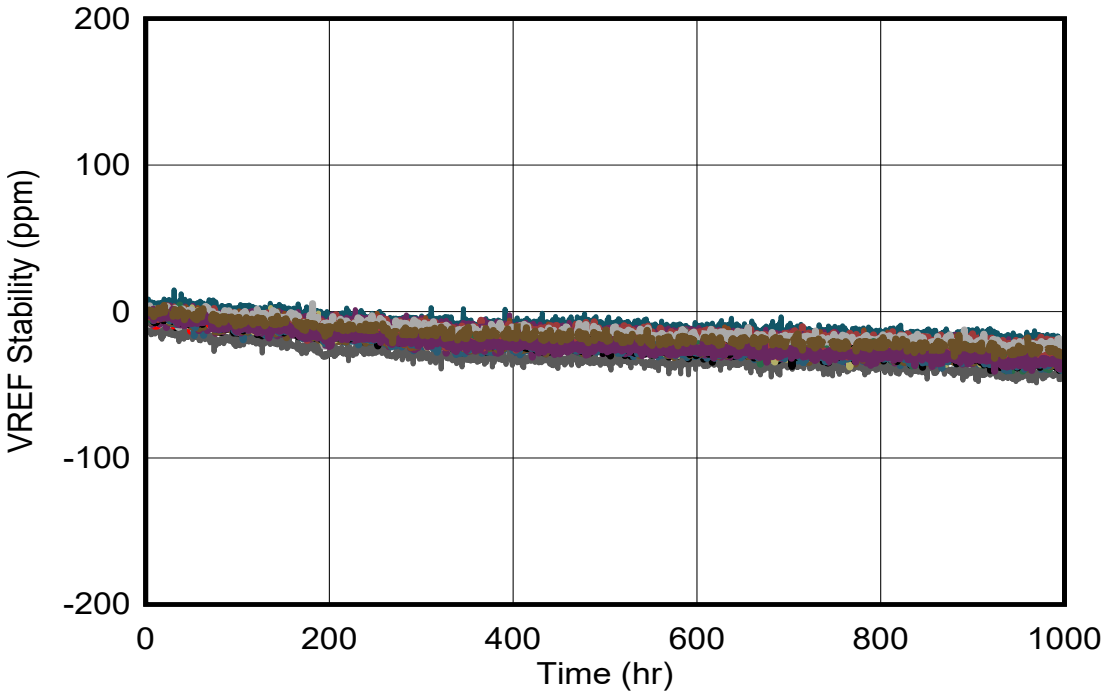


図 8-4. Long Term Stability - 1000 hours (V_{REF})

8.4 Thermal Hysteresis

Thermal hysteresis is measured with the REF35-Q1 soldered to a PCB, similar to a real-world application. Thermal hysteresis for the device is defined as the change in output voltage after operating the device at 25°C, cycling the device through the specified temperature range, and returning to 25°C. The PCB was baked at 150°C for 30 minutes before thermal hysteresis was measured. Use 式 2 to calculate the thermal hysteresis.

$$V_{HYST} = \left(\frac{| V_{PRE} - V_{POST} |}{V_{NOM}} \right) \times 10^6 \text{ (ppm)} \quad (2)$$

where

- V_{HYST} = thermal hysteresis (in units of ppm)
- V_{NOM} = the specified output voltage
- V_{PRE} = output voltage measured at 25°C pre-temperature cycling
- V_{POST} = output voltage measured after the device has cycled from 25°C through the specified temperature range of –40°C to +125°C and returns to 25°C.

図 8-5 and 図 8-6 show the typical thermal hysteresis distribution across various temperature ranges in two cycles.

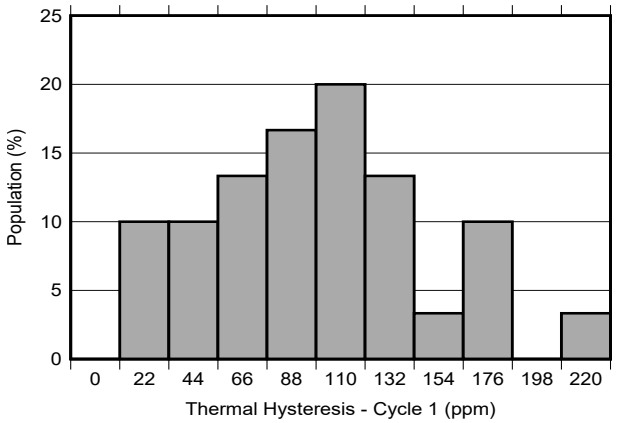


図 8-5. Thermal Hysteresis Distribution -40ºC to 125ºC, Cycle 1

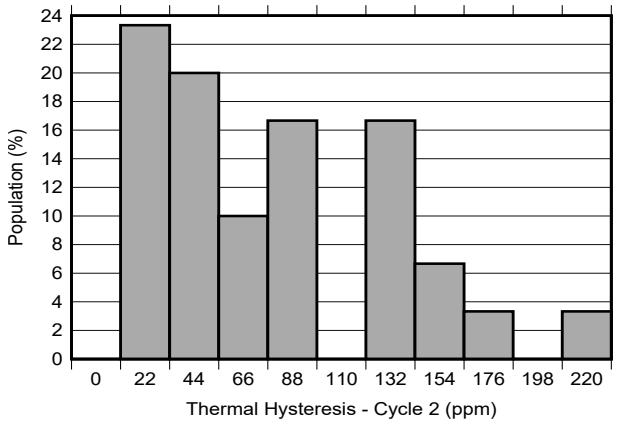


図 8-6. Thermal Hysteresis Distribution -40ºC to 125ºC, Cycle 2

8.5 Noise Performance

The reference pin output noise is categorized as low frequency and broadband noise. The following sections describe these categories in detail.

8.5.1 Low-Frequency (1/f) Noise

Flicker noise, also known as 1/f noise, is a low-frequency noise that affects the device output voltage which can affect precision measurements in ADCs. This noise increases proportionally with output voltage and operating temperature. The noise is measured by filtering the output from 0.1 Hz to 10 Hz. The 1/f noise is an extremely low value, therefore the frequency of interest must be amplified and band-pass filtered. This is done by using a high-pass filter to block the DC voltage. The resulting noise is then amplified by a gain of 1000. The bandpass filter is created by a series of high-pass and low-pass filter that adds additional gain to make it more visible on a oscilloscope as shown in 図 8-7. 図 8-8 shows the effect of flicker noise over 10 second. Flicker noise must be tested in a Faraday cage enclosure to block environmental noise.

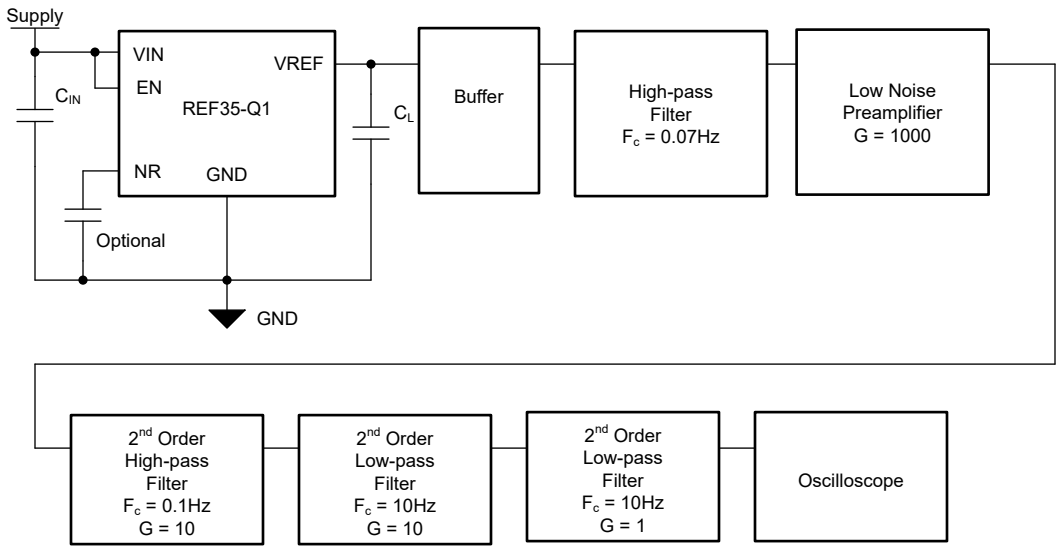


図 8-7. Low-Frequency (1/f) Noise Test Setup

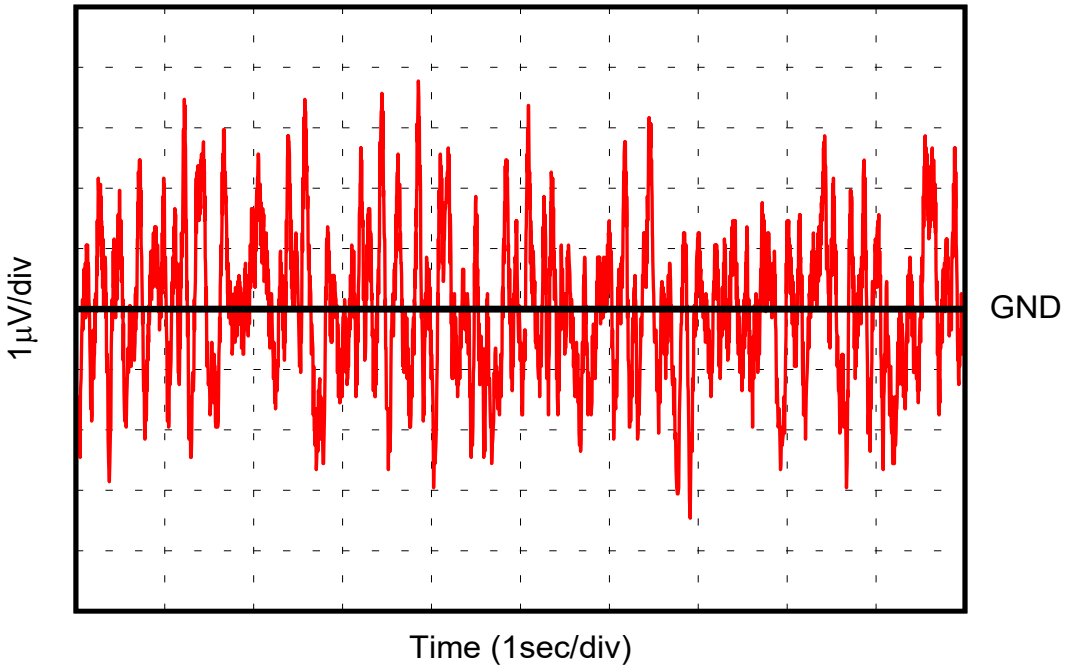


図 8-8. 0.1 Hz to 10 Hz Voltage Noise

図 8-9 shows the typical 1/f noise (0.1 Hz to 10 Hz) distribution across various load conditions. The REF35-Q1 device also offers noise reduction functionality by adding an optional capacitor between NR (pin 5) and ground pins.

図 8-10 shows the typical 1/f noise (0.1 Hz to 10 Hz) distribution across REF35-Q1 devices with various capacitance between NR pin and GND.

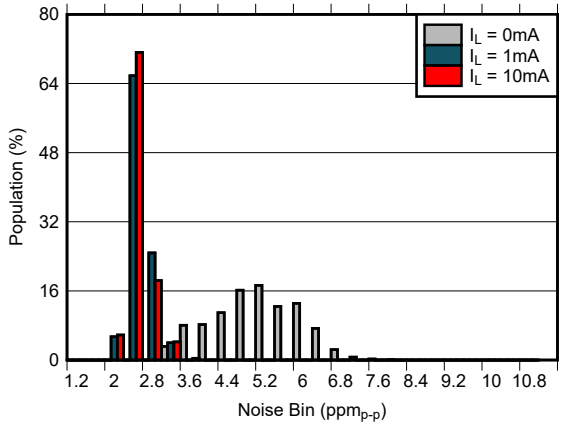


図 8-9. 0.1 Hz to 10 Hz Noise Distribution vs Load Conditions

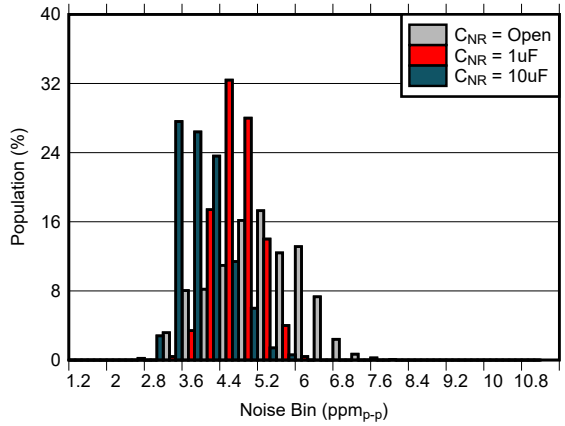


図 8-10. 0.1 Hz to 10 Hz Noise Distribution vs NR Capacitance

8.5.2 Broadband Noise

Broadband noise is a noise that appears at higher frequency compared to 1/f noise. The broadband noise is measured by high-pass filtering the output of the reference device, followed by a gain stage and measuring the result on a spectrum analyzer as shown in 図 8-11

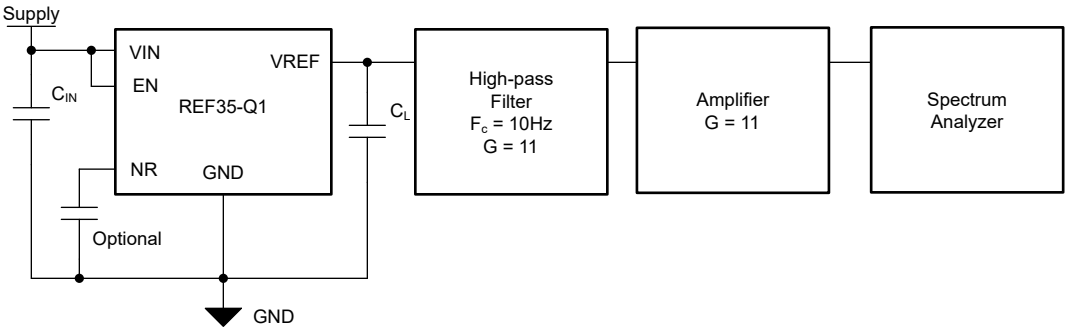


図 8-11. Broadband Noise Test Setup

For noise sensitive designs, a low-pass filter can be used to reduce broadband noise output noise levels by removing the high frequency components. When designing a low-pass filter, take special care to make sure the output impedance of the filter does not degrade AC performance. This can occur in RC low-pass filters where a large series resistance can impact the load transients due to output current fluctuations. The REF35-Q1 device also offers noise reduction functionality by adding an optional capacitor between NR (pin 5) and ground pins. 図 8-12 and 図 8-13 show the noise spectrum for REF35250 and REF35500 devices respectively across various NR pin capacitance.

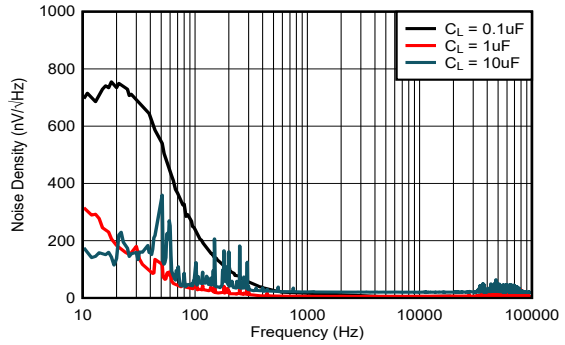


図 8-12. Noise Spectrum 10 Hz to 100 kHz (V_{REF} = 2.5 V)

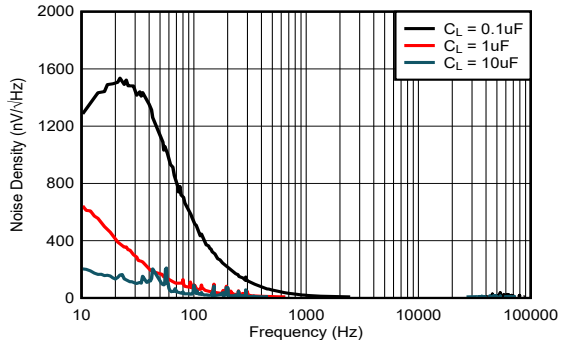


図 8-13. Noise Spectrum 10 Hz to 100 kHz (V_{REF} = 5 V)

8.6 Power Dissipation

The REF35-Q1 voltage references are capable of source up to 10 mA and sink up to 5 mA of load current across the rated input voltage range. However, when used in applications subject to high ambient temperatures, the input voltage and load current must be carefully monitored to ensure that the device does not exceeded its maximum power dissipation rating. The maximum power dissipation of the device can be calculated with 式 3:

$$T_J = T_A + P_D \times R_{\theta JA} \quad (3)$$

where

- P_D is the device power dissipation
- T_J is the device junction temperature
- T_A is the ambient temperature
- $R_{\theta JA}$ is the package (junction-to-air) thermal resistance

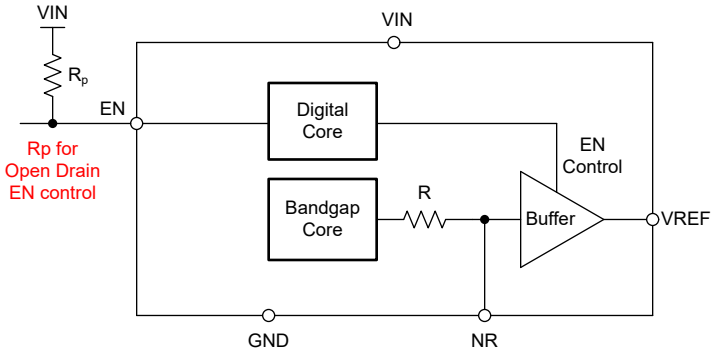
Because of this relationship, acceptable load current in high temperature conditions may be less than the maximum current-sourcing capability of the device. In no case should the device be operated outside of its maximum power rating because doing so can result in premature failure or permanent damage to the device.

9 Detailed Description

9.1 Overview

The REF35-Q1 is family of ultralow current, low-noise, precision band-gap voltage references that are specifically designed for excellent initial voltage accuracy and drift. The *Functional Block Diagram* is a simplified block diagram of the REF35-Q1 showing basic band-gap topology.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Supply Voltage

The REF35-Q1 family of references features an extremely low dropout voltage. For 10 mA loaded conditions, a maximum dropout voltage is 250 mV. 図 7-25 shows a typical dropout voltage (V_{DO}) versus load current. The device supports operation with input voltage range from V_{REF} + V_{DO} to 6 V. The typical quiescent current is 680 nA and maximum quiescent current over temperature is only 2.6 µA. The low dropout voltage coupled with ultralow current enable the operation across multiple battery powered applications.

9.3.2 EN Pin

The REF35-Q1 family supports device enable and disable functionality through logic level control on EN pin. The EN pin of REF35-Q1 does not use an internal pull-up resistor. Instead, the pin uses new 'clean EN' technology. This allows the EN pin to be in a no connect condition at start-up, and no extra current is drawn from the supply when the EN pin is pulled low in shutdown mode. When EN pin is pulled high or left unconnected, the device is in active mode. When EN pin is drive by an open-drain outputs, a pull-up resistor to VIN is required. The device must be in active mode for normal operation. The EN pin must not be pulled higher than VIN supply voltage.

The device can be placed in shutdown mode by pulling the EN pin low. When in shutdown mode, the output of the device becomes high impedance and the quiescent current of the device drops to 50 nA.

Also note that for applications where EN pin is no-connect, total parasitic capacitance on EN pin should be restricted within 30 pF.

See the セクション 7.5 for logic high and logic low voltage levels.

9.3.3 NR Pin

The REF35-Q1 pin allows access to the band gap through the NR pin. Placing a capacitor from the NR pin to GND creates a low-pass filter in combination with the internal resistance of 60 kΩ. Leakage of the capacitance directly impacts the accuracy and temperature drift. If NR functionality is used, choose a low leakage capacitor. A capacitance of 1 µF creates a low-pass filter with corner frequency around 2.7 Hz. Such a filter decreases the overall noise on the VREF pin. Higher capacitance results in a lower filter cut off frequency, further reducing output noise. Please note, using the capacitor on NR pin also increases start-up time.

9.4 Device Functional Modes

9.4.1 Basic Connections

図 9-1 shows the typical connections for the REF35-Q1. TI recommends a supply bypass capacitor (C_{IN}) ranging from 0.1 µF to 10 µF. A 0.1 µF to 10 µF output capacitor (C_L) must be connected from REF to GND. The equivalent series resistance (ESR) value of C_L must be lower than 400 mΩ to ensure output stability.

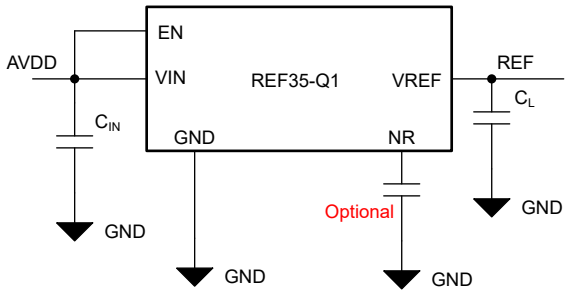


図 9-1. Basic Connections

9.4.2 Start-Up

図 9-2 shows the start-up behavior of REF35250 device with 1 µF load capacitance. REF35-Q1 device ensures the output voltage settles to the expected output voltage within specified accuracy without oscillations. The start-up time is dependent on the output voltage variant, output capacitance and NR pin capacitance. Higher capcitance leads to longer start-up time.

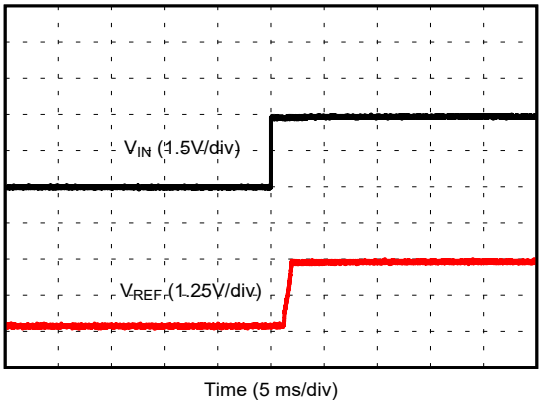


図 9-2. REF35250 Start-Up Behavior, C_L = 1 µF

9.4.3 Output Transient Behavior

The REF35-Q1 output buffer is capable of sourcing 10 mA load current as well as sink 5 mA of load current. The output stage is designed using class AB architecture with ultra-low quiescent current. This architecture avoids the dead zone around the no load condition. The output buffer uses a fast start-up implementation to achieve 2ms typical turn-on time at C_L = 1 µF and no-load current condition.

図 9-3 and 図 9-4 show the output settling behavior for light load transient and high load transient respectively.

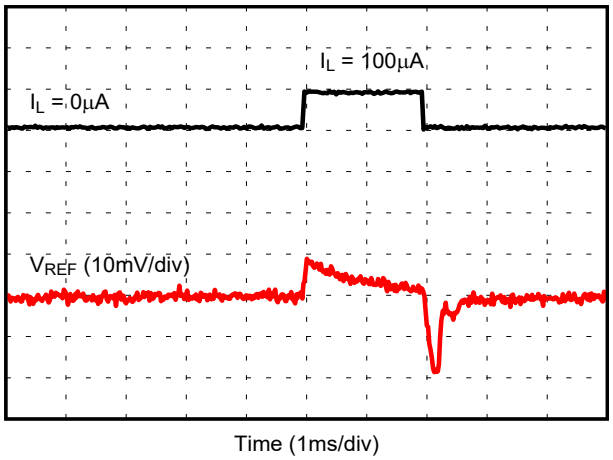


図 9-3. Load Transient Response 0 µA to 100 µA, C_{REF} = 1 µF

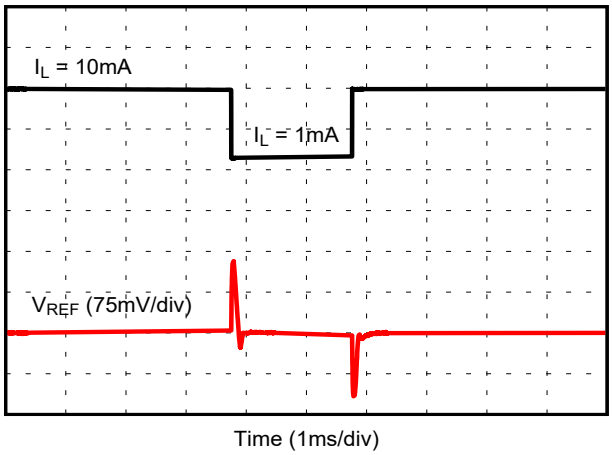


図 9-4. Load Transient Response 1 mA to 10 mA, C_{REF} = 1 µF

10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

REF35-Q1 with low current consumption and class leading performance specifcations is suitable reference for multiple applications. The device can also be used as a precision low noise power supply to sensor or data converter instead of traditional LDO or DC/DC based power supply. Basic applications includes positive/negative voltage reference and data acquisition.

10.2 Typical Application: Negative Reference Voltage

For applications requiring a negative and positive reference voltage, the REF35-Q1 and OPA188-Q1 can be used to provide a dual-supply reference from a 5 V supply. 図 10-1 shows the REF35250 used to provide a 2.5 V supply reference voltage. The low drift performance of the REF35250-Q1 complements the low offset voltage and low-drift of the OPA188-Q1 to provide an accurate solution for split-supply applications. Take care to match the temperature coefficients of R1 and R2.

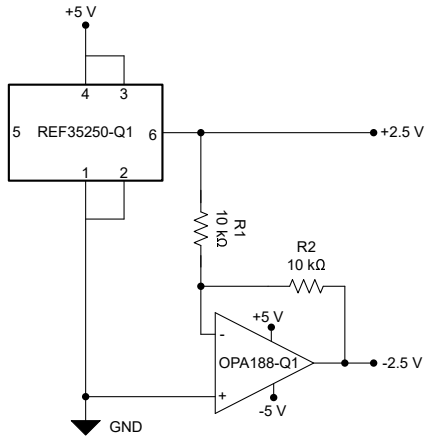


図 10-1. REF35-Q1 and OPA188-Q1 Create Positive and Negative Reference Voltages

10.3 Typical Application: Precision Power Supply and Reference

図 10-2 shows the basic configuration for the REF35-Q1 device as precision power supply to ADS7038-Q1 data converter which uses its power supply AVDD as reference. Connect bypass capacitors according to the guidelines in セクション 10.3.2.2 section.

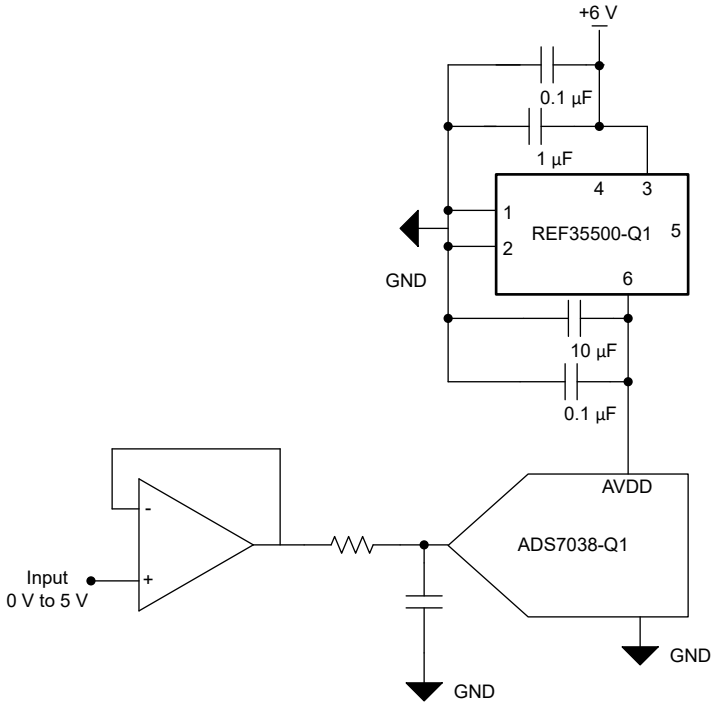


図 10-2. Basic Reference Connection

10.3.1 Design Requirements

A detailed design procedure is described based on a design example. For this design example, use the parameters listed in 表 10-1 as the input parameters.

表 10-1. Design Example Parameters

DESIGN PARAMETER	VALUE
Input voltage range V_{IN}	0 V - 5 V
Output resolution	12-bit
REF input capacitor	1 µF
REF output capacitor	10 µF

10.3.2 Detailed Design Procedure

10.3.2.1 Selection of Reference

The REF35500-Q1 reference is selected for this design. The REF35500-Q1 device operates of very low quiescent current while offering ±0.05 % initial accuracy and very low noise. These parameters help improve system accuracy as compared to external LDO based power supply. The 5 V reference voltage supports the 0 V to 5 V input range specification.

10.3.2.2 Input and Output Capacitors

A 1 µF to 10 µF electrolytic or ceramic capacitor can be connected to the input to improve transient response in applications where the supply voltage may fluctuate.

A ceramic capacitor of at least a 0.1 µF must be connected to the output to improve stability and help filter out high frequency noise. Add an additional 10 µF capacitor in parallel to improve transient performance in response to sudden changes in load current; however, keep in mind that doing so increases the start-up time of the device.

Best performance and stability is attained with low-ESR, low-inductance ceramic chip-type output capacitors (X5R, X7R, or similar). If using an electrolytic capacitor on the output, place a 0.1 µF ceramic capacitor in parallel to reduce overall ESR on the output. Place the input and output capacitors as close as possible to the device.

10.3.2.3 Selection of ADC

ADS7038-Q1 12-bit 8 channel multiplexed ADC is chosen for this application. The ADC offers low current operation with averaging mode to increase the resolution to 16-bit with internal averaging modes while operating with slow sampling speed.

10.3.3 Application Curves

表 10-2 shows the captured measurement results for various DC inputs. The ADC output is captured and analyzed for output accuracy, code spread and sigma with REF35500-Q1 as power supply vs LDO as power supply.

REF35-Q1 offers better accuracy and lower noise than the LDO device at lower quiescent current. This results in lower error in measurement as well as lower ADC output code variation across various OSR seetings.

表 10-2. DC Input Performance Test Results

INPUT V	ADC OSR SETTING	REF35500		LDO	
		ERROR	CODE SPREAD	ERROR	CODE SPREAD
1.0 V	0	0.01 mV	32 LSB	8.9 mV	48 LSB
	8	0.3 mV	10 LSB	9.21 mV	16 LSB
	128	0.38 mV	6 LSB	9.26 mV	6 LSB
2.5 V	0	0.69 mV	32 LSB	22.89 mV	64 LSB
	8	1.44 mV	10 LSB	23.63 mV	18 LSB
	128	1.17 mV	3 LSB	23.41 mV	5 LSB
4 V	0	2.27 mV	32 LSB	37.84 mV	48 LSB
	8	3.01 mV	24 LSB	38.62 mV	24 LSB
	128	2.46 mV	3 LSB	38.09 mV	17 LSB

10.4 Power Supply Recommendations

The REF35 family of references feature an extremely low-dropout voltage. These references can be operated with a supply of only 50 mV above the output voltage at no load. TI recommends a supply bypass capacitor ranging between 0.1 µF to 10 µF.

10.5 Layout

10.5.1 Layout Guidelines

図 10-3 shows an example of a PCB layout for a data acquisition system using the REF35-Q1. Some key considerations are:

- Connect low-ESR, 0.1 µF ceramic bypass capacitors at V_{IN}, V_{REF} of the REF35-Q1.
- Decouple other active devices in the system per the device specifications.
- Using a solid ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup.
- Place the external components as close to the device as possible.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when absolutely necessary.

図 10-4 shows the pin compatibility with TI REF31xx series reference in the 3-pin SOT-23 package when using the REF35xxx family footprint. You must rotate the REF31xx reference device by 180º before assembly.

10.5.2 Layout Examples

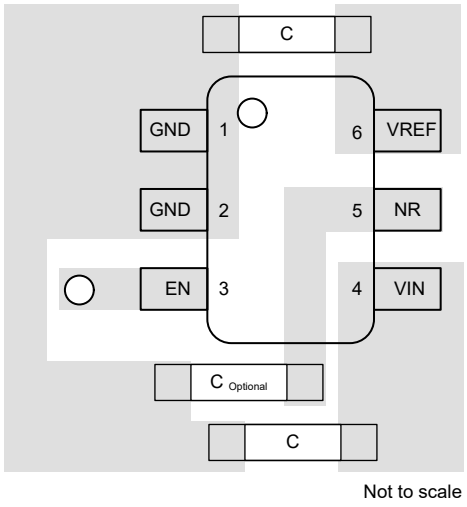


図 10-3. Layout Example

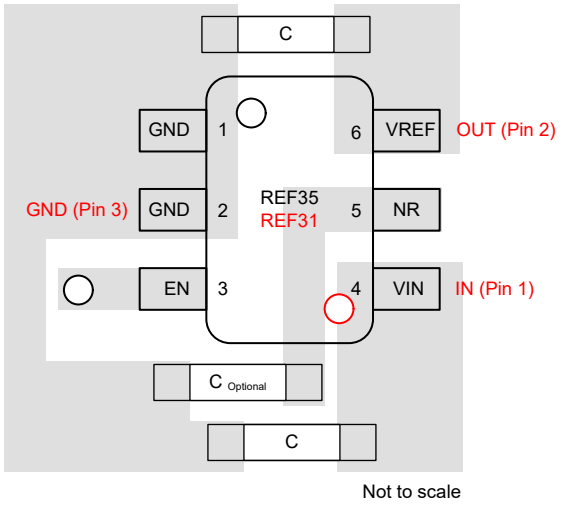


図 10-4. Pin Compatibility With REF31xx

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *INA21x Voltage Output, Low- or High-Side Measurement, Bidirectional, Zero-Drift Series, Current-Shunt Monitors*
- *Low-Drift Bidirectional Single-Supply Low-Side Current Sensing Reference Design*

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 サポート・リソース

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11.4 Trademarks

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11.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
REF35180QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	34AI	Samples
REF35300QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	34DI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF REF35-Q1 :

- Catalog : REF35

NOTE: Qualified Version Definitions:

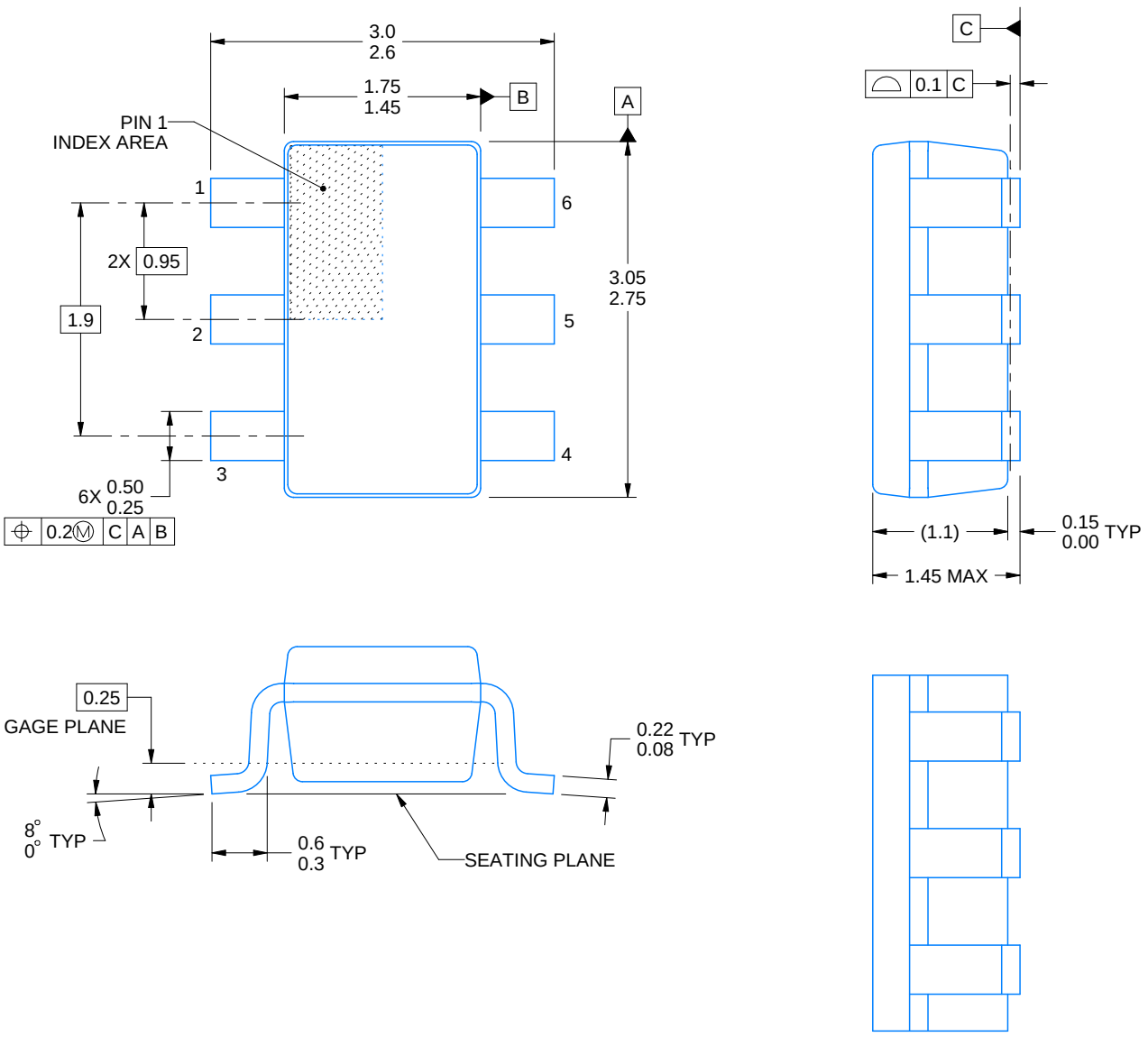
- Catalog - TI's standard catalog product

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



ALTERNATIVE PACKAGE SINGULATION VIEW

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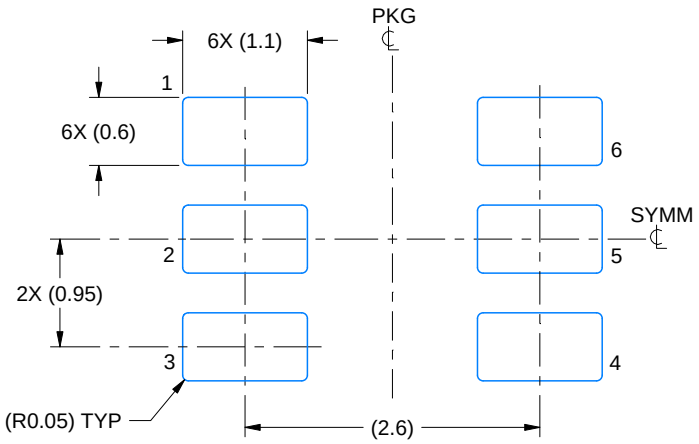
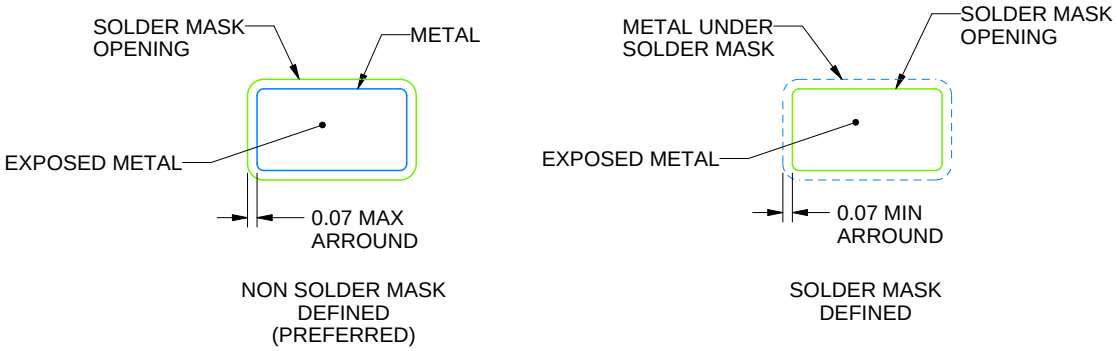
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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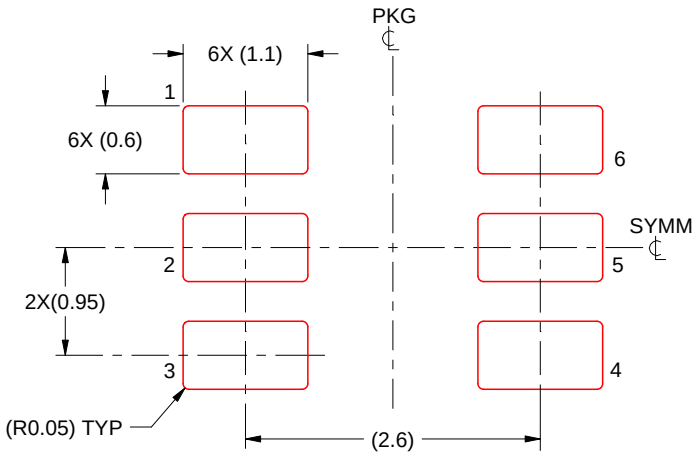
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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