TEXAS INSTRUMENTS
SN65HVD3080E, SN65HVD3083E, SN65HVD3086E
JAJSPZ4F – NOVEMBER 2006 – REVISED MARCH 2023

SN65HVD308xE 低消費電力 RS-485 全二重ドライバおよびレシーバ

1 特長

- 低静止時電力
  - 375µA (標準値) のイネーブル・モード
  - 2nA (標準値) のシャットダウン・モード
- 小型 MSOP パッケージ
- 1/8 ユニット負荷 (バスごとに最大 256 ノード)
- 16kV バス・ピンは ESD 保護、すべてのピンは 6kV
- フェイル・セーフ・レシーバ (バス開放、短絡、アイドル)
- TIA/EIA-485A 標準に準拠
- RS-422 互換
- グリッチのない電源オン、電源オフ動作

2 アプリケーション

- モーション・コントローラ
- POS 端末
- ラック・ツー・ラック通信
- 産業用ネットワーク
- 電力インバータ
- バッテリ駆動のアプリケーション
- ビル・オートメーション

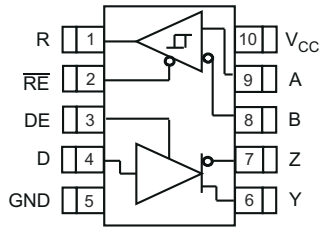
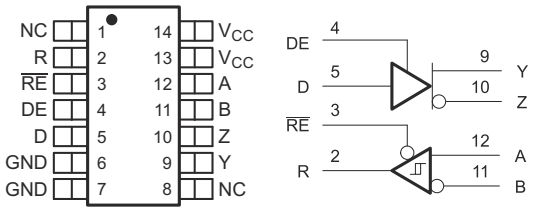


図 2-1. DGS パッケージ (上面図)



NC - No internal connection
Pins 6 and 7 are connected together internally
Pins 13 and 14 are connected together internally

図 2-2. D パッケージ (上面図)

3 概要

これらの各デバイスは、全二重 RS-485 または RS-422 データ・バス・ネットワーク用に設計された平衡型ドライバおよびレシーバです。5V の電源供給により、TIA/EIA-485A 標準に完全準拠しています。

これらのデバイスは、バス出力遷移時間が制御されており、200kbps～20Mbps の信号速度に適しています。

これらのデバイスは、1mA 未満 (標準値、負荷を除く) の非常に小さな電源電流で動作するよう設計されています。非アクティブなシャットダウン・モードでは電源電流は数ナノアンペアまで低下するため、これらのデバイスは消費電力の制約が厳しいアプリケーションに適しています。

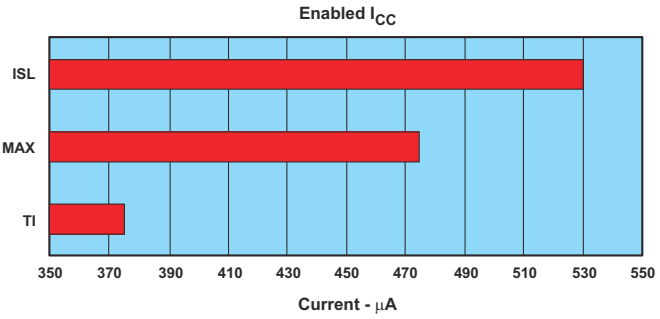
これらのデバイスは幅広い同相モード範囲と高 ESD 保護レベルを備えているため、モーション・コントローラ、電気インバータ、産業用ネットワーク、ノイズ耐性が重要となるケーブル接続シャーシの相互接続などの要求の厳しいアプリケーションに適しています。

これらのデバイスは、-40℃～85℃の温度範囲で動作するように規定されています

製品情報

部品番号	信号速度	パッケージ (1)
SN65HVD3080E	200kbps	DGS、DGSR 10 ピン MSOP (2)
SN65HVD3083E	1Mbps	
SN65HVD3086E	20Mbps	D 14 ピン SOIC

(1) 最新のパッケージ情報と発注情報については、このデータシートの末尾にある「付録:パッケージ・オプション」を参照するか、テキサス・インスツルメンツの Web サイト www.ti.com または www.tij.co.jp を参照してください。
(2) R の接尾辞は、テープ・アンド・リールを示しています。



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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision E (November 2012) to Revision F (March 2023) — **Page**

- 「注文情報」表を削除 ... 1
- 「製品情報」の表を追加 ... 1
- Added the *Thermal Information* table ... 4
- Changed the *Typical Characteristics* ... 7

Changes from Revision D (January 2011) to Revision E (November 2012) — **Page**

- 「特長」にグリッチのない電源オン、電源オフ動作を追加 ... 1
- Changed ENABLE in DRIVER FUNCTION TABLE from L to L or OPEN ... 11
- Changed ENABLE in RECEIVER FUNCTION TABLE from H to H or OPEN ... 11
- Added *Application Information* section ... 13

Changes from Revision C (December 2009) to Revision D (January 2011) — **Page**

- Added Differential input voltage dynamic to RECOMMENDED OPERATING CONDITIONS ... 4
- Added 図 7-1 ... 11

Changes from Revision B (March 2007) to Revision C () — **Page**

- D パッケージを追加 ... 1
- Added D package information to Power Dissipation Ratings ... 3
- Changed Electrostatic Discharge Protection ... 3
- Changed Supply Current information ... 4
- Changed Receiver Switching Characteristics ... 6
- Changed 図 6-5 ... 8
- Changed 図 6-6 ... 8

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted(1)

		UNIT
V_{CC}	Supply voltage range(2)	–0.3 V to 7 V
$V_{(A)}$, $V_{(B)}$, $V_{(Y)}$, $V_{(Z)}$	Voltage range at any bus terminal (A, B, Y, Z)	–9 V to 14 V
$V_{(TRANS)}$	Voltage input, transient pulse through 100 Ω. See 図 6-10 (A, B, Y, Z)	–50 to 50 V
V_I	Input voltage range (D, DE, $\overline{RE}$)	-0.3 V to V_{CC}+0.3 V
P_D	Continuous total power dissipation	See the dissipation rating table
T_J	Junction temperature	170°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

5.2 Power Dissipation Ratings

PACKAGE	T_A < 25°C	DERATING FACTOR(1) ABOVE T_A < 25°C	T_A = 85°C
10-pin MSOP (DGS)	463 mW	3.71 mW/°C	241 mW
14-pin SOIC (D)	765 mW	6.1 mW/°C	400 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

5.3 Electrostatic Discharge Protection

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Human Body Model(1)	A,B,Y,Z, and GND		16		kV
	All pins		6		kV
Charged Device Mode(2)	All pins		1.5		kV
Machine Model(3)	All pins		400		V

(1) Tested in accordance JEDEC Standard 22, Test Method A114-A. Bus pin stressed with respect to a common connection of GND and V_{CC}.
(2) Tested in accordance JEDEC Standard 22, Test Method C101.
(3) Tested in accordance JEDEC Standard 22, Test Method A115.

5.4 Supply Current

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply current	$\overline{RE}$ at 0 V, D and DE at V_{CC}, No load	Receiver enabled, Driver enabled		375	750	µA
		$\overline{RE}$ at 0 V, D and DE at 0 V, No load	Receiver enabled, Driver disabled		300	680	µA
		$\overline{RE}$ at V_{CC}, D and DE at V_{CC}, No load	Receiver disabled, Driver enabled		240	600	µA
		$\overline{RE}$ and D at V_{CC}, DE at 0 V, No load	Receiver disabled, Driver disabled		2	1000	nA

5.5 Recommended Operating Conditions

over operating free-air temperature range unless otherwise noted

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.5	5	5.5	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–7(1)		12	
V_{IH}	High-level input voltage	D, DE, $\overline{RE}$	2		V_{CC}	V
V_{IL}	Low-level input voltage	D, DE, $\overline{RE}$	0		0.8	
V_{ID}	Differential input voltage		–12		12	V
		Dynamic, See 図 7-1				V
I_{OH}	High-level output current	Driver	–60			mA
		Receiver	–10			
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			10	
T_J	Junction temperature				150	°C
T_A	Ambient still-air temperature		–40		85	

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.

5.6 Thermal Information

THERMAL METRIC(1)		D (SOIC) 14 PINS	DGS (VSSOP) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	93.2	75.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	47.5	22.0	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.4	44.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	11.2	1.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	48.9	44.3	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

5.7 Driver Electrical Characteristics

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$\|V_{OD}\|$	Differential output voltage	No load, I_O = 0	3	4.3	V_{CC}	V
		R_L = 54 Ω, See 図 6-1	1.5	2.3		
		V_{test} = –7 V to 12 V, See 図 6-2	1.5			
		R_L = 100 Ω, See 図 6-1	2			
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage	R_L = 54 Ω, See 図 6-1 and 図 6-2	–0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See 図 6-3	1	2.6	3	V
$\Delta V_{OC(SS)}$	Common-mode output voltage (Dominant)		-0.1	0	0.1	
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage			0.5		
$I_{Z(Y)}$ or $I_{Z(Z)}$	High-impedance state output current	V_{CC} = 0 V, $V_{(Z)}$ or $V_{(Y)}$ = 12 V Other input at 0 V			1	μA
		V_{CC} = 0 V, $V_{(Z)}$ or $V_{(Y)}$ = -7 V Other input at 0 V	-1			
		V_{CC} = 5 V, $V_{(Z)}$ or $V_{(Y)}$ = 12 V Other input at 0 V			1	
		V_{CC} = 5 V, $V_{(Z)}$ or $V_{(Y)}$ = -7 V Other input at 0 V	-1			
I_I	Input current	D, DE	-100		100	μA
I_{OS}	Short-circuit output current	–7 V ≤ V_O ≤ 12 V	-250		250	mA

5.8 Driver Switching Characteristics

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}, t_{PHL}	Propagation delay time, low-to-high-level output Propagation delay time, high-to-low-level output	HVD3080E	R_L = 54 Ω, C_L = 50 pF, See 図 6-4		0.7	1.3	μs
		HVD3083E			150	500	ns
		HVD3086E			12	20	ns
t_r, t_f	Differential output signal rise time Differential output signal fall time	HVD3080E		0.5	0.9	1.5	μs
		HVD3083E			200	300	ns
		HVD3086E			7	15	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} - t_{PLH}\|$)	HVD3080E			20	200	ns
		HVD3083E			5	50	ns
		HVD3086E			1.4	5	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	HVD3080E	R_L = 110 Ω, $\overline{RE}$ at 0 V, See 図 6-5		2.5	7	μs
		HVD3083E			1	2.5	μs
		HVD3086E			13	30	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	HVD3080E			80	200	ns
		HVD3083E			60	100	ns
		HVD3086E			12	30	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	HVD3080E	R_L = 110 Ω, $\overline{RE}$ at 0 V, See 図 6-6		2.5	7	μs
		HVD3083E			1	2.5	μs
		HVD3086E			13	30	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	HVD3080E			80	200	ns
		HVD3083E			60	100	ns
		HVD3086E			12	30	ns
t_{PZH}	Propagation delay time, standby-to-high-level output (See 図 6-5)		R_L = 110 Ω, $\overline{RE}$ at 3 V		3.5	7	μs
t_{PZL}	Propagation delay time, standby-to-low-level output (See 図 6-6)						

5.9 Receiver Electrical Characteristics

over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
V_{IT+}	Positive-going differential input threshold voltage		I_O = –10 mA		-0.08	–0.01	V
V_{IT-}	Negative-going differential input threshold voltage		I_O = 10 mA	–0.2	-0.1		
V_{hys}	Hysteresis voltage (V_{IT+} - V_{IT-})				30		mV
V_{OH}	High-level output voltage		V_{ID} = 200 mV, I_{OH} = –10 mA, See 図 6-7 and 図 6-8	4	4.6		V
V_{OL}	Low-level output voltage		V_{ID} = –200 mV, I_{OH} = 10 mA, See 図 6-7 and 図 6-8		0.15	0.4	V
I_{OZ}	High-impedance-state output current		V_O = 0 or V_{CC}	–1		1	µA
I_I	Bus input current	Other input at 0V	V_A or V_B = 12 V		0.04	0.11	mA
			V_A or V_B = 12 V, V_{CC} = 0 V		0.06	0.13	
			V_A or V_B = -7 V	–0.1	–0.04		
			V_A or V_B = -7 V, V_{CC} = 0 V	–0.05	–0.03		
I_{IH}	High-level input current		V_{IH} = 2 V	–60	-30		µA
I_{IL}	Low-level input current		V_{IL} = 0.8 V	-60	-30		µA
C_{ID}	Differential input capacitance		V_I = 0.4 sin (4E6πt) + 0.5 V		7		pF

(1) All typical values are at 25°C and with a 3.3-V supply.

5.10 Receiver Switching Characteristics

over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	V_{ID} = -1.5 V to 1.5 V, C_L = 15 pF, See 図 6-8			75	100	ns
t_{PHL}	Propagation delay time, high-to-low-level output				79	100	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} - t_{PLH} \rvert$)				4	10	
t_r	Output signal rise time				1.5	3	
t_f	Output signal fall time				1.8	3	
t_{PZH}, t_{PZL}	Output enable time		DE at V_{CC}, See 図 6-9		10	50	ns
		From standby	DE at GND, See 図 6-9		1.7	3.5	µs
t_{PHZ}, t_{PLZ}	Output disable time	DE at GND or V_{CC}, See 図 6-9			7	50	ns

5.11 Typical Characteristics

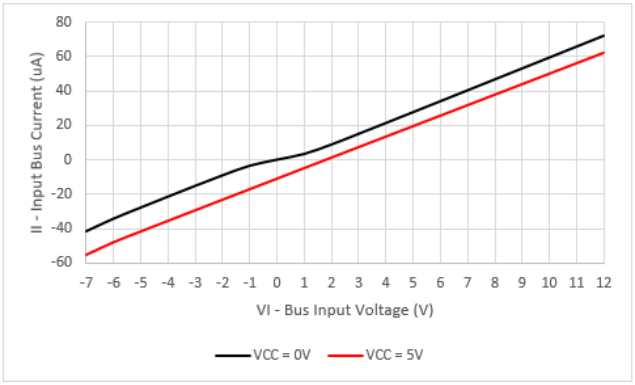


図 5-1. Input Bias Current vs BUS Input Voltage

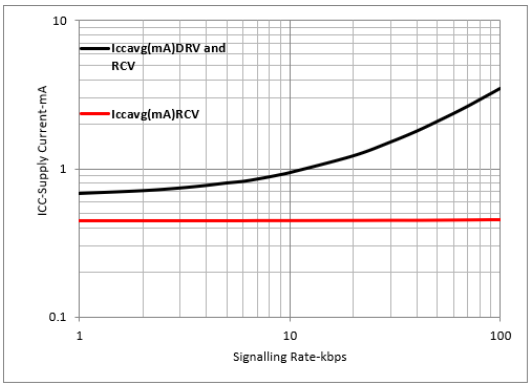


図 5-2. HVD3080E Supply Current vs Signaling Rate

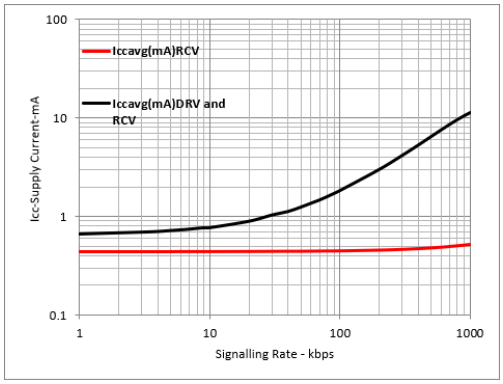


図 5-3. HVD3083E Supply Current vs Signaling Rate

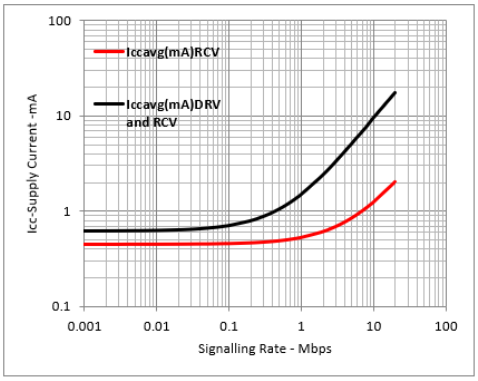


図 5-4. HVD3086E Supply Current vs Signaling Rate

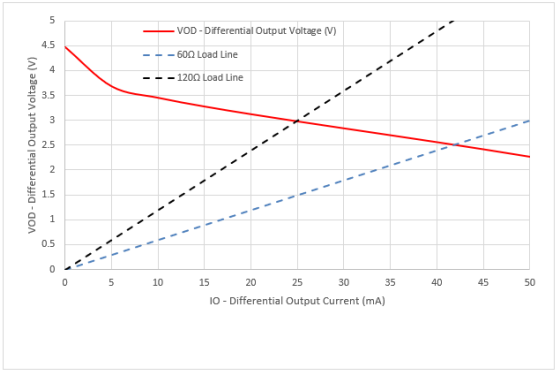


図 5-5. Differential Output Voltage vs Differential Output Current

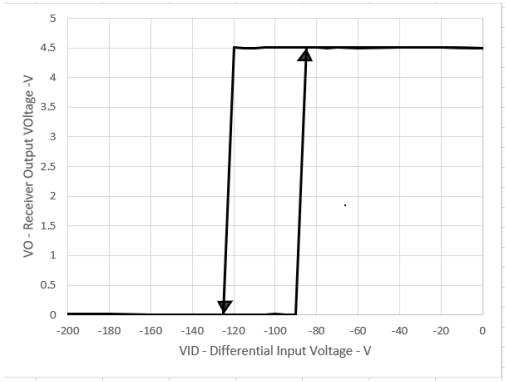


図 5-6. Receiver Output Voltage vs Differential Input Voltage

6 Parameter Measurement Information

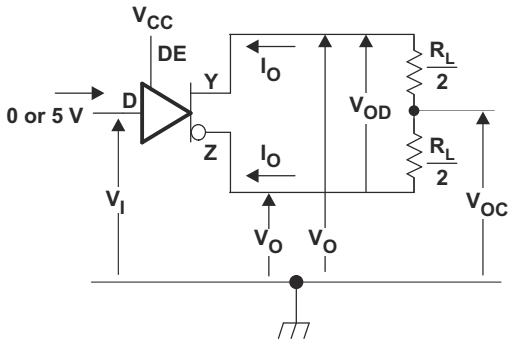


図 6-1. Driver V_{OD} Test Circuit and Current Definitions

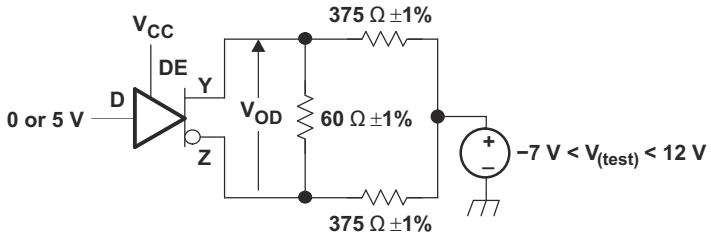


図 6-2. Driver V_{OD} With Common-Mode Loading Test Circuit

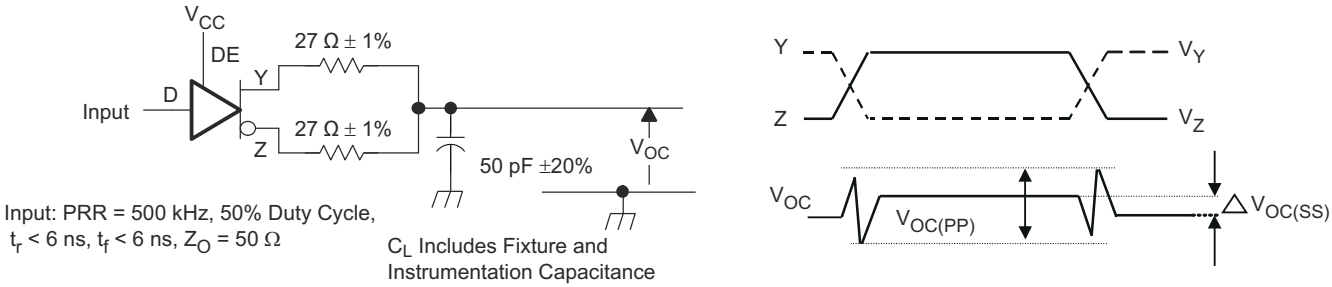


図 6-3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage

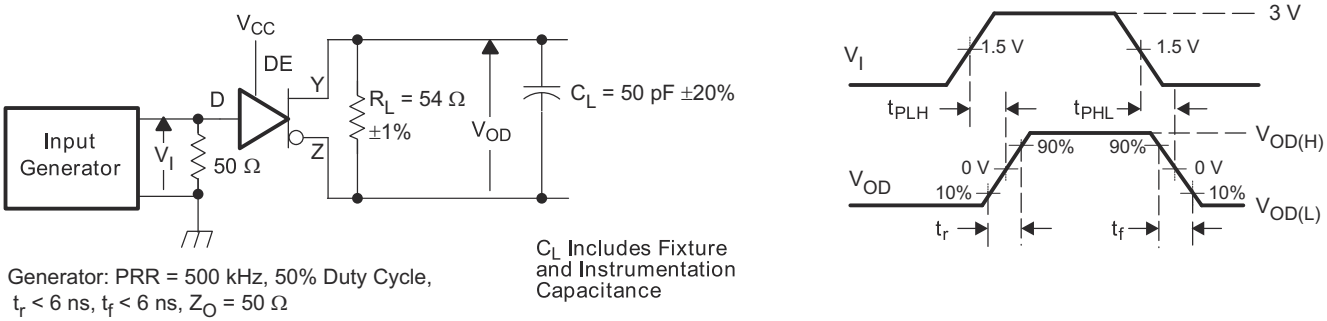


図 6-4. Driver Switching Test Circuit and Voltage Waveforms

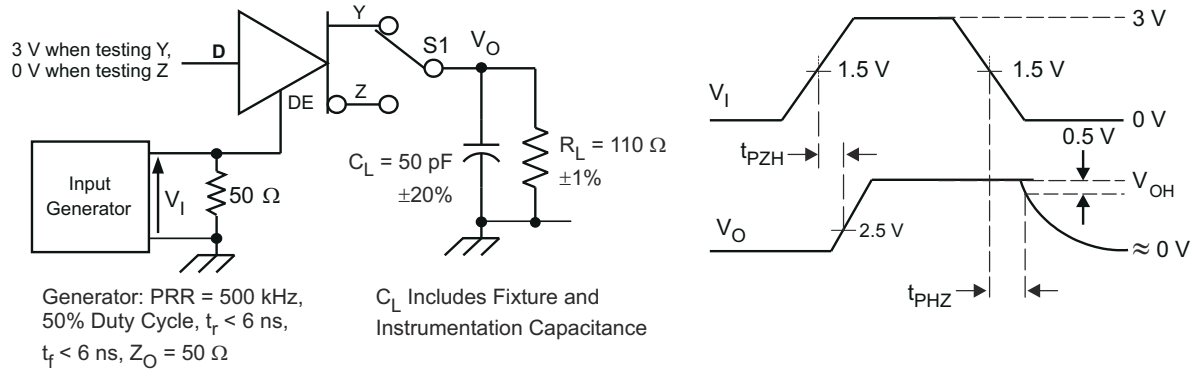


図 6-5. Driver High-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

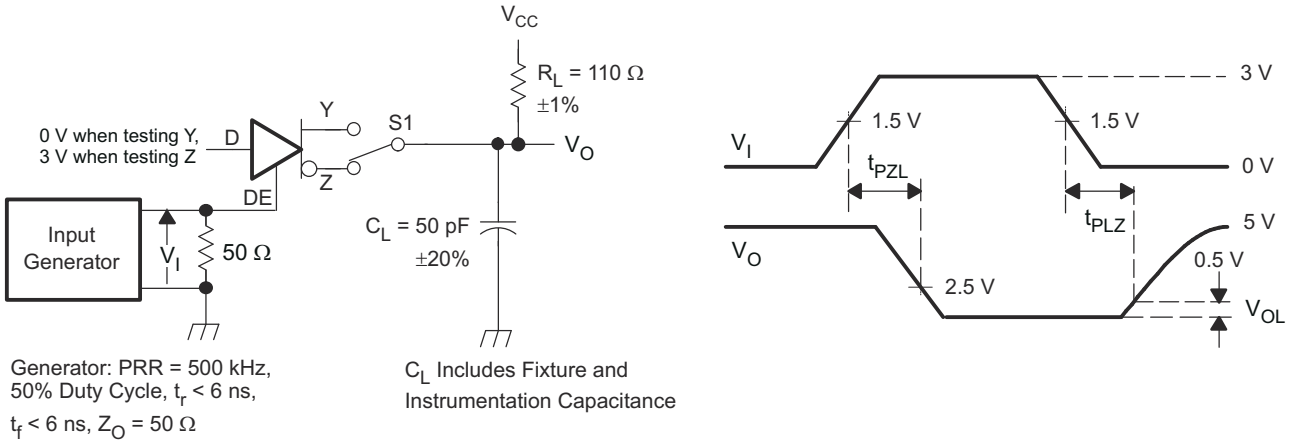


図 6-6. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms

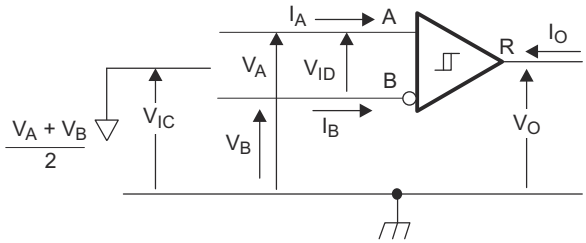


図 6-7. Receiver Voltage and Current Definitions

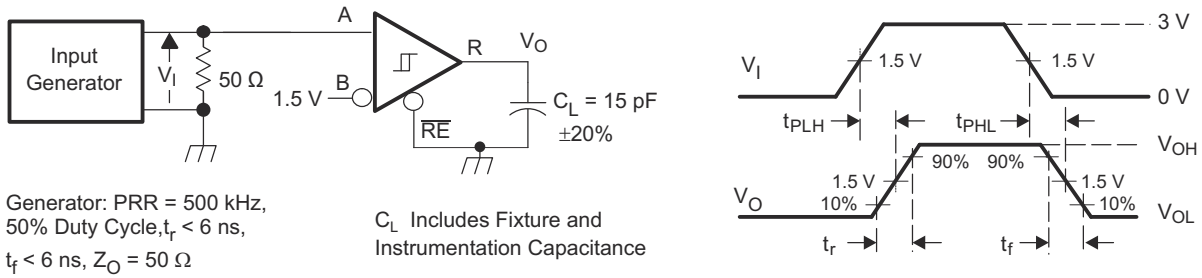


図 6-8. Receiver Switching Test Circuit and Voltage Waveforms

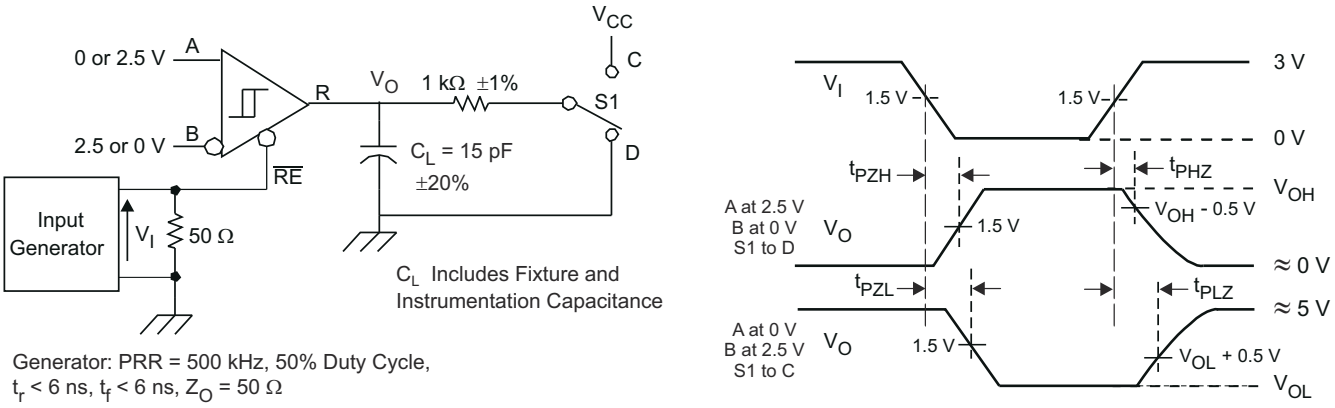
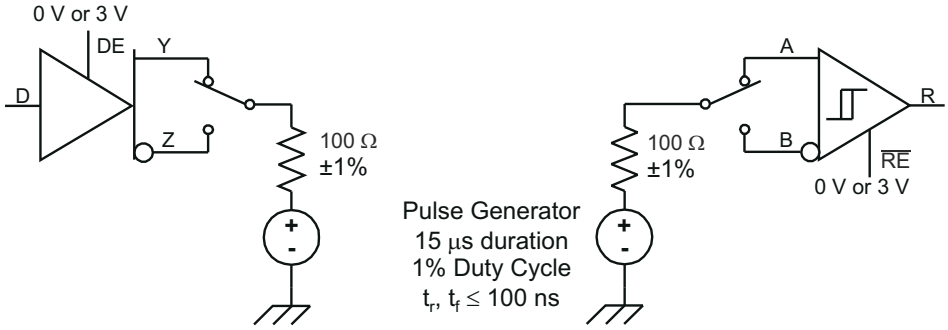


図 6-9. Receiver Enable and Disable Test Circuit and Voltage Waveforms



A. This test is conducted to test survivability only. Data stability at the R output is not specified.

図 6-10. Transient Overvoltage Test Circuit

7 Device Information

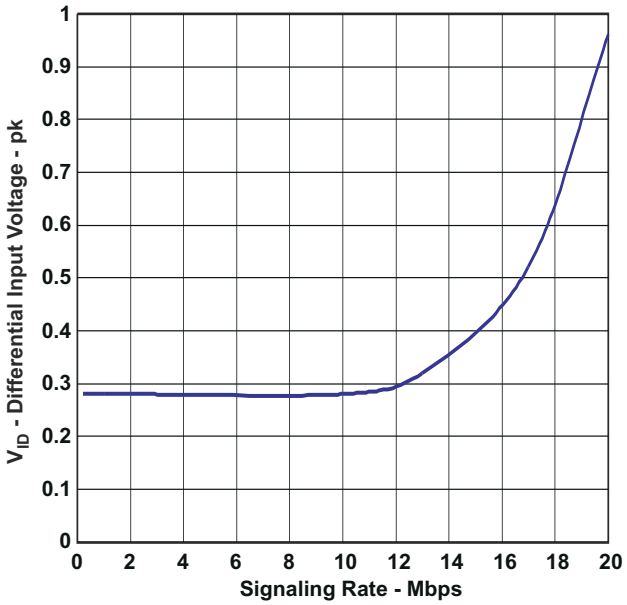


図 7-1. Recommended Minimum Differential Input Voltage vs Signaling Rate

7.1 Function Tables

DRIVER

INPUT(1)	ENABLE	OUTPUTS	
D	DE	Y	Z
H	H	H	L
L	H	L	H
X	L or OPEN	Z	Z
Open	H	H	L

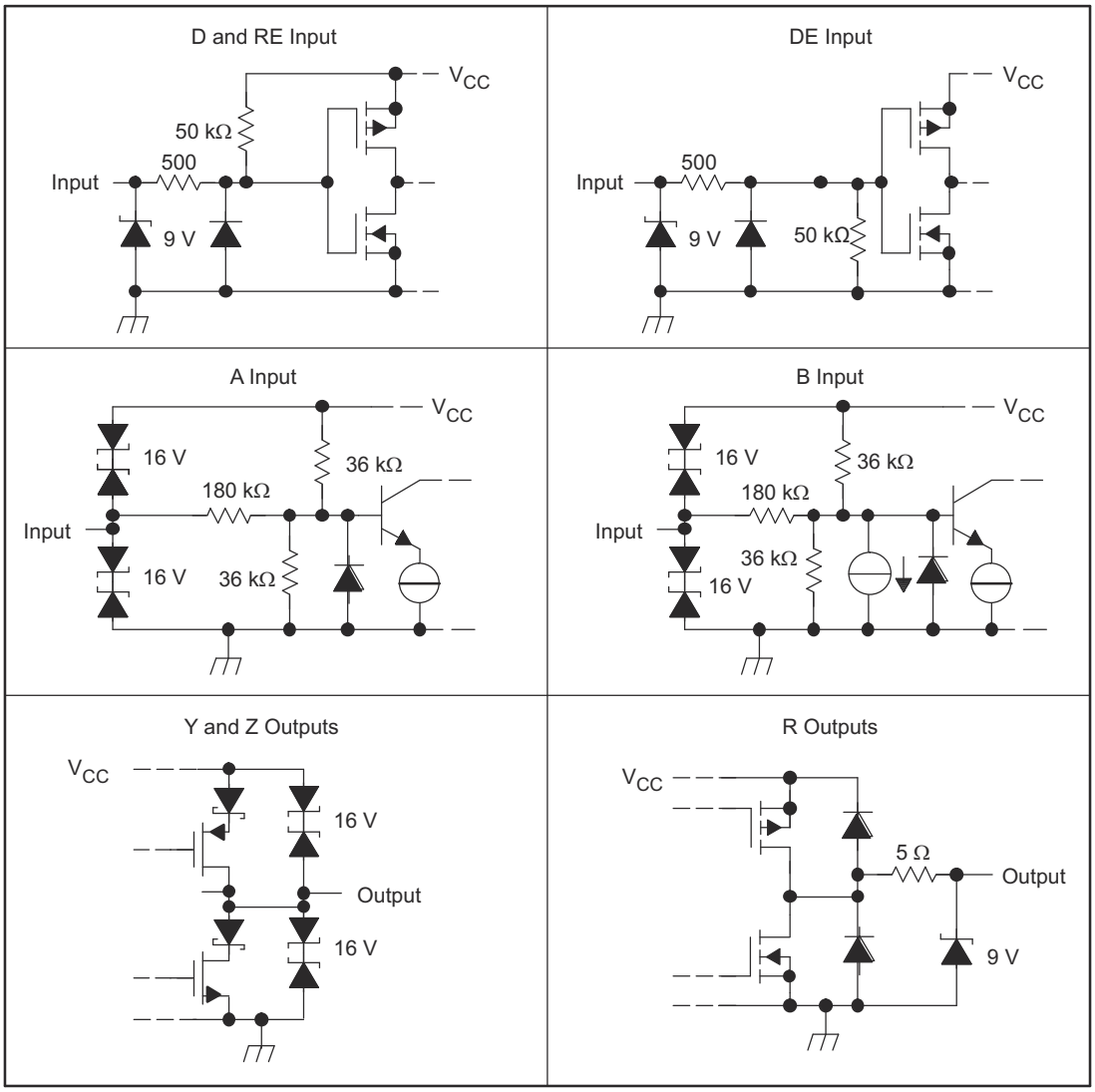
(1) H = high level, L = low level, Z = high impedance, X = irrelevant, ? = indeterminate

RECEIVER

DIFFERENTIAL INPUTS(1) $V_{ID} = V_{(A)} - V_{(B)}$	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \leq -0.2$ V	L	L
-0.2 V < V_{ID} < -0.01 V	L	?
-0.01 V ≤ V_{ID}	L	H
X	H or OPEN	Z
Open Circuit	L	H
BUS Idle	L	H
Short Circuit	L	H

(1) H = high level, L = low level, Z = high impedance, X = irrelevant, ? = indeterminate

7.2 Equivalent Input and Output Schematic Diagrams



8 Application Information

注

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8.1 Hot-Plugging

These devices are designed to operate in “hot swap” or “hot pluggable” applications. Key features for hot-pluggable applications are power-up, power-down glitch free operation, default disabled input/output pins, and receiver failsafe. An internal Power-On Reset circuit keeps the outputs in a high-impedance state until the supply voltage has reached a level at which the device will reliably operate. This ensures that no spurious transitions (glitches) will occur on the bus pin outputs as the power supply turns on or turns off.

As shown in the device FUNCTION TABLES, the ENABLE inputs have the feature of default disable on both the driver enable and receiver enable. This ensures that the device will neither drive the bus nor report data on the R pin until the associated controller actively drives the enable pins.

9 Device and Documentation Support

9.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.2 サポート・リソース

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9.3 商標

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9.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN65HVD3080EDGS	NRND	VSSOP	DGS	10	80	RoHS & Green	Call TI | NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BTT	
SN65HVD3080EDGSG4	NRND	VSSOP	DGS	10	80	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BTT	
SN65HVD3080EDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 85	BTT	Samples
SN65HVD3083EDGS	NRND	VSSOP	DGS	10	80	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BTU	
SN65HVD3083EDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 85	BTU	Samples
SN65HVD3086ED	NRND	SOIC	D	14	50	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD3086E	
SN65HVD3086EDGS	NRND	VSSOP	DGS	10	80	RoHS & Green	Call TI | NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BTF	
SN65HVD3086EDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 85	BTF	Samples
SN65HVD3086EDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	HVD3086E	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

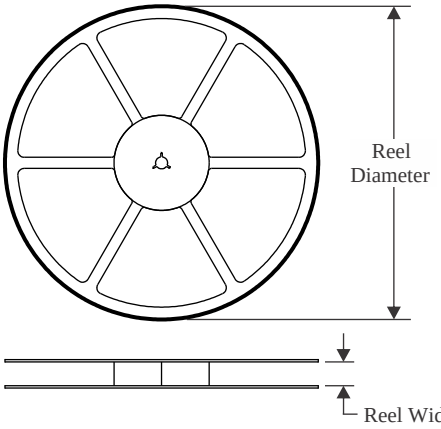
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

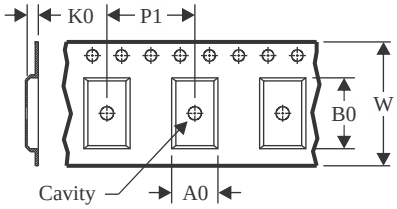
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

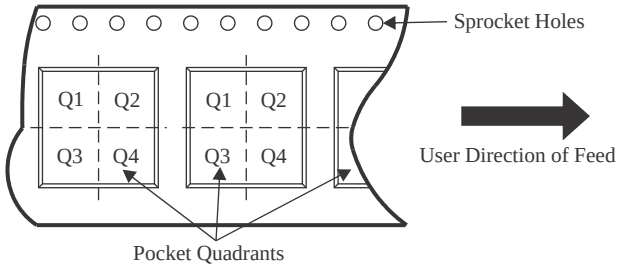


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

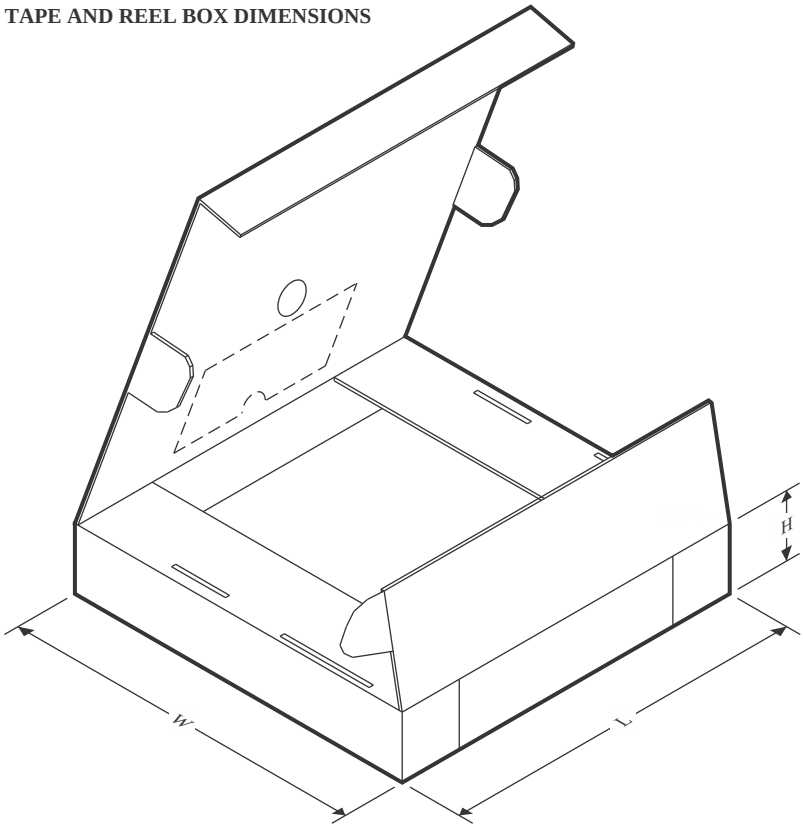
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD3080EDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65HVD3083EDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65HVD3086EDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
SN65HVD3086EDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

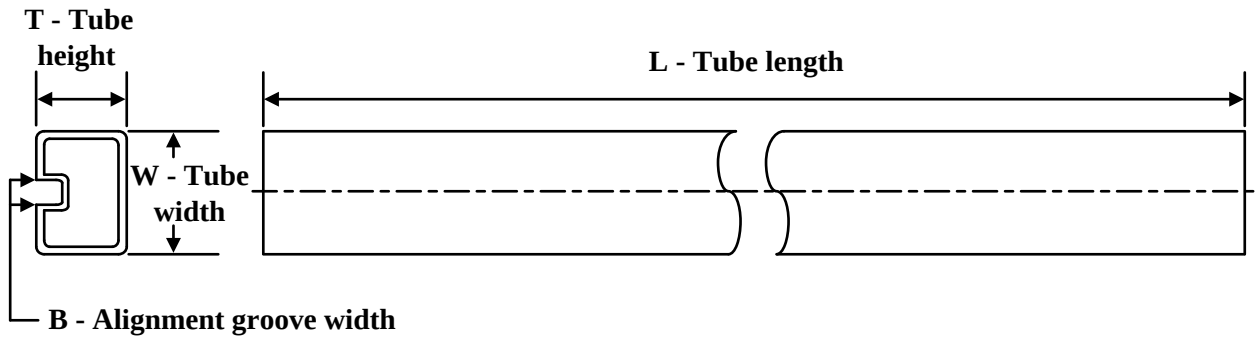
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD3080EDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
SN65HVD3083EDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
SN65HVD3086EDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
SN65HVD3086EDR	SOIC	D	14	2500	356.0	356.0	35.0

TUBE



*All dimensions are nominal

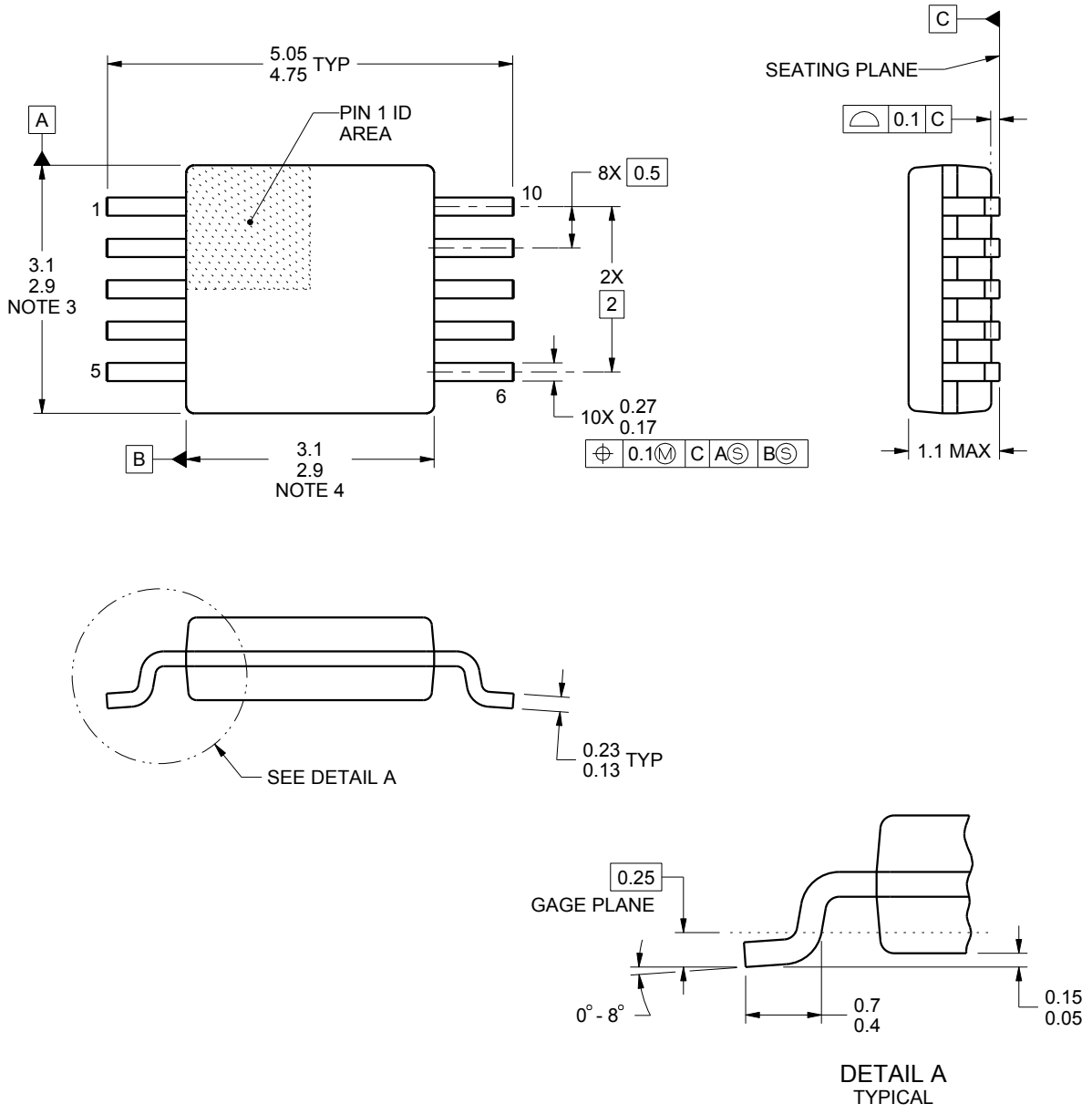
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65HVD3080EDGS	DGS	VSSOP	10	80	330.2	6.6	3005	1.88
SN65HVD3080EDGSG4	DGS	VSSOP	10	80	330.2	6.6	3005	1.88
SN65HVD3083EDGS	DGS	VSSOP	10	80	330.2	6.6	3005	1.88
SN65HVD3086ED	D	SOIC	14	50	506.6	8	3940	4.32
SN65HVD3086EDGS	DGS	VSSOP	10	80	330.2	6.6	3005	1.88

PACKAGE OUTLINE

DGS0010A

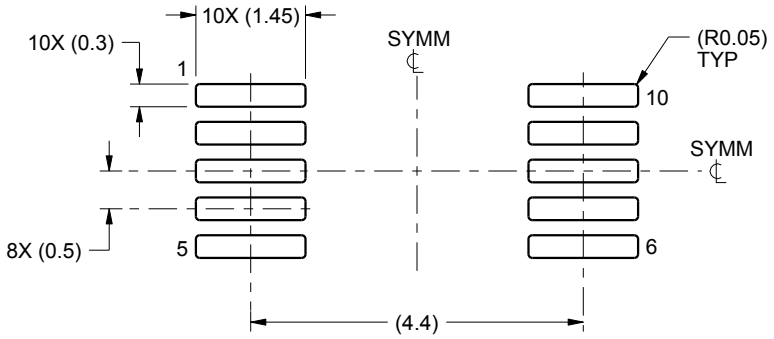
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

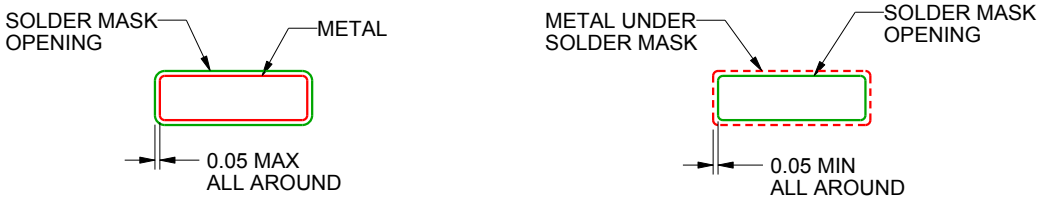


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

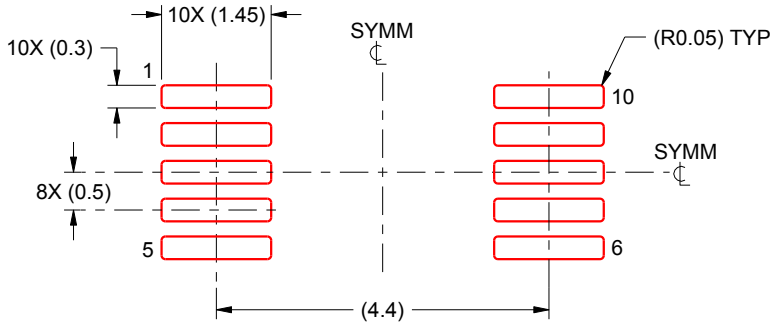


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



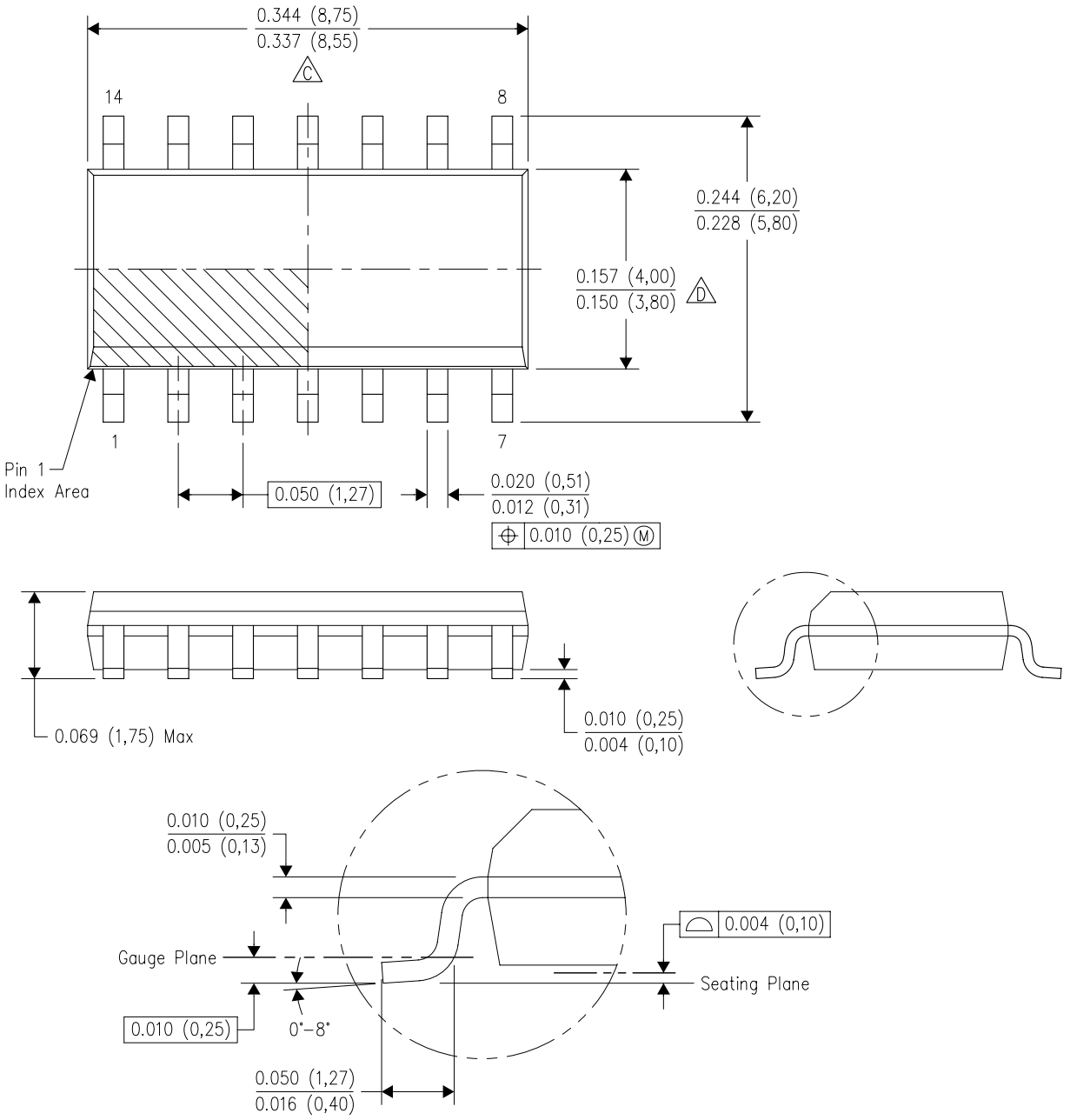
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

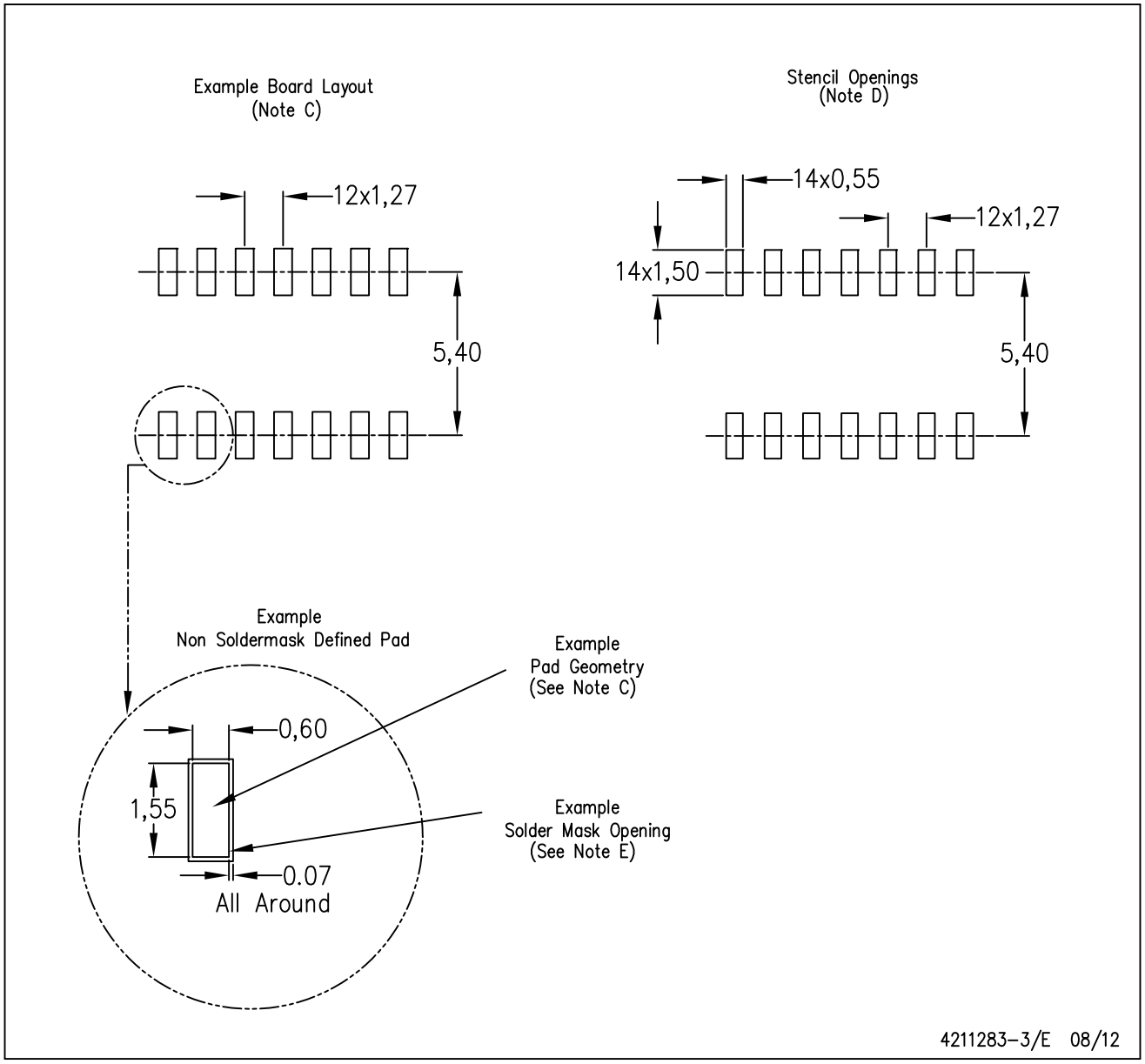
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

D (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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