# SN65HVDA195-Q1 LIN および MOST ECL 物理層インターフェイス

## 1 特長

- LIN 物理層仕様 レビジョン 2.0、および SAEJ2602 LIN 用推奨プラクティスに準拠
- LIN バスの速度は最大 20kbps (LIN 仕様最大および MOST ECL 速度) 、最小 0 ボーまで
- ISO9141 (K-LINE) をサポート
- 車載アプリケーション認定済み
- スリープ・モード:超低消費電流で、LIN バス、ウェークアップ入力 (外部スイッチ)、ホスト・マイクロコントローラからのウェークアップ・イベントが可能
- 高速受信に対応
- ±12kV (人体モデル) までの ESD 保護 (LIN ピン)
- LIN ピンは -40V～40V の電圧を入力可能
- 車載環境での過渡的なストレス (ISO 7637) への耐性
- 動作可能電源範囲 7V～27V DC に拡張 (LIN 仕様 7V～18V)
- 5V または 3.3V I/O ピンで MCU と接続
- RXD ピンでのウェイクアップ要求
- 外部電圧レギュレータの制御 (INH ピン)
- LIN レスポンダ・アプリケーション向けのプルアップ抵抗と直列ダイオードを内蔵
- 低い電磁放射 (EME)、高い電磁耐性 (EMI)
- バス端子はバッテリへの短絡、グランドへの短絡に対して保護
- 熱保護
- システム・レベルでグランド切断に対してフェイルセーフ
- システム・レベルでのグランド・シフト動作
- 電源オフのノードはネットワークに影響なし

## 2 アプリケーション

- 車載用
- 産業用センシング
- 大型家電製品の分散制御

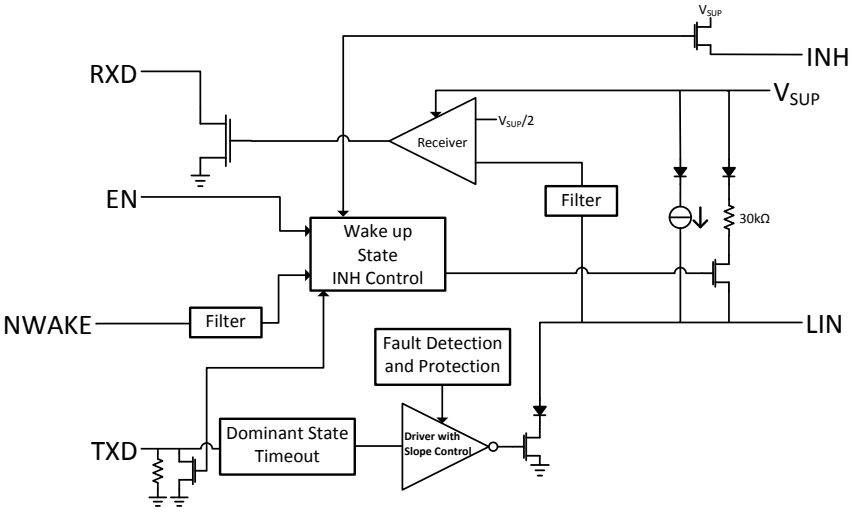
## 3 概要

SN65HVDA195 デバイスは、LIN (Local Interconnect Network) 物理層インターフェイスおよび MOST ECL インターフェイスであり、ウェイクアップおよび保護機能付きシリアル・トランシーバを内蔵しています。このバスは、最大 20kbps のデータ・レートの低速車載ネットワークで一般的に使用されている単線式双方向バスです。このデバイスは、ドミナント状態タイムアウトを持たないので、有効データ・レート 0kbps で送信できます。LIN 物理層仕様 レビジョン 2.0 で規定されているように、TXD 上のプロトコル出力データ・ストリームは、SN65HVDA195 によって、電流制限波形整形ドライバを通してバス信号に変換されます。このレシーバは、バスからのデータ・ストリームを変換し、RXD 経由でデータ・ストリームを出力します。バスには、ドミナント状態 (グランドに近い電圧) とリセッシブ状態 (バッテリに近い電圧) という 2 つの状態があります。リセッシブ状態では、バスは SN65HVDA195 の内部プルアップ抵抗と直列ダイオードによって HIGH にプルアップされるため、レスポンダ用途では外付けプルアップ部品は不要です。コマンダ用途では、LIN 仕様に従って外付けプルアップ抵抗 (1kΩ) と直列ダイオードが必要です。

**製品情報**

| 部品番号 | パッケージ(1) | 本体サイズ (公称) |
|---|---|---|
| SN65HVDA195-Q1 | SOIC (8) | 4.90mm × 3.91mm |

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。




**概略ブロック図**

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## 4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

**Changes from Revision B (March 2015) to Revision C (June 2022)** **Page**

- 旧式の用語を使っている場合、すべてコマンダおよびレスポンダに変更.....1

**Changes from Revision A (October 2009) to Revision B (March 2015)** **Page**

- 「*ピン構成および機能*」セクション、「*ESD 定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加.....1
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## 5 概要 (続き)

スリープ・モードでは、SN65HVDA195 は、ウェイクアップ回路がアクティブの状態のままですが、わずかな静止電流を必要とするだけです。これにより、LIN バスを介したリモート・ウェイクアップ、または NWake もしくは EN ピンを介したローカル・ウェイクアップが可能になります。

SN65HVDA195 は、過酷な車載用環境で動作するよう設計されています。このデバイスは、40V からグランドまでの LIN バス電圧のスイングを処理でき、-40V に耐えられます。また、グランド・シフトや電源電圧切断が発生した場合でも、電流が LIN 経由で電源入力へ逆流することを防止します。このデバイスは、低電圧、過熱、グランド喪失保護機能も備えています。フォルト条件が発生した場合、出力は即座にオフになり、フォルト条件が解消するまでオフに維持されます。

## 6 Pin Configuration and Functions

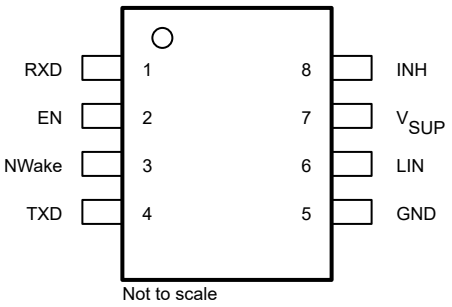



**図 6-1. D (SOIC) Package 8-Pin (Top View)**

**表 6-1. Pin Functions**

| PIN | | TYPE(1) | DESCRIPTION |
|---|---|---|---|
| NO. | NAME | | |
| 1 | RXD | O | RXD output (open drain) interface reporting state of LIN bus voltage |
| 2 | EN | I | Enable input |
| 3 | NWake | I | High voltage input for device wake up |
| 4 | TXD | I | TXD input interface to control state of LIN output |
| 5 | GND | GND | Ground |
| 6 | LIN | I/O | LIN bus single-wire transmitter and receiver |
| 7 | $V_{SUP}$ | Supply | Device supply voltage (connected to battery in series with external reverse blocking diode) |
| 8 | INH | O | Inhibit controls external voltage regulator with inhibit input |

(1) I = Input, O = Output, I/O = Input or Output, G = Ground.

# 7 Specifications

## 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

| PARAMETER | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{SUP}$ (2) | Supply line supply voltage(3) | | 0 | 40 | V |
| $V_{NWake}$ | NWake DC and transient input voltage (through serial resistor) | | –0.3 | 40 | |
| $I_{NWake}$ | $N_{Wake}$ current if due to ground shifts $V_{NWake} \le V_{GND} – 0.3$ V, thus the current into NWake must be limited through a serial resistance. | | | –3.6 | mA |
| $V_{INH}$ | INH voltage | | –0.3 | $V_{SUP}$ + 0.3 | V |
| $V_{Logic\_Input}$ | Logic pin input voltage | RXD, TXD, EN | –0.3 | 5.5 | |
| $V_{LIN}$ | LIN DC-input voltage | | –40 | 40 | |
| $T_A$ | Operational free-air temperature | | –40 | 125 | °C |
| $T_J$ | Junction temperature | | –40 | 150 | °C |
| $T_{SD}$ | Thermal shutdown | | | 200 | °C |
| $T_{SD\_HYS}$ | Thermal shutdown hysteresis | | | 25 | °C |
| $T_{stg}$ | Storage temperature | | –40 | 165 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) The device is specified for operation in the range of $V_{SUP}$ from 7 V to 27 V. Operating the device more than 27 V may significantly raise the junction temperature of the device and system level thermal design must be considered.
(4) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.

## 7.2 ESD Ratings

| | | | | VALUE | UNIT |
|---|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002(1) | All pins except LIN and NWake | ±4000 | V |
| | | | Pin LIN | ±12000 | |
| | | | Pin NWake | ±11000 | |
| | | Charged-device model (CDM), per AEC Q100-011 | All pins | ±1500 | |

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | MIN | MAX | UNIT |
|---|---|---|---|
| $V_{SUP}$ | 7 | 27 | V |
| $T_{AMB}$ | –40 | 125 | °C |

## 7.4 Thermal Information

| THERMAL METRIC(1) | | D (SOIC) | UNIT |
|---|---|---|---|
| | | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 112.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 66.3 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 52.9 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 19.3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 52.4 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 7.5 Electrical Characteristics

$V_{SUP}$ = 7 V to 27 V, $T_A$ = –40°C to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SUPPLY** | | | | | | |
| | Operational supply voltage(2) | Device is operational beyond the LIN 2.0 defined nominal supply line voltage range of 7 V ≤ $V_{SUP}$ ≤ 18 V | 7 | 14 | 27 | V |
| | Nominal supply line voltage | Normal and standby modes | 7 | 14 | 18 | V |
| | | Sleep mode | 7 | 12 | 18 | V |
| | $V_{SUP}$ undervoltage threshold | | | 4.8 | 6 | V |
| $I_{SUP}$ | Supply current | Normal mode, EN = High, Bus dominant (total bus load where $R_{LIN}$ ≥ 500 Ω and $C_{LIN}$ ≤ 10 nF (see 図 8-1)(3), INH = $V_{SUP}$, NWake = $V_{SUP}$ | | 1.2 | 7.5 | mA |
| | | Standby mode, EN = low, Bus dominant (total bus load where $R_{LIN}$ ≥ 500 Ω and $C_{LIN}$ ≤ 10 nF (see 図 8-1)(3), INH = $V_{SUP}$, NWake = $V_{SUP}$ | | 1 | 2.1 | mA |
| | | Normal mode, EN = High, Bus recessive, LIN = $V_{SUP}$, INH = $V_{SUP}$, NWake = $V_{SUP}$ | | 450 | 775 | µA |
| | | Standby mode, EN = Low, Bus recessive, LIN = $V_{SUP}$, INH = $V_{SUP}$, NWake = $V_{SUP}$ | | 450 | 775 | µA |
| | | Sleep mode, EN = 0, $T_A$ = –40°C to 95°C, 7 V < $V_{SUP}$ ≤ 12 V, LIN = $V_{SUP}$, NWake = $V_{SUP}$ | | 13 | 26 | µA |
| | | Sleep mode, EN = 0, $T_A$ = –40°C to 95°C, 12 V < $V_{SUP}$ < 18 V, LIN = $V_{SUP}$, NWake = $V_{SUP}$ | | | 35 | µA |
| $\Delta I_{SUP}$ | Delta supply current in sleep mode | Sleep mode, EN = 0, $T_A$ = –40°C to 95°C, Supply line voltage range of 7 V ≤ $V_{SUP}$ ≤ 18 V, LIN bus voltage: $V_{SUP}$ – 1.85 V ≤ LIN ≤ $V_{SUP}$ | | | 20 | µA |
| **RXD OUTPUT PIN** | | | | | | |
| $V_O$ | Output voltage | | –0.3 | | 5.5 | V |
| $I_{OL}$ | Low-level output current, open drain | LIN = 0 V, RXD = 0.4 V | 3.5 | | | mA |
| $I_{IKG}$ | Leakage current, high-level | LIN = $V_{SUP}$, RXD = 5 V | –5 | 0 | 5 | µA |
| **TXD INPUT PIN** | | | | | | |
| $V_{IL}$ | Low-level input voltage | | –0.3 | | 0.8 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 5.5 | V |
| $V_{IT}$ | Input threshold hysteresis voltage | | 30 | | 500 | mV |
| | Pulldown resistor | | 125 | 350 | 800 | kΩ |
| $I_{IL}$ | Low-level input current | TXD = Low | –5 | 0 | 5 | µA |
| **LIN PIN (REFERENCED TO $V_{SUP}$)** | | | | | | |
| $V_{OH}$ | High-level output voltage | LIN recessive, TXD = High, $I_O$ = 0 mA, $V_{SUP}$ = 14 V | $V_{SUP}$ – 1 | | | V |
| $V_{OL}$ | Low-level output voltage | LIN dominant, TXD = Low, $I_O$ = 40 mA, $V_{SUP}$ = 14 V | 0 | | 0.2 × $V_{SUP}$ | V |
| $R_{responder}$ | Pullup resistor to $V_{SUP}$ | Normal and standby modes | 20 | 30 | 60 | kΩ |
| | Pullup current source to $V_{SUP}$ | Sleep mode, $V_{SUP}$ = 14 V, LIN = GND | –2 | | –20 | µA |
| $I_L$ | Limiting current | TXD = 0 V | 45 | 160 | 220 | mA |
| | | TXD = 0 V, $T_A$ = –10°C to 125°C | | | 200 | mA |

## 7.5 Electrical Characteristics (continued)

$V_{SUP}$ = 7 V to 27 V, $T_A$ = –40°C to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_{LKG}$ | Leakage current | LIN = $V_{SUP}$ | –5 | 0 | 5 | µA |
| $I_{LKG}$ | Leakage current, loss of supply | 7 V < LIN ≤ 12 V, $V_{SUP}$ = GND | | | 5 | µA |
| | | 12 V < LIN < 18 V, $V_{SUP}$ = GND | | | 10 | µA |
| $V_{IL}$ | Low-level input voltage | LIN dominant | | | 0.4 × $V_{SUP}$ | V |
| $V_{IH}$ | High-level input voltage | LIN recessive | 0.6 × $V_{SUP}$ | | | V |
| $V_{IT}$ | Input threshold voltage | | 0.4 × $V_{SUP}$ | 0.5 × $V_{SUP}$ | 0.6 × $V_{SUP}$ | V |
| $V_{hys}$ | Hysteresis voltage | | 0.05 × $V_{SUP}$ | | 0.175 × $V_{SUP}$ | V |
| $V_{IL}$ | Low-level input voltage for wakeup | | | | 0.4 × $V_{SUP}$ | V |
| **EN PIN** | | | | | | |
| $V_{IL}$ | Low-level input voltage | | –0.3 | | 0.8 | V |
| $V_{IH}$ | High-level input voltage | | 2 | | 5.5 | V |
| $V_{hys}$ | Hysteresis voltage | | 30 | | 500 | mV |
| | Pulldown resistor | | 125 | 350 | 800 | kΩ |
| $I_{IL}$ | Low-level input current | EN = Low | –5 | 0 | 5 | µA |
| **INH PIN** | | | | | | |
| $V_o$ | DC output voltage | | –0.3 | | $V_{SUP}$ + 0.3 | V |
| $R_{on}$ | On state resistance | Between $V_{SUP}$ and INH, INH = 2-mA drive, Normal or standby mode | | 35 | 85 | Ω |
| $I_{IKG}$ | Leakage current | Low-power mode, 0 < INH < $V_{SUP}$ | –5 | 0 | 5 | µA |
| **NWAKE PIN** | | | | | | |
| $V_{IL}$ | Low-level input voltage | | –0.3 | | $V_{SUP}$ – 3.3 | V |
| $V_{IH}$ | High-level input voltage | | $V_{SUP}$ – 1 | | $V_{SUP}$ + 0.3 | V |
| | Pullup current | NWake = 0 V | –45 | –10 | –2 | µA |
| $I_{IKG}$ | Leakage current | $V_{SUP}$ = NWake | –5 | 0 | 5 | µA |
| **THERMAL SHUTDOWN** | | | | | | |
| | Shutdown junction thermal temperature | | | 190 | | °C |
| **AC CHARACTERISTICS** | | | | | | |
| D1 | Duty cycle 1(4) | $TH_{REC(max)}$ = 0.744 × $V_{SUP}$, $TH_{DOM(max)}$ = 0.581 × $V_{SUP}$, $V_{SUP}$ = 7 V to 18 V, $t_{BIT}$ = 50 µs (20 kbps), D1 = $t_{Bus\_rec(min)}$/ (2 × $t_{BIT}$). See 図 7-1 | 0.396 | | | |
| D2 | Duty cycle 2(4) | $TH_{REC(min)}$ = 0.422 × $V_{SUP}$, $TH_{DOM(min)}$ = 0.284 × $V_{SUP}$, $V_{SUP}$ = 7.6 V to 18 V, $t_{BIT}$ = 50 µs (20 kbps), D2 = $t_{Bus\_rec(max)}$/ (2 × $t_{BIT}$). See 図 7-1 | | | 0.581 | |
| D3 | Duty cycle 3(4) | $TH_{REC(max)}$ = 0.778 × $V_{SUP}$, $TH_{DOM(max)}$ = 0.616 × $V_{SUP}$, $V_{SUP}$ = 7 V to 18 V, $t_{BIT}$ = 96 µs (10.4 kbps), D3 = $t_{Bus\_rec(min)}$/ (2 × $t_{BIT}$). See 図 7-1 | 0.417 | | | |

## 7.5 Electrical Characteristics (continued)

$V_{SUP}$ = 7 V to 27 V, $T_A$ = –40°C to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP(1) | MAX | UNIT |
|---|---|---|---|---|---|---|
| D4 | Duty cycle 4(4) | $TH_{REC(min)}$ = 0.389 × $V_{SUP}$, $TH_{DOM(min)}$ = 0.251 × $V_{SUP}$,<br>$V_{SUP}$ = 7.6 V to 18 V,<br>$t_{BIT}$ = 96 µs (10.4 kbps),<br>D4 = $t_{Bus\_rec(max)}$/ (2 × $t_{BIT}$).<br>See 図 7-1 | | | 0.59 | |
| $t_{rx\_pdr}$ | Receiver rising propagation delay time | $R_{RXD}$ = 2.4 kΩ, $C_{RXD}$ = 20 pF<br>See 図 7-2<br>See 図 8-1 | | | 6 | µs |
| $t_{rx\_pdf}$ | Receiver falling propagation delay time | $R_{RXD}$ = 2.4 kΩ, $C_{RXD}$ = 20 pF<br>See 図 7-2<br>See 図 8-1 | | | 6 | |
| $t_{rx\_sym}$ | Symmetry of receiver propagation delay time | rising edge with respect to falling edge ($t_{rx\_sym}$ = $t_{rx\_pdf}$ – $t_{rx\_pdr}$)<br>$R_{RXD}$ = 2.4 kΩ, $C_{RXD}$ = 20 pF<br>See 図 7-2<br>See 図 8-1 | –2 | | 2 | |
| $t_{NWake}$ | NWake filter time for local wakeup | See 図 9-4 | 25 | 50 | 150 | |
| $t_{LINBUS}$ | LIN wake-up filter time (dominant time for wakeup through LIN bus) | See 図 9-3 | 25 | 50 | 150 | |
| $t_{go\_to\_operate}$ | | See 図 9-2 to 図 9-3 | | 0.5 | 1 | |

(1) Typical values are given for $V_{SUP}$ = 14 V at 25°C, except for low power mode where typical values are given for $V_{SUP}$ = 12 V at 25°C.
(2) All voltages are defined with respect to ground; positive currents flow into the SN65HVDA195 device.
(3) In the dominant state, the supply current increases as the supply voltage increases due to the integrated LIN responder termination resistance. At higher voltages the majority of supply current is through the termination resistance. The minimum resistance of the LIN responder termination is 20 kΩ, so the maximum supply current attributed to the termination is:
$I_{SUP\ (dom)\ max\ termination} ≠ (V_{SUP} – (V_{LIN\_Dominant} + 0.7\ V) / 20\ kΩ$
(4) Duty cycles: LIN driver bus load conditions ($C_{LINBUS}$, $R_{LINBUS}$): Load1 = 1 nF, 1 kΩ; Load2 = 10 nF, 500 Ω. Duty cycles 3 and 4 are defined for 10.4-kbps operation. The SN65HVDA195 also meets these lower data rate requirements, while it is capable of the higher speed 20-kbps operation as specified by Duty cycles 1 and 2. SAEJ2602 derives propagation delay equations from the LIN 2.0 duty cycle definitions, for details see the SAEJ2602 specification.

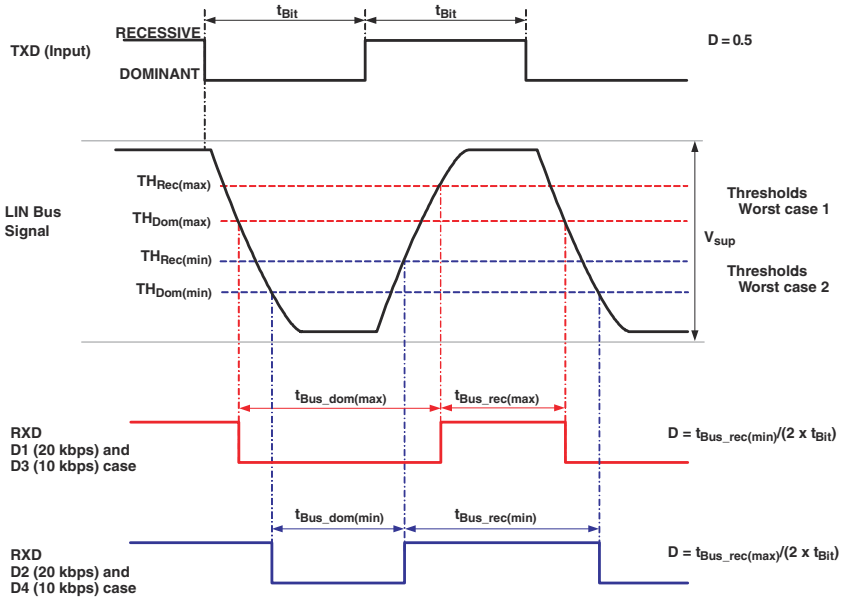



**図 7-1. Definition of Bus Timing Parameters**

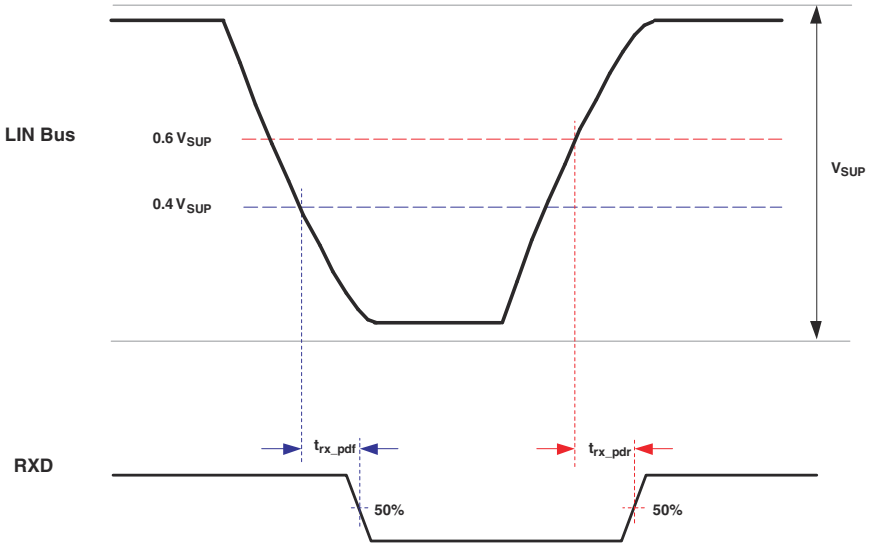



図 7-2. Propagation Delay

## 7.6 Typical Characteristics

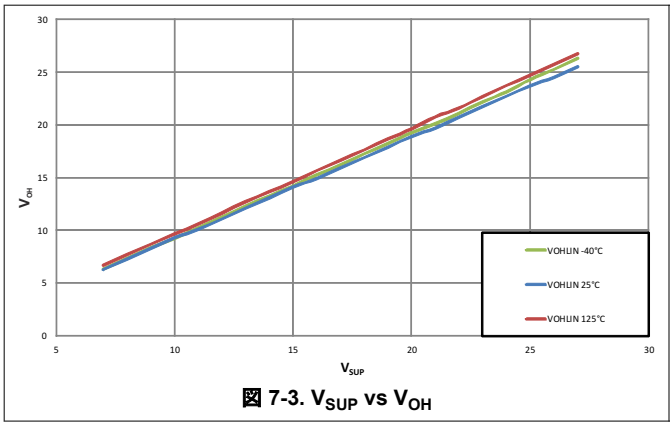



図 7-3. $V_{SUP}$ vs $V_{OH}$

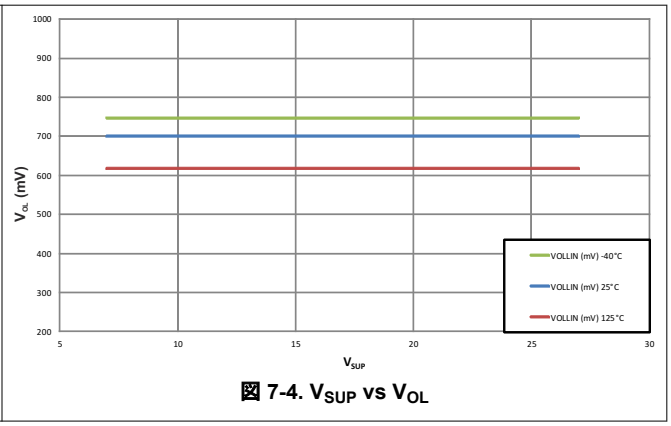



図 7-4. $V_{SUP}$ vs $V_{OL}$

# 8 Parameter Measurement Information

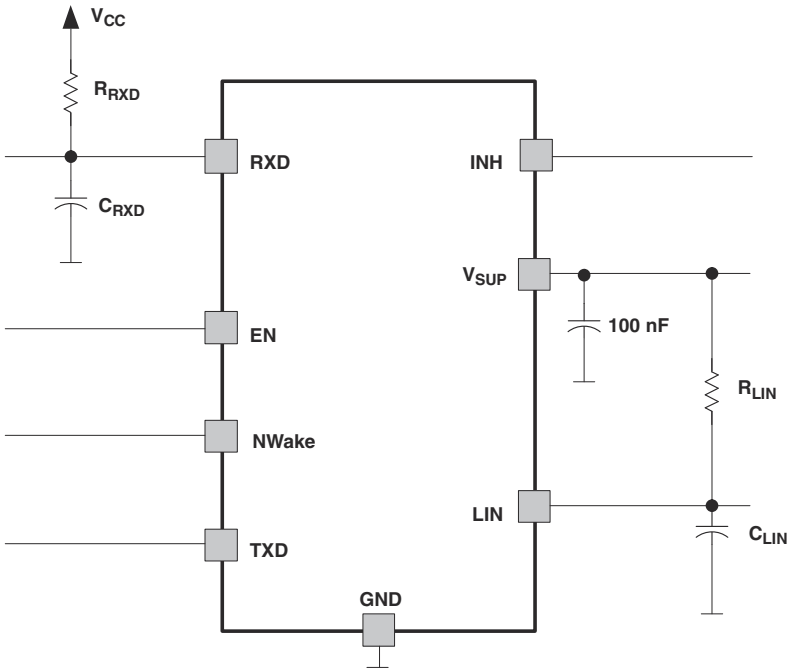


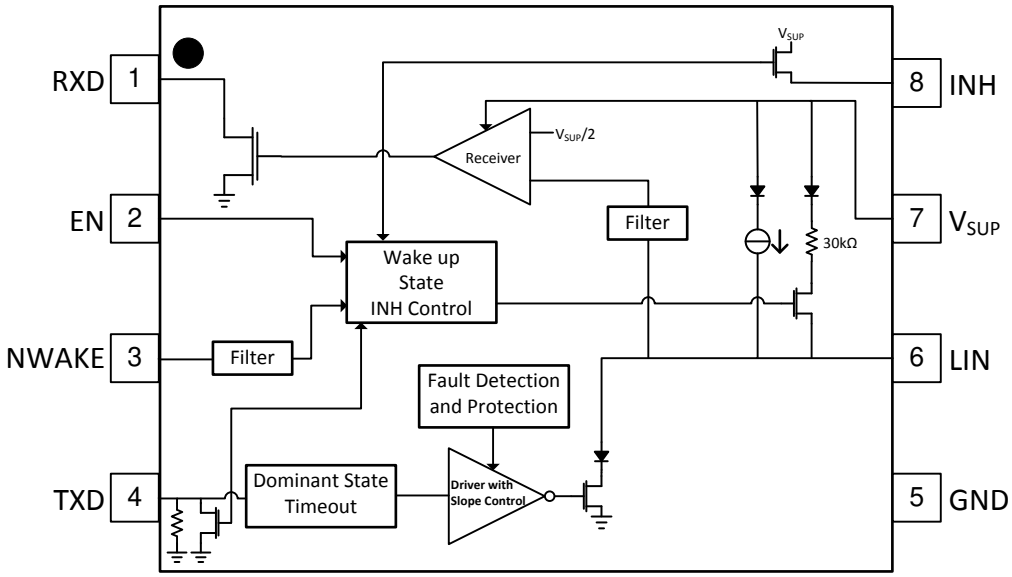

**図 8-1. Test Circuit for AC Characteristics**

# 9 Detailed Description

## 9.1 Overview

The SN65HVDA195-Q1 LIN transceiver is a LIN (Local Interconnect Network) physical layer transceiver which integrates a serial transceiver with wake up and protection features. The LIN bus is a single wire, bi-directional bus that typically is used in low speed in vehicle networks with data rates that range from 2.4 kbps to 20 kbps

## 9.2 Functional Block Diagram




## 9.3 Feature Description

### 9.3.1 Local Interconnect Network (LIN) Bus

This I/O pin is the single-wire LIN bus transmitter and receiver.

#### *9.3.1.1 Transmitter Characteristics*

The driver is a low-side transistor with internal current limitation and thermal shutdown. There is an internal 30-kΩ pullup resistor with a serial diode structure to $V_{SUP}$, so no external pullup components are required for LIN responder mode applications. An external pullup resistor of 1 kΩ, plus a series diode to $V_{SUP}$ must be added when the device is used for commander node applications.

Voltage on LIN can go from –40-V to 40-V DC without any currents other than through the pullup resistance. There are no reverse currents from the LIN bus to supply ($V_{SUP}$), even in the event of a ground shift or loss of supply ($V_{SUP}$).

The LIN thresholds and AC parameters are LIN Protocol Specification Revision 2.0 compliant.

During a thermal shut down condition, the driver is disabled.

#### *9.3.1.2 Receiver Characteristics*

The receiver's characteristic thresholds are ratio-metric with the device supply pin. Typical thresholds are 50%, with a hysteresis from 5% to 17.5% of supply.

The receiver is capable of receiving higher data rates (>100 kbps) than supported by LIN or SAEJ2602 specifications. This allows the SN65HVDA195 to be used for high-speed downloads at end-of-line production or other applications. The actual data rates achievable depend on system time constants (bus capacitance and pullup resistance) and driver characteristics used in the system.

### 9.3.2 Transmit Input (TXD)

TXD is the interface to the MCU's LIN protocol controller or SCI/UART used to control the state of the LIN output. When TXD is low, the LIN output is dominant (near ground). When TXD is high, the LIN output is recessive (near battery). The TXD input structure is compatible with microcontrollers with 3.3-V and 5-V I/O. TXD has an internal pulldown resistor. This device does not have a TXD dominant time-out protection circuit so that low data rates may be used.

### 9.3.3 Receive Output (RXD)

RXD is the interface to the MCU's LIN protocol controller or SCI/UART, which reports the state of the LIN bus voltage. LIN recessive (near battery) is represented by a high level on RXD and LIN dominant (near ground) is represented by a low level on RXD. The RXD output structure is an open-drain output stage. This allows the SN65HVDA195 to be used with 3.3-V and 5-V I/O microcontrollers. If the microcontroller's RXD pin does not have an integrated pullup, an external pullup resistor to the microcontroller I/O supply voltage is required.

#### *9.3.3.1 RXD Wake-Up Request*

When the SN65HVDA195 has been in low-power mode and encounters a wake-up event from the LIN bus or NWake pin, RXD goes low, while the device enters and remains in standby mode (until EN is reasserted high and the device enters normal mode).

### 9.3.4 Supply Voltage ($V_{SUP}$)

$V_{SUP}$ is the SN65HVDA195 device power supply pin. $V_{SUP}$ is connected to the battery through an external reverse battery blocking diode. The characterized operating voltage range for the SN65HVDA195 is from 7 V to 27 V. $V_{SUP}$ is protected for harsh automotive conditions up to 40 V.

The device contains a reset circuit to avoid false bus messages during undervoltage conditions when $V_{SUP}$ is less than $V_{SUP\_UNDER}$.

### 9.3.5 Ground (GND)

GND is the SN65HVDA195 device ground connection. The SN65HVDA195 can operate with a ground shift as long as the ground shift does not reduce $V_{SUP}$ below the minimum operating voltage. If there is a loss of ground at the ECU level, the SN65HVDA195 does not have a significant current consumption on LIN bus.

### 9.3.6 Enable Input (EN)

EN controls the operation mode of the SN65HVDA195 (normal or sleep mode). When EN is high, the SN65HVDA195 is in normal mode allowing a transmission path from TXD to LIN and from LIN to RXD. When EN is low, the device is put into sleep mode and there are no transmission paths available. The device can enter normal mode only after being woken up. EN has an internal pulldown resistor to make sure the device remains in low-power mode even if EN floats.

### 9.3.7 NWake Input (NWake)

NWake is a high-voltage input used to wake up the SN65HVDA195 from low-power mode. NWake is usually connected to an external switch in the application. A low on NWake that is asserted longer than the filter time ($t_{NWAKE}$) results in a local wakeup. NWake provides an internal pullup source to $V_{SUP}$.

### 9.3.8 Inhibit Output (INH)

INH is used to control an external voltage regulator that has an inhibit input. When the SN65HVDA195 is in normal operating mode, the inhibit high-side switch is enabled and the external voltage regulator is activated. When SN65HVDA195 is in low-power mode, the inhibit switch is turned off, which disables the voltage regulator. A wake-up event on for the SN65HVDA195 returns INH to $V_{SUP}$ level. INH can also drive an external transistor connected to an MCU interrupt input.

## 9.4 Device Functional Modes

### 9.4.1 Operating Modes

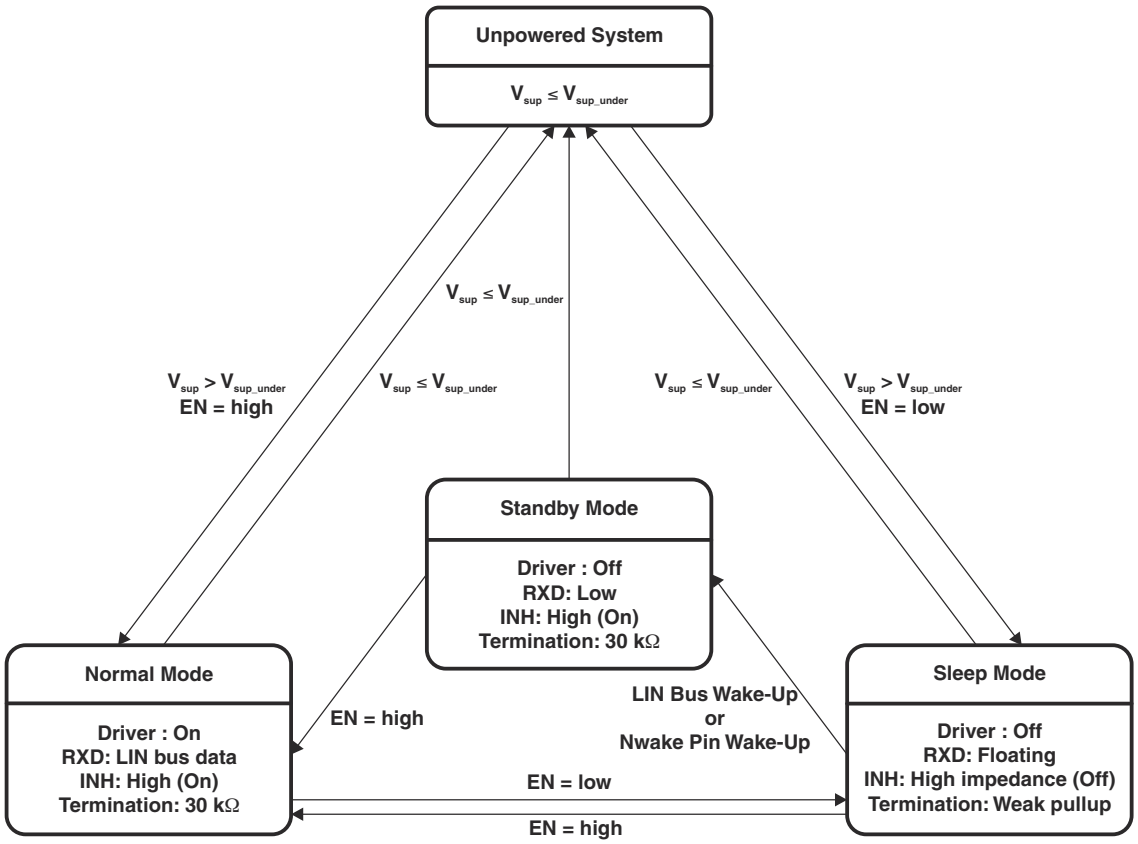



**図 9-1. Operating States Diagram**

**表 9-1. Operating Modes**

| MODE | EN | RXD | LIN BUS TERMINATION | INH | TRANSMITTER | COMMENTS |
|---|---|---|---|---|---|---|
| Sleep | Low | Floating | Weak current pullup | High impedance | Off | |
| Standby | Low | Low | 30 kΩ (typ) | High | Off | Wake-up event detected, waiting on MCU to set EN |
| Normal | High | LIN bus data | 30 kΩ (typ) | High | On | LIN transmission up to 20 kbps |

### 9.4.2 Normal Mode

This is the normal operational mode, in which the receiver and driver are active, and LIN transmission up to the LIN specified maximum of 20 kbps is supported. The receiver detects the data stream on the LIN bus and outputs it on RXD for the LIN controller, where recessive on the LIN bus is a digital high, and dominate on the LIN bus is digital low. The driver transmits input data on TXD to the LIN bus. Normal mode is entered as EN transitions high while the SN65HVDA195 is in sleep or standby mode.

### 9.4.3 Sleep Mode

Sleep mode is the power saving mode for the SN65HVDA195 and the default state after power up (assuming EN is low during power up). Even with the extremely low current consumption in this mode, the SN65HVDA195 can still wake up from LIN bus through a wake-up signal, a low on NWake, or if EN is set high. The LIN bus and NWake are filtered to prevent false wake-up events. The wake-up events must be active for their respective time periods ($t_{LINBUS}$, $t_{NWake}$).

The sleep mode is entered by setting EN low.

While the device is in sleep mode, the following conditions exist:

- The LIN bus driver is disabled and the internal LIN bus termination is switched off (to minimize power loss if LIN is short-circuited to ground). However, the weak current pullup is active to prevent false wake-up events in case an external connection to the LIN bus is lost.
- The normal receiver is disabled.
- INH is high impedance.
- EN input, NWake input, and the LIN wake-up receiver are active.

### 9.4.4 Wake-Up Events

There are three ways to wake up the SN65HVDA195 from sleep mode:

- Remote wakeup through recessive (high) to dominant (low) state transition on LIN bus. The dominant state must be held for $t_{LINBUS}$ filter time and then the bus must return to the recessive state (to eliminate false wake-ups from disturbances on the LIN bus or if the bus is shorted to ground).
- Local wakeup through a low on NWake, which is asserted low longer than the filter time $t_{NWake}$ (to eliminate false wake-ups from disturbances on NWake)
- Local wakeup through EN being set high

### 9.4.5 Standby Mode

This mode is entered whenever a wake-up event occurs through LIN bus or NWake while the SN65HVDA195 is in sleep mode. The LIN bus responder termination circuit and INH are turned on when standby mode is entered. The application system powers up once INH is turned on, assuming the system is using a voltage regulator connected through INH. Standby mode is signaled through a low level on RXD.

When EN is set high while the SN65HVDA195 is in standby mode the device returns to normal mode and the normal transmission paths from TXD to LIN bus and LIN bus to RXD are enabled.

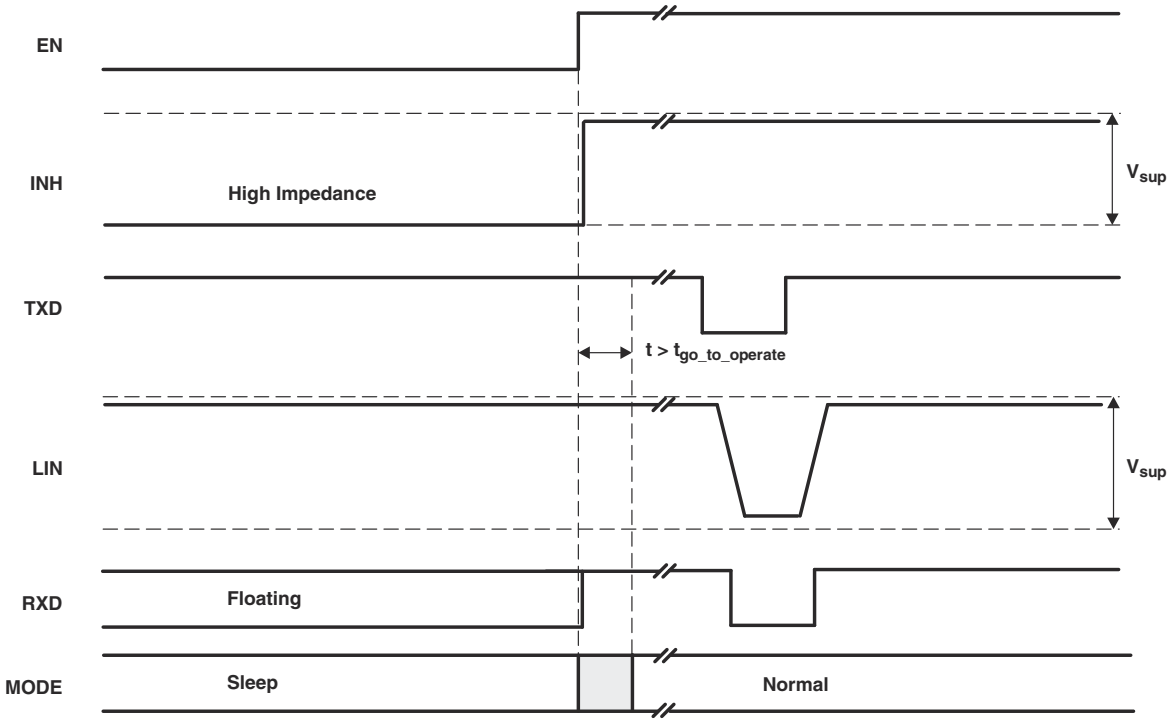



**図 9-2. Wakeup Through EN**

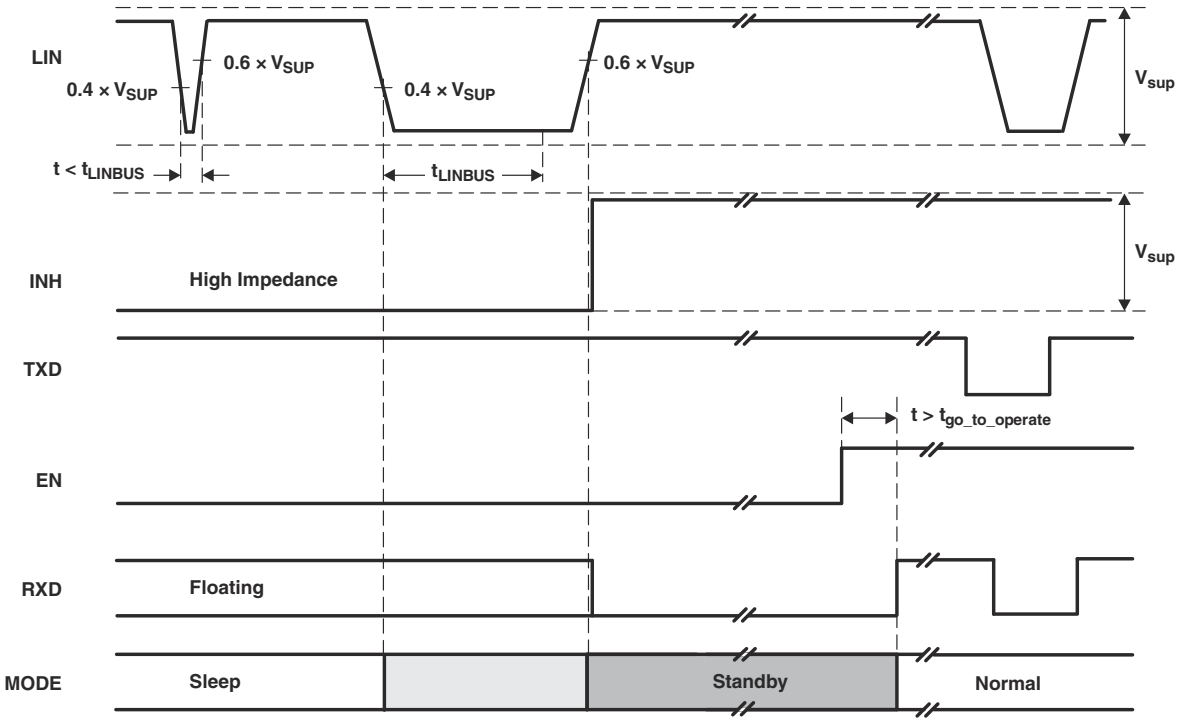



**図 9-3. Wakeup Through LIN**

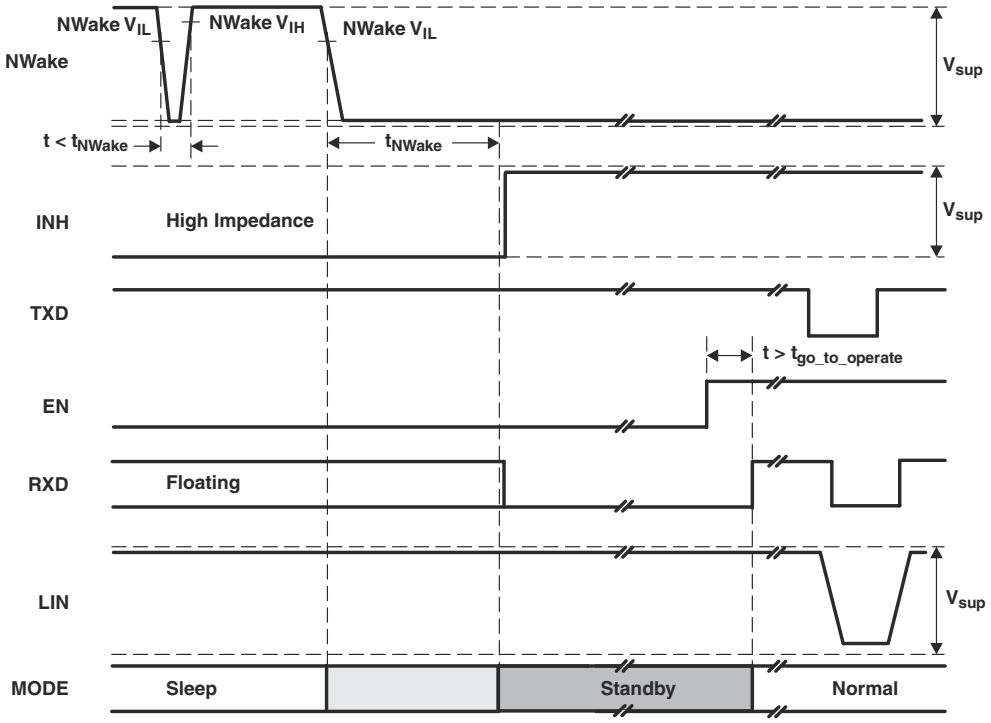



**図 9-4. Wakeup Through NWake**

# 10 Application and Implementation

注

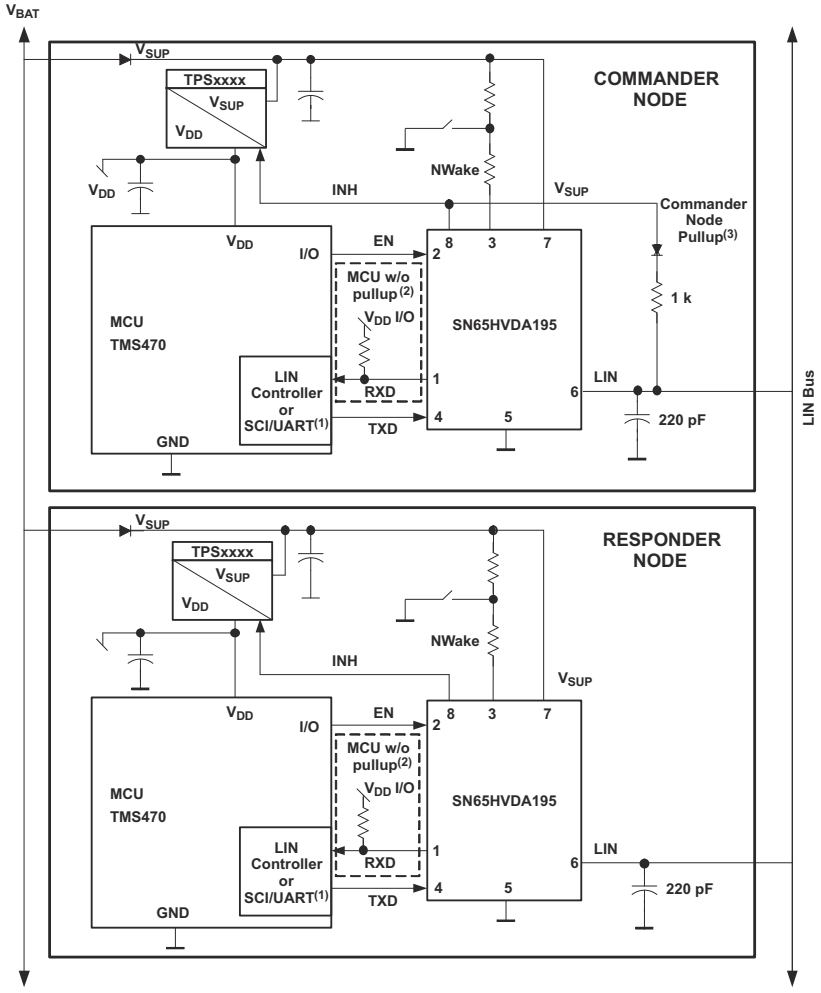
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 10.1 Application Information

The SN65HVDA195-Q1 can be used as both a responder device and a commander device in a LIN network. It comes with the ability to support both remote wake-up requests and local wake-up requests.

### 10.1.1 Typical Application

The device comes with an integrated 30-kΩ pullup resistor and series diode for responder applications, and for commander applications an external 1-kΩ pullup with series blocking diode can be used. 図 10-1 shows the device being used in both types of applications.




A. RXD on MCU or LIN responder has internal pullup, no external pullup resistor is needed.
B. RXD on MCU or LIN responder without internal pullup, requires external pullup resistor.
C. Commander node applications require an external 1-kΩ pullup resistor and serial diode.

**図 10-1. SN65HVDA195-Q1 Application Diagram**

#### 10.1.1.1 Design Requirements

For this design, use these requirements:

- RXD on MCU or LIN responder has internal pullup, no external pullup resistor is needed.
- RXD on MCU or LIN responder without internal pullup, requires external pullup resistor.
- Commander node applications require an external 1-kΩ pullup resistor and serial diode

#### 10.1.1.2 Detailed Design Procedure

The RXD output structure is an open-drain output stage. This allows the SN65HVDA195-Q1 to be used with 3.3-V and 5-V I/O microcontrollers. If the RXD pin of the microcontroller does not have an integrated pullup, an external pullup resistor to the microcontroller I/O supply voltage is required.

The $V_{SUP}$ pin of the device should be decoupled with a 100-nF capacitor as close to the supply pin of the device as possible.

The NWAKE pin is a high voltage wake-up input to the device. If this pin is not being used it should be tied to $V_{SUP}$.

#### 10.1.1.3 Application Curves

図 10-2 and 図 10-3 show the propagation delay from the TXD pin to the LIN pin for both the recessive to dominant and dominant to recessive states under lightly loaded conditions.

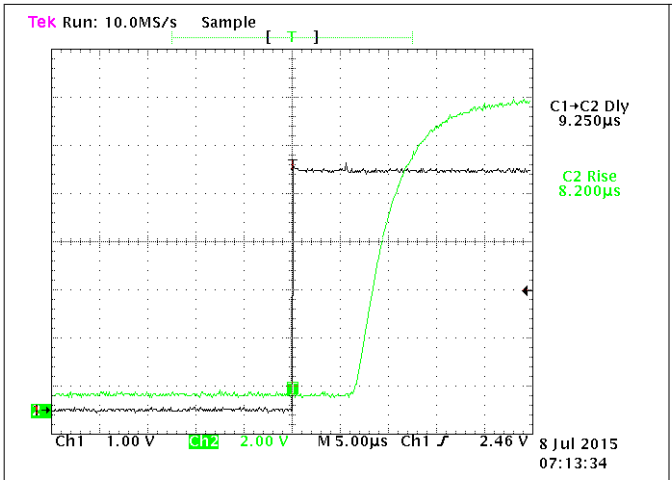



**図 10-2. SN65HVDA195-Q1 Dominant to Recessive Prop Delay**

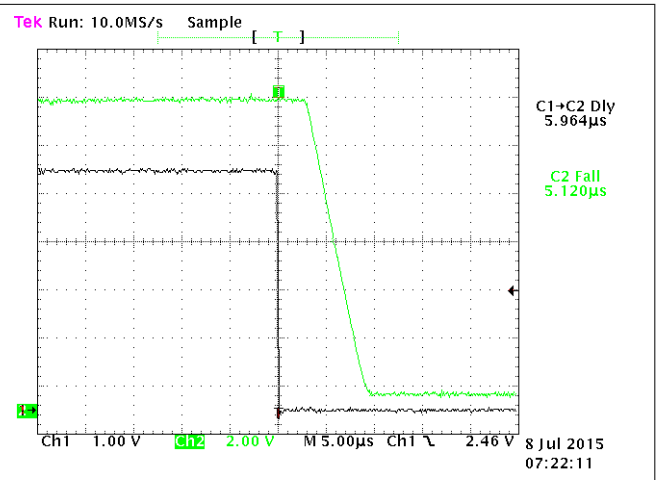



**図 10-3. SN65HVDA195-Q1 Recessive to Dominant Prop Delay**

### Power Supply Recommendations

The SN65HVDSA195-Q1 was designed to operate directly off a car battery, or any other DC supply ranging from 7 V to 27 V. A100-nF decoupling capacitor should be placed as close to the $V_{SUP}$ pin of the device as possible.

### 10.1.2 Layout

#### *10.1.2.1 Layout Guidelines*

Pin 1 is the RXD output of the SN65HVDA195-Q1. It is an open-drain output and requires an external pullup resistor in the range of 1-kΩ to 10 kΩ to function properly. If the micro-processor paired with the transceiver does not have an integrated pullup and external resistor should be placed between RXD and the regulated voltage supply for the micro-processor.

Pin 2 is the EN input pin for the device that is used to place the device in low power sleep mode. If this feature is not used on the device, the pin should be pulled high to the regulated voltage supply of the microprocessor through a series 1-kΩ to 10-kΩ series resistor. Additionally, a series resistor may be placed on the pin to limit the current on the digital lines in the case of an overvoltage fault.

Pin 3 is a high-voltage local wake up input pin. The device is typically externally controlled by a normally open switch tied between NWAKE and ground. When the momentary switch is pressed the NWAKE pin is pulled to ground signaling a local wake-up event. A series resistor between $V_{BATT}$ and the switch, and NWAKE and the switch should be placed to limit current. If the NWAKE local wake-up feature is not used, the pin can be tied to $V_{SUP}$ through a 1-kΩ to 10-kΩ pullup resistor.

Pin 4 is the transmit input signal to the device. A series resistor can be placed to limit the input current to the device in the case of an overvoltage on this pin. Also a capacitor to ground can be placed close to the input pin of the device to filter noise.

Pin 5 is the ground connection of the device. This pin should be tied to a ground plane through a short trace with the use of two vias to limit total return inductance.

Pin 6 is the LIN bus connection of the device. For responder applications a 220-pF bus capacitor is implemented. For commander applications an additional series resistor and blocking diode should be placed between the LIN pin and the $V_{SUP}$ pin.

Pin 7 is the supply pin for the device. A 100-nF decoupling capacitor should be placed as close to the device as possible.

Pin 8 is a high-voltage output pin that may be used to control the local power supplies. If this feature is not used the pin may be left floating.

注

All ground and power connections should be made as short as possible and use at least two vias to minimize the total loop inductance.

#### *10.1.2.2 Layout Example*

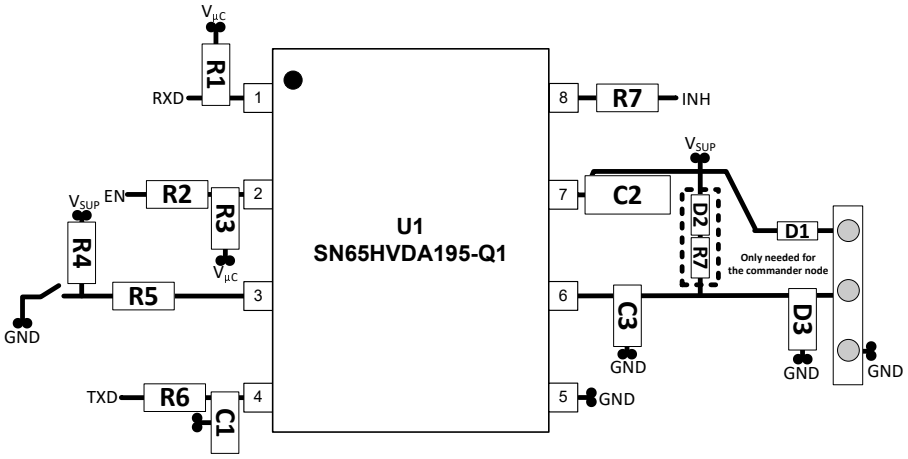



**図 10-4. Layout Example**

# 11 Device and Documentation Support

## 11.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 11.2 サポート・リソース

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## 11.3 Trademarks

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## 11.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 11.5 Glossary

TI Glossary — This glossary lists and explains terms, acronyms, and definitions.

# 12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable part number | Status (1) | Material type (2) | Package \| Pins | Package qty \| Carrier | RoHS (3) | Lead finish/ Ball material (4) | MSL rating/ Peak reflow (5) | Op temp (°C) | Part marking (6) |
|---|---|---|---|---|---|---|---|---|---|
| SN65HVDA195QDRQ1 | Active | Production | SOIC (D) \| 8 | 2500 \| LARGE T&R | Yes | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | A195Q |

**(1) Status:** For more details on status, see our product life cycle.

**(2) Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

**(3) RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

**(4) Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

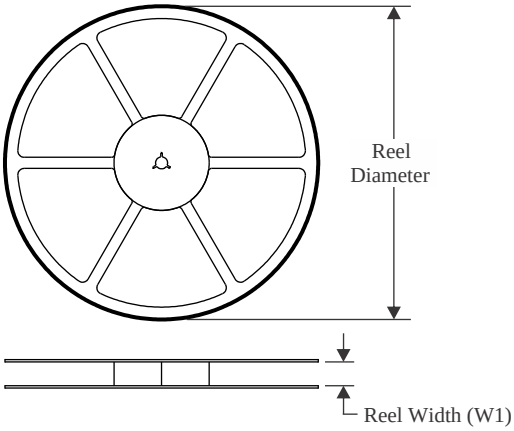
**(5) MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

**(6) Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

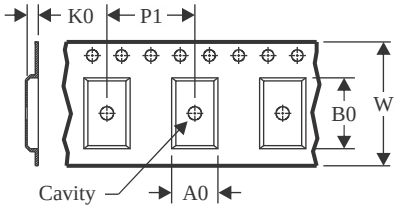
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

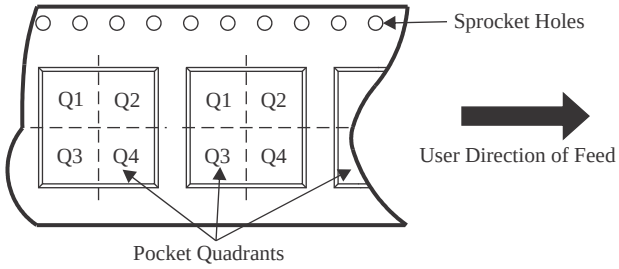



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

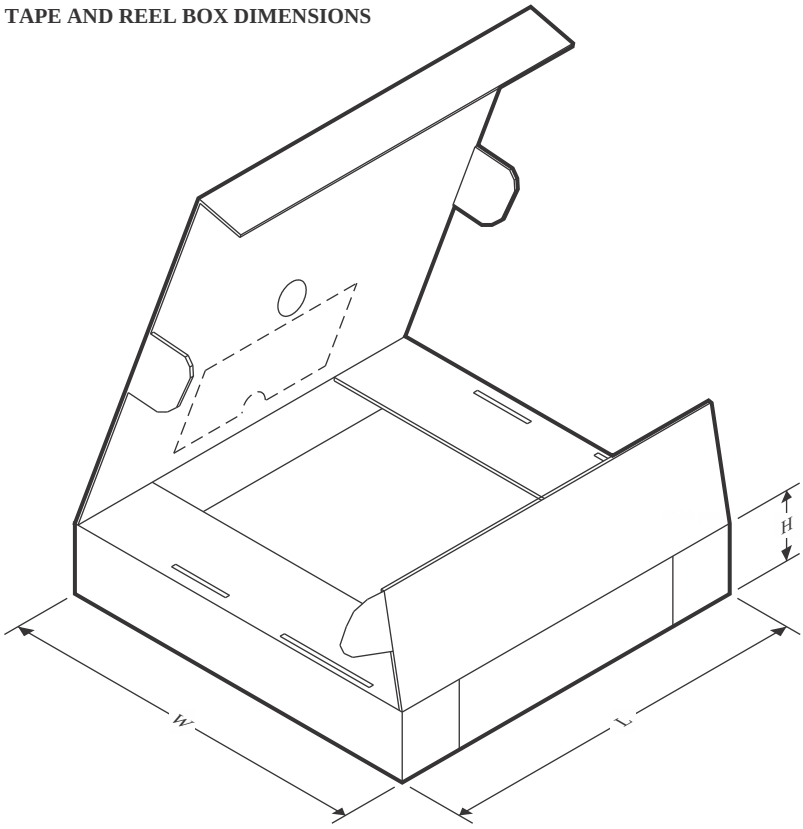
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

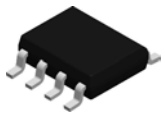
| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN65HVDA195QDRQ1 | SOIC | D | 8 | 2500 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN65HVDA195QDRQ1 | SOIC | D | 8 | 2500 | 356.0 | 356.0 | 35.0 |

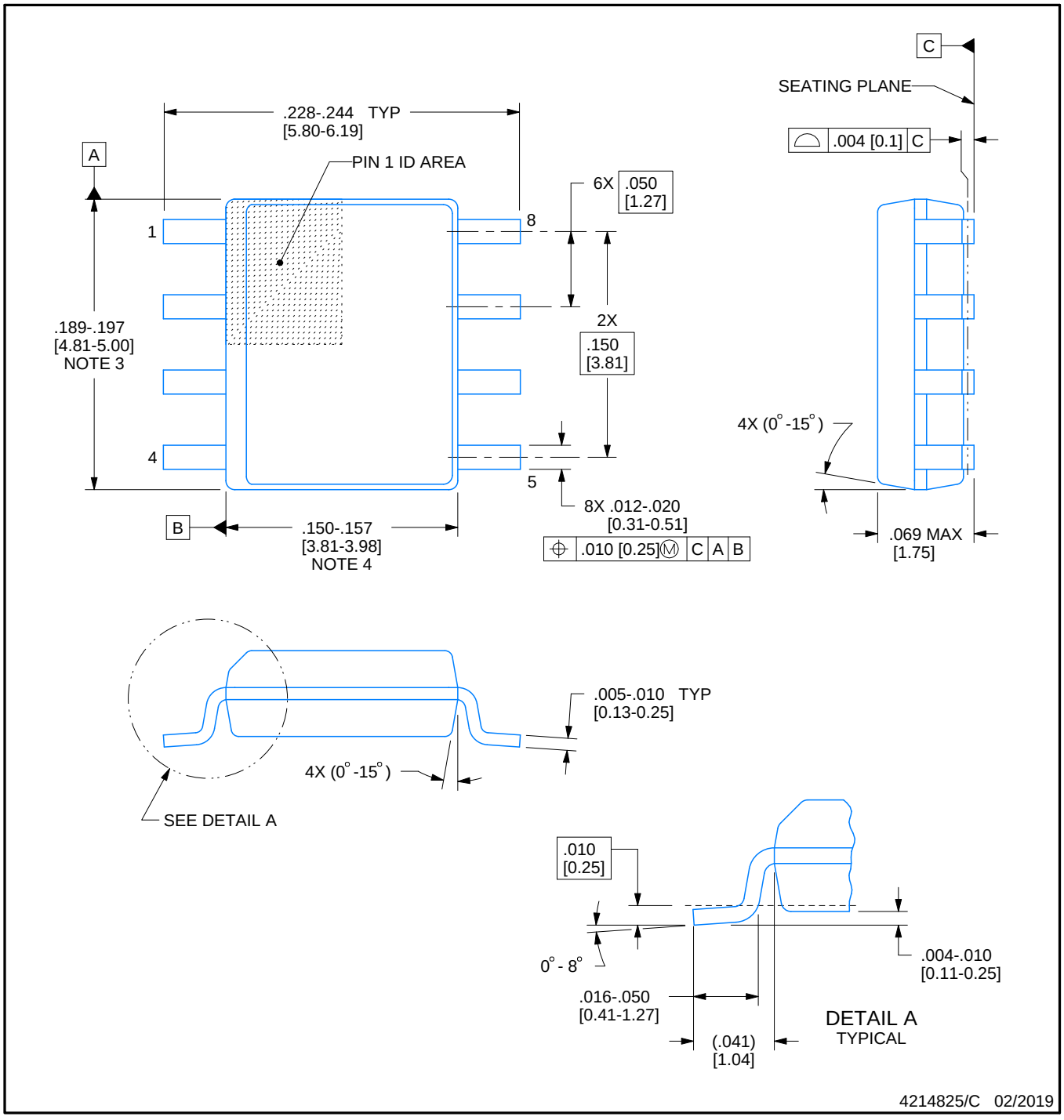


# PACKAGE OUTLINE

## D0008A

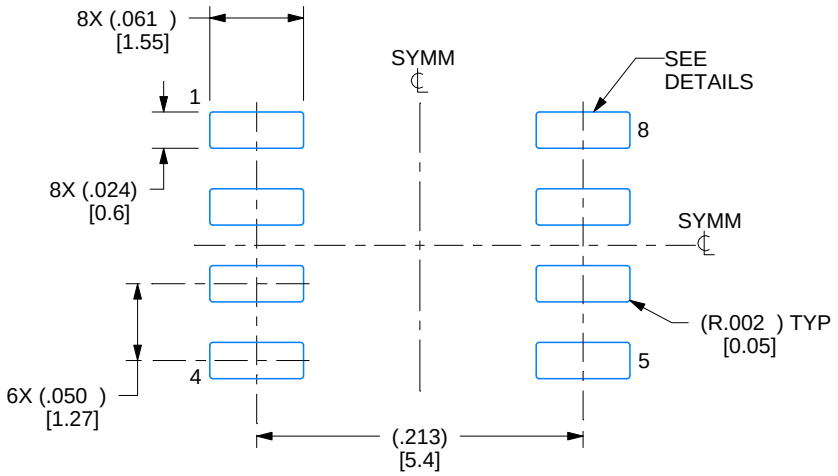
## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

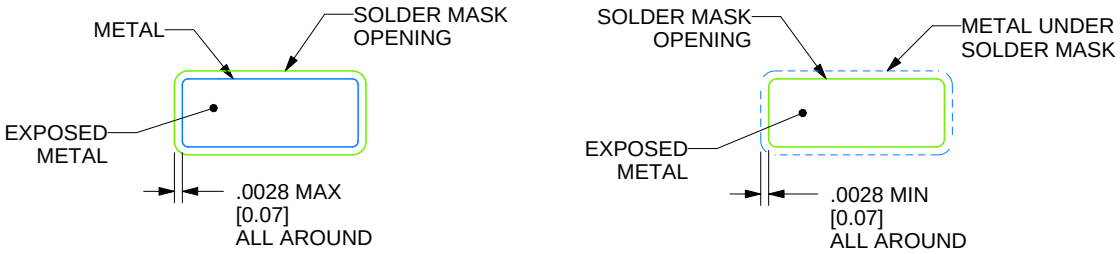



NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X




SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

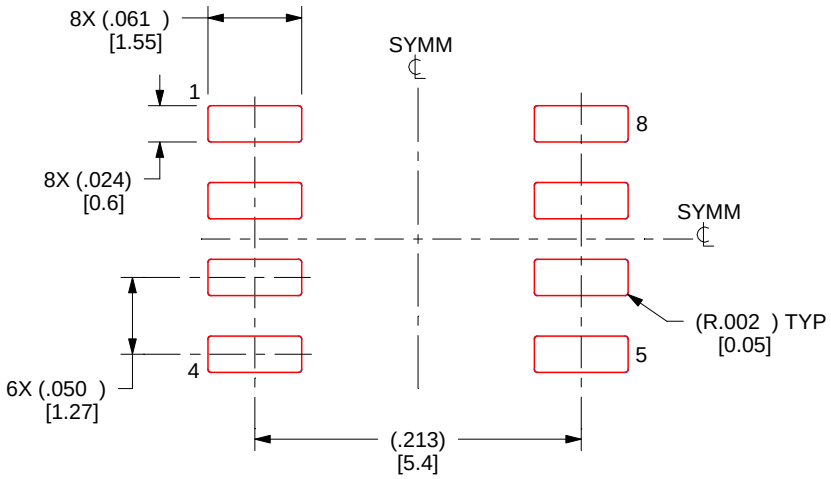
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

## D0008A

## SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT




SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

# 重要なお知らせと免責事項

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