

SN74AHC244-Q1 車載用、3 ステート出力のオクタール・バッファ / ドライバ

1 特長

- 車載アプリケーション向け認定済み
- EPIC™ (Enhanced-Performance Implanted CMOS) プロセス
- 動作範囲: $V_{CC} = 2V \sim 5.5V$

2 概要

SN74AHC244-Q1 には 1 つのインバータ・ゲートが搭載されています。このデバイスは、ブール関数 $Y = \bar{A}$ を実行します。

パッケージ情報

部品番号	パッケージ ⁽¹⁾	パッケージ・サイズ ⁽²⁾
SN74AHC244-Q1	DBV (SOT-23, 5)	2.90 × 1.60mm
	DCK (SOT-SC70, 5)	2.00 × 1.25mm

- (1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
- (2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



概略回路図



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3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (April 2008) to Revision B (August 2023)	Page
「パッケージ情報」表、「ピンの機能」表、「ESD 定格」表、「熱に関する情報」表、「デバイスの機能モード」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1

4 Function Table

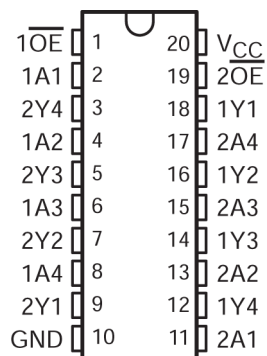


図 4-1. DW or PW Package (Top View)

表 4-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	1 $\overline{OE}$	I	Output Enable 1
2	1A1	I	1A1 Input
3	2Y4	O	2Y4 Output
4	1A2	I	1A2 Input
5	2Y3	O	2Y3 Output
6	1A3	I	1A3 Input
7	2Y2	O	2Y2 Output
8	1A4	I	1A4 Input
9	2Y1	O	2Y1 Output
10	GND	—	Ground pin
11	2A1	I	2A1 Input
12	1Y4	O	1Y4 Output
13	2A2	I	2A2 Input
14	1Y3	O	1Y3 Output
15	2A3	I	2A3 Input
16	1Y2	O	1Y2 Output
17	2A4	I	2A4 Input
18	1Y1	O	1Y1 Output
19	2 $\overline{OE}$	I	Output Enable 2
20	VCC	—	Power Pin

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range	-0.5	7	V
V _I ²	Input voltage range	-0.5	7	V
V _O ²	Output voltage range	-0.5	V _{CC} + 0.5	V
I _{IK}	Input clamp current	(V _I < 0)	-20	mA
I _{OK}	Output clamp current	(V _O < 0 or V _O > V _{CC})	±20	mA
I _O	Continuous output current	(V _O = 0 to V _{CC})	±25	mA
	Continuous current through V _{CC} or GND		±50	mA
T _{stg}	Storage temperature range	-65	150	°C

- (1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 ¹	All pins ±1500 V

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)¹

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2	5.5	V
V _{IH}	High-level input voltage	V _{CC} = 2 V	1.5	V
		V _{CC} = 3 V	2.1	
		V _{CC} = 5.5 V	3.85	
V _{IL}	Low-level input voltage	V _{CC} = 2 V	0.5	V
		V _{CC} = 3 V	0.9	
		V _{CC} = 5.5 V	1.65	
V _I	Input voltage	0	5.5	V
V _O	Output voltage	0	V _{CC}	V
I _{OH}	High-level output current	V _{CC} = 2 V	-50	μA
		V _{CC} = 3.3 V ± 0.3 V	-4	mA
		V _{CC} = 5 V ± 0.5 V	-8	
I _{OL}	Low-level output current	V _{CC} = 2 V	50	mA
		V _{CC} = 3.3 V ± 0.3 V	4	mA
		V _{CC} = 5 V ± 0.5 V	8	
Δt/Δv	Input transition rise or fall rate	V _{CC} = 3.3 V ± 0.3 V	100	ns/V
		V _{CC} = 5 V ± 0.5 V	20	
T _A	Operating free-air temperature	-40	125	°C

- (1) All unused inputs of the device must be held at V_{CC} or GND for proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

5.4 Thermal Information

THERMAL METRIC ⁽¹⁾		SN74AHC244-Q1		UNIT
		DW	PW	
		20 PINS	20 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	58	83	°C/W

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

5.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V _{OH}	I _{OH} = -50 μA	2 V	1.9	2		1.9		V
		3 V	2.9	3		2.9		
		4.5 V	4.4	4.5		4.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		
	I _{OH} = -8 mA	4.5 V	3.94			3.8		
V _{OL}	I _{OL} = 50 μA	2 V			0.1		0.1	V
		3 V			0.1		0.1	
		4.5 V			0.1		0.1	
	I _{OL} = 4 mA	3 V			0.36		0.5	
	I _{OL} = 8 mA	4.5 V			0.36		0.5	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1	μA
I _{OZ}	V _O = V _{CC} or GND, V _I ($\overline{\text{OE}}$) = V _{IL} or V _{IH}	5.5 V			±0.25		±2.5	μA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		40	μA
C _i	V _I = V _{CC} or GND	5 V			2	10		pF
C _o	V _O = V _{CC} or GND	5 V			3.5			pF

5.6 Switching Characteristics

over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T _A = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t _{PLH}	A	Y	C _L = 15 pF		5.8	8.4	1	10	ns
t _{PHL}					5.8	8.4	1	10	
t _{PZH}	$\overline{\text{OE}}$	Y	C _L = 15 pF		6.6	10.6	1	12.5	ns
t _{PZL}					6.6	10.6	1	12.5	
t _{PHZ}	$\overline{\text{OE}}$	Y	C _L = 15 pF		5	9.7	1	11	ns
t _{PLZ}					5	9.7	1	11	
t _{PLH}	A	Y	C _L = 50 pF		8.3	11.9	1	13.5	ns
t _{PHL}					8.3	11.9	1	13.5	
t _{PZH}	$\overline{\text{OE}}$	Y	C _L = 50 pF		9.1	14.1	1	16	ns
t _{PZL}					9.1	14.1	1	16	
t _{PHZ}	$\overline{\text{OE}}$	Y	C _L = 50 pF		10.3	14	1	16	ns
t _{PLZ}					10.3	14	1	16	

5.7 Switching Characteristics

over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see [Load Circuit and Voltage Waveforms](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			MIN	MAX	UNIT
				MIN	TYP	MAX			
t_{PLH}	A	Y	$C_L = 15\text{ pF}$	3.9	5.5		1	6.5	ns
t_{PHL}				3.9	5.5		1	6.5	
t_{PZH}	$\overline{OE}$	Y	$C_L = 15\text{ pF}$	4.7	7.3		1	8.5	ns
t_{PZL}				4.7	7.3		1	8.5	
t_{PHZ}	$\overline{OE}$	Y	$C_L = 15\text{ pF}$	5	7.2		1	8.5	ns
t_{PLZ}				5	7.2		1	8.5	
t_{PLH}	A	Y	$C_L = 50\text{ pF}$	5.4	7.5		1	8.5	ns
t_{PHL}				5.4	7.5		1	8.5	
t_{PZH}	$\overline{OE}$	Y	$C_L = 50\text{ pF}$	6.2	9.3		1	10.5	ns
t_{PZL}				6.2	9.3		1	10.5	
t_{PHZ}	$\overline{OE}$	Y	$C_L = 50\text{ pF}$	6.7	9.2		1	10.5	ns
t_{PLZ}				6.7	9.2		1	10.5	

5.8 Noise Characteristics

$V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ ⁽¹⁾

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}		0.5		V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}		-0.2		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}		4.8		V
$V_{IH(D)}$	High-level dynamic input voltage	3.5			V
$V_{IL(D)}$	Low-level dynamic input voltage			1.5	V

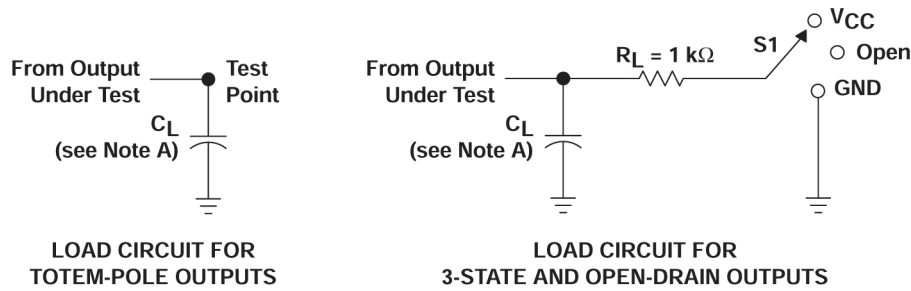
(1) Characteristics are for surface-mount packages only.

5.9 Operating Characteristics

$V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

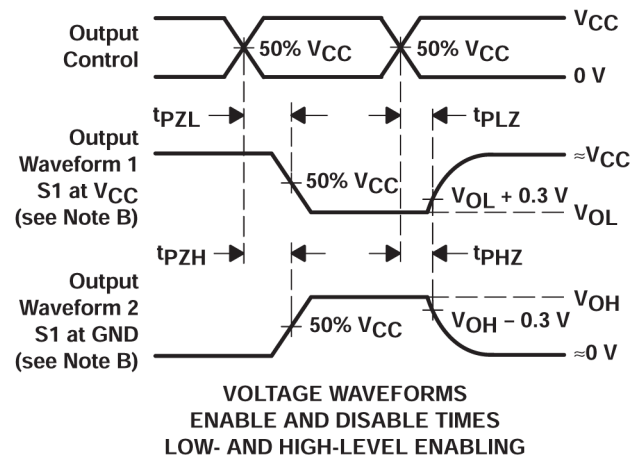
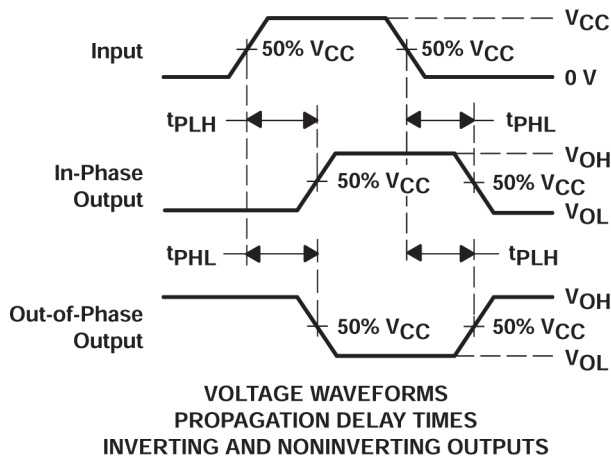
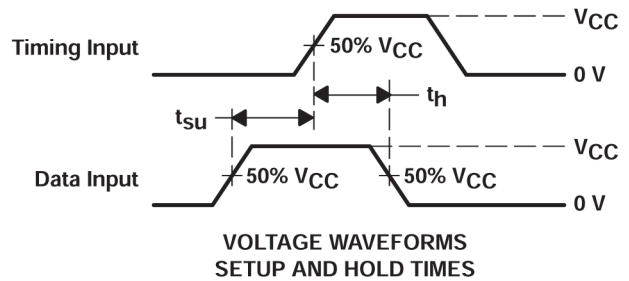
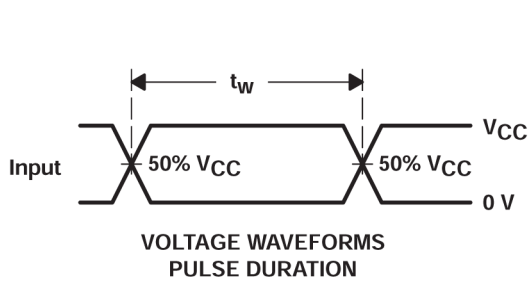
PARAMETER		TEST CONDITIONS		TYP	UNIT
C_{pd}	Power dissipation capacitance	No load,	$f = 1\text{ MHz}$	8.6	pF

6 Parameter Measurement Information



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS



- A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
D. The outputs are measured one at a time with one input transition per measurement.

6-1. Load Circuit and Voltage Waveforms

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{CC}
t_{PHZ}/t_{PZH}	GND
Open Drain	V_{CC}

7 Detailed Description

7.1 Overview

This octal buffer/driver is designed specifically to improve the performance and density of 3-state memory-address drivers, clock drivers, and bus-oriented receivers and transmitters.

The SN74AHC244 is organized as two 4-bit buffers/line drivers with separate output-enable ($\overline{OE}$) inputs. When $\overline{OE}$ is low, the device passes data from the A inputs to the Y outputs. When $\overline{OE}$ is high, the outputs are in the high-impedance state.

For the specified high-impedance state during power up or power down, $\overline{OE}$ must be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

7.2 Functional Block Diagram

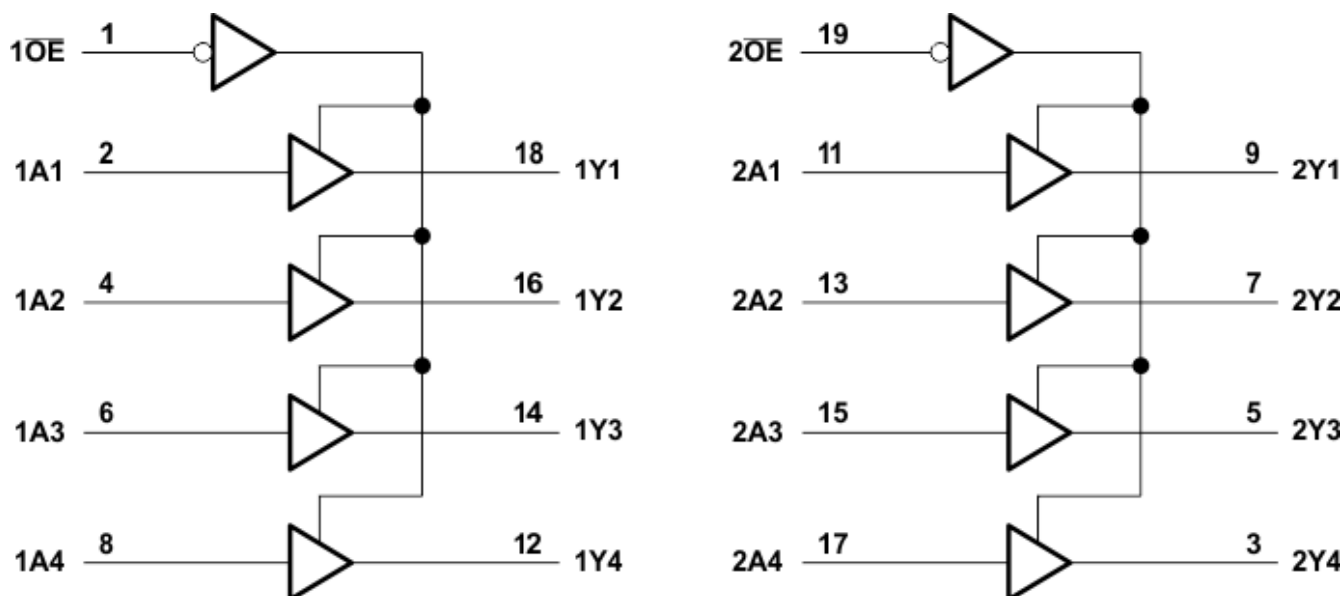
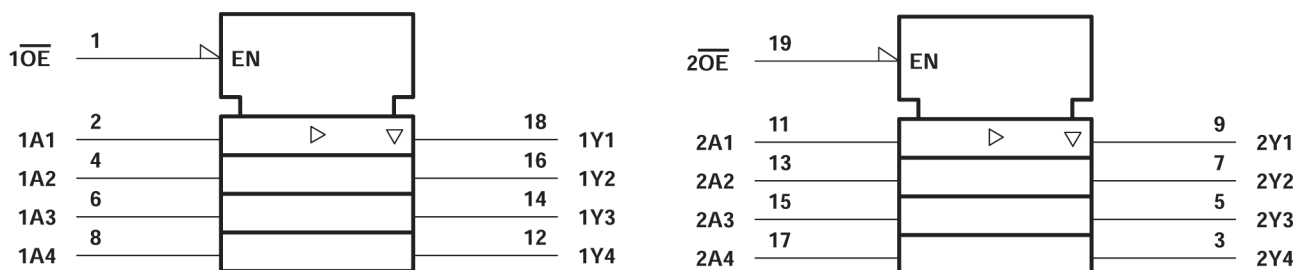


图 7-1. Logic Diagram (Positive Logic)



This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

图 7-2. Logic Symbol

7.3 Device Functional Modes

**表 7-1. (Each 4-Bit Buffer/
Driver)**

INPUTS		OUTPUT Y
OE	A	
L	H	H
L	L	L
H	X	Z

8 Device and Documentation Support

8.1 Documentation Support

8.1.1 Related Documentation

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 8-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN74AHC244-Q1	Click here	Click here	Click here	Click here	Click here

8.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、[ti.com](#) のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

8.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

8.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

8.5 静電気放電に関する注意事項



この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.6 用語集

[テキサス・インスツルメンツ用語集](#)

この用語集には、用語や略語の一覧および定義が記載されています。

9 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74AHC244QDWRQ1	ACTIVE	SOIC	DW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC244Q1	Samples
SN74AHC244QPWRG4Q1	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC244Q1	Samples
SN74AHC244QPWRQ1	ACTIVE	TSSOP	PW	20	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	AHC244Q1	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN74AHC244-Q1 :

- Catalog : [SN74AHC244](#)
- Enhanced Product : [SN74AHC244-EP](#)
- Military : [SN54AHC244](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Enhanced Product - Supports Defense, Aerospace and Medical Applications
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC244QDWRQ1	SOIC	DW	20	2000	330.0	24.4	10.8	13.3	2.7	12.0	24.0	Q1
SN74AHC244QPWRG4Q1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.1	1.6	8.0	16.0	Q1
SN74AHC244QPWRQ1	TSSOP	PW	20	2000	330.0	16.4	6.95	7.0	1.4	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC244QDWRQ1	SOIC	DW	20	2000	367.0	367.0	45.0
SN74AHC244QPWRG4Q1	TSSOP	PW	20	2000	356.0	356.0	35.0
SN74AHC244QPWRQ1	TSSOP	PW	20	2000	356.0	356.0	35.0



TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



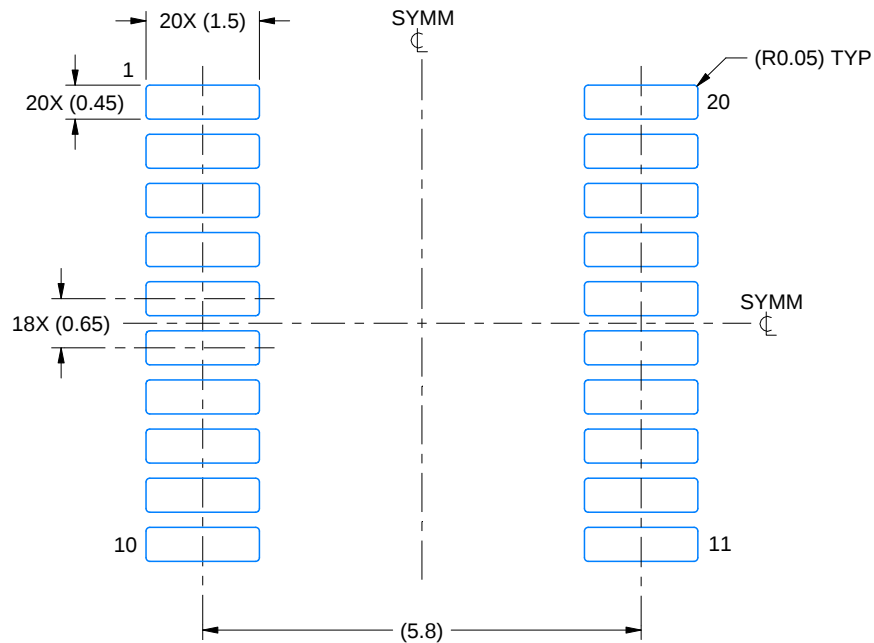
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

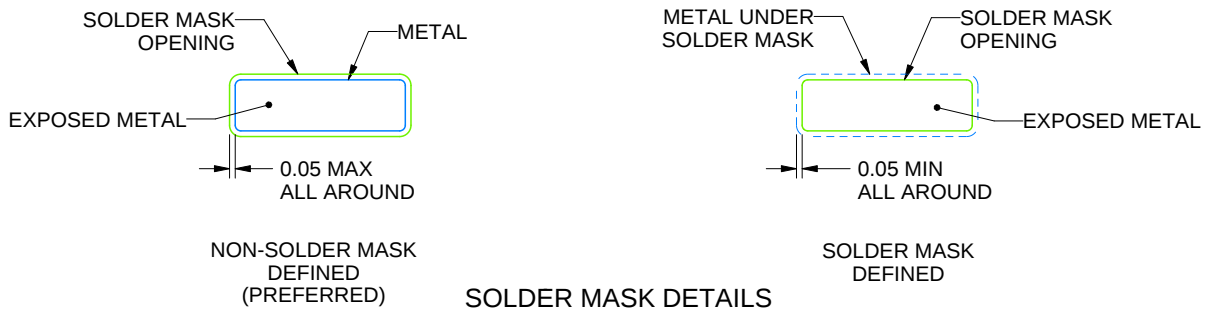
PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220206/A 02/2017

NOTES: (continued)

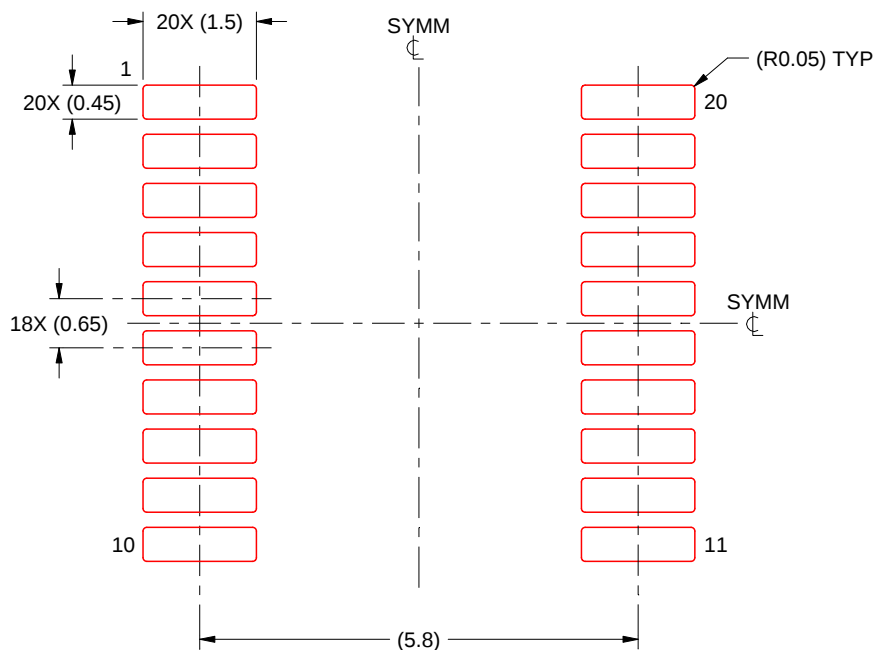
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0020A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

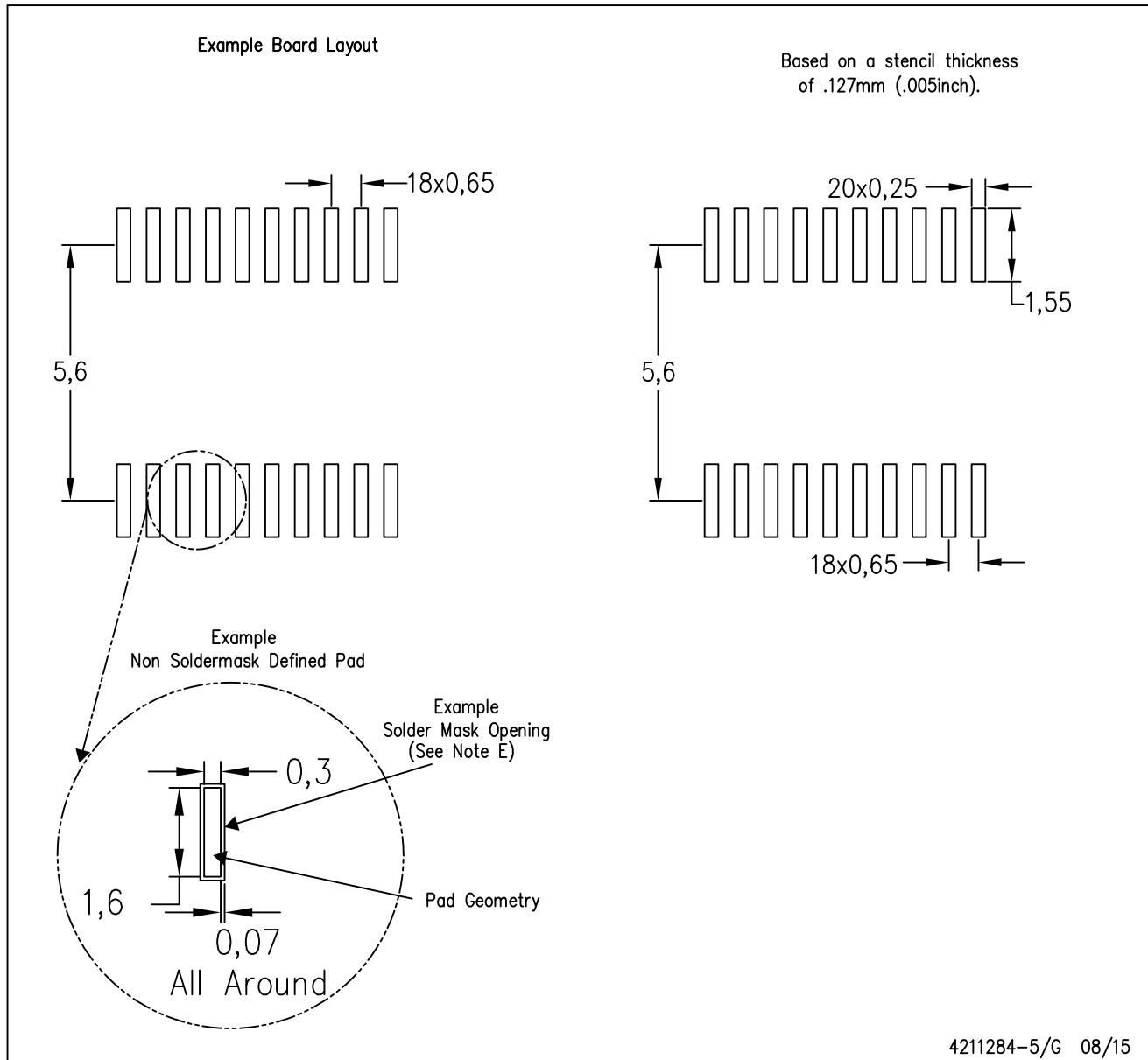
4220206/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PW (R-PDSO-G20)

PLASTIC SMALL OUTLINE



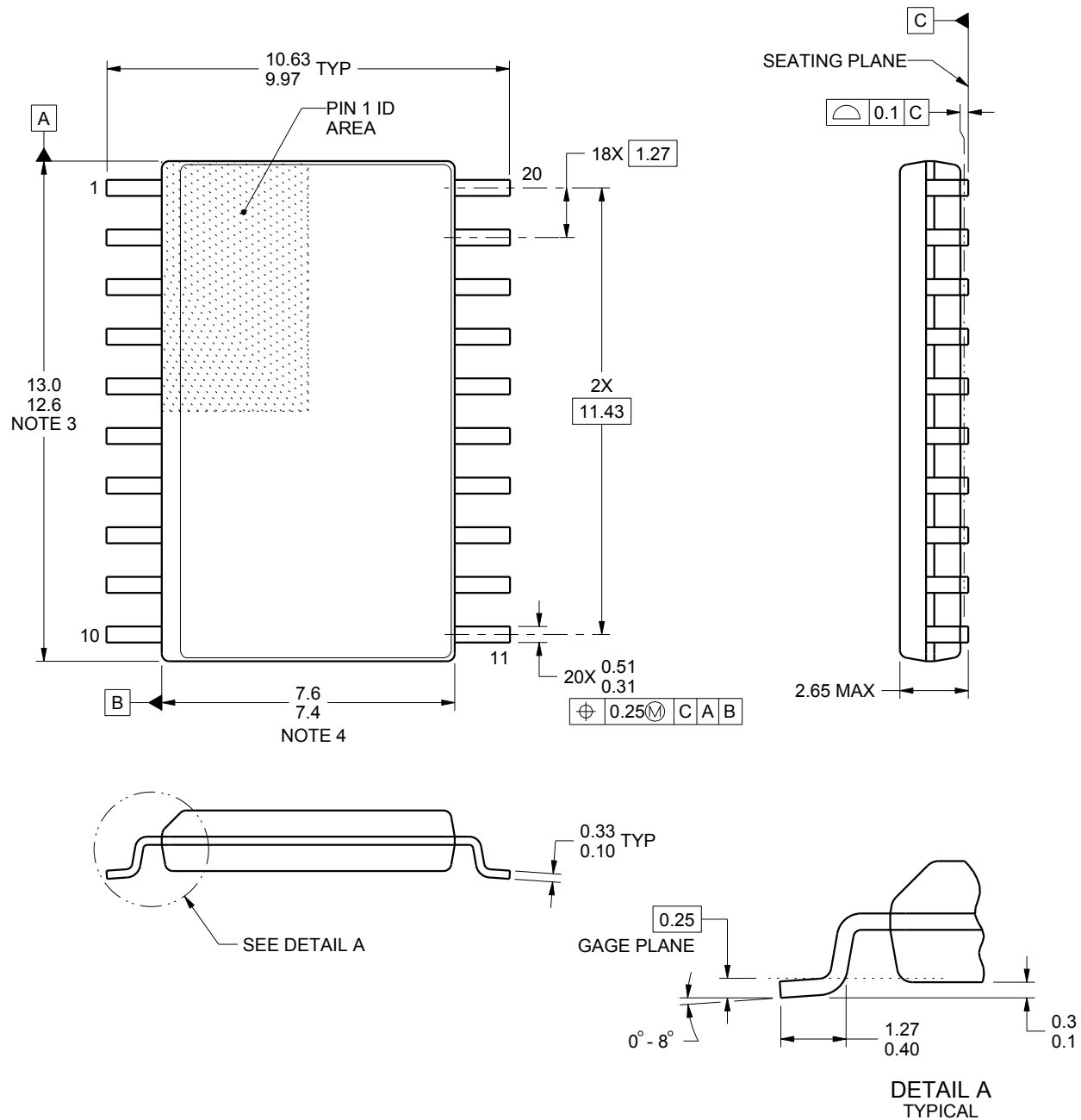
- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DW0020A

PACKAGE OUTLINE

SOIC - 2.65 mm max height

SOIC



4220724/A 05/2016

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.

EXAMPLE BOARD LAYOUT

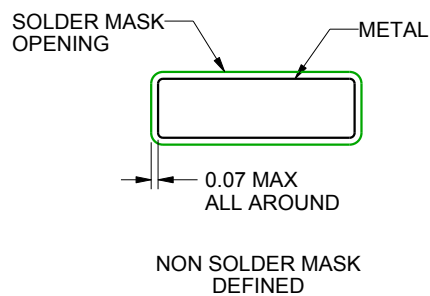
DW0020A

SOIC - 2.65 mm max height

SOIC



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DW0020A

SOIC - 2.65 mm max height

SOIC



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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