TEXAS INSTRUMENTS
SN74AVC4T774
JAJSKE9G – FEBRUARY 2008 – REVISED MAY 2021

SN74AVC4T774 構成可能な電圧レベル・シフト機能と 3 ステート出力 (独立した方向制御入力付き) を備えた 4 ビット、デュアル電源バス・トランシーバ

1 特長

- 各チャネルに独立した DIR 制御入力
- V_{CCA} 電圧基準の制御入力 V_{IH}/V_{IL} レベル
- 完全に構成可能なデュアル・レール設計により、1.1V ～3.6V の電源電圧の全範囲にわたって各ポートが動作可能
- 4.6V 許容の I/O
- I_{off} により部分的パワーダウン・モード動作をサポート
- データ・レート (標準値)
  - 380Mbps (1.8V から 3.3V に変換)
  - 200Mbps (1.8V 未満から 3.3V に変換)
  - 200Mbps (2.5V または 1.8V に変換)
  - 150Mbps (1.5V に変換)
  - 100Mbps (1.2V に変換)
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- 次の水準を上回る ESD 保護 (JESD 22 に準拠してテスト済み)
  - ±8000V、人体モデル (A114-A)
  - 250V、マシン・モデル (A115-A)
  - ±1500V、デバイス帯電モデル (C101)

2 アプリケーション

- パーソナル・エレクトロニクス
- 産業用
- エンタープライズ
- 通信機器

3 概要

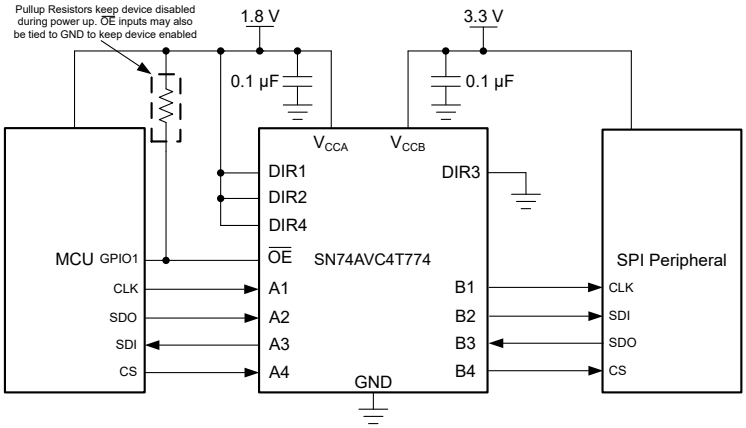
この 4 ビット非反転バス・トランシーバは、設定可能な 2 本の独立した電源レールを使用します。A ポートは V_{CCA} に追従する設計で、V_{CCA} は 1.1V～3.6V の電源電圧に対応します。B ポートは V_{CCB} に追従する設計で、V_{CCB} は 1.1V ～ 3.6V の電源電圧に対応します。SN74AVC4T774 は、V_{CCA} と V_{CCB} を 1.4V～3.6V に設定した状態で動作するよう最適化されています。本デバイスは 1.2V の V_{CCA} と V_{CCB} でも動作します。したがって、1.2V、1.5V、1.8V、2.5V、3.3V のいずれかの電圧ノード間で自在な低電圧双方向変換が可能です。

SN74AVC4T774 は、データ・バス間の非同期通信用に設計されています。方向制御 (DIR) 入力および出力イネーブル ($\overline{OE}$) 入力のロジック・レベルに応じて、B ポート出力もしくは A ポート出力のいずれかがアクティブになるか、または、両方の出力ポートが高インピーダンス・モードになります。本デバイスは、B ポート出力がアクティブになったた場合、A バスから B バスにデータを転送し、A ポート出力がアクティブになった場合、B バスから A バスにデータを転送します。A ポートと B ポートの入力回路はどちらも常にアクティブであるため、これらのポートには論理 HIGH または LOW レベルを印加して、I_{CC} と I_{CCZ} が過剰に流れないようにする必要があります。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
SN74AVC4T774PW	TSSOP (16)	5.00mm × 4.40mm
SN74AVC4T774RGY	VQFN (16)	4.00mm × 3.50mm
SN74AVC4T774RSV	UQFN (16)	2.60mm × 1.80mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



代表的なアプリケーション回路図

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision F (November 2020) to Revision G (May 2021) — **Page**

- 「*概要*」セクションの「*代表的なアプリケーション回路図*」を更新 ... 1
- Updated the *Typical Application of the SN74AVC4T774* figure in the *Typical Application* section ... 16

Changes from Revision E (October 2017) to Revision F (November 2020) — **Page**

- 文書全体にわたって表、図、相互参照の採番方法を更新 ... 1
- V_{CCA} and V_{CCB} supply voltage min in *Recommended Operating Conditions* table expanded down to 1.1 V ... 6

Changes from Revision D (January 2015) to Revision E (October 2017) — **Page**

Changes from Revision C (December 2014) to Revision D (January 2015) — **Page**

- Changed Pin Functions table order for Pins B4, B3, B2 and B1 ... 4

Changes from Revision B (May 2008) to Revision C (December 2014) — **Page**

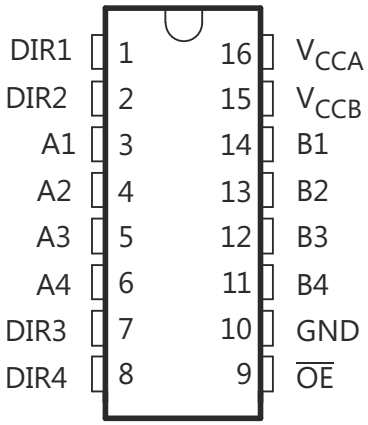
- 「*ピン構成および機能*」セクション、「*ESD 定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1

5 Description (continued)

The SN74AVC4T774 is designed so that the control pins (DIR1, DIR2, DIR3, DIR4, and $\overline{OE}$) are supplied by V_{CCA}. This device is fully specified for partial-power-down applications using I_{off}. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down. The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, then both ports are in the high-impedance state.

To ensure the high-impedance state during power-up or power-down, $\overline{OE}$ should be tied to V_{CCA} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver. Since this device has CMOS inputs, it is very important to not allow them to float. If the inputs are not driven to either a high V_{CC} state, or a low-GND state, an undesirable larger than expected I_{CC} current may result. Since the input voltage settlement is governed by many factors (for example, capacitance, board-layout, package inductance, surrounding conditions, and so forth), ensuring that they these inputs are kept out of erroneous switching states and tying them to either a high or a low level minimizes the leakage-current.

6 Pin Configuration and Functions



A. Shown for a single channel

図 6-1. PW Package 16-Pin TSSOP Top View

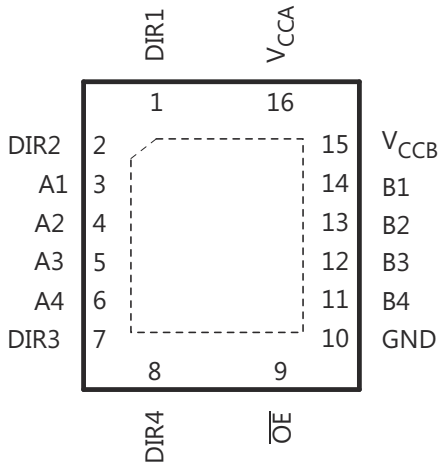


図 6-2. RGY Package 16-Pin VQFN Top View

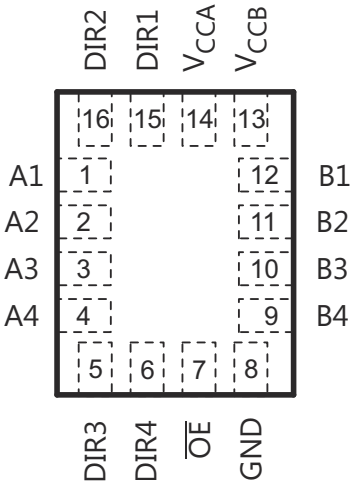


図 6-3. RSV Package 16-Pin UQFN Top View

表 6-1. Pin Functions

PIN			I/O	DESCRIPTION
NAME	PW RGY	RSV		
DIR1	1	15	I	Direction-control input referenced to V_{CCA}, controls signal flow for the first (A1/B1) I/O channels.
DIR2	2	16	I	Direction-control input referenced to V_{CCA} , controls signal flow for the second (A2/B2) I/O channels.
A1	3	1	I/O	Input/output A1. Referenced to V_{CCA}.
A2	4	2	I/O	Input/output A2. Referenced to V_{CCA}.
A3	5	3	I/O	Input/output A3. Referenced to V_{CCA}.
A4	6	4	I/O	Input/output A4. Referenced to V_{CCA}.
DIR3	7	5	I	Direction-control input referenced to V_{CCA} , controls signal flow for the third (A3/B3) I/O channels.
DIR4	8	6	I	Direction-control input referenced to V_{CCA} , controls signal flow for the fourth (A4/B4) I/O channels.
$\overline{OE}$	9	7	I	3-state output-mode enables. Pull $\overline{OE}$ high to place all outputs in 3-state mode. Referenced to V_{CCA}.
GND	10	8	—	Ground.
B4	11	9	I/O	Input/output B4. Referenced to V_{CCB}.
B3	12	10	I/O	Input/output B3. Referenced to V_{CCB}.
B2	13	11	I/O	Input/output B2. Referenced to V_{CCB}.
B1	14	12	I/O	Input/output B1. Referenced to V_{CCB}.
V_{CCB}	15	13	—	B-port supply voltage. 1.1 V ≤ V_{CCB} ≤ 3.6 V.
V_{CCA}	16	14	—	A-port supply voltage. 1.1 V ≤ V_{CCA} ≤ 3.6 V.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
VCCA VCCB	Supply voltage		–0.5	4.6	V
VI	Input voltage range(2)	I/O ports (A port)	–0.5	4.6	V
		I/O ports (B port)	–0.5	4.6	
		Control inputs	–0.5	4.6	
VO	Voltage range applied to any output in the high-impedance or power-off state(2)	A port	–0.5	4.6	V
		B port	–0.5	4.6	
VO	Voltage range applied to any output in the high or low state(2) (3)	A port	–0.5	VCCA + 0.5	V
		B port	–0.5	VCCB + 0.5	
IIK	Input clamp current	VI< 0		–50	mA
IOK	Output clamp current	VO < 0		–50	mA
IO	Continuous output current			±50	mA
	Continuous current through VCCA, VCCB, or GND			±100	mA
TJ	Junction temperature			150	°C
Tstg	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±8000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	
		Machine model (A115-A)	250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{CCA}	Supply voltage				1.1	3.6	V
V_{CCB}	Supply voltage				1.1	3.6	V
V_{IH}	High-level input voltage	Data inputs(4)	1.1 V to 1.95 V		V_{CCI} × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	Data inputs(4)	1.1 V to 1.95 V			V_{CCI} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	

7.3 Recommended Operating Conditions (continued)

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

			V_{CCI}	V_{CCO}	MIN	MAX	UNIT
V_{IH}	High-level input voltage	Control Inputs (referenced to V_{CCA}) (5) (DIRx, $\overline{OE}$)	1.1 V to 1.95 V		V_{CCA} × 0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V_{IL}	Low-level input voltage	Control Inputs (referenced to V_{CCA}) (5) (DIRx, $\overline{OE}$)	1.1 V to 1.95 V			V_{CCA} × 0.35	V
			1.95 V to 2.7 V			0.7	
			2.7 V to 3.6 V			0.8	
V_I	Input voltage				0	3.6	V
V_O	Output voltage	Active state			0	V_{CCO}	V
		3-state			0	3.6	
I_{OH}	High-level output current			1.1 V to 1.3 V		–3	mA
				1.4 V to 1.6 V		–6	
				1.65 V to 1.95 V		–8	
				2.3 V to 2.7 V		–9	
				3 V to 3.6 V		–12	
I_{OL}	Low-level output current			1.1 V to 1.3 V		3	mA
				1.4 V to 1.6 V		6	
				1.65 V to 1.95 V		8	
				2.3 V to 2.7 V		9	
				3 V to 3.6 V		12	
Δt/Δv	Input transition rise or fall rate					5	ns/V
T_A	Operating free-air temperature				–40	85	°C

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs.
(4) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCI} × 0.7 V, V_{IL} max = V_{CCI} × 0.3 V
(5) For V_{CCI} values not specified in the data sheet, V_{IH} min = V_{CCA} × 0.7 V, V_{IL} max = V_{CCA} × 0.3 V

7.4 Thermal Information

THERMAL METRIC(1)		SN74AVC4T774			UNIT
		PW	RGY	RSV	
		16 PINS			
$R_{\Theta JA}$	Junction-to-ambient thermal resistance	118.2	37.7	139.2	°C/W
$R_{\Theta JC(top)}$	Junction-to-case (top) thermal resistance	52.8	56.1	64.9	
$R_{\Theta JB}$	Junction-to-board thermal resistance	63.3	15.9	67.7	
ψ_{JT}	Junction-to-top characterization parameter	8.8	0.5	1.7	
ψ_{JB}	Junction-to-board characterization parameter	62.7	16.1	67.4	
$R_{\Theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	N/A	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report.

7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)(1) (2) (3)

PARAMETER		TEST CONDITIONS		V_{CCA}	V_{CCB}	TA = 25°C			–40°C to 85°C			UNIT
						MIN	TYP	MAX	MIN	TYP	MAX	
V_{OH}		I_{OH} = –100 µA	$V_I = V_{IH}$	1.1 V to 3.6 V	1.1 V to 3.6 V				V_{CCO} – 0.2			V
		I_{OH} = –3 mA		1.2 V	1.2 V		0.95					
		I_{OH} = –6 mA		1.4 V	1.4 V				1.05			
		I_{OH} = –8 mA		1.65 V	1.65 V				1.2			
		I_{OH} = –9 mA		2.3 V	2.3 V				1.75			
		I_{OH} = –12 mA		3 V	3 V				2.3			
V_{OL}		I_{OL} = 100 µA	$V_I = V_{IL}$	1.1 V to 3.6 V	1.1 V to 3.6 V						0.2	V
		I_{OL} = 3 mA		1.2 V	1.2 V		0.25					
		I_{OL} = 6 mA		1.4 V	1.4 V						0.35	
		I_{OL} = 8 mA		1.65 V	1.65 V						0.45	
		I_{OL} = 9 mA		2.3 V	2.3 V						0.55	
		I_{OL} = 12 mA		3 V	3 V						0.7	
I_I	Control inputs	$V_I = V_{CCA}$ or GND		1.1 V to 3.6 V	1.1 V to 3.6 V		±0.025	±0.25			±1	µA
I_{off}	A or B port	V_I or V_O = 0 to 3.6 V		0 V	0 V to 3.6 V		±0.1	±1			±5	µA
				0 V to 3.6 V	0 V		±0.1	±1			±5	
I_{OZ}	A or B port	$V_O = V_{CCO}$ or GND, VI = V_{CCI} or GND, $\overline{OE}$ = V_{IH}		3.6 V	3.6 V		±0.5	±2.5			±5	µA
I_{CCA}		$V_I = V_{CCI}$ or GND, I_O = 0		1.1 V to 3.6 V	1.1 V to 3.6 V						8	µA
				0 V	0 V to 3.6 V				–2			
				0 V to 3.6 V	0 V						8	
I_{CCB}		$V_I = V_{CCI}$ or GND, I_O = 0		1.1 V to 3.6 V	1.1 V to 3.6 V						8	µA
				0 V	0 V to 3.6 V						8	
				0 V to 3.6 V	0 V				–2			
I_{CCA} + I_{CCB}		$V_I = V_{CCI}$ or GND, I_O = 0		1.1 V to 3.6 V	1.1 V to 3.6 V						16	µA
C_i	Control inputs	V_I = 3.3 V or GND		3.3 V	3.3 V		2.5				4.5	pF
C_{io}	A or B port	V_O = 3.3 V or GND		3.3 V	3.3 V		5				7	pF

(1) V_{CCI} is the V_{CC} associated with the input port.
(2) V_{CCO} is the V_{CC} associated with the output port.
(3) All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, Implications of Slow or Floating CMOS Inputs.

7.6 Switching Characteristics: VCCA = 1.2 V ± 0.1 V

See Figure 8-1 and Table 8-1 for test circuit and loading. See Figure 8-2, Figure 8-3, and Figure 8-4 for measurement waveforms.

PARAMETER	PARAMETER	FROM	TO	Test Conditions	V_{CCB} = 1.2 V ± 0.1 V		V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	t_{PLH}	A	B	-40°C to 85°C	2	7.5	1.5	5.5	1	4.5	1	4	0.5	4	ns
t_{PHL}	t_{PHL}				1.5	5.5	1	4	1	4	0.5	4.5	0.5	6	
t_{PLH}	t_{PLH}	B	A		2	7	1.5	6.5	1	6	1	6	1	6	
t_{PHL}	t_{PHL}				1.5	5.5	1	5	1	4.5	0.5	4	0.5	4	
t_{PZH}	t_{PZH}	$\overline{OE}$	A		2.5	8	2	8	1	8	1	8	1	8.5	
t_{PZL}	t_{PZL}				2.5	9	2	9	1.5	9	1	9	1	9	
t_{PZH}	t_{PZH}	$\overline{OE}$	B		2	7.5	1.5	5.5	1	6.5	1	9.5	0.5	30	
t_{PZL}	t_{PZL}				2.5	8.5	1.5	6.5	1	7	1	8.5	0.5	24	
t_{PHZ}	t_{PHZ}	$\overline{OE}$	A		3	6.5	2	6.5	2	6.5	1.5	6.5	2	6.5	
t_{PLZ}	t_{PLZ}				3	6.5	2.5	6.5	2.5	6.5	2	6.5	2	6.5	
t_{PHZ}	t_{PHZ}	$\overline{OE}$	B		3	6	2.5	5.5	2	6	1.5	5	2	6.5	
t_{PLZ}	t_{PLZ}				3	6	2.5	5.5	2.5	5.5	1.5	5	2	6	

7.7 Switching Characteristics: VCCA = 1.5 V ± 0.1 V

See Figure 8-1 and Table 8-1 for test circuit and loading. See Figure 8-2, Figure 8-3, and Figure 8-4 for measurement waveforms.

PARAMETER	PARAMETER	FROM	TO	V_{CCB} = 1.2 V ± 0.1 V		V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	t_{PLH}	A	B	1.5	6.5	0.3	6.3	0.3	5.2	0.4	4.2	0.4	4.2	ns
t_{PHL}	t_{PHL}			1.5	4.5	0.3	6.3	0.3	5.2	0.4	4.2	0.4	4.2	
t_{PLH}	t_{PLH}	B	A	1.5	5	0.7	6.3	0.5	6	0.4	5.7	0.3	5.6	ns
t_{PHL}	t_{PHL}			1.5	4	0.7	6.3	0.5	6	0.4	5.7	0.3	5.6	
t_{PZH}	t_{PZH}	$\overline{OE}$	A	1.5	5	1.4	9.6	1.1	9.5	0.7	9.4	0.4	9.4	ns
t_{PZL}	t_{PZL}			2	5.5	1.4	9.6	1.1	9.5	0.7	9.4	0.4	9.4	
t_{PZH}	t_{PZH}	$\overline{OE}$	B	2	6.5	1.4	9.6	1.1	7.7	0.9	5.8	0.9	5.6	ns
t_{PZL}	t_{PZL}			2	7.5	1.4	9.6	1.1	7.7	0.9	5.8	0.9	5.6	
t_{PHZ}	t_{PHZ}	$\overline{OE}$	A	2	5	1.8	10.2	1.5	10.2	1.3	10.2	1.6	10.2	ns
t_{PLZ}	t_{PLZ}			2.5	4.5	1.8	10.2	1.5	10.2	1.3	10.2	1.6	10.2	
t_{PHZ}	t_{PHZ}	$\overline{OE}$	B	3	5.5	1.9	10.3	1.9	9.1	1.4	7.4	1.2	7.6	ns
t_{PLZ}	t_{PLZ}			3	5.5	1.9	10.3	1.9	9.1	1.4	7.4	1.2	7.6	

7.8 Switching Characteristics: VCCA = 1.8 V ± 0.15 V

See Figure 8-1 and Table 8-1 for test circuit and loading. See Figure 8-2, Figure 8-3, and Figure 8-4 for measurement waveforms.

PARAMETER	PARAMETER	FROM	TO	Test Conditions	V_{CCB} = 1.2 V ± 0.1 V		V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
					MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	t_{PLH}	A	B	-40°C to 85°C	1.5	6.5	0.3	6.3	0.3	5.2	0.4	4.2	0.4	4.2	ns
t_{PHL}	t_{PHL}				1	4.5	0.3	6.3	0.3	5.2	0.4	4.2	0.4	4.2	
t_{PLH}	t_{PLH}	B	A		1.5	6	0.7	6.3	0.5	6	0.4	5.7	0.3	5.6	
t_{PHL}	t_{PHL}				1	4.5	0.7	6.3	0.5	6	0.4	5.7	0.3	5.6	
t_{PZH}	t_{PZH}	$\overline{OE}$	A		1	6.5	1.4	9.6	1.1	9.5	0.7	9.4	0.4	9.4	
t_{PZL}	t_{PZL}				1.5	7.5	1.4	9.6	1.1	9.5	0.7	9.4	0.4	9.4	
t_{PZH}	t_{PZH}	$\overline{OE}$	B		2	6	1.4	9.6	1.1	7.7	0.9	5.8	0.9	5.6	
t_{PZL}	t_{PZL}				2	7	1.4	9.6	1.1	7.7	0.9	5.8	0.9	5.6	
t_{PHZ}	t_{PHZ}	$\overline{OE}$	A		2	6	1.8	10.2	1.5	10.2	1.3	10.2	1.6	10.2	
t_{PLZ}	t_{PLZ}				2.5	5.5	1.8	10.2	1.5	10.2	1.3	10.2	1.6	10.2	
t_{PHZ}	t_{PHZ}	$\overline{OE}$	B		2.5	5	1.9	10.3	1.9	9.1	1.4	7.4	1.2	7.6	
t_{PLZ}	t_{PLZ}				2.5	5	1.9	10.3	1.9	9.1	1.4	7.4	1.2	7.6	

7.9 Switching Characteristics: VCCA = 2.5 V ± 0.2 V

See Figure 8-1 and Table 8-1 for test circuit and loading. See Figure 8-2, Figure 8-3, and Figure 8-4 for measurement waveforms.

PARAMETER	PARAMETER	FROM	TO	V_{CCB} = 1.2 V ± 0.1 V		V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	t_{PLH}	A	B	1.5	6.5	0.1	5.7	0.1	4.6	0.2	3.5	0.1	3.6	ns
t_{PHL}	t_{PHL}			1	4.5	0.1	5.7	0.1	4.6	0.2	3.5	0.1	3.6	
t_{PLH}	t_{PLH}	B	A	1.5	4	0.6	4.2	0.4	3.9	0.2	3.4	0.2	3.3	ns
t_{PHL}	t_{PHL}			1	5	0.6	4.2	0.4	3.9	0.2	3.4	0.2	3.3	
t_{PZH}	t_{PZH}	$\overline{OE}$	A	1	2.5	0.7	6.5	0.7	5.2	0.6	4.8	0.4	4.8	ns
t_{PZL}	t_{PZL}			1	3	0.7	6.5	0.7	5.2	0.6	4.8	0.4	4.8	
t_{PZH}	t_{PZH}	$\overline{OE}$	B	1.5	6	0.9	8.8	0.8	7	0.6	4.8	0.6	4	ns
t_{PZL}	t_{PZL}			2	7	0.9	8.8	0.8	7	0.6	4.8	0.6	4	
t_{PHZ}	t_{PHZ}	$\overline{OE}$	A	1.5	3.5	1	8.4	1	8.4	1	6.2	1	6.6	ns
t_{PLZ}	t_{PLZ}			2	3.5	1	8.4	1	8.4	1	6.2	1	6.6	
t_{PHZ}	t_{PHZ}	$\overline{OE}$	B	2	5	1.5	9.4	1.3	8.2	1.1	6.2	0.9	5.2	ns
t_{PLZ}	t_{PLZ}			2.5	5	1.5	9.4	1.3	8.2	1.1	6.2	0.9	5.2	

7.10 Switching Characteristics: VCCA = 3.3 V ± 0.3 V

See Figure 8-1 and Table 8-1 for test circuit and loading. See Figure 8-2, Figure 8-3, and Figure 8-4 for measurement waveforms.

PARAMETER	PARAMETER	FROM	TO	V_{CCB} = 1.2 V ± 0.1 V		V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	t_{PLH}	A	B	1.5	6	0.1	5.6	0.1	4.5	0.1	3.3	0.1	2.9	ns
t_{PHL}	t_{PHL}			1	4	0.1	5.6	0.1	4.5	0.1	3.3	0.1	2.9	
t_{PLH}	t_{PLH}	B	A	1.5	4	0.6	4.2	0.4	3.4	0.2	3	0.1	2.8	ns
t_{PHL}	t_{PHL}			1.5	7.5	0.6	4.2	0.4	3.4	0.2	3	0.1	2.8	

7.10 Switching Characteristics: VCCA = 3.3 V ± 0.3 V (continued)

See Figure 8-1 and Table 8-1 for test circuit and loading. See Figure 8-2, Figure 8-3, and Figure 8-4 for measurement waveforms.

PARAMETER	PARAMETER	FROM	TO	V_{CCB} = 1.2 V ± 0.1 V		V_{CCB} = 1.5 V ± 0.1 V		V_{CCB} = 1.8 V ± 0.15 V		V_{CCB} = 2.5 V ± 0.2 V		V_{CCB} = 3.3 V ± 0.3 V		UNIT
				MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PZH}	t_{PZH}	$\overline{OE}$	A	1	2.5	0.6	8.7	0.6	5.2	0.6	3.8	0.4	3.8	ns
t_{PZL}	t_{PZL}			1	2.5	0.6	8.7	0.6	5.2	0.6	3.8	0.4	3.8	
t_{PZH}	t_{PZH}	$\overline{OE}$	B	1.5	6	0.8	8.7	0.6	6.8	0.5	4.7	0.5	3.8	ns
t_{PZL}	t_{PZL}			1.5	7	0.8	8.7	0.6	6.8	0.5	4.7	0.5	3.8	
t_{PHZ}	t_{PHZ}	$\overline{OE}$	A	2	4	0.7	9.3	0.7	8.3	0.7	5.6	0.7	6.6	ns
t_{PLZ}	t_{PLZ}			2	4	0.7	9.3	0.7	8.3	0.7	5.6	0.7	6.6	
t_{PHZ}	t_{PHZ}	$\overline{OE}$	B	2	5	1.4	9.3	1.2	8.1	1	6.4	0.8	6.2	ns
t_{PLZ}	t_{PLZ}			2	4.5	1.4	9.3	1.2	8.1	1	6.4	0.8	6.2	

7.11 Typical Characteristics

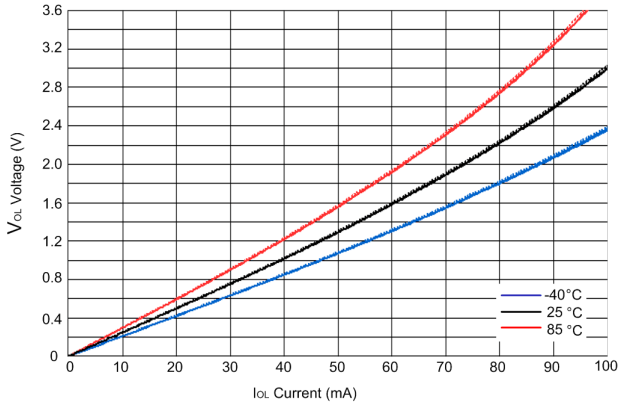


図 7-1. Low-Level Output Voltage (V_{OL}) vs Low-Level Current (I_{OL}) at V_{CCA} = V_{CCB} = 3.6 V

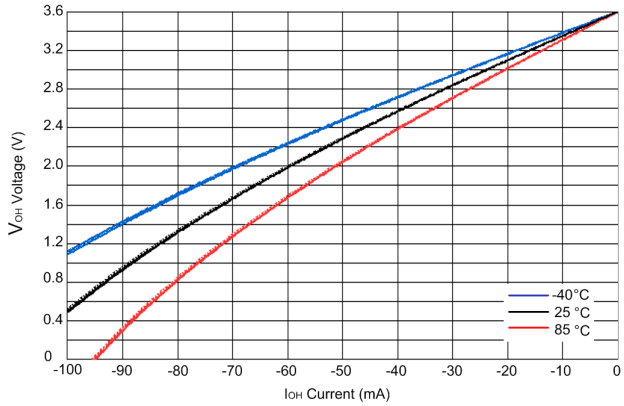


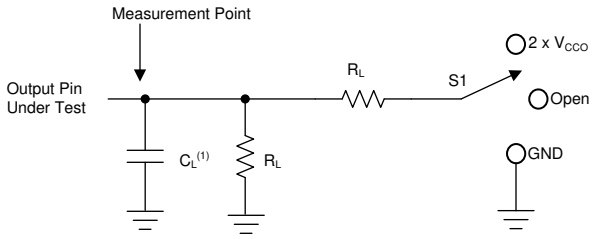
図 7-2. High-Level Output Voltage (V_{OH}) vs High-Level Current (I_{OH}) at V_{CCA} = V_{CCB} = 3.6 V

8 Parameter Measurement Information

8.1 Load Circuit and Voltage Waveforms

Unless otherwise noted, all input pulses are supplied by generators having the following characteristics:

- f = 10 MHz
- Z_O = 50 Ω
- Δt/ΔV ≤ 1 ns/V



A. C_L includes probe and jig capacitance.

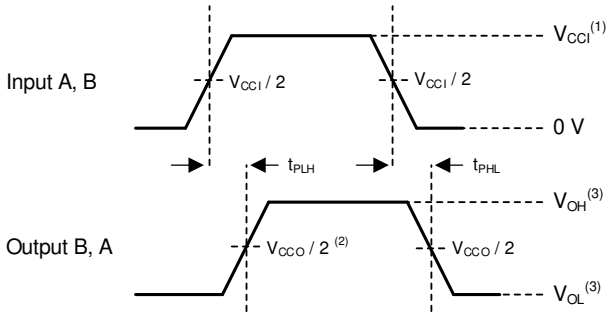
図 8-1. Load Circuit

表 8-1. Load Circuit Parameters

Test Parameter		S_1
t_{pd}	Propagation (delay) time	Open
t_{PZL}, t_{PLZ}	Enable time, disable time	2 × V_{CCO}
t_{PZH}, t_{PHZ}	Enable time, disable time	GND

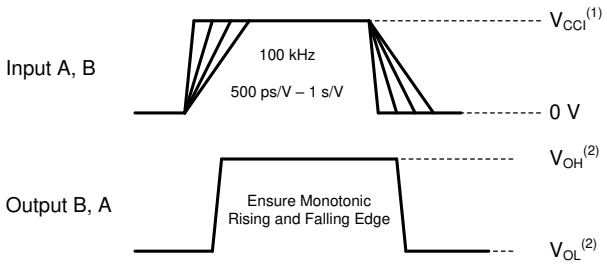
表 8-2. Load Circuit Conditions

V_{CCO}	R_L	C_L	V_{TP}
1.2 V ± 0.1 V	2 kΩ	15 pF	0.1 V
1.5 V ± 0.1 V	2 kΩ	15 pF	0.1 V
1.8 V ± 0.15 V	2 kΩ	15 pF	0.15 V
2.5 V ± 0.2 V	2 kΩ	15 pF	0.15 V
3.3 V ± 0.3 V	2 kΩ	15 pF	0.3 V



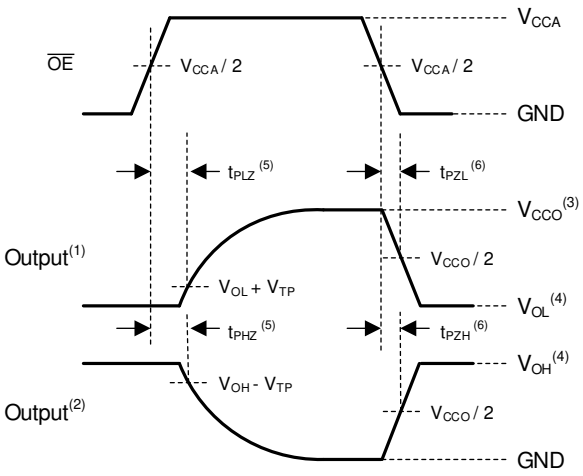
1. V_{CCI} is the V_{CC} associated with the input port.
2. V_{CCO} is the V_{CC} associated with the output port.
3. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1.
4. t_{PLH} and t_{PHL} are the same as t_{pd}.
5. The outputs are measured one at a time, with one transition per measurement.

図 8-2. Propagation Delay



1. V_{CCI} is the supply pin associated with the input port.
2. V_{OH} and V_{OL} are typical output voltage levels that occur with specified R_L, C_L, and S_1.

図 8-3. Input Transition Rise and Fall Rate



A. Output waveform on the condition that input is driven to a valid Logic Low.
B. Output waveform on the condition that input is driven to a valid Logic High.
C. V_{CCO} is the supply pin associated with the output port.
D. V_{OH} and V_{OL} are typical output voltage levels with specified R_L, C_L, and S_1.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.

図 8-4. Enable Time And Disable Time

9 Detailed Description

9.1 Overview

The SN74AVC4T774 is a 4-bit, dual-supply, noninverting, bi-directional voltage level translation. Pins An and control pins (DIR1, DIR2, DIR3, DIR4 and $\overline{OE}$) are support by V_{CCA} and pins Bn are support by V_{CCB}. The A port is able to accept I/O voltages ranging from 1.1 V to 3.6 V, while the B port can accept I/O voltages from 1.1 V to 3.6 V. A high on DIR allows data transmission from An to Bn and a low on DIR allows data transmission from B to A when $\overline{OE}$ is set to low. When $\overline{OE}$ is set to high, both An and Bn are in the high-impedance state.

9.2 Functional Block Diagram

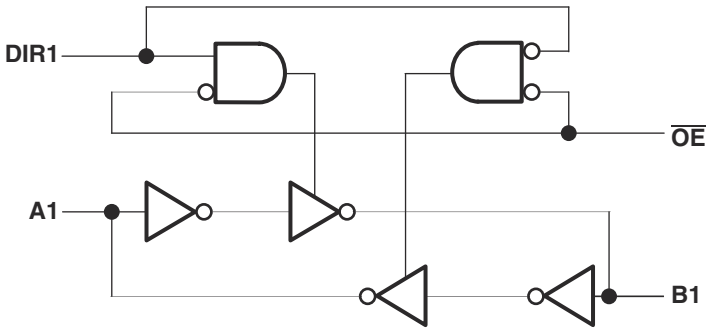


図 9-1. Logic Diagram (Positive Logic)

9.3 Feature Description

9.3.1 Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.1-V to 3.6-V Power-Supply Range

Both V_{CCA} and V_{CCB} can be supplied at any voltage between 1.1 V and 3.6 V making the device suitable for translating between any of the low-voltage nodes (1.2 V, 1.8 V, 2.5 V and 3.3 V).

9.3.2 Support High-Speed Translation

SN74AVC4T774 can support high data rate application. The translated signal data rate can be up to 380 Mbps when signal is translated from 1.8 V to 3.3 V.

9.3.3 I_{off} Supports Partial-Power-Down Mode Operation

I_{off} will prevent backflow current by disabling I/O output circuits when device is in partial-power-down mode.

9.4 Device Functional Modes

表 9-1. Function Table (Each Bit)

CONTROL INPUTS		OUTPUT CIRCUITS		OPERATION
$\overline{OE}$	DIR	A PORT	B PORT	
L	L	Enabled	Hi-Z	B data to A data
L	H	Hi-Z	Enabled	A data to B data
H	X	Hi-Z	Hi-Z	Isolation

10 Application and Implementation

Note

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

10.1 Application Information

The SN74AVC4T774 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The SN74AVC4T774 device is ideal for use in applications where a push-pull driver is connected to the data I/Os. Its max data rate can be up to 380 Mbps when device translate signal from 1.8 V to 3.3 V.

10.2 Typical Application

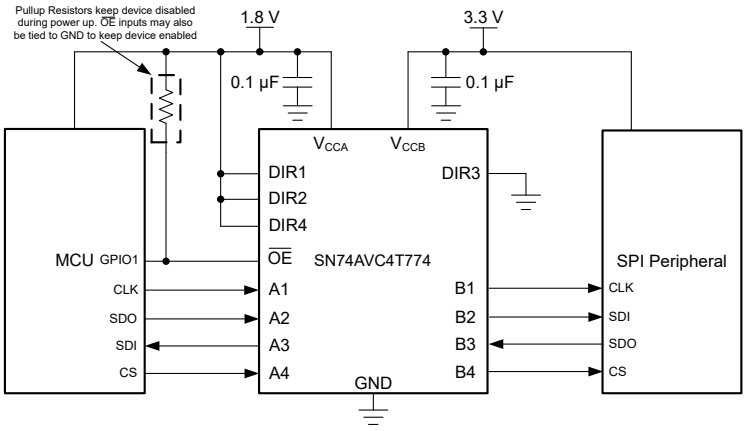


図 10-1. Typical Application of the SN74AVC4T774

10.2.1 Design Requirements

For this design example, use the parameters listed in 表 10-1.

表 10-1. Design Parameters

DESIGN PARAMETERS	EXAMPLE VALUE
Input Voltage Range	1.1 V to 3.6 V
Output Voltage Range	1.1 V to 3.6 V

10.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range
  - Use the supply voltage of the device that is driving the SN74AVC4T774 device to determine the input voltage range. For a valid logic high, the value must exceed the V_{IH} of the input port. For a valid logic low, the value must be less than the V_{IL} of the input port.
- Output voltage range
  - Use the supply voltage of the device that the SN74AVC4T774 device is driving to determine the output voltage range.

10.2.3 Application Curve

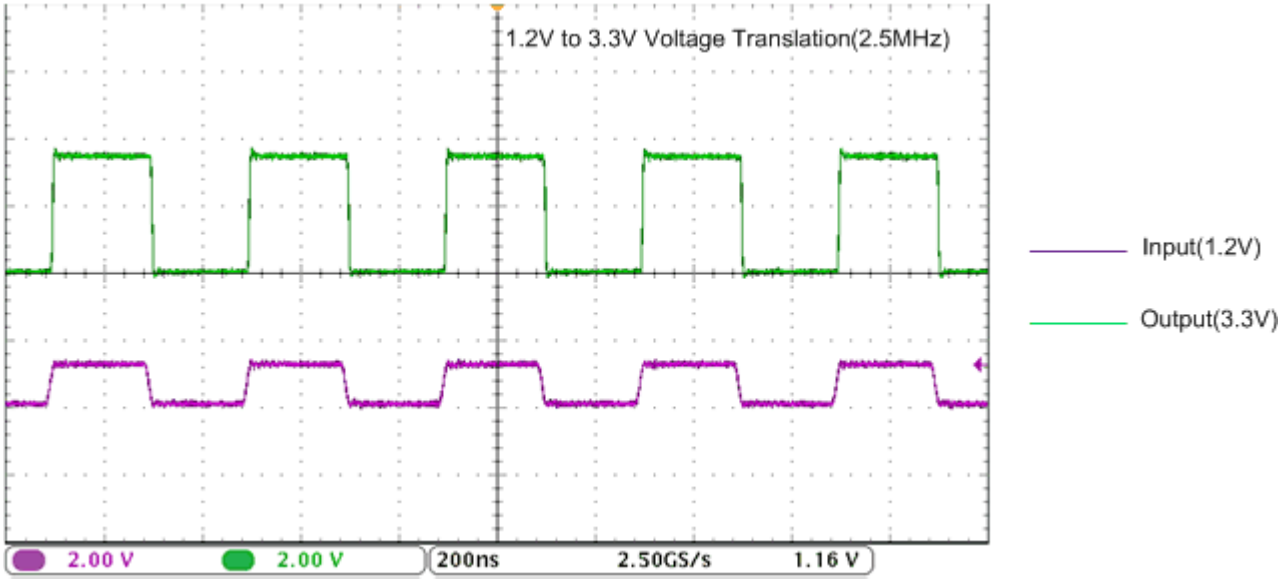


図 10-2. Translation Up (1.2 V to 3.3 V) at 2.5 MHz

11 Power Supply Recommendations

The SN74AVC4T774 device uses two separate configurable power-supply rails, V_{CCA} and V_{CCB}. V_{CCA} accepts any supply voltage from 1.1 V to 3.6 V and V_{CCB} accepts any supply voltage from 1.1 V to 3.6 V. The A port and B port are designed to track V_{CCA} and V_{CCB} respectively allowing for low-voltage, bi-directional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V and 3.3-V voltage nodes.

The output-enable $\overline{OE}$ input circuit is designed so that it is supplied by V_{CCA} and when the $\overline{OE}$ input is high, all outputs are placed in the high-impedance state. To ensure the high-impedance state of the outputs during power-up or power-down, the $\overline{OE}$ input pin must be tied to V_{CCA} through a pullup resistor and must not be enabled until V_{CCA} and V_{CCB} are fully ramped and stable. The minimum value of the pullup resistor to V_{CCA} is determined by the current-sinking capability of the driver.

12 Layout

12.1 Layout Guidelines

To ensure reliability of the device, following common printed-circuit board layout guidelines are recommended:

- Bypass capacitors should be used on power supplies.
- Short trace lengths should be used to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements

12.2 Layout Example

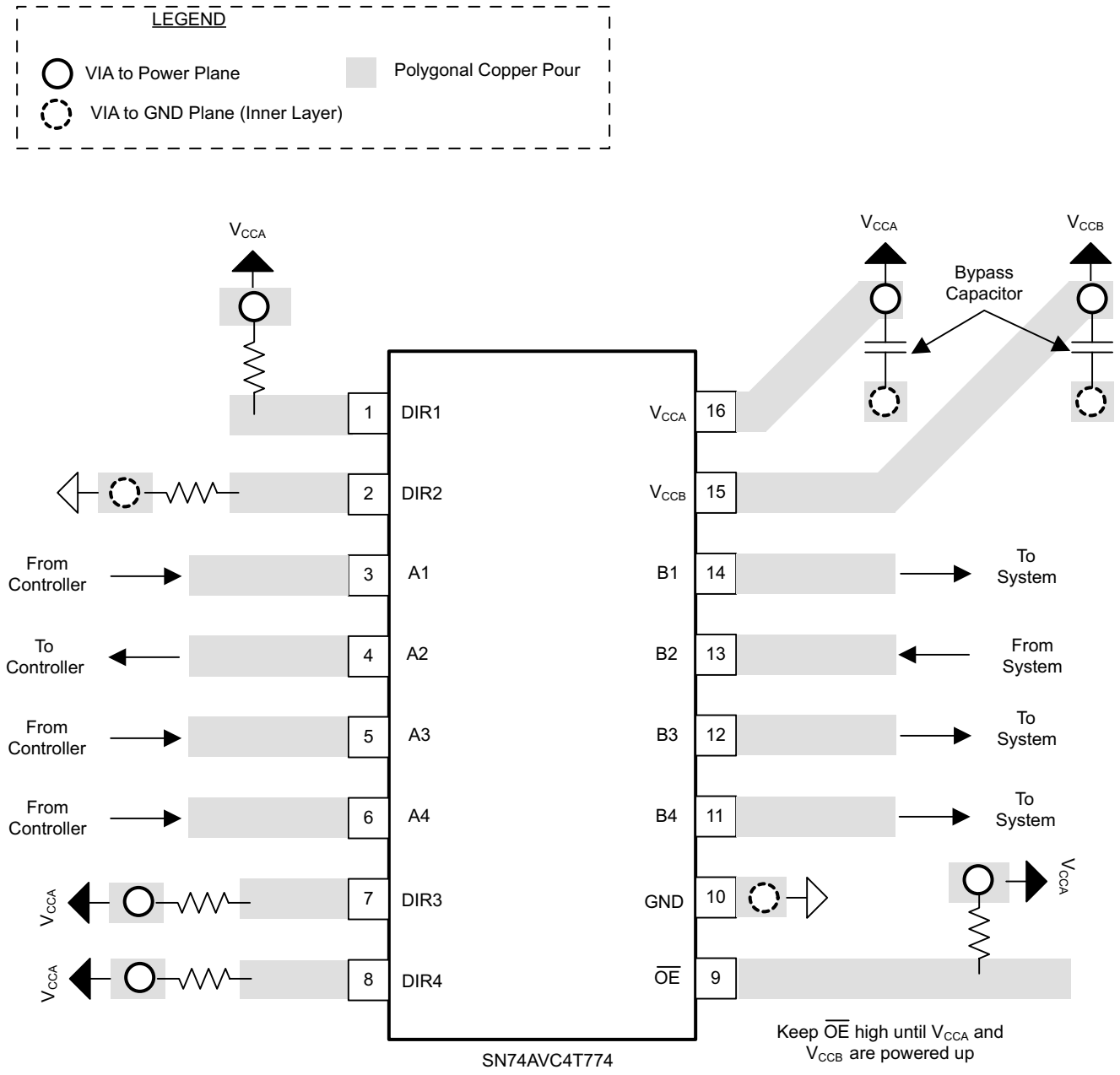


図 12-1. PCB Layout Example

13 Device and Documentation Support

13.1 Documentation Support

13.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *16-Bit Widebus Logic Families in 56-Ball, 0.65-mm Pitch Very Thin Fine-Pitch BGA* application report
- Texas Instruments, *AVC Logic Family Technology and Applications* application report
- Texas Instruments, *AVC Advanced Very-Low-Voltage CMOS Logic Data Book, March 2000* data book
- Texas Instruments, *Dynamic Output Control (DOC) Circuitry Technology And Applications (Rev. B)* application report
- Texas Instruments, *Introduction to Logic* application report
- Texas Instruments, *LCD Module Interface Application Clip* brochure
- Texas Instruments, *Logic Cross-Reference* application note
- Texas Instruments, *Logic Guide* marketing selection guide
- Texas Instruments, *LOGIC Pocket Data Book* data book
- Texas Instruments, *Selecting the Right Level Translation Solution* application report
- Texas Instruments, *Semiconductor Packing Material Electrostatic Discharge (ESD) Protection* application report
- Texas Instruments, *Solving CMOS Transition Rate Issues Using Schmitt Trigger Solution* white paper
- Texas Instruments, *Standard Linear & Logic for PCs, Servers & Motherboards* brochure
- Texas Instruments, *TI Tablet Solutions* solution guide
- Texas Instruments, *Understanding and Interpreting Standard-Logic Data Sheets* application report
- Texas Instruments, *Voltage Translation Between 3.3-V, 2.5-V, 1.8-V, and 1.5-V Logic Standards* application report

13.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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13.4 Trademarks

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すべての商標は、それぞれの所有者に帰属します。

13.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
74AVC4T774RSVR-NT	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZVK	Samples
74AVC4T774RSVRG4	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZVK	Samples
SN74AVC4T774PW	ACTIVE	TSSOP	PW	16	90	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT774	Samples
SN74AVC4T774PWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	WT774	Samples
SN74AVC4T774RGYR	ACTIVE	VQFN	RGY	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	WT774	Samples
SN74AVC4T774RSVR	ACTIVE	UQFN	RSV	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	ZVK	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

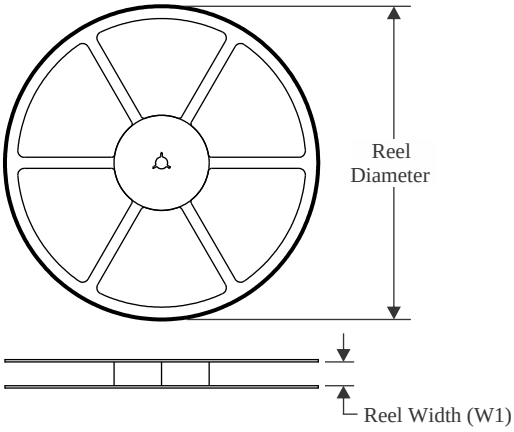
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

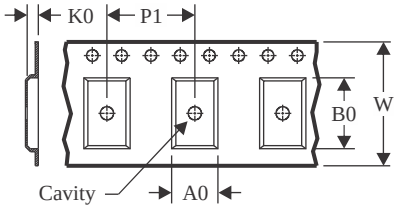
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

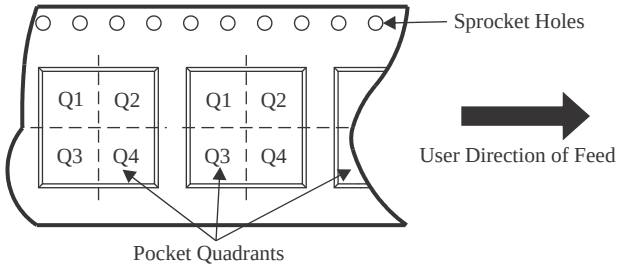


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

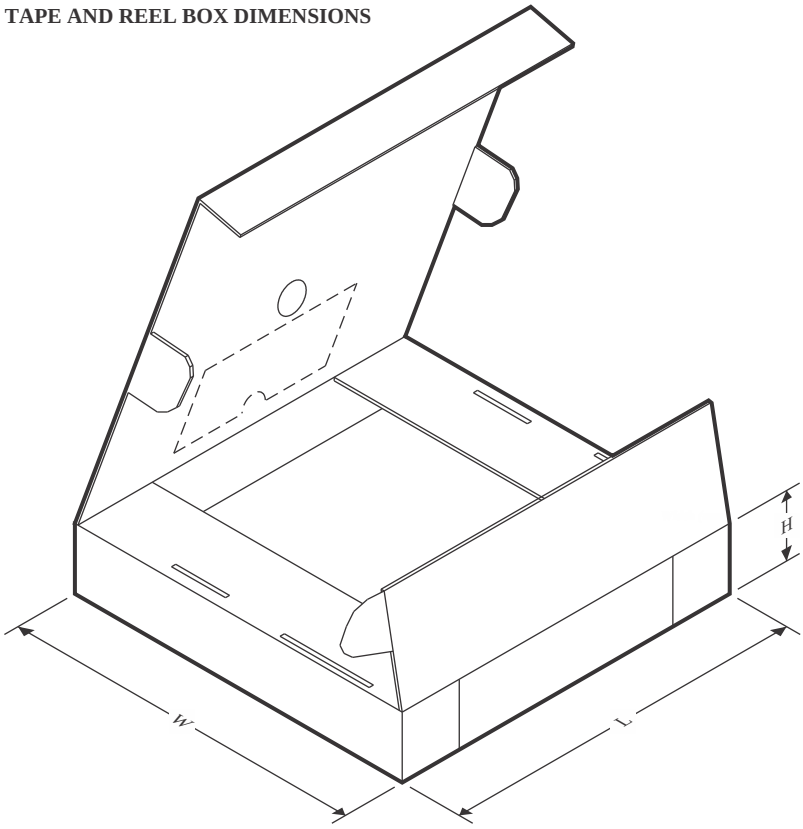
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
74AVC4T774RSVR-NT	UQFN	RSV	16	3000	180.0	9.5	2.1	2.9	0.75	4.0	8.0	Q1
SN74AVC4T774PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
SN74AVC4T774RGYR	VQFN	RGY	16	3000	330.0	12.4	3.8	4.3	1.5	8.0	12.0	Q1
SN74AVC4T774RSVR	UQFN	RSV	16	3000	178.0	13.5	2.1	2.9	0.75	4.0	12.0	Q1

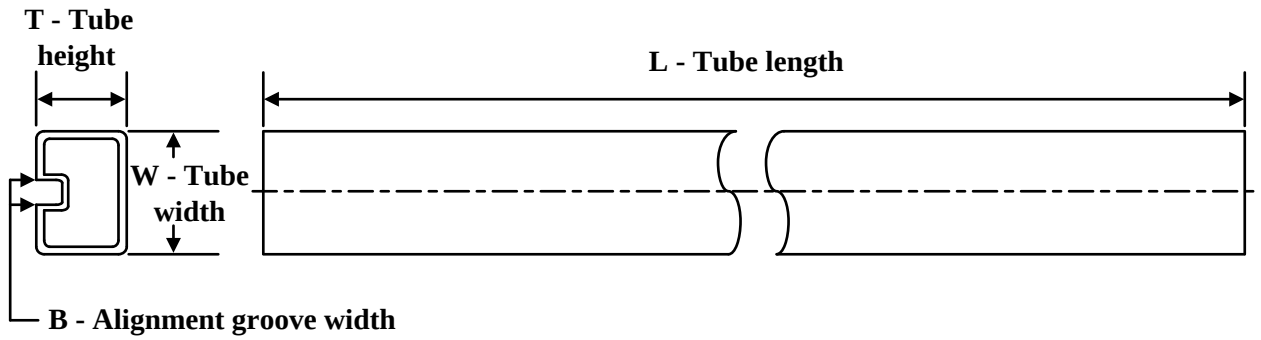
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
74AVC4T774RSVR-NT	UQFN	RSV	16	3000	189.0	185.0	36.0
SN74AVC4T774PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
SN74AVC4T774RGYR	VQFN	RGY	16	3000	356.0	356.0	35.0
SN74AVC4T774RSVR	UQFN	RSV	16	3000	189.0	185.0	36.0

TUBE



*All dimensions are nominal

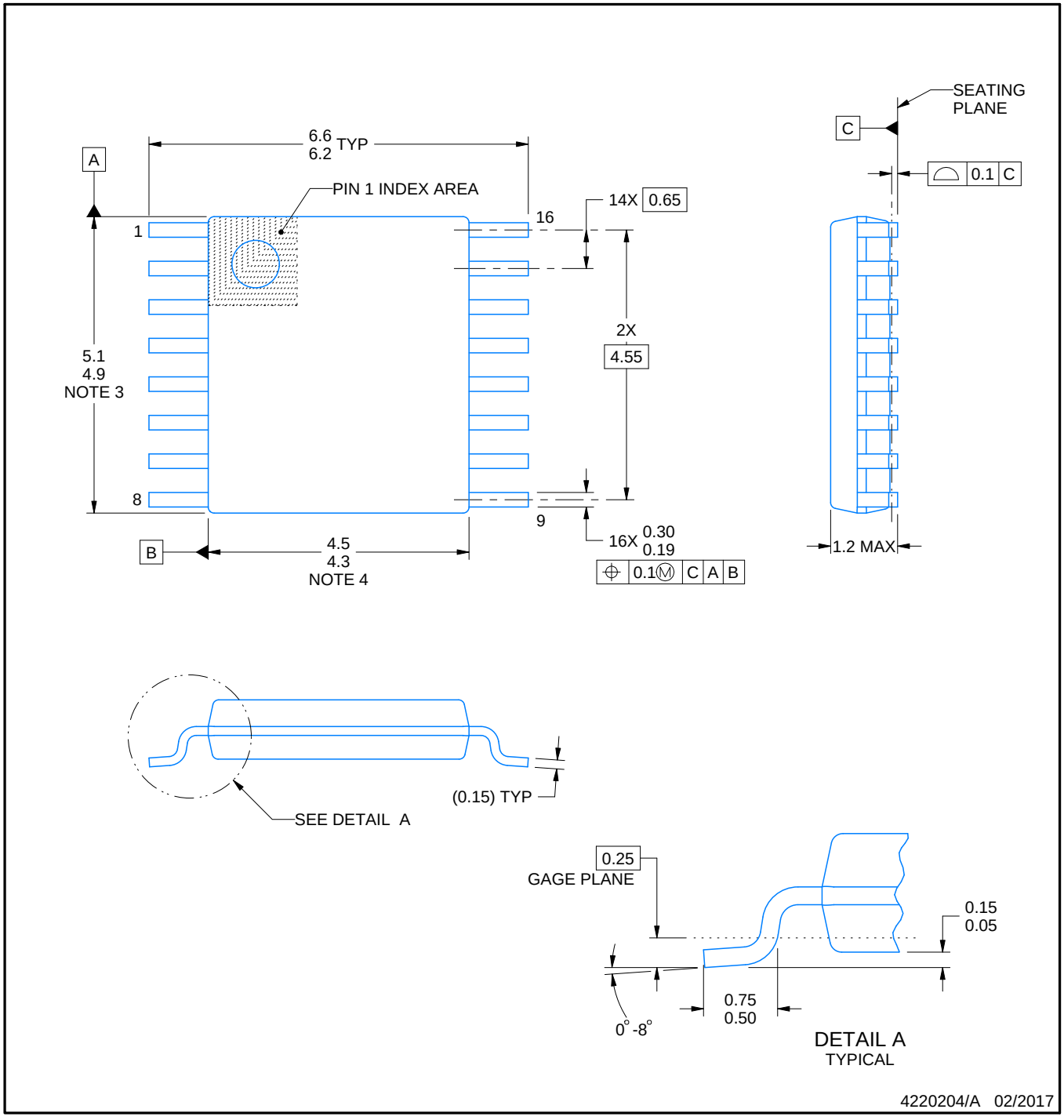
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN74AVC4T774PW	PW	TSSOP	16	90	530	10.2	3600	3.5

PACKAGE OUTLINE

PW0016A

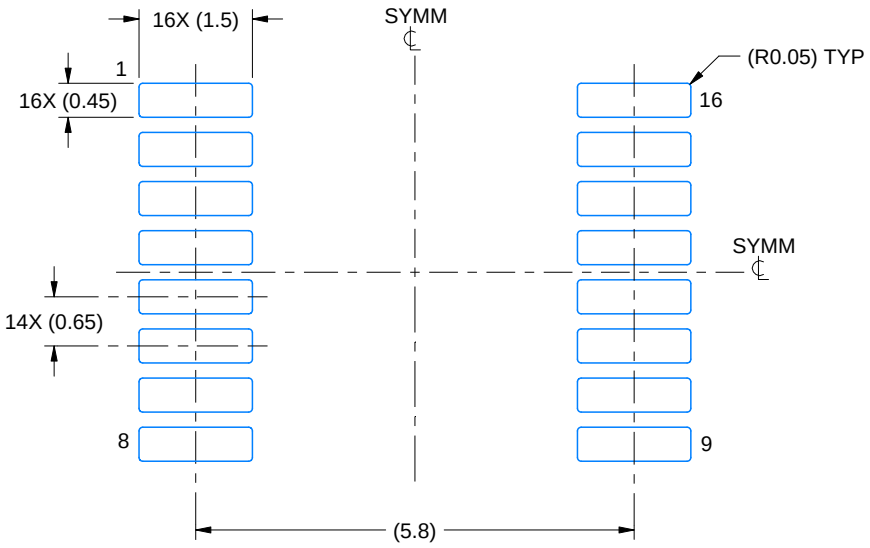
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

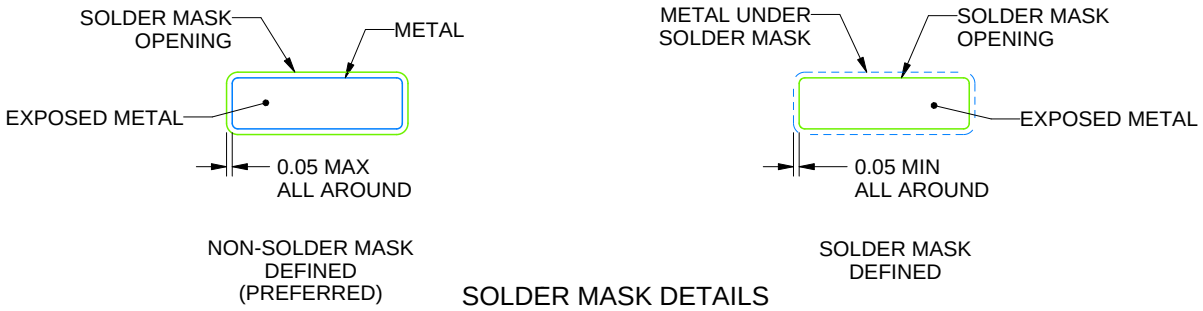


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

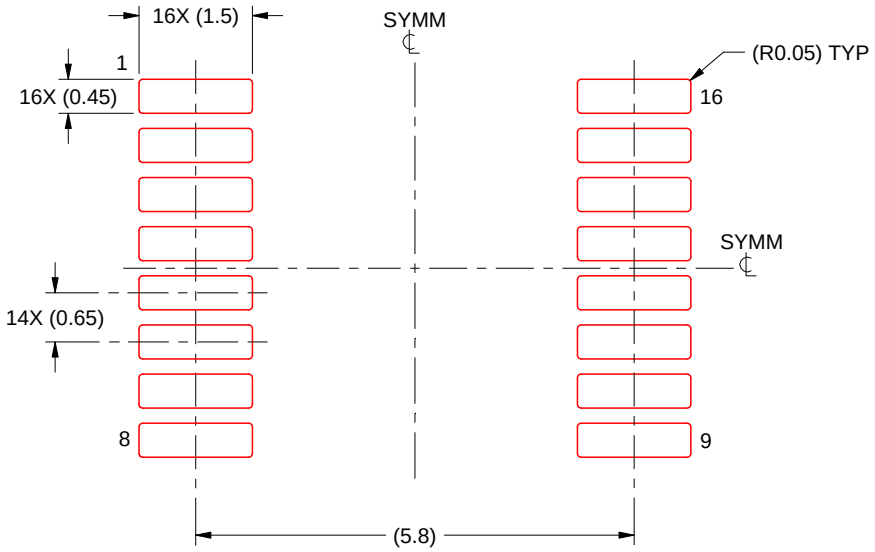


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



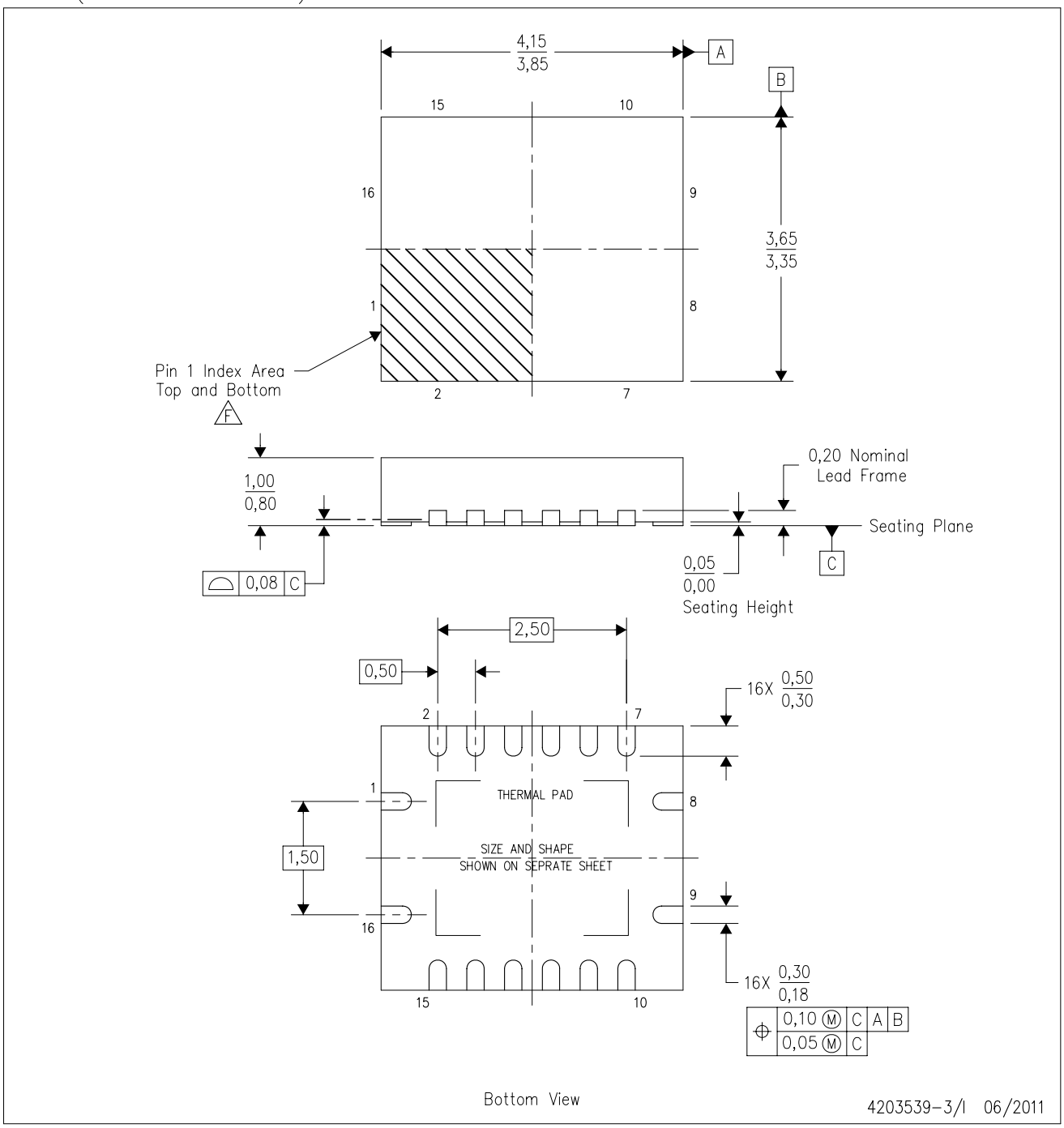
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
F. Pin 1 identifiers are located on both top and bottom of the package and within the zone indicated. The Pin 1 identifiers are either a molded, marked, or metal feature.
G. Package complies to JEDEC MO–241 variation BA.

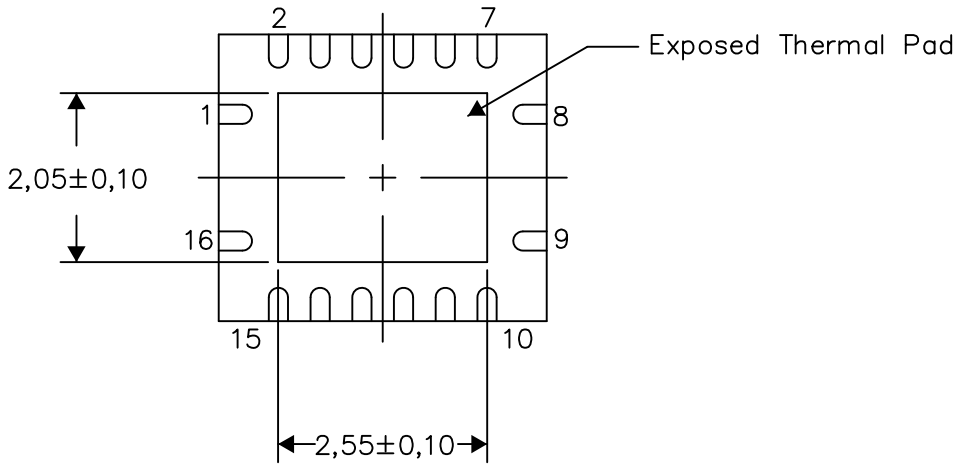
RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



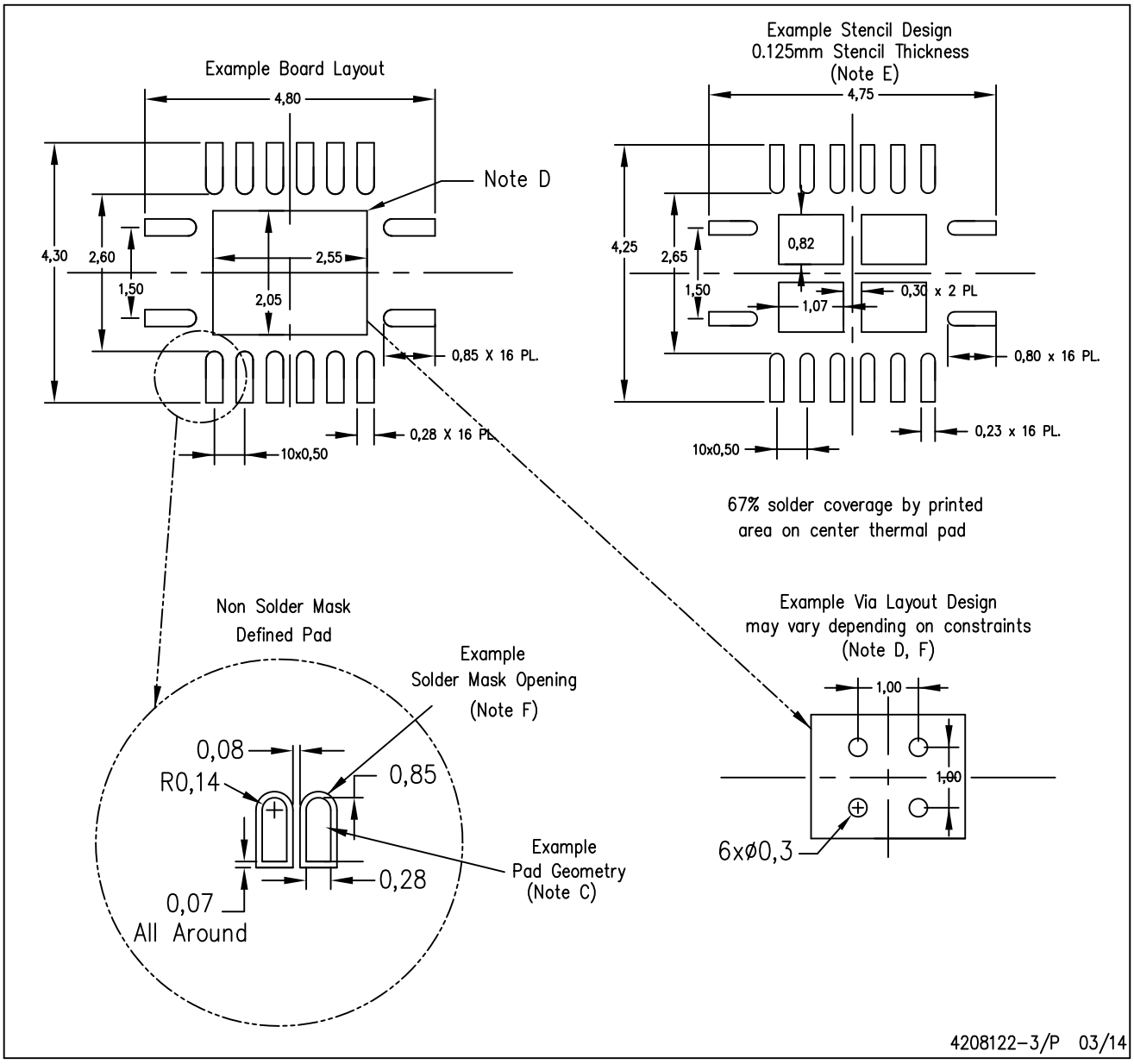
Bottom View

Exposed Thermal Pad Dimensions

4206353–3/P 03/14

NOTE: All linear dimensions are in millimeters

RGY (R–PVQFN–N16) PLASTIC QUAD FLATPACK NO–LEAD



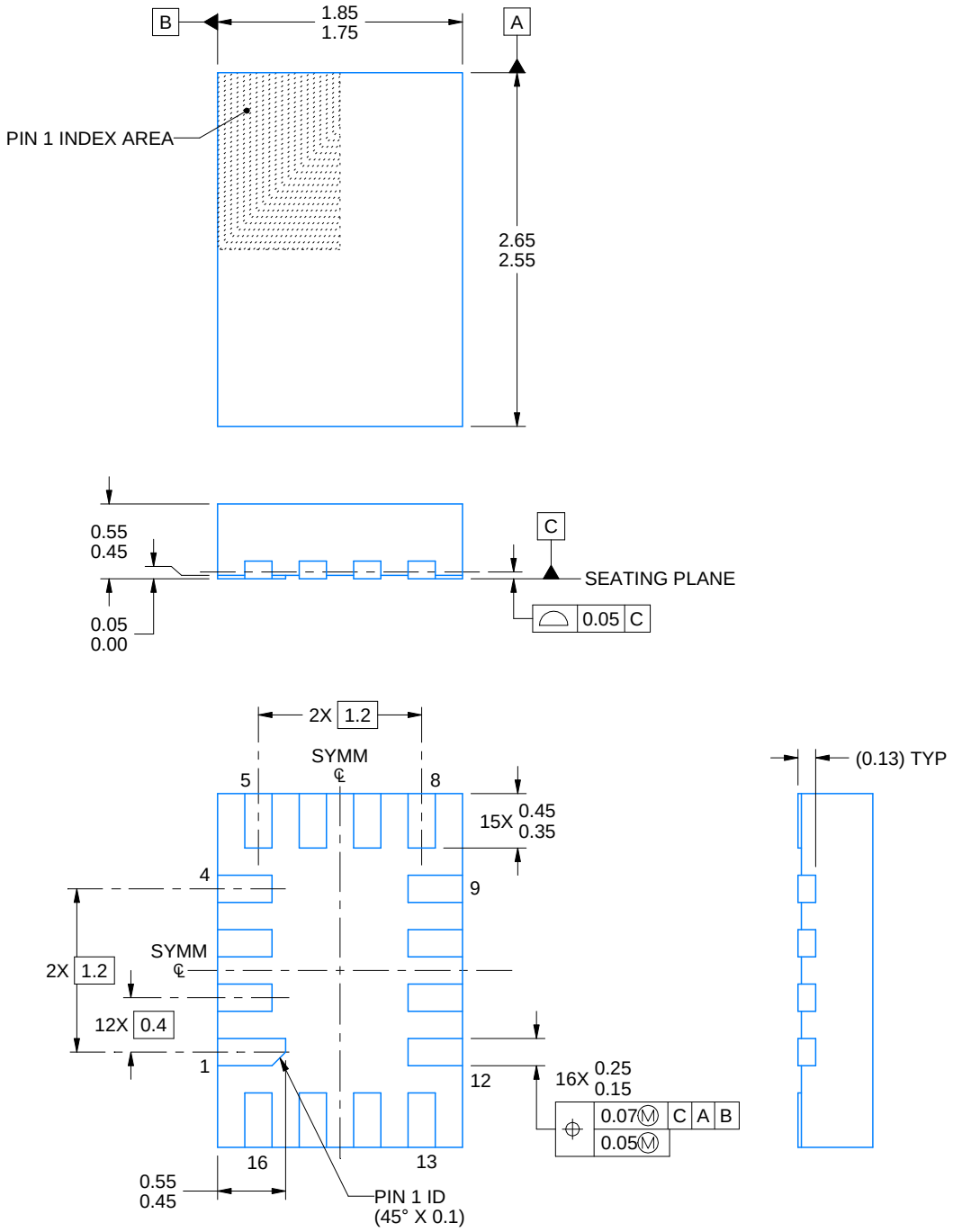
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, Quad Flat–Pack QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
F. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.

RSV0016A

PACKAGE OUTLINE

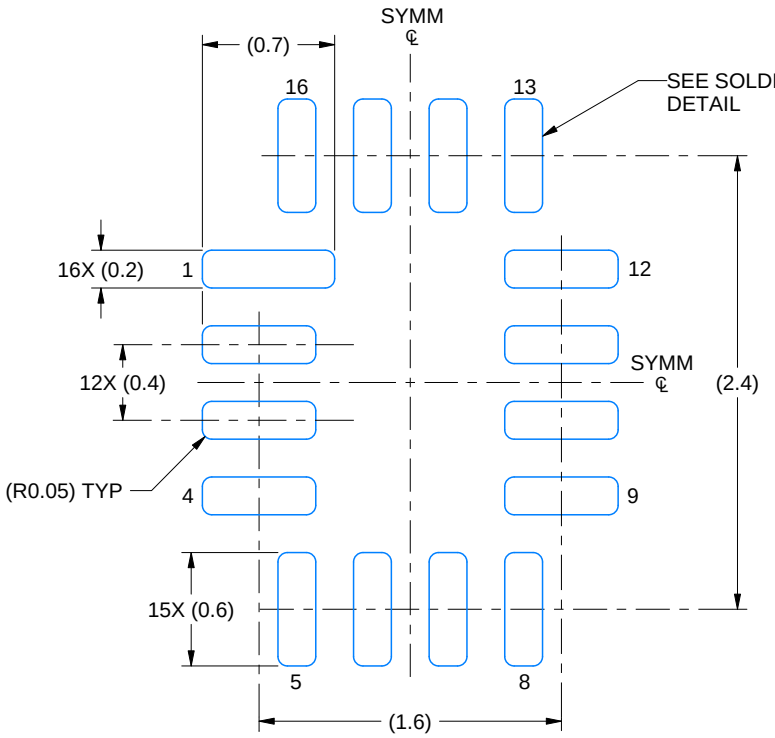
UQFN - 0.55 mm max height

ULTRA THIN QUAD FLATPACK - NO LEAD

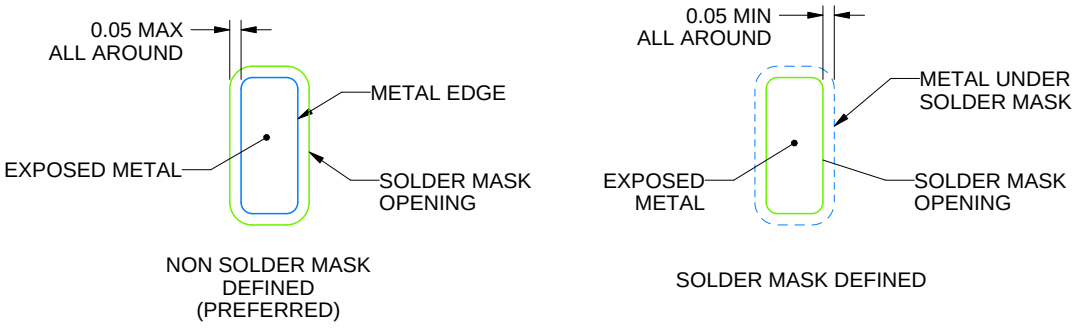


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 25X

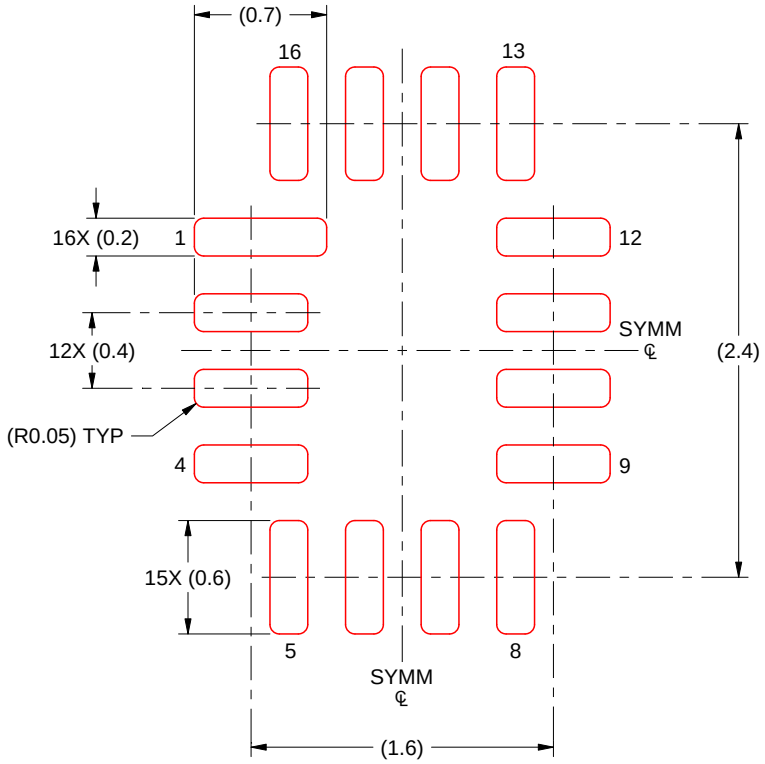


SOLDER MASK DETAILS

4220314/C 02/2020

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 25X

4220314/C 02/2020

NOTES: (continued)

4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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