# SN74AVCH8T245 8 ビット デュアル電源 バス トランシーバ、構成可能レベルシフト、電圧変換、3 ステート出力

## 1 特長

- 制御入力 (DIR および $\overline{OE}$) の $V_{IH}$ および $V_{IL}$ レベルは $V_{CCA}$ 電圧を基準
- データ入力時のバス ホールドにより、外付けのプルアップまたはプルダウン抵抗が不要
- $V_{CC}$ 絶縁機能
- 完全に構成可能なデュアル レール設計
- 4.6V 許容の I/O
- $I_{off}$ により部分的パワーダウン モードでの動作をサポート
- 最大データ レート:
  - 320Mbps ($V_{CCA}$ ≥ 1.8V および $V_{CCB}$ ≥ 1.8V)
  - 170Mbps ($V_{CCA}$ ≤ 1.8V または $V_{CCB}$ ≤ 1.8V)
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能
- JESD 22 を上回る ESD 保護:
  - 8000V、人体モデル (A114-A)
  - マシン モデルで 200V (A115-A)
  - 1000V、荷電デバイス モデル (C101)

## 2 アプリケーション

- パーソナル・エレクトロニクス
- 産業用
- エンタープライズ
- テレコミュニケーション

## 3 概要

SN74AVCH8T245 は、設定可能な 2 本の独立した電源レールを採用した 8 ビット非反転バス トランシーバです。A ポートは $V_{CCA}$ (1.2V～3.6V の任意の電源電圧を入力できます) に追従するように設計されています。同様に B ポートは $V_{CCB}$ (1.2V～3.6V の任意の電源電圧を入力できます) に追従するように設計されています。このため 1.2V、1.5V、1.8V、2.5V、3.3V の任意の電圧ノード間で、低電圧の双方向変換を自在に行うことが可能になります。

SN74AVCH8T245 は、データ バス間の非同期通信用に設計されています。このデバイスは、方向制御 (DIR) 入力の論理レベルに応じて、A バスから B バス、または B バスから A バスへデータを転送します。出力イネーブル ($\overline{OE}$) 入力を使用すると、出力をディセーブルにして、バスを実質的に絶縁できます。

SN74AVCH8T245 の設計では、制御ピン (DIR および $\overline{OE}$) は $V_{CCA}$ を基準としています。

アクティブなバス ホールド回路により、使用されていない、または駆動されていないピンは、有効なロジック状態に保持されます。プルアップ抵抗またはプルダウン抵抗をバス ホールド回路と組み合わせて使用することは推奨しません。

このデバイスは、$I_{off}$ を使用する部分的パワーダウン アプリケーション用の動作が完全に規定されています。$I_{off}$ 回路が出力をディセーブルにするため、デバイスに電流が逆流して損傷に至ることを回避できます。

$V_{CC}$ 絶縁機能により、$V_{CCA}$ または $V_{CCB}$ のいずれかが GND レベルのとき、出力をハイ インピーダンス状態にできます。電源オン側のバス ホールド回路は常にアクティブのままです。

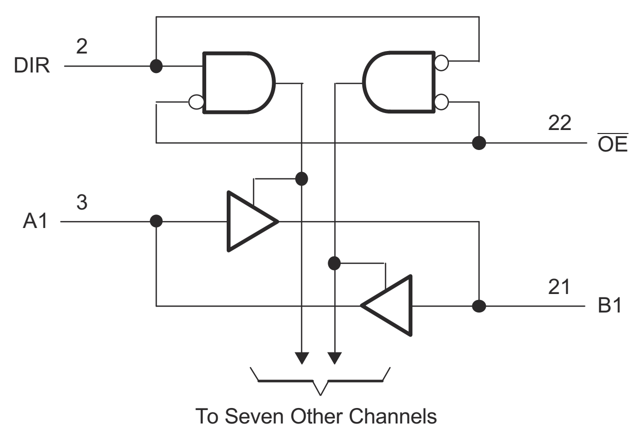
SN74AVCH8T245 ソリューションは単一電源システムと互換性があり、プリント基板の再設計を最小限に抑えながら、後で '245 機能に置き換えることができます。

電源投入時または切断時にデバイスをハイ インピーダンス状態を確保するには、$\overline{OE}$ をプルダウン抵抗で $V_{CCA}$ につなぐ必要があります。この抵抗の最小値は、ドライバの電流ソース能力によって決まります。

**パッケージ情報**

| 部品番号 | パッケージ (1) | パッケージ サイズ(2) |
|---|---|---|
| SN74AVCH8T245 | DGV (TVSOP、24) | 5 mm × 6.4 mm |
| | PW (TSSOP、24) | 7.8 mm × 6.4 mm |
| | RHL (VQFN、24) | 5.5 mm × 3.5 mm |

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。




**論理図 (正論理)**

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## 4 Pin Configuration and Functions

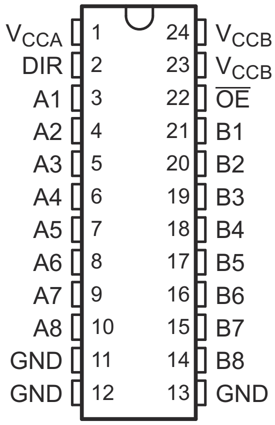



図 4-1. DGV or PW Package, 24-Pin TVSOP or TSSOP (Top View)

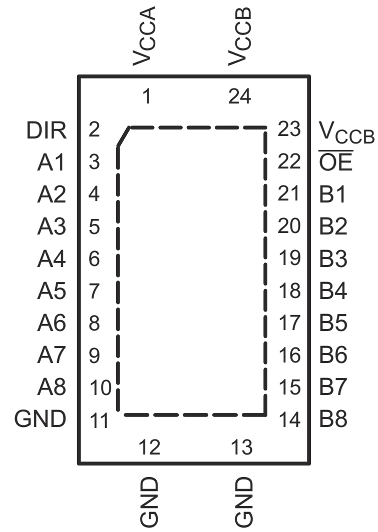



図 4-2. RHL Package, 24-Pin VQFN (Top View)

表 4-1. Pin Functions

| PIN | | I/O | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| A1 | 3 | I/O | Input/output A1. Referenced to $V_{CCA}$. |
| A2 | 4 | I/O | Input/output A2. Referenced to $V_{CCA}$. |
| A3 | 5 | I/O | Input/output A3. Referenced to $V_{CCA}$. |
| A4 | 6 | I/O | Input/output A4. Referenced to $V_{CCA}$. |
| A5 | 7 | I/O | Input/output A5. Referenced to $V_{CCA}$. |
| A6 | 8 | I/O | Input/output A6. Referenced to $V_{CCA}$. |
| A7 | 9 | I/O | Input/output A7. Referenced to $V_{CCA}$. |
| A8 | 10 | I/O | Input/output A8. Referenced to $V_{CCA}$. |
| B1 | 21 | I/O | Input/output B1. Referenced to $V_{CCB}$. |
| B2 | 20 | I/O | Input/output B2. Referenced to $V_{CCB}$. |
| B3 | 19 | I/O | Input/output B3. Referenced to $V_{CCB}$. |
| B4 | 18 | I/O | Input/output B4. Referenced to $V_{CCB}$. |
| B5 | 17 | I/O | Input/output B5. Referenced to $V_{CCB}$. |
| B6 | 16 | I/O | Input/output B6. Referenced to $V_{CCB}$. |
| B7 | 15 | I/O | Input/output B7. Referenced to $V_{CCB}$. |
| B8 | 14 | I/O | Input/output B8. Referenced to $V_{CCB}$. |
| DIR | 2 | I | Direction-control signal. Referenced to $V_{CCA}$. |
| GND | 11, 12, 13 | — | Ground |
| $\overline{OE}$ | 22 | I | 3-state output-mode enables. Pull $\overline{OE}$ high to place all outputs in 3-state mode. Referenced to $V_{CCA}$. |
| $V_{CCA}$ | 1 | — | A-port supply voltage. 1.2V ≤ $V_{CCA}$ ≤ 3.6V |
| $V_{CCB}$ | 23, 24 | — | B-port supply voltage. 1.2V ≤ $V_{CCA}$ ≤ 3.6V |

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[(1)]

| | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|
| $V_{CCA}$ / $V_{CCB}$ | Supply voltage | | –0.5 | 4.6 | V |
| $V_I$ | Input voltage[(2)] | I/O ports (A port) | –0.5 | 4.6 | V |
| | | I/O ports (B port) | –0.5 | 4.6 | |
| | | Control inputs | –0.5 | 4.6 | |
| $V_O$ | Voltage applied to any output in the high-impedance or power-off state[(2)] | A port | –0.5 | 4.6 | V |
| | | B port | –0.5 | 4.6 | |
| $V_O$ | Voltage applied to any output in the high or low state[(2) (3)] | A port | –0.5 | $V_{CCA}$ + 0.5 | V |
| | | B port | –0.5 | $V_{CCB}$ + 0.5 | |
| $I_{IK}$ | Input clamp current | $V_I < 0$ | | –50 | mA |
| $I_{OK}$ | Output clamp current | $V_O < 0$ | | –50 | mA |
| $I_O$ | Continuous output current | | | ±50 | mA |
| | Continuous current through $V_{CCA}$, $V_{CCB}$, or GND | | | ±100 | mA |
| $T_J$ | Junction temperature | | –40 | 150 | °C |
| $T_{stg}$ | Storage temperature | | –65 | 150 | °C |

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
(3) The output positive-voltage rating may be exceeded up to 4.6V maximum if the output current rating is observed.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[(1)] | ±8000 | V |
| | | Charged-device model (CDM), per JEDEC specification JESD22-C101[(2)] | ±1000 | |
| | | Machine model (MM) | ±200 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 5.3 Recommended Operating Conditions

See [(1)](2)

| | | | | MIN | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{CCA}$ | Supply voltage | | | 1.2 | 3.6 | V |
| $V_{CCB}$ | Supply voltage | | | 1.2 | 3.6 | V |
| $V_{IH}$ | High-level input voltage[(1)] | Data inputs | $V_{CCI}$ = 1.2V to 1.95V | $V_{CCI}$ × 0.65 | | V |
| | | | $V_{CCI}$ = 1.95V to 2.7V | 1.6 | | |
| | | | $V_{CCI}$ = 2.7V to 3.6V | 2 | | |
| $V_{IL}$ | Low-level input voltage[(1)] | Data inputs | $V_{CCI}$ = 1.2V to 1.95V | | $V_{CCI}$ × 0.35 | V |
| | | | $V_{CCI}$ = 1.95V to 2.7V | | 0.7 | |
| | | | $V_{CCI}$ = 2.7V to 3.6V | | 0.8 | |
| $V_{IH}$ | High-level input voltage | DIR and $\overline{OE}$ (referenced to $V_{CCA}$) | $V_{CCI}$ = 1.2V to 1.95V | $V_{CCA}$ × 0.65 | | V |
| | | | $V_{CCI}$ = 1.95V to 2.7V | 1.6 | | |
| | | | $V_{CCI}$ = 2.7V to 3.6V | 2 | | |
| $V_{IL}$ | Low-level input voltage | DIR and $\overline{OE}$ (referenced to $V_{CCA}$) | $V_{CCI}$ = 1.2V to 1.95V | | $V_{CCA}$ × 0.35 | V |
| | | | $V_{CCI}$ = 1.95V to 2.7V | | 0.7 | |
| | | | $V_{CCI}$ = 2.7V to 3.6V | | 0.8 | |
| $V_I$ | Input voltage | Control Inputs | | 0 | 3.6 | V |
| $V_O$ | Output voltage[(2)] | Active state | | 0 | $V_{CCO}$ | V |
| | | 3-state | | 0 | 3.6 | |
| $I_{OH}$ | High-level output current | | $V_{CCO}$ = 1.2V | | –3 | mA |
| | | | $V_{CCO}$ = 1.4V to 1.6V | | –6 | |
| | | | $V_{CCO}$ = 1.65V to 1.95V | | –8 | |
| | | | $V_{CCO}$ = 2.3V to 2.7V | | –9 | |
| | | | $V_{CCO}$ = 3V to 3.6V | | –12 | |
| $I_{OL}$ | Low-level output current | | $V_{CCO}$ = 1.2V | | 3 | mA |
| | | | $V_{CCO}$ = 1.4V to 1.6V | | 6 | |
| | | | $V_{CCO}$ = 1.65V to 1.95V | | 8 | |
| | | | $V_{CCO}$ = 2.3V to 2.7V | | 9 | |
| | | | $V_{CCO}$ = 3V to 3.6V | | 12 | |
| Δt/Δv | Input transition rise or fall rate | | | | 5 | ns/V |
| $T_A$ | Operating free-air temperature | | | –40 | 85 | °C |

(1) $V_{CCI}$ is the $V_{CC}$ associated with the input port.
(2) $V_{CCO}$ is the $V_{CC}$ associated with the output port.

## 5.4 Thermal Information

| THERMAL METRIC[1] | | SN74AVCH8T245 | | | UNIT |
|---|---|---|---|---|---|
| | | DGV (TVSOP) | PW (TSSOP) | RHL (VQFN) | |
| | | 24 PINS | 24 PINS | 24 PINS | |
| $R_{θJA}$ | Junction-to-ambient thermal resistance[4] | 116.7 | 93.1 | 36.8 | °C/W |
| $R_{θJC(top)}$ | Junction-to-case (top) thermal resistance | 48.5 | 36.7 | 32.5 | °C/W |
| $R_{θJB}$ | Junction-to-board thermal resistance | 62.1 | 48.4 | 15.7 | °C/W |
| $Ψ_{JT}$ | Junction-to-top characterization parameter | 7.0 | 93.1 | 0.7 | °C/W |
| $Ψ_{JB}$ | Junction-to-board characterization parameter | 61.6 | 48.0 | 15.6 | °C/W |
| $R_{θJC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | 5.6 | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 5.5 Electrical Characteristics

All typical limits apply over $T_A$ = 25°C, and all maximum and minimum limits apply over $T_A$ = –40°C to 85°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{OH}$ | High-level output voltage[1] | $I_{OH}$ = –100μA, $V_I$= $V_{IH}$ | $V_{CCA}$ = $V_{CCB}$ = 1.2V to 3.6V | $V_{CCO}$ – 0.2 | | | V |
| | | $I_{OH}$ = –3mA, $V_I$= $V_{IH}$ | $V_{CCA}$ = $V_{CCB}$ = 1.2V | | 0.95 | | |
| | | $I_{OH}$ = –6mA, $V_I$= $V_{IH}$ | $V_{CCA}$ = $V_{CCB}$ = 1.4V | 1.05 | | | |
| | | $I_{OH}$ = –8mA, $V_I$= $V_{IH}$ | $V_{CCA}$ = $V_{CCB}$ = 1.65V | 1.2 | | | |
| | | $I_{OH}$ = –9mA, $V_I$= $V_{IH}$ | $V_{CCA}$ = $V_{CCB}$ = 2.3V | 1.75 | | | |
| | | $I_{OH}$ = –12mA, $V_I$= $V_{IH}$ | $V_{CCA}$ = $V_{CCB}$ = 3V | 2.3 | | | |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 100μA, $V_I$= $V_{IL}$ | $V_{CCA}$ = $V_{CCB}$ = 1.2V to 3.6V | | | 0.2 | V |
| | | $I_{OL}$ = 3mA, $V_I$= $V_{IL}$ | $V_{CCA}$ = $V_{CCB}$ = 1.2V | | 0.15 | | |
| | | $I_{OL}$ = 6mA, $V_I$= $V_{IL}$ | $V_{CCA}$ = $V_{CCB}$ = 1.4V | | | 0.35 | |
| | | $I_{OL}$ = 8mA, $V_I$= $V_{IL}$ | $V_{CCA}$ = $V_{CCB}$ = 1.65V | | | 0.45 | |
| | | $I_{OL}$ = 9mA, $V_I$= $V_{IL}$ | $V_{CCA}$ = $V_{CCB}$ = 2.3V | | | 0.55 | |
| | | $I_{OL}$ = 12mA, $V_I$= $V_{IL}$ | $V_{CCA}$ = $V_{CCB}$ = 3V | | | 0.7 | |
| $I_I$ | Control inputs | $V_I$ = $V_{CCA}$ or GND | $V_{CCA}$ = $V_{CCB}$ = 1.2V to 3.6V | | ±0.025 | ±1 | μA |
| $I_{BHL}$ | Bus-hold low sustaining current[5] | $V_I$ = 0.42V | $V_{CCA}$ = $V_{CCB}$ = 1.2V | | 25 | | μA |
| | | $V_I$ = 0.49V | $V_{CCA}$ = $V_{CCB}$ = 1.4V | 15 | | | |
| | | $V_I$ = 0.58V | $V_{CCA}$ = $V_{CCB}$ = 1.65V | 25 | | | |
| | | $V_I$ = 0.7V | $V_{CCA}$ = $V_{CCB}$ = 2.3V | 45 | | | |
| | | $V_I$ = 0.8V | $V_{CCA}$ = $V_{CCB}$ = 3.3V | 100 | | | |
| $I_{BHH}$ | Bus-hold high sustaining current[6] | $V_I$ = 0.78V | $V_{CCA}$ = $V_{CCB}$ = 1.2V | | –25 | | μA |
| | | $V_I$ = 0.91V | $V_{CCA}$ = $V_{CCB}$ = 1.4V | –15 | | | |
| | | $V_I$ = 1.07V | $V_{CCA}$ = $V_{CCB}$ = 1.65V | –25 | | | |
| | | $V_I$ = 1.6V | $V_{CCA}$ = $V_{CCB}$ = 2.3V | –45 | | | |
| | | $V_I$ = 2V | $V_{CCA}$ = $V_{CCB}$ = 3.3V | –100 | | | |
| $I_{BHLO}$ | Bus-hold low overdrive current[3] | $V_I$ = 0 to $V_{CC}$ | $V_{CCA}$ = $V_{CCB}$ = 1.2V | | 50 | | μA |
| | | | $V_{CCA}$ = $V_{CCB}$ = 1.6V | 125 | | | |
| | | | $V_{CCA}$ = $V_{CCB}$ = 1.95V | 200 | | | |
| | | | $V_{CCA}$ = $V_{CCB}$ = 2.7V | 300 | | | |
| | | | $V_{CCA}$ = $V_{CCB}$ = 3.6V | 500 | | | |

## 5.5 Electrical Characteristics (続き)

All typical limits apply over $T_A$ = 25°C, and all maximum and minimum limits apply over $T_A$ = –40°C to 85°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $I_{BHHO}$ | Bus-hold high overdrive current(4) | $V_I$ = 0 to $V_{CC}$ | $V_{CCA}$ = $V_{CCB}$ = 1.2V | | | –50 | | µA |
| | | | $V_{CCA}$ = $V_{CCB}$ = 1.6V | | –125 | | | |
| | | | $V_{CCA}$ = $V_{CCB}$ = 1.95V | | –200 | | | |
| | | | $V_{CCA}$ = $V_{CCB}$ = 2.7V | | –300 | | | |
| | | | $V_{CCA}$ = $V_{CCB}$ = 3.6V | | –500 | | | |
| $I_{off}$ | Input/output power-off leakage current | $V_I$ = 0V to 3.6V, $V_O$= 0V to 3.6V | $V_{CCA}$ = 0V, $V_{CCB}$ = 0V to 3.6V | A Port | | ±0.1 | ±5 | µA |
| | | | $V_{CCA}$ = 0V to 3.6V, $V_{CCB}$ = 0V | B Port | | ±0.1 | ±5 | |
| $I_{OZ}$ | Off-state output current (1) (2) (7) | $V_O$ = $V_{CCO}$ or GND, $V_I$ = $V_{CCI}$ or GND, $\overline{OE}$ = $V_{IH}$ | $V_{CCA}$ = $V_{CCB}$ = 3.6V | A Port, B Port | | ±0.5 | ±5 | µA |
| | | $V_O$ = $V_{CCO}$ or GND, $V_I$ = $V_{CCI}$ or GND, $\overline{OE}$ = Don't Care | $V_{CCA}$ = 0V, $V_{CCB}$ = 3.6V | B Port | | | ±5 | |
| | | | $V_{CCA}$ = 3.6V, $V_{CCB}$ = 0V | A Port | | | ±5 | |
| $I_{CCA}$ | Supply current A port(2) | $V_I$ = $V_{CCI}$ or GND, $I_O$ = 0 | $V_{CCA}$ = $V_{CCB}$ = 1.2V to 3.6V | | | | 8 | µA |
| | | | $V_{CCA}$ = 0V, $V_{CCB}$ = 3.6V | | | | –2 | |
| | | | $V_{CCA}$ = 3.6V, $V_{CCB}$ = 0V | | | | 8 | |
| $I_{CCB}$ | Supply current B port(2) | $V_I$ = $V_{CCI}$ or GND, $I_O$ = 0 | $V_{CCA}$ = $V_{CCB}$ = 1.2V to 3.6V | | | | 8 | µA |
| | | | $V_{CCA}$ = 0V, $V_{CCB}$ = 3.6V | | | | 8 | |
| | | | $V_{CCA}$ = 3.6V, $V_{CCB}$ = 0V | | | | –2 | |
| $I_{CCA}$+ $I_{CCB}$ | Combined supply current(2) | $V_I$ = $V_{CCI}$ or GND, $I_O$ = 0 | $V_{CCA}$ = $V_{CCB}$ = 1.2V to 3.6V | | | | 16 | µA |
| $C_i$ | Input capacitance control pins | $V_I$ = 3.3V or GND | $V_{CCA}$ = $V_{CCB}$ = 3.3V | | | 3.5 | 4.5 | pF |
| $C_{io}$ | Input/output capacitance a or b port | $V_O$ = 3.3V or GND | $V_{CCA}$ = $V_{CCB}$ = 3.3V | | | 6 | 7 | pF |

(1) $V_{CCO}$ is the $V_{CC}$ associated with the output port.
(2) $V_{CCI}$ is the $V_{CC}$ associated with the input port.
(3) An external driver must source at least $I_{BHLO}$ to switch this node from low to high.
(4) An external driver must sink at least $I_{BHHO}$ to switch this node from high to low.
(5) The bus-hold circuit can sink at least the minimum low sustaining current at $V_{IL}$ max. $I_{BHL}$ should be measured after lowering $V_{IN}$ to GND and then raising it to $V_{IL}$ max.
(6) The bus-hold circuit can source at least the minimum high sustaining current at $V_{IH}$ min. $I_{BHH}$ should be measured after raising $V_{IN}$ to $V_{CC}$ and then lowering it to $V_{IH}$ min.
(7) For I/O ports, the parameter $I_{OZ}$ includes the input leakage current.

## 5.6 Switching Characteristics, $V_{CCA}$ = 1.2V

$T_A$= 25°C (see 図 6-1)

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time: low-to-high-level output and high-to-low level output | A | B | $V_{CCB}$ = 1.2V | | 3.1 | | ns |
| | | | | $V_{CCB}$ = 1.5V | | 2.6 | | |
| | | | | $V_{CCB}$ = 1.8V | | 2.5 | | |
| | | | | $V_{CCB}$ = 2.5V | | 3 | | |
| | | | | $V_{CCB}$ = 3.3V | | 3.5 | | |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time: low-to-high-level output and high-to-low level output | B | A | $V_{CCB}$ = 1.2V | | 3.1 | | ns |
| | | | | $V_{CCB}$ = 1.5V | | 2.7 | | |
| | | | | $V_{CCB}$ = 1.8V | | 2.5 | | |
| | | | | $V_{CCB}$ = 2.5V | | 2.4 | | |
| | | | | $V_{CCB}$ = 3.3V | | 2.3 | | |
| $t_{PZH}$, $t_{PZL}$ | Enable time: to high level and to low level | $\overline{OE}$ | A | $V_{CCB}$ = 1.2V | | 5.3 | | ns |
| | | | | $V_{CCB}$ = 1.5V | | 5.3 | | |
| | | | | $V_{CCB}$ = 1.8V | | 5.3 | | |
| | | | | $V_{CCB}$ = 2.5V | | 5.3 | | |
| | | | | $V_{CCB}$ = 3.3V | | 5.3 | | |
| $t_{PZH}$, $t_{PZL}$ | Enable time: to high level and to low level | $\overline{OE}$ | B | $V_{CCB}$ = 1.2V | | 5.1 | | ns |
| | | | | $V_{CCB}$ = 1.5V | | 4 | | |
| | | | | $V_{CCB}$ = 1.8V | | 3.5 | | |
| | | | | $V_{CCB}$ = 2.5V | | 3.2 | | |
| | | | | $V_{CCB}$ = 3.3V | | 3.1 | | |
| $t_{PHZ}$, $t_{PLZ}$ | Disable time: from high level and from low level | $\overline{OE}$ | A | $V_{CCB}$ = 1.2V | | 4.8 | | ns |
| | | | | $V_{CCB}$ = 1.5V | | 4.8 | | |
| | | | | $V_{CCB}$ = 1.8V | | 4.8 | | |
| | | | | $V_{CCB}$ = 2.5V | | 4.8 | | |
| | | | | $V_{CCB}$ = 3.3V | | 4.8 | | |
| $t_{PHZ}$, $t_{PLZ}$ | Disable time: from high level and from low level | $\overline{OE}$ | B | $V_{CCB}$ = 1.2V | | 4.7 | | ns |
| | | | | $V_{CCB}$ = 1.5V | | 4 | | |
| | | | | $V_{CCB}$ = 1.8V | | 4.1 | | |
| | | | | $V_{CCB}$ = 2.5V | | 4.3 | | |
| | | | | $V_{CCB}$ = 3.3V | | 5.1 | | |

## 5.7 Switching Characteristics, $V_{CCA}$= 1.5V ± 0.1V

All typical limits apply over $T_A$ = 25°C, and all maximum and minimum limits apply over $T_A$ = –40°C to 85°C (unless otherwise noted) (see 図 6-1)

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time: low-to-high-level output and high-to-low level output | A | B | $V_{CCB}$ = 1.2V | | 2.7 | | ns |
| | | | | $V_{CCB}$ = 1.5V | 0.5 | | 5.4 | |
| | | | | $V_{CCB}$ = 1.8V | 0.5 | | 4.6 | |
| | | | | $V_{CCB}$ = 2.5V | 0.5 | | 4.9 | |
| | | | | $V_{CCB}$ = 3.3V | 0.5 | | 6.8 | |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time: low-to-high-level output and high-to-low level output | B | A | $V_{CCB}$ = 1.2V | | 2.6 | | ns |
| | | | | $V_{CCB}$ = 1.5V | 0.5 | | 5.4 | |
| | | | | $V_{CCB}$ = 1.8V | 0.5 | | 5.1 | |
| | | | | $V_{CCB}$ = 2.5V | 0.5 | | 4.7 | |
| | | | | $V_{CCB}$ = 3.3V | 0.5 | | 4.5 | |
| $t_{PZH}$, $t_{PZL}$ | Enable time: to high level and to low level | $\overline{OE}$ | A | $V_{CCB}$ = 1.2V | | 3.7 | | ns |
| | | | | $V_{CCB}$ = 1.5V | 1.1 | | 8.7 | |
| | | | | $V_{CCB}$ = 1.8V | 1.1 | | 8.7 | |
| | | | | $V_{CCB}$ = 2.5V | 1.1 | | 8.7 | |
| | | | | $V_{CCB}$ = 3.3V | 1.1 | | 8.7 | |
| $t_{PZH}$, $t_{PZL}$ | Enable time: to high level and to low level | $\overline{OE}$ | B | $V_{CCB}$ = 1.2V | | 4.8 | | ns |
| | | | | $V_{CCB}$ = 1.5V | 1.1 | | 7.6 | |
| | | | | $V_{CCB}$ = 1.8V | 1.1 | | 7.1 | |
| | | | | $V_{CCB}$ = 2.5V | 1.1 | | 5.6 | |
| | | | | $V_{CCB}$ = 3.3V | 1.1 | | 5.2 | |
| $t_{PHZ}$, $t_{PLZ}$ | Disable time: from high level and from low level | $\overline{OE}$ | A | $V_{CCB}$ = 1.2V | | 3.1 | | ns |
| | | | | $V_{CCB}$ = 1.5V | 0.5 | | 8.6 | |
| | | | | $V_{CCB}$ = 1.8V | 0.5 | | 8.6 | |
| | | | | $V_{CCB}$ = 2.5V | 0.5 | | 8.6 | |
| | | | | $V_{CCB}$ = 3.3V | 0.5 | | 8.6 | |
| $t_{PHZ}$, $t_{PLZ}$ | Disable time: from high level and from low level | $\overline{OE}$ | B | $V_{CCB}$ = 1.2V | | 4.1 | | ns |
| | | | | $V_{CCB}$ = 1.5V | 0.5 | | 8.4 | |
| | | | | $V_{CCB}$ = 1.8V | 0.5 | | 7.6 | |
| | | | | $V_{CCB}$ = 2.5V | 0.5 | | 7.2 | |
| | | | | $V_{CCB}$ = 3.3V | 0.5 | | 7.8 | |

## 5.8 Switching Characteristics, $V_{CCA}$= 1.8V ± 0.15V

All typical limits apply over $T_A$ = 25°C, and all maximum and minimum limits apply over $T_A$ = –40°C to 85°C (unless otherwise noted) (see 図 6-1)

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time: low-to-high-level output and high-to-low level output | A | B | $V_{CCB}$ = 1.2V | | 2.5 | | ns |
| | | | | $V_{CCB}$ = 1.5V | 0.5 | | 5.1 | |
| | | | | $V_{CCB}$ = 1.8V | 0.5 | | 4.4 | |
| | | | | $V_{CCB}$ = 2.5V | 0.5 | | 4 | |
| | | | | $V_{CCB}$ = 3.3V | 0.5 | | 3.9 | |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time: low-to-high-level output and high-to-low level output | B | A | $V_{CCB}$ = 1.2V | | 2.5 | | ns |
| | | | | $V_{CCB}$ = 1.5V | 0.5 | | 4.6 | |
| | | | | $V_{CCB}$ = 1.8V | 0.5 | | 4.4 | |
| | | | | $V_{CCB}$ = 2.5V | 0.5 | | 3.9 | |
| | | | | $V_{CCB}$ = 3.3V | 0.5 | | 3.7 | |
| $t_{PZH}$, $t_{PZL}$ | Enable time: to high level and to low level | $\overline{OE}$ | A | $V_{CCB}$ = 1.2V | | 3 | | ns |
| | | | | $V_{CCB}$ = 1.5V | 1 | | 6.8 | |
| | | | | $V_{CCB}$ = 1.8V | 1 | | 6.8 | |
| | | | | $V_{CCB}$ = 2.5V | 1 | | 6.8 | |
| | | | | $V_{CCB}$ = 3.3V | 1 | | 6.8 | |
| $t_{PZH}$, $t_{PZL}$ | Enable time: to high level and to low level | $\overline{OE}$ | B | $V_{CCB}$ = 1.2V | | 4.6 | | ns |
| | | | | $V_{CCB}$ = 1.5V | 1.1 | | 8.2 | |
| | | | | $V_{CCB}$ = 1.8V | 1 | | 6.7 | |
| | | | | $V_{CCB}$ = 2.5V | 0.5 | | 5.1 | |
| | | | | $V_{CCB}$ = 3.3V | 0.5 | | 4.5 | |
| $t_{PHZ}$, $t_{PLZ}$ | Disable time: from high level and from low level | $\overline{OE}$ | A | $V_{CCB}$ = 1.2V | | 2.8 | | ns |
| | | | | $V_{CCB}$ = 1.5V | 0.5 | | 7.1 | |
| | | | | $V_{CCB}$ = 1.8V | 0.5 | | 7.1 | |
| | | | | $V_{CCB}$ = 2.5V | 0.5 | | 7.1 | |
| | | | | $V_{CCB}$ = 3.3V | 0.5 | | 7.1 | |
| $t_{PHZ}$, $t_{PLZ}$ | Disable time: from high level and from low level | $\overline{OE}$ | B | $V_{CCB}$ = 1.2V | | 3.9 | | ns |
| | | | | $V_{CCB}$ = 1.5V | 0.5 | | 7.8 | |
| | | | | $V_{CCB}$ = 1.8V | 0.5 | | 6.9 | |
| | | | | $V_{CCB}$ = 2.5V | 0.5 | | 6 | |
| | | | | $V_{CCB}$ = 3.3V | 0.5 | | 5.8 | |

### 5.9 Switching Characteristics, $V_{CCA}$= 2.5V ± 0.2V

All typical limits apply over $T_A$ = 25°C, and all maximum and minimum limits apply over $T_A$ = –40°C to 85°C (unless otherwise noted) (see 図 6-1)

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time: low-to-high-level output and high-to-low level output | A | B | $V_{CCB}$ = 1.2V | | 2.4 | | ns |
| | | | | $V_{CCB}$ = 1.5V | 0.5 | | 4.7 | |
| | | | | $V_{CCB}$ = 1.8V | 0.5 | | 3.9 | |
| | | | | $V_{CCB}$ = 2.5V | 0.5 | | 3.1 | |
| | | | | $V_{CCB}$ = 3.3V | 0.5 | | 2.8 | |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time: low-to-high-level output and high-to-low level output | B | A | $V_{CCB}$ = 1.2V | | 3 | | ns |
| | | | | $V_{CCB}$ = 1.5V | 0.5 | | 4.9 | |
| | | | | $V_{CCB}$ = 1.8V | 0.5 | | 4 | |
| | | | | $V_{CCB}$ = 2.5V | 0.5 | | 3.1 | |
| | | | | $V_{CCB}$ = 3.3V | 0.5 | | 2.9 | |
| $t_{PZH}$, $t_{PZL}$ | Enable time: to high level and to low level | $\overline{OE}$ | A | $V_{CCB}$ = 1.2V | | 2.2 | | ns |
| | | | | $V_{CCB}$ = 1.5V | 0.5 | | 4.8 | |
| | | | | $V_{CCB}$ = 1.8V | 0.5 | | 4.8 | |
| | | | | $V_{CCB}$ = 2.5V | 0.5 | | 4.8 | |
| | | | | $V_{CCB}$ = 3.3V | 0.5 | | 4.8 | |
| $t_{PZH}$, $t_{PZL}$ | Enable time: to high level and to low level | $\overline{OE}$ | B | $V_{CCB}$ = 1.2V | | 4.5 | | ns |
| | | | | $V_{CCB}$ = 1.5V | 1.1 | | 7.9 | |
| | | | | $V_{CCB}$ = 1.8V | 0.5 | | 6.4 | |
| | | | | $V_{CCB}$ = 2.5V | 0.5 | | 4.6 | |
| | | | | $V_{CCB}$ = 3.3V | 0.5 | | 4 | |
| $t_{PHZ}$, $t_{PLZ}$ | Disable time: from high level and from low level | $\overline{OE}$ | A | $V_{CCB}$ = 1.2V | | 1.8 | | ns |
| | | | | $V_{CCB}$ = 1.5V | 0.5 | | 5.1 | |
| | | | | $V_{CCB}$ = 1.8V | 0.5 | | 5.1 | |
| | | | | $V_{CCB}$ = 2.5V | 0.5 | | 5.1 | |
| | | | | $V_{CCB}$ = 3.3V | 0.5 | | 5.1 | |
| $t_{PHZ}$, $t_{PLZ}$ | Disable time: from high level and from low level | $\overline{OE}$ | B | $V_{CCB}$ = 1.2V | | 3.6 | | ns |
| | | | | $V_{CCB}$ = 1.5V | 0.5 | | 7.1 | |
| | | | | $V_{CCB}$ = 1.8V | 0.5 | | 6.3 | |
| | | | | $V_{CCB}$ = 2.5V | 0.5 | | 5.1 | |
| | | | | $V_{CCB}$ = 3.3V | 0.5 | | 3.9 | |

## 5.10 Switching Characteristics, $V_{CCA}$= 3.3V ± 0.3V

All typical limits apply over $T_A$ = 25°C, and all maximum and minimum limits apply over $T_A$ = –40°C to 85°C (unless otherwise noted) (see 図 6-1)

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|---|
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time: low-to-high-level output and high-to-low level output | A | B | $V_{CCB}$ = 1.2V | | 2.3 | | ns |
| | | | | $V_{CCB}$ = 1.5V | 0.5 | | 4.5 | |
| | | | | $V_{CCB}$ = 1.8V | 0.5 | | 3.7 | |
| | | | | $V_{CCB}$ = 2.5V | 0.5 | | 2.9 | |
| | | | | $V_{CCB}$ = 3.3V | 0.5 | | 2.5 | |
| $t_{PLH}$, $t_{PHL}$ | Propagation delay time: low-to-high-level output and high-to-low level output | B | A | $V_{CCB}$ = 1.2V | | 3.5 | | ns |
| | | | | $V_{CCB}$ = 1.5V | 0.5 | | 6.8 | |
| | | | | $V_{CCB}$ = 1.8V | 0.5 | | 3.9 | |
| | | | | $V_{CCB}$ = 2.5V | 0.5 | | 2.8 | |
| | | | | $V_{CCB}$ = 3.3V | 0.5 | | 2.5 | |
| $t_{PZH}$, $t_{PZL}$ | Enable time: to high level and to low level | $\overline{OE}$ | A | $V_{CCB}$ = 1.2V | | 2 | | ns |
| | | | | $V_{CCB}$ = 1.5V | 0.5 | | 4 | |
| | | | | $V_{CCB}$ = 1.8V | 0.5 | | 4 | |
| | | | | $V_{CCB}$ = 2.5V | 0.5 | | 4 | |
| | | | | $V_{CCB}$ = 3.3V | 0.5 | | 4 | |
| $t_{PZH}$, $t_{PZL}$ | Enable time: to high level and to low level | $\overline{OE}$ | B | $V_{CCB}$ = 1.2V | | 4.5 | | ns |
| | | | | $V_{CCB}$ = 1.5V | 1.1 | | 7.8 | |
| | | | | $V_{CCB}$ = 1.8V | 0.5 | | 6.2 | |
| | | | | $V_{CCB}$ = 2.5V | 0.5 | | 4.5 | |
| | | | | $V_{CCB}$ = 3.3V | 0.5 | | 3.9 | |
| $t_{PHZ}$, $t_{PLZ}$ | Disable time: from high level and from low level | $\overline{OE}$ | A | $V_{CCB}$ = 1.2V | | 1.7 | | ns |
| | | | | $V_{CCB}$ = 1.5V | 0.5 | | 4 | |
| | | | | $V_{CCB}$ = 1.8V | 0.5 | | 4 | |
| | | | | $V_{CCB}$ = 2.5V | 0.5 | | 4 | |
| | | | | $V_{CCB}$ = 3.3V | 0.5 | | 4 | |
| $t_{PHZ}$, $t_{PLZ}$ | Disable time: from high level and from low level | $\overline{OE}$ | B | $V_{CCB}$ = 1.2V | | 3.4 | | ns |
| | | | | $V_{CCB}$ = 1.5V | 0.5 | | 6.9 | |
| | | | | $V_{CCB}$ = 1.8V | 0.5 | | 6 | |
| | | | | $V_{CCB}$ = 2.5V | 0.5 | | 4.8 | |
| | | | | $V_{CCB}$ = 3.3V | 0.5 | | 4.2 | |

## 5.11 Operating Characteristics

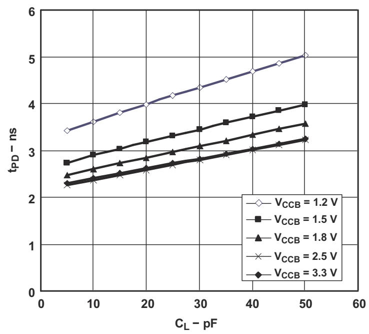
$T_A$= 25°C

| PARAMETER | | FROM (INPUT) | TO (OUTPUT) | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|---|---|
| $C_{pdA}$ | Power dissipation capacitance per transceiver[(1)] port A - outputs enabled | A | B | $C_L$ = 0pF, f = 10MHz, $t_r$ = $t_f$ = 1ns | $V_{CCA}$ = $V_{CCB}$ = 1.2V | 1 | pF |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 1.5V | 1 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 1.8V | 1 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 2.5V | 1 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 3.3V | 1 | |
| | Power dissipation capacitance per transceiver[(1)] port A - outputs disabled | A | B | $C_L$ = 0pF, f = 10MHz, $t_r$ = $t_f$ = 1ns | $V_{CCA}$ = $V_{CCB}$ = 1.2V | 1 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 1.5V | 1 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 1.8V | 1 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 2.5V | 1 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 3.3V | 1 | |
| | Power dissipation capacitance per transceiver[(1)] port A - outputs enabled | B | A | $C_L$ = 0pF, f = 10MHz, $t_r$ = $t_f$ = 1ns | $V_{CCA}$ = $V_{CCB}$ = 1.2V | 12 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 1.5V | 12 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 1.8V | 12 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 2.5V | 13 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 3.3V | 14 | |
| | Power dissipation capacitance per transceiver[(1)] port A - outputs disabled | B | A | $C_L$ = 0pF, f = 10MHz, $t_r$ = $t_f$ = 1ns | $V_{CCA}$ = $V_{CCB}$ = 1.2V | 1 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 1.5V | 1 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 1.8V | 1 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 2.5V | 1 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 3.3V | 1 | |
| $C_{pdB}$ | Power dissipation capacitance per transceiver[(1)] port B - outputs enabled | A | B | $C_L$ = 0pF, f = 10MHz, $t_r$ = $t_f$ = 1ns | $V_{CCA}$ = $V_{CCB}$ = 1.2V | 12 | pF |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 1.5V | 12 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 1.8V | 12 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 2.5V | 13 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 3.3V | 14 | |
| | Power dissipation capacitance per transceiver[(1)] port B - outputs disabled | A | B | $C_L$ = 0pF, f = 10MHz, $t_r$ = $t_f$ = 1ns | $V_{CCA}$ = $V_{CCB}$ = 1.2V | 1 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 1.5V | 1 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 1.8V | 1 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 2.5V | 1 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 3.3V | 1 | |
| | Power dissipation capacitance per transceiver[(1)] port B - outputs enabled | B | A | $C_L$ = 0pF, f = 10MHz, $t_r$ = $t_f$ = 1ns | $V_{CCA}$ = $V_{CCB}$ = 1.2V | 1 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 1.5V | 1 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 1.8V | 1 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 2.5V | 1 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 3.3V | 1 | |
| | Power dissipation capacitance per transceiver[(1)] port B - outputs disabled | B | A | $C_L$ = 0pF, f = 10MHz, $t_r$ = $t_f$ = 1ns | $V_{CCA}$ = $V_{CCB}$ = 1.2V | 1 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 1.5V | 1 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 1.8V | 1 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 2.5V | 1 | |
| | | | | | $V_{CCA}$ = $V_{CCB}$ = 3.3V | 1 | |

(1) See to TI application report, *CMOS Power Consumption and Cpd Calculation* (SCAA035).

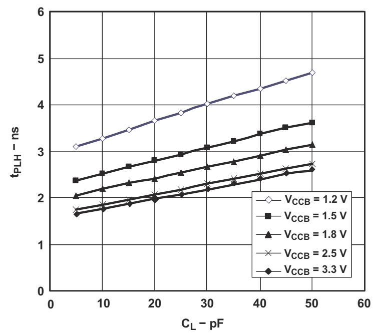
## 5.12 Typical Characteristics

$T_A$ = 25°C



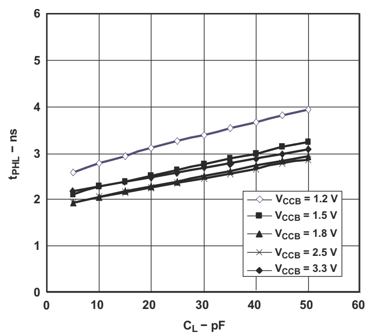

$V_{CCA}$ = 1.2V

**図 5-1. Typical Propagation Delay (A to B) vs Load Capacitance**



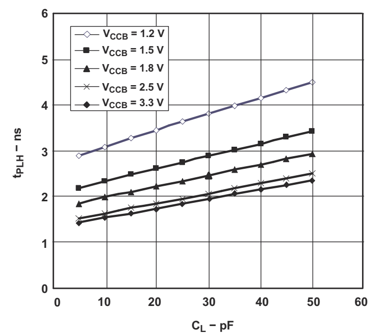

$V_{CCA}$ = 1.5V

**図 5-2. Typical Propagation Delay (A to B) vs Load Capacitance**



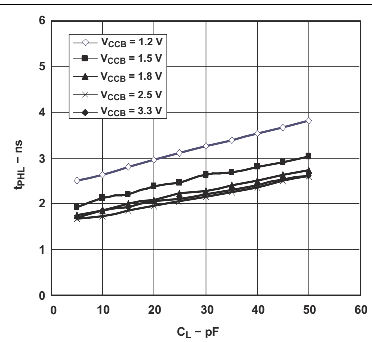

$V_{CCA}$ = 1.5V

**図 5-3. Typical Propagation Delay (A to B) vs Load Capacitance**



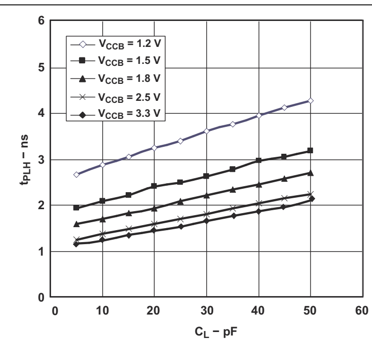

$V_{CCA}$ = 1.8V

**図 5-4. Typical Propagation Delay (A to B) vs Load Capacitance**




$V_{CCA}$ = 1.8V

**図 5-5. Typical Propagation Delay (A to B) vs Load Capacitance**

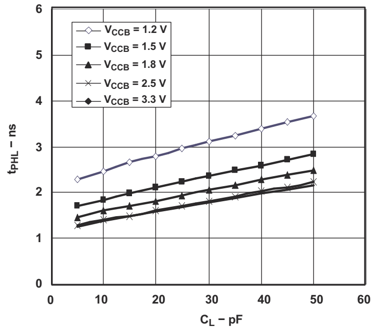



$V_{CCA}$ = 2.5V

**図 5-6. Typical Propagation Delay (A to B) vs Load Capacitance**

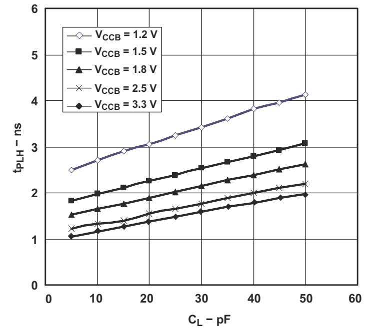
## 5.12 Typical Characteristics (continued)

$T_A$ = 25°C



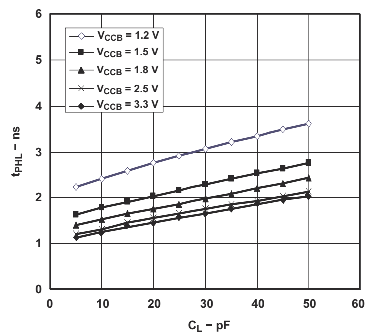

$V_{CCA}$ = 2.5V

**図 5-7. Typical Propagation Delay (A to B) vs Load Capacitance**




$V_{CCA}$ = 3.3V

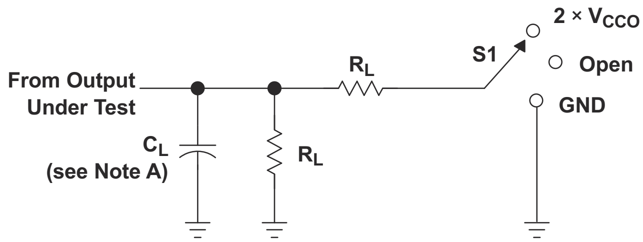
**図 5-8. Typical Propagation Delay (A to B) vs Load Capacitance**




$V_{CCA}$ = 3.3V

**図 5-9. Typical Propagation Delay (A to B) vs Load Capacitance**

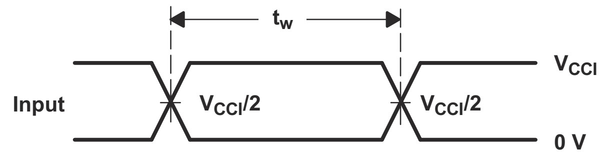
## 6 Parameter Measurement Information



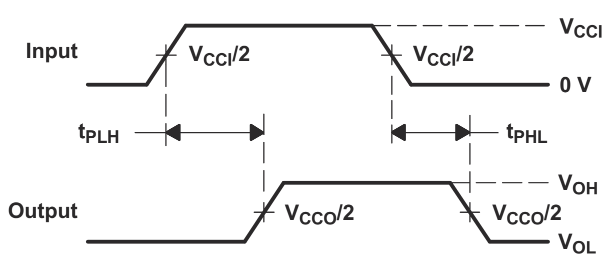

LOAD CIRCUIT

| TEST | S1 |
|---|---|
| $t_{pd}$ | Open |
| $t_{PLZ}/t_{PZL}$ | 2 × $V_{CCO}$ |
| $t_{PHZ}/t_{PZH}$ | GND |

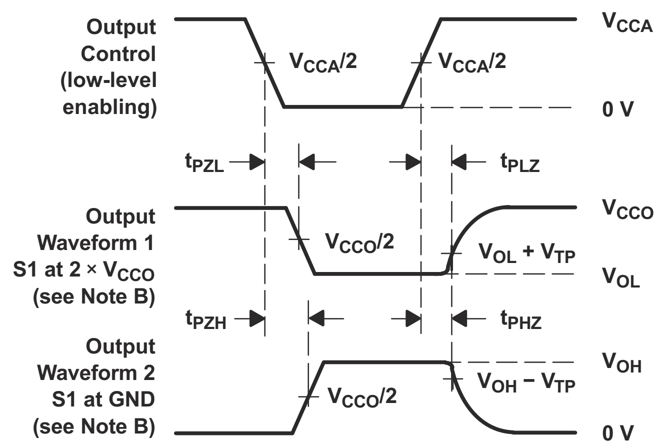
| $V_{CCO}$ | $C_L$ | $R_L$ | $V_{TP}$ |
|---|---|---|---|
| 1.2 V | 15 pF | 2 kΩ | 0.1 V |
| 1.5 V ± 0.1 V | 15 pF | 2 kΩ | 0.1 V |
| 1.8 V ± 0.15 V | 15 pF | 2 kΩ | 0.15 V |
| 2.5 V ± 0.2 V | 15 pF | 2 kΩ | 0.15 V |
| 3.3 V ± 0.3 V | 15 pF | 2 kΩ | 0.3 V |




VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

NOTES:
- A. $C_L$ includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, $Z_O$ = 50Ω, dv/dt ≥ 1 V/ns.
- D. The outputs are measured one at a time, with one transition per measurement.
- E. $t_{PLZ}$ and $t_{PHZ}$ are the same as $t_{dis}$.
- F. $t_{PZL}$ and $t_{PZH}$ are the same as $t_{en}$.
- G. $t_{PLH}$ and $t_{PHL}$ are the same as $t_{pd}$.
- H. $V_{CCI}$ is the $V_{CC}$ associated with the input port.
- I. $V_{CCO}$ is the $V_{CC}$ associated with the output port.

**図 6-1. Load Circuit and Voltage Waveforms**

# 7 Detailed Description

## 7.1 Overview

The SN74AVCH8T245 is an 8-bit, dual supply noninverting bidirectional voltage level translator. Pins A1 through A4, and the control pins (DIR and $\overline{OE}$) are referenced to $V_{CCA}$, while pins B1 through B4 are referenced to $V_{CCB}$. Both the A port and B port can accept I/O voltages ranging from 1.2V to 3.6V. With $\overline{OE}$ set to low, a high on DIR allows data transmission from Port A to Port B, and a low on DIR allows data transmission from Port B to Port A. When $\overline{OE}$ is set to high, both Port A and Port B outputs are in the high-impedance state. For more information, see *AVC Logic Family Technology and Application*.

## 7.2 Functional Block Diagram

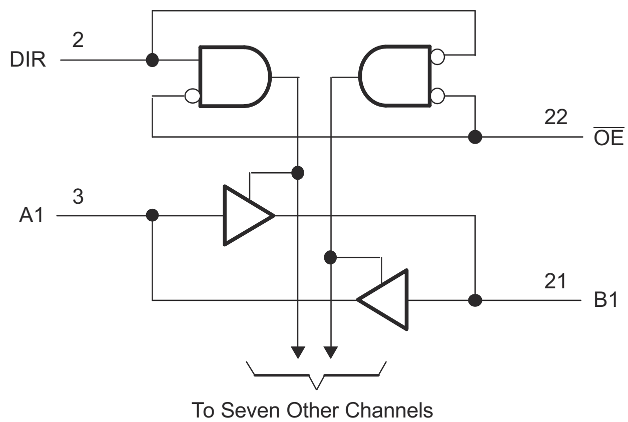



**図 7-1. Logic Diagram (Positive Logic)**

## 7.3 Feature Description

### 7.3.1 Fully Configurable Dual-Rail Design

Both $V_{CCA}$ and $V_{CCB}$ can be supplied at any voltage from 1.2V to 3.6V, making the device an excellent choice for translating between any of the low voltage nodes: 1.2V, 1.8V, 2.5V, and 3.3V.

**表 7-1. Typical Total Static Power Consumption ($I_{CCA}$ + $I_{CCB}$)**

| $V_{CCB}$ | $V_{CCA}$ | | | | | | UNIT |
|---|---|---|---|---|---|---|---|
| | 0V | 1.2V | 1.5V | 1.8V | 2.5V | 3.3V | |
| 0V | 0 | <0.5 | <0.5 | <0.5 | <0.5 | <0.5 | μA |
| 1.2V | <0.5 | <1 | <1 | <1 | <1 | 1 | |
| 1.5V | <0.5 | <1 | <1 | <1 | <1 | 1 | |
| 1.8V | <0.5 | <1 | <1 | <1 | <1 | <1 | |
| 2.5V | <0.5 | 1 | <1 | <1 | <1 | <1 | |
| 3.3V | <0.5 | 1 | <1 | <1 | <1 | <1 | |

### 7.3.2 Supports High-Speed Translation

SN74AVCH8T245 can support high data rate applications, which can be calculated from the maximum propagation delay. This is also dependent on output load. The translated signal data rate can be up to 320Mbps when both $V_{CCA}$ and $V_{CCB}$ are at least 1.8V.

### 7.3.3 Partial-Power-Down Mode Operation

$I_{off}$ circuitry disables the outputs, preventing damaging current backflow through the SN74AVCH8T245 when it is powered down. Damaging current backflow can occur in applications where subsections of a system are powered down (partial-power-down) to reduce power consumption.

### 7.3.4 Bus-Hold Circuitry

Active bus-hold circuitry holds unused or undriven data inputs at a valid logic state, which helps with board space savings and reduced component costs. Use of pull-up or pull-down resistors with the bus-hold circuitry is not recommended. For more information, see *Bus-Hold Circuit*.

### 7.3.5 $V_{CC}$ Isolation Feature

The $V_{CC}$ isolation feature allows both ports to be in a high-impedance state if either $V_{CCA}$ or $V_{CCB}$ are at GND (or < 0.4V). For more information, see $I_{OZ}$ in the *Electrical Characteristics*. This feature prevents false logic levels from being presented to either bus.

## 7.4 Device Functional Modes

表 7-2 lists the functional modes of the SN74AVCH8T245.

**表 7-2. Function Table (Each 8-Bit Section)**

| CONTROL INPUTS[(1)] | | OUTPUT CIRCUITS | | OPERATION |
|---|---|---|---|---|
| $\overline{OE}$ | DIR | A PORT | B PORT | |
| L | L | Enabled | Hi-Z | B data to A bus |
| L | H | Hi-Z | Enabled | A data to B bus |
| H | X | Hi-Z | Hi-Z | Isolation |

(1) Input circuits of the data I/Os are always active.

# 8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

## 8.1 Application Information

The SN74AVCH8T245 device can be used in level-translation applications for interfacing devices or systems operating at different interface voltages with one another. The SN74AVCH8T245 device is an excellent choice for data transmission when direction is different. The maximum data rate can be up to 320Mbps when device voltage power supply is more than 1.8V.

## 8.2 Typical Application

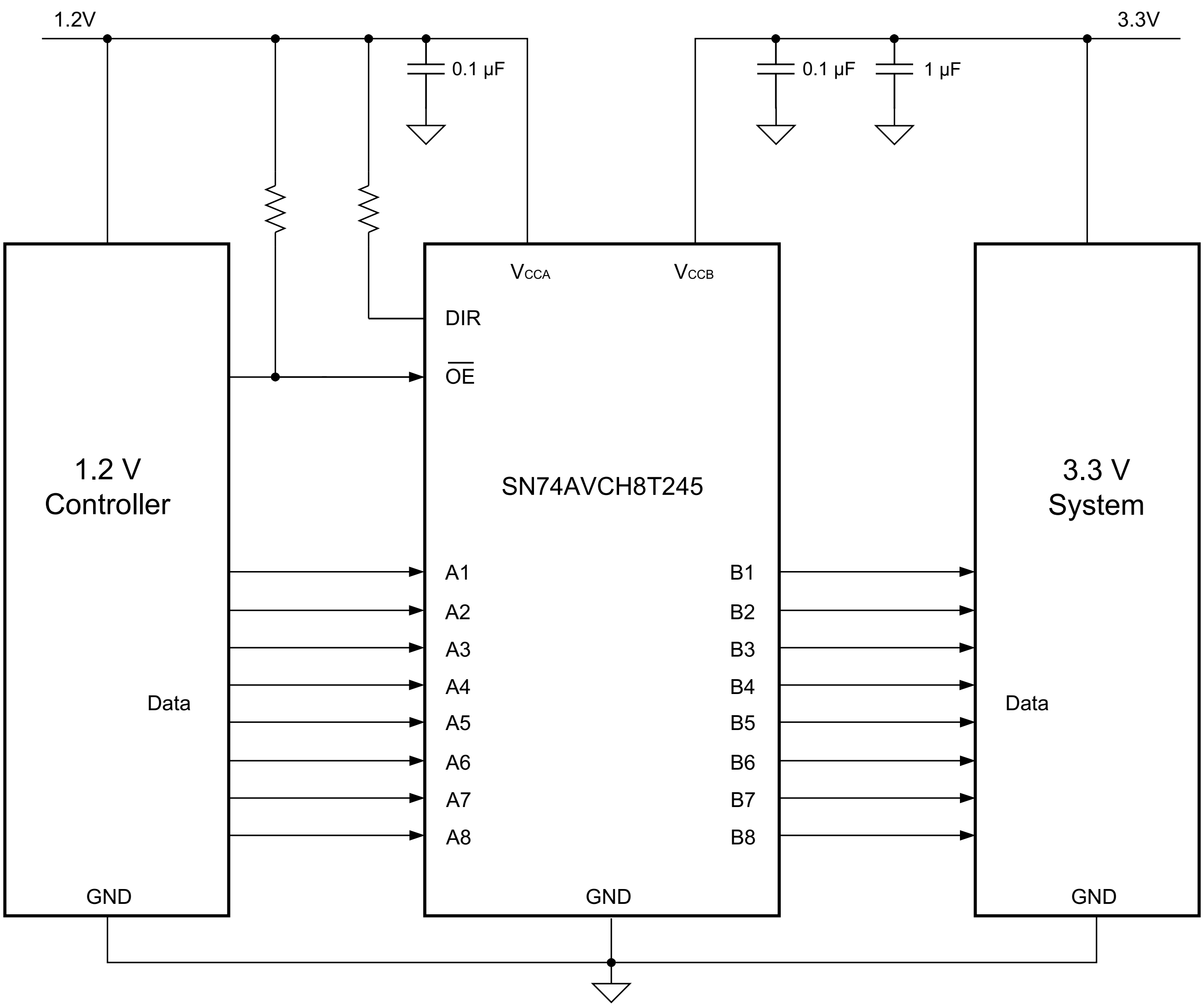



**図 8-1. Typical Application Schematic**

### 8.2.1 Design Requirements

For this design example, use the parameters listed in 表 8-1.

**表 8-1. Design Parameters**

| DESIGN PARAMETERS | EXAMPLE VALUE |
|---|---|
| Input voltage | 1.2V to 3.6V |
| Output voltage | 1.2V to 3.6V |

### 8.2.2 Detailed Design Procedure

To begin the design process, determine the following:

- Input voltage range:
  - Use the supply voltage of the device that is driving the SN74AVCH8T245 device to determine the input voltage range. For a valid logic high, the value must exceed the $V_{IH}$ of the input port. For a valid logic low, the value must be less than the $V_{IL}$ of the input port.
- Output voltage range:
  - Use the supply voltage of the device that the SN74AVCH8T245 device is driving to determine the output voltage range.

### 8.2.3 Application Curves

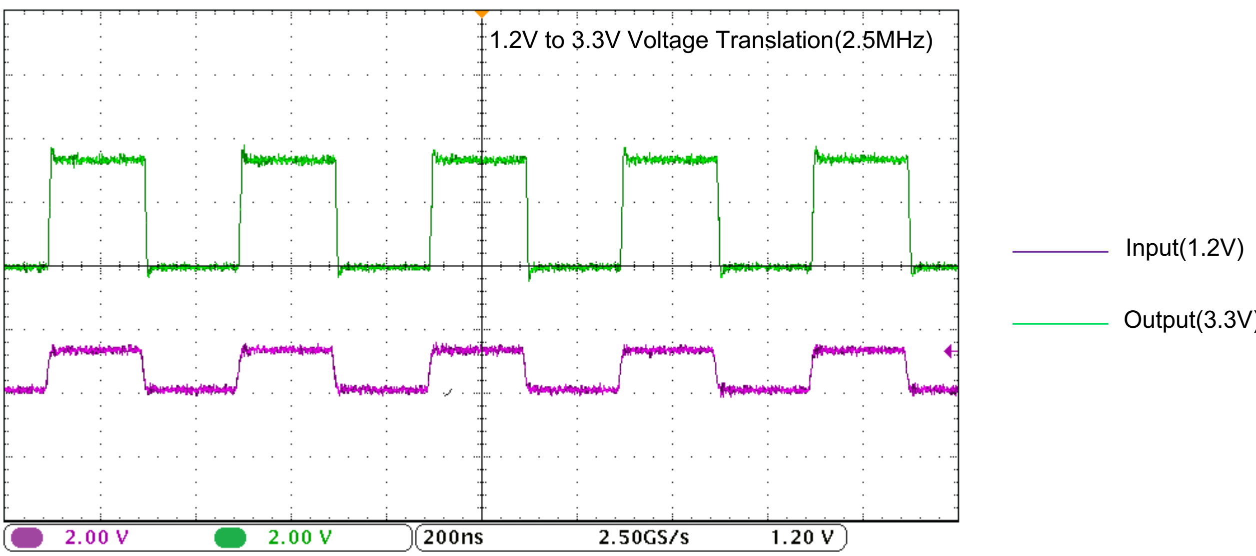



**図 8-2. Translation Up (1.2V to 3.3V) at 2.5MHz**

## 8.3 Power Supply Recommendations

The design of the output-enable ($\overline{OE}$) input circuit is referenced to VCCA so that all outputs are placed in the high-impedance state when the $\overline{OE}$ input is high. To put the outputs in a high-impedance state during power up or power down, the $\overline{OE}$ input pin must be tied to $V_{CCA}$ through a pullup resistor and must not be enabled until $V_{CCA}$ and $V_{CCB}$ are fully ramped and stable. The current-sinking capability of the driver determines the minimum value of the pullup resistor to $V_{CCA}$.

$V_{CCA}$ or $V_{CCB}$ can be powered up first. If the SN74AVCH8T245 is powered up in a permanently enabled state (for example $\overline{OE}$ is always kept low), then pullup resistors are recommended at the input. Doing this allows for proper, glitch-free, power-up. For more information, see *Designing with SN4LVCXT245 and SN74LVCHXT245 Family of Direction Controlled Voltage Translators/Level-Shifters*. In addition, the $\overline{OE}$ pin may be shorted to GND if the application does not require use of the high-impedance state at any time.

## 8.4 Layout

### 8.4.1 Layout Guidelines

For device reliability, TI recommends following the common printed-circuit board layout guidelines.

- Use bypass capacitors on power supplies.
- Use short trace lengths to avoid excessive loading.
- Placing pads on the signal paths for loading capacitors or pullup resistors to help adjust rise and fall times of signals depending on the system requirements.

### 8.4.2 Layout Example

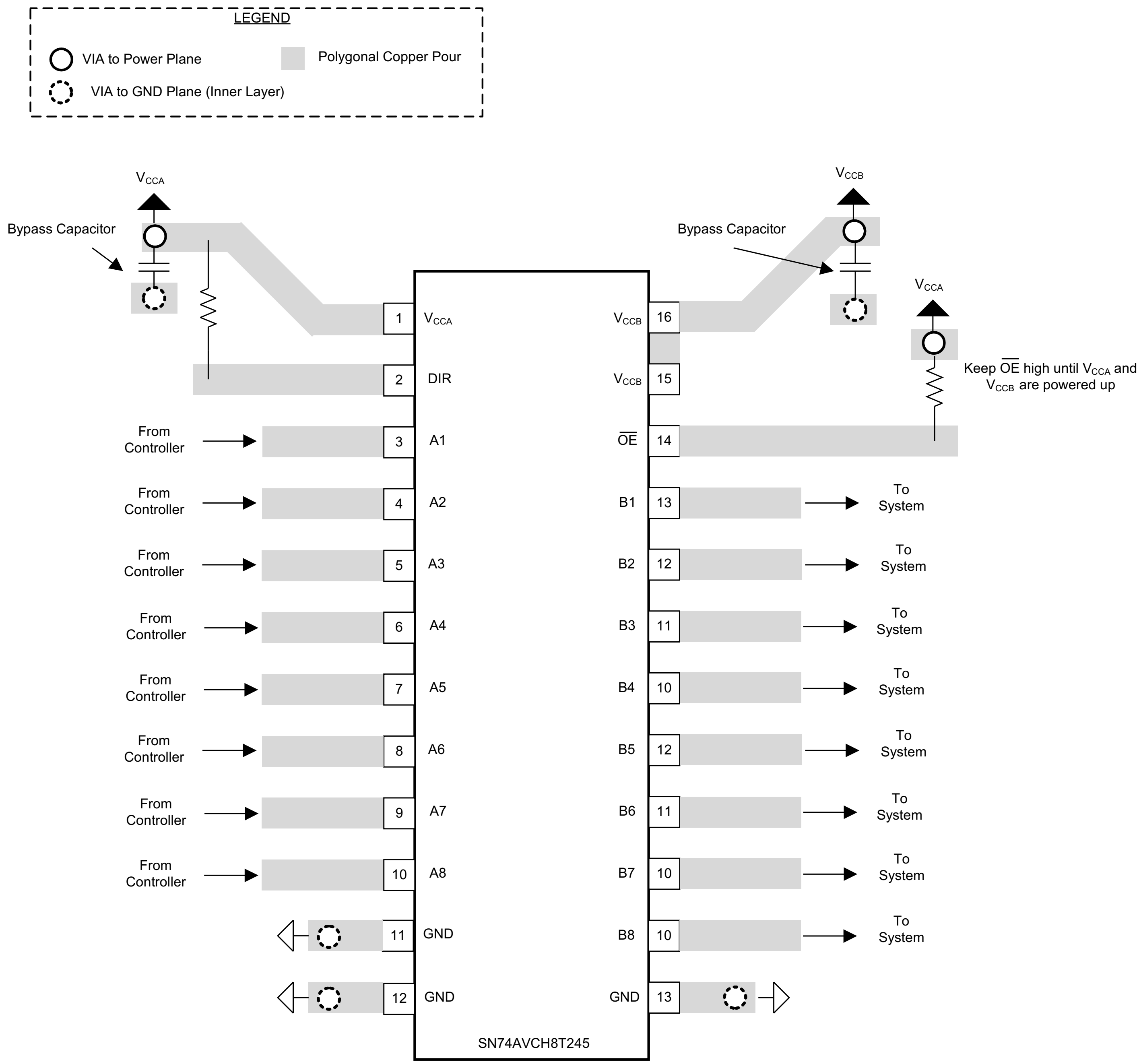



**図 8-3. SN74AVCH8T245 Layout Example**

# 9 Device and Documentation Support

## 9.1 Documentation Support

### 9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Designing with SN74LVCXT245 and SN74LVCHXT245 Family of Direction Controlled Voltage Translators/Level-Shifters*
- Texas Instruments, *Bus-Hold Circuit*
- Texas Instruments, *AVC Logic Family Technology and Applications*
- Texas Instruments, *CMOS Power Consumption and Cpd Calculation*

## 9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

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## 9.6 用語集

| | |
|---|---|
| テキサス・インスツルメンツ用語集 | この用語集には、用語や略語の一覧および定義が記載されています。 |

# 10 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

| Changes from Revision I (November 2023) to Revision J (April 2024) | Page |
|---|---|
| • Changed kW to kΩ in the *Load Circuit and Voltage Waveforms* figure | 16 |

| Changes from Revision H (January 2016) to Revision I (November 2023) | Page |
|---|---|
| • ドキュメント全体にわたって表、図、相互参照の採番方法を更新 | 1 |
| • パッケージ リード サイズを含めるよう「パッケージ情報」表を更新 | 1 |
| • Updated the *Thermal Information* table for the *DGV*, *PW*, and *RHL* packages | 6 |

**Changes from Revision G (March 2007) to Revision H (January 2016)** **Page**

- 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加。 ............................................................................................ 1
- 「注文情報」表を削除 ........................................................................................................................................ 1

## 11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 74AVCH8T245PWRG4 | ACTIVE | TSSOP | PW | 24 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | WP245 | Samples |
| 74AVCH8T245RHLRG4 | ACTIVE | VQFN | RHL | 24 | 1000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | WP245 | Samples |
| SN74AVCH8T245DGVR | ACTIVE | TVSOP | DGV | 24 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | WP245 | Samples |
| SN74AVCH8T245PW | ACTIVE | TSSOP | PW | 24 | 60 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | WP245 | Samples |
| SN74AVCH8T245PWG4 | ACTIVE | TSSOP | PW | 24 | 60 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | WP245 | Samples |
| SN74AVCH8T245PWR | ACTIVE | TSSOP | PW | 24 | 2000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | WP245 | Samples |
| SN74AVCH8T245RHLR | ACTIVE | VQFN | RHL | 24 | 1000 | RoHS & Green | NIPDAU | Level-2-260C-1 YEAR | -40 to 85 | WP245 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

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**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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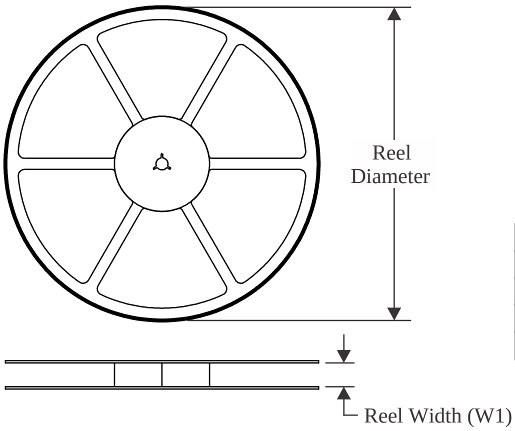
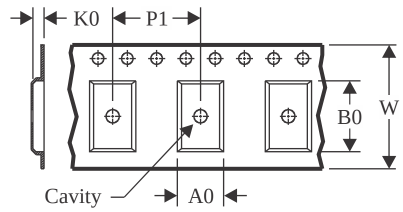
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

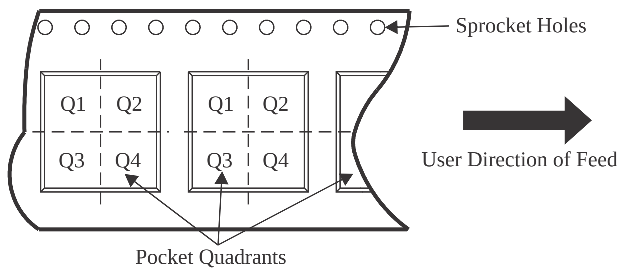



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

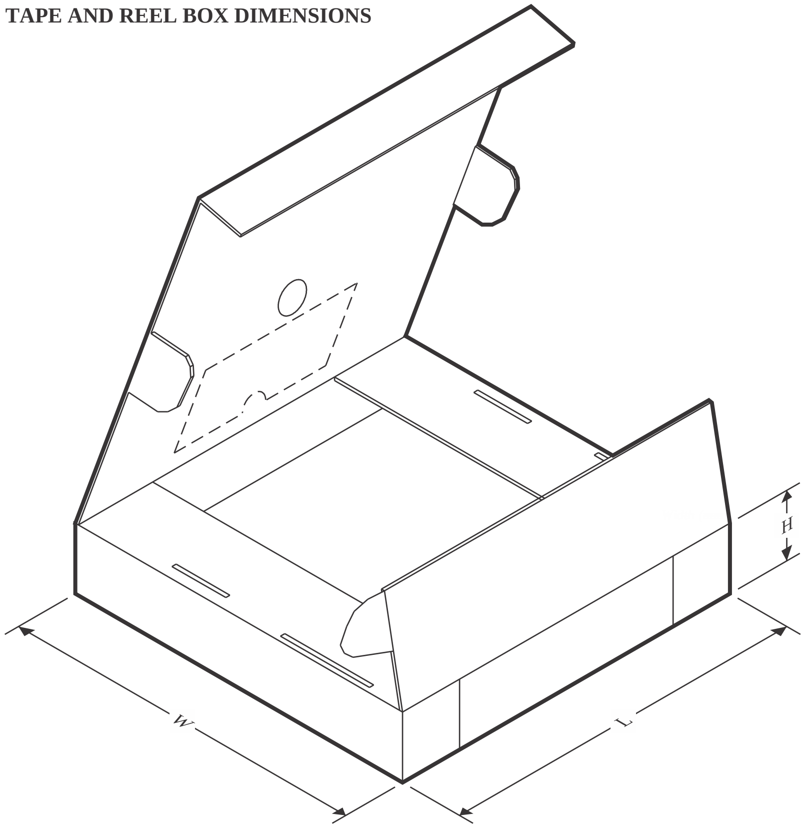
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AVCH8T245DGVR | TVSOP | DGV | 24 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AVCH8T245PWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |
| SN74AVCH8T245RHLR | VQFN | RHL | 24 | 1000 | 180.0 | 12.4 | 3.8 | 5.8 | 1.2 | 8.0 | 12.0 | Q1 |

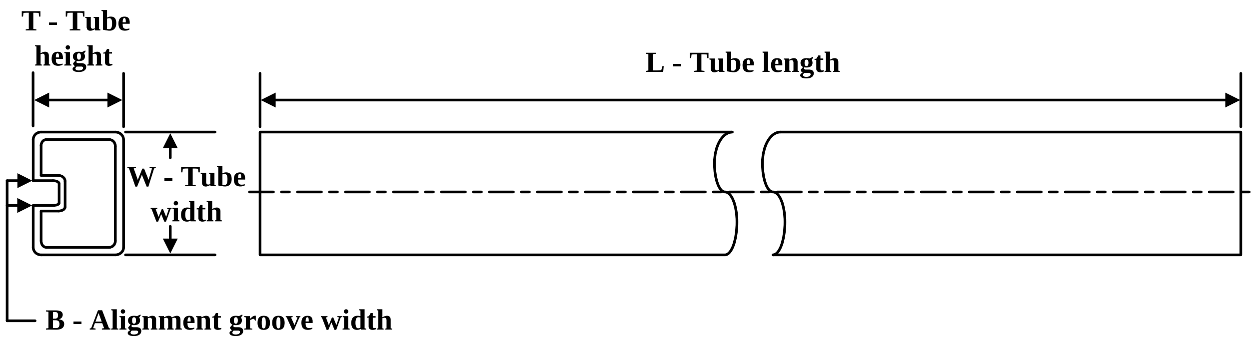
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74AVCH8T245DGVR | TVSOP | DGV | 24 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74AVCH8T245PWR | TSSOP | PW | 24 | 2000 | 356.0 | 356.0 | 35.0 |
| SN74AVCH8T245RHLR | VQFN | RHL | 24 | 1000 | 210.0 | 185.0 | 35.0 |

## TUBE

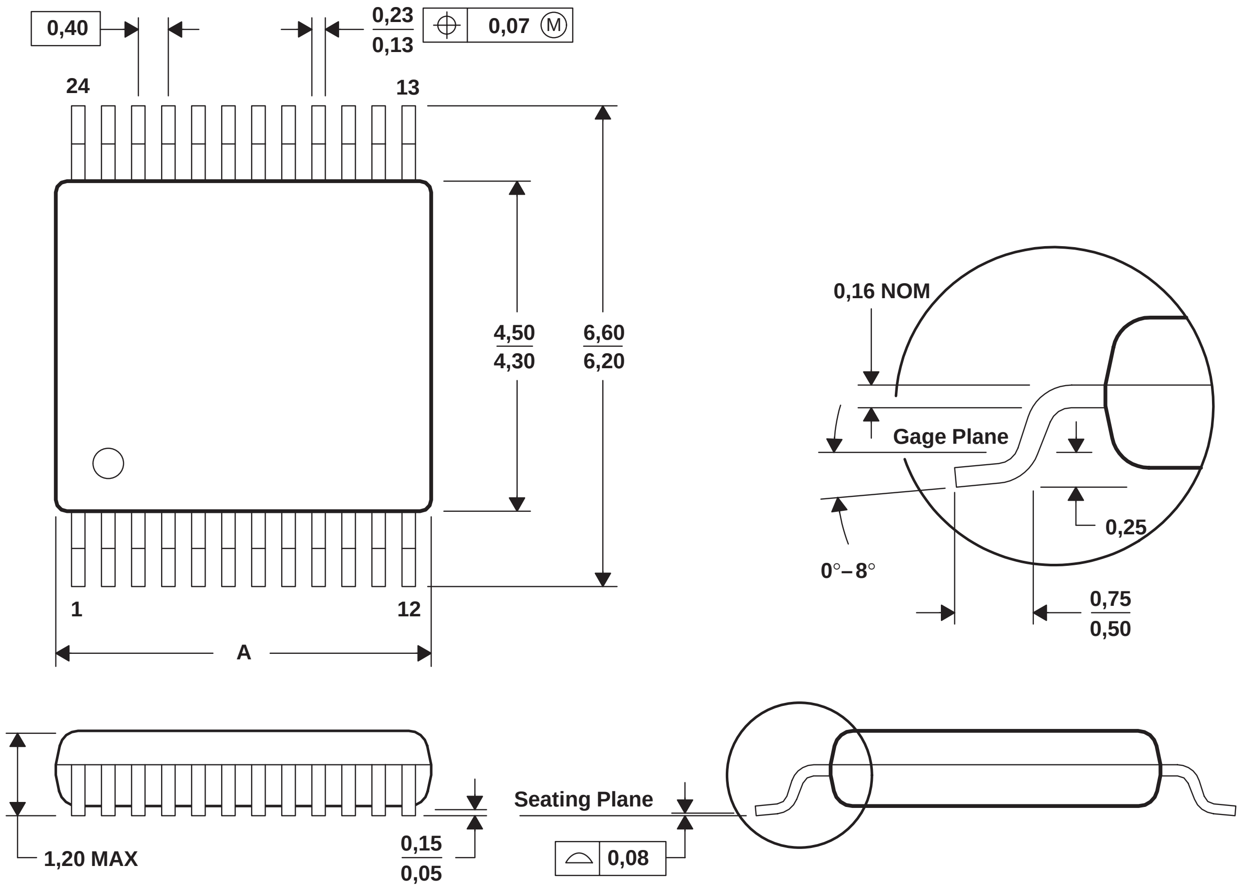



*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| SN74AVCH8T245PW | PW | TSSOP | 24 | 60 | 530 | 10.2 | 3600 | 3.5 |
| SN74AVCH8T245PWG4 | PW | TSSOP | 24 | 60 | 530 | 10.2 | 3600 | 3.5 |

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**




| PINS ** / DIM | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| **A MAX** | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| **A MIN** | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

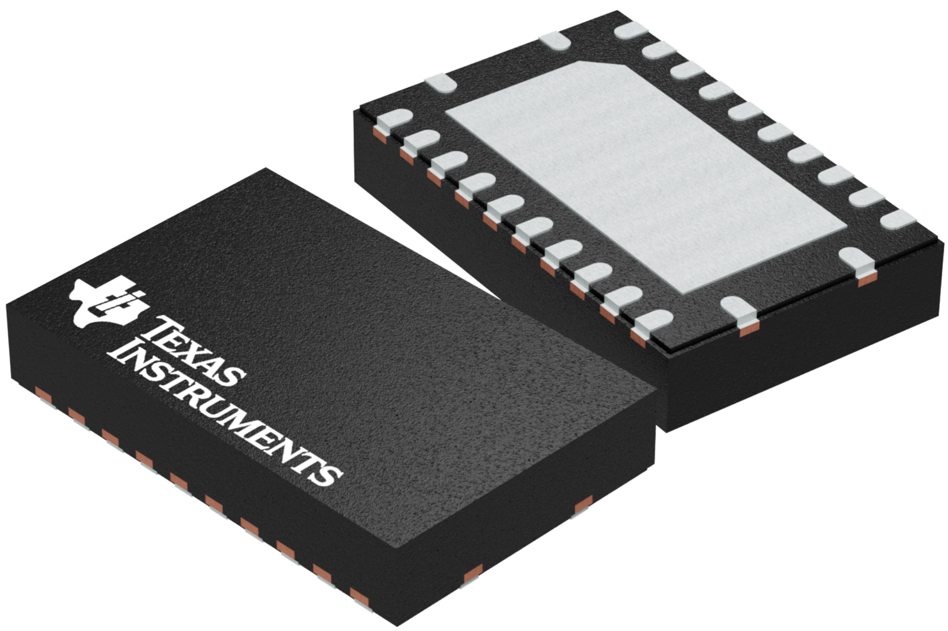
NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
- D. Falls within JEDEC: 24/48 Pins – MO-153
  14/16/20/56 Pins – MO-194

# GENERIC PACKAGE VIEW

# RGY 24 VQFN - 1 mm max height

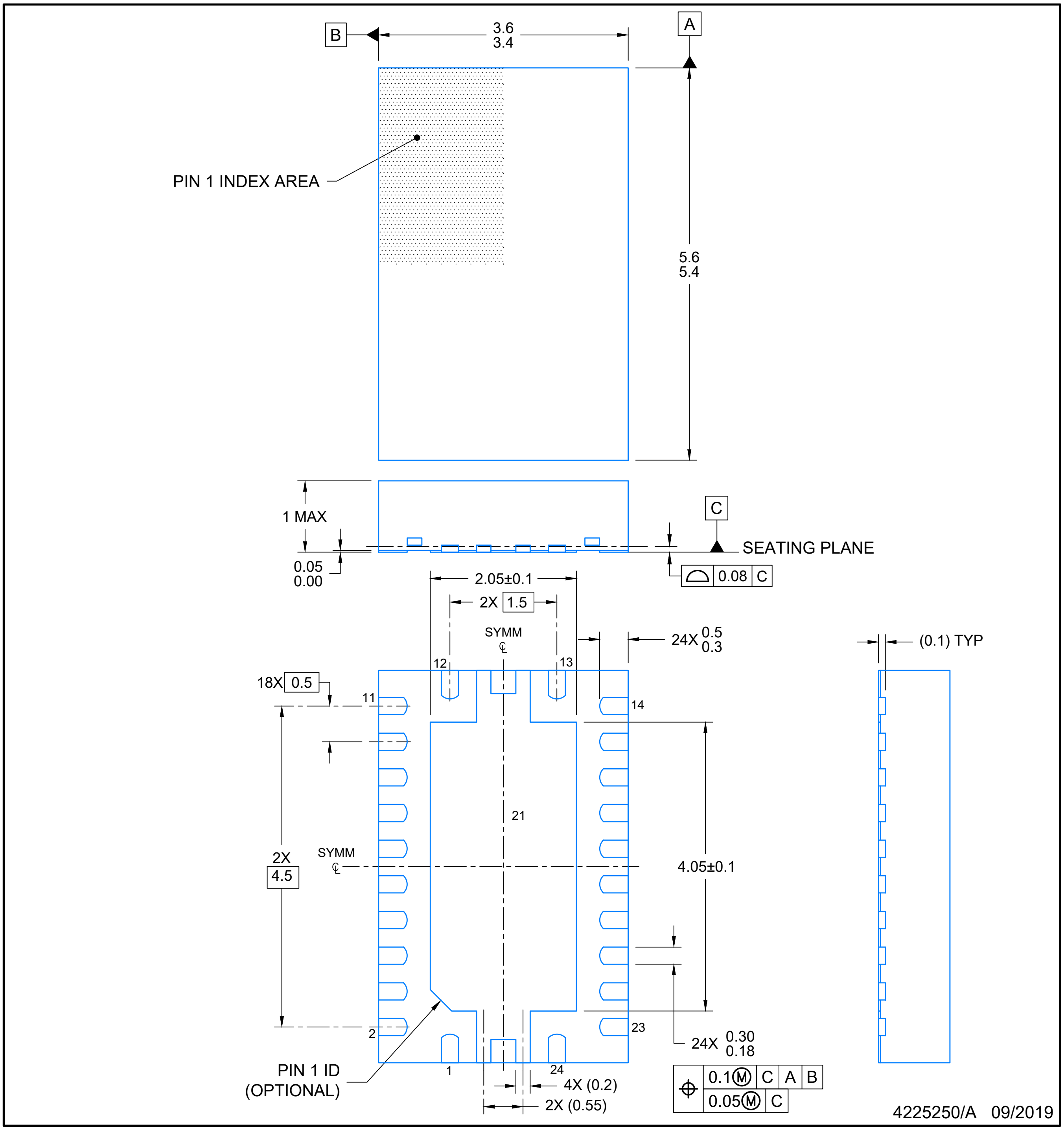
**5.5 x 3.5 mm, 0.5 mm pitch**

PLASTIC QUAD FLATPACK - NO LEAD



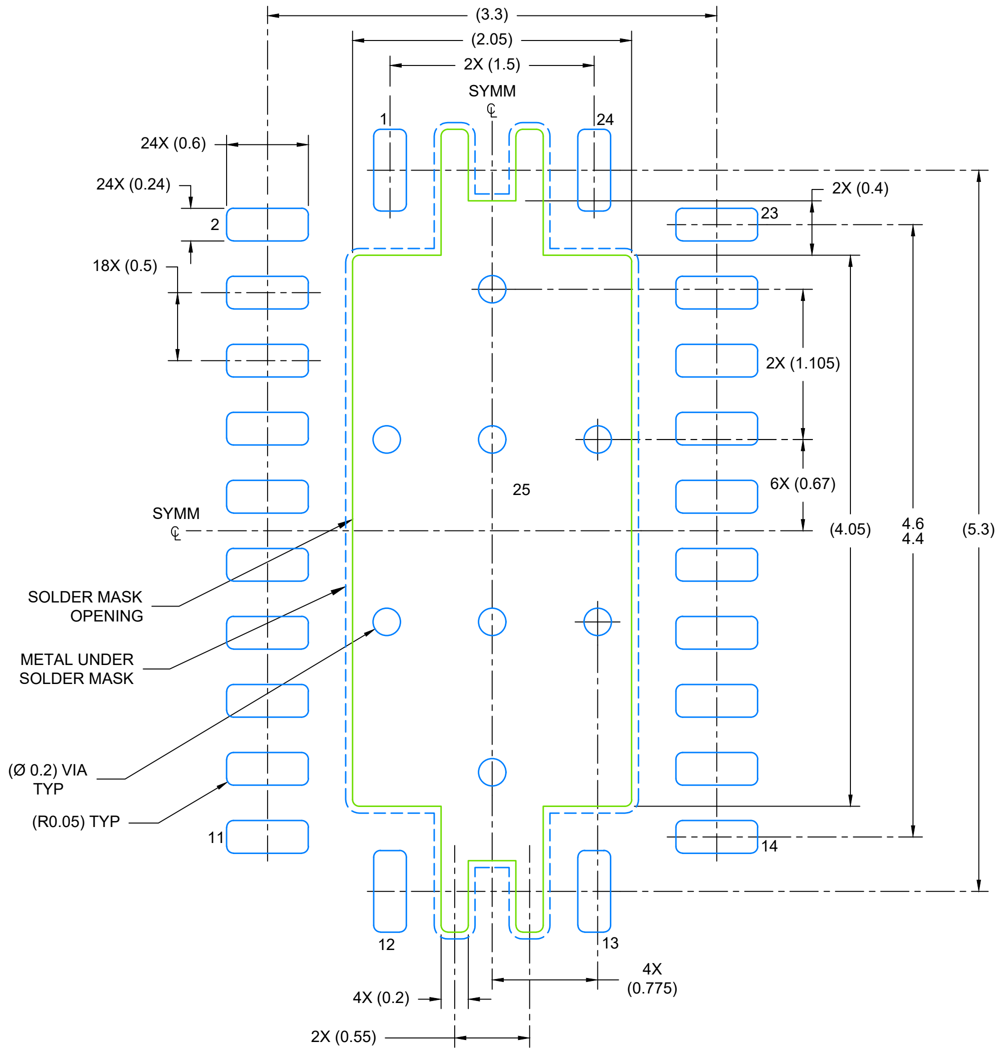

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203539-5/J

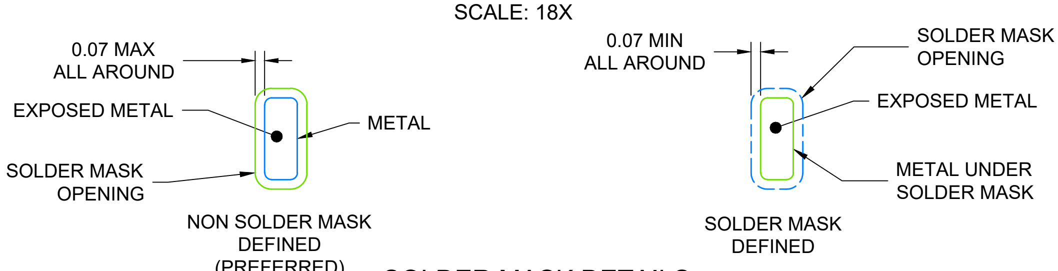



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 18X

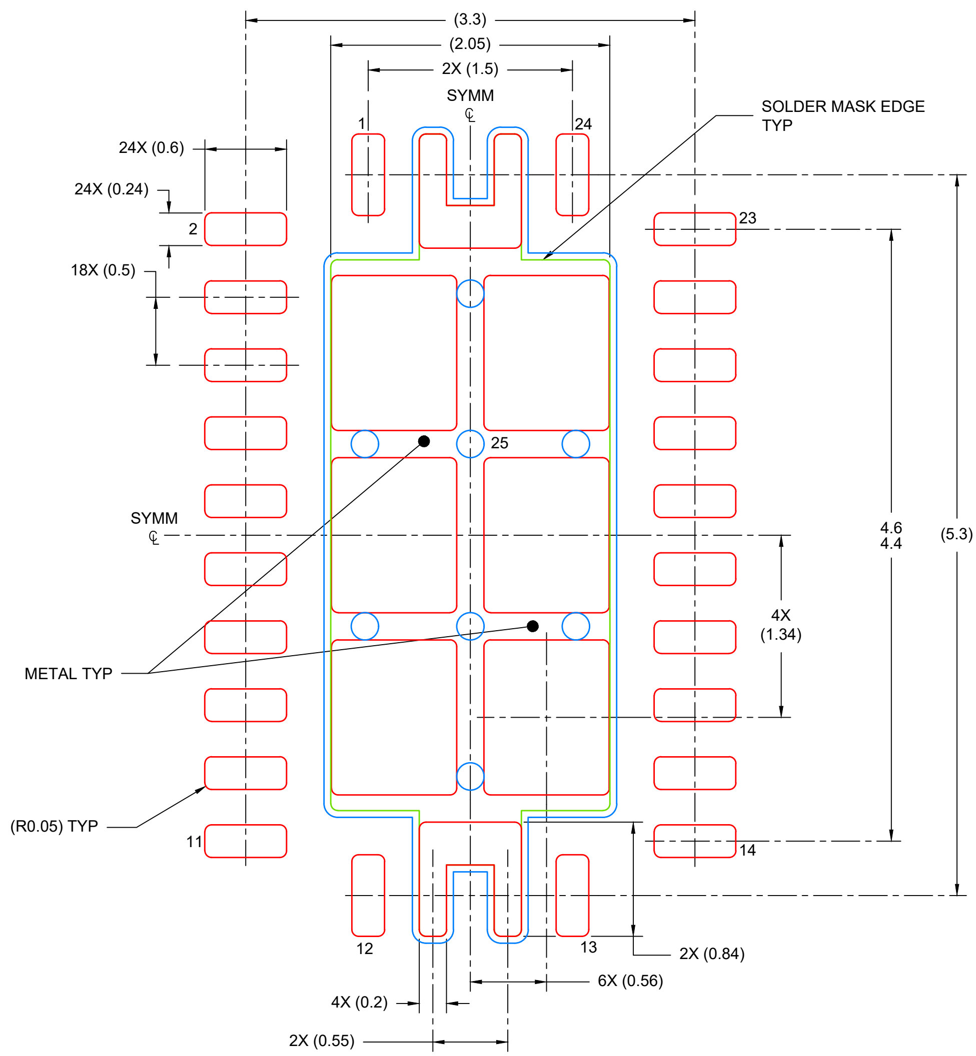



SOLDER MASK DETAILS

4225250/A 09/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



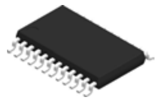

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

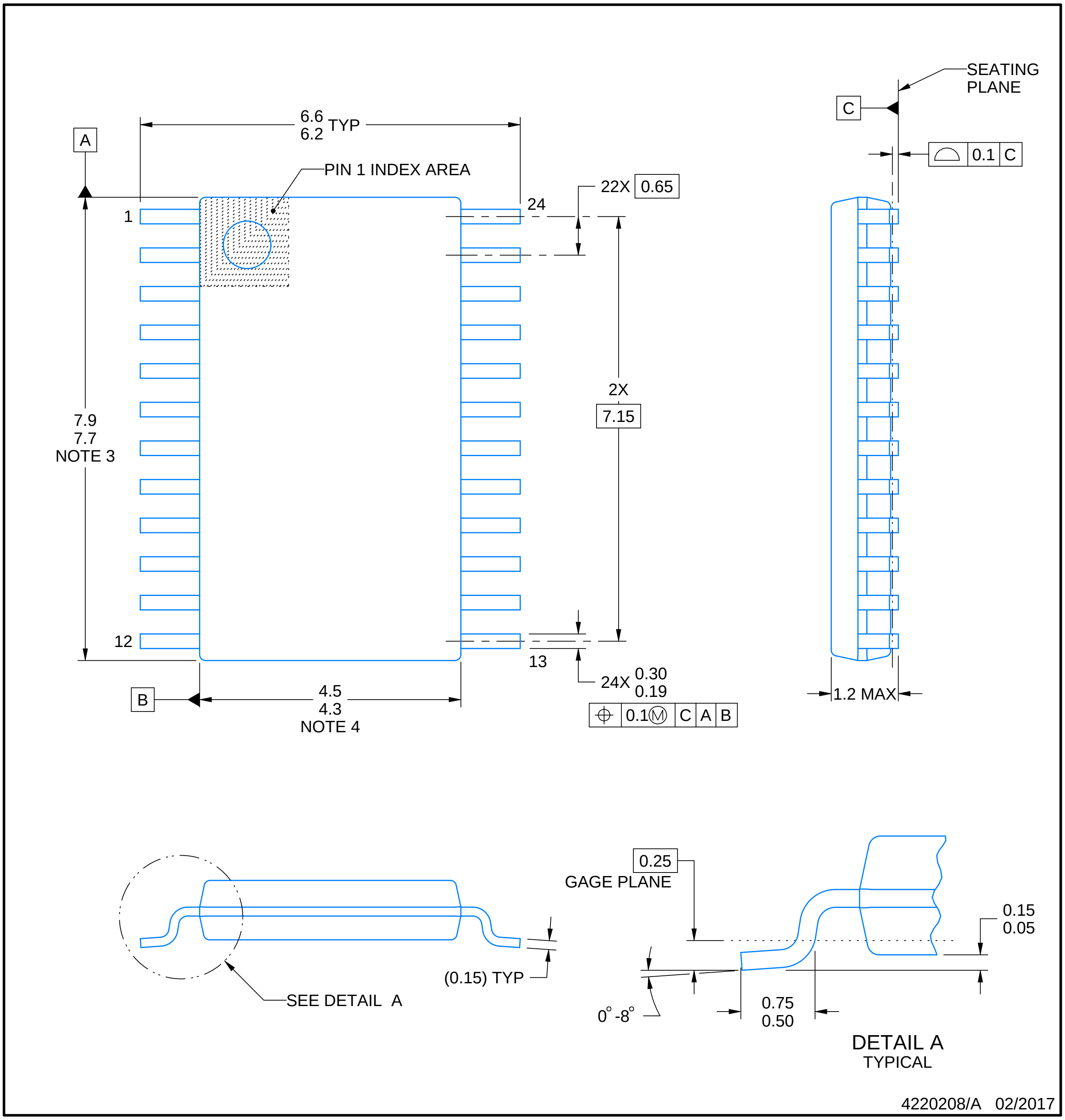
EXPOSED PAD
80% PRINTED COVERAGE BY AREA
SCALE: 18X

4225250/A 09/2019

NOTES: (continued)

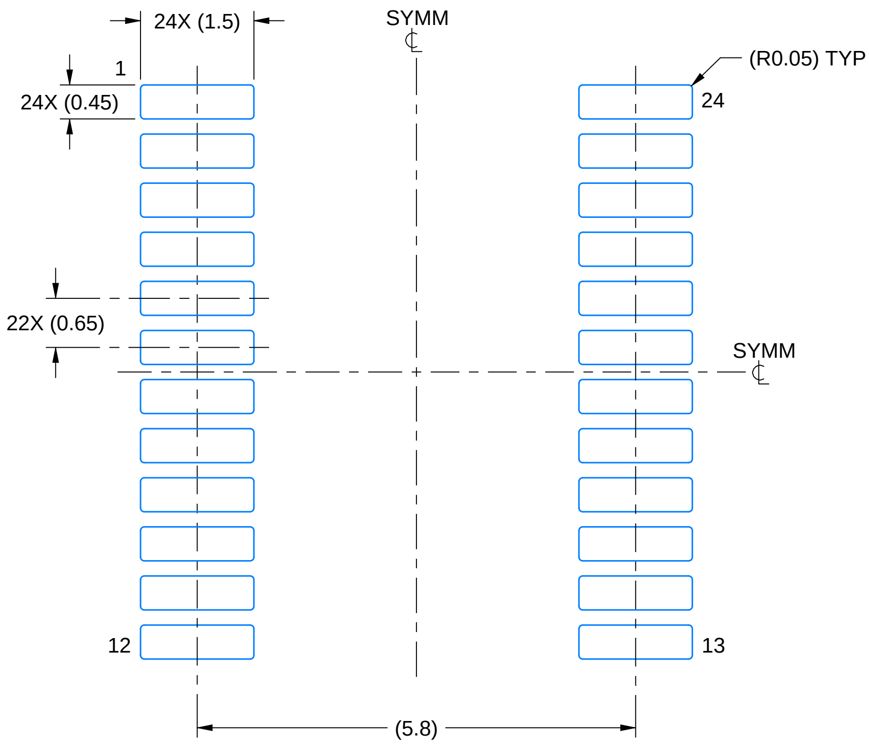
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



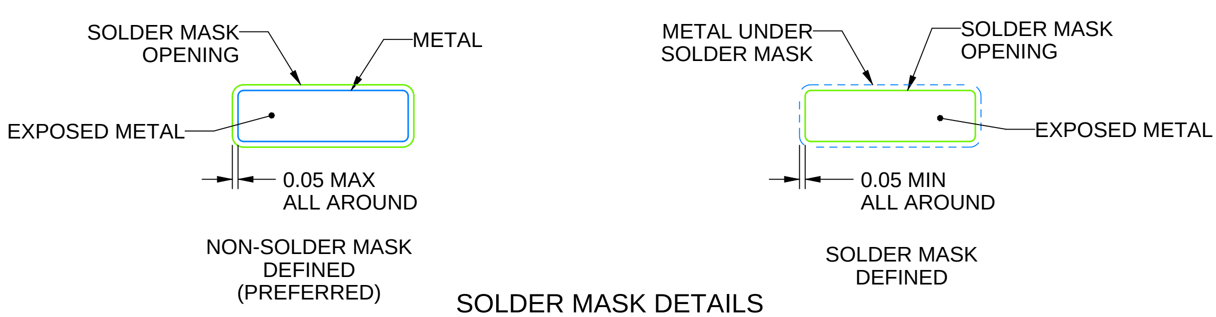



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

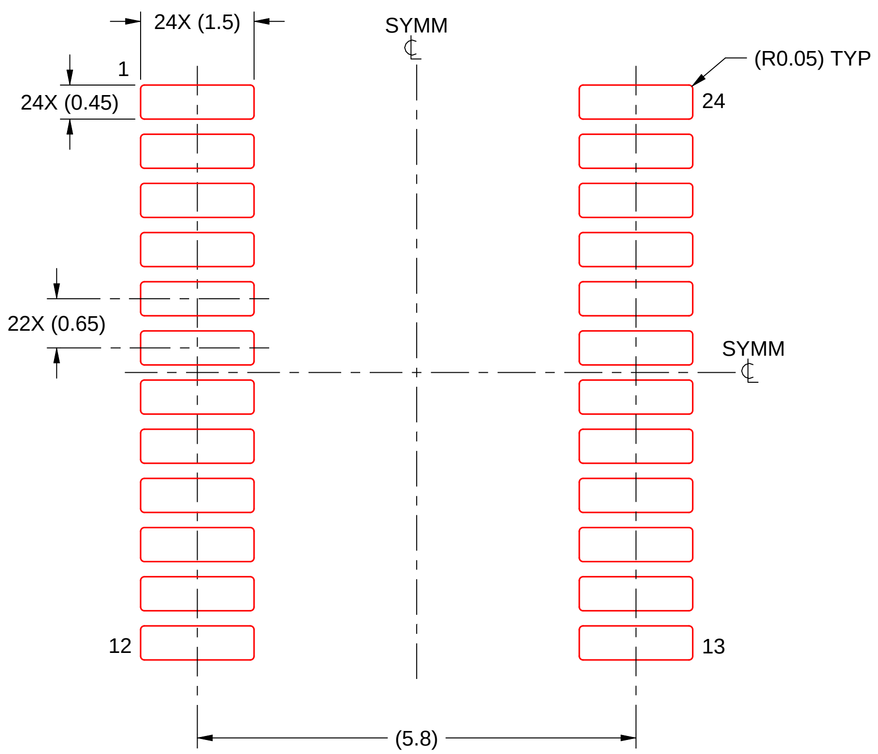



SOLDER MASK DETAILS

4220208/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220208/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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