SN74LVC11A、トリプル 3 入力 AND ゲート

1 特長

- 1.1V～3.6V の動作範囲
- 5.5V 耐圧入力ピン
- 標準ピン配置をサポート
- JESD 17 準拠で
  250mA 超のラッチアップ性能
- JESD 22 を上回る ESD 保護
  - 2000V、人体モデル (A114-A)
  - 1000V、デバイス帯電モデル (C101)

2 アプリケーション

- パワー・グッド信号の結合
- デジタル信号のイネーブル

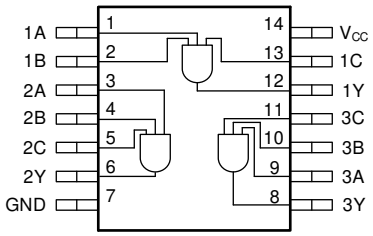
3 概要

このデバイスには、3 つの独立した 3 入力 AND ゲートが内蔵されています。各ゲートはブール関数 Y = A × B × C を正論理で実行します。

パッケージ情報

部品番号	パッケージ (1)	パッケージ サイズ(2)	本体サイズ (3)
SN74LVC11A	D (SOIC、14)	8.65mm × 6mm	8.65mm × 3.9mm
	BQA (WQFN、14)	3mm × 2.5mm	3mm × 2.5mm
	PW (TSSOP、14)	5mm × 6.4mm	5mm × 4.4mm

(1) 詳細については、セクション 11 を参照してください。
(2) パッケージ サイズ (長さ × 幅) は公称値であり、該当する場合はピンも含まれます。
(3) 本体サイズ (長さ×幅) は公称値であり、ピンは含まれません。



機能的なピン配置

このリソースの元の言語は英語です。翻訳は概要を便宜的に提供するもので、自動化ツール (機械翻訳) を使用していることがあり、TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、ti.com で必ず最新の英語版をご参照くださいますようお願いいたします。

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4 Pin Configuration and Functions

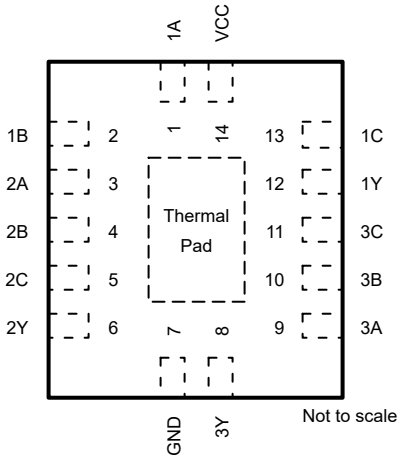

図 4-1. SN74LVC11A BQA Package, 14-Pin WQFN (Top View)

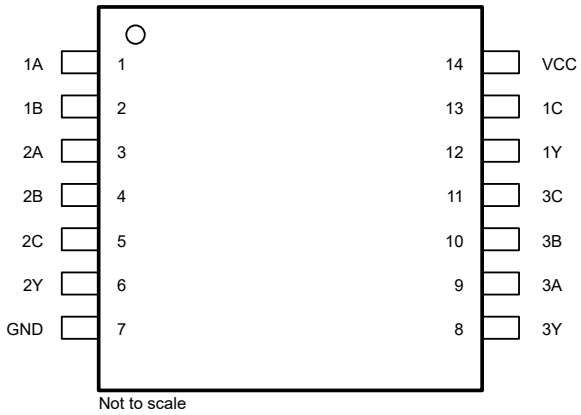

図 4-2. SN74LVC11A D or PW (Preview) Packages, 14-Pin SOIC or TSSOP (Top View)

表 4-1. Pin Functions

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
1A	1	入力	チャネル 1、入力 A
1B	2	入力	チャネル 1、入力 B
2A	3	入力	チャネル 2、入力 A
2B	4	入力	チャネル 2、入力 B
2C	5	入力	チャネル 2、入力 C
2Y	6	出力	チャネル 2、出力 Y
GND	7	—	グランド
3Y	8	出力	チャネル 3、出力 Y
3A	9	入力	チャネル 3、入力 A
3B	10	入力	チャネル 3、入力 B
3C	11	入力	チャネル 3、入力 C
1Y	12	出力	チャネル 1、出力 Y
1C	13	入力	チャネル 1、入力 C
V_{CC}	14	—	正の電源
Thermal Pad[(2)]		—	The thermal pad can be connected to GND or left floating. Do not connect to any other signal or supply.

(1) I = input, O = output, I/O = input or output, G = ground, P = power.
(2) BQA パッケージのみ。

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)[1]

			MIN	MAX	UNIT
V_{CC}	Supply voltage range		-0.5	6.5	V
V_I	Input voltage range[2]		-0.5	6.5	V
V_O	Output voltage range[2]		-0.5	V_{CC} + 0.5	V
I_{IK}	Input clamp current	V_I < 0 V		-50	mA
I_{OK}	Output clamp current	V_O < 0 V		-50	mA
I_O	Continuous output current			±50	mA
I_O	Continuous output current through V_{CC} or GND			±100	mA
T_J	Junction temperature		-65	150	°C
T_{stg}	Storage temperature		-65	150	°C

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If briefly operating outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings*, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

5.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged-device model (CDM), per ANSI/ESDA/JEDEC JS-002[2]	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
V_{CC}	Supply voltage		1.1	3.6	V
V_I	Input voltage			5.5	V
V_O	Output voltage	(High or low state)		V_{CC}	V
I_{OH}	High-level output current	V_{CC} = 1.8 V		-4	mA
		V_{CC} = 2.3 V		-8	
		V_{CC} = 2.7 V		-12	
		V_{CC} = 3 V		-24	
I_{OL}	Low-level output current	V_{CC} = 1.8 V		4	mA
		V_{CC} = 2.3 V		8	
		V_{CC} = 2.7 V		12	
		V_{CC} = 3 V		24	
Δt/Δv	Input transition rise or fall rate			10	ns/V
T_A	Operating free-air temperature		-40	125	°C
V_{IH}	High-level input voltage	V_{CC} = 1.1 V	0.75		V
V_{IH}	High-level input voltage	V_{CC} = 1.2 V	0.78		V
V_{IH}	High-level input voltage	V_{CC} = 1.5 V	0.975		V
V_{IH}	High-level input voltage	V_{CC} = 1.65 V	1.075		V
V_{IH}	High-level input voltage	V_{CC} = 1.95 V	1.2675		V

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over operating free-air temperature range (unless otherwise noted)

Specifications	Description	Condition	MIN	MAX	UNIT
V_{IH}	High-level input voltage	V_{CC} = 2.3 V	1.7		V
V_{IH}	High-level input voltage	V_{CC} = 2.7 V	1.7		V
V_{IH}	High-level input voltage	V_{CC} = 3.6 V	2		V
V_{IL}	Low-Level input voltage	V_{CC} = 1.1 V		0.40	V
V_{IL}	Low-Level input voltage	V_{CC} = 1.2 V		0.42	V
V_{IL}	Low-Level input voltage	V_{CC} = 1.5 V		0.525	V
V_{IL}	Low-Level input voltage	V_{CC} = 1.65 V		0.5775	V
V_{IL}	Low-Level input voltage	V_{CC} = 1.95 V		0.6825	V
V_{IL}	Low-Level input voltage	V_{CC} = 2.3 V		0.7	V
V_{IL}	Low-Level input voltage	V_{CC} = 2.7 V		0.7	V
V_{IL}	Low-Level input voltage	V_{CC} = 3.6 V		0.8	V

5.4 Thermal Information

THERMAL METRIC[1]		Package Options			UNIT
		PW (TSSOP)	D (SOIC)	BQA (WQFN)	
		14 PINS	14 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	150.8	127.8	102.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	78.3	81.9	96.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	93.8	84.4	70.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	24.7	39.6	16.6	°C/W
Y_{JB}	Junction-to-board characterization parameter	93.2	83.9	70.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	-	-	50.1	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

5.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	-40°C to 125°C			UNIT
			MIN	TYP	MAX	
V_{OH}	I_{OH}= –100 µA	1.1 V to 3.6 V	V_{CC} - 0.2			V
V_{OH}	I_{OH}= –4 mA	1.65 V	1.2			V
V_{OH}	I_{OH}= –8 mA	2.3 V	1.75			V
V_{OH}	I_{OH}= –12 mA	2.7 V	2.2			V
V_{OH}		3 V	2.4			V
V_{OH}	I_{OH}= –24 mA	3 V	2.2			V
V_{OL}	I_{OH}= 100 µA	1.1 V to 3.6 V			0.15	V
V_{OL}	I_{OH}= 4 mA	1.65 V			0.45	V
V_{OL}	I_{OH}= 8 mA	2.3 V			0.7	V
V_{OL}	I_{OH}= 12 mA	2.7 V			0.4	V
V_{OL}	I_{OH}= 24 mA	3 V			0.55	V
I_I	V_I = V_{CC} or GND	3.6 V			±5	µA
I_{off}	V_I or V_O = V_{CC}	0 V			±10	µA
I_{CC}	V_I = V_{CC} or GND, I_O = 0	3.6 V			40	µA
ΔI_{CC}	One input at V_{CC} - 0.6 V, other inputs at V_{CC} or GND	2.7 V to 3.6 V			500	µA

over operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V_{CC}	-40°C to 125°C			UNIT
			MIN	TYP	MAX	
C_I	$V_I = V_{CC}$ or GND	3.3 V		4.9		pF
C_O	$V_O = V_{CC}$ or GND	3.3 V		6.3		pF
C_{PD}	f = 10 MHz	1.8 V		31		pF
C_{PD}	f = 10 MHz	2.5 V		31		pF
C_{PD}	f = 10 MHz	3.3 V		32		pF

5.6 Switching Characteristics

over operating free-air temperature range; typical values measured at T_A = 25°C (unless otherwise noted). See *Parameter Measurement Information*

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	V_{CC}	-40°C to 125°C			UNIT
					MIN	TYP	MAX	
t_{pd}	A, B or C	Y	C_L = 15 pF	1.2 V ± 0.1 V		12	23	ns
			C_L = 15 pF	1.5 V ± 0.12 V		9	12	
t_{pd}	A, B or C	Y	C_L = 30 pF	1.8 V ± 0.15 V			10.2	ns
			C_L = 30 pF	2.5 V ± 0.2 V			6.9	
			C_L = 50 pF	2.7 V			4.8	
			C_L = 50 pF	3.3 V ± 0.3 V			4.1	
$t_{sk(o)}$				3.3 V ± 0.3 V			1.5	ns

5.7 Noise Characteristics

VCC = 3.3 V, CL = 50 pF, TA = 25°C

PARAMETER	DESCRIPTION	MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic V_{OL}			0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic V_{OL}	-0.8	-0.3		V
$V_{OH(V)}$	Quiet output, minimum dynamic V_{OH}	2.2	3.3		V
$V_{IH(D)}$	High-level dynamic input voltage	2.0			V
$V_{IL(D)}$	Low-level dynamic input voltage			0.8	V

5.8 Typical Characteristics

T_A = 25°C (unless otherwise noted)

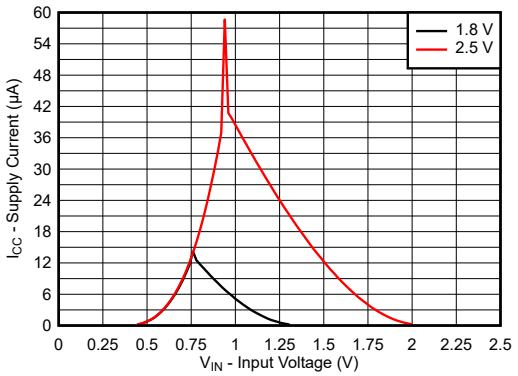

図 5-1. Supply Current Across Input Voltage 1.8V and 2.5V Supply

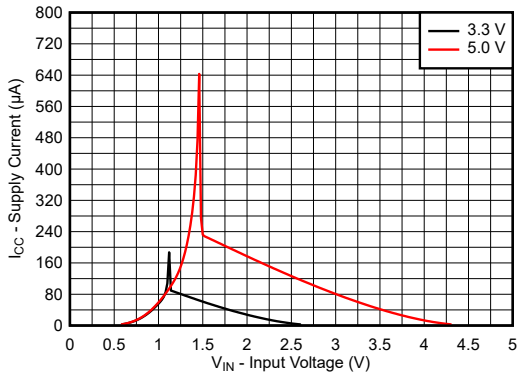

図 5-2. Supply Current Across Input Voltage 3.3V and 5.0V Supply

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5.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

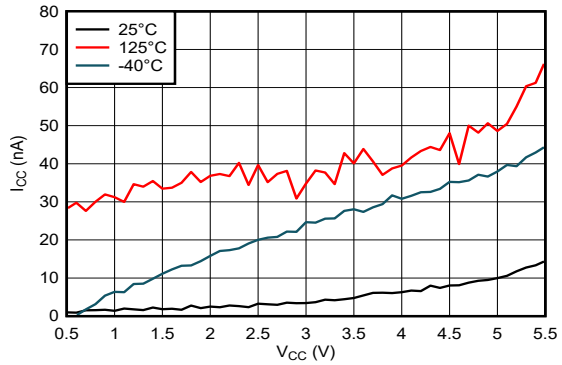

図 5-3. Supply Current Across Supply Voltage

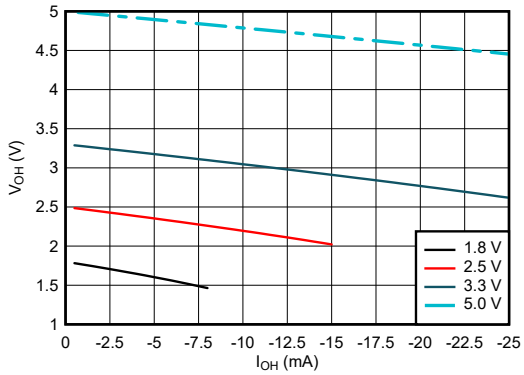

図 5-4. Output Voltage vs Current in HIGH State

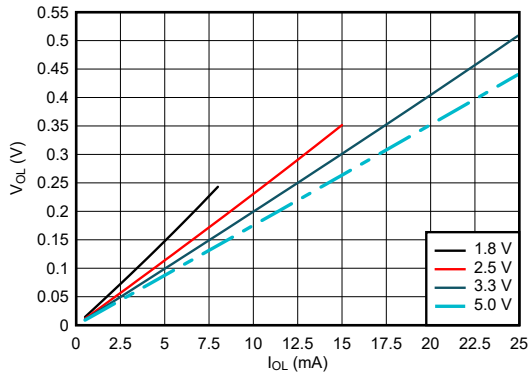

図 5-5. Output Voltage vs Current in LOW State

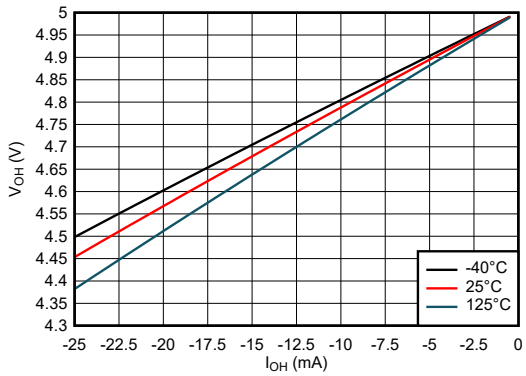

図 5-6. Output Voltage vs Current in HIGH State; 5V Supply

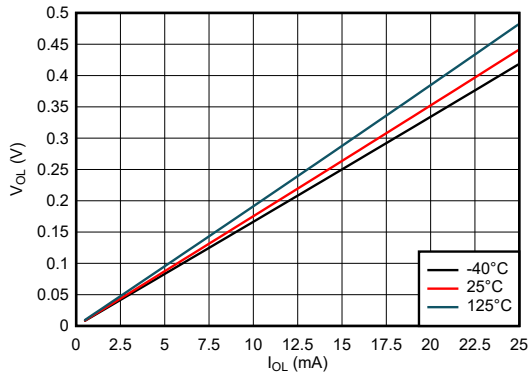

図 5-7. Output Voltage vs Current in LOW State; 5V Supply

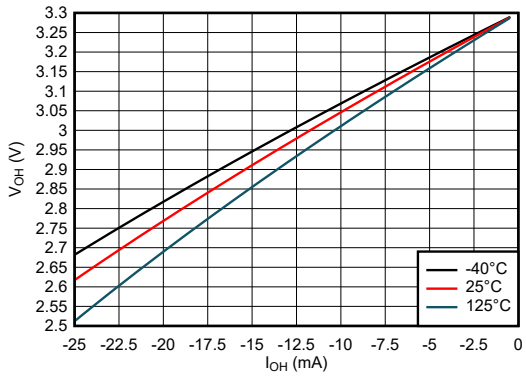

図 5-8. Output Voltage vs Current in HIGH State; 3.3V Supply

5.8 Typical Characteristics (continued)

T_A = 25°C (unless otherwise noted)

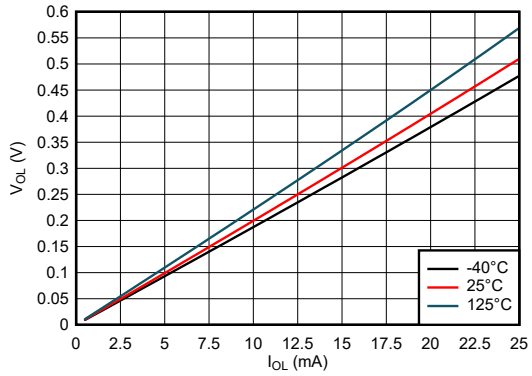

図 5-9. Output Voltage vs Current in LOW State; 3.3V Supply

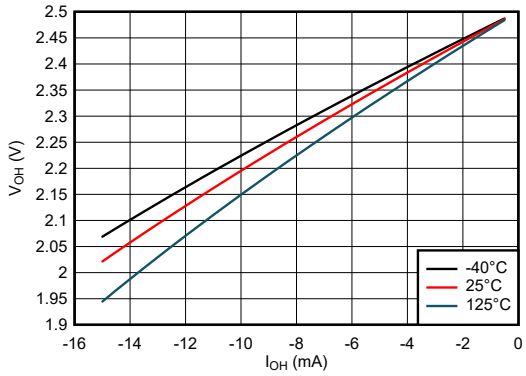

図 5-10. Output Voltage vs Current in HIGH State; 2.5V Supply

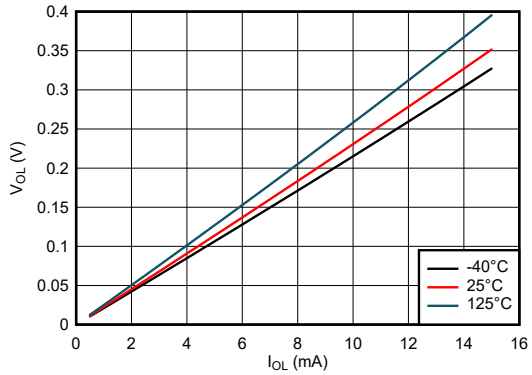

図 5-11. Output Voltage vs Current in LOW State; 2.5V Supply

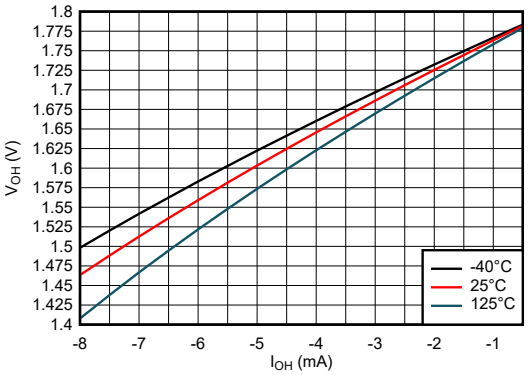

図 5-12. Output Voltage vs Current in HIGH State; 1.8V Supply

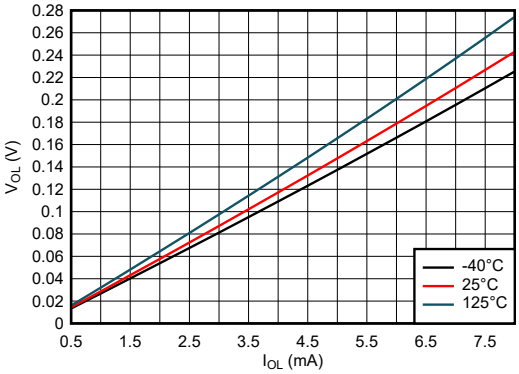

図 5-13. Output Voltage vs Current in LOW State; 1.8V Supply

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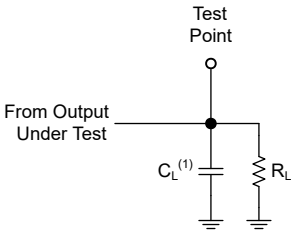
6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily for the examples listed in the following table. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1MHz, Z_O = 50Ω, t_t ≤ 2.5ns.

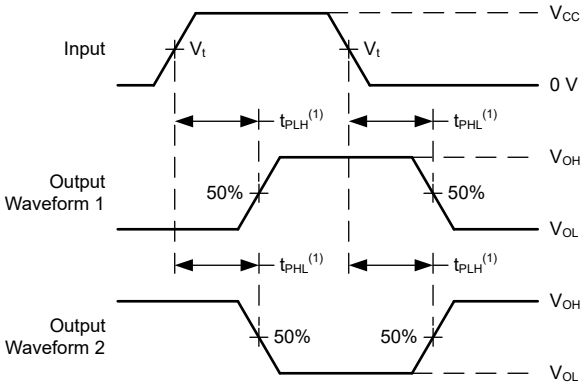
The outputs are measured individually with one input transition per measurement.

V_{CC}	V_t	R_L	C_L	ΔV
1.2V ± 0.1V	$V_{CC}/2$	2kΩ	15pF	0.1V
1.5V ± 0.12V	$V_{CC}/2$	2kΩ	15pF	0.1V
1.8V ± 0.15V	$V_{CC}/2$	1kΩ	30pF	0.15V
2.5V ± 0.2V	$V_{CC}/2$	500Ω	30pF	0.15V
2.7V	1.5V	500Ω	50pF	0.3V
3.3V ± 0.3V	1.5V	500Ω	50pF	0.3V



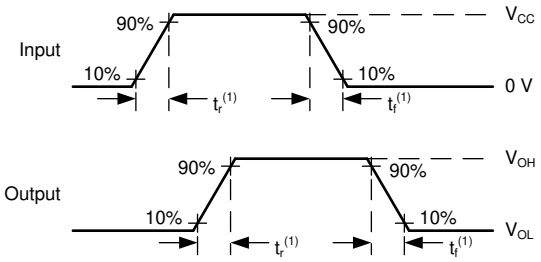
(1) C_L includes probe and test-fixture capacitance.

図 6-1. Load Circuit for Push-Pull Outputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

図 6-2. Voltage Waveforms Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

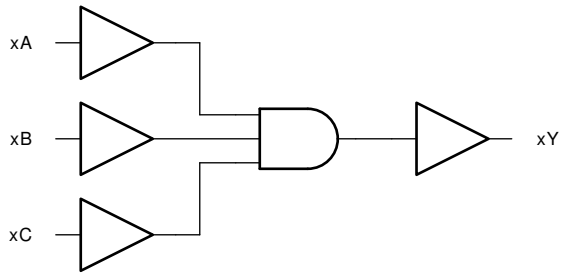
図 6-3. Voltage Waveforms, Input and Output Transition Times

7 Detailed Description

7.1 Overview

This device contains three independent 3-input AND gates. Each gate performs the Boolean function Y = A × B × C in positive logic.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Standard CMOS Inputs

Standard CMOS inputs are high impedance and are typically modeled as a resistor from the input to ground in parallel with the input capacitance given in the *Electrical Characteristics - 74*. The worst case resistance is calculated with the maximum input voltage, given in the *Absolute Maximum Ratings*, and the maximum input leakage current, given in the *Electrical Characteristics - 74*, using ohm's law (R = V ÷ I).

Signals applied to the inputs need to have fast edge rates, as defined by the input transition time in the *Recommended Operating Conditions* to avoid excessive current consumption and oscillations. If a slow or noisy input signal is required, a device with a Schmitt-trigger input should be used to condition the input signal prior to the standard CMOS input.

7.3.2 Balanced CMOS Push-Pull Outputs

A balanced output allows the device to sink and source similar currents. The drive capability of this device may create fast edges into light loads, so routing and load conditions should be considered to prevent ringing. Additionally, the outputs of this device are capable of driving larger currents than the device can sustain without being damaged. It is important for the output power of the device to be limited to avoid damage due to over-current. The electrical and thermal limits defined in the *Absolute Maximum Ratings* must be followed at all times.

The SN74LVC11A can drive a load with a total capacitance less than or equal to the maximum load listed in the *Switching Characteristics -74* connected to a high-impedance CMOS input while still meeting all of the data sheet specifications. Larger capacitive loads can be applied, however it is not recommended to exceed the provided load value. If larger capacitive loads are required, it is recommended to add a series resistor between the output and the capacitor to limit output current to the values given in the *Absolute Maximum Ratings*.

7.3.3 Clamp Diode Structure

図 7-1 shows the inputs and outputs to this device have negative clamping diodes only.

> 注意
> Voltages beyond the values specified in the *Absolute Maximum Ratings* table can cause damage to the device. The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.

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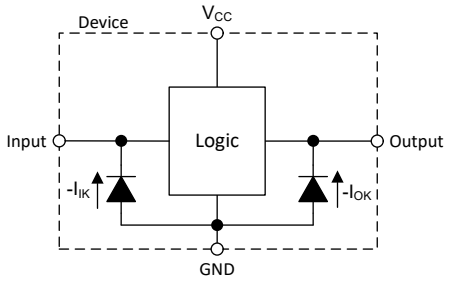

図 7-1. Electrical Placement of Clamping Diodes for Each Input and Output

7.4 Device Functional Modes

表 7-1. Function Table(1)

INPUTS			OUTPUT
A	B	C	Y
H	H	H	H
L	X	X	L
X	L	X	L
X	X	L	L

(1) H = high voltage level, L = low voltage level, X = do not care

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

In this application, this device is used to directly control the RESET pin of a motor controller. The controller requires three input signals to all be HIGH before being enabled, and should be disabled in the event that any one signal goes LOW. The 3-input AND gate function combines the three individual reset signals into a single active-low reset signal.

8.2 Typical Application

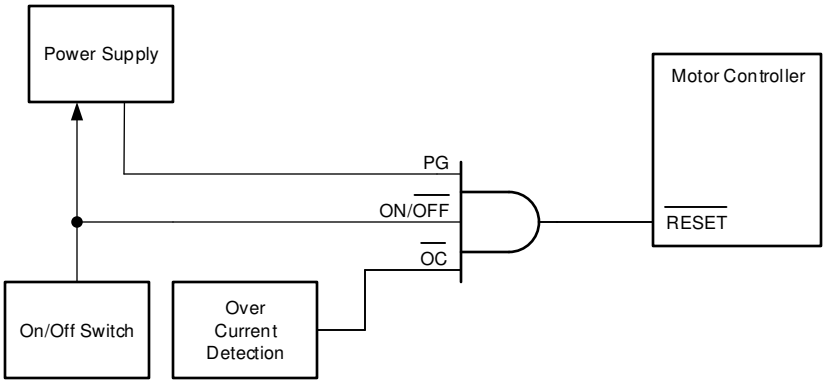

図 8-1. Typical Application Schematic

8.2.1 Design Requirements

8.2.1.1 Power Considerations

Ensure the desired supply voltage is within the range specified in the *Recommended Operating Conditions*. The supply voltage sets the electrical characteristics of the device as described in the *Electrical Characteristics* section.

The positive voltage supply must be capable of sourcing current equal to the total current to be sourced by all outputs of the SN74LVC11A plus the maximum static supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only source as much current that is provided by the positive supply source. Be sure to not exceed the maximum total current through V_{CC} listed in the *Absolute Maximum Ratings*.

The ground must be capable of sinking current equal to the total current to be sunk by all outputs of the SN74LVC11A plus the maximum supply current, I_{CC}, listed in the *Electrical Characteristics*, and any transient current required for switching. The logic device can only sink as much current that can be sunk into its ground connection. Be sure to not exceed the maximum total current through GND listed in the *Absolute Maximum Ratings*.

The SN74LVC11A can drive a load with a total capacitance less than or equal to 50pF while still meeting all of the data sheet specifications. Larger capacitive loads can be applied; however, it is not recommended to exceed 50pF.

The SN74LVC11A can drive a load with total resistance described by $R_L \geq V_O / I_O$, with the output voltage and current defined in the *Electrical Characteristics* table with V_{OH} and V_{OL}. When outputting in the HIGH state, the

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output voltage in the equation is defined as the difference between the measured output voltage and the supply voltage at the V_{CC} pin.

Total power consumption can be calculated using the information provided in the *CMOS Power Consumption and Cpd Calculation* application note.

Thermal increase can be calculated using the information provided in the *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note.

> 注意
> The maximum junction temperature, $T_{J(max)}$ listed in the *Absolute Maximum Ratings*, is an additional limitation to prevent damage to the device. Do not violate any values listed in the *Absolute Maximum Ratings*. These limits are provided to prevent damage to the device.

8.2.1.2 Input Considerations

Input signals must cross $V_{IL(max)}$ to be considered a logic LOW, and $V_{IH(min)}$ to be considered a logic HIGH. Do not exceed the maximum input voltage range found in the *Absolute Maximum Ratings*.

Unused inputs must be terminated to either V_{CC} or ground. The unused inputs can be directly terminated if the input is completely unused, or they can be connected with a pull-up or pull-down resistor if the input will be used sometimes, but not always. A pull-up resistor is used for a default state of HIGH, and a pull-down resistor is used for a default state of LOW. The drive current of the controller, leakage current into the SN74LVC11A (as specified in the *Electrical Characteristics*), and the desired input transition rate limits the resistor size. A 10kΩ resistor value is often used due to these factors.

The SN74LVC11A has CMOS inputs and thus requires fast input transitions to operate correctly, as defined in the *Recommended Operating Conditions* table. Slow input transitions can cause oscillations, additional power consumption, and reduction in device reliability.

Refer to the *Feature Description* section for additional information regarding the inputs for this device.

8.2.1.3 Output Considerations

The positive supply voltage is used to produce the output HIGH voltage. Drawing current from the output will decrease the output voltage as specified by the V_{OH} specification in the *Electrical Characteristics*. The ground voltage is used to produce the output LOW voltage. Sinking current into the output will increase the output voltage as specified by the V_{OL} specification in the *Electrical Characteristics*.

Push-pull outputs that could be in opposite states, even for a very short time period, should never be connected directly together. This can cause excessive current and damage to the device.

Two channels within the same device with the same input signals can be connected in parallel for additional output drive strength.

Unused outputs can be left floating. Do not connect outputs directly to V_{CC} or ground.

Refer to the *Feature Description* section for additional information regarding the outputs for this device.

8.2.2 Detailed Design Procedure

1. Add a decoupling capacitor from V_{CC} to GND. The capacitor needs to be placed physically close to the device and electrically close to both the V_{CC} and GND pins. An example layout is shown in *Layout Examples*.
2. Ensure the capacitive load at the output is ≤ 70pF. This is not a hard limit; by design, however, it will optimize performance. This can be accomplished by providing short, appropriately sized traces from the SN74LVC11A to the receiving device.
3. Ensure the resistive load at the output is larger than (V_{CC} / I_O(max)) Ω, so that the maximum output current from the *Absolute Maximum Ratings* is not violated. Most CMOS inputs have a resistive load measured in mega ohms; much larger than the minimum calculated previously.

4. Thermal issues are rarely a concern for logic gates, however the power consumption and thermal increase can be calculated using the steps provided in the application report, *CMOS Power Consumption and Cpd Calculation*

8.2.3 Application Curves

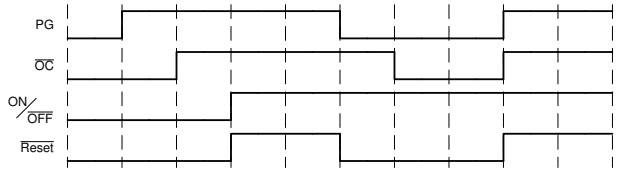

図 8-2. Typical Application Timing Diagram

8.3 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a bypass capacitor to prevent power disturbance. A 0.1µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass capacitors to reject different frequencies of noise. The 0.1µF and 1µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results, as shown in *Layout Example*.

8.4 Layout

8.4.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

8.4.2 Layout Example

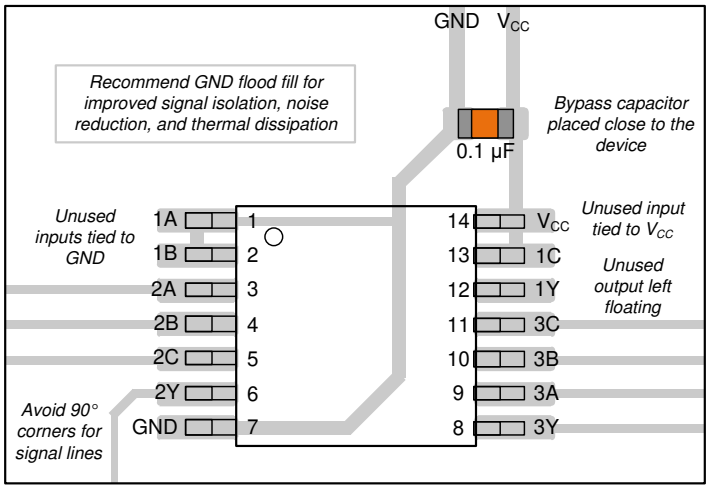

図 8-3. Example Layout for the SN74LVC11A

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9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *CMOS Power Consumption and Cpd Calculation* application note
- Texas Instruments, *Designing With Logic* application note
- Texas Instruments, *Thermal Characteristics of Standard Linear and Logic (SLL) Packages and Devices* application note
- Texas Instruments, *Implications of Slow or Floating CMOS Inputs* application note

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10 Revision History

Changes from Revision * (February 2024) to Revision A (May 2024)	Page
• 「パッケージ情報」表、「ピン構成および機能」セクション、「熱に関する情報」表に D パッケージを追加	1
• 「特長」セクションの動作範囲を 1.2V から 1.1V に更新し、「概要」セクションから注を削除	1

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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