TEXAS INSTRUMENTS
SN74LVC1G3157-Q1
JAJSH66H – JUNE 2003 – REVISED DECEMBER 2021

SN74LVC1G3157-Q1 車載用単極双投アナログ・スイッチ

1 特長

- 機能安全対応
  - 機能安全システムの設計に役立つ資料を利用可能
- 車載アプリケーション用に AEC-Q100 認定済み:
  - 温度グレード 1:-40℃～+125℃、T_A
- MIL-STD-883、手法 3015 に従い 2000V を超える ESD 保護、マシン・モデルで 200V 超 (C = 200pF、R = 0)
- 1.65V～5.5V の V_{CC} で動作
- アナログおよびデジタル・アプリケーションに有用
- Break-Before-Make スイッチングを規定
- レール・ツー・レールの信号処理
- 高度な線形性
- 高速、標準値 0.5ns
  (V_{CC} = 3V、C_L = 50pF)
- 低いオン抵抗、標準値≠6Ω
  (V_{CC} = 4.5V)
- JESD 78、Class II 準拠で 100mA 超のラッチアップ性能

2 アプリケーション

- 先進運転支援システム (ADAS)

3 概要

SN74LVC1G3157-Q1 デバイスは単極双投 (SPDT) アナログ・スイッチで、1.65V～5.5V の V_{CC} で動作するよう設計されています。

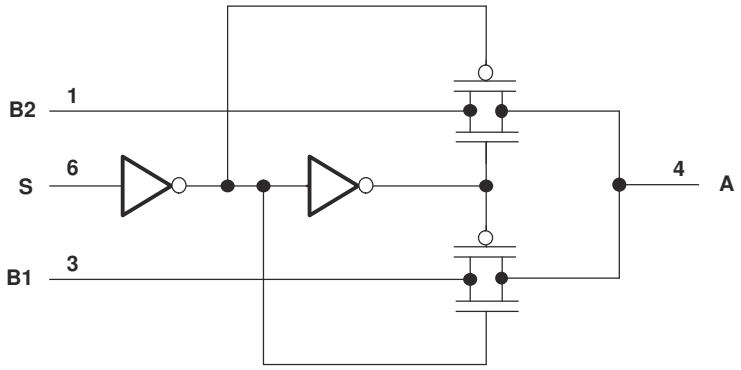
SN74LVC1G3157 デバイスは、アナログとデジタルの両方の信号を扱うことができます。このデバイスは、最高で V_{CC} (ピーク) までの振幅の信号を、どちらの方向にも転送できます。

信号ゲーティング、チョッピング、変調または復調 (モデム)、およびアナログ / デジタルやデジタル / アナログ変換システム用の信号多重化などのアプリケーションに使用できます。

製品情報(1)

部品番号	パッケージ	本体サイズ (公称)
SN74LVC1G3157-Q1	SOT-23 (6)	2.90mm × 1.60mm
	SC70 (6)	2.00mm × 1.25mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



論理図 (正論理)

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision G (April 2019) to Revision H (December 2021)	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• データシートに機能安全の文を追加	1

Changes from Revision F (March 2015) to Revision G (April 2019)	Page
• 車載用の特長を変更	1
• Changed the *Pin Configuration* images	3
• Changed the *ESD Ratings* table	4

Changes from Revision E (April 2008) to Revision F (March 2015)	Page
• 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1

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5 Pin Configuration and Functions

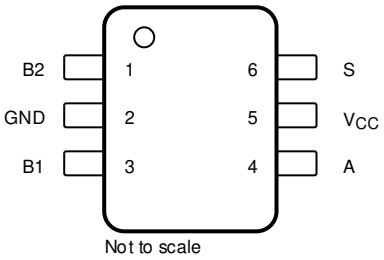

図 5-1. DBV Package 6-Pin SOT-23 Top View

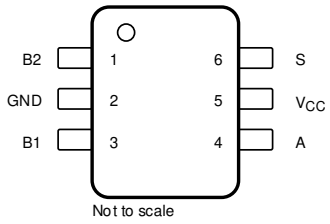

図 5-2. DCK Package 6-Pin SC70 Top View

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
A	4	I/O	Common terminal
B1	3	I/O	First terminal
B2	1	I/O	Second terminal
GND	2	—	Ground
S	6	I	Select
V_{CC}	5	I	Power supply

(1) I = input, O = output, GND = ground.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage(2)		–0.5	6.5	V
V_{IN}	Control input voltage(2) (3)		–0.5	6.5	V
$V_{I/O}$	Switch I/O voltage(2) (3) (4) (5)		–0.5	V_{CC} + 0.5	V
I_{IK}	Control input clamp current	V_{IN} < 0	–50		mA
I_{IOK}	I/O port diode current	$V_{I/O}$ < 0	–50		mA
$I_{I/O}$	ON-state switch current	$V_{I/O}$ = 0 to V_{CC} (6)		±128	mA
	Continuous current through V_{CC} or GND			±100	mA
θ_{JA}	Package thermal impedance(7)	DBV package		165	°C/W
		DCK package		258	
T_{stg}	Storage temperature		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are with respect to ground, unless otherwise specified.
(3) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
(4) This value is limited to 5.5 V maximum.
(5) V_I, V_O, V_A, and V_{Bn} are used to denote specific conditions for $V_{I/O}$.
(6) I_I, I_O, I_A, and I_{Bn} are used to denote specific conditions for $I_{I/O}$.
(7) The package thermal impedance is calculated in accordance with JESD 51-7.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 1C		±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C6	Other pins	±1000	
			Corner pins (B2, B1, S, and A)	±1000	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	NOM	MAX	UNIT
V_{CC}			1.65		5.5	V
$V_{I/O}$			0		V_{CC}	V
V_{IN}			0		5.5	V
V_{IH}	High-level input voltage, control input	V_{CC} = 1.65 V to 1.95 V	V_{CC} × 0.75			V
		V_{CC} = 2.3 V to 5.5 V	V_{CC} × 0.7			
V_{IL}	Low-level input voltage, control input	V_{CC} = 1.65 V to 1.95 V			V_{CC} × 0.25	V
		V_{CC} = 2.3 V to 5.5 V			V_{CC} × 0.3	
Δt/Δv	Input transition rise/fall time	V_{CC} = 1.65 V to 1.95 V			20	ns/V
		V_{CC} = 2.3 V to 2.7 V			20	
		V_{CC} = 3 V to 3.6 V			10	
		V_{CC} = 4.5 V to 5.5 V			10	
T_A			–40		125	°C

(1) All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, SCBA004.

6.4 Thermal Information

THERMAL METRIC(1)		SN74LVC1G3157-Q1		UNIT
		DBV (SOT-23)	DCK (SC70)	
		6 PINS	6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	201.8	233.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	103.7	107.9	
$R_{\theta JB}$	Junction-to-board thermal resistance	51.8	52.7	
ψ_{JT}	Junction-to-top characterization parameter	12	4.9	
ψ_{JB}	Junction-to-board characterization parameter	51.4	52.4	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER			TEST CONDITIONS		V_{CC}	MIN	TYP(1)	MAX	UNIT
r_{on}	ON-state switch resistance(2)	See 図 7-1 and 図 6-1	V_I = 0 V,	I_O = 4 mA	1.65 V		11	20	Ω
			V_I = 1.65 V,	I_O = –4 mA			15	50	
			V_I = 0 V,	I_O = 8 mA	2.3 V		8	12	
			V_I = 2.3 V,	I_O = –8 mA			11	30	
			V_I = 0 V,	I_O = 24 mA	3 V		7	9.5	
			V_I = 3 V,	I_O = –24 mA			9	20	
			V_I = 0 V,	I_O = 30 mA	4.5 V		6	7.5	
			V_I = 2.4 V,	I_O = –30 mA			7	12	
			V_I = 4.5 ,	I_O = –30 mA			7	15	
r_{range}	ON-state switch resistance over signal range(2) (3)	$0 \le V_{Bn} \le V_{CC}$ (see 図 7-1 and 図 6-1)		I_A = –4 mA	1.65 V			140	Ω
				I_A = –8 mA	2.3 V			45	
				I_A = –24 mA	3 V			18	
				I_A = –30 mA	4.5 V			10	
Δr_{on}	Difference in on-state resistance between switches(2) (4) (5)	See 図 7-1	V_{Bn} = 1.15 V,	I_A = –4 mA	1.65 V		0.5		Ω
			V_{Bn} = 1.6 V,	I_A = –8 mA	2.3 V		0.1		
			V_{Bn} = 2.1 V,	I_A = –24 mA	3 V		0.1		
			V_{Bn} = 3.15 V,	I_A = –30 mA	4.5 V		0.1		
$r_{on(flat)}$	ON-state resistance flatness(2) (4) (6)	$0 \le V_{Bn} \le V_{CC}$		I_A = –4 mA	1.65 V		110		Ω
				I_A = –8 mA	2.3 V		26		
				I_A = –24 mA	3 V		9		
				I_A = –30 mA	4.5 V		4		
I_{off} (7)	OFF-state switch leakage current	$0 \le V_I$, $V_O \le V_{CC}$ (see 図 7-2)			1.65 V to 5.5 V			±1	μA
							±0.05	±1(1)	
$I_{S(on)}$	ON-state switch leakage current	$V_I = V_{CC}$ or GND, V_O = Open (see 図 7-3)			5.5 V			±1	μA
								±0.1(1)	
I_{IN}	Control input current	$0 \le V_{IN} \le V_{CC}$			0 V to 5.5 V			±1	μA
							±0.05	±1(1)	
I_{CC}	Supply current	$V_{IN} = V_{CC}$ or GND			5.5 V		1	10	μA
ΔI_{CC}	Supply-current change	$V_{IN} = V_{CC}$ – 0.6 V			5.5 V			500	μA
C_{in}	Control input capacitance	S			5 V		2.7		pF
$C_{io(off)}$	Switch I/O capacitance	Bn			5 V		5.2		pF
$C_{io(on)}$	Switch I/O capacitance	Bn			5 V		17.3		pF
		A					17.3		

(1) T_A = 25°C
(2) Measured by the voltage drop between I/O pins at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages on the two (A or B) ports.
(3) Specified by design
(4) $\Delta r_{on} = r_{on(max)} - r_{on(min)}$ measured at identical V_{CC}, temperature, and voltage levels
(5) This parameter is characterized, but not tested in production.
(6) Flatness is defined as the difference between the maximum and minimum values of ON-state resistance over the specified range of conditions.
(7) I_{off} is the same as $I_{S(off)}$ (OFF-state switch leakage current).

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6.6 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see 図 7-4 and 図 7-10)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V_{CC} = 1.8 V ± 0.15 V		V_{CC} = 2.5 V ± 0.2 V		V_{CC} = 3.3 V ± 0.3 V		V_{CC} = 5 V ± 0.5 V		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{pd} (1)	A or Bn	Bn or A		2		1.2		0.8		0.3	ns
t_{en} (2)	S	Bn	7	24	3.5	14	2.5	7.6	1.7	5.7	ns
t_{dis} (3)			3	13	2	7.5	1.5	5.3	0.8	3.8	
t_{B-M} (4)			0.5		0.5		0.5		0.5		ns

(1) t_{pd} is the slower of t_{PLH} or t_{PHL}. Propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance when driven by an ideal voltage source (zero output impedance).
(2) t_{en} is the slower of t_{PZL} or t_{PZH}.
(3) t_{dis} is the slower of t_{PLZ} or t_{PHZ}.
(4) Specified by design

6.7 Analog Switch Characteristics

T_A = 25°C

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	V_{CC}	TYP	UNIT
Frequency response (switch on)(1)	A or Bn	Bn or A	R_L = 50 Ω, f_{in} = sine wave (see 図 7-5)	1.65 V	300	MHz
				2.3 V	300	
				3 V	300	
				4.5 V	300	
Crosstalk (between switches)(2)	B1 or B2	B2 or B1	R_L = 50 Ω, f_{in} = 10 MHz (sine wave) (see 図 7-6)	1.65 V	–54	dB
				2.3 V	–54	
				3 V	–54	
				4.5 V	–54	
Feedthrough attenuation (switch off)(2)	A or Bn	Bn or A	C_L = 5 pF, R_L = 50 Ω, f_{in} = 10 MHz (sine wave) (see 図 7-7)	1.65 V	–57	dB
				2.3 V	–57	
				3 V	–57	
				4.5 V	–57	
Charge injection(3)	S	A	C_L = 0.1 nF, R_L = 1 MΩ (see 図 7-8)	3.3 V	3	pC
				5 V	7	
Total harmonic distortion	A or Bn	Bn or A	V_I = 0.5 Vp-p, R_L = 600 Ω, f_{in} = 600 Hz to 20 kHz (sine wave) (see 図 7-9)	1.65%	0.1%	V
				2.3%	0.025%	
				3%	0.015%	
				4.5%	0.01%	

(1) Adjust f_{in} voltage to obtain 0 dBm at output. Increase f_{in} frequency until dB meter reads –3 dB.
(2) Adjust f_{in} voltage to obtain 0 dBm at input.
(3) Specified by design

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6.8 Typical Characteristics

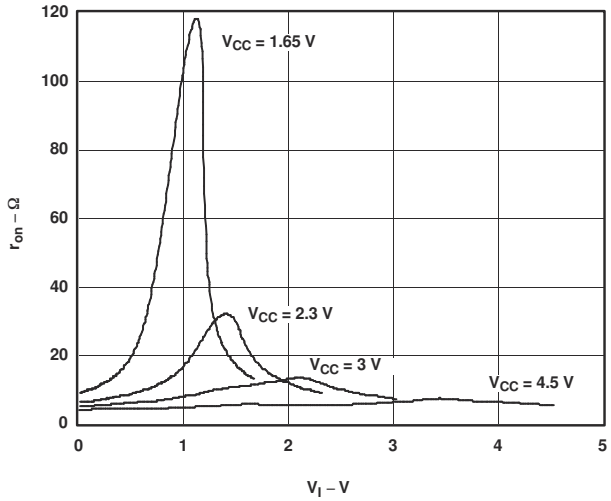

図 6-1. Typical R_{on} as a Function of Input Voltage (V_I) for V_I = 0 To V_{CC}

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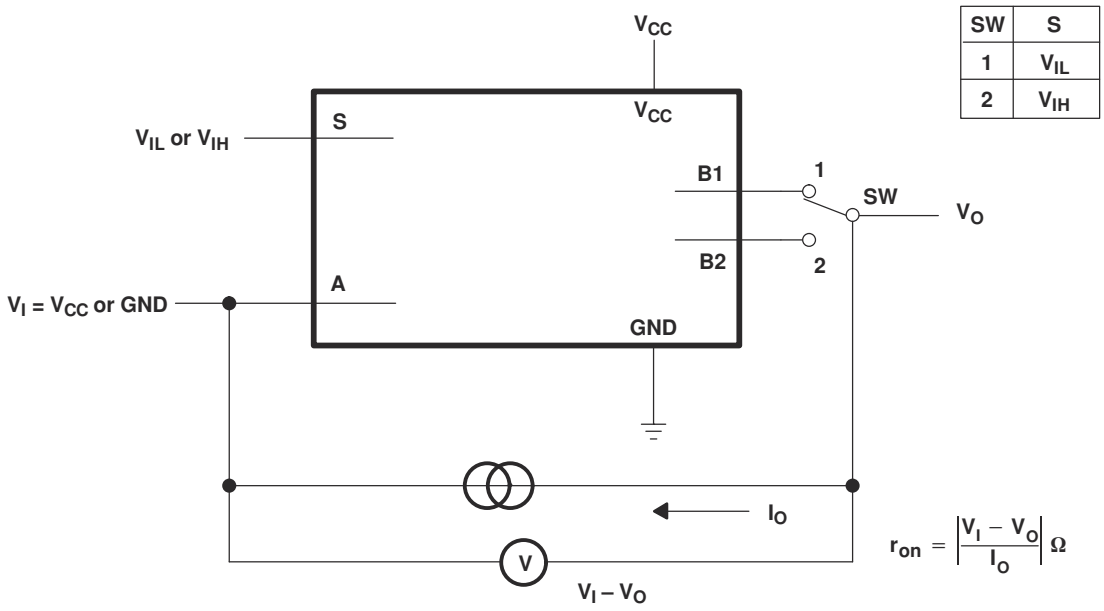
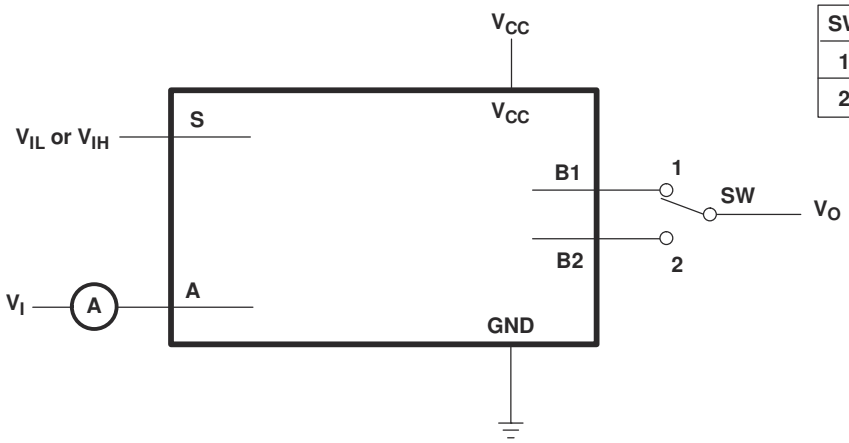
7 Parameter Measurement Information



SW	S
1	V_{IL}
2	V_{IH}

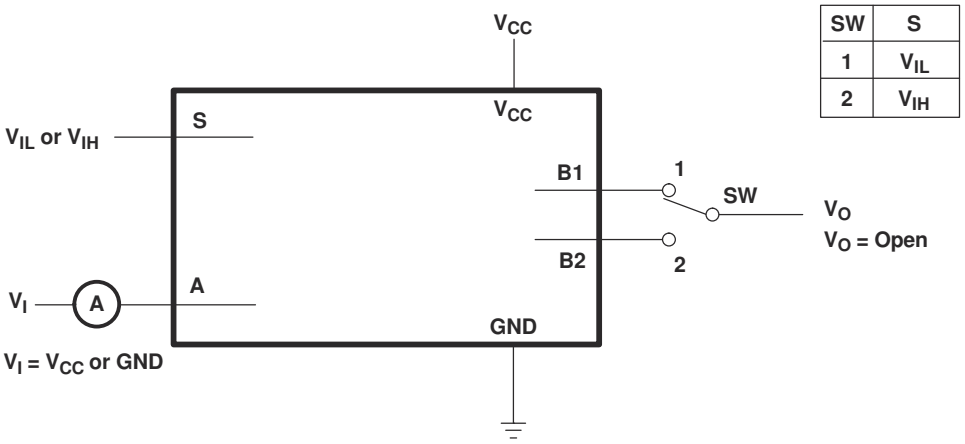
図 7-1. ON-State Resistance Test Circuit



SW	S
1	V_{IL}
2	V_{IH}

Condition 1: V_I = GND, V_O = V_{CC}
Condition 2: V_I = V_{CC}, V_O = GND

図 7-2. OFF-State Switch Leakage-Current Test Circuit



SW	S
1	V_{IL}
2	V_{IH}

図 7-3. ON-State Switch Leakage-Current Test Circuit

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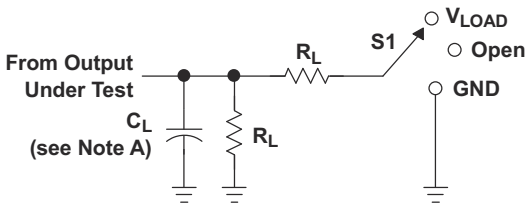
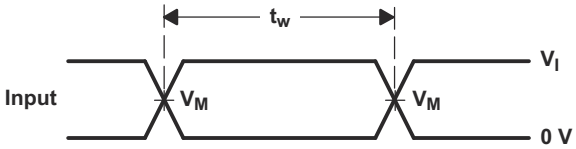


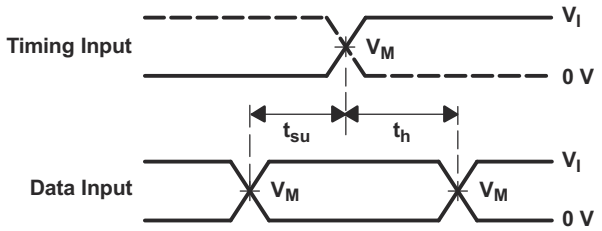
LOAD CIRCUIT

TEST	S1
t_{PLH}/t_{PHL}	Open
t_{PLZ}/t_{PZL}	V_{LOAD}
t_{PHZ}/t_{PZH}	GND

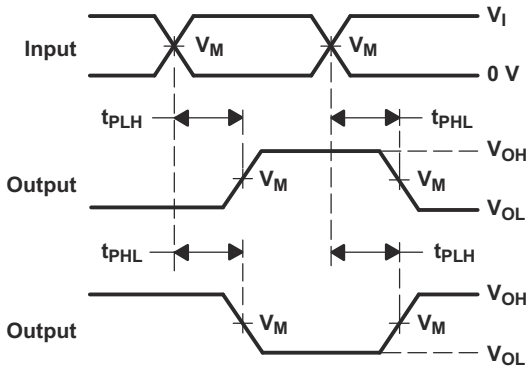
V_{CC}	INPUTS		V_M	V_{LOAD}	C_L	R_L	V_Δ
	V_I	t_r/t_f					
1.8 V ± 0.15 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V
2.5 V ± 0.2 V	V_{CC}	≤2 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V
3.3 V ± 0.3 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V
5 V ± 0.5 V	V_{CC}	≤2.5 ns	$V_{CC}/2$	$2 \times V_{CC}$	50 pF	500 Ω	0.3 V



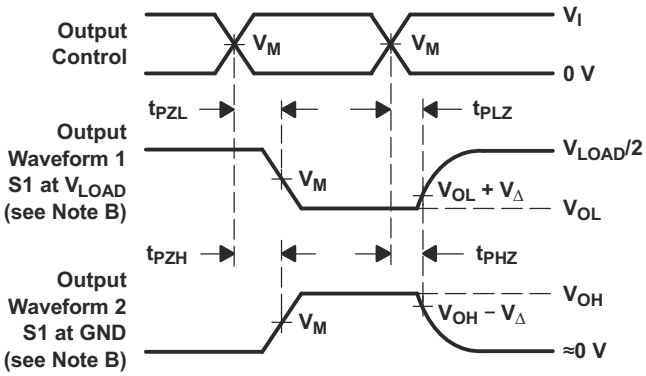
VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. C_L includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR≤ 10-MHz, Z_O = 50 Ω.
D. The outputs are measured one at a time, with one transition per measurement.
E. t_{PLZ} and t_{PHZ} are the same as t_{dis}.
F. t_{PZL} and t_{PZH} are the same as t_{en}.
G. t_{PLH} and t_{PHL} are the same as t_{pd}.
H. All parameters and waveforms are not applicable to all devices.

図 7-4. Load Circuit and Voltage Waveforms

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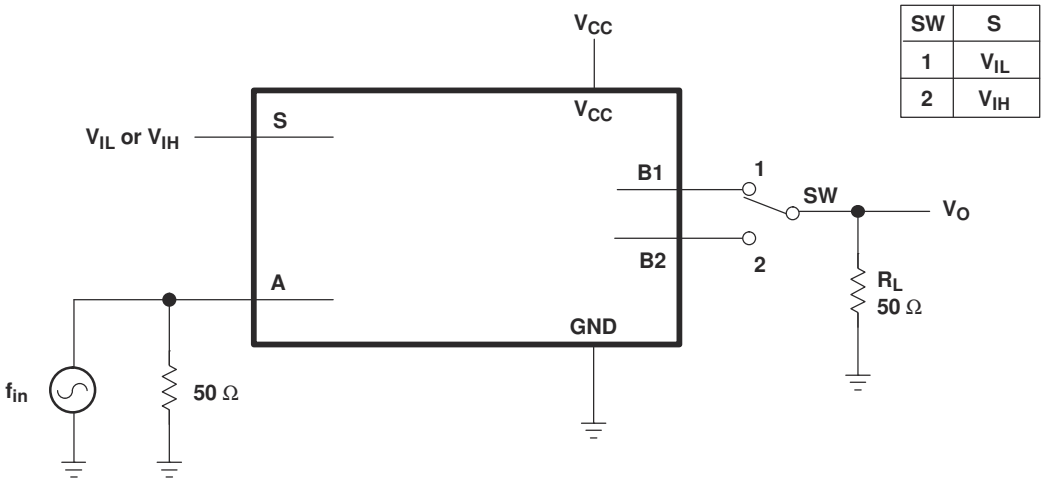

図 7-5. Frequency Response (Switch On)

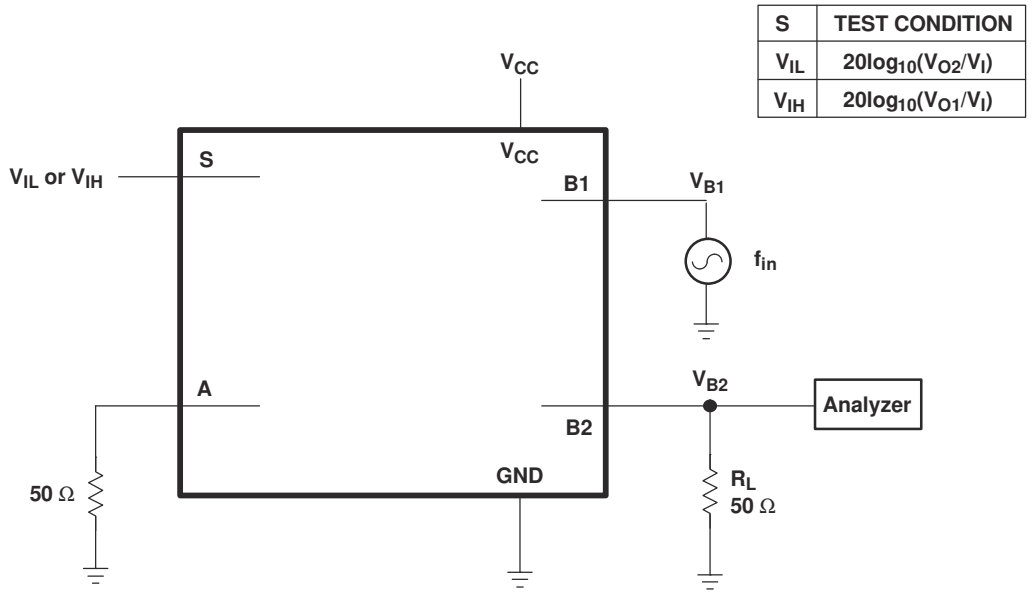

図 7-6. Crosstalk (Between Switches)

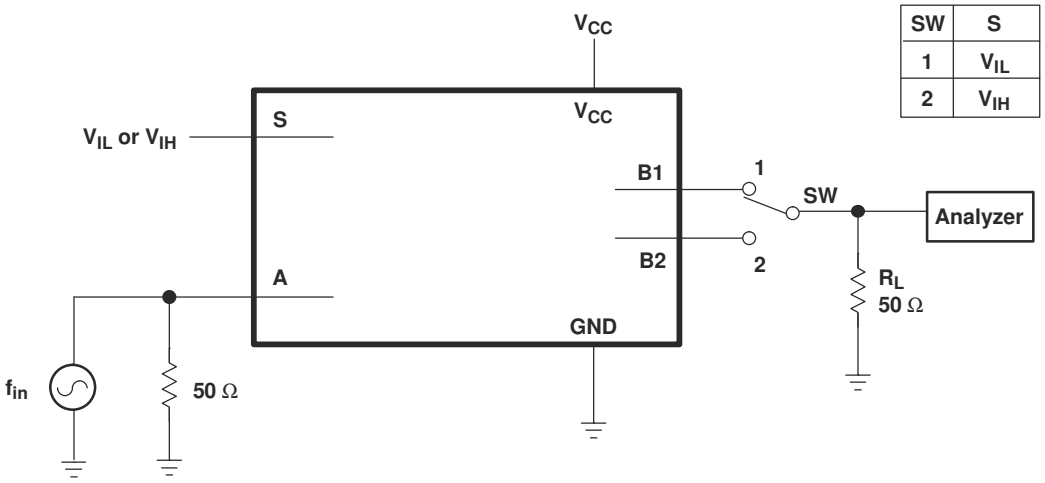

図 7-7. Feedthrough

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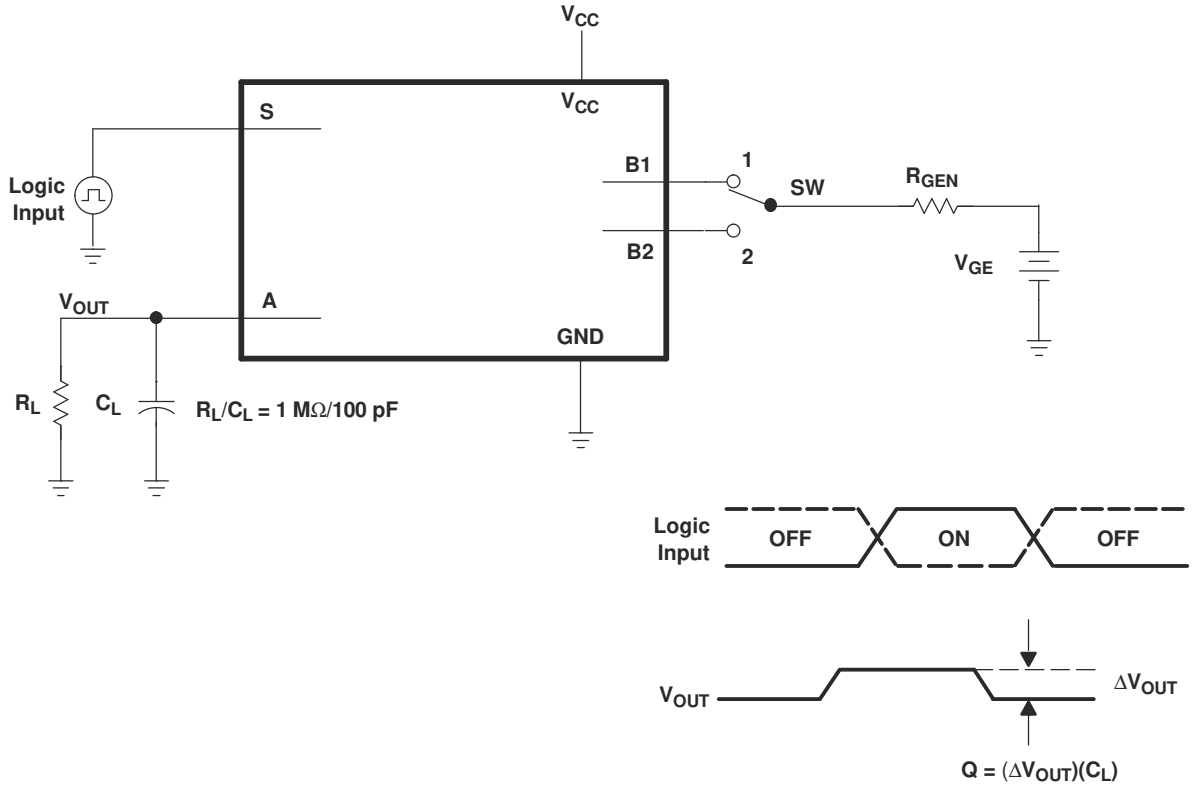
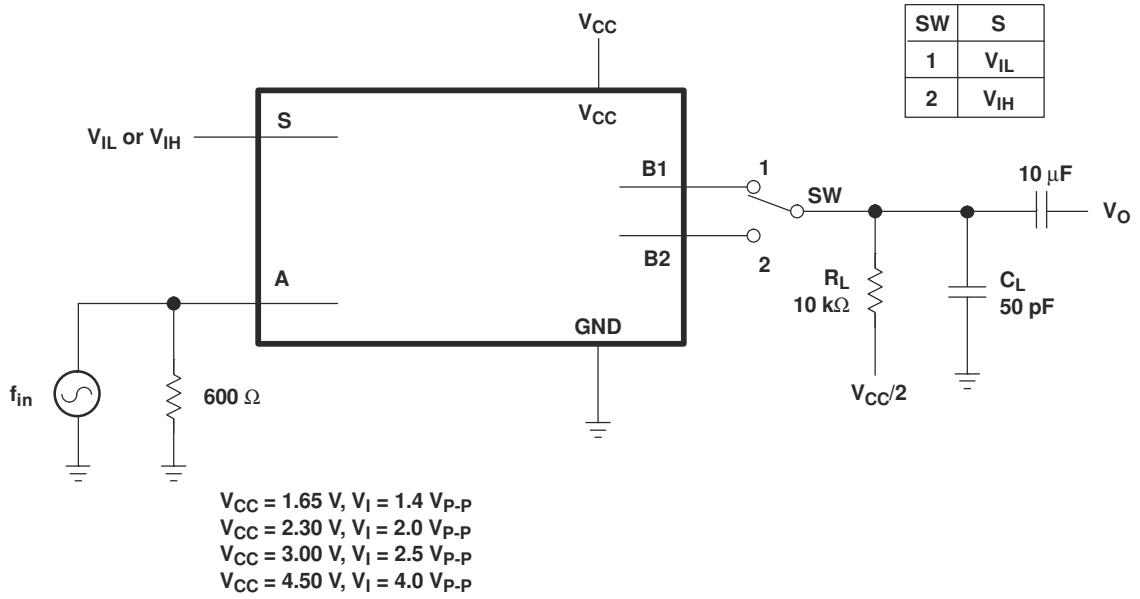


図 7-8. Charge-Injection Test



SW	S
1	V_{IL}
2	V_{IH}

図 7-9. Total Harmonic Distortion

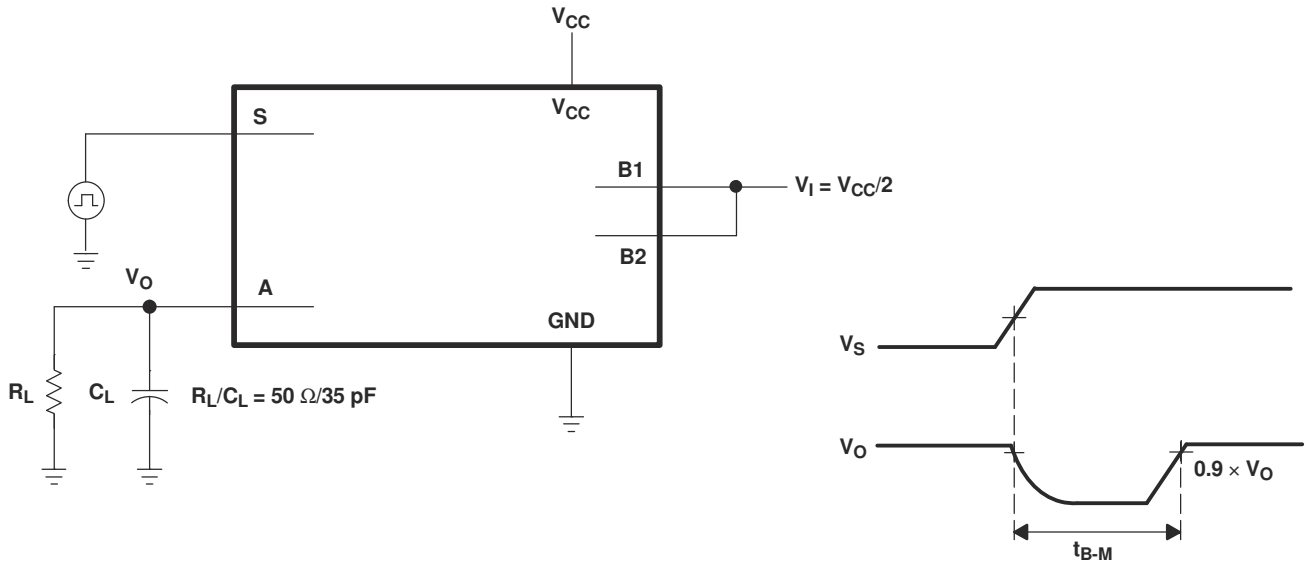


図 7-10. Break-Before-Make Internal Timing

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8 Detailed Description

8.1 Overview

The SN74LVC1G3157-Q1 device is a single-pole double-throw (SPDT) analog switch designed for 1.65-V to 5.5-V
V_{CC} operation. The SN74LVC1G3157-Q1 device can handle analog and digital signals. The device permits signals with amplitudes of up to V_{CC} (peak) to be transmitted in either direction.

8.2 Functional Block Diagram

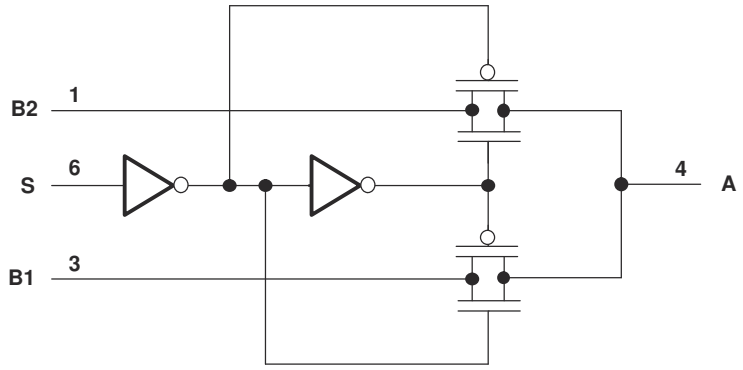

図 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

These devices are qualified for automotive applications. The 1.65-V to 5.5-V supply operation allows the device to function in many different systems comprised of different logic levels, allowing rail-to-rail signal switching. Either the B1 channel or the B2 channel is activated depending upon the control input. If the control input is low, B1 channel is selected. If the control input is high, B2 channel is selected.

8.4 Device Functional Modes

表 8-1 lists the ON channel when one of the control inputs is selected.

表 8-1. Function Table

CONTROL INPUTS	ON CHANNEL
L	B1
H	B2

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9 Application and Implementation

Note

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9.1 Application Information

The SN74LVC1G3157-Q1 SPDT analog switch is flexible enough for use in a variety of circuits such as analog audio routing, power-up monitor, memory sharing and so on. For details on the applications, you can also view SCYB014.

9.2 Typical Application

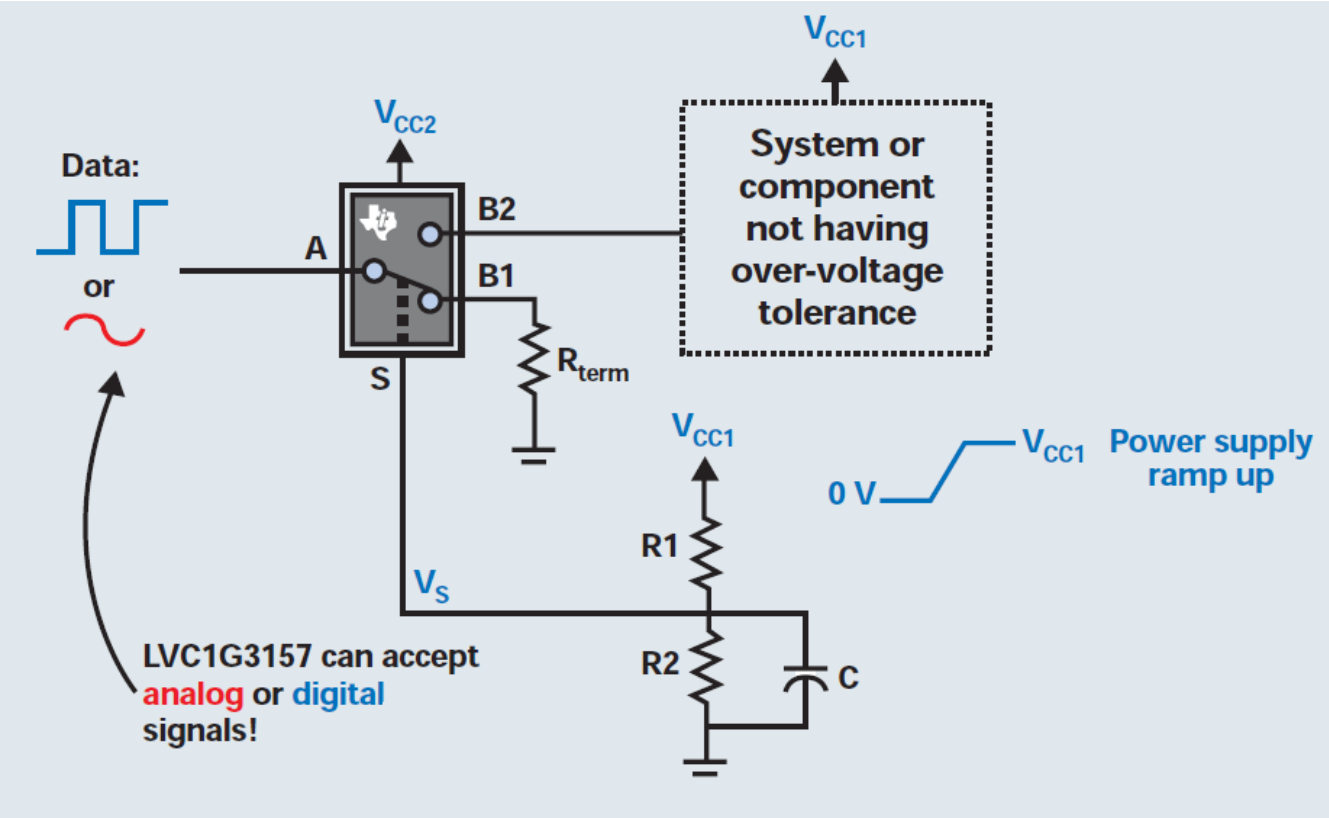

図 9-1. Typical Application Schematic

9.2.1 Design Requirements

The inputs can be analog or digital, but TI recommends waiting until VCC has ramped to a level in *セクション 6.3* before applying any signals. Appropriate termination resistors should be used depending on the type of signal and specification. The Select pin should not be left floating; either pull up or pull down with a resistor that can be overdriven by a GPIO.

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9.2.2 Detailed Design Procedure

Using this circuit idea, a system designer can ensure a component or subsystem power has ramped up before allowing signals to be applied to its input. This is useful for integrated circuits that do not have overvoltage tolerant inputs. The basic idea uses a resistor divider on the VCC1 power rail, which is ramping up. The RC time constant of the resistor divider further delays the voltage ramp on the select pin of the SPDT bus switch. By carefully selecting values for R1, R2 and C, it is possible to ensure that VCC1 will reach its nominal value before the path from A to B2 is established, thus preventing a signal being present on an I/O before the device/system is powered up. To ensure the minimum desired delay is achieved, the designer should use 式 1 to calculate the time required from a transition from ground (0 V) to half the supply voltage (VCC1/2).

$$\text{Set}\left(\frac{R2}{R1+R2}\times V_{CC1} > V_{IH}\right)\text{of the select pin} \tag{1}$$

Choose Rs and C to achieve the desired delay.

When Vs goes high, the signal will be passed.

9.2.3 Application Curve

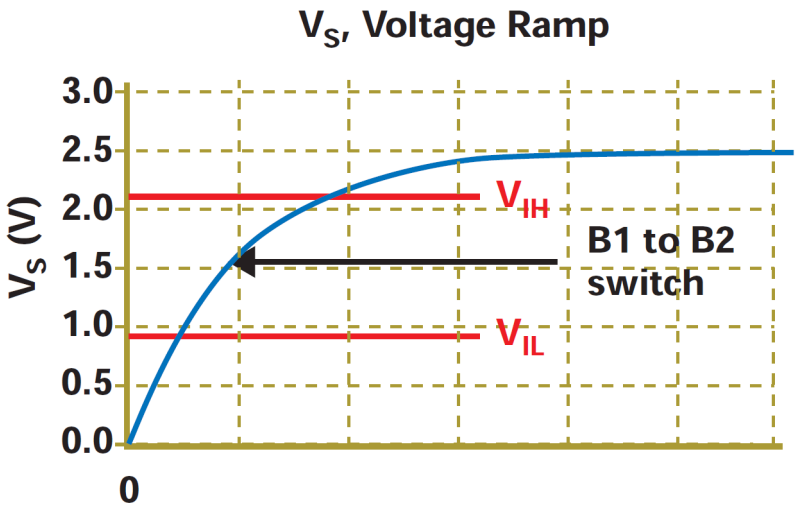

図 9-2. V_S Voltage Ramp

10 Power Supply Recommendations

Most systems have a common 3.3-V or 5-V rail that can supply the V_{CC} pin of this device. If this is not available, a Switch-Mode-Power-Supply (SMPS) or a Linear Dropout Regulator (LDO) can be used to provide supply to this device from another voltage rail.

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11 Layout

11.1 Layout Guidelines

TI recommends keeping signal lines as short as possible. TI also recommends incorporating microstrip or stripline techniques when signal lines are greater than 1 inch in length. These traces must be designed with a characteristic impedance of either 50 Ω or 75 Ω, as required by the application. Do not place this device too close to high-voltage switching components, as they may interfere with the device.

11.2 Layout Example

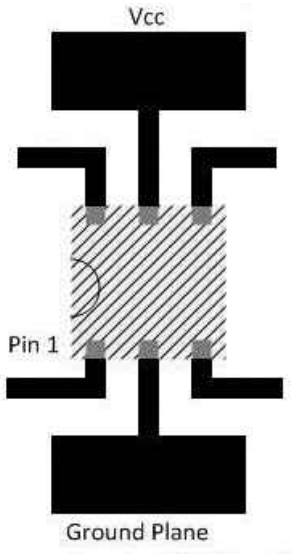

図 11-1. Recommended Layout Example

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12 Device and Documentation Support

12.1 Documentation Support

12.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *SN74LVC1G3157 and SN74LVC2G53 SPDT Analog Switches* product overview
- Texas Instruments, *SN74LVC1G3157-Q1 Functional Safety, FIT Rate, FMD, and Pin FMA* report

12.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

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12.4 Trademarks

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12.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
1P1G3157QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	CC5O	Samples
1P1G3157QDCKRQ1	ACTIVE	SC70	DCK	6	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	(C5J, C5O)	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF SN74LVC1G3157-Q1 :

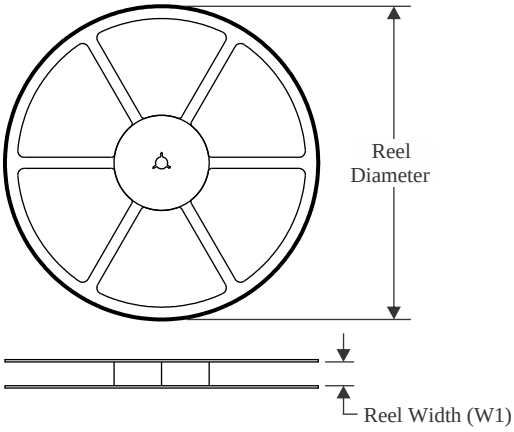
- Catalog : SN74LVC1G3157

NOTE: Qualified Version Definitions:

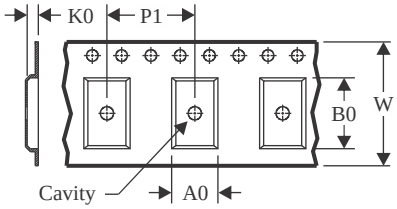
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

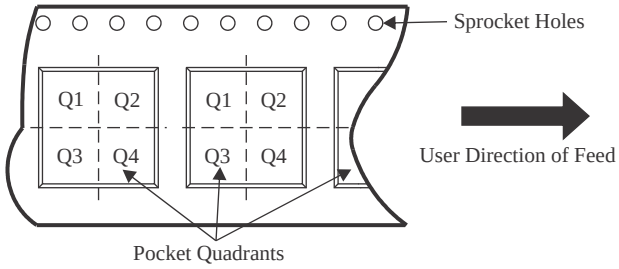


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

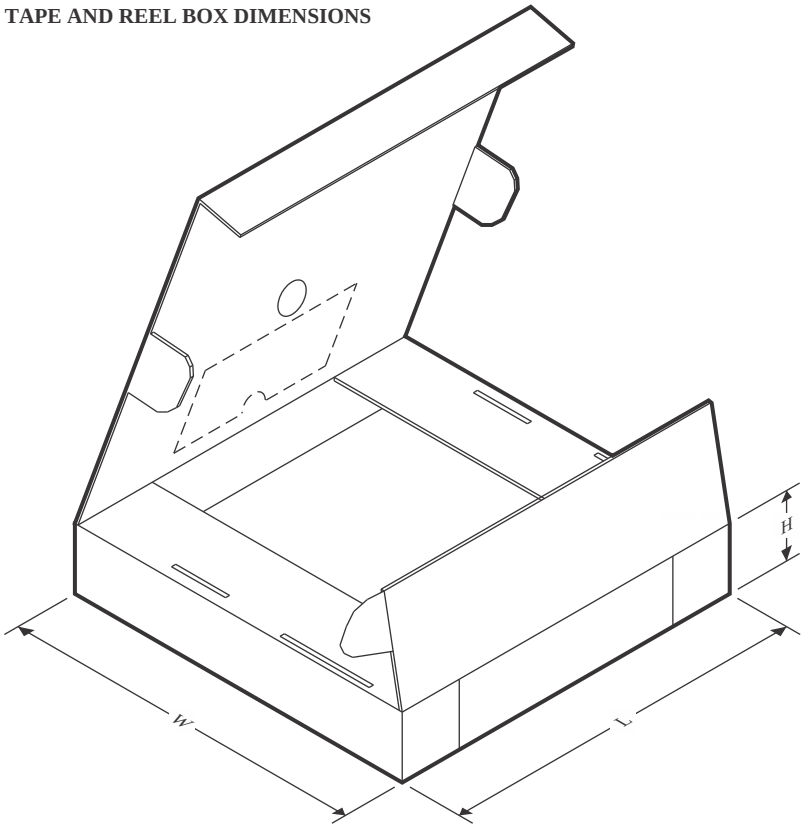
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
1P1G3157QDBVRQ1	SOT-23	DBV	6	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
1P1G3157QDCKRQ1	SC70	DCK	6	3000	179.0	8.4	2.2	2.5	1.2	4.0	8.0	Q3
1P1G3157QDCKRQ1	SC70	DCK	6	3000	178.0	9.0	2.4	2.5	1.2	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

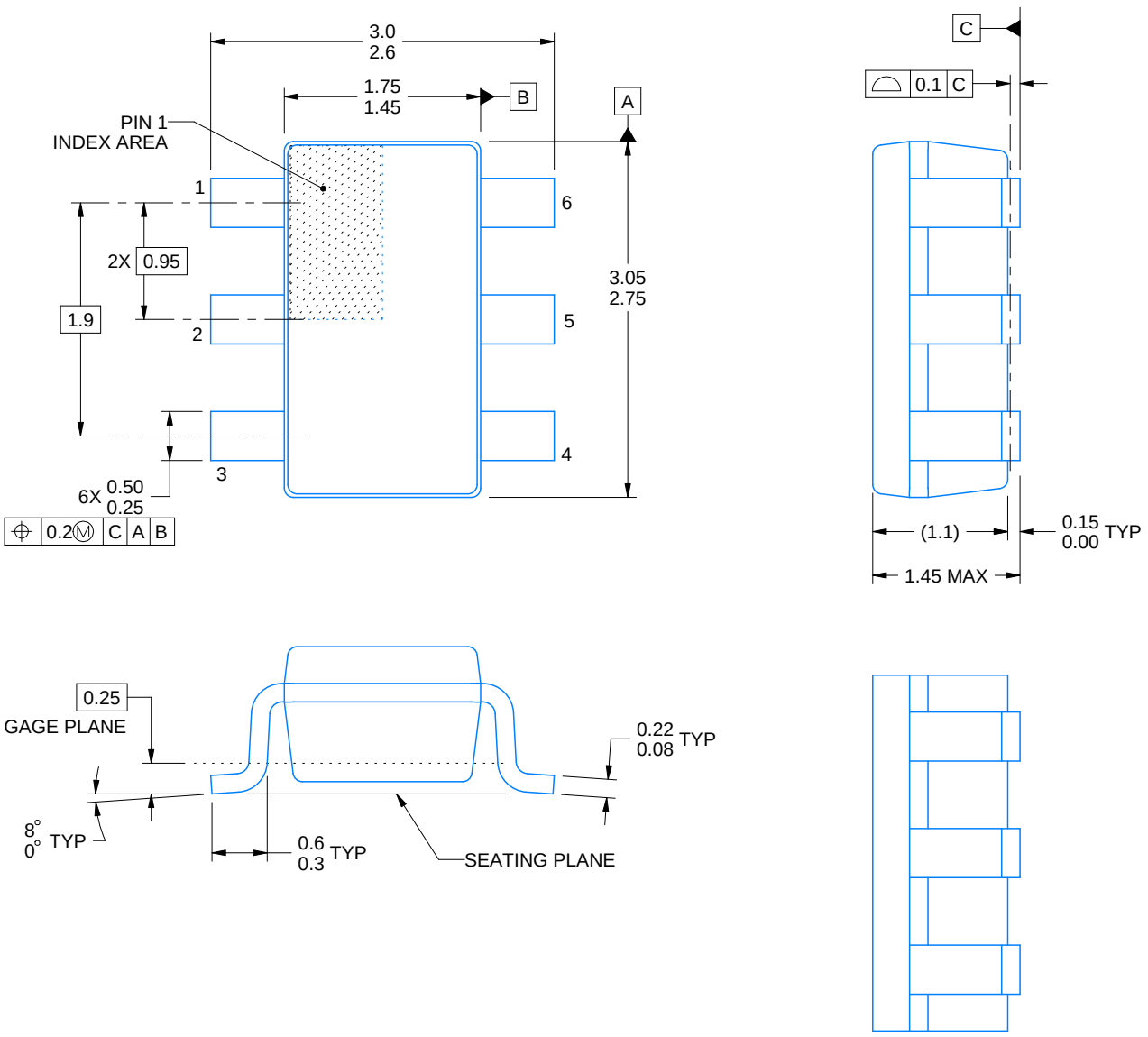
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
1P1G3157QDBVRQ1	SOT-23	DBV	6	3000	200.0	183.0	25.0
1P1G3157QDCKRQ1	SC70	DCK	6	3000	200.0	183.0	25.0
1P1G3157QDCKRQ1	SC70	DCK	6	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

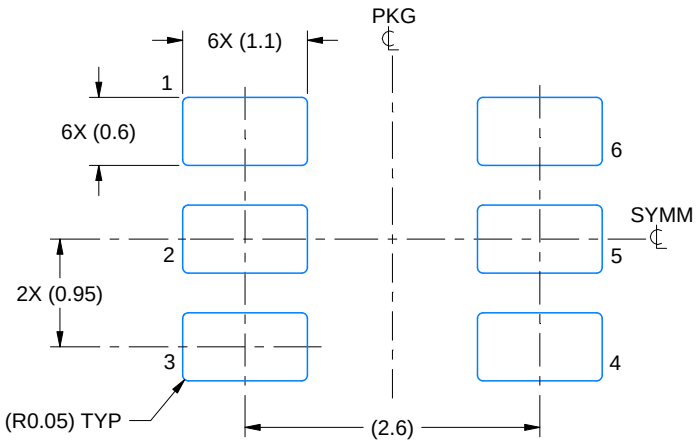


ALTERNATIVE PACKAGE SINGULATION VIEW

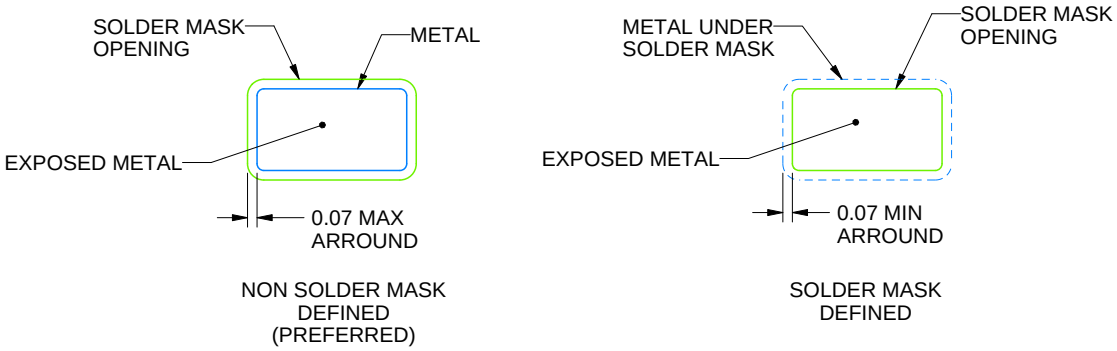
4214840/E 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

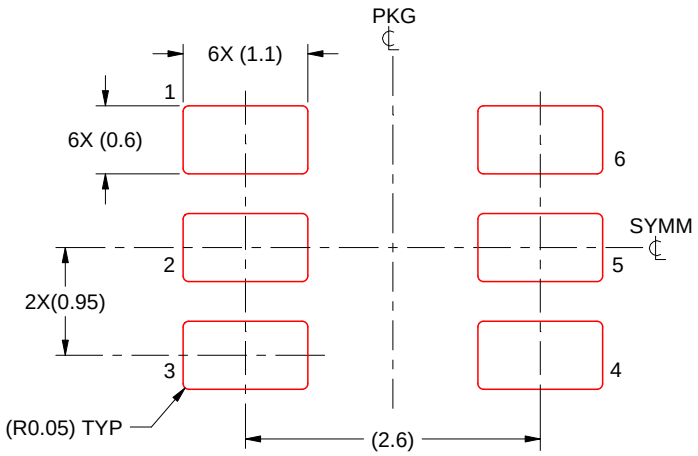


SOLDER MASK DETAILS

4214840/E 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



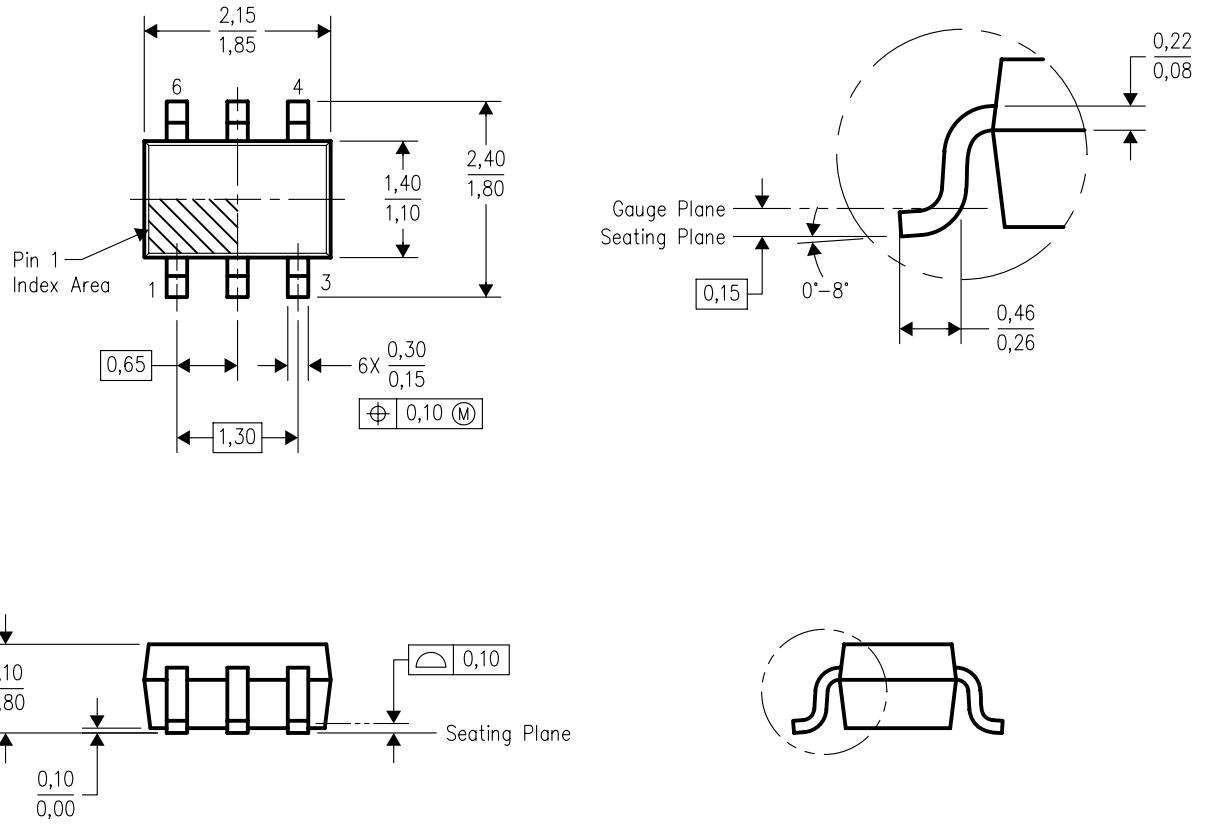
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/E 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

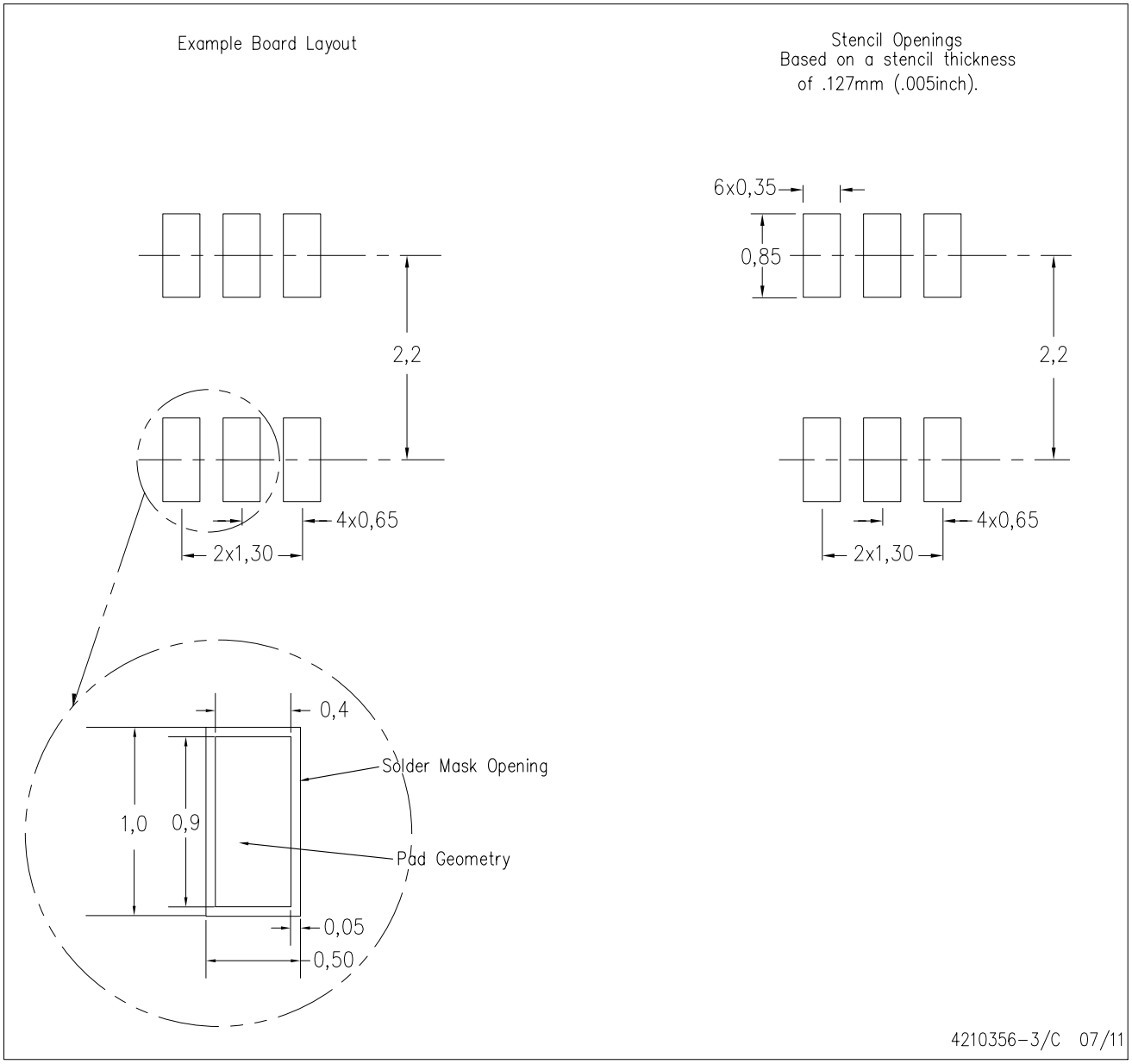
DCK (R–PDSO–G6) PLASTIC SMALL–OUTLINE PACKAGE



4093553–4/G 01/2007

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
D. Falls within JEDEC MO–203 variation AB.

DCK (R–PDSO–G6) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
D. Publication IPC–7351 is recommended for alternate designs.
E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC–7525 for other stencil recommendations.

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