TAC5312-Q1 車載対応、低消費電力、ステレオ オーディオ コーデック、プログラマブル昇圧機能、マイクバイアス、診断機能内蔵

1 特長

- 車載アプリケーション向けに AEC-Q100 認証済み
  - 温度グレード 1:-40℃ ≤ T_A ≤ +125℃
- ADC チャネル
  - 性能:
    - ライン差動入力のダイナミック レンジ:100dB
    - マイクロフォン差動入力のダイナミック レンジ:100dB
    - THD+N:-95dB
    - チャネル加算モードで高 SNR をサポート
  - 入力電圧:
    - 差動、$10V_{RMS}$ フルスケール入力
    - シングルエンド、$5V_{RMS}$ フルスケール入力
  - サンプル レート (f_S) = 8kHz～768kHz
  - プログラム可能なマイクロフォン バイアス (5V～10V)
    - 内蔵の高効率昇圧コンバータ
    - または外部の高電圧 HVDD 電源を使用
  - プログラム可能なマイクロフォン入力フォルト診断機能
    - 入力オープンまたは入力短絡
    - グランド、MICBIAS、VBAT との短絡
    - マイクロフォン バイアスの過電流保護
- DAC チャネル
  - DAC 性能:
    - DAC からライン出力までのダイナミック レンジ:106dB
    - DAC から HP 出力までのダイナミック レンジ:106dB
    - THD+N:-95dB
  - ヘッドフォン / ライン出力出力電圧:
    - 差動、$2V_{RMS}$ フルスケール
    - シングルエンド、$1V_{RMS}$ フルスケール
  - DAC サンプル レート (f_s) = 8KHz～768KHz
- 共通機能
  - 低レイテンシ フィルタ選択
  - プログラム可能な HPF およびバイクワッド フィルタ
  - I^2C 制御インターフェイス
  - オーディオ シリアル インターフェイス
    - フォーマット:TDM、I^2S、または左揃え
    - ワード長:16、20、24 または 32 ビット
  - プログラム可能な PLL による柔軟なクロック供給
  - 単電源動作 3.3V
  - I/O 電源動作:1.2V、1.8V、3.3V

2 アプリケーション

- 緊急通報 (E-Call)
- テレマティクス制御ユニット
- 車載用アクティブ ノイズ キャンセル
- 車載ヘッド ユニット

3 概要

TAC5312-Q1 は、$10V_{RMS}$ の差動入力、100dB のステレオ ADC および $2V_{RMS}$ のステレオ DAC チャネルを備えた、高性能な低消費電力ステレオ コーデックです。TAC5312-Q1 は、差動とシングルエンドの両方の入力および出力をサポートしています。デバイスは、ADC チャネルでマイク入力とライン入力の両方をサポートしています。DAC 出力は、ライン出力とヘッドフォン負荷のいずれかに構成できます。TAC5312-Q1 は、ヘッドホン負荷に最大 62.5mW を駆動できます。また、このデバイスは、高電圧のプログラム可能なマイクロフォン バイアスと、入力診断回路 (直結入力に対する完全なフォルト診断機能により、マイクロフォンを使用した車載用システムに直接接続可能) を内蔵しています。TAC5312-Q1 は、外部の低電圧 3.3V 電源を使用して高電圧のマイクロフォン バイアスを生成するために高効率昇圧コンバータを内蔵しています。また、このデバイスは、外部の高電圧電源 (HVDD) を直接使用することもできます。この HVDD は、プログラム可能な高電圧マイクロフォン バイアスを生成するためにシステムですぐに利用できる電源です。TAC5312-Q1 は、プログラム可能なチャネル ゲイン、デジタル音量制御、低ジッタのフェーズ ロック ループ (PLL)、プログラム可能なハイパス フィルタ (HPF)、プログラム可能な EQ およびバイクワッド フィルタ、低レイテンシのフィルタ モードを備えています。最大 768kHz のサンプリング レートに対応可能です。TAC5312-Q1 は時分割多重化 (TDM)、I^2S、左揃え (LJ) オーディオ フォーマットに対応しており、I^2C で制御できます。これらの高性能な機能を内蔵し、3.3V の単一電源で動作するため、TAC5312-Q1 は、スペースに制約のある車載用システムに最適な選択肢です。

製品情報

部品番号	パッケージ (1)	パッケージ サイズ(2)
TAC5312-Q1	WQFN (28)	4.0mm × 4.0mm
	WQFN (32)	5.0mm × 5.0mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。

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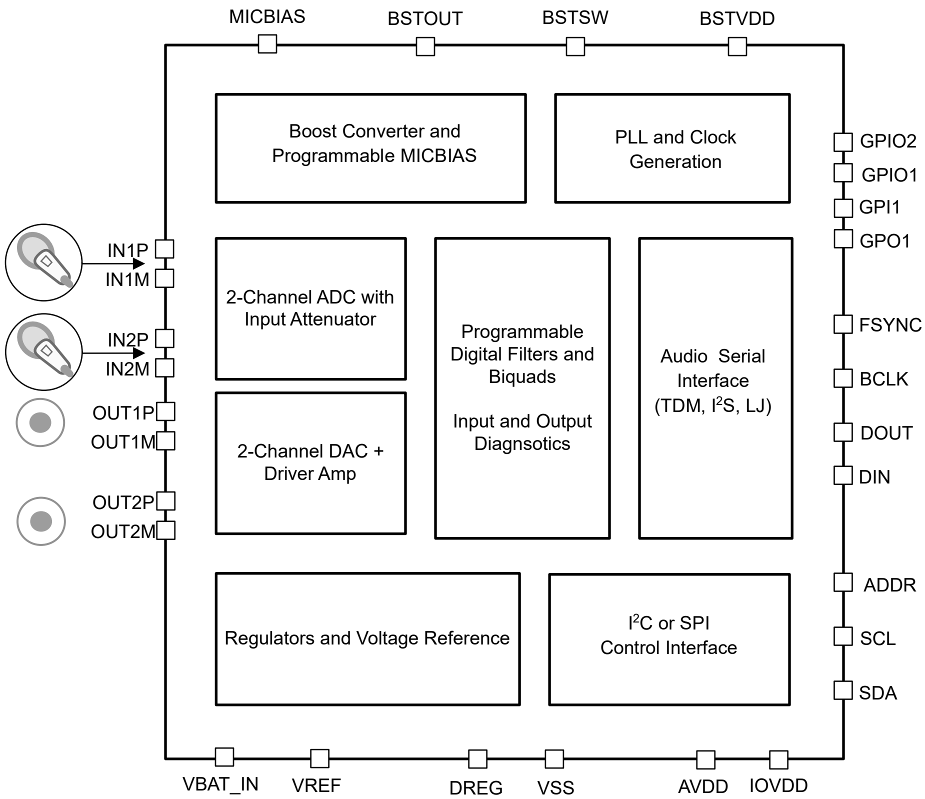

概略ブロック図

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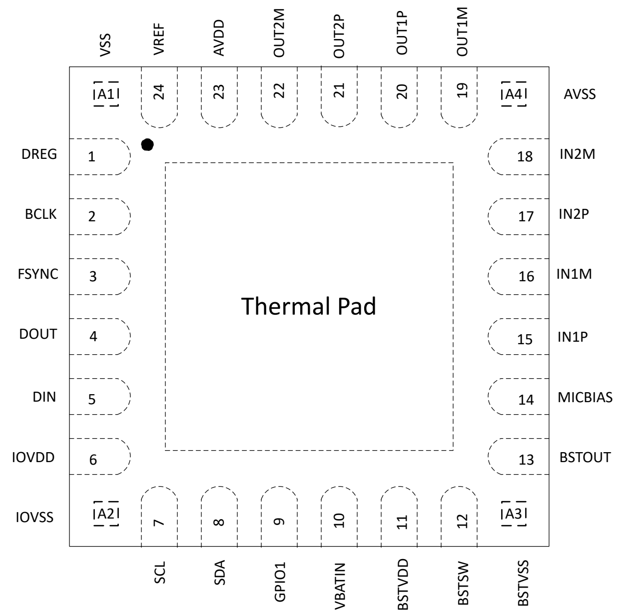
4 Pin Configuration and Functions



Not to scale
Pinout is subject to changes

図 4-1. TAC5312-Q1 RGE Package, 28-Pin WQFN With Exposed Thermal Pad, Top View

表 4-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VSS	A1	Ground	Short directly to board Ground Plane.
DREG	1	Digital Supply	Digital on-chip regulator output voltage for digital supply (1.5V, nominal)
BCLK	2	Digital I/O	Audio serial data interface bus bit clock
FSYNC	3	Digital I/O	Audio serial data interface bus frame synchronization signal
DOUT	4	Digital Output	Audio serial data interface bus output
DIN	5	Digital Input	Audio serial data interface bus input
IOVDD	6	Digital Supply	Digital I/O power supply (1.8V or 3.3V, nominal)
IOVSS	A2	Ground	Short directly to board Ground Plane.
SCL	7	Digital Input	Clock for I^2C Control Interface
SDA	8	Digital I/O	Data for I^2C Control Interface
GPIO1	9	Digital I/O	General-purpose digital input/output 1 (multipurpose functions such as daisy-chain input, audio data output, PLL input clock source, interrupt, and so forth)
VBAT_IN	10	Analog	Analog VBAT input monitoring pin (used for input diagnostics)
BSTVDD	11	Analog Supply	Boost converter supply voltage (3.3V, nominal)
BSTSW	12	Analog Supply	Boost converter switching Pin
BSTVSS	A3	Ground	Short directly to board Ground Plane.

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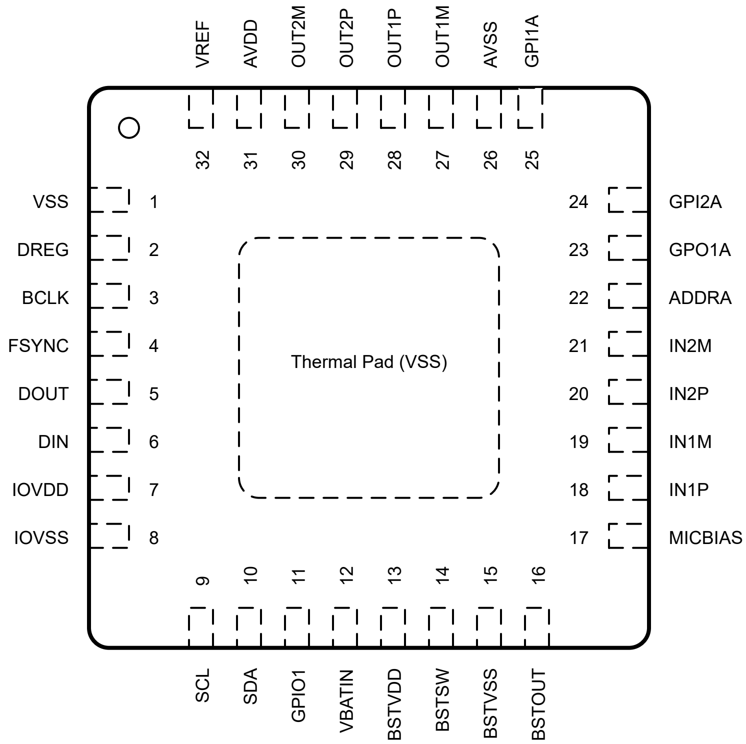
表 4-1. Pin Functions (続き)

PIN		TYPE[(1)]	DESCRIPTION
NAME	NO.		
BSTOUT	13	Analog Supply	Boost Convertor Output Voltage
MICBIAS	14	Analog	MICBIAS Output (Porgrammable output upto 11V)
IN1P	15	Analog Input	Analog Input 1P Pin
IN1M	16	Analog Input	Analog Input 1M Pin
IN2P	17	Analog Input	Analog Input 2P Pin
IN2M	18	Analog Input	Analo Input 2M Pin
AVSS	A4	Ground	Short directly to board Ground Plane.
OUT1M	19	Analog Output	Analog Output 1M Pin
OUT1P	20	Analog Output	Analog Output 1P Pin
OUT2P	21	Analog Output	Analog Output 2P Pin
OUT2M	22	Analog Output	Analog Output 2M Pin
AVDD	23	Analog Supply	Analog power (3.3V, nominal)
VREF	24	Analog	Analog reference voltage filter output



Not to scale
Pinout is subject to changes

図 4-2. TAC5312-Q1 RTV Package, 32-Pin WQFN With Exposed Thermal Pad, Top View

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表 4-2. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
VSS	1	Ground	Short directly to board Ground Plane.
DREG	2	Digital Supply	Digital on-chip regulator output voltage for digital supply (1.5V, nominal)
BCLK	3	Digital I/O	Audio serial data interface bus bit clock
FSYNC	4	Digital I/O	Audio serial data interface bus frame synchronization signal
DOUT	5	Digital Output	Audio serial data interface bus output
DIN	6	Digital Input	Audio serial data interface bus input
IOVDD	7	Digital Supply	Digital I/O power supply (1.8V or 3.3V, nominal)
IOVSS	8	Ground	Short directly to board Ground Plane.
SCL	9	Digital Input	Clock for I^2C Control Interface
SDA	10	Digital I/O	Data for I^2C Control Interface
GPIO1	11	Digital I/O	General-purpose digital input/output 1 (multipurpose functions such as daisy-chain input, audio data output, PLL input clock source, interrupt, and so forth)
VBAT_IN	12	Analog	Analog VBAT input monitoring pin (used for input diagnostics)
BSTVDD	13	Analog Supply	Boost converter supply voltage (3.3V, nominal)
BSTSW	14	Analog Supply	Boost converter switching Pin
BSTVSS	15	Ground	Short directly to board Ground Plane.
BSTOUT	16	Analog Supply	Boost Convertor Output Voltage
MICBIAS	17	Analog	MICBIAS Output (Porgrammable output upto 11V)
IN1P	18	Analog Input	Analog Input 1P Pin
IN1M	19	Analog Input	Analog Input 1M Pin
IN2P	20	Analog Input	Analog Input 2P Pin
IN2M	21	Analog Input	Analo Input 2M Pin
ADDRA	22	Digital Input	I2C Address Pin
GPO1A	23	Digital Output	General-purpose digital output 1 (multipurpose functions such as audio data output, interrupt, and so forth)
GPI2A	24	Digital Input	General-purpose digital input 2 (multipurpose functions such as daisy-chain input, PLL input clock source, and so forth)
GPI1A	25	Digital Input	General-purpose digital input 1 (multipurpose functions such as daisy-chain input, PLL input clock source, and so forth)
AVSS	26	Ground	Short directly to board Ground Plane.
OUT1M	27	Analog Output	Analog Output 1M Pin
OUT1P	28	Analog Output	Analog Output 1P Pin

表 4-2. Pin Functions (続き)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
OUT2P	29	Analog Output	Analog Output 2P Pin
OUT2M	30	Analog Output	Analog Output 2M Pin
AVDD	31	Analog Supply	Analog power (3.3V, nominal)
VREF	32	Analog	Analog reference voltage filter output

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power.

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5 Specifications

5.1 Absolute Maximum Ratings

over the operating ambient temperature range (unless otherwise noted)[(1)]

		MIN	MAX	UNIT
Supply voltage	AVDD to AVSS	–0.3	3.9	V
Supply voltage	BSTVDD to VSS (thermal pad)	–0.3	3.9	V
Supply voltage	IOVDD to VSS (thermal pad)	–0.3	3.9	V
Supply voltage	BSTOUT(External HVDD Mode) to VSS (thermal pad)	–0.3	14	V
Ground voltage differences	AVSS to VSS (thermal pad)	–0.3	0.3	V
Battery voltage	VBAT_IN to AVSS	–0.3	18	V
Analog input voltage	Analog input pins voltage to AVSS	–0.3	18	V
Digital input voltage	Digital input pins voltage to VSS (thermal pad)	–0.3	IOVDD + 0.3	V
Temperature	Operating ambient, T_A	–40	125	°C
	Junction, T_J	–40	150	
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002[(1)]		±2000	V
		Charged-device model (CDM), per AEC Q100-011	Corner package pins	±750	
			All other non-corner package pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
POWER					
AVDD[(1)]	Analog supply voltage to AVSS AVDD-3.3V Operation	3.0	3.3	3.6	V
BSTVDD	Boost converter supply voltage to VSS (thermal pad)	3.0	3.3	3.6	V
IOVDD	IO supply voltage to VSS (thermal pad) - IOVDD 3.3-V operation	3.0	3.3	3.6	V
	IO supply voltage to VSS (thermal pad) - IOVDD 1.8-V operation	1.65	1.8	1.95	
IOVDD	IO supply voltage to VSS (thermal pad) - IOVDD 1.2-V operation	1.08	1.2	1.32	V
BSTOUT	BSTOUT supply voltage to VSS in external HVDD Mode (thermal pad)	5.6	9	12	V
INPUTS					
VBAT_IN	VBAT_IN input pin voltage to AVSS	0	12.6	18	V
INxx	Analog input pins voltage to AVSS for line-in recording	0		14.2	V
	Analog input pins voltage to AVSS for microphone recording	0.1		MICBIAS – 0.1	V
	Analog input pins voltage to AVSS during short to VBAT_IN			VBAT_IN	V
	Digital input pins(except ADDRA, GPO1A, GPI1A, GPI2A) voltage to VSS (thermal pad)	0		IOVDD	V
	Digital input pins(ADDRA, GPO1A, GPI1A, GPI2A) w.r.t AVSS	0		AVDD	V
TEMPERATURE					
T_A	Operating ambient temperature	–40		125	°C

		MIN	NOM	MAX	UNIT
OTHERS					
	GPIOx or GPIx (used as MCLK input) clock frequency			36.864(2)	MHz
C_b	SCL and SDA bus capacitance for I^2C interface supports standard-mode and fast-mode			400	pF
	SCL and SDA bus capacitance for I^2C interface supports fast-mode plus			550	
C_L	Digital output load capacitance		20	50	pF
	Boost converter inductor for TBD clocking mode		TBD		µH

(1) AVSS and VSS (thermal pad); all ground pins must be tied together and must not differ in voltage by more than 0.2 V.
(2) MCLK input rise time (V_{IL} to V_{IH}) and fall time (V_{IH} to V_{IL}) must be less than 5 ns. For better audio noise performance, MCLK input must be used with low jitter.

5.4 Thermal Information

THERMAL METRIC(1)		TAC5312-Q1 RGE (VQFN) 24 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	38.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	26.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	15.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	13.8	°C/W

(1) For more information about traditional and new thermal metrics, see the spra953 application report.

5.5 Thermal Information

THERMAL METRIC(1)		TAC5312-Q1 RTV (WQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	19.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	11.5	°C/W

(1) For more information about traditional and new thermal metrics, see the spra953 application report.

5.6 Thermal Information

THERMAL METRIC(1)		TAC5311-Q1 RTV (WQFN) 32 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	39.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	18.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	19.5	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.2	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	19.5	°C/W

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THERMAL METRIC[1]		TAC5311-Q1 RTV (WQFN) 32 PINS	UNIT
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	11.5	°C/W

(1) For more information about traditional and new thermal metrics, see the spra953 application report.

5.7 Electrical Characteristics

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, BSTVDD = 3.3 V, HVDD = 11 V (for external HVDD case), f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 x f_S, TDM slave mode and PLL on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
ADC PERFORMANCE FOR LINE INPUT RECORDING						
	Differential input full-scale AC signal voltage	AC-coupled input, input fault diagnostic not supported		10		V_{RMS}
		DC-coupled input, DC common-mode voltage INxP = INxM = 7.1 V, input fault diagnostic not supported				
	Single-ended input full-scale AC signal voltage	AC-coupled input, input fault diagnostic not supported		5		V_{RMS}
		DC-coupled input, DC common-mode voltage INxP = INxM = 7.1 V, input fault diagnostic not supported				
SNR	Signal-to-noise ratio, A-weighted[1] [2]	IN1 differential AC-coupled input selected and AC signal shorted to ground, 0-dB channel gain		100		dB
		IN1 differential DC-coupled input selected and AC signal shorted to ground, 0-dB channel gain		100		
		IN1 differential DC-coupled input selected and AC signal shorted to ground, 12-dB channel gain		90		
DR	Dynamic range, A-weighted[2]	IN1 differential AC-coupled input selected and –60-dB full-scale AC signal input, 0-dB channel gain		100		dB
		IN1 differential DC-coupled input selected and –60-dB full-scale AC signal input, 0-dB channel gain		100		
		IN1 differential DC-coupled input selected and –72-dB full-scale AC signal input, 12-dB channel gain		96		
THD+N	Total harmonic distortion[2]	IN1 differential AC-coupled input selected and –1-dB full-scale AC signal input, 0-dB channel gain		–88	TBD	dB
		IN1 differential DC-coupled input selected and –1-dB full-scale AC signal input, 0-dB channel gain		–88		
		IN1 differential DC-coupled input selected and –13-dB full-scale AC signal input, 12-dB channel gain		–91		
ADC PERFORMANCE FOR MICROPHONE INPUT RECORDING						
ADC OTHER PARAMETERS						
	Input impedance	Differential input, between INxP and INxM		66.6		kΩ
		Single-ended input, between INxP and INxM		33.3		
	Offset	Shorted Input.		TBD		mV
	Digital volume control range	Programmable 0.5-dB steps	–120		42	dB
	Input Signal Bandwidth	Upto 192KSPS FS Rate		0.46		FS
		>192KSPS		90		kHz
	Output data sample rate	Programmable	3.675		768	kHz

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, BSTVDD = 3.3 V, HVDD = 11 V (for external HVDD case), f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 x f_S, TDM slave mode and PLL on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
	Output data sample word length	Programmable	16		32	Bits
	Digital high-pass filter cutoff frequency	First-order IIR filter with programmable coefficients, –3-dB point (default setting)		2		Hz
	Interchannel isolation	–1-dB full-scale AC signal line-in input to non measurement channel		–134		dB
	Interchannel gain mismatch	–6-dB full-scale AC signal line-in input, 0-dB channel gain		0.1		dB
	Interchannel phase mismatch	1-kHz sinusoidal signal		0.01		Degrees
PSRR	Power-supply rejection ratio	100-mV$_{PP}$, 1-kHz sinusoidal signal on AVDD, differential input selected, 0-dB channel gain		92		dB
CMRR	Common-mode rejection ratio	Differential microphone input selected, 0-dB channel gain, 1-V$_{RMS}$ AC input, 1-kHz signal on both pins and measure level at output, CHx_CFG0 D3-2 register bits set to 2b'10 to configure device in high CMRR performance mode		54		dB
MICROPHONE BIAS						
	MICBIAS noise	BW = 20 Hz to 20 kHz, A-weighted, 1-μF capacitor between MICBIAS and AVSS		20		μV$_{RMS}$
	MICBIAS voltage	Programmable 0.5-V steps	3		10	V
	MICBIAS current drive	MICBIAS voltage 10 V			30	mA
	MICBIAS load regulation	MICBIAS voltage 10 V, measured up to maximum load	0		1	%
	MICBIAS over current protection threshold	MICBIAS voltage 10 V	35			mA
INPUT DIAGNOSTICS						
	Fault monitoring repetition rate	Programmable, DC-coupled input	1	4	8	ms
	Fault response time	Fault monitoring repetition rate 4-ms, DC-coupled input		16		ms
	Threshold voltage for (INxx – AVSS) input shorted to ground	Programmable 60-mV steps, DC-coupled input	0		900	mV
	Threshold voltage for (INxP – INxM) input shorted together	Programmable 30-mV steps, DC-coupled input	0		450	mV
	Threshold voltage for (MICBIAS – INxx) input shorted to MICBIAS	Programmable 30-mV steps, DC-coupled input	0		450	mV
	Threshold voltage for (VBAT – INxx) input shorted to VBAT_IN	Programmable 30-mV steps, DC-coupled input	0		450	mV
Analog Bypass to Line Out/Head Phone Amplifier						
	Input impedance	Differential input, between INxP and INxM		TBD		kΩ
		Single-ended input, between INxP and INxM		TBD		
	Single Ended Full Scale Output	AVDD=3.3V		5		Vrms
	Differential Full Scale Output	AVDD=3.3V		10		Vrms

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at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, BSTVDD = 3.3 V, HVDD = 11 V (for external HVDD case), f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 x f_S, TDM slave mode and PLL on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
	Gain Error			0.1		dB
	Noise, A-Weighted	Idle Channel, Input Shorted to Ground		4		μV_{RMS}
SNR	Signal-to-noise ratio, A-weighted(1) (2)	Idle Channel, Input Shorted to Ground, AVDD=3.3V		102		dB
THD+N	Total harmonic distortion(2)	IN1 differential AC-coupled input selected and -1-dB full-scale AC signal input, 0-dB channel gain		TBD		dB
DAC Performance for Line Output/Head Phone Playback						
	Full Scale Output Voltage	Differential output between OUTxP and OUTxM, AVDD=3.3V		2		V_{RMS}
		Single-ended Output, AVDD=3.3V		1		
		Pseudo Differential Output between OUTxP and OUTxM, AVDD=3.3V		1		
SNR	Signal-to-noise ratio, A-weighted(1) (2)	Differential Output, 0dBFS Signal, AVDD=3.3V		106		dB
		Single Ended Output, 0dBFS Signal, AVDD=3.3V		103		
		Pseudo Differential Output, 0dBFS Signal, AVDD=3.3V		96		
		Differential Output, 0dBFS Signal, AVDD=3.3V, 0dBFS Signal, Power Tune Mode		TBD		dB
		Single Ended Output, 0dBFS Signal, AVDD=3.3V, Power Tune Mode		TBD		
		Pseudo Differential Output, 0dBFS Signal, AVDD=3.3V, Power Tune Mode				
DR	Dynamic range, A-weighted(2)	Differential Output, -60dBFS Signal, AVDD=3.3V		106		dB
		Single Ended Output, -60dBFS Signal, AVDD=3.3V		103		
		Pseudo Differential Output, -60dBFS Signal, AVDD=3.3V		96		
		Differential Output, -60dBFS Signal, AVDD=3.3V, 0dBFS Signal, Power Tune Mode				dB
		Single Ended Output, -60dBFS Signal, AVDD=3.3V, Power Tune Mode				
		Pseudo Differential Output, -60dBFS Signal, AVDD=3.3V, Power Tune Mode				
THD+N	Total harmonic distortion(2)			–95		dB
	Head Phone Load Range			16		Ω
	Line Out Load Range		600			Ω
	Channel gain control range	Programmable 1-dB steps	–6		12	dB
DAC Channel OTHER PARAMETERS						
	Output Offset	0 Input		TBD		mV
	Output Common Mode	Common Mode Level for OUTxP and OUTxM AVDD=3.3V (Register Configurable) Common Mode Level for OUTxP and OUTxM AVDD=3.3V		1.625		V
	Common Mode Error	DC Error in Common Mode Voltage		±10		mV
	Digital volume control range	Programmable 0.5-dB steps	–120		42	dB

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, BSTVDD = 3.3 V, HVDD = 11 V (for external HVDD case), f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 x f_S, TDM slave mode and PLL on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
	Output Signal Bandwidth	Upto 192KSPS FS Rate		0.46		FS
		>192KSPS		90		kHz
	Input data sample rate	Programmable	7.35		768	kHz
	Input data sample word length	Programmable	16		32	Bits
	Digital high-pass filter cutoff frequency	First-order IIR filter with programmable coefficients, –3-dB point (default setting)		2		Hz
	Interchannel isolation			–134		dB
	Interchannel gain mismatch			0.1		dB
	Interchannel phase mismatch	1-kHz sinusoidal signal		0.01		Degrees
PSRR	Power-supply rejection ratio	100-mV_{PP}, 1-kHz sinusoidal signal on AVDD, differential input selected, 0-dB channel gain		92		dB
	Mute Attenuation			–130		dB
P_{out}	Output Power Delivery	Single ended/Pseudo Differential R_L=16 Ohms, THD+N<1%		62.5		mW
Line Out DIAGNOSTICS						
DIGITAL I/O						
V_{IL}	Low-level digital input logic voltage threshold	All digital pins except GPI1A, GPI2A, ADDRA, SDA and SCL, IOVDD 1.8-V operation	–0.3		0.35 x IOVDD	V
		All digital pins except GPI1A, GPI2A, ADDRA, SDA and SCL, IOVDD 3.3-V operation	–0.3		0.8	
V_{IH}	High-level digital input logic voltage threshold	All digital pins except GPI1A, GPI2A, ADDRA, SDA and SCL, IOVDD 1.8-V operation	0.65 x IOVDD		IOVDD + 0.3	V
		All digital pins except GPI1A, GPI2A, ADDRA, SDA and SCL, IOVDD 3.3-V operation	2		IOVDD + 0.3	
V_{OL}	Low-level digital output voltage	All digital pins except GPO1A, SDA and SCL, I_{OL} = –2 mA, IOVDD 1.8-V operation			0.45	V
		All digital pins except GPO1A, SDA and SCL, I_{OL} = –2 mA, IOVDD 3.3-V operation			0.4	
V_{OH}	High-level digital output voltage	All digital pins except GPO1A, SDA and SCL, I_{OH} = 2 mA, IOVDD 1.8-V operation	IOVDD – 0.45			V
		All digital pins except GPO1A, SDA and SCL, I_{OH} = 2 mA, IOVDD 3.3-V operation	2.4			
$V_{IL(AVDD)}$	Low-level digital input logic voltage threshold	For Pins GPI1A, GPI2A, ADDRA	–0.3		0.35 x AVDD	V
$V_{IH(AVDD)}$	High-level digital input logic voltage threshold	For Pins GPI1A, GPI2A, ADDRA	0.65 x AVDD		AVDD + 0.3	V
$V_{OL(AVDD)}$	Low-level digital output voltage	For GPO1A Pin			0.45	V
$V_{OH(AVDD)}$	High-level digital output voltage	For GPO1A Pin	AVDD – 0.45			V
$V_{IL(I2C)}$	Low-level digital input logic voltage threshold	SDA and SCL	–0.5		0.3 x IOVDD	V
$V_{IH(I2C)}$	High-level digital input logic voltage threshold	SDA and SCL	0.7 x IOVDD		IOVDD + 0.5	V
$V_{OL1(I2C)}$	Low-level digital output voltage	SDA, $I_{OL(I2C)}$ = –3 mA, IOVDD > 2 V			0.4	V

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at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, BSTVDD = 3.3 V, HVDD = 11 V (for external HVDD case), f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 x f_S, TDM slave mode and PLL on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
$V_{OL2(I2C)}$	Low-level digital output voltage	SDA, $I_{OL(I2C)}$ = –2 mA, IOVDD [char_not_recognized] 2 V			0.2 x IOVDD	V
$I_{OL(I2C)}$	Low-level digital output current	SDA, $V_{OL(I2C)}$ = 0.4 V, standard-mode or fast-mode	3			mA
		SDA, $V_{OL(I2C)}$ = 0.4 V, fast-mode plus	20			
I_{IL}	Input logic-low leakage for digital inputs	All digital pins, input = 0 V	–5	0.1	5	µA
I_{IH}	Input logic-high leakage for digital inputs	All digital pins, input = IOVDD	–5	0.1	5	µA
C_{IN}	Input capacitance for digital inputs	All digital pins		5		pF
R_{PD}	Pulldown resistance for digital I/O pins when asserted on			20		kΩ
TYPICAL SUPPLY CURRENT CONSUMPTION						
I_{AVDD}	Current consumption in hardware shutdown mode	SHDNZ = 0, all device external clocks stopped		0.5		µA
I_{BSTVDD}, or I_{HVDD}				0.1		
I_{IOVDD}				0.1		
I_{AVDD}	Current consumption in sleep mode (software shutdown mode)	All device external clocks stopped		TBD		µA
I_{BSTVDD}, or I_{HVDD}				0.1		
I_{IOVDD}				0.1		
I_{AVDD}	Current consumption when MICBIAS ON, MICBIAS voltage 10 V, 30 mA load, ADC off	f_S = 48 kHz, BCLK = 256 [char_not_recognized] f_S		TBD		mA
I_{BSTVDD}				TBD		
I_{HVDD}				TBD		
I_{IOVDD}				0.01		
I_{AVDD}	Current consumption with ADC 2-channel operation at f_S 16-kHz, MICBIAS off, PLL on, BCLK = 512 [char_not_recognized] f_S			TBD		mA
I_{BSTVDD}, or I_{HVDD}				0		
I_{IOVDD}				0.1		
I_{AVDD}	Current consumption with ADC 2-channel operation at f_S 48-kHz, MICBIAS on, PLL off, BCLK = 512 [char_not_recognized] f_S			TBD		mA
I_{BSTVDD}, or I_{HVDD}				0		
I_{IOVDD}				0.1		
I_{AVDD}	Current consumption with DAC to HP 2-channel operation at f_S 16-kHz, MICBIAS off, PLL on, BCLK = 512 [char_not_recognized] f_S			TBD		mA
I_{BSTVDD}, or I_{HVDD}				0		
I_{IOVDD}				0.2		

at T_A = 25°C, AVDD = 3.3 V, IOVDD = 3.3 V, BSTVDD = 3.3 V, HVDD = 11 V (for external HVDD case), f_{IN} = 1-kHz sinusoidal signal, f_S = 48 kHz, 32-bit audio data, BCLK = 256 x f_S, TDM slave mode and PLL on (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
I_{AVDD}	Current consumption with DAC to HP 2-channel operation at f_S 48-kHz, MICBIAS off, PLL off, BCLK = 512 [char_not_recognized] f_S			TBD		mA
I_{BSTVDD}, or I_{HVDD}				0		
I_{IOVDD}				TBD		

(1) Ratio of output level with 1-kHz full-scale sine-wave input, to the output level with the AC signal input shorted to ground, measured A-weighted over a 20-Hz to 20-kHz bandwidth using an audio analyzer.
(2) All performance measurements done with 20-kHz low-pass filter and, where noted, A-weighted filter. Failure to use such a filter can result in higher THD and lower SNR and dynamic range readings than shown in the Electrical Characteristics. The low-pass filter removes out-of-band noise, which, although not audible, can affect dynamic specification values.

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5.8 Timing Requirements: I²C Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V (unless otherwise noted); see TBD for timing diagram

		MIN	NOM	MAX	UNIT
STANDARD-MODE					
f_{SCL}	SCL clock frequency	0		100	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	4			µs
t_{LOW}	Low period of the SCL clock	4.7			µs
t_{HIGH}	High period of the SCL clock	4			µs
$t_{SU;STA}$	Setup time for a repeated START condition	4.7			µs
$t_{HD;DAT}$	Data hold time	0		3.45	µs
$t_{SU;DAT}$	Data setup time	250			ns
t_r	SDA and SCL rise time			1000	ns
t_f	SDA and SCL fall time			300	ns
$t_{SU;STO}$	Setup time for STOP condition	4			µs
t_{BUF}	Bus free time between a STOP and START condition	4.7			µs
FAST-MODE					
f_{SCL}	SCL clock frequency	0		400	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.6			µs
t_{LOW}	Low period of the SCL clock	1.3			µs
t_{HIGH}	High period of the SCL clock	0.6			µs
$t_{SU;STA}$	Setup time for a repeated START condition	0.6			µs
$t_{HD;DAT}$	Data hold time	0		0.9	µs
$t_{SU;DAT}$	Data setup time	100			ns
t_r	SDA and SCL rise time	20		300	ns
t_f	SDA and SCL fall time	20 × (IOVDD / 5.5 V)		300	ns
$t_{SU;STO}$	Setup time for STOP condition	0.6			µs
t_{BUF}	Bus free time between a STOP and START condition	1.3			µs
FAST-MODE PLUS					
f_{SCL}	SCL clock frequency	0		1000	kHz
$t_{HD;STA}$	Hold time (repeated) START condition. After this period, the first clock pulse is generated.	0.26			µs
t_{LOW}	Low period of the SCL clock	0.5			µs
t_{HIGH}	High period of the SCL clock	0.26			µs
$t_{SU;STA}$	Setup time for a repeated START condition	0.26			µs
$t_{HD;DAT}$	Data hold time	0			µs
$t_{SU;DAT}$	Data setup time	50			ns
t_r	SDA and SCL Rise Time			120	ns
t_f	SDA and SCL Fall Time	20 × (IOVDD / 5.5 V)		120	ns
$t_{SU;STO}$	Setup time for STOP condition	0.26			µs
t_{BUF}	Bus free time between a STOP and START condition	0.5			µs

5.9 Switching Characteristics: I²C Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V (unless otherwise noted); seeTBD for timing diagram

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(SDA)}$	SCL to SDA delay	Standard-mode	200		1250	ns
		Fast-mode	200		850	ns
		Fast-mode plus			400	ns

5.10 Timing Requirements: TDM, I²S or LJ Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see for timing diagram

			MIN	NOM	MAX	UNIT
$t_{(BCLK)}$	BCLK period		40			ns
$t_{H(BCLK)}$	BCLK high pulse duration (1)		18			ns
$t_{L(BCLK)}$	BCLK low pulse duration (1)		18			ns
$t_{SU(FSYNC)}$	FSYNC setup time		8			ns
$t_{HLD(FSYNC)}$	FSYNC hold time		8			ns
$t_{r(BCLK)}$	BCLK rise time	10% - 90% rise time			10	ns
$t_{f(BCLK)}$	BCLK fall time	90% - 10% fall time			10	ns

(1) The BCLK minimum high or low pulse duration must be higher than 25 ns (to meet the timing specifications), if the SDOUT data line is latched on the opposite BCLK edge polarity than the edge used by the device to transmit SDOUT data.

5.11 Switching Characteristics: TDM, I²S or LJ Interface

at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see TBD for timing diagram

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{d(SDOUT-BCLK)}$	BCLK to SDOUT delay	50% of BCLK to 50% of SDOUT, IOVDD = 1.8 V			18	ns
		50% of BCLK to 50% of SDOUT, IOVDD = 3.3 V			14	
$t_{d(SDOUT-FSYNC)}$	FSYNC to SDOUT delay in TDM or LJ mode (for MSB data with TX_OFFSET = 0)	50% of FSYNC to 50% of SDOUT, IOVDD = 1.8 V			18	ns
		50% of FSYNC to 50% of SDOUT, IOVDD = 3.3 V			14	
$f_{(BCLK)}$	BCLK output clock frequency; master mode (1)				24.576	MHz
$t_{H(BCLK)}$	BCLK high pulse duration; master mode	IOVDD = 1.8 V	14			ns
		IOVDD = 3.3 V	14			
$t_{L(BCLK)}$	BCLK low pulse duration; master mode	IOVDD = 1.8 V	14			ns
		IOVDD = 3.3 V	14			
$t_{d(FSYNC)}$	BCLK to FSYNC delay; master mode	50% of BCLK to 50% of FSYNC, IOVDD = 1.8 V			18	ns
		50% of BCLK to 50% of FSYNC, IOVDD = 3.3 V			14	
$t_{r(BCLK)}$	BCLK rise time; master mode	10% - 90% rise time, IOVDD = 1.8 V			10	ns
		10% - 90% rise time, IOVDD = 3.3 V			10	

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at T_A = 25°C, IOVDD = 3.3 V or 1.8 V and 20-pF load on all outputs (unless otherwise noted); see TBD for timing diagram

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{f(BCLK)}$	BCLK fall time; master mode	90% - 10% fall time, IOVDD = 1.8 V			8	ns
		90% - 10% fall time, IOVDD = 3.3 V			8	

(1) The BCLK output clock frequency must be lower than 18.5 MHz (to meet the timing specifications), if the SDOUT data line is latched on the opposite BCLK edge polarity than the edge used by the device to transmit SDOUT data.

6 Detailed Description

6.1 Overview

The TAC5312-Q1 is from a scalable TAC5x1x-Q1 family of devices. As with the extended family of devices, the TAC5312-Q1 consists of a high-performance, low-power, flexible, mono/stereo, audio analog-to-digital converter (ADC) and audio digital-to-analog converter (DAC) with extensive feature integration. This device is intended for automotive applications such as telematics control unit, hands-free in-vehicle communication, emergency call, and multimedia applications. The high dynamic range of this device enables far-field audio recording with high fidelity. This device integrates a host of features that reduce cost, board space, and power consumption in space-constrained automotive sub-system designs. Package, performance, and device-compatible configuration registers make this device well suited for scalable system designs.

The TAC5312-Q1 consists of the following blocks:

- 2-channel, multibit, high-performance delta-sigma (ΔΣ) ADCs
- Configurable single-ended or differential audio inputs with high voltage signal swing
- High-voltage, Low-noise programmable microphone bias output
- Highly flexible, comprehensive input fault diagnostic
- 2-channel, multibit, high-performance delta-sigma (ΔΣ) DACs
- Configurable single-ended, differential or pseudo-differential audio outputs
- Over Current Diagnostics and Protection for MICBIAS and analog outputs
- Automatic gain controller (AGC)
- Advanced Thermal foldback and protection
- Advanced Battery guard and distortion limiter
- Programmable decimation filters with linear-phase or low-latency filter
- Programmable channel gain, volume control, and biquad filters for each channel
- Programmable phase and gain calibration with fine resolution for each channel
- Programmable high-pass filter (HPF) and digital channel mixer
- Pulse density modulation (PDM) digital microphone interface(only available in 5x5mm Package) with high-performance decimation filter
- Integrated low-jitter, phase-locked loop (PLL) supporting a wide range of system clocks
- Integrated digital and analog voltage regulators to support single-supply operation

Communication to the TAC5312-Q1 for configuring the control registers is supported using an I^2C interface. The device supports a highly flexible audio serial interface [time-division multiplexing (TDM), I^2S, or left-justified (LJ)] to transmit audio data seamlessly in the system across devices.

6.2 Functional Block Diagram

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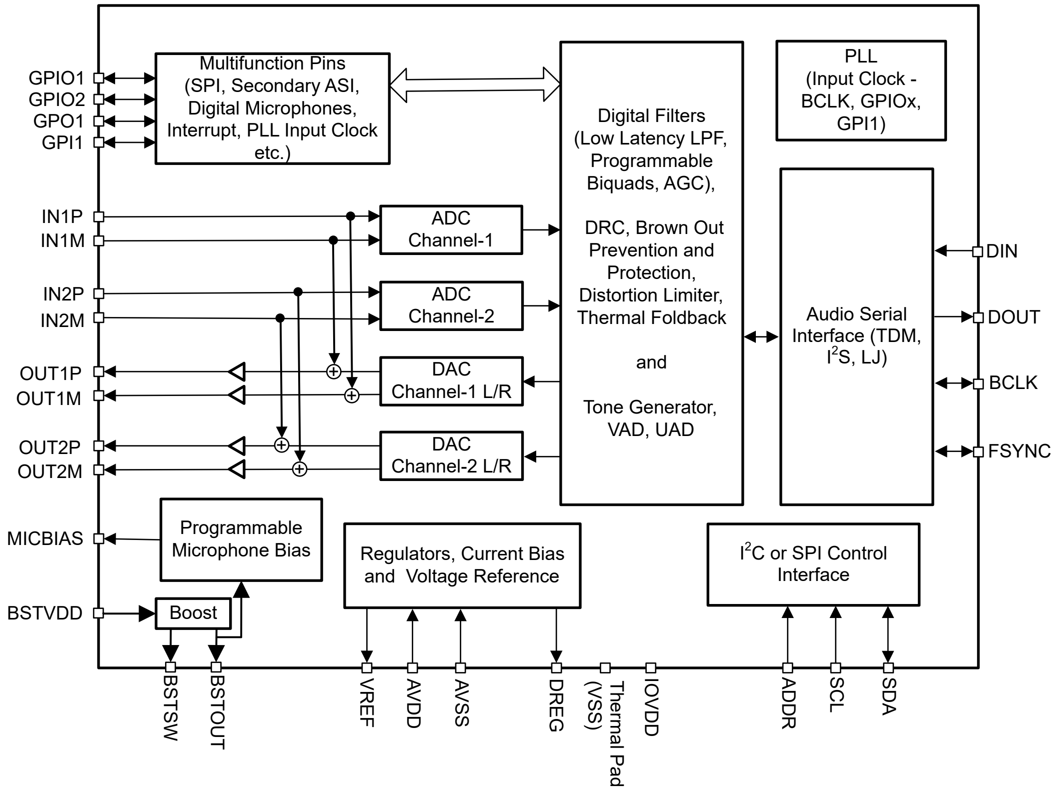

図 6-1. Functional Block Diagram

6.3 Feature Description

6.3.1 Serial Interfaces

This device has two serial interfaces: control and audio data. The control serial interface is used for device configuration. The audio data serial interface is used for transmitting audio data to the host device.

6.3.1.1 Control Serial Interfaces

The device contains configuration registers and programmable coefficients that can be set to the desired values for a specific system and application use. All these registers can be accessed using either I^{2}C or SPI communication to the device. For more information, see the *セクション 7* section.

6.3.1.2 Audio Serial Interfaces

Digital audio data flows between the host processor and the TAC5312-Q1 on the digital audio serial interface (ASI), or audio bus. This highly flexible ASI bus includes a TDM mode for multichannel operation, support for I^{2}S or left-justified protocols format, programmable data length options, very flexible controller-target configurability for bus clock lines, and the ability to communicate with multiple devices within a system directly.

The TAC5312-Q1 supports up to two ASI Interfaces. Secondary ASI Clock and Data Pins can be configured by setting GPIO's. Frame Sync of two ASI's must be synchronous.

The bus protocol TDM, I^2S, or left-justified (LJ) format can be selected for primary ASI by using the PASI_FORMAT[1:0], P0_R26_D[7:6] register bits. As shown in 表 6-1 and.表 6-2, these modes are all most significant byte (MSB)-first, pulse code modulation (PCM) data format, with the output channel data word-length programmable as 16, 20, 24, or 32 bits by configuring the PASI_WLEN[1:0], P0_R26_D[5:4] register bits.

表 6-1. Primary Audio Serial Interface Format

P0_R26_D[7:6] : PASI_FORMAT[1:0]	PRIMARY AUDIO SERIAL INTERFACE FORMAT
00 (default)	Time division multiplexing (TDM) mode
01	Inter IC sound (I^2S) mode
10	Left-justified (LJ) mode
11	Reserved (do not use this setting)

表 6-2. Primary Audio Serial Interface Data Word-Length

P0_R7_D[5:4] : PASI_WLEN[1:0]	PRIMARY AUDIO OUTPUT CHANNEL DATA WORD-LENGTH
00	Data word-length set to 16 bits
01	Data word-length set to 20 bits
10	Data word-length set to 24 bits
11 (default)	Data word-length set to 32 bits

The frame sync pin, FSYNC, is used in this audio bus protocol to define the beginning of a frame and has the same frequency as the output data sample rates. The bit clock pin, BCLK, is used to clock out the digital audio data across the serial bus. The number of bit-clock cycles in a frame must accommodate multiple device active output channels with the programmed data word length.

A frame consists of multiple time-division channel slots (up to 32) to allow all input/output channel audio data transmissions to be completed on the audio bus by a device or multiple devices sharing the same audio bus. The device supports up to eight input channels and eight output channels that can be configured on the primary ASI bus to place their audio data on bus slot 0 to slot 31. 表 6-3 lists the output channel-1 slot configuration settings. In I^2S and LJ mode, the slots are divided into two sets, left-channel slots, and right-channel slots, as described in the *セクション 6.3.1.2.2* and *セクション 6.3.1.2.3* sections.

表 6-3. Output Channel-1 Slot Assignment Settings

P0_R30_D[4:0] : PASI_TX_CH1_SLOT[4:0]	OUTPUT CHANNEL 1 SLOT ASSIGNMENT
0 0000 = 0d (default)	Slot 0 for TDM or left slot 0 for I^2S, LJ.
0 0001 = 1d	Slot 1 for TDM or left slot 1 for LJ.
…	…
0 1111 = 15d	Slot 15 for TDM or left slot 15 for LJ.
1 0000 = 32d	Slot 16 for TDM or right slot 0 for I^2S, LJ.
…	…
1 1110 = 30d	Slot 30 for TDM or right slot 14 for LJ.
1 1111 = 31d	Slot 31 for TDM or right slot 15 for LJ.

Similarly, the slot assignment setting for output channel 2 to channel 8 can be done using the PASI_TX_CH2_SLOT (P0_R31) to PASI_TX_CH8_SLOT (P0_R37) registers and for input channel 1 to channel 8 by using the PASI_RX_CH1_SLOT(P0_R40) to PAS_RX_CH8_SLOT(P0_R47), respectively.

The slot word length is the same as the primary ASI channel word length set for the device. The output channel data word length must be set to the same value for all TAC5312-Q1 devices if all devices share the same ASI bus in a system. The maximum number of slots possible for the ASI bus in a system is limited by the available bus bandwidth, which depends upon the BCLK frequency, output data sample rate used, and the channel data word length configured.

The device also includes a feature that offsets the start of the slot data transfer concerning the frame sync by up to 31 cycles of the bit clock. Offset can be configured independently for input and output data paths. 表 6-4 and 表 6-5lists the programmable offset configuration settings for transmission and receive paths respectively.

表 6-4. Programmable Offset Settings for the ASI Slot Start for transmission

P0_R28_D[4:0] : PASI_TX_OFFSET[4:0]	PROGRAMMABLE OFFSET SETTING FOR SLOT DATA TRANSMISSION START
0 0000 = 0d (default)	The device follows the standard protocol timing without any offset.
0 0001 = 1d	Slot start is offset by one BCLK cycle, as compared to standard protocol timing. For I^2S or LJ, the left and right slot start is offset by one BCLK cycle, as compared to standard protocol timing.
......	......
1 1110 = 30d	Slot start is offset by 30 BCLK cycles, as compared to standard protocol timing. For I^2S or LJ, the left and right slot start is offset by 30 BCLK cycles, as compared to standard protocol timing.
1 1111 = 31d	Slot start is offset by 31 BCLK cycles, as compared to standard protocol timing. For I^2S or LJ, the left and right slot start is offset by 31 BCLK cycles, as compared to standard protocol timing.

表 6-5. Programmable Offset Settings for the ASI Slot Start for Receive

P0_R38_D[4:0] : PASI_RX_OFFSET[4:0]	PROGRAMMABLE OFFSET SETTING FOR SLOT DATA RECEIVE START
0 0000 = 0d (default)	The device follows the standard protocol timing without any offset.
0 0001 = 1d	Slot start is offset by one BCLK cycle, as compared to standard protocol timing. For I^2S or LJ, the left and right slot start is offset by one BCLK cycle, as compared to standard protocol timing.
......	......
1 1110 = 30d	Slot start is offset by 30 BCLK cycles, as compared to standard protocol timing. For I^2S or LJ, the left and right slot start is offset by 30 BCLK cycles, as compared to standard protocol timing.
1 1111 = 31d	Slot start is offset by 31 BCLK cycles, as compared to standard protocol timing. For I^2S or LJ, the left and right slot start is offset by 31 BCLK cycles, as compared to standard protocol timing.

The device also features the ability to invert the polarity of the frame sync pin, FSYNC, used to transfer the audio data as compared to the default FSYNC polarity used in standard protocol timing. This feature can be set using the PASI_FSYNC_POL, P0_R26_D3 register bit. Similarly, the device can invert the polarity of the bit clock pin, BCLK, which can be set using the PASI_BCLK_POL, P0_R26_D2 register bit.

In addition, the word clock and bit clock can be independently configured in either Controller or Target mode, for flexible connectivity to a wide variety of processors. The word clock is used to define the beginning of a frame and may be programmed as either a pulse or a square-wave signal. The frequency of this clock corresponds to the maximum of the selected ADC sampling frequencies.

6.3.1.2.1 Time Division Multiplexed Audio (TDM) Interface

In TDM mode, also known as DSP mode, the rising edge of FSYNC starts the data transfer with the slot 0 data first. Immediately after the slot 0 data transmission, the remaining slot data are transmitted in order. FSYNC and each data bit (except the MSB of slot 0 when TX_OFFSET equals 0) is transmitted on the rising edge of BCLK. 図 6-2 to 図 6-5 illustrate the protocol timing for TDM operation with various configurations.

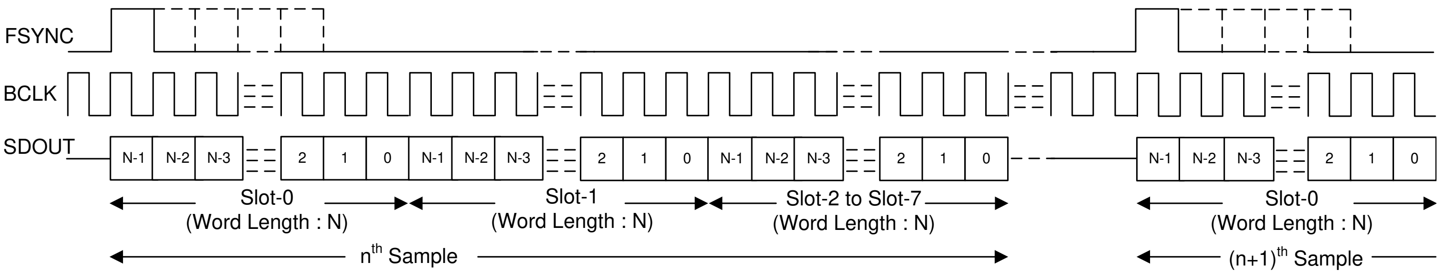

図 6-2. TDM Mode Standard Protocol Timing (PASI_TX_OFFSET = 0)

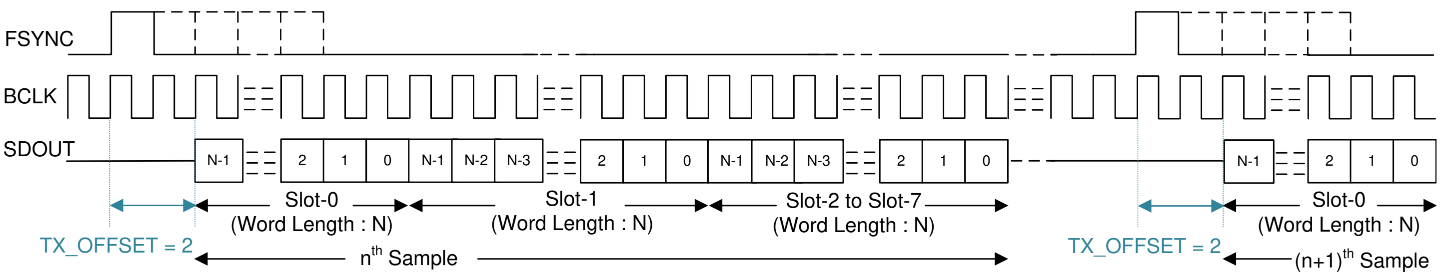

図 6-3. TDM Mode Protocol Timing (PASI_TX_OFFSET = 2)

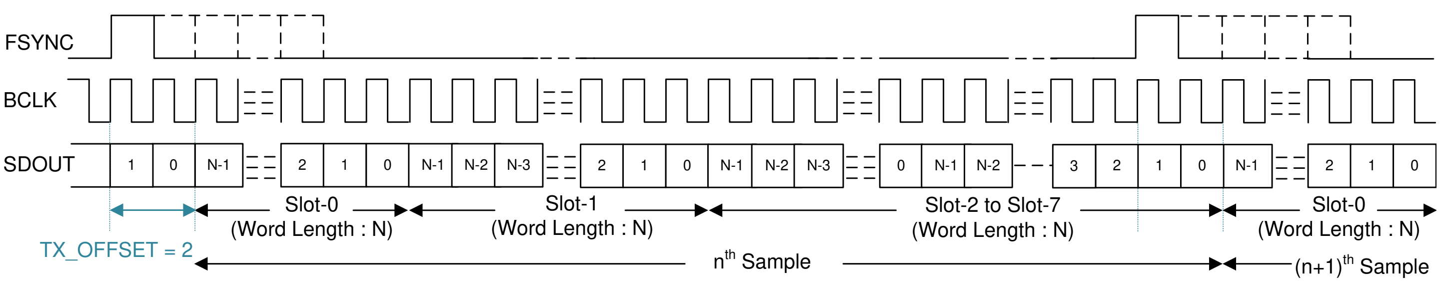

図 6-4. TDM Mode Protocol Timing (No Idle BCLK Cycles, PASI_TX_OFFSET = 2)

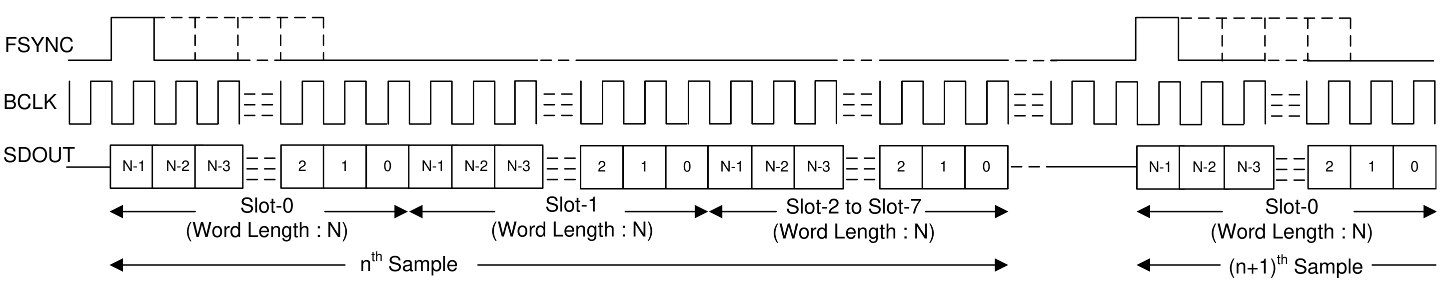

図 6-5. TDM Mode Protocol Timing (PASI_TX_OFFSET = 0 and PASI_BCLK_POL = 1)

For proper operation of the audio bus in TDM mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels times the programmed word length of the output channel data. The device supports FSYNC as a pulse with a 1-cycle-wide bit clock, but also supports multiples as well. For a higher BCLK frequency operation, using TDM mode with a PASI_TX_OFFSET value higher than 0 is recommended.

6.3.1.2.2 Inter IC Sound (I^2S) Interface

The standard I^2S protocol is defined for only two channels: left and right. The device extends the same protocol timing for multichannel operation. In I^2S mode, the MSB of the left slot 0 is transmitted on the falling edge of BCLK in the second cycle after the *falling* edge of FSYNC. Immediately after the left slot 0 data transmission, the

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remaining left slot data are transmitted in order. The MSB of the right slot 0 is transmitted on the falling edge of BCLK in the second cycle after the *rising* edge of FSYNC. Immediately after the right slot 0 data transmission, the remaining right slot data are transmitted in order. FSYNC and each data bit is transmitted on the falling edge of BCLK. 図 6-6 to 図 6-9 illustrate the protocol timing for I²S operation with various configurations.

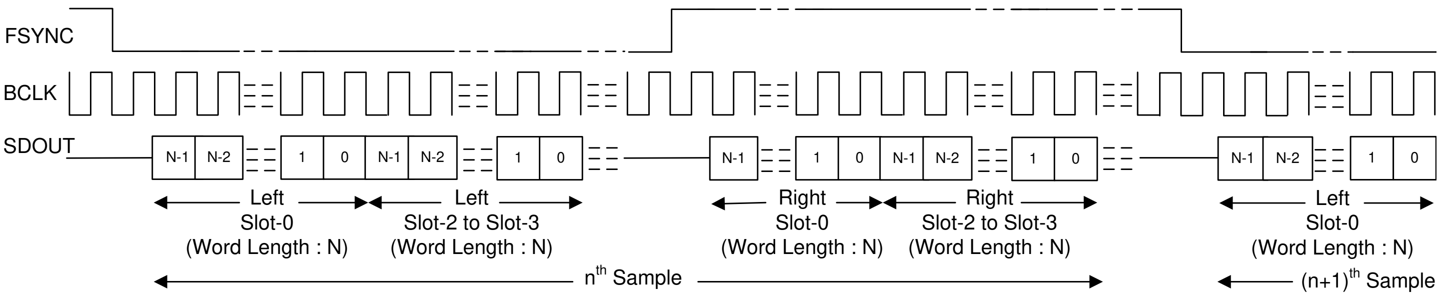

図 6-6. I²S Mode Standard Protocol Timing (PASI_TX_OFFSET = 0)

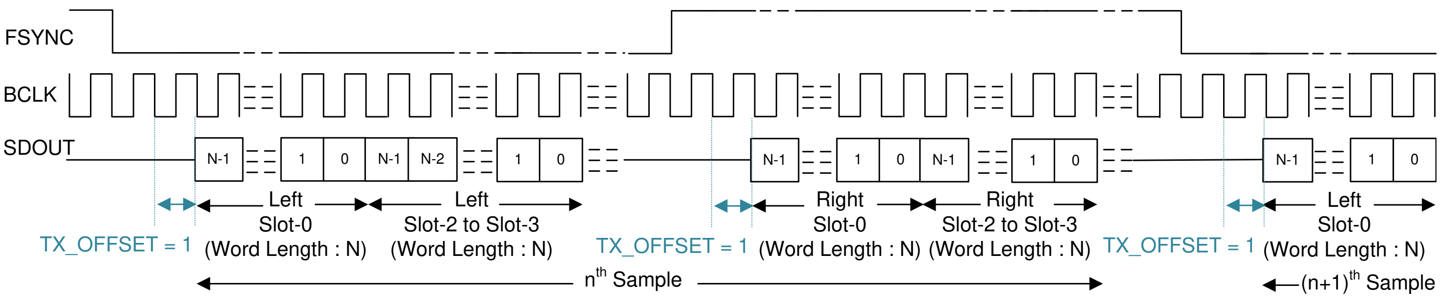

図 6-7. I²S Protocol Timing (PASI_TX_OFFSET = 1)

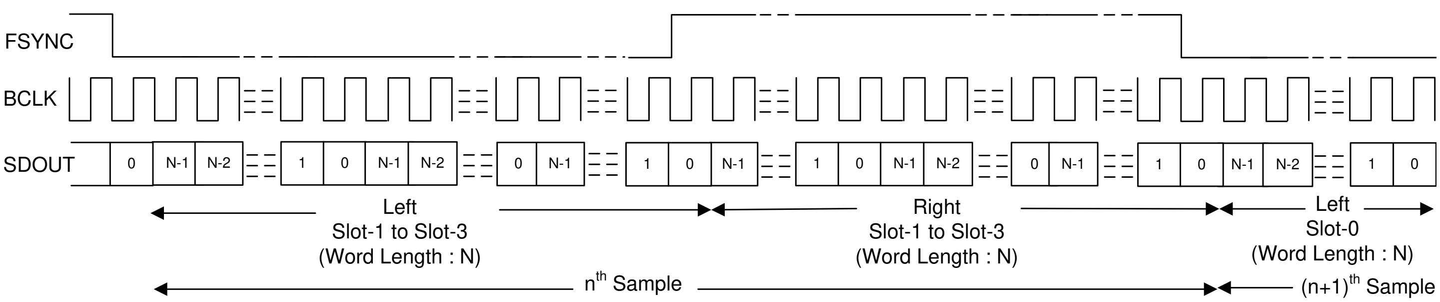

図 6-8. I²S Protocol Timing (No Idle BCLK Cycles, PASI_TX_OFFSET = 0)

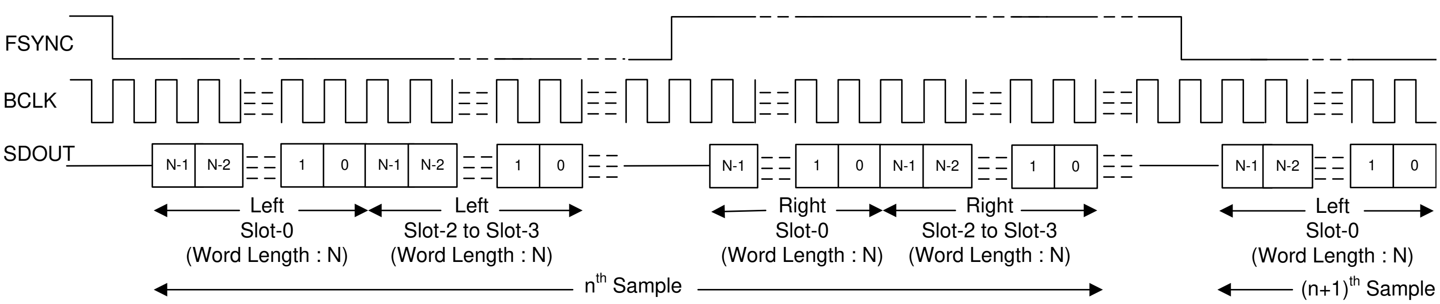

図 6-9. I²S Protocol Timing (PASI_TX_OFFSET = 0 and PASI_BCLK_POL = 1)

For proper operation of the audio bus in I²S mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels (including left and right slots) times the programmed word length of the output channel data. The device FSYNC low pulse must be a number of BCLK cycles wide that is greater than or equal to the number of active left slots times the data word length configured. Similarly, the FSYNC high pulse must be a number of BCLK cycles wide that is greater than or equal to the number of active right slots times the data word length configured.

6.3.1.2.3 Left-Justified (LJ) Interface

The standard LJ protocol is defined for only two channels: left and right. The device extends the same protocol timing for multichannel operation. In LJ mode, the MSB of the left slot 0 is transmitted in the same BCLK cycle after the *rising* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK. Immediately after the left slot 0 data transmission, the remaining left slot data are transmitted in order. The MSB of the right slot 0 is transmitted in the same BCLK cycle after the *falling* edge of FSYNC. Each subsequent data bit is transmitted on the falling edge of BCLK. Immediately after the right slot 0 data transmission, the remaining right slot data are transmitted in order. FSYNC is transmitted on the falling edge of BCLK. 図 6-10 to 図 6-13 illustrate the protocol timing for LJ operation with various configurations.

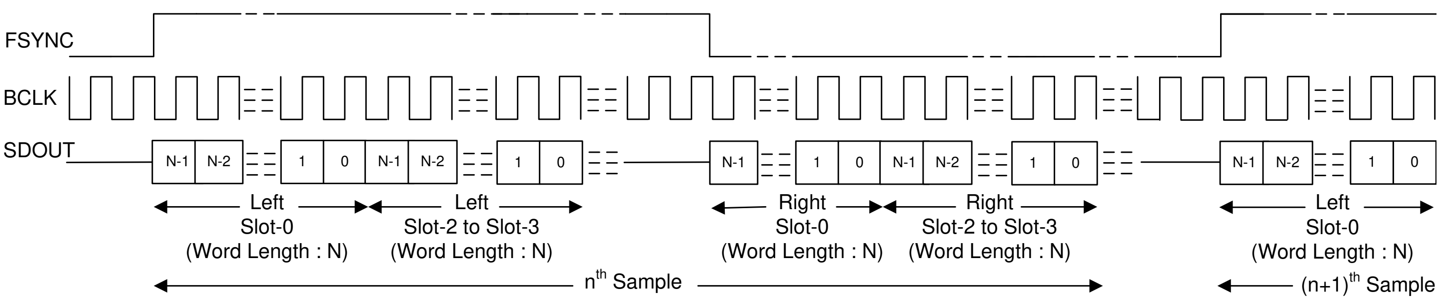

図 6-10. LJ Mode Standard Protocol Timing (TX_OFFSET = 0)

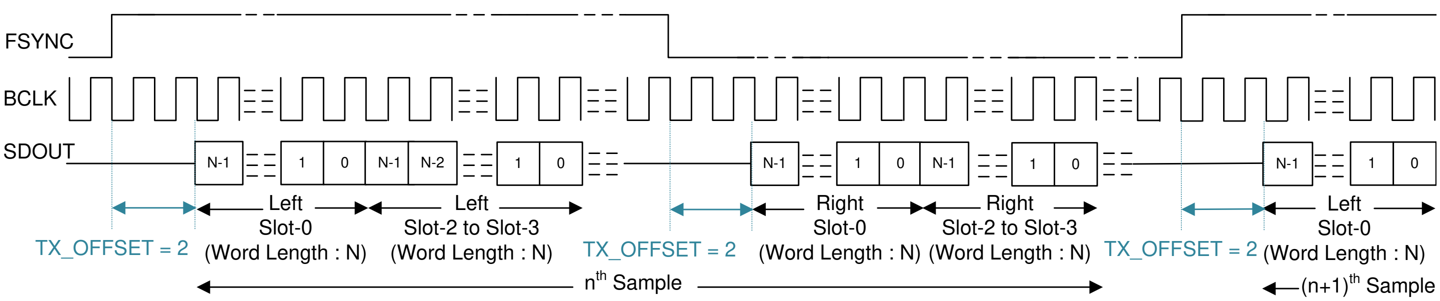

図 6-11. LJ Protocol Timing (TX_OFFSET = 2)

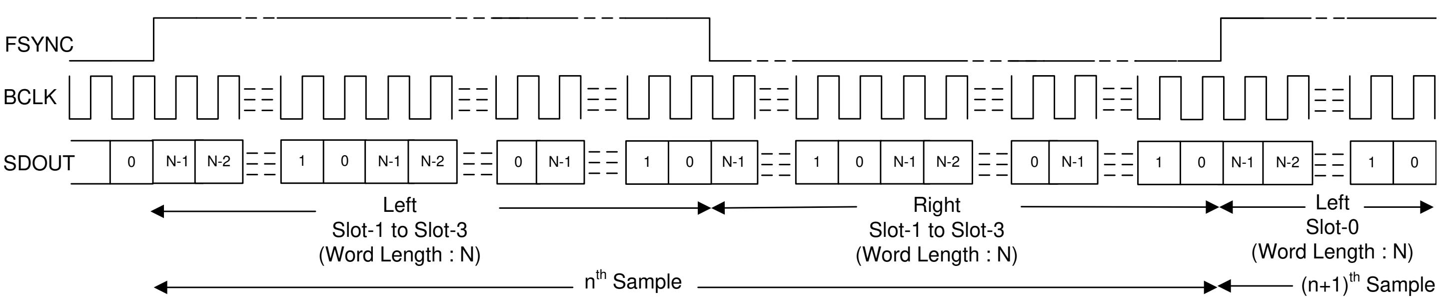

図 6-12. LJ Protocol Timing (No Idle BCLK Cycles, TX_OFFSET = 0)

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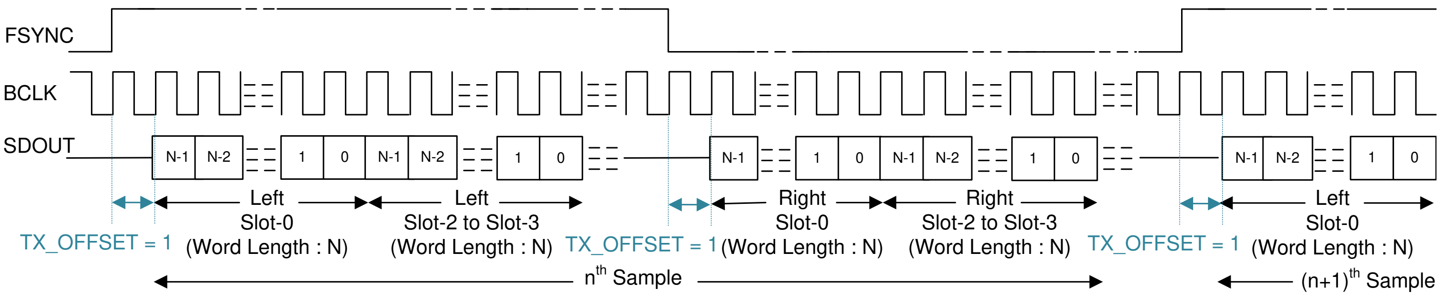

図 6-13. LJ Protocol Timing (TX_OFFSET = 1 and BCLK_POL = 1)

For proper operation of the audio bus in LJ mode, the number of bit clocks per frame must be greater than or equal to the number of active output channels (including left and right slots) times the programmed word length of the output channel data. The device FSYNC high pulse must be a number of BCLK cycles wide that is greater than or equal to the number of active left slots times the data word length configured. Similarly, the FSYNC low pulse must be number of BCLK cycles wide that is greater than or equal to the number of active right slots times the data word length configured. For a higher BCLK frequency operation, using LJ mode with a TX_OFFSET value higher than 0 is recommended.

6.3.2 Using Multiple Devices With Shared Buses

The device has many supported features and flexible options that can be used in the system to seamlessly connect multiple TAC5312-Q1 devices by sharing a single common I^{2}C or SPI control bus and an audio serial interface bus. This architecture enables multiple applications to be applied to a system that require a microphone or speaker array for beam-forming operation, audio conferencing, noise cancellation, and so forth. 図 6-14 shows a diagram of multiple TAC5312-Q1 devices in a configuration where the control and audio data buses are shared.

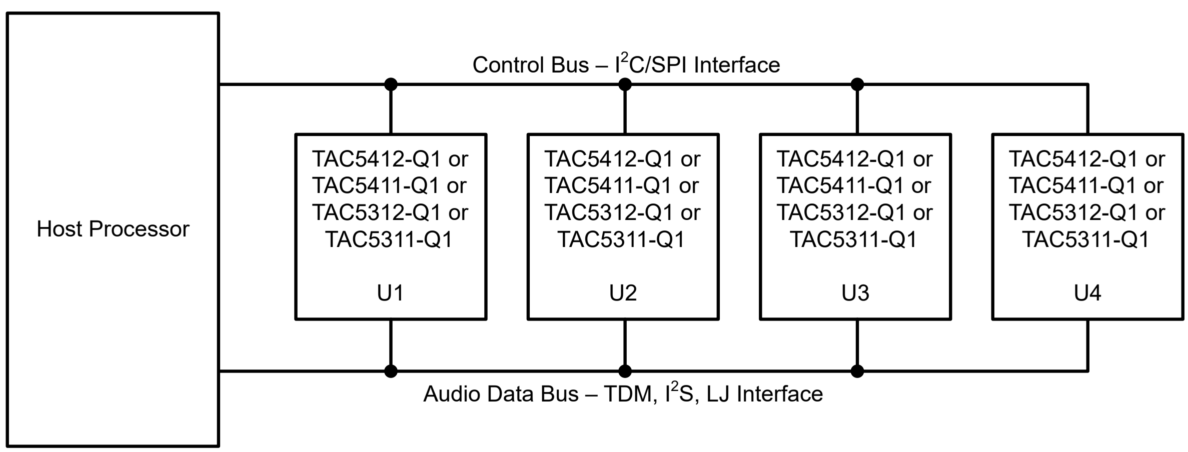

図 6-14. Multiple TAC5312-Q1 Devices With Shared Control and Audio Data Buses

The TAC5312-Q1 consists of the following features to enable seamless connection and interaction of multiple devices using a shared bus:

- Supports up to four pin-programmable I^{2}C target addresses
- I^{2}C broadcast simultaneously writes to (or triggers) all TAC5312-Q1 devices
- Supports up to 32 configuration input/output channel slots for the audio serial interface
- Tri-state feature (with enable and disable) for the unused audio data slots of the device
- Supports a bus-holder feature (with enable and disable) to keep the last driven value on the audio bus
- The GPIOx, GPI1 or GPO1 pin can be configured as a secondary input/output data lane or as a secondary audio serial interface

- The GPIOx, GPI1 or GPO1 pin can be used in a daisy-chain configuration of multiple TAC5312-Q1 devices
- Supports one BCLK cycle data latching timing to relax the timing requirement for the high-speed interface
- Programmable controller and target options for both primary and secondary audio serial interface
- Ability to synchronize the multiple devices for the simultaneous sampling requirement across devices

See the *Multiple TAC5x1x Devices With a Shared TDM and I²C/SPI Bus* application report for further details.

6.3.3 Phase-Locked Loop (PLL) and Clock Generation

The device has a smart auto-configuration block to generate all necessary internal clocks required for the ADC modulator and the digital filter engine used for signal processing. This configuration is done by monitoring the frequency of the FSYNC and BCLK signal on the audio buses.

The device supports the various data sample rates (of the FSYNC signal frequency) and the BCLK to FSYNC ratio to configure all clock dividers, including the PLL configuration, internally without host programming. 表 6-6 and 表 6-7 list the supported FSYNC and BCLK frequencies.

表 6-6. Supported FSYNC (Multiples or Submultiples of 48kHz) and BCLK Frequencies

BCLK TO FSYNC RATIO	BCLK (MHz)								
	FSYNC (8 kHz)	FSYNC (16 kHz)	FSYNC (24 kHz)	FSYNC (32 kHz)	FSYNC (48 kHz)	FSYNC (96 kHz)	FSYNC (192 kHz)	FSYNC (384 kHz)	FSYNC (768 kHz)
16	**Reserved**	0.256	0.384	0.512	0.768	1.536	3.072	6.144	12.288
24	**Reserved**	0.384	0.576	0.768	1.152	2.304	4.608	9.216	18.432
32	0.256	0.512	0.768	1.024	1.536	3.072	6.144	12.288	24.576
48	0.384	0.768	1.152	1.536	2.304	4.608	9.216	18.432	**Reserved**
64	0.512	1.024	1.536	2.048	3.072	6.144	12.288	24.576	**Reserved**
96	0.768	1.536	2.304	3.072	4.608	9.216	18.432	**Reserved**	**Reserved**
128	1.024	2.048	3.072	4.096	6.144	12.288	24.576	**Reserved**	**Reserved**
192	1.536	3.072	4.608	6.144	9.216	18.432	**Reserved**	**Reserved**	**Reserved**
256	2.048	4.096	6.144	8.192	12.288	24.576	**Reserved**	**Reserved**	**Reserved**
384	3.072	6.144	9.216	12.288	18.432	**Reserved**	**Reserved**	**Reserved**	**Reserved**
512	4.096	8.192	12.288	16.384	24.576	**Reserved**	**Reserved**	**Reserved**	**Reserved**
1024	8.192	16.384	24.576	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**
2048	16.384	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**

表 6-7. Supported FSYNC (Multiples or Submultiples of 44.1kHz) and BCLK Frequencies

BCLK TO FSYNC RATIO	BCLK (MHz)								
	FSYNC (7.35 kHz)	FSYNC (14.7 kHz)	FSYNC (22.05 kHz)	FSYNC (29.4 kHz)	FSYNC (44.1 kHz)	FSYNC (88.2 kHz)	FSYNC (176.4 kHz)	FSYNC (352.8 kHz)	FSYNC (705.6 kHz)
16	**Reserved**	**Reserved**	0.3528	0.4704	0.7056	1.4112	2.8224	5.6448	11.2896
24	**Reserved**	0.3528	0.5292	0.7056	1.0584	2.1168	4.2336	8.4672	16.9344
32	**Reserved**	0.4704	0.7056	0.9408	1.4112	2.8224	5.6448	11.2896	22.5792
48	0.3528	0.7056	1.0584	1.4112	2.1168	4.2336	8.4672	16.9344	**Reserved**
64	0.4704	0.9408	1.4112	1.8816	2.8224	5.6448	11.2896	22.5792	**Reserved**
96	0.7056	1.4112	2.1168	2.8224	4.2336	8.4672	16.9344	**Reserved**	**Reserved**
128	0.9408	1.8816	2.8224	3.7632	5.6448	11.2896	22.5792	**Reserved**	**Reserved**
192	1.4112	2.8224	4.2336	5.6448	8.4672	16.9344	**Reserved**	**Reserved**	**Reserved**
256	1.8816	3.7632	5.6448	7.5264	11.2896	22.5792	**Reserved**	**Reserved**	**Reserved**
384	2.8224	5.6448	8.4672	11.2896	16.9344	**Reserved**	**Reserved**	**Reserved**	**Reserved**
512	3.7632	7.5264	11.2896	15.0528	22.5792	**Reserved**	**Reserved**	**Reserved**	**Reserved**
1024	7.5264	15.0528	22.5792	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**

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表 6-7. Supported FSYNC (Multiples or Submultiples of 44.1kHz) and BCLK Frequencies (続き)

BCLK TO FSYNC RATIO	BCLK (MHz)								
	FSYNC (7.35 kHz)	FSYNC (14.7 kHz)	FSYNC (22.05 kHz)	FSYNC (29.4 kHz)	FSYNC (44.1 kHz)	FSYNC (88.2 kHz)	FSYNC (176.4 kHz)	FSYNC (352.8 kHz)	FSYNC (705.6 kHz)
2048	15.0528	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**	**Reserved**

The TAC5312-Q1 also supports non-Audio sample rates beyond those listed in prior tables. Refer to Configuring Non-Audio Sample Rates for TAC5x1x devices for more details.

The TAC5312-Q1 sample rate can be configured using registers CLK_DET0 (P0_R62) and CLK_DET1 (P0_R63) for primary and secondary ASI respectively. These registers also capture the device auto detect result for the FSYNC frequency in auto detection mode. The registers CLK_DET2 (P0_R64) and CLK_DET3 (P0_R65) capture the BCLK to FSYNC ratio detected by the device. If the device finds any unsupported combinations of FSYNC frequency and BCLK to FSYNC ratios, the device generates an ASI clock-error interrupt and mutes all the channels accordingly.

The TAC5312-Q1 also supports enabling channels while some ADC channels are already in operation. This requires a pre-configuration before power to describe the maximum number of channels that can be enabled while in operation to ensure proper clock generation and use. This can be configured by using register DYN_PUPD_CFG (P0_R119). ADC_DYN_PUPD_EN bit can be used to enable ADC channel's dynamic power up. The number of channels can be configured using ADC_DYN_MAXCH_SEL bit.

The device uses an integrated, low-jitter, phase-locked loop (PLL) to generate internal clocks required for the modulators and digital filter engine, as well as other control blocks. The device also supports an option to use BCLK, GPIOx, or the GPI1 pin (as CCLK) as the audio clock source without using the PLL to reduce power consumption. However, the ADC performance may degrade based on jitter from the external clock source, and some processing features may not be supported if the external audio clock source frequency is not high enough. Therefore, TI recommends using the PLL for high-performance applications. More details and information on how to configure and use the device in low-power mode without using the PLL are discussed in the *TAC5x1x Power Consumption Matrix Across Various Usage Scenarios* application report.

The device also supports an audio bus controller mode operation using the GPIOx or GPI1 pin (as CCLK) as the reference input clock source and supports various flexible options and a wide variety of system clocks. More details and information on controller mode configuration and operation are discussed in the *Configuring and Operating TAC5x1x as an Audio Bus Controller* application report.

The audio bus clock error detection and auto-detect feature automatically generates all internal clocks, but can be disabled using the IGNORE_CLK_ERR (P0_R4_D6) and CUSTOM_CLK_CFG (P0_R50_D0) register bits, respectively. In the system, this disable feature can be used to support custom clock frequencies that are not covered by the auto detect scheme. For such application use cases, care must be taken to ensure that the multiple clock dividers are all configured appropriately. Therefore, TI recommends using the PPC3 GUI for device configuration settings; for more details see the *TAC5212EVM-PDK Evaluation module* user's guide and the PurePath™ console graphical development suite.

6.3.4 Input Channel Configuration

The TAC5312-Q1 consists of two pairs of analog input pins (INxP and INxM) that can be configured as either differential or single-ended inputs for the recording channel. The device supports simultaneous recording of up to two channels using the multichannel ADC. The input source for the analog pins can be either analog microphones or line, aux inputs from the system board. 表 6-8 describes how to set the input configuration for the record channel.

表 6-8. Input Source Selection for the Record Channel

P0_R80_D[7:6] : ADC_CH1_INSRC[1:0]	INPUT CHANNEL 1 RECORD SOURCE SELECTION
00 (default)	Analog differential input for channel 1
01	Analog single-ended input for channel 1

表 6-8. Input Source Selection for the Record Channel (続き)

P0_R80_D[7:6] : ADC_CH1_INSRC[1:0]	INPUT CHANNEL 1 RECORD SOURCE SELECTION
10 or 11	Reserved (do not use this setting)

Similarly, the input source selection setting for input channel 2 can be configured using the ADC_CH2_INSRC[1:0] (P0_R85_D[7:6]) register bits.

The device supports the input DC fault diagnostic feature for microphone recording with the DC-coupled inputs configuration; however, the device also supports an option for AC-coupled inputs if the DC diagnostic is not required for the specific input pins.

For the DC-coupled line input configuration, the DC common-mode difference (INxP – INxM) for the analog input pins must be 0V to support the 10-V_{RMS} full-scale differential input. For the DC-coupled microphone input configuration, the DC common-mode difference (INxP – INxM) for the analog input pins must be within 3.4V to 6.0V to support the 2-V_{RMS} full-scale differential input in the default mode of operation. The DC differential common-mode voltage is later filtered out by the digital high-pass filter and the digital output full-scale corresponds to the 10V_{RMS} AC signal in this case.

図 6-15 and 図 6-16 show how to connect a DC-coupled microphone for a differential and single-ended input, respectively. The value of the external bias resistor, R1, must be appropriately chosen based upon the microphone impedance. For a differential input, the value of the external bias resistor is recommended to be used for half of the microphone impedance, whereas for a single-ended input, the external bias resistor is recommended to be the same as the microphone impedance.

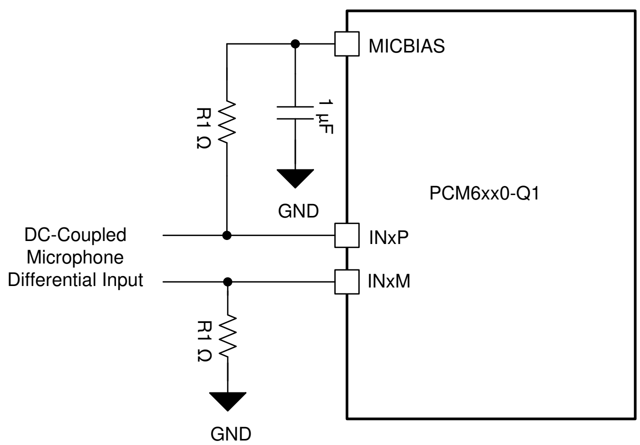

図 6-15. DC-Coupled Microphone Differential Input Connection

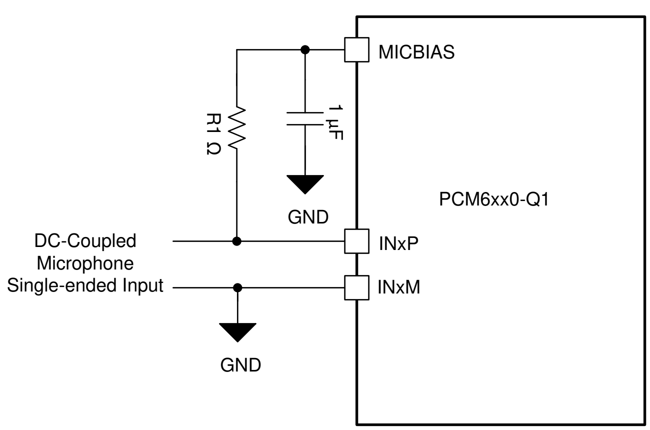

図 6-16. DC-Coupled Microphone Single-Ended Input Connection

In AC-coupled mode, the value of the coupling capacitor must be so chosen that the high-pass filter formed by the coupling capacitor and the input impedance do not affect the signal content. At power-up, before proper recording can begin, this coupling capacitor must be charged up to the common-mode voltage. For single-ended input configuration, the INxM pin must be grounded after the AC coupling capacitor in AC-coupled mode.

図 6-17 and 図 6-18 show how to connect an AC-coupled microphone or line source for a differential and single-ended input, respectively. In AC-coupled mode, the device input pins INxP and INxM, must be biased appropriately for the DC common-mode value either using the on-chip MICBIAS output voltage along with external bias resistor, R0, or using an external bias generator circuit. The maximum value for resistor R0 depends upon the signal swing and the MICBIAS value programmed. See the *TAC5xxx-Q1 AC Coupled External Resistor Calculator* to calculate the R0 value for the desired system configuration.

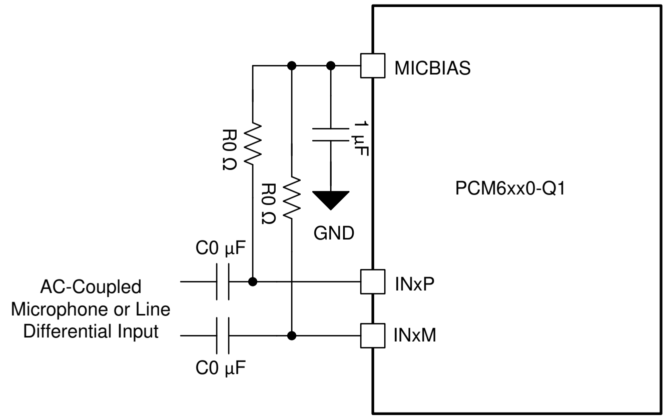

図 6-17. AC-Coupled Microphone or Line Differential Input Connection

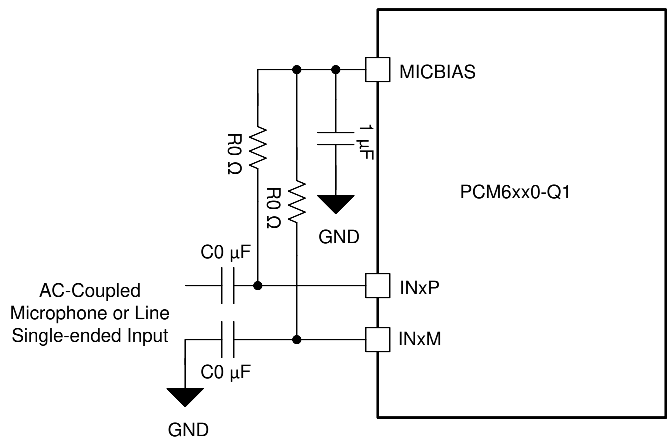

図 6-18. AC-Coupled Microphone or Line Single-Ended Input Connection

6.3.5 Reference Voltage

All audio data converters require a DC reference voltage. The TAC5312-Q1 achieves its low-noise performance by internally generating a low-noise reference voltage. This reference voltage is generated using a band-gap circuit with good PSRR performance. This audio converter reference voltage must be filtered externally using a minimum 1µF capacitor connected from the VREF pin to the analog ground (VSS).

To achieve low power consumption, this audio reference block is powered down in sleep mode or software shutdown. When exiting sleep mode, the audio reference block should be powered up by setting SLEEP_EXIT_VREF_EN(P0_R2_D3) to 1'b1. An internal fast-charge scheme helps the VREF pin to settle to its steady-state voltage faster (a function of the decoupling capacitor on the VREF pin). This time is approximately equal to 3.5ms when using a 1µF decoupling capacitor. If a higher value of the decoupling capacitor is used on the VREF pin, the fast-charge setting must be reconfigured using the VREF_QCHG, P0_R2_D[5:4] register bits, which support options of 3.5ms (default), 10ms, 50ms, or 100ms.

6.3.6 Microphone Bias

The device integrates a built-in, low-noise, programmable, high-voltage, microphone bias pin (MICBIAS) that can be used in the system for biasing the analog microphone. The integrated bias amplifier supports up to 30mA of load current, which can be used for multiple microphones and is designed to provide a combination of high PSRR, low noise, and programmable bias voltages to allow the biasing to be fine tuned for specific microphone combinations. The TAC5312-Q1 has an integrated efficient boost converter to generate the high voltage supply for the programmable microphone bias using an external, low-voltage, 3.3-V BSTVDD supply.

When using the MICBIAS pin for biasing multiple microphones, TI recommends avoiding common impedance on the board layout for the MICBIAS connection to minimize coupling across microphones. 表 6-9 shows the available microphone bias programmable options.

表 6-9. MICBIAS Programmable Settings

P1_R115_D[7:4] : MBIAS_VAL[3:0]	MICBIAS OUTPUT VOLTAGE
0000	Bypass to BSTOUT
0001	Set to 3.0 V
0010	Set to 3.5 V
0011-1000	Set to 4.0 V- 6.5 V
1001	Set to 7.0 V
1010	Set to 7.5 V(default)
1011	Set to 8.0 V
1100	Set to 8.5 V
1101	Set to 9.0 V
1110	Set to 9.5 V
1111	Set to 10.0 V

The microphone bias output can be powered on or powered off (default) by configuring the MICBIAS_PDZ, P0_R120_D5 register bit. Additionally, the device provides an option to configure the GPIOx pins to directly control the microphone bias output power on or power off. This feature is useful in some systems to control the microphone directly without engaging the host for I^2C or SPI communication. The MICBIAS_PDZ, P0_R120_D5 register bit value is ignored if the GPIOx pins are configured to control the microphone bias power on or power off.

6.3.7 Input DC Fault Diagnostics

Each input of the TAC5312-Q1 features highly comprehensive DC fault diagnostics that can be configured to detect fault conditions in the DC-coupled input configuration and trigger an interrupt request to a host processor. Diagnostics are enabled for each channel by configuring DIAG_CFG0, P1_R70. For channels with diagnostics enabled, the input pins are scanned automatically by an integrated SAR ADC with a programmable repetition rate. The repetition rate can be configured using the REP_RATE, P1_R74_D[7:6] register bits. For fastest fault response time and also to get better signal integrity and signal chain performance for the record channel, REP_RATE must be configured to 0 (non-default setting). The diagnostic processor averages eight consecutive samples per test to improve noise performance. The DC fault diagnostics is not supported in the AC-coupled input configuration.

The device features various programmable threshold registers, P1_R71 to P1_R72, which can by configured by the host processor to define the fault region for a different category of fault condition detection. Additionally, there is also a debounce feature, configured with FAULT_DBNCE_SEL, P1_R74_D[3:2]. This feature sets the number of consecutive scan counts where the fault condition occurs before the latched status register is tripped, thus reducing false triggers by transient events. The device also has a moving average feature, P1_R75, which continuously averages out the newly measured data with old measured data and thus reduces the false triggers by any short-duration transient events.

6.3.7.1 Fault Conditions

6.3.7.1.1 Input Pin Short to Ground

A short to ground fault occurs when the voltage of the input pin is measured below the threshold voltage with respect to ground (AVSS). The threshold can be set by configuring DIAG_SHT_GND, P1_R72_D[7:4].

6.3.7.1.2 Input Pin Short to MICBIAS

A short to MICBIAS fault occurs when the difference between the voltage measured for the MICBIAS pin and the input pin (MICBIAS – INxx) is less than the threshold. The threshold can be set by configuring DIAG_SHT_MICBIAS, P1_R72_D[3:0].

6.3.7.1.3 Open Inputs

In the event that a microphone becomes disconnected from the inputs, the microphone bias resistors pull INxP to MICBIAS and INxM to ground. The combination of INxP shorted to MICBIAS and INxM shorted to ground for the same channel in a diagnostic sweep results in an open input fault condition.

6.3.7.1.4 Short Between INxP and INxM

An input terminal shorted fault occurs when the difference between the voltage measured for the input pin INxP and the input pin INxM of the same channel is less than the threshold. The threshold can be set by configuring DIAG_SHT_TERM, P1_R71_D[7:4].

6.3.7.1.5 Input Pin Overvoltage

An input terminal overvoltage fault occurs when the voltage measured for the input pin is above the voltage measured for the MICBIAS pin.

6.3.7.1.6 Input Pin Short to VBAT_IN

A short to VBAT_IN fault occurs when the difference between the voltage measured for the VBAT_IN pin and the input pin, ABS(VBAT_IN – INxx), is less than the threshold or both the VBAT_IN and INxx pin measured voltages are above 11.7V. The threshold can be set by configuring DIAG_SHT_VBAT_IN, P1_R71_D[3:0].

When VBAT_IN is less than MICBIAS, false fault detections can exist based on the signal level of the INxx pin. To minimize false detections there is also a separate debounce count for this condition set by configuring VSHORT_DBNCE, P1_R74_D1.

6.3.7.2 Fault Reporting

Faults are reported in live and latched status registers. The live registers, P1_R45 to P1_R55, are updated continuously with each new scan and report the most recent measurements reported by the diagnostics processor. The latched status of each diagnostic fault is reported by the channel in P1_R60 to P1_R67, and a latched summary by the channel is reported in P1_R52 to P1_R59. If the LTCH_CLR_ON_READ, P1_R66_D0, bit is set to '0', then the latched registers clear upon reading, and are latched if the associated bit in the live fault registers transitions from a ‘0’ to a ‘1’. A transition of any bit in the latched register from a ‘0’ to ‘1’ triggers an interrupt request.

For detecting a persistent fault, an additional mode is available for the latched registers. In this mode, the latched registers are only cleared upon reading if the status bit in the associated live status register is ‘0’ at the time of reading. This mode is enabled (default setting) by configuring LTCH_CLR_ON_READ, P0_R66_D0 to a ‘1’.

6.3.7.2.1 Overcurrent and Overtemperature Protection

The device has an overcurrent protection circuit that limits the current drawn out of the MICBIAS output to the maximum supported level when an external undesired short event occurs on the MICBIAS pin. The device sets the status flag, P1_R59_D2 bit, on an overcurrent detection. Additionally, the device has an overtemperature detection circuit that is enabled by default and sets the status flag, P1_R52_D5 bit, whenever the die junction temperature goes higher than the supported level.

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Additionally, the P1_R80 and P0_R66_D[4:3] register can be configured to shutdown MICBIAS along with the on-chip boost on an overtemperature detection. TI recommends configuring PD_ON_FLT_CFG, P0_R66_D4-3 to '10' so that on an overtemperature detection, the device powers-down MICBIAS, the on-chip boost, and all ADC channels.

More details and information on fault diagnostics are discussed in the *TAC5xxx-Q1 Fault Diagnostics, Interrupts, and Protection Features* application report.

6.3.8 Signal-Chain Processing

The TAC5312-Q1 signal chain is comprised of very-low-noise, high-performance, and low-power analog blocks and highly flexible and programmable digital processing blocks. The high performance and flexibility combined with a compact package makes the TAC5312-Q1 optimized for a variety of end-equipments and applications that require multichannel audio capture and playback. セクション 6.3.8.1 describe key components in ADC signal chain further.

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6.3.8.1 ADC Signal-Chain

図 6-19 shows the key components of the record path signal chain.

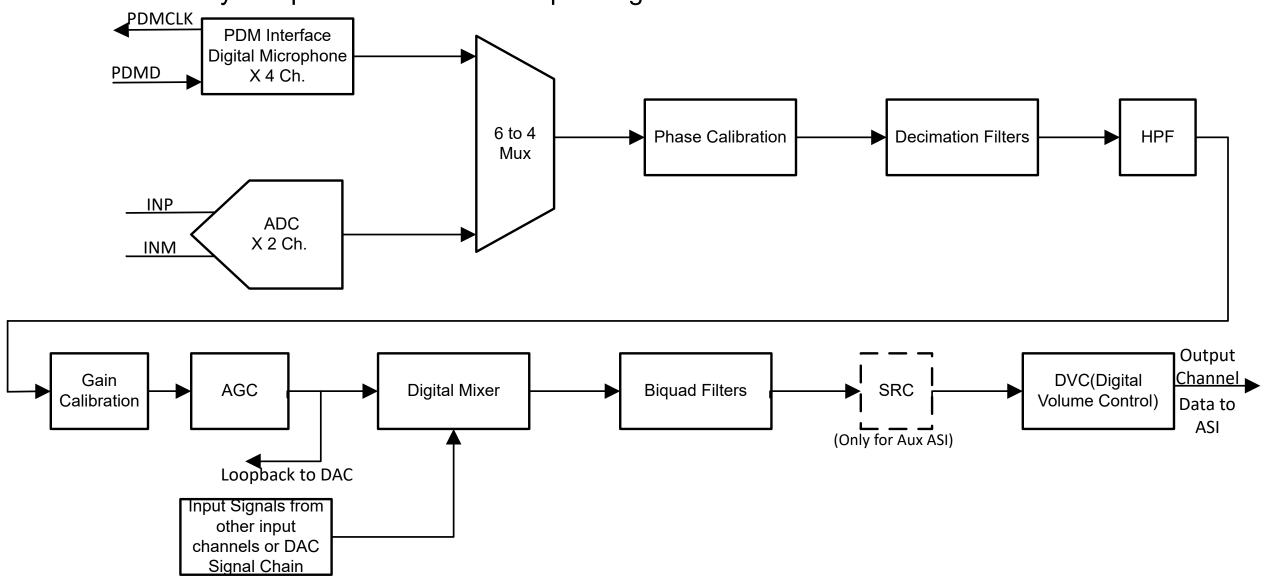

図 6-19. ADC Signal-Chain Processing Flowchart

The front-end ADC is very low noise, with a 115dB dynamic range performance. This low-noise and low-distortion, multibit, delta-sigma ADC enables the TAC5312-Q1 to record a far-field audio signal with very high fidelity, both in quiet and loud environments. Moreover, the ADC architecture has inherent antialias filtering with a high rejection of out-of-band frequency noise around multiple modulator frequency components. Therefore, the device prevents noise from aliasing into the audio band during ADC sampling. Further on in the signal chain, an integrated, high-performance multistage digital decimation filter sharply cuts off any out-of-band frequency noise with high stop-band attenuation.

The device also has an integrated programmable biquad filter that allows for custom low-pass, high-pass, or any other desired frequency shaping. Thus, the overall signal chain architecture removes the requirement to add external components for antialiasing low-pass filtering and thus saves drastically on the external system component cost and board space. See the *TAC5212 Integrated Analog Antialiasing Filter and Flexible Digital Filter* application report for further details.

The signal chain also consists of various highly programmable digital processing blocks such as phase calibration, gain calibration, high-pass filter, digital summer or mixer, biquad filters, synchronous sample rate converter, and volume control. The details of these processing blocks are discussed further in this section. The device also supports up to four digital PDM microphone recording channels when the analog recording channels are not used.

The desired input channels for recording can be enabled or disabled by using the CH_EN (P0_R118) register, and the output channels for the audio serial interface can be enabled or disabled by using the ASI_TX_CHx_CFG register. In general, the device supports simultaneous power-up and power-down of all active channels for simultaneous recording. However, based on the application's needs, if some channels must be powered up or powered down dynamically when the other channel recording is on, then that use case is supported by setting the DYN_PUPD_CFG register.

The device supports an input signal bandwidth up to 100kHz, which allows the high-frequency non-audio signal to be recorded by using a 216kHz (or higher) sample rate. Wide bandwidth mode can be enabled or disabled by setting ADC_CHx_BW_MODE bit.

For sample rates of 48kHz or lower, the device supports all features and various programmable processing blocks. However, for sample rates higher than 48kHz, there are limitations in the number of simultaneous channel recordings and playback supported and the number of biquad filters and such. See the *TAC5212 Sampling Rates and Programmable Processing Blocks Supported* application report for further details.

6.3.8.1.1 Programmable Channel Gain and Digital Volume Control

The device has an independent programmable channel gain setting for each input channel that can be set to the appropriate value based on the maximum input signal expected in the system and the ADC VREF setting used (see the *セクション 6.3.5* section), which determines the ADC full-scale signal level.

The device has a programmable digital volume control with a range from –80dB to 47dB in steps of 0.5dB with the option to mute the channel recording. The digital volume control value can be changed dynamically while the ADC channel is powered-up and recording. During volume control changes, the soft ramp-up or ramp-down volume feature is used internally to avoid any audible artifacts. Soft-stepping can be entirely disabled using the ADC_DSP_DISABLE_SOFT_STEP (P0_R114_D1) register bit.

The digital volume control setting is independently available for each output channel, including the digital microphone record channel. However, the device also supports an option to gang-up the volume control setting for all channels together using the channel 1 digital volume control setting, regardless if channel 1 is powered up or powered down. This gang-up can be enabled using the ADC_DSP_DVOL_GANG (P0_R114_D0) register bit.

表 6-10 shows the programmable options available for the digital volume control.

表 6-10. Digital Volume Control (DVC) Programmable Settings

P0_R82_D[7:0] : ADC_CH1_DVOL[7:0]	DVC SETTING FOR OUTPUT CHANNEL 1
0000 0000 = 0d	Output channel 1 DVC is set to mute
0000 0001 = 1d	Output channel 1 DVC is set to –80dB
0000 0010 = 2d	Output channel 1 DVC is set to –79.5dB
0000 0011 = 3d	Output channel 1 DVC is set to –79dB
…	…
1010 0000 = 160d	Output channel 1 DVC is set to –0.5dB
1010 0001 = 161d (default)	Output channel 1 DVC is set to 0dB
1010 0010 = 162d	Output channel 1 DVC is set to 0.5dB
…	…
1111 1101 = 253d	Output channel 1 DVC is set to 46dB
1111 1110 = 254d	Output channel 1 DVC is set to 46.5dB
1111 1111 = 255d	Output channel 1 DVC is set to 47dB

Similarly, the digital volume control setting for output channel 2 to channel 4 can be configured using the CH2_DVOL (P0_R87) to CH4_DVOL (P0_R95) register bits, respectively.

The internal digital processing engine soft ramps up the volume from a muted level to the programmed volume level when the channel is powered up, and the internal digital processing engine soft ramps down the volume from a programmed volume to mute when the channel is powered down. This soft-stepping of volume is done to prevent abruptly powering up and powering down the record channel. This feature can also be entirely disabled using the ADC_DSP_DISABLE_SOFT_STEP (P0_R114_D1) register bit.

6.3.8.1.2 Programmable Channel Gain Calibration

Along with the digital volume control, this device also provides programmable channel gain calibration. The gain of each channel can be finely calibrated or adjusted in steps of 0.1dB for a range of –0.8dB to 0.7dB gain error. This adjustment is useful when trying to match the gain across channels resulting from external components and microphone sensitivity. This feature, in combination with the regular digital volume control, allows the gains across all channels to be matched for a wide gain error range with a resolution of 0.1dB. 表 6-11 shows the programmable options available for the channel gain calibration.

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表 6-11. Channel Gain Calibration Programmable Settings

P0_R83_D[7:4] : ADC_CH1_FGAIN[3:0]	CHANNEL GAIN CALIBRATION SETTING FOR INPUT CHANNEL 1
0000 = 0d	Input channel 1 gain calibration is set to –0.8dB
0001 = 1d	Input channel 1 gain calibration is set to –0.7dB
…	…
1000 = 8d (default)	Input channel 1 gain calibration is set to 0dB
…	…
1110 = 14d	Input channel 1 gain calibration is set to 0.6dB
1111 = 15d	Input channel 1 gain calibration is set to 0.7dB

Similarly, the channel gain calibration setting for input channel 2 to channel 4 can be configured using the ADC_CH2_CFG3 (P0_R88) to ADC_CH4_CFG3 (P0_R96) register bits, respectively.

6.3.8.1.3 Programmable Channel Phase Calibration

In addition to the gain calibration, the phase delay in each channel can be finely calibrated or adjusted in steps of one modulator clock cycle for a cycle range of 0 to 255 for the phase error. The modulator clock, the same clock used for ADC_MOD_CLK, is 6.144MHz (the output data sample rate is multiples or submultiples of 48kHz) or 5.6448MHz (the output data sample rate is multiples or submultiples of 44.1kHz) irrespective of the analog microphone or digital microphone use case. This feature is very useful for many applications that must match the phase with fine resolution between each channel, including any phase mismatch across channels resulting from external components or microphones. 表 6-12 shows the available programmable options for channel phase calibration.

表 6-12. Channel Phase Calibration Programmable Settings

P0_R64_D[7:0] : CH1_PCAL[7:0]	CHANNEL PHASE CALIBRATION SETTING FOR INPUT CHANNEL 1
0000 0000 = 0d (default)	Input channel 1 phase calibration with no delay
0000 0001 = 1d	Input channel 1 phase calibration delay is set to one cycle of the modulator clock
0000 0010 = 2d	Input channel 1 phase calibration delay is set to two cycles of the modulator clock
…	…
1111 1110 = 254d	Input channel 1 phase calibration delay is set to 254 cycles of the modulator clock
1111 1111 = 255d	Input channel 1 phase calibration delay is set to 255 cycles of the modulator clock

Similarly, the channel phase calibration setting for input channel 2 to channel 8 can be configured using the CH2_PCAL (P0_R69) to CH8_PCAL (P0_R99) register bits, respectively.

The phase calibration feature must not be used when the analog input and PDM input are used together for simultaneous conversion.

6.3.8.1.4 Programmable Digital High-Pass Filter

To remove the DC offset component and attenuate the undesired low-frequency noise content in the record data, the device supports a programmable high-pass filter (HPF). The HPF is not a channel-independent filter setting but is globally applicable for all ADC channels. This HPF is constructed using the first-order infinite impulse response (IIR) filter, and is efficient enough to filter out possible DC components of the signal. 表 6-13 shows the predefined –3-dB cutoff frequencies available that can be set by using the ADC_DSP_HPF_SEL[1:0] register bits of P0_R114. Additionally, to achieve a custom –3-dB cutoff frequency for a specific application, the device also allows the first-order IIR filter coefficients to be programmed when the HPF_SEL[1:0] register bits are set to 2'b00. 図 6-20 illustrates a frequency response plot for the HPF filter.

表 6-13. HPF Programmable Settings

P0_R107_D[1:0] : HPF_SEL[1:0]	-3dB CUTOFF FREQUENCY SETTING	-3dB CUTOFF FREQUENCY AT 16-kHz SAMPLE RATE	-3dB CUTOFF FREQUENCY AT 48-kHz SAMPLE RATE
00	Programmable 1st-order IIR filter	Programmable 1st-order IIR filter	Programmable 1st-order IIR filter

表 6-13. HPF Programmable Settings (続き)

P0_R107_D[1:0] : HPF_SEL[1:0]	-3dB CUTOFF FREQUENCY SETTING	-3dB CUTOFF FREQUENCY AT 16-kHz SAMPLE RATE	-3dB CUTOFF FREQUENCY AT 48-kHz SAMPLE RATE
01 (default)	0.00002 × f_S	0.25Hz	1Hz
10	0.00025 × f_S	4Hz	12Hz
11	0.002 × f_S	32Hz	96Hz

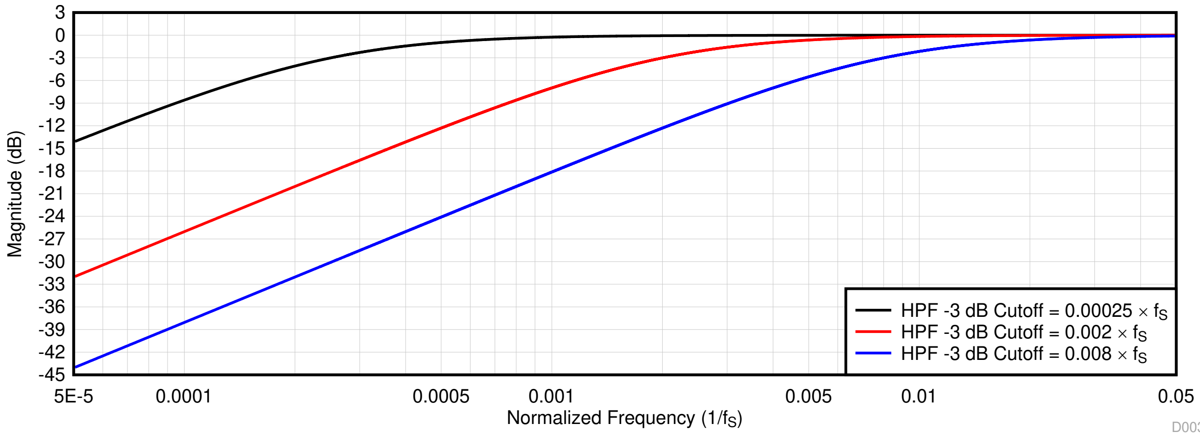

図 6-20. HPF Filter Frequency Response Plot

式 1 gives the transfer function for the first-order programable IIR filter:

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{31} - D_1 z^{-1}} \quad (1)$$

The frequency response for this first-order programmable IIR filter with default coefficients is flat at a gain of 0dB (all-pass filter). The host device can override the frequency response by programming the IIR coefficients in 表 6-14 to achieve the desired frequency response for high-pass filtering or any other desired filtering. If HPF_SEL[1:0] is set to 2'b00, the host device must write these coefficient values for the desired frequency response before powering-up any ADC channel for recording. 表 6-14 shows the filter coefficients for the first-order IIR filter.

表 6-14. 1st-Order IIR Filter Coefficients

FILTER	FILTER COEFFICIENT	DEFAULT COEFFICIENT VALUE	COEFFICIENT REGISTER MAPPING
Programmable 1st-order IIR filter (can be allocated to HPF or any other desired filter)	N_0	0x7FFFFFFF	P4_R72-R75
	N_1	0x00000000	P4_R76-R79
	D_1	0x00000000	P4_R80-R83

6.3.8.1.5 Programmable Digital Biquad Filters

The device supports up to 12 programmable digital biquad filters available for ADC signal chain limited to 3/channel. These highly efficient filters achieve the desired frequence response. The TAC5312-Q1 also supports on the fly programmable Biquad filters for two channel record use case. In digital signal processing, a digital biquad filter is a second-order, recursive linear filter with two poles and two zeros. 式 2 gives the transfer function of each biquad filter:

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$$H(z) = \frac{N_0 + 2N_1 z^{-1} + N_2 z^{-2}}{2^{31} - 2D_1 z^{-1} - D_2 z^{-2}} \quad (2)$$

The frequency response for the biquad filter section with default coefficients is flat at a gain of 0 dB (all-pass filter). The host device can override the frequency response by programming the biquad coefficients to achieve the desired frequency response for a low-pass, high-pass, or any other desired frequency shaping. If biquad filtering is required, then the host device must write these coefficients values before powering up any ADC channels for recording. In two channel use case, the TAC5312-Q1 also supports on the fly programmable filters. In this case, Device uses two banks of filters for one channel with a switch bit to perform the switch from one filter bank to the other. As described in 表 6-15, these biquad filters can be allocated for each output channel based on the ADC_DSP_BQ_CFG[1:0] register setting of P0_R114. By setting BIQUAD_CFG[1:0] to 2'b00, the biquad filtering for all record channels is disabled and the host device can choose this setting if no additional filtering is required for the system application.

表 6-15. Biquad Filter Allocation to the Record Output Channel

PROGRAMMABLE BIQUAD FILTER	RECORD OUTPUT CHANNEL ALLOCATION USING P0_R114_D[3:2] REGISTER SETTING		
	ADC_DSP_BQ_CFG[1:0] = 2'b01 (1 Biquad per Channel)	ADC_DSP_BQ_CFG[1:0] = 2'b10 (Default) (2 Biquads per Channel)	ADC_DSP_BQ_CFG[1:0] = 2'b11 (3 Biquads per Channel)
Biquad filter 1	Allocated to output channel 1	Allocated to output channel 1	Allocated to output channel 1
Biquad filter 2	Allocated to output channel 2	Allocated to output channel 2	Allocated to output channel 2
Biquad filter 3	Allocated to output channel 3	Allocated to output channel 3	Allocated to output channel 3
Biquad filter 4	Allocated to output channel 4	Allocated to output channel 4	Allocated to output channel 4
Biquad filter 5	Not used	Allocated to output channel 1	Allocated to output channel 1
Biquad filter 6	Not used	Allocated to output channel 2	Allocated to output channel 2
Biquad filter 7	Not used	Allocated to output channel 3	Allocated to output channel 3
Biquad filter 8	Not used	Allocated to output channel 4	Allocated to output channel 4
Biquad filter 9	Not used	Not used	Allocated to output channel 1
Biquad filter 10	Not used	Not used	Allocated to output channel 2
Biquad filter 11	Not used	Not used	Allocated to output channel 3
Biquad filter 12	Not used	Not used	Allocated to output channel 4

表 6-16 shows the biquad filter coefficients mapping to the register space.

表 6-16. Biquad Filter Coefficients Register Mapping

PROGRAMMABLE BIQUAD FILTER	BIQUAD FILTER COEFFICIENTS REGISTER MAPPING	PROGRAMMABLE BIQUAD FILTER	BIQUAD FILTER COEFFICIENTS REGISTER MAPPING
Biquad filter 1	P8_R8-R27	Biquad filter 7	P9_R8-R27
Biquad filter 2	P8_R28-R47	Biquad filter 8	P9_R28-R47
Biquad filter 3	P8_R48-R67	Biquad filter 9	P9_R48-R67
Biquad filter 4	P8_R68-R87	Biquad filter 10	P9_R68-R87
Biquad filter 5	P8_R88-R107	Biquad filter 11	P9_R88-R107
Biquad filter 6	P8_R108-R127	Biquad filter 12	P9_R108-R127

6.3.8.1.6 Programmable Channel Summer and Digital Mixer

For applications that require an even higher SNR than that supported for each channel, the device digital summing mode can be used. In this mode, the digital record data are summed up across the channel with an equal weightage factor, which helps in reducing the effective record noise.

The device supports a fully programmable mixer feature that can mix the various input channels with their custom programmable scale factor to generate the final output channels. 図 6-21 shows a block diagram that describes the mixer 1 operation to generate output channel 1.

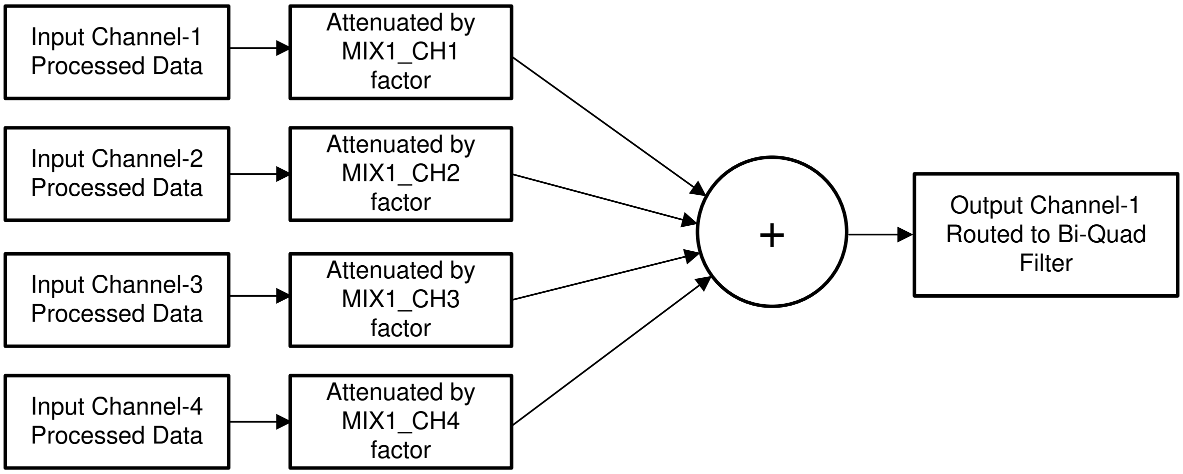

図 6-21. Programmable Digital Mixer Block Diagram

A similar mixer operation is performed by mixer 2, mixer 3, and mixer 4 to generate output channel 2, channel 3, and channel 4, respectively.

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6.3.8.1.7 Configurable Digital Decimation Filters

The device record channel includes a high dynamic range and a built-in digital decimation filter to process the oversampled data from the multibit delta-sigma (ΔΣ) modulator to generate digital data at the same Nyquist sampling rate as the FSYNC rate. As illustrated in 図 6-19, this decimation filter can also be used for processing the oversampled PDM stream from the digital microphone. The decimation filter can be chosen from four different types, depending on the required frequency response, group delay, power consumption, and phase linearity requirements for the target application. The selection of the decimation filter option can be done by configuring the ADC_DSP_DECI_FILT, P0_R114_D[7:6] register bits. Low power filter can be configured by setting ADC_LOW_PWR_FILT, P0_R78_D2 bit. 表 6-17 shows the configuration register setting for the decimation filter mode selection for the record channel.

表 6-17. Decimation Filter Mode Selection for the Record Channel

P0_R78_D2 : ADC_LOW_PWR_FILT	P0_R114_D[7:6] : ADC_DSP_DECI_FILT[1:0]	DECIMATION FILTER MODE SELECTION
0	00 (default)	Linear phase filters are used for the decimation
0	01	Low latency filters are used for the decimation
0	10	Ultra-low latency filters are used for the decimation
0	11	Reserved (do not use this setting)
1	x	Low power filters are used for the decimation

6.3.8.1.7.1 Linear Phase Filters

The linear phase decimation filters are the default filters set by the device and can be used for all applications that require a perfect linear phase with zero-phase deviation within the pass-band specification of the filter. The filter performance specifications and various plots for all supported output sampling rates are listed in this section.

6.3.8.1.7.1.1 Sampling Rate: 16kHz or 14.7kHz

図 6-22 and 図 6-23 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 16kHz or 14.7kHz. 表 6-18 lists the specifications for a decimation filter with a 16kHz or 14.7kHz sampling rate.

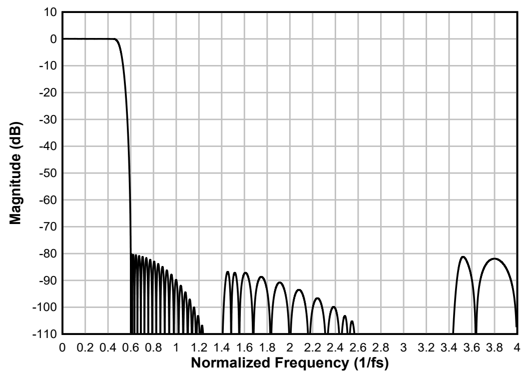

図 6-22. Linear Phase Decimation Filter Magnitude Response

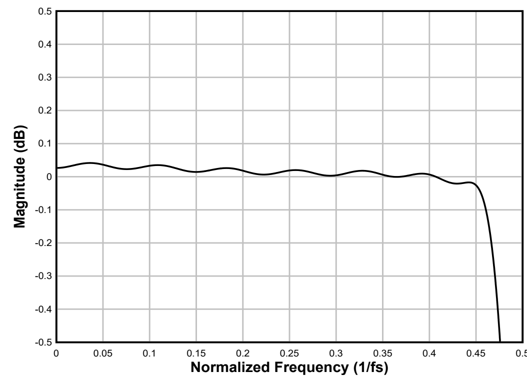

図 6-23. Linear Phase Decimation Filter Pass-Band Ripple

表 6-18. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.6 × f_S to 4 × f_S	80.2			dB
	Frequency range is 4 × f_S onwards	84.7			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		16.1		$1/f_S$

6.3.8.1.7.1.2 Sampling Rate: 24kHz or 22.05kHz

図 6-24 and 図 6-25 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 24kHz or 22.05kHz. 表 6-19 lists the specifications for a decimation filter with a 24kHz or 22.05kHz sampling rate.

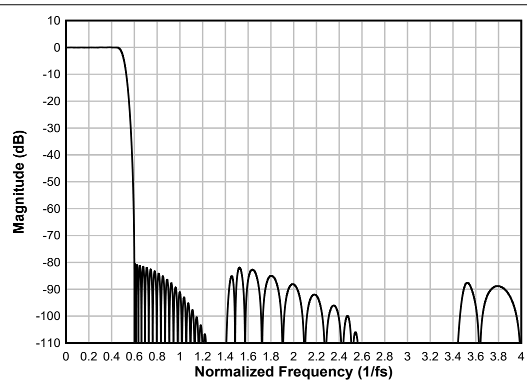

図 6-24. Linear Phase Decimation Filter Magnitude Response

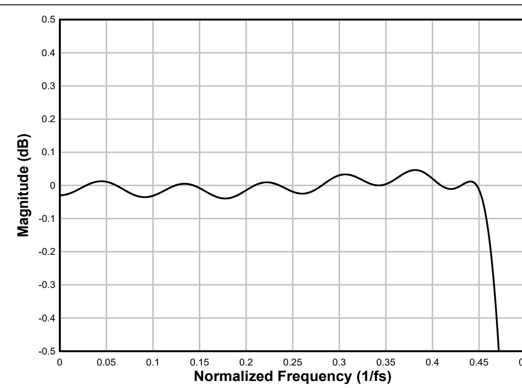

図 6-25. Linear Phase Decimation Filter Pass-Band Ripple

表 6-19. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB

表 6-19. Linear Phase Decimation Filter Specifications (続き)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Stop-band attenuation	Frequency range is 0.6 × f_S to 4 × f_S	80.6			dB
	Frequency range is 4 × f_S onwards	92.9			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		14.7		1/f_S

6.3.8.1.7.1.3 Sampling Rate: 32kHz or 29.4kHz

図 6-26 and 図 6-27 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 32kHz or 29.4kHz. 表 6-20 lists the specifications for a decimation filter with a 32kHz or 29.4kHz sampling rate.

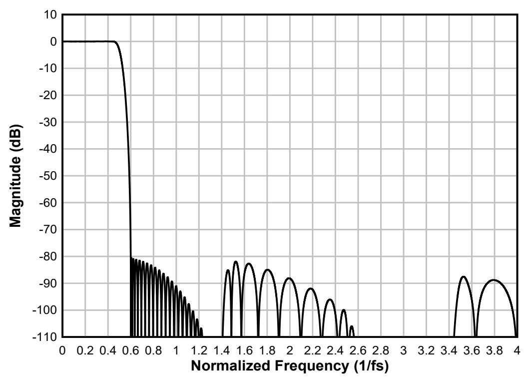

図 6-26. Linear Phase Decimation Filter Magnitude Response

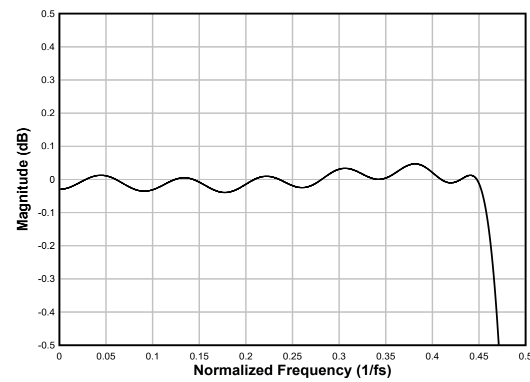

図 6-27. Linear Phase Decimation Filter Pass-Band Ripple

表 6-20. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.05	dB
Stop-band attenuation	Frequency range is 0.6 × f_S to 4 × f_S	80.6			dB
	Frequency range is 4 × f_S onwards	92.9			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		14.7		1/f_S

6.3.8.1.7.1.4 Sampling Rate: 48kHz or 44.1kHz

図 6-28 and 図 6-29 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 48kHz or 44.1kHz. 表 6-21 lists the specifications for a decimation filter with a 48kHz or 44.1kHz sampling rate.

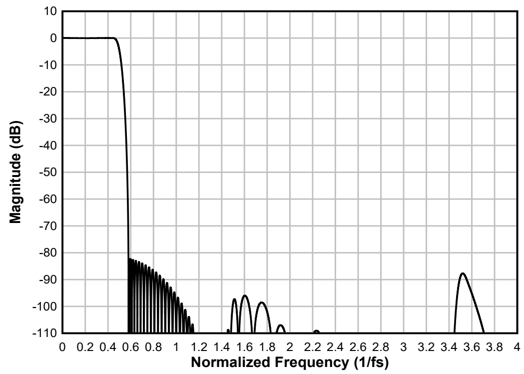

図 6-28. Linear Phase Decimation Filter Magnitude Response

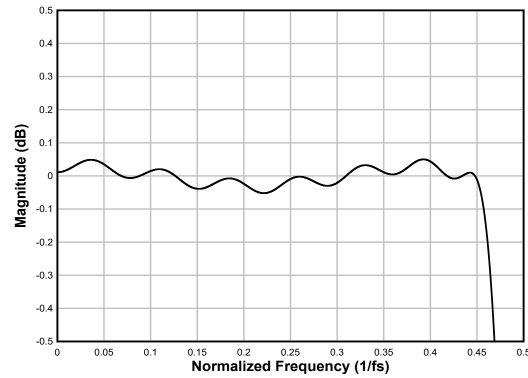

図 6-29. Linear Phase Decimation Filter Pass-Band Ripple

表 6-21. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.052		0.05	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	82.2			dB
	Frequency range is 4 × f_S onwards	97.9			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		17.0		$1/f_S$

6.3.8.1.7.1.5 Sampling Rate: 96kHz or 88.2kHz

図 6-30 and 図 6-31 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 96kHz or 88.2kHz. 表 6-22 lists the specifications for a decimation filter with a 96kHz or 88.2kHz sampling rate.

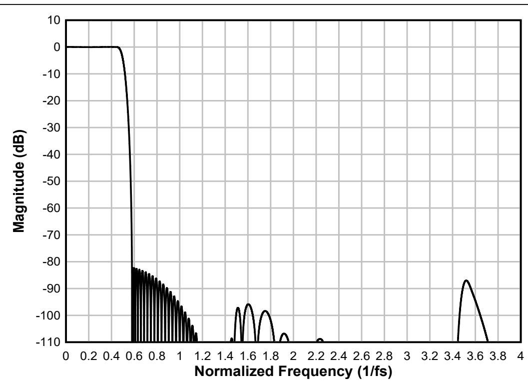

図 6-30. Linear Phase Decimation Filter Magnitude Response

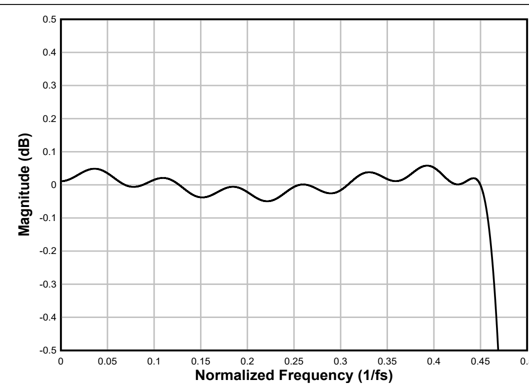

図 6-31. Linear Phase Decimation Filter Pass-Band Ripple

表 6-22. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.058	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	82.2			dB
	Frequency range is 4 × f_S onwards	96.9			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		16.9		$1/f_S$

6.3.8.1.7.1.6 Sampling Rate: 384kHz or 352.8kHz

図 6-32 and 図 6-33 respectively show the magnitude response and the pass-band ripple for a decimation filter with a sampling rate of 384kHz or 352.8kHz. 表 6-23 lists the specifications for a decimation filter with an 384kHz or 352.8kHz sampling rate.

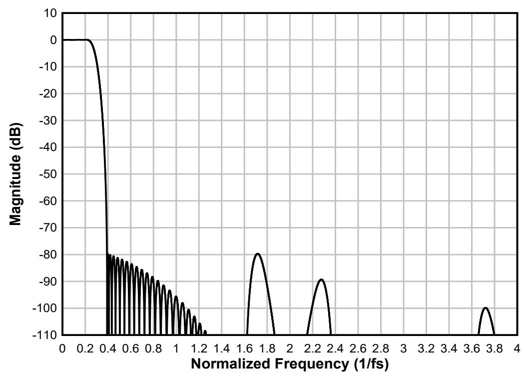

図 6-32. Linear Phase Decimation Filter Magnitude Response

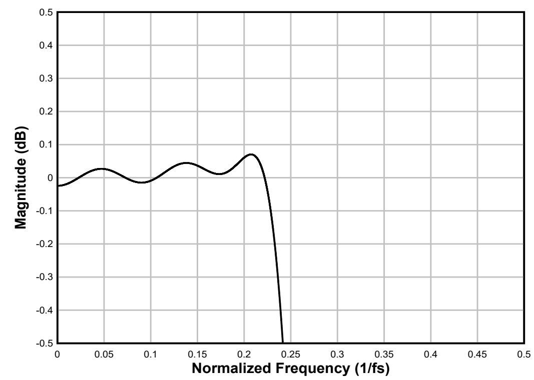

図 6-33. Linear Phase Decimation Filter Pass-Band Ripple

表 6-23. Linear Phase Decimation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.227 × f_S	–0.07		0.07	dB
Stop-band attenuation	Frequency range is 0.391 × f_S to 2 × f_S	79.7			dB
	Frequency range is 2 × f_S onwards	89.3			
Group delay or latency	Frequency range is 0 to 0.212 × f_S		11.45		$1/f_S$

6.3.9 DAC Signal-Chain

図 6-34 shows the key components of the playback signal chain.

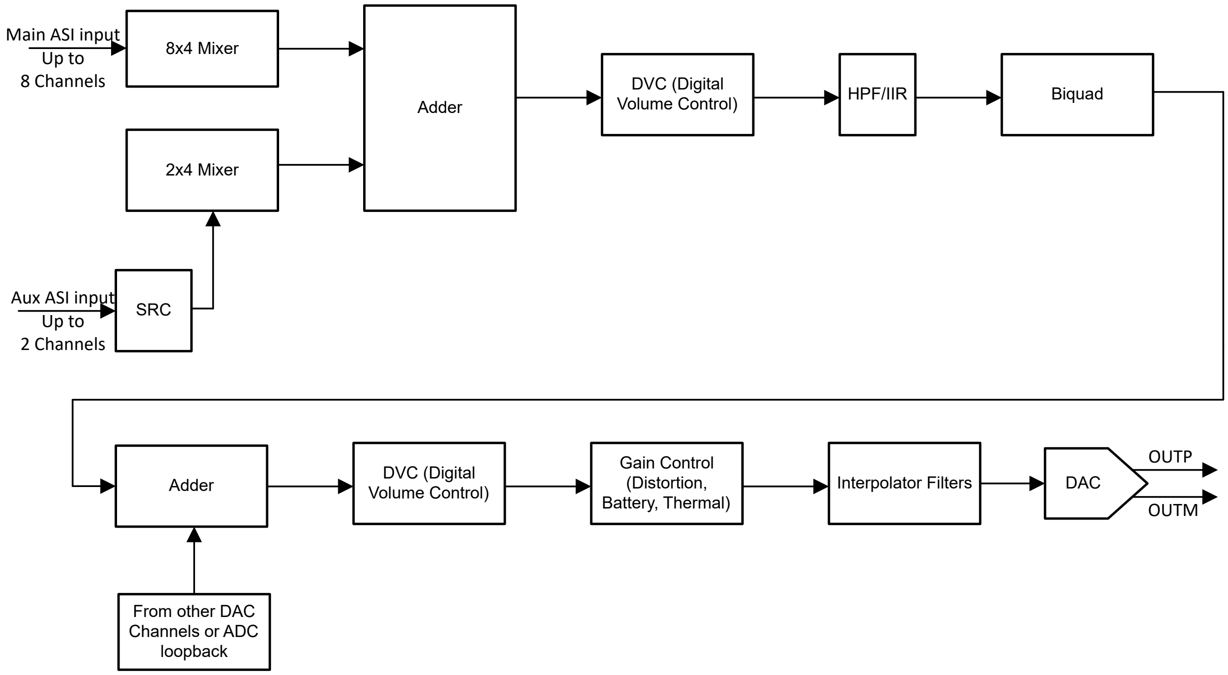

図 6-34. DAC Signal-Chain Processing Flowchart

The DAC signal chain offers a highly flexible low noise playback path for low noise and high-fidelity audio applications. This low-noise and low-distortion, multibit, delta-sigma DAC enables the TAC5312-Q1 to achieve 120dB dynamic range in a very low power. Moreover, the DAC architecture has inherent antialias filtering with a high rejection of out-of-band frequency noise around multiple modulator frequency components. Therefore, the device prevents noise from aliasing into the audio band. Further on in the signal chain, an integrated, high-performance multistage digital interpolation filter sharply cuts off any out-of-band frequency noise with high stop-band attenuation.

The signal chain also consists of various highly programmable digital processing blocks such as biquad filters, phase calibration, gain calibration, high-pass filter, digital summer or mixer, synchronous sample rate converter, distortion limiter, thermal foldback, brownout prevention, and volume control. The details of these processing blocks are discussed further in this section. The device also supports up to four channel single-ended output modes and an analog bypass option from ADC input to DAC output.

The output channels for playback can be enabled or disabled by using the CH_EN (P0_R118) register, and the input channels for the audio serial interface can be enabled or disabled by using the PASI_RX_CHx_CFG or SASI_RX_CHx_CFG bits. The device supports simultaneous power-up and power-down of all active channels for simultaneous playback. However, based on the application needs, if some channels must be powered-up or powered-down dynamically when the other channel playback is on, then that use case is supported by setting the DYN_PUPD_CFG register.

The device supports multiple data mixing options where up to 8 Input Channels from Main ASI, 2 Input Channels from Aux ASI, ADC loopback data, and tone generator can be mixed with flexible gain options for each path before playback on DAC output. By default, these mixers are disabled and channels are configured for only one channel data. Mixers can be configured by setting ASI_DIN_Mixers on Page 17.

The device supports an output signal bandwidth up to 100kHz, which allows the high-frequency non-audio signal to be played by using a 216kHz (or higher) sample rate. Wide band mode can be enabled or disabled by using the DAC_CHx_BW_Mode bit.

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For sample rates of 48kHz or lower, the device supports all features and various programmable processing blocks. However, for sample rates higher than 48kHz, there are limitations in the number of simultaneous channel recording and playback supported and the number of biquad filters and such. See the *TAC5212 Sampling Rates and Programmable Processing Blocks Supported* application report for further details.

6.3.9.1 Programmable Channel Gain and Digital Volume Control

The device has an independent programmable channel gain setting for each output channel that can be set to the appropriate value based on the maximum input signal expected in the system, This can be done by configuring OUT1x_LVL_CTRL and OUT2x_LVL_CTRL bits. Coarse gain configuration from -6dB to +24dB is available with these controls in steps of 6dB. .

The device has a programmable digital volume control with a range from –100dB to 27dB in steps of 0.5dB with the option to mute the channel recording. The digital volume control value can be changed dynamically while the DAC channel is powered-up and playing. During volume control changes, the soft ramp-up or ramp-down volume feature is used internally to avoid any audible artifacts. Soft-stepping can be entirely disabled using the DAC_DSP_DISABLE_SOFT_STEP (P0_R115_D1) register bit.

The digital volume control setting is independently available for each of the 4 single ended output channels. In the case of 2 Channel Differential DAC, Only settings for DAC_CH1A and DAC_CH2A are applicable. The device also supports an option to gang-up the volume control setting for all channels together using the channel 1A digital volume control setting, regardless if channel 1A is powered up or powered down. This gang-up can be enabled using the DAC_DSP_DVOL_GANG (P0_R115_D0) register bit.

表 6-24 shows the programmable options available for the digital volume control.

表 6-24. Digital Volume Control (DVC) Programmable Settings

P0_R103_D[7:0] : DAC_CH1A_DVOL[7:0]	DVC SETTING FOR OUTPUT CHANNEL 1A
0000 0000 = 0d	Output channel 1 DVC is set to mute
0000 0001 = 1d	Output channel 1 DVC is set to –100dB
0000 0010 = 2d	Output channel 1 DVC is set to –99.5dB
0000 0011 = 3d	Output channel 1 DVC is set to –99dB
…	…
1100 1000 = 200d	Output channel 1 DVC is set to –0.5dB
1100 1001 = 201d (default)	Output channel 1 DVC is set to 0dB
1100 1010 = 202d	Output channel 1 DVC is set to 0.5dB
…	…
1111 1101 = 253d	Output channel 1 DVC is set to 26dB
1111 1110 = 254d	Output channel 1 DVC is set to 26.5dB
1111 1111 = 255d	Output channel 1 DVC is set to 27dB

Similarly, the digital volume control setting for output channel 1B,2A and 2B can be configured using the CH1B_DVOL (P0_R103) to CH2B_DVOL (P0_R112) register bits, respectively.

The internal digital processing engine soft ramps up the volume from a muted level to the programmed volume level when the channel is powered up, and the internal digital processing engine soft ramps down the volume from a programmed volume to mute when the channel is powered down. This soft-stepping of volume is done to prevent abruptly powering up and powering down the playback channel which can cause audible artifacts. This feature can also be entirely disabled using the DAC_DSP_DISABLE_SOFT_STEP (P0_R115_D1) register bit.

6.3.9.2 Programmable Channel Gain Calibration

Along with the digital volume control, this device also provides programmable channel gain calibration. The gain of each channel can be finely calibrated or adjusted in steps of 0.1dB for a range of –0.8dB to 0.7dB gain error. This adjustment is useful when trying to match the gain across channels resulting from transducer sensitivity and load impedance mismatch. This feature, in combination with the regular digital volume control, allows the gains across all channels to be matched for a wide gain error range with a resolution of 0.1dB. 表 6-25 shows the programmable options available for the channel gain calibration.

表 6-25. DAC Channel Gain Calibration Programmable Settings

P0_R104_D[7:4] : DAC_CH1A_FGAIN[3:0]	CHANNEL GAIN CALIBRATION SETTING FOR INPUT CHANNEL 1A
0000 = 0d	Input channel 1 gain calibration is set to –0.8dB
0001 = 1d	Input channel 1 gain calibration is set to –0.7dB
…	…
1000 = 8d (default)	Input channel 1 gain calibration is set to 0dB
…	…
1110 = 14d	Input channel 1 gain calibration is set to 0.6dB
1111 = 15d	Input channel 1 gain calibration is set to 0.7dB

Similarly, the channel gain calibration setting for input channels 1B,2A and 2B can be configured using the DAC_CH1B_CFG1 (P0_R106), DAC_CH2A_CFG1 (P0_R111), and DAC_CH2B_CFG1 (P0_R113) register bits, respectively.

6.3.9.3 Programmable Digital High-Pass Filter

To remove the DC offset component and attenuate the undesired low-frequency noise content in the record data, the device supports a programmable high-pass filter (HPF). The HPF is not a channel-independent filter setting but is globally applicable for all DAC channels. This HPF is constructed using the first-order infinite impulse response (IIR) filter, and is efficient enough to filter out possible DC components of the signal. 表 6-26 shows the predefined –3dB cutoff frequencies available that can be set by using the DAC_DSP_HPF_SEL[1:0] register bits of P0_R115. Additionally, to achieve a custom –3dB cutoff frequency for a specific application, the device also allows the first-order IIR filter coefficients to be programmed when the DAC_DSP_HPF_SEL[1:0] register bits are set to 2'b00. 図 6-35 illustrates a frequency response plot for the HPF filter.

表 6-26. HPF Programmable Settings

P0_R115_D[5:4] : DAC_DSP_HPF_SEL[1:0]	-3-dB CUTOFF FREQUENCY SETTING	-3-dB CUTOFF FREQUENCY AT 16-kHz SAMPLE RATE	-3-dB CUTOFF FREQUENCY AT 48-kHz SAMPLE RATE
00	Programmable 1st-order IIR filter	Programmable 1st-order IIR filter	Programmable 1st-order IIR filter
01 (default)	$0.00002 \times f_S$	0.25Hz	1Hz
10	$0.00025 \times f_S$	4Hz	12Hz
11	$0.002 \times f_S$	32Hz	96Hz

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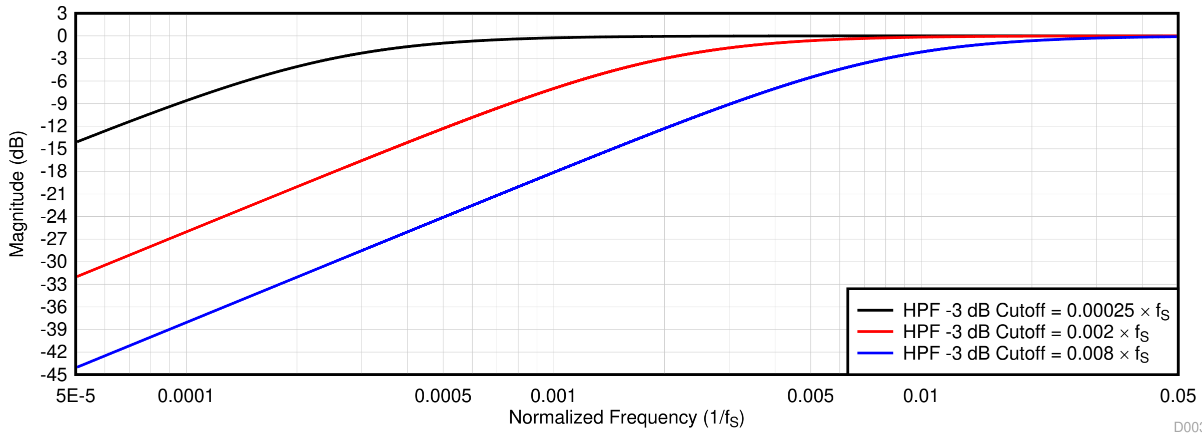

図 6-35. HPF Filter Frequency Response Plot

式 3 gives the transfer function for the first-order programable IIR filter:

$$H(z) = \frac{N_0 + N_1 z^{-1}}{2^{31} - D_1 z^{-1}} \quad (3)$$

The frequency response for this first-order programmable IIR filter with default coefficients is flat at a gain of 0 dB (all-pass filter). The host device can override the frequency response by programming the IIR coefficients in 表 6-27 to achieve the desired frequency response for high-pass filtering or any other desired filtering. If DAC_DSP_HPF_SEL[1:0] is set to 2'b00, the host device must write these coefficients values for the desired frequency response before powering-up any DAC channel for playback. 表 6-27 shows the filter coefficients for the first-order IIR filter.

表 6-27. 1st-Order IIR Filter Coefficients

FILTER	FILTER COEFFICIENT	DEFAULT COEFFICIENT VALUE	COEFFICIENT REGISTER MAPPING
Programmable 1st-order IIR filter (can be allocated to HPF or any other desired filter)	N_0	0x7FFFFFFF	P17_R120-R124
	N_1	0x00000000	P17_R125-R128
	D_1	0x00000000	P18_R8-R11

6.3.9.4 Programmable Digital Biquad Filters

The device supports up to 12 programmable digital biquad filters available for DAC signal chain limited to 3/ channel. These highly efficient filters achieve the desired frequence response. The TAC5312-Q1 also supports on the fly programmable Biquad filters for two channel playback use case. In digital signal processing, a digital biquad filter is a second-order, recursive linear filter with two poles and two zeros. 式 4 gives the transfer function of each biquad filter:

$$H(z) = \frac{N_0 + 2N_1 z^{-1} + N_2 z^{-2}}{2^{31} - 2D_1 z^{-1} - D_2 z^{-2}} \quad (4)$$

The frequency response for the biquad filter section with default coefficients is flat at a gain of 0 dB (all-pass filter). The host device can override the frequency response by programming the biquad coefficients to achieve the desired frequency response for a low-pass, high-pass, or any other desired frequency shaping. If biquad filtering is required, then the host device must write these coefficients values before powering up any ADC channels for recording. In two channel use case, the TAC5312-Q1 also supports on the fly programmable filters.

In this case, Device uses two banks of filters for one channel with a switch bit to perform the switch from one filter bank to the other. As described in 表 6-28, these biquad filters can be allocated for each output channel based on the DAC_DSP_BQ_CFG[1:0] register setting of P0_R115. By setting DAC_DSP_BQ_CFG[1:0] to 2'b00, the biquad filtering for all playback channels are disabled and the host device can choose this setting if no additional filtering is required for the system application. See the *TAC5212 Programmable Biquad Filter Configuration and Applications* application report for further details.

表 6-28. Biquad Filter Allocation to the Record Output Channel

PROGRAMMABLE BIQUAD FILTER	RECORD OUTPUT CHANNEL ALLOCATION USING P0_R115_D[3:2] REGISTER SETTING		
	DAC_DSP_BQ_CFG[1:0] = 2'b01 (1 Biquad per Channel)	DAC_DSP_BQ_CFG[1:0] = 2'b10 (Default) (2 Biquads per Channel)	DAC_DSP_BQ_CFG[1:0] = 2'b11 (3 Biquads per Channel)
Biquad filter 1	Allocated to output channel 1	Allocated to output channel 1	Allocated to output channel 1
Biquad filter 2	Allocated to output channel 2	Allocated to output channel 2	Allocated to output channel 2
Biquad filter 3	Allocated to output channel 3	Allocated to output channel 3	Allocated to output channel 3
Biquad filter 4	Allocated to output channel 4	Allocated to output channel 4	Allocated to output channel 4
Biquad filter 5	Not used	Allocated to output channel 1	Allocated to output channel 1
Biquad filter 6	Not used	Allocated to output channel 2	Allocated to output channel 2
Biquad filter 7	Not used	Allocated to output channel 3	Allocated to output channel 3
Biquad filter 8	Not used	Allocated to output channel 4	Allocated to output channel 4
Biquad filter 9	Not used	Not used	Allocated to output channel 1
Biquad filter 10	Not used	Not used	Allocated to output channel 2
Biquad filter 11	Not used	Not used	Allocated to output channel 3
Biquad filter 12	Not used	Not used	Allocated to output channel 4

表 6-29 shows the biquad filter coefficients mapping to the register space.

表 6-29. Biquad Filter Coefficients Register Mapping

PROGRAMMABLE BIQUAD FILTER	BIQUAD FILTER COEFFICIENTS REGISTER MAPPING	PROGRAMMABLE BIQUAD FILTER	BIQUAD FILTER COEFFICIENTS REGISTER MAPPING
Biquad filter 1	P16_R8-R27	Biquad filter 7	P17_R8-R27
Biquad filter 2	P16_R28-R47	Biquad filter 8	P17_R28-R47
Biquad filter 3	P16_R48-R67	Biquad filter 9	P17_R48-R67
Biquad filter 4	P16_R68-R87	Biquad filter 10	P17_R68-R87
Biquad filter 5	P16_R88-R107	Biquad filter 11	P17_R88-R107
Biquad filter 6	P16_R108-R127	Biquad filter 12	P17_R108-R127

6.3.9.5 Programmable Digital Mixer

The device supports a fully programmable mixer feature that can mix the various input channels with their custom programmable scale factor to generate the final output channels.

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6.3.9.6 Configurable Digital Interpolation Filters

The device playback channel includes a high dynamic range, built-in digital interpolation filter to process the input data stream to generate digital data stream for multibit delta-sigma (ΔΣ) modulator. The interpolation filter can be chosen from four different types, depending on the required frequency response, group delay, power consumption, and phase linearity requirements for the target application. The selection of the interpolation filter option can be done by configuring the DAC_DSP_INTX_FILT, P0_R115_D[7:6] register bits. Low power filter can be configured by setting DAC_LOW_PWR_FILT, P0_R79_D2 bit. 表 6-30 shows the configuration register setting for the decimation filter mode selection for the record channel.

表 6-30. Interpolation Filter Mode Selection for the Playback Channel

P0_R79_D2 : DAC_LOW_PWR_FILT	P0_R115_D[7:6] : DAC_DSP_INTX_FILT[1:0]	INTERPOLATION FILTER MODE SELECTION
0	00 (default)	Linear phase filters are used for the interpolation
0	01	Low latency filters are used for the interpolation
0	10	Ultra-low latency filters are used for the interpolation
0	11	Reserved (do not use this setting)
1	x	Low power filters are used for the interpolation

6.3.9.6.1 Linear Phase Filters

The linear phase interpolation filters are the default filters set by the device and can be used for all applications that require a perfect linear phase with zero-phase deviation within the pass-band specification of the filter. The filter performance specifications and various plots for all supported output sampling rates are listed in this section.

6.3.9.6.1.1 Sampling Rate: 16kHz or 14.7kHz

図 6-36 and 図 6-37 respectively show the magnitude response and the pass-band ripple for an interpolation filter with a sampling rate of 16kHz or 14.7kHz. 表 6-31 lists the specifications for an interpolation filter with a 16kHz or 14.7-kHz sampling rate.

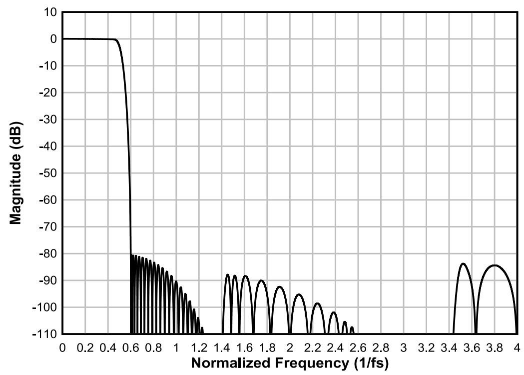

図 6-36. Linear Phase Interpolation Filter Magnitude Response

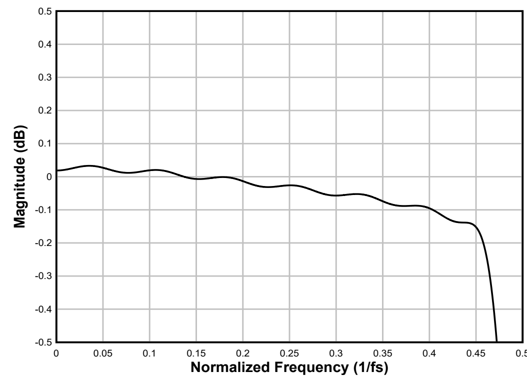

図 6-37. Linear Phase Interpolation Filter Pass-Band Ripple

表 6-31. Linear Phase Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.17		0.03	dB
Stop-band attenuation	Frequency range is 0.6 × f_S to 4 × f_S	80.4			dB
	Frequency range is 4 × f_S to 7.43 × f_S	86.9			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		16.0		1/f_S

6.3.9.6.1.2 Sampling Rate: 24kHz or 22.05kHz

図 6-38 and 図 6-39 respectively show the magnitude response and the pass-band ripple for an interpolation filter with a sampling rate of 24kHz or 22.05kHz. 表 6-32 lists the specifications for an interpolation filter with a 24kHz or 22.05kHz sampling rate.

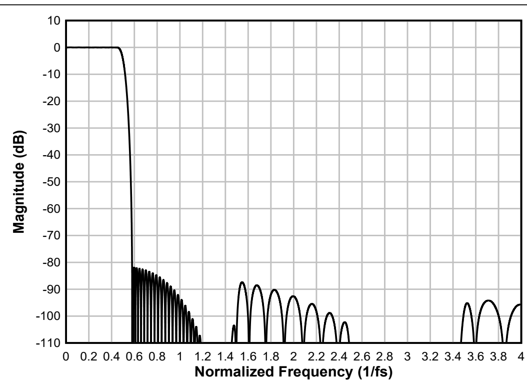

図 6-38. Linear Phase Interpolation Filter Magnitude Response

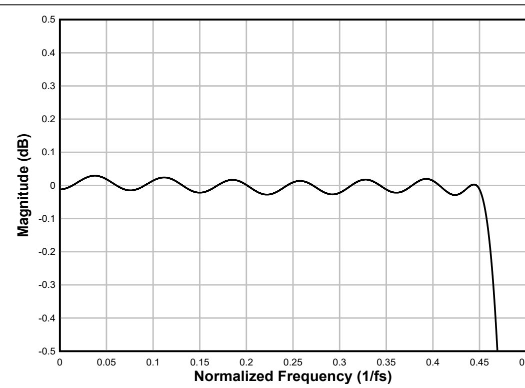

図 6-39. Linear Phase Interpolation Filter Pass-Band Ripple

表 6-32. Linear Phase Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.03	dB

表 6-32. Linear Phase Interpolation Filter Specifications (続き)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Stop-band attenuation	Frequency range is 0.58 × f_S to 4 × f_S	81.9			dB
	Frequency range is 4 × f_S to 15.42 × f_S	87.6			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		17.6		1/f_S

6.3.9.6.1.3 Sampling Rate: 32kHz or 29.4kHz

図 6-40 and 図 6-41 respectively show the magnitude response and the pass-band ripple for an interpolation filter with a sampling rate of 32kHz or 29.4kHz. 表 6-33 lists the specifications for an interpolation filter with a 32kHz or 29.4kHz sampling rate.

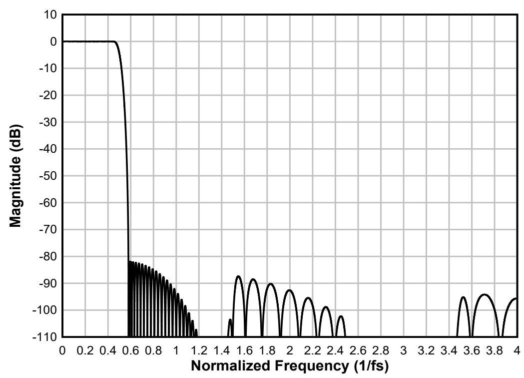

図 6-40. Linear Phase Interpolation Filter Magnitude Response

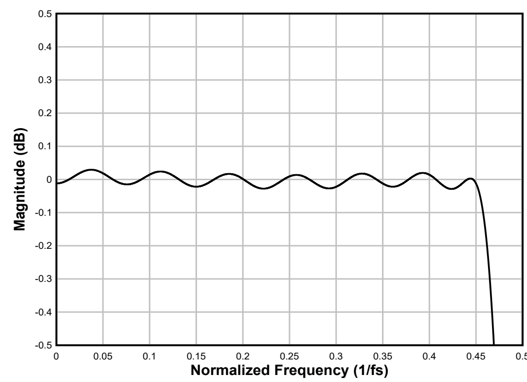

図 6-41. Linear Phase Interpolation Filter Pass-Band Ripple

表 6-33. Linear Phase Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.05		0.03	dB
Stop-band attenuation	Frequency range is 0.586 × f_S to 4 × f_S	81.9			dB
	Frequency range is 4 × f_S to 15.42 × f_S	87.6			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		17.6		1/f_S

6.3.9.6.1.4 Sampling Rate: 48kHz or 44.1kHz

図 6-42 and 図 6-43 respectively show the magnitude response and the pass-band ripple for an interpolation filter with a sampling rate of 48kHz or 44.1kHz. 表 6-34 lists the specifications for an interpolation filter with a 48kHz or 44.1kHz sampling rate.

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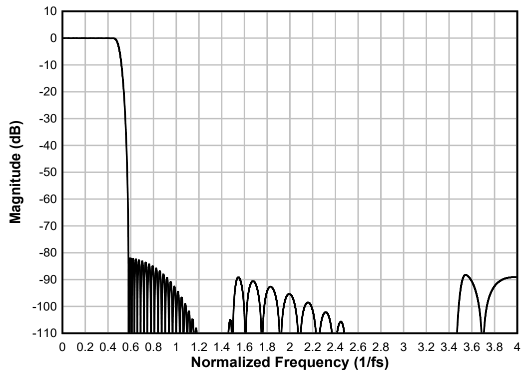

図 6-42. Linear Phase Interpolation Filter Magnitude Response

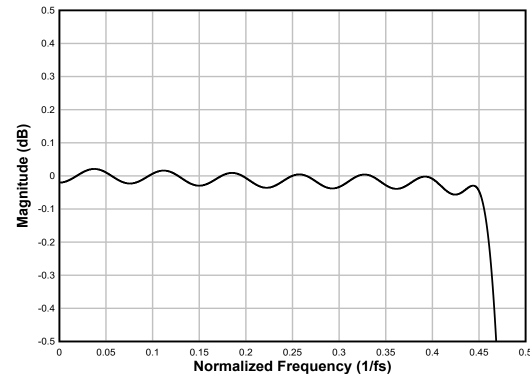

図 6-43. Linear Phase Interpolation Filter Pass-Band Ripple

表 6-34. Linear Phase Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.454 × f_S	–0.08		0.02	dB
Stop-band attenuation	Frequency range is 0.585 × f_S to 4 × f_S	82.0			dB
	Frequency range is 4 × f_S to 7.42 × f_S onwards	89.0			
Group delay or latency	Frequency range is 0 to 0.454 × f_S		17.3		1/f_S

6.3.9.6.1.5 Sampling Rate: 96kHz or 88.2kHz

図 6-44 and 図 6-45 respectively show the magnitude response and the pass-band ripple for an interpolation filter with a sampling rate of 96kHz or 88.2kHz. 表 6-35 lists the specifications for an interpolation filter with a 96kHz or 88.2kHz sampling rate.

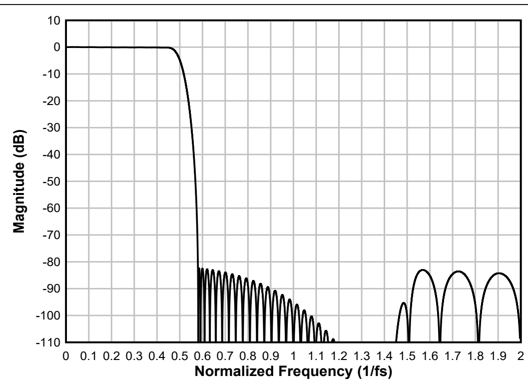

図 6-44. Linear Phase Interpolation Filter Magnitude Response

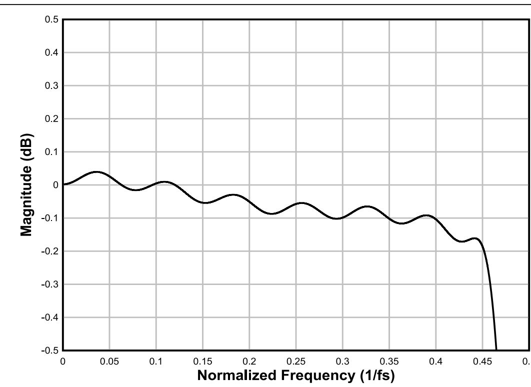

図 6-45. Linear Phase Interpolation Filter Pass-Band Ripple

表 6-35. Linear Phase Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.452 × f_S	–0.2		0.04	dB
Stop-band attenuation	Frequency range is 0.58 × f_S to 3.42 × f_S	82.4			dB
Group delay or latency	Frequency range is 0 to 0.454 × f_S		16.7		1/f_S

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6.3.9.6.1.6 Sampling Rate: 384kHz or 352.8kHz

図 6-46 and 図 6-47 respectively show the magnitude response and the pass-band ripple for an interpolation filter with a sampling rate of 384kHz or 352.8kHz. 表 6-36 lists the specifications for an interpolation filter with a 384kHz or 352.8kHz sampling rate.

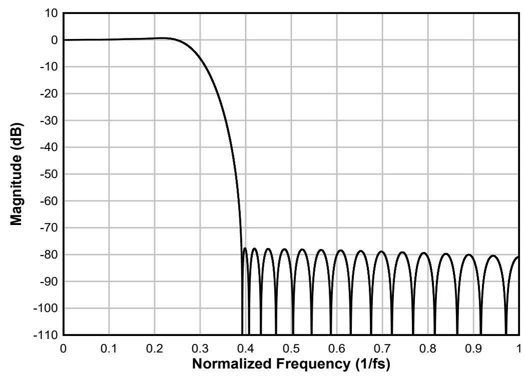

図 6-46. Linear Phase Interpolation Filter Magnitude Response

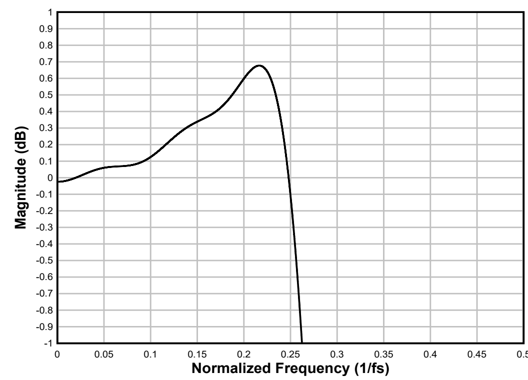

図 6-47. Linear Phase Interpolation Filter Pass-Band Ripple

表 6-36. Linear Phase Interpolation Filter Specifications

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Pass-band ripple	Frequency range is 0 to 0.245 × f_S	–0.03		0.67	dB
Stop-band attenuation	Frequency range is 0.391 × f_S to 1.61 × f_S	77.6			dB
Group delay or latency	Frequency range is 0 to 0.212 × f_S		10.7		1/f_S

6.3.10 Interrupts, Status, and Digital I/O Pin Multiplexing

Certain events in the device may require host processor intervention and can be used to trigger interrupts to the host processor. One such event is an audio serial interface (ASI) bus error. The device powers down the record channels if any faults are detected with the ASI bus error clocks, such as:

- Invalid FSYNC frequency
- Invalid SBCLK to FSYNC ratio
- Long pauses of the SBCLK or FSYNC clocks

When an ASI bus clock error is detected, the device shuts down all the record and playback channels as quickly as possible. After all ASI bus clock errors are resolved, the device volume ramps back to its previous state to recover the audio. During an ASI bus clock error, the internal interrupt request (IRQ) interrupt signal asserts low if the clock error interrupt mask register bit INT_MASK0[7] (P1_R47_D7) is set low. The clock fault is also available for readback in the latched fault status register bit INT_LTCH0 (P1_R52), which is a read-only register. Reading the latched fault status register, INT_LTCH0, clears all latched fault status. The device can be additionally configured to route the internal IRQ interrupt signal on the GPIOx or GPO1 pins and also can be configured as open-drain outputs so that these pins can be wire-ANDed to the open-drain interrupt outputs of other devices.

The IRQ interrupt signal can either be configured as active low or active high polarity by setting the INT_POL (P0_R66_D7) register bit. This signal can also be configured as a single pulse or a series of pulses by programming the INT_EVENT[1:0] (P0_R66_D[6:5]) register bits. If the interrupts are configured as a series of pulses, the events trigger the start of pulses that stop when the latched fault status register is read to determine the cause of the interrupt.

The device also supports read-only live-status registers to determine if the channels are powered up or down and if the device is in sleep mode or not. These status registers are located in the DEV_STS0 (P0_R121) and DEV_STS1 (P0_R122) register bits.

The device has a multifunctional GPIO1 pin that can be configured for a desired specific function. 表 6-37 lists all possible allocations of these multifunctional pins for the various features.

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表 6-37. Multifunction Pin Assignments

ROW	PIN FUNCTION	GPIO1	GPIO2	GPO1	GPI1
—	—	GPIO1_CFG	GPO2_CFG	GPO1_CFG	GPI1_CFG
—	—	P0_R10[7:4]	P0_R11[7:4]	P0_R12[7:4]	P0_R13[1]
A	Pin disabled	S[(1)]	S (default)	S (default)	S (default)
B	General-purpose output (GPO)	S	S	S	NS
C	Interrupt output (IRQ)	S (default)	S	S	NS
D	Power down for all ADC channels	S	S	NS	S
E	PDM clock output (PDMCLK)	S	S	S	NS
F	MiCBIAS on/off input (BIASEN)	S	S	NS	S
G	General-purpose input (GPI)	S	S	NS	S
H	Controller clock input (CCLK)	S	S	S	S
I	ASI daisy-chain input	S	S	NS	S
J	PDM data input 1 (PDMDIN1)	S	S	NS	S
K	PDM data input 2 (PDMDIN2)	S	S	NS	S
L	ASI DOUT	S	S	S	NS
M	ASI BCLK	S	S	S	S
N	ASI FSYNC	S	S	S	S
O	General Purpose Clock Out	S	S	S	NS
P	Incremental ADC Conversion Start	S	S	NS	S

(1) S means the feature mentioned in this row is *supported* for the respective GPIO1, GPOx, or GPIx pin mentioned in this column.

Each GPOx or GPIOx pin can be independently set for the desired drive configurations setting using the GPIOx_DRV[2:0] or GPO1_DRV[2:0] register bits. 表 6-38 lists the drive configuration settings.

表 6-38. GPIO or GPOx Pins Drive Configuration Settings

P0_R10_D[2:0] : GPIO1_DRV[2:0]	GPIO OUTPUT DRIVE CONFIGURATION SETTINGS FOR GPIO1
000	The GPIO1 pin is set to high impedance (floated)
001	The GPIO1 pin is set to be driven active low or active high
010 (default)	The GPIO1 pin is set to be driven active low or weak high (on-chip pullup)
011	The GPIO1 pin is set to be driven active low or Hi-Z (floated)
100	The GPIO1 pin is set to be driven weak low (on-chip pulldown) or active high
101	The GPIO1 pin is set to be driven Hi-Z (floated) or active high
110 and 111	Reserved (do not use these settings)

Similarly, the GPO1 pin can be configured using the GPO1_DRV(P0_R12) register bits.

When configured as a general-purpose output (GPO), the GPIOx or GPO1 pin values can be driven by writing the GPO_GPI_VAL (P0_R14) registers. The GPIO_MON bits (P0_R14_D[3:1]) can be used to readback the status of the GPIOx or GPI1 pin when configured as a general-purpose input (GPI).

7 Register Maps

This section describes the control registers for the device in detail. All these registers are eight bits in width and allocated to device configuration and programmable coefficients settings. These registers are mapped internally using a page scheme that can be controlled using either I^2C or SPI communication to the device. Each page contains 128 bytes of registers. All device configuration registers are stored in page 0, page 1 and page 3. Page 0 is the default page setting at power up (and after a software reset). The device current page can be switch to a new desired page by using the PAGE[7:0] bits located in register 0 of every page.

Do not read from or write to reserved pages or reserved registers. Write only default values for the reserved bits in the valid registers.

The procedure for register access across pages is:

- Select page N (write data *N* to register 0 regardless of the current page number)
- Read or write data from or to valid registers in page N
- Select the new page M (write data *M* to register 0 regardless of the current page number)
- Read or write data from or to valid registers in page M
- Repeat as needed

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7.1 Page 0 Registers

表 7-1 lists the memory-mapped registers for the Page 0 registers. All register offset addresses not listed in 表 7-1 should be considered as reserved locations and the register contents should not be modified.

表 7-1. PAGE 0 Registers

Address	Acronym	Register Name	Reset Value	Section
0x0	PAGE_CFG	Device page register	0x00	セクション 7.1.1
0x1	SW_RESET	Software reset register	0x00	セクション 7.1.2
0x2	VREF_CFG		0x00	セクション 7.1.3
0x3	AVDD_IOVDD_STS		0x00	セクション 7.1.4
0x4	MISC_CFG		0x00	セクション 7.1.5
0x5	MISC_CFG1		0x15	セクション 7.1.6
0x6	DAC_CFG_A0	DAC DEPOP configuration register	0x55	セクション 7.1.7
0x7	MISC_CFG0	Misc. configuration register	0x00	セクション 7.1.8
0xA	GPIO1_CFG0	GPIO1 configuration register 0	0x32	セクション 7.1.9
0xC	GPO1A_CFG0	GPO1A configuration register 0	0x00	セクション 7.1.10
0xD	GPI_CFG	GPI1 configuration register 0	0x00	セクション 7.1.11
0xE	GPO_GPI_VAL	GPIO, GPO output value register	0x00	セクション 7.1.12
0xF	INTF_CFG0	Interface configuration register 0	0x00	セクション 7.1.13
0x10	INTF_CFG1	Interface configuration register 1	0x52	セクション 7.1.14
0x11	INTF_CFG2	Interface configuration register 2	0x80	セクション 7.1.15
0x12	INTF_CFG3	Interface configuration register 3	0x00	セクション 7.1.16
0x13	INTF_CFG4	Interface configuration register 3	0x00	セクション 7.1.17
0x14	INTF_CFG5	Interface configuration register 4	0x00	セクション 7.1.18
0x15	INTF_CFG6	Interface configuration register 5	0x00	セクション 7.1.19
0x18	ASI_CFG0	ASI configuration register 0	0x40	セクション 7.1.20
0x19	ASI_CFG1	ASI configuration register 1	0x00	セクション 7.1.21
0x1A	PASI_CFG0	Primary ASI configuration register 0	0x30	セクション 7.1.22
0x1B	PASI_TX_CFG0	PASI TX configuration register 0	0x00	セクション 7.1.23
0x1C	PASI_TX_CFG1	PASI TX configuration register 1	0x00	セクション 7.1.24
0x1D	PASI_TX_CFG2	PASI TX configuration register 2	0x00	セクション 7.1.25
0x1E	PASI_TX_CH1_CFG	PASI TX Channel 1 configuration register	0x20	セクション 7.1.26
0x1F	PASI_TX_CH2_CFG	PASI TX Channel 2 configuration register	0x21	セクション 7.1.27
0x20	PASI_TX_CH3_CFG	PASI TX Channel 3 configuration register	0x02	セクション 7.1.28
0x21	PASI_TX_CH4_CFG	PASI TX Channel 4 configuration register	0x03	セクション 7.1.29
0x22	PASI_TX_CH5_CFG	PASI TX Channel 5 configuration register	0x04	セクション 7.1.30
0x23	PASI_TX_CH6_CFG	PASI TX Channel 6 configuration register	0x05	セクション 7.1.31
0x24	PASI_TX_CH7_CFG	PASI TX Channel 7 configuration register	0x06	セクション 7.1.32
0x25	PASI_TX_CH8_CFG	PASI TX Channel 8 configuration register	0x07	セクション 7.1.33
0x26	PASI_RX_CFG0	PASI RX configuration register 0	0x00	セクション 7.1.34
0x27	PASI_RX_CFG1	PASI RX configuration register 1	0x00	セクション 7.1.35
0x28	PASI_RX_CH1_CFG	PASI RX Channel 1 configuration register	0x20	セクション 7.1.36
0x29	PASI_RX_CH2_CFG	PASI RX Channel 2 configuration register	0x21	セクション 7.1.37
0x2A	PASI_RX_CH3_CFG	PASI RX Channel 3 configuration register	0x02	セクション 7.1.38
0x2B	PASI_RX_CH4_CFG	PASI RX Channel 4 configuration register	0x03	セクション 7.1.39

表 7-1. PAGE 0 Registers (続き)

Address	Acronym	Register Name	Reset Value	Section
0x2C	PASI_RX_CH5_CFG	PASI RX Channel 5 configuration register	0x04	セクション 7.1.40
0x2D	PASI_RX_CH6_CFG	PASI RX Channel 6 configuration register	0x05	セクション 7.1.41
0x2E	PASI_RX_CH7_CFG	PASI RX Channel 7 configuration register	0x06	セクション 7.1.42
0x2F	PASI_RX_CH8_CFG	PASI RX Channel 8 configuration register	0x07	セクション 7.1.43
0x32	CLK_CFG0	Clock configuration register 0	0x00	セクション 7.1.44
0x33	CLK_CFG1	Clock configuration register 1	0x00	セクション 7.1.45
0x34	CLK_CFG2	Clock configuration register 2	0x40	セクション 7.1.46
0x35	CNT_CLK_CFG0	controller mode clock configuration register 0	0x00	セクション 7.1.47
0x36	CNT_CLK_CFG1	controller mode clock configuration register 1	0x00	セクション 7.1.48
0x37	CNT_CLK_CFG2	controller mode clock configuration register 2	0x20	セクション 7.1.49
0x38	CNT_CLK_CFG3	controller mode clock configuration register 3	0x00	セクション 7.1.50
0x39	CNT_CLK_CFG4	controller mode clock configuration register 4	0x00	セクション 7.1.51
0x3A	CNT_CLK_CFG5	controller mode clock configuration register 5	0x00	セクション 7.1.52
0x3B	CNT_CLK_CFG6	controller mode clock configuration register 6	0x00	セクション 7.1.53
0x3C	CLK_ERR_STS0	Clock error and status register 0	0x00	セクション 7.1.54
0x3D	CLK_ERR_STS1	Clock error and status register 1	0x00	セクション 7.1.55
0x3E	CLK_DET_STS0	Clock ratio detection register 0	0x00	セクション 7.1.56
0x3F	CLK_DET_STS1	Clock ratio detection register 1	0x00	セクション 7.1.57
0x40	CLK_DET_STS2	Clock ratio detection register 2	0x00	セクション 7.1.58
0x41	CLK_DET_STS3	Clock ratio detection register 3	0x00	セクション 7.1.59
0x42	INT_CFG	Interrupt configuration register	0x00	セクション 7.1.60
0x43	DAC_FLT_CFG	Interrupt configuration register	0x50	セクション 7.1.61
0x4B	ADC_DAC_MISC_CFG	ADC overload Response configuration register	0x00	セクション 7.1.62
0x4D	VREF_CFG	Power tune configuration register 0	0x00	セクション 7.1.3
0x4E	PWR_TUNE_CFG0	Power tune configuration register 0	0x00	セクション 7.1.63
0x4F	PWR_TUNE_CFG1	Power tune configuration register 1	0x00	セクション 7.1.64
0x50	ADC_CH1_CFG0	ADC Channel 1 configuration register 0	0x00	セクション 7.1.65
0x52	ADC_CH1_CFG2	ADC Channel 1 configuration register 2	0xA1	セクション 7.1.66
0x53	ADC_CH1_CFG3	ADC Channel 1 configuration register 3	0x80	セクション 7.1.67
0x54	ADC_CH1_CFG4	ADC Channel 1 configuration register 4	0x00	セクション 7.1.68
0x55	ADC_CH2_CFG0	ADC Channel 2 configuration register 0	0x00	セクション 7.1.69
0x57	ADC_CH2_CFG2	Channel 2 configuration register 2	0xA1	セクション 7.1.70
0x58	ADC_CH2_CFG3	ADC Channel 2 configuration register 3	0x80	セクション 7.1.71
0x59	ADC_CH2_CFG4	ADC Channel 2 configuration register 4	0x00	セクション 7.1.72
0x5A	ADC_CH3_CFG0	ADC Channel 3 configuration register 0	0x00	セクション 7.1.73
0x5B	ADC_CH3_CFG2	ADC Channel 3 configuration register 2	0xA1	セクション 7.1.74
0x5C	ADC_CH3_CFG3	ADC Channel 3 configuration register 3	0x80	セクション 7.1.75
0x5D	ADC_CH3_CFG4	ADC Channel 3 configuration register 4	0x00	セクション 7.1.76
0x5E	ADC_CH4_CFG0	ADC Channel 4 configuration register 0	0x00	セクション 7.1.77
0x5F	ADC_CH4_CFG2	Channel 4 configuration register 2	0xA1	セクション 7.1.78
0x60	ADC_CH4_CFG3	ADC Channel 4 configuration register 3	0x80	セクション 7.1.79
0x61	ADC_CH4_CFG4	ADC Channel 4 configuration register 4	0x00	セクション 7.1.80

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表 7-1. PAGE 0 Registers (続き)

Address	Acronym	Register Name	Reset Value	Section
0x64	OUT1x_CFG0	Channel OUT1x configuration register 0	0x20	セクション 7.1.81
0x65	OUT1x_CFG1	Channel OUT1x configuration register 1	0x20	セクション 7.1.82
0x66	OUT1x_CFG2	Channel OUT2x configuration register 2	0x20	セクション 7.1.83
0x67	DAC_CH1A_CFG0	DAC Channel 1A configuration register 0	0xC9	セクション 7.1.84
0x68	DAC_CH1A_CFG1	DAC Channel 1A configuration register 1	0x80	セクション 7.1.85
0x69	DAC_CH1B_CFG0	DAC Channel 1B configuration register 0	0xC9	セクション 7.1.86
0x6A	DAC_CH1B_CFG1	DAC Channel 1B configuration register 1	0x80	セクション 7.1.87
0x6B	OUT2x_CFG0	Channel OUT2x configuration register 0	0x20	セクション 7.1.88
0x6C	OUT2x_CFG1	Channel OUT2x configuration register 1	0x20	セクション 7.1.89
0x6D	OUT2x_CFG2	Channel OUT2x configuration register 2	0x20	セクション 7.1.90
0x6E	DAC_CH2A_CFG0	DAC Channel 2A configuration register 0	0xC9	セクション 7.1.91
0x6F	DAC_CH2A_CFG1	DAC Channel 2A configuration register 1	0x80	セクション 7.1.92
0x70	DAC_CH2B_CFG0	DAC Channel 2B configuration register 0	0xC9	セクション 7.1.93
0x71	DAC_CH2B_CFG1	DAC Channel 2B configuration register 1	0x80	セクション 7.1.94
0x72	DSP_CFG0	DSP configuration register 0	0x18	セクション 7.1.95
0x73	DSP_CFG1	DSP configuration register 0	0x18	セクション 7.1.96
0x76	CH_EN	Channel enable configuration register	0xCC	セクション 7.1.97
0x77	DYN_PUPD_CFG	Power up configuration register	0x00	セクション 7.1.98
0x78	PWR_CFG	Power up configuration register	0x00	セクション 7.1.99
0x79	DEV_STS0	Device status value register 0	0x00	セクション 7.1.100
0x7A	DEV_STS1	Device status value register 1	0x80	セクション 7.1.101
0x7E	I2C_CKSUM	I^{2}C checksum register	0x00	セクション 7.1.102

7.1.1 PAGE_CFG Register (Address = 0x0) [Reset = 0x00]

PAGE_CFG is shown in 図 7-1 and described in 表 7-2.

Return to the Summary Table.

The device memory map is divided into pages. This register sets the page.

図 7-1. PAGE_CFG Register

7	6	5	4	3	2	1	0
PAGE[7:0]							
R/W-00000000b							

表 7-2. PAGE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	R/W	0x0	These bits set the device page. 0d = Page 0 1d = Page 1 2d to 254d = Page 2 to page 254 respectively 255d = Page 255

7.1.2 SW_RESET Register (Address = 0x1) [Reset = 0x00]

SW_RESET is shown in 図 7-2 and described in 表 7-3.

Return to the Summary Table.

This register is the software reset register. Asserting a software reset places all register values in their default power-on-reset (POR) state.

図 7-2. SW_RESET Register

7	6	5	4	3	2	1	0
RESERVED							SW_RESET
R-0000000b							R/W-0b

表 7-3. SW_RESET Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	RESERVED	R	0x0	Reserved bits; Write only reset value
0	SW_RESET	R/W	0x0	Software reset. This bit is self clearing. 0d = Do not reset 1d = Reset all registers to their reset values

7.1.3 VREF_CFG Register (Address = 0x2) [Reset = 0x00]

VREF_CFG is shown in 図 7-3 and described in 表 7-4.

Return to the Summary Table.

図 7-3. VREF_CFG Register

7	6	5	4	3	2	1	0
RESERVED		VREF_QCHG[1:0]		SLEEP_EXIT_VREF_EN	AVDD_MODE	IOVDD_IO_MODE	SLEEP_ENZ
R-00b		R/W-00b		R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 7-4. VREF_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved bits; Write only reset values
5-4	VREF_QCHG[1:0]	R/W	0x0	The duration of the quick-charge for the VREF external capacitor is set using an internal series impedance of 200 Ω. 0d = VREF quick-charge duration of 3.5 ms (typical) 1d = VREF quick-charge duration of 10 ms (typical) 2d = VREF quick-charge duration of 50 ms (typical) 3d = VREF quick-charge duration of 100 ms (typical)
3	SLEEP_EXIT_VREF_EN	R/W	0x0	Sleep mode exit configuration 0d = Only DREG Enabled 1d = DREG and VREF enabled
2	AVDD_MODE	R/W	0x0	AVDD mode configuration. 0d = Internal AREG regulator is used (Should be used for AVDD > 2V) 1d = AVDD 1.8V used directly for AREG (Strictly use this setting for AVDD 1.7V-1.9V)
1	IOVDD_IO_MODE	R/W	0x0	IOVDD mode configuration. 0d = IOVDD at 3.3V / 1.8V / 1.2V (speed limitation applicable for 1.8V and 1.2V) 1d = IOVDD at 1.8V / 1.2V only (no speed limitation - Strictly don't use this setting for IOVDD > 2V).

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表 7-4. VREF_CFG Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
0	SLEEP_ENZ	R/W	0x0	Sleep mode setting. 0d = Device is in sleep mode 1d = Device is not in sleep mode

7.1.4 AVDD_IOVDD_STS Register (Address = 0x3) [Reset = 0x00]

AVDD_IOVDD_STS is shown in 図 7-4 and described in 表 7-5.

Return to the Summary Table.

図 7-4. AVDD_IOVDD_STS Register

7	6	5	4	3	2	1	0
AVDD_MODE_STS	IOVDD_IO_MODE_STS	RESERVED				BRWNOUT_SHDN_STS	BRWNOUT_SHDN_EXIT_SLEEP
R-0b	R-0b	R-0000b				R-0b	R/W-0b

表 7-5. AVDD_IOVDD_STS Register Field Descriptions

Bit	Field	Type	Reset	Description
7	AVDD_MODE_STS	R	0x0	AVDD mode status flag register. 0d = AVDD_MODE as per configured 1d = AVDD > 2V (AVDD_MODE forced to 0d)
6	IOVDD_IO_MODE_STS	R	0x0	IOVDD mode status flag register. 0d = IOVDD_MODE as per configured 1d = IOVDD > 2V (IOVDD_IO_MODE forced to 0d)
5-2	RESERVED	R	0x0	Reserved bits; Write only reset values
1	BRWNOUT_SHDN_STS	R	0x0	Brwnout shutdown status 0d = No brwnout shutdown 1d = Brwnout shutdown
0	BRWNOUT_SHDN_EXIT_SLEEP	R/W	0x0	Brwnout shutdown sleep exit config 0d = Stay in sleep mode 1d = Exit sleep mode

7.1.5 MISC_CFG Register (Address = 0x4) [Reset = 0x00]

MISC_CFG is shown in 図 7-5 and described in 表 7-6.

Return to the Summary Table.

図 7-5. MISC_CFG Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	I2C_BRDCAST_EN	RESERVED
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R/W-0b	R-0b

表 7-6. MISC_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved bit; Write only reset value
6	RESERVED	R	0x0	Reserved bit; Write only reset value
5	RESERVED	R	0x0	Reserved bit; Write only reset value
4	RESERVED	R	0x0	Reserved bit; Write only reset value
3	RESERVED	R	0x0	Reserved bit; Write only reset value

表 7-6. MISC_CFG Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
2	RESERVED	R	0x0	Reserved bit; Write only reset value
1	I2C_BRDCAST_EN	R/W	0x0	I^2C broadcast addressing setting. 0d = I^2C broadcast mode disabled 1d = I^2C broadcast mode enabled; the I^2C target address is fixed with pin-controlled LSB bits as '0'
0	RESERVED	R	0x0	Reserved bit; Write only reset value

7.1.6 MISC_CFG1 Register (Address = 0x5) [Reset = 0x15]

MISC_CFG1 is shown in 図 7-6 and described in 表 7-7.

Return to the Summary Table.

図 7-6. MISC_CFG1 Register

7	6	5	4	3	2	1	0
INCAP_QCHG[1:0]		SHDN_CFG[1:0]		DREG_KA_TIME[1:0]		RESERVED	
R/W-00b		R/W-01b		R/W-01b		R-00b	

表 7-7. MISC_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	INCAP_QCHG[1:0]	R/W	0x0	The duration of the quick-charge for the external AC-coupling capacitor is set using an internal series impedance of 800 Ω. 0d = INxP, INxM quick-charge duration of 2.5 ms (typical) 1d = INxP, INxM quick-charge duration of 12.5 ms (typical) 2d = INxP, INxM quick-charge duration of 25 ms (typical) 3d = INxP, INxM quick-charge duration of 50 ms (typical)
5-4	SHDN_CFG[1:0]	R/W	0x1	Shutdown configuration. 0d = DREG is powered down immediately after IOVDD is deasserted 1d = DREG remains active to enable a clean shut down until a time-out(DREG_KA_TIME) is reached; after the time-out period, DREG is forced to power off 2d = DREG remains active until the device cleanly shuts down 3d = Reserved; Don't use
3-2	DREG_KA_TIME[1:0]	R/W	0x1	These bits set how long DREG remains active after IOVDD is deasserted. 0d = DREG remains active for 30 ms (typical) 1d = DREG remains active for 25 ms (typical) 2d = DREG remains active for 10 ms (typical) 3d = DREG remains active for 5 ms (typical)
1-0	RESERVED	R	0x0	Reserved bits; Write only reset values

7.1.7 DAC_CFG_A0 Register (Address = 0x6) [Reset = 0x55]

DAC_CFG_A0 is shown in 図 7-7 and described in 表 7-8.

Return to the Summary Table.

This register configures the device DAC DEPOP

図 7-7. DAC_CFG_A0 Register

7	6	5	4	3	2	1	0
RSERIES_DE_POP[3:0]				PWR_UP_TIME_DE_POP[3:0]			
R/W-0101b				R/W-0101b			

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表 7-8. DAC_CFG_A0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	RSERIES_DE_POP[3:0]	R/W	0x5	HP Amp series resistor select config. 0d = Open 1d = 1K 2d = 2.5K 3d = 0.715k 4d = 10K 5d = 0.91k 6d = 2K 7d = 0.667k 8d = 20K Dont use Dont use Dont use Dont use Dont use Dont use Dont use
3-0	PWR_UP_TIME_DE_POP[3:0]	R/W	0x5	HP Amp external cap charging time config. 0d = 2ms 1d = 4ms 2d = 8ms 3d = 16ms 4d = 50ms 5d = 100ms 6d = 250ms 7d = 500ms 8d = 1s 9d = 5s 10d-15d = Reserved

7.1.8 MISC_CFG0 Register (Address = 0x7) [Reset = 0x00]

MISC_CFG0 is shown in 図 7-8 and described in 表 7-9.

Return to the Summary Table.

This register configures the device Misc.

図 7-8. MISC_CFG0 Register

7	6	5	4	3	2	1	0
DAC_ST_W_CAP_DIS	DAC_DLYD_PWRUP	DAC_DLYD_PWRUP_TIME	HW_RESET_ON_CLK_STOP_EN	RESERVED			
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R-0000b			

表 7-9. MISC_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DAC_ST_W_CAP_DIS	R/W	0x0	DAC start with dc blocking capacitor discharge sequence. 0d = disable 1d = enable
6	DAC_DLYD_PWRUP	R/W	0x0	DAC power up delayed config. 0d = disable 1d = enable (Delay power-up by based on DAC_DLYD_PWRUP_TIME config)
5	DAC_DLYD_PWRUP_TIME	R/W	0x0	DAC power up delayed time config. 0d = 64-128ms 1d = 256-512ms

表 7-9. MISC_CFG0 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
4	HW_RESET_ON_CLK_STOP_EN	R/W	0x0	Assertion of Hard Reset when clock selected by CLK_SRC_SEL is not available for 2ms config 0d = disable 1d = enable
3-0	RESERVED	R	0x0	Reserved bits; Write only reset values

7.1.9 GPIO1_CFG0 Register (Address = 0xA) [Reset = 0x32]

GPIO1_CFG0 is shown in 図 7-9 and described in 表 7-10.

Return to the Summary Table.

This register is the GPIO1 configuration register 0.

図 7-9. GPIO1_CFG0 Register

7	6	5	4	3	2	1	0
GPIO1_CFG[3:0]				RESERVED	GPIO1_DRV[2:0]		
R/W-0011b				R-0b	R/W-010b		

表 7-10. GPIO1_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPIO1_CFG[3:0]	R/W	0x3	GPIO1 configuration. 0d = GPIO1 is disabled 1d = GPIO1 is configured as a general-purpose input (GPI) or any other input function 2d = GPIO1 is configured as a general-purpose output (GPO) 3d = GPIO1 is configured as a chip interrupt output (IRQ) 4d = GPIO1 is configured as a PDM clock output (PDMCLK) 5d = GPIO1 is configured as primary ASI DOUT 6d = GPIO1 is configured as primary ASI DOUT2 7d = GPIO1 is configured as secondary ASI DOUT 8d = GPIO1 is configured as secondary ASI DOUT2 9d = GPIO1 is configured as secondary ASI BCLK output 10d = GPIO1 is configured as secondary ASI FSYNC output 11d = GPIO1 is configured as general purpose CLKOUT 12d = GPIO1 is configured as PASI DOUT and SASI DOUT muxed 13d = GPIO1 is configured as DAISY_OUT for DIN Daisy 14d to 15d = Reserved
3	RESERVED	R	0x0	Reserved bit; Write only reset value
2-0	GPIO1_DRV[2:0]	R/W	0x2	GPIO1 output drive configuration. (Not valid if GPIO1_CFG configured as I^2S out) 0d = Hi-Z output 1d = Drive active low and active high 2d = Drive active low and weak high 3d = Drive active low and Hi-Z 4d = Drive weak low and active high 5d = Drive Hi-Z and active high 6d to 7d = Reserved; Don't use

7.1.10 GPO1A_CFG0 Register (Address = 0xC) [Reset = 0x00]

GPO1A_CFG0 is shown in 図 7-10 and described in 表 7-11.

Return to the Summary Table.

This register is the GPO1 configuration register 0.

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図 7-10. GPO1A_CFG0 Register

7	6	5	4	3	2	1	0
GPO1A_CFG[3:0]				SPI_POCI_CFG	GPO1A_DRV[2:0]		
R/W-0000b				R/W-0b	R/W-000b		

表 7-11. GPO1A_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	GPO1A_CFG[3:0]	R/W	0x0	GPO1A configuration.(Max frequency is limited to 6MHz. For SPI mode, this pin act as POCI and the below configuration settings are not applicable) (Buskeeper en is not supported when used as DOUT) 0d = GPO1A is disabled 1d = GPO1A is configured as a general-purpose input (GPI) or any other input function 2d = GPO1A is configured as a general-purpose output (GPO) 3d = GPO1A is configured as a chip interrupt output (IRQ) 4d = GPO1A is configured as a PDM clock output (PDMCLK) 5d = GPO1A is configured as primary ASI DOUT 6d = GPO1A is configured as primary ASI DOUT2 7d = GPO1A is configured as secondary ASI DOUT 8d = GPO1A is configured as secondary ASI DOUT2 9d = GPO1A is configured as secondary ASI BCLK output 10d = GPO1A is configured as secondary ASI FSYNC output 11d = GPO1A is configured as general purpose CLKOUT 12d = GPO1A is configured as PASI DOUT and SASI DOUT muxed 13d = GPO1A is configured as DAISY_OUT for DIN Daisy 14d to 15d = Reserved
3	SPI_POCI_CFG	R/W	0x0	SPI POCI configuration. 0d = GPO1A pin act as SPI POCI output (max frequency limited to 6MHz) and GPO1A_CFG and GPO1A_DRV settings are ignored. 0d = GPIO1A pin act as SPI POCI output for high speed use case and GPIO1A_CFG and GPIO1A_DRV settings are ignored.
2-0	GPO1A_DRV[2:0]	R/W	0x0	GPO1A output drive configuration. (Not valid if GPO1A_CFG configured as I^{2}S out) (This is GPO1A in Auto-device but max frequency is limited to 6MHz. For SPI mode, this pin act as SSZ and the below configuration settings are not applicable) 0d = Hi-Z output 1d = Drive active low and active high 2d = Drive active low and weak high 3d = Drive active low and Hi-Z 4d = Drive weak low and active high 5d = Drive Hi-Z and active high 6d to 7d = Reserved; Don't use

7.1.11 GPI_CFG Register (Address = 0xD) [Reset = 0x00]

GPI_CFG is shown in 図 7-11 and described in 表 7-12.

Return to the Summary Table.

This register is the GPI1 configuration register 0.

図 7-11. GPI_CFG Register

7	6	5	4	3	2	1	0
RESERVED						GPI1A_CFG	GPI2A_CFG
R-000000b						R/W-0b	R/W-0b

表 7-12. GPI_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	0x0	Reserved bits; Write only reset values
1	GPI1A_CFG	R/W	0x0	GPI1A configuration. 0d = GPI1A is disabled 1d = GPI1A is configured as a general-purpose input (GPI) or any other input function
0	GPI2A_CFG	R/W	0x0	GPI2A configuration. 0d = GPI2A is disabled 1d = GPI2A is configured as a general-purpose input (GPI) or any other input function

7.1.12 GPO_GPI_VAL Register (Address = 0xE) [Reset = 0x00]

GPO_GPI_VAL is shown in 図 7-12 and described in 表 7-13.

Return to the Summary Table.

This register is the GPIO and GPO output value register.

図 7-12. GPO_GPI_VAL Register

7	6	5	4	3	2	1	0
GPIO1_VAL	RESERVED	GPO1A_VAL	RESERVED	GPIO1_MON	GPI2A_MON	GPI1A_MON	RESERVED
R/W-0b	R-0b	R/W-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 7-13. GPO_GPI_VAL Register Field Descriptions

Bit	Field	Type	Reset	Description
7	GPIO1_VAL	R/W	0x0	GPIO1 output value when configured as a GPO. 0d = Drive the output with a value of 0 1d = Drive the output with a value of 1
6	RESERVED	R	0x0	Reserved bit; Write only reset value
5	GPO1A_VAL	R/W	0x0	GPO1A output value when configured as a GPO. 0d = Drive the output with a value of 0 1d = Drive the output with a value of 1
4	RESERVED	R	0x0	Reserved bit; Write only reset value
3	GPIO1_MON	R	0x0	GPIO1 monitor value when configured as a GPI. 0d = Input monitor value 0 1d = Input monitor value 1
2	GPI2A_MON	R	0x0	GPI2A monitor value when configured as a GPI. 0d = Input monitor value 0 1d = Input monitor value 1
1	GPI1A_MON	R	0x0	GPI1A monitor value when configured as a GPI. 0d = Input monitor value 0 1d = Input monitor value 1
0	RESERVED	R	0x0	Reserved bit; Write only reset value

7.1.13 INTF_CFG0 Register (Address = 0xF) [Reset = 0x00]

INTF_CFG0 is shown in 図 7-13 and described in 表 7-14.

Return to the Summary Table.

This register is the interface configuration register 0.

図 7-13. INTF_CFG0 Register

7	6	5	4	3	2	1	0

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図 7-13. INTF_CFG0 Register (続き)

RESERVED	CCLK_SEL[1:0]	PASI_DIN2_SEL[2:0]	PASI_BCLK_SEL	PASI_FSYNC_SEL
R-0b	R/W-00b	R/W-000b	R/W-0b	R/W-0b

表 7-14. INTF_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved bit; Write only reset value
6-5	CCLK_SEL[1:0]	R/W	0x0	CCLK select configuration. 0d = cclk is disabled 1d = GPIO1 2d = GPI2A 3d = GPI1A
4-2	PASI_DIN2_SEL[2:0]	R/W	0x0	Primary ASI DIN2 select configuration. 0d = Primary ASI DIN2 is disabled 1d = GPIO1 2d = GPI2A 3d = GPI1A 4d = DOUT 5d = Primary ASI DIN 6d to 7d = Reserved
1	PASI_BCLK_SEL	R/W	0x0	Primary ASI BCLK select configuration. 0d = Primary ASI BCLK is BCLK 1d = Primary ASI BCLK is Secondary ASI BCLK
0	PASI_FSYNC_SEL	R/W	0x0	Primary ASI FSYNC select configuration. 0d = Primary ASI FSYNC is FSYNC 1d = Primary ASI FSYNC is Secondary ASI FSYNC

7.1.14 INTF_CFG1 Register (Address = 0x10) [Reset = 0x52]

INTF_CFG1 is shown in 図 7-14 and described in 表 7-15.

Return to the Summary Table.

This register is the interface configuration register 1.

図 7-14. INTF_CFG1 Register

7	6	5	4	3	2	1	0
DOUT_SEL[3:0]				DOUT_VAL	DOUT_DRV[2:0]		
R/W-0101b				R/W-0b	R/W-010b		

表 7-15. INTF_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DOUT_SEL[3:0]	R/W	0x5	DOUT select configuration. 0d = DOUT is disabled 1d = DOUT is configured as input 2d = DOUT is configured as a general-purpose output (GPO) 3d = DOUT is configured as a chip interrupt output (IRQ) 4d = DOUT is configured as a PDM clock output (PDMCLK) 5d = DOUT is configured as primary ASI DOUT 6d = DOUT is configured as primary ASI DOUT2 7d = DOUT is configured as secondary ASI DOUT 8d = DOUT is configured as secondary ASI DOUT2 9d = DOUT is configured as secondary ASI BCLK output 10d = DOUT is configured as secondary ASI FSYNC output 11d = DOUT is configured as general purpose CLKOUT 12d = DOUT is configured as PASI DOUT and SASI DOUT muxed 13d = DOUT is configured as DAISY_OUT for DIN Daisy 14d = DOUT is configured as DIN(LOOPBACK) 15d = Reserved
3	DOUT_VAL	R/W	0x0	DOUT output value when configured as a GPO. 0d = Drive the output with a value of 0 1d = Drive the output with a value of 1
2-0	DOUT_DRV[2:0]	R/W	0x2	DOUT output drive configuration. 0d = Hi-Z output 1d = Drive active low and active high 2d = Drive active low and weak high 3d = Drive active low and Hi-Z 4d = Drive weak low and active high 5d = Drive Hi-Z and active high 6d to 7d = Reserved; Don't use

7.1.15 INTF_CFG2 Register (Address = 0x11) [Reset = 0x80]

INTF_CFG2 is shown in 図 7-15 and described in 表 7-16.

Return to the Summary Table.

This register is the interface configuration register 2.

図 7-15. INTF_CFG2 Register

7	6	5	4	3	2	1	0
PASI_DIN_EN	SASI_FSYNC_SEL[2:0]			SASI_BCLK_SEL[2:0]			RESERVED
R/W-1b	R/W-000b			R/W-000b			R-0b

表 7-16. INTF_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PASI_DIN_EN	R/W	0x1	Primary ASI DIN enable configuration. 0d = Primary ASI DIN is disabled 1d = Primary ASI DIN is enabled
6-4	SASI_FSYNC_SEL[2:0]	R/W	0x0	Secondary ASI FSYNC select configuration. 0d = Secondary ASI disabled 1d = GPIO1 2d = GPI2A 3d = GPI1A 4d = Reserved 5d = Primary ASI FSYNC 6d to 7d = Reserved

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表 7-16. INTF_CFG2 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
3-1	SASI_BCLK_SEL[2:0]	R/W	0x0	Secondary ASI BCLK select configuration. 0d = Secondary ASI disabled 1d = GPIO1 2d = GPI2A 3d = GPI1A 4d = Reserved 5d = Primary ASI BCLK 6d to 7d = Reserved
0	RESERVED	R	0x0	Reserved bit; Write only reset value

7.1.16 INTF_CFG3 Register (Address = 0x12) [Reset = 0x00]

INTF_CFG3 is shown in 図 7-16 and described in 表 7-17.

Return to the Summary Table.

This register is the interface configuration register 3.

図 7-16. INTF_CFG3 Register

7	6	5	4	3	2	1	0
SASI_DIN_SEL[2:0]			SASI_DIN2_SEL[2:0]			RESERVED	
R/W-000b			R/W-000b			R-00b	

表 7-17. INTF_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	SASI_DIN_SEL[2:0]	R/W	0x0	Secondary ASI DIN select configuration. 0d = Seondary ASI DIN is disabled 1d = GPIO1 2d = GPI2A 3d = GPI1A 4d = DOUT 5d = Primary ASI DIN 6d to 7d = Reserved
4-2	SASI_DIN2_SEL[2:0]	R/W	0x0	Seondary ASI DIN2 select configuration. 0d = Seondary ASI DIN2 is disabled 1d = GPIO1 2d = GPI2A 3d = GPI1A 4d = DOUT 5d = Primary ASI DIN 6d to 7d = Reserved
1-0	RESERVED	R	0x0	Reserved bits; Write only reset values

7.1.17 INTF_CFG4 Register (Address = 0x13) [Reset = 0x00]

INTF_CFG4 is shown in 図 7-17 and described in 表 7-18.

Return to the Summary Table.

This register is the interface configuration register 3.

図 7-17. INTF_CFG4 Register

7	6	5	4	3	2	1	0
PDM_CH1_SEL	PDM_CH2_SEL	PDMDIN1_EDGE	PDMDIN2_EDGE	PDM_DIN1_SEL[1:0]		PDM_DIN2_SEL[1:0]	
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-00b		R/W-00b	

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図 7-17. INTF_CFG4 Register (続き)

表 7-18. INTF_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PDM_CH1_SEL	R/W	0x0	PDM select configuration for channel 1 of record path. 0d = Channel 1 is analog (ADC) type on the record path 1d = Channel 1 is digital (PDM) type on the record path
6	PDM_CH2_SEL	R/W	0x0	PDM select configuration for channel 2 of record path. 0d = Channel 2 is analog (ADC) type on the record path 1d = Channel 2 is digital (PDM) type on the record path
5	PDMDIN1_EDGE	R/W	0x0	PDMCLK latching edge used for channel 1 and channel 2 data. 0d = Channel 1 data are latched on the negative edge, channel 2 data are latched on the positive edge 1d = Channel 1 data are latched on the positive edge, channel 2 data are latched on the negative edge
4	PDMDIN2_EDGE	R/W	0x0	PDMCLK latching edge used for channel 3 and channel 4 data. 0d = Channel 3 data are latched on the negative edge, channel 4 data are latched on the positive edge 1d = Channel 3 data are latched on the positive edge, channel 4 data are latched on the negative edge
3-2	PDM_DIN1_SEL[1:0]	R/W	0x0	PDM data channels 1 and 2 select configuration. 0d = PDM data channels 1 and 2 are disabled 1d = GPIO1 2d = GPI2A 3d = GPI1A
1-0	PDM_DIN2_SEL[1:0]	R/W	0x0	PDM data channels 3 and 4 select configuration. 0d = PDM data channels 3 and 4 are disabled 1d = GPIO1 2d = GPI2A 3d = GPI1A

7.1.18 INTF_CFG5 Register (Address = 0x14) [Reset = 0x00]

INTF_CFG5 is shown in 図 7-18 and described in 表 7-19.

Return to the Summary Table.

This register is the interface configuration register 4.

図 7-18. INTF_CFG5 Register

7	6	5	4	3	2	1	0
PDM_DIN_SEL_OVRD	DOUT_WITH_DIN	PD_ADC_GPIO[1:0]		PD_DAC_GPIO[1:0]		PLIM_GPIO	GPA_GPIO
R/W-0b	R/W-0b	R/W-00b		R/W-00b		R/W-0b	R/W-0b

表 7-19. INTF_CFG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PDM_DIN_SEL_OVRD	R/W	0x0	PDM data channels (1 and 2)/(3 and 4) select configuration override. 0d = No Override 1d = PDM_DIN1/2_SEL if configured as GPI1 will be overriden as DIN
6	DOUT_WITH_DIN	R/W	0x0	DOUT used as both ASI OUT and ASI IN 0d = DOUT based on DOUT_SEL 1d = DOUT used as both ASI OUT and ASI DIN

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表 7-19. INTF_CFG5 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
5-4	PD_ADC_GPIO[1:0]	R/W	0x0	Power down ADC using GPIO select configuration.(ADC powered down if any one of the PD_ADC_GPIO/ADC_PDZ is configured power down) 0d = Power down ADC using GPIO is disabled 1d = Power down ADC using GPIO1 2d = Power down ADC using GPI2A 3d = Power down ADC using GPI1A
3-2	PD_DAC_GPIO[1:0]	R/W	0x0	Power down DAC using GPIO select configuration.(DAC powered down if any one of the PD_DAC_GPIO/DAC_PDZ is configured power down) 0d = Power down DAC using GPIO is disabled 1d = Power down DAC using GPIO1 2d = Power down DAC using GPI2A 3d = Power down DAC using GPI1A
1	PLIM_GPIO	R/W	0x0	PLIM using GPIO1 configuration. 0d = PLIM using GPIO1 is disabled 1d = PLIM using GPIO1
0	GPA_GPIO	R/W	0x0	GPA using GPIO1 configuration. 0d = GPA using GPIO1 is disabled 1d = GPA using GPIO1

7.1.19 INTF_CFG6 Register (Address = 0x15) [Reset = 0x00]

INTF_CFG6 is shown in 図 7-19 and described in 表 7-20.

Return to the Summary Table.

This register is the interface configuration register 5.

図 7-19. INTF_CFG6 Register

7	6	5	4	3	2	1	0
EN_MBIAS_GPIO[1:0]		IADC_CONVST_GPIO[1:0]		RESERVED			
R/W-00b		R/W-00b		R-0000b			

表 7-20. INTF_CFG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	EN_MBIAS_GPIO[1:0]	R/W	0x0	Enable MICBIAS using GPIO select configuration. 0d = Enable MICBIAS using GPIO is disabled 1d = Enable MICBIAS using GPIO1 2d = Enable MICBIAS using GPI2A 3d = Enable MICBIAS using GPI1A
5-4	IADC_CONVST_GPIO[1:0]	R/W	0x0	IADC conversion start using GPIO select configuration. 0d = Enable IADC using GPIO is disabled 1d = Enable IADC using GPIO1 2d = Enable IADC using GPI2A 3d = Enable IADC using GPI1A
3-0	RESERVED	R	0x0	Reserved bits; Write only reset value

7.1.20 ASI_CFG0 Register (Address = 0x18) [Reset = 0x40]

ASI_CFG0 is shown in 図 7-20 and described in 表 7-21.

Return to the Summary Table.

This register is the ASI configuration register 0.

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図 7-20. ASI_CFG0 Register

7	6	5	4	3	2	1	0
PASI_DIS	SASI_DIS	SASI_CFG_GANG	DAISY_EN[1:0]		DAISY_IN_SEL[2:0]		
R/W-0b	R/W-1b	R/W-0b	R/W-00b		R/W-000b		

表 7-21. ASI_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PASI_DIS	R/W	0x0	Disable or enable primary ASI (PASI). 0d = Primary ASI enabled 1d = Primary ASI disabled
6	SASI_DIS	R/W	0x1	Disable or enable secondary ASI (SASI). 0d = Secondary ASI enabled 1d = Secondary ASI disabled
5	SASI_CFG_GANG	R/W	0x0	All configurations of secondary ASI ganged with primary ASI. 0d = Secondary ASI has independent configurations 1d = Secondary ASI configurations same as primary ASI
4-3	DAISY_EN[1:0]	R/W	0x0	Daisy chain feature enable (Daisy buffer length is 64, only 1 ASI with 1 DOUT AND DIN available) 0d = Daisy chain disabled 1d = PASI daisy chain enabled (Secondary ASI not available) 2d = SASI daisy chain enabled (Primary ASI not available) 3d = Reserved; Don't use
2-0	DAISY_IN_SEL[2:0]	R/W	0x0	Daisy input select configuration. 0d = Daisy input disabled 1d = GPIO1 2d = GPI2A 3d = GPI1A 4d = Reserved 5d = DIN 6d to 7d = Reserved

7.1.21 ASI_CFG1 Register (Address = 0x19) [Reset = 0x00]

ASI_CFG1 is shown in 図 7-21 and described in 表 7-22.

Return to the Summary Table.

This register is the ASI configuration register 1.

図 7-21. ASI_CFG1 Register

7	6	5	4	3	2	1	0
ASI_DOUT_CFG[1:0]		ASI_DIN_CFG[1:0]		DAISY_DIR	RESERVED	RESERVED	RESERVED
R/W-00b		R/W-00b		R/W-0b	R-0b	R-0b	R-0b

表 7-22. ASI_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	ASI_DOUT_CFG[1:0]	R/W	0x0	ASI data output configuration. 0d = 1 data output for Primary ASI and 1 data output for Secondary ASI 1d = 2 data outputs for Primary ASI 2d = 2 data outputs for Secondary ASI 3d = Reserved; Don't use
5-4	ASI_DIN_CFG[1:0]	R/W	0x0	ASI data input configuration. 0d = 1 data input for Primary ASI and 1 data input for Secondary ASI 1d = 2 data inputs for Primary ASI 2d = 2 data inputs for Secondary ASI 3d = Reserved; Don't use

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表 7-22. ASI_CFG1 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
3	DAISY_DIR	R/W	0x0	Daisy direction configuration. 0d = ASI DOUT daisy 1d = ASI DIN daisy
2	RESERVED	R	0x0	Reserved bit; Write only reset value
1	RESERVED	R	0x0	Reserved bit; Write only reset value
0	RESERVED	R	0x0	Reserved bit; Write only reset value

7.1.22 PASI_CFG0 Register (Address = 0x1A) [Reset = 0x30]

PASI_CFG0 is shown in 図 7-22 and described in 表 7-23.

Return to the Summary Table.

This register is the ASI configuration register 0.

図 7-22. PASI_CFG0 Register

7	6	5	4	3	2	1	0
PASI_FORMAT[1:0]		PASI_WLEN[1:0]		PASI_FSYNC_POL	PASI_BCLK_POL	PASI_BUS_ERR	PASI_BUS_ERR_RCOV
R/W-00b		R/W-11b		R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 7-23. PASI_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PASI_FORMAT[1:0]	R/W	0x0	Primary ASI protocol format. 0d = TDM mode 1d = I^2S mode 2d = LJ (left-justified) mode 3d = Reserved; Don't use
5-4	PASI_WLEN[1:0]	R/W	0x3	Primary ASI word or slot length. 0d = 16 bits (Recommended this setting to be used with 10-kΩ input impedance configuration) 1d = 20 bits 2d = 24 bits 3d = 32 bits
3	PASI_FSYNC_POL	R/W	0x0	ASI FSYNC polarity (for PASI protocol only). 0d = Default polarity as per standard protocol 1d = Inverted polarity with respect to standard protocol
2	PASI_BCLK_POL	R/W	0x0	ASI BCLK polarity (for PASI protocol only). 0d = Default polarity as per standard protocol 1d = Inverted polarity with respect to standard protocol
1	PASI_BUS_ERR	R/W	0x0	ASI bus error detection. 0d = Enable bus error detection 1d = Disable bus error detection
0	PASI_BUS_ERR_RCOV	R/W	0x0	ASI bus error auto resume. 0d = Enable auto resume after bus error recovery 1d = Disable auto resume after bus error recovery and remain powered down until host configures the device

7.1.23 PASI_TX_CFG0 Register (Address = 0x1B) [Reset = 0x00]

PASI_TX_CFG0 is shown in 図 7-23 and described in 表 7-24.

Return to the Summary Table.

This register is the PASI TX configuration register 0.

図 7-23. PASI_TX_CFG0 Register

7	6	5	4	3	2	1	0
PASI_TX_EDGE	PASI_TX_FILL	PASI_TX_LSB	PASI_TX_KEEPER[1:0]		PASI_TX_USE_INT_FSYNC	PASI_TX_USE_INT_BCLK	PASI_TDM_PULSE_WIDTH
R/W-0b	R/W-0b	R/W-0b	R/W-00b		R/W-0b	R/W-0b	R/W-0b

表 7-24. PASI_TX_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PASI_TX_EDGE	R/W	0x0	Primary ASI data output (on the primary and secondary data pin) transmit edge. 0d = Default edge as per the protocol configuration setting in PASI_BCLK_POL 1d = Inverted following edge (half cycle delay) with respect to the default edge setting
6	PASI_TX_FILL	R/W	0x0	Primary ASI data output (on the primary and secondary data pin) for any unused cycles 0d = Always transmit 0 for unused cycles 1d = Always use Hi-Z for unused cycles
5	PASI_TX_LSB	R/W	0x0	Primary ASI data output (on the primary and secondary data pin) for LSB transmissions. 0d = Transmit the LSB for a full cycle 1d = Transmit the LSB for the first half cycle and Hi-Z for the second half cycle
4-3	PASI_TX_KEEPER[1:0]	R/W	0x0	Primary ASI data output (on the primary and secondary data pin) bus keeper. 0d = Bus keeper is always disabled 1d = Bus keeper is always enabled 2d = Bus keeper is enabled during LSB transmissions only for one cycle 3d = Bus keeper is enabled during LSB transmissions only for one and half cycles
2	PASI_TX_USE_INT_FSYNC	R/W	0x0	Primary ASI uses internal FSYNC for output data generation in Controller mode configuration as applicable. 0d = Use external FSYNC for ASI protocol data generation 1d = Use internal FSYNC for ASI protocol data generation
1	PASI_TX_USE_INT_BCLK	R/W	0x0	Primary ASI uses internal BCLK for output data generation in Controller mode configuration. 0d = Use external BCLK for ASI protocol data generation 1d = Use internal BCLK for ASI protocol data generation
0	PASI_TDM_PULSE_WIDTH	R/W	0x0	Primary ASI fsync pulse width in TDM format. (Valid for Controller mode) 0d = Fsync pulse is 1 bclk period wide 1d = Fsync pulse is 2 bclk period wide

7.1.24 PASI_TX_CFG1 Register (Address = 0x1C) [Reset = 0x00]

PASI_TX_CFG1 is shown in 図 7-24 and described in 表 7-25.

Return to the Summary Table.

This register is the PASI TX configuration register 1.

図 7-24. PASI_TX_CFG1 Register

7	6	5	4	3	2	1	0
RESERVED			PASI_TX_OFFSET[4:0]				
R-000b			R/W-00000b				

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図 7-24. PASI_TX_CFG1 Register (続き)

表 7-25. PASI_TX_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved bits; Write only reset values
4-0	PASI_TX_OFFSET[4:0]	R/W	0x0	Primary ASI output data MSB slot 0 offset (on the primary and secondary data pin). 0d = ASI data MSB location has no offset and is as per standard protocol 1d = ASI data MSB location (TDM mode is slot 0 or I^{2}S, LJ mode is the left and right slot 0) offset of one BCLK cycle with respect to standard protocol 2d = ASI data MSB location (TDM mode is slot 0 or I^{2}S, LJ mode is the left and right slot 0) offset of two BCLK cycles with respect to standard protocol 3d to 30d = ASI data MSB location (TDM mode is slot 0 or I^{2}S, LJ mode is the left and right slot 0) offset assigned as per configuration 31d = ASI data MSB location (TDM mode is slot 0 or I^{2}S, LJ mode is the left and right slot 0) offset of 31 BCLK cycles with respect to standard protocol

7.1.25 PASI_TX_CFG2 Register (Address = 0x1D) [Reset = 0x00]

PASI_TX_CFG2 is shown in 図 7-25 and described in 表 7-26.

Return to the Summary Table.

This register is the PASI TX configuration register 2.

図 7-25. PASI_TX_CFG2 Register

7	6	5	4	3	2	1	0
PASI_TX_CH8_SEL	PASI_TX_CH7_SEL	PASI_TX_CH6_SEL	PASI_TX_CH5_SEL	PASI_TX_CH4_SEL	PASI_TX_CH3_SEL	PASI_TX_CH2_SEL	PASI_TX_CH1_SEL
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 7-26. PASI_TX_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PASI_TX_CH8_SEL	R/W	0x0	Primary ASI output channel 8 select. 0d = Primary ASI channel 8 output is on DOUT 1d = Primary ASI channel 8 output is on DOUT2
6	PASI_TX_CH7_SEL	R/W	0x0	Primary ASI output channel 7 select. 0d = Primary ASI channel 7 output is on DOUT 1d = Primary ASI channel 7 output is on DOUT2
5	PASI_TX_CH6_SEL	R/W	0x0	Primary ASI output channel 6 select. 0d = Primary ASI channel 6 output is on DOUT 1d = Primary ASI channel 6 output is on DOUT2
4	PASI_TX_CH5_SEL	R/W	0x0	Primary ASI output channel 5 select. 0d = Primary ASI channel 5 output is on DOUT 1d = Primary ASI channel 5 output is on DOUT2
3	PASI_TX_CH4_SEL	R/W	0x0	Primary ASI output channel 4 select. 0d = Primary ASI channel 4 output is on DOUT 1d = Primary ASI channel 4 output is on DOUT2
2	PASI_TX_CH3_SEL	R/W	0x0	Primary ASI output channel 3 select. 0d = Primary ASI channel 3 output is on DOUT 1d = Primary ASI channel 3 output is on DOUT2
1	PASI_TX_CH2_SEL	R/W	0x0	Primary ASI output channel 2 select. 0d = Primary ASI channel 2 output is on DOUT 1d = Primary ASI channel 2 output is on DOUT2

表 7-26. PASI_TX_CFG2 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
0	PASI_TX_CH1_SEL	R/W	0x0	Primary ASI output channel 1 select. 0d = Primary ASI channel 1 output is on DOUT 1d = Primary ASI channel 1 output is on DOUT2

7.1.26 PASI_TX_CH1_CFG Register (Address = 0x1E) [Reset = 0x20]

PASI_TX_CH1_CFG is shown in 図 7-26 and described in 表 7-27.

Return to the Summary Table.

This register is the PASI TX Channel 1 configuration register.

図 7-26. PASI_TX_CH1_CFG Register

7	6	5	4	3	2	1	0
RESERVED		PASI_TX_CH1_CFG	PASI_TX_CH1_SLOT_NUM[4:0]				
R-00b		R/W-1b	R/W-00000b				

表 7-27. PASI_TX_CH1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved bits; Write only reset values
5	PASI_TX_CH1_CFG	R/W	0x1	Primary ASI output channel 1 configuration. 0d = Primary ASI channel 1 output is in a tri-state condition 1d = Primary ASI channel 1 output corresponds to ADC/PDM Channel 1 data
4-0	PASI_TX_CH1_SLOT_NUM[4:0]	R/W	0x0	Primary ASI output channel 1 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^2S, LJ is left slot 15 16d = TDM is slot 16 or I^2S, LJ is right slot 0 17d = TDM is slot 17 or I^2S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is right slot 15

7.1.27 PASI_TX_CH2_CFG Register (Address = 0x1F) [Reset = 0x21]

PASI_TX_CH2_CFG is shown in 図 7-27 and described in 表 7-28.

Return to the Summary Table.

This register is the PASI TX Channel 2 configuration register.

図 7-27. PASI_TX_CH2_CFG Register

7	6	5	4	3	2	1	0
RESERVED		PASI_TX_CH2_CFG	PASI_TX_CH2_SLOT_NUM[4:0]				
R-00b		R/W-1b	R/W-00001b				

表 7-28. PASI_TX_CH2_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved bits; Write only reset values

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表 7-28. PASI_TX_CH2_CFG Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
5	PASI_TX_CH2_CFG	R/W	0x1	Primary ASI output channel 2 configuration. 0d = Primary ASI channel 2 output is in a tri-state condition 1d = Primary ASI channel 2 output corresponds to ADC/PDM Channel 2 data
4-0	PASI_TX_CH2_SLOT_NUM[4:0]	R/W	0x1	Primary ASI output channel 2 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^2S, LJ is left slot 15 16d = TDM is slot 16 or I^2S, LJ is right slot 0 17d = TDM is slot 17 or I^2S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is right slot 15

7.1.28 PASI_TX_CH3_CFG Register (Address = 0x20) [Reset = 0x02]

PASI_TX_CH3_CFG is shown in 図 7-28 and described in 表 7-29.

Return to the Summary Table.

This register is the PASI TX Channel 3 configuration register.

図 7-28. PASI_TX_CH3_CFG Register

7	6	5	4	3	2	1	0
RESERVED	PASI_TX_CH3_CFG[1:0]		PASI_TX_CH3_SLOT_NUM[4:0]				
R-0b	R/W-00b		R/W-00010b				

表 7-29. PASI_TX_CH3_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved bit; Write only reset value
6-5	PASI_TX_CH3_CFG[1:0]	R/W	0x0	Primary ASI output channel 3 configuration. 0d = Primary ASI channel 3 output is in a tri-state condition 1d = Primary ASI channel 3 output corresponds to PDM Channel 3 data 2d = Primary ASI channel 3 output corresponds to VBAT data 3d = Reserved
4-0	PASI_TX_CH3_SLOT_NUM[4:0]	R/W	0x2	Primary ASI output channel 3 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^2S, LJ is left slot 15 16d = TDM is slot 16 or I^2S, LJ is right slot 0 17d = TDM is slot 17 or I^2S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is right slot 15

7.1.29 PASI_TX_CH4_CFG Register (Address = 0x21) [Reset = 0x03]

PASI_TX_CH4_CFG is shown in 図 7-29 and described in 表 7-30.

Return to the Summary Table.

This register is the PASI TX Channel 4 configuration register.

図 7-29. PASI_TX_CH4_CFG Register

7	6	5	4	3	2	1	0

図 7-29. PASI_TX_CH4_CFG Register (続き)

RESERVED	PASI_TX_CH4_CFG[1:0]		PASI_TX_CH4_SLOT_NUM[4:0]				
R-0b	R/W-00b		R/W-00011b				

表 7-30. PASI_TX_CH4_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved bit; Write only reset value
6-5	PASI_TX_CH4_CFG[1:0]	R/W	0x0	Primary ASI output channel 4 configuration. 0d = Primary ASI channel 4 output is in a tri-state condition 1d = Primary ASI channel 4 output corresponds to PDM Channel 4 data 2d = Primary ASI channel 4 output corresponds to TEMP data 3d = Reserved
4-0	PASI_TX_CH4_SLOT_NUM[4:0]	R/W	0x3	Primary ASI output channel 4 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^2S, LJ is left slot 15 16d = TDM is slot 16 or I^2S, LJ is right slot 0 17d = TDM is slot 17 or I^2S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is right slot 15

7.1.30 PASI_TX_CH5_CFG Register (Address = 0x22) [Reset = 0x04]

PASI_TX_CH5_CFG is shown in 図 7-30 and described in 表 7-31.

Return to the Summary Table.

This register is the PASI TX Channel 5 configuration register.

図 7-30. PASI_TX_CH5_CFG Register

7	6	5	4	3	2	1	0
RESERVED	PASI_TX_CH5_CFG[1:0]		PASI_TX_CH5_SLOT_NUM[4:0]				
R-0b	R/W-00b		R/W-00100b				

表 7-31. PASI_TX_CH5_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved bit; Write only reset value
6-5	PASI_TX_CH5_CFG[1:0]	R/W	0x0	Primary ASI output channel 5 configuration. 0d = Primary ASI channel 5 output is in a tri-state condition 1d = Primary ASI channel 5 output corresponds to ASI Input Channel 1 loopback data 2d = Primary ASI channel 5 output corresponds to echo reference Channel 1 data 3d = Reserved
4-0	PASI_TX_CH5_SLOT_NUM[4:0]	R/W	0x4	Primary ASI output channel 5 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^2S, LJ is left slot 15 16d = TDM is slot 16 or I^2S, LJ is right slot 0 17d = TDM is slot 17 or I^2S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is right slot 15

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7.1.31 PASI_TX_CH6_CFG Register (Address = 0x23) [Reset = 0x05]

PASI_TX_CH6_CFG is shown in 図 7-31 and described in 表 7-32.

Return to the Summary Table.

This register is the PASI TX Channel 6 configuration register.

図 7-31. PASI_TX_CH6_CFG Register

7	6	5	4	3	2	1	0
RESERVED	PASI_TX_CH6_CFG[1:0]		PASI_TX_CH6_SLOT_NUM[4:0]				
R-0b	R/W-00b		R/W-00101b				

表 7-32. PASI_TX_CH6_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved bit; Write only reset value
6-5	PASI_TX_CH6_CFG[1:0]	R/W	0x0	Primary ASI output channel 6 configuration. 0d = Primary ASI channel 6 output is in a tri-state condition 1d = Primary ASI channel 6 output corresponds to ASI Input Channel 2 loopback data 2d = Primary ASI channel 6 output corresponds to echo reference Channel 2 data 3d = Reserved
4-0	PASI_TX_CH6_SLOT_NUM[4:0]	R/W	0x5	Primary ASI output channel 6 slot assignment. 0d = TDM is slot 0 or I^{2}S, LJ is left slot 0 1d = TDM is slot 1 or I^{2}S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^{2}S, LJ is left slot 15 16d = TDM is slot 16 or I^{2}S, LJ is right slot 0 17d = TDM is slot 17 or I^{2}S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^{2}S, LJ is right slot 15

7.1.32 PASI_TX_CH7_CFG Register (Address = 0x24) [Reset = 0x06]

PASI_TX_CH7_CFG is shown in 図 7-32 and described in 表 7-33.

Return to the Summary Table.

This register is the PASI TX Channel 7 configuration register.

図 7-32. PASI_TX_CH7_CFG Register

7	6	5	4	3	2	1	0
RESERVED	PASI_TX_CH7_CFG[1:0]		PASI_TX_CH7_SLOT_NUM[4:0]				
R-0b	R/W-00b		R/W-00110b				

表 7-33. PASI_TX_CH7_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved bit; Write only reset value
6-5	PASI_TX_CH7_CFG[1:0]	R/W	0x0	Primary ASI output channel 7 configuration. 0d = Primary ASI channel 7 output is in a tri-state condition 1d = Primary ASI channel 7 output corresponds to {VBAT_WLby2, TEMP_WLby2} 2d = Primary ASI channel 7 output corresponds to {echo_ref_ch1, echo_ref_ch2} 3d = Reserved

表 7-33. PASI_TX_CH7_CFG Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
4-0	PASI_TX_CH7_SLOT_NUM[4:0]	R/W	0x6	Primary ASI output channel 7 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^2S, LJ is left slot 15 16d = TDM is slot 16 or I^2S, LJ is right slot 0 17d = TDM is slot 17 or I^2S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is right slot 15

7.1.33 PASI_TX_CH8_CFG Register (Address = 0x25) [Reset = 0x07]

PASI_TX_CH8_CFG is shown in 図 7-33 and described in 表 7-34.

Return to the Summary Table.

This register is the PASI TX Channel 8 configuration register.

図 7-33. PASI_TX_CH8_CFG Register

7	6	5	4	3	2	1	0
RESERVED		PASI_TX_CH8_CFG	PASI_TX_CH8_SLOT_NUM[4:0]				
R-00b		R/W-0b	R/W-00111b				

表 7-34. PASI_TX_CH8_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved bits; Write only reset values
5	PASI_TX_CH8_CFG	R/W	0x0	Primary ASI output channel 8 configuration. 0d = Primary ASI channel 8 output is in a tri-state condition 1d = Primary ASI channel 8 output corresponds to ICLA data
4-0	PASI_TX_CH8_SLOT_NUM[4:0]	R/W	0x7	Primary ASI output channel 8 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^2S, LJ is left slot 15 16d = TDM is slot 16 or I^2S, LJ is right slot 0 17d = TDM is slot 17 or I^2S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is right slot 15

7.1.34 PASI_RX_CFG0 Register (Address = 0x26) [Reset = 0x00]

PASI_RX_CFG0 is shown in 図 7-34 and described in 表 7-35.

Return to the Summary Table.

This register is the PASI RX configuration register 0.

図 7-34. PASI_RX_CFG0 Register

7	6	5	4	3	2	1	0
PASI_RX_EDGE	PASI_RX_USE_INT_FSYNC	PASI_RX_USE_INT_BCLK	PASI_RX_OFFSET[4:0]				
R/W-0b	R/W-0b	R/W-0b	R/W-00000b				

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表 7-35. PASI_RX_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PASI_RX_EDGE	R/W	0x0	Primary ASI data input (on the primary and secondary data pin) receive edge. 0d = Default edge as per the protocol configuration setting in PASI_BCLK_POL 1d = Inverted following edge (half cycle delay) with respect to the default edge setting
6	PASI_RX_USE_INT_FSYNC	R/W	0x0	Primary ASI uses internal FSYNC for input data latching in Controller mode configuration as applicable. 0d = Use external FSYNC for ASI protocol data latching 1d = Use internal FSYNC for ASI protocol data latching
5	PASI_RX_USE_INT_BCLK	R/W	0x0	Primary ASI uses internal BCLK for input data latching in Controller mode configuration. 0d = Use external BCLK for ASI protocol data latching 1d = Use internal BCLK for ASI protocol data latching
4-0	PASI_RX_OFFSET[4:0]	R/W	0x0	Primary ASI data input MSB slot 0 offset (on the primary and secondary data pin). 0d = ASI data MSB location has no offset and is as per standard protocol 1d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset of one BCLK cycle with respect to standard protocol 2d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset of two BCLK cycles with respect to standard protocol 3d to 30d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset assigned as per configuration 31d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset of 31 BCLK cycles with respect to standard protocol

7.1.35 PASI_RX_CFG1 Register (Address = 0x27) [Reset = 0x00]

PASI_RX_CFG1 is shown in 図 7-35 and described in 表 7-36.

Return to the Summary Table.

This register is the PASI RX configuration register 1.

図 7-35. PASI_RX_CFG1 Register

7	6	5	4	3	2	1	0
PASI_RX_CH8_SEL	PASI_RX_CH7_SEL	PASI_RX_CH6_SEL	PASI_RX_CH5_SEL	PASI_RX_CH4_SEL	PASI_RX_CH3_SEL	PASI_RX_CH2_SEL	PASI_RX_CH1_SEL
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 7-36. PASI_RX_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PASI_RX_CH8_SEL	R/W	0x0	Primary ASI input channel 8 select. 0d = Primary ASI channel 8 input is on DIN 1d = Primary ASI channel 8 input is on DIN2
6	PASI_RX_CH7_SEL	R/W	0x0	Primary ASI input channel 7 select. 0d = Primary ASI channel 7 input is on DIN 1d = Primary ASI channel 7 input is on DIN2
5	PASI_RX_CH6_SEL	R/W	0x0	Primary ASI input channel 6 select. 0d = Primary ASI channel 6 input is on DIN 1d = Primary ASI channel 6 input is on DIN2

表 7-36. PASI_RX_CFG1 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
4	PASI_RX_CH5_SEL	R/W	0x0	Primary ASI input channel 5 select. 0d = Primary ASI channel 5 input is on DIN 1d = Primary ASI channel 5 input is on DIN2
3	PASI_RX_CH4_SEL	R/W	0x0	Primary ASI input channel 4 select. 0d = Primary ASI channel 4 input is on DIN 1d = Primary ASI channel 4 input is on DIN2
2	PASI_RX_CH3_SEL	R/W	0x0	Primary ASI input channel 3 select. 0d = Primary ASI channel 3 input is on DIN 1d = Primary ASI channel 3 input is on DIN2
1	PASI_RX_CH2_SEL	R/W	0x0	Primary ASI input channel 2 select. 0d = Primary ASI channel 2 input is on DIN 1d = Primary ASI channel 2 input is on DIN2
0	PASI_RX_CH1_SEL	R/W	0x0	Primary ASI input channel 1 select. 0d = Primary ASI channel 1 input is on DIN 1d = Primary ASI channel 1 input is on DIN2

7.1.36 PASI_RX_CH1_CFG Register (Address = 0x28) [Reset = 0x20]

PASI_RX_CH1_CFG is shown in 図 7-36 and described in 表 7-37.

Return to the Summary Table.

This register is the PASI RX Channel 1 configuration register.

図 7-36. PASI_RX_CH1_CFG Register

7	6	5	4	3	2	1	0
RESERVED		PASI_RX_CH1_CFG	PASI_RX_CH1_SLOT_NUM[4:0]				
R-00b		R/W-1b	R/W-00000b				

表 7-37. PASI_RX_CH1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved bits; Write only reset values
5	PASI_RX_CH1_CFG	R/W	0x1	Primary ASI input channel 1 configuration. 0d = Primary ASI channel 1 input is disabled 1d = Primary ASI channel 1 input corresponds to DAC Channel 1 data
4-0	PASI_RX_CH1_SLOT_NUM[4:0]	R/W	0x0	Primary ASI input channel 1 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^2S, LJ is left slot 15 16d = TDM is slot 16 or I^2S, LJ is right slot 0 17d = TDM is slot 17 or I^2S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is right slot 15

7.1.37 PASI_RX_CH2_CFG Register (Address = 0x29) [Reset = 0x21]

PASI_RX_CH2_CFG is shown in 図 7-37 and described in 表 7-38.

Return to the Summary Table.

This register is the PASI RX Channel 2 configuration register.

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図 7-37. PASI_RX_CH2_CFG Register

7	6	5	4	3	2	1	0
RESERVED		PASI_RX_CH2_CFG	PASI_RX_CH2_SLOT_NUM[4:0]				
R-00b		R/W-1b	R/W-00001b				

表 7-38. PASI_RX_CH2_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved bits; Write only reset values
5	PASI_RX_CH2_CFG	R/W	0x1	Primary ASI input channel 2 configuration. 0d = Primary ASI channel 2 input is disabled 1d = Primary ASI channel 2 input corresponds to DAC Channel 2 data
4-0	PASI_RX_CH2_SLOT_NUM[4:0]	R/W	0x1	Primary ASI input channel 2 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^2S, LJ is left slot 15 16d = TDM is slot 16 or I^2S, LJ is right slot 0 17d = TDM is slot 17 or I^2S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is right slot 15

7.1.38 PASI_RX_CH3_CFG Register (Address = 0x2A) [Reset = 0x02]

PASI_RX_CH3_CFG is shown in 図 7-38 and described in 表 7-39.

Return to the Summary Table.

This register is the PASI RX Channel 3 configuration register.

図 7-38. PASI_RX_CH3_CFG Register

7	6	5	4	3	2	1	0
RESERVED		PASI_RX_CH3_CFG	PASI_RX_CH3_SLOT_NUM[4:0]				
R-00b		R/W-0b	R/W-00010b				

表 7-39. PASI_RX_CH3_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved bits; Write only reset values
5	PASI_RX_CH3_CFG	R/W	0x0	Primary ASI input channel 3 configuration. 0d = Primary ASI channel 3 input is disabled 1d = Primary ASI channel 3 input corresponds to DAC Channel 3 data
4-0	PASI_RX_CH3_SLOT_NUM[4:0]	R/W	0x2	Primary ASI input channel 3 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^2S, LJ is left slot 15 16d = TDM is slot 16 or I^2S, LJ is right slot 0 17d = TDM is slot 17 or I^2S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is right slot 15

7.1.39 PASI_RX_CH4_CFG Register (Address = 0x2B) [Reset = 0x03]

PASI_RX_CH4_CFG is shown in 図 7-39 and described in 表 7-40.

Return to the Summary Table.

This register is the PASI RX Channel 4 configuration register.

図 7-39. PASI_RX_CH4_CFG Register

7	6	5	4	3	2	1	0
RESERVED		PASI_RX_CH4_CFG	PASI_RX_CH4_SLOT_NUM[4:0]				
R-00b		R/W-0b	R/W-00011b				

表 7-40. PASI_RX_CH4_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved bits; Write only reset values
5	PASI_RX_CH4_CFG	R/W	0x0	Primary ASI input channel 4 configuration. 0d = Primary ASI channel 4 input is disabled 1d = Primary ASI channel 4 input corresponds to DAC Channel 4 data
4-0	PASI_RX_CH4_SLOT_NUM[4:0]	R/W	0x3	Primary ASI input channel 4 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^2S, LJ is left slot 15 16d = TDM is slot 16 or I^2S, LJ is right slot 0 17d = TDM is slot 17 or I^2S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is right slot 15

7.1.40 PASI_RX_CH5_CFG Register (Address = 0x2C) [Reset = 0x04]

PASI_RX_CH5_CFG is shown in 図 7-40 and described in 表 7-41.

Return to the Summary Table.

This register is the PASI RX Channel 5 configuration register.

図 7-40. PASI_RX_CH5_CFG Register

7	6	5	4	3	2	1	0
RESERVED	PASI_RX_CH5_CFG[1:0]		PASI_RX_CH5_SLOT_NUM[4:0]				
R-0b	R/W-00b		R/W-00100b				

表 7-41. PASI_RX_CH5_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved bit; Write only reset value
6-5	PASI_RX_CH5_CFG[1:0]	R/W	0x0	Primary ASI input channel 5 configuration. 0d = Primary ASI channel 5 input is disabled 1d = Primary ASI channel 5 input corresponds to DAC Channel 5 data 2d = Primary ASI channel 5 input corresponds to ADC Channel 1 output loopback 3d = Reserved

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表 7-41. PASI_RX_CH5_CFG Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
4-0	PASI_RX_CH5_SLOT_NUM[4:0]	R/W	0x4	Primary ASI input channel 5 slot assignment. 0d = TDM is slot 0 or I^{2}S, LJ is left slot 0 1d = TDM is slot 1 or I^{2}S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^{2}S, LJ is left slot 15 16d = TDM is slot 16 or I^{2}S, LJ is right slot 0 17d = TDM is slot 17 or I^{2}S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^{2}S, LJ is right slot 15

7.1.41 PASI_RX_CH6_CFG Register (Address = 0x2D) [Reset = 0x05]

PASI_RX_CH6_CFG is shown in 図 7-41 and described in 表 7-42.

Return to the Summary Table.

This register is the PASI RX Channel 6 configuration register.

図 7-41. PASI_RX_CH6_CFG Register

7	6	5	4	3	2	1	0
RESERVED	PASI_RX_CH6_CFG[1:0]		PASI_RX_CH6_SLOT_NUM[4:0]				
R-0b	R/W-00b		R/W-00101b				

表 7-42. PASI_RX_CH6_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved bit; Write only reset value
6-5	PASI_RX_CH6_CFG[1:0]	R/W	0x0	Primary ASI input channel 6 configuration. 0d = Primary ASI channel 6 input is disabled 1d = Primary ASI channel 6 input corresponds to DAC Channel 6 data 2d = Primary ASI channel 6 input corresponds to ADC Channel 2 output loopback 3d = Primary ASI channel 6 input corresponds to ICLA device 1 data
4-0	PASI_RX_CH6_SLOT_NUM[4:0]	R/W	0x5	Primary ASI input channel 6 slot assignment. 0d = TDM is slot 0 or I^{2}S, LJ is left slot 0 1d = TDM is slot 1 or I^{2}S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^{2}S, LJ is left slot 15 16d = TDM is slot 16 or I^{2}S, LJ is right slot 0 17d = TDM is slot 17 or I^{2}S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^{2}S, LJ is right slot 15

7.1.42 PASI_RX_CH7_CFG Register (Address = 0x2E) [Reset = 0x06]

PASI_RX_CH7_CFG is shown in 図 7-42 and described in 表 7-43.

Return to the Summary Table.

This register is the PASI RX Channel 7 configuration register.

図 7-42. PASI_RX_CH7_CFG Register

7	6	5	4	3	2	1	0
RESERVED	PASI_RX_CH7_CFG[1:0]		PASI_RX_CH7_SLOT_NUM[4:0]				
R-0b	R/W-00b		R/W-00110b				

表 7-43. PASI_RX_CH7_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved bit; Write only reset value
6-5	PASI_RX_CH7_CFG[1:0]	R/W	0x0	Primary ASI input channel 7 configuration. 0d = Primary ASI channel 7 input is disabled 1d = Primary ASI channel 7 input corresponds to DAC Channel 7 data 2d = Primary ASI channel 7 input corresponds to ADC Channel 3 output loopback 3d = Primary ASI channel 7 input corresponds to ICLA device 2 data
4-0	PASI_RX_CH7_SLOT_NUM[4:0]	R/W	0x6	Primary ASI input channel 7 slot assignment. 0d = TDM is slot 0 or I²S, LJ is left slot 0 1d = TDM is slot 1 or I²S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I²S, LJ is left slot 15 16d = TDM is slot 16 or I²S, LJ is right slot 0 17d = TDM is slot 17 or I²S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I²S, LJ is right slot 15

7.1.43 PASI_RX_CH8_CFG Register (Address = 0x2F) [Reset = 0x07]

PASI_RX_CH8_CFG is shown in 図 7-43 and described in 表 7-44.

Return to the Summary Table.

This register is the PASI RX Channel 8 configuration register.

図 7-43. PASI_RX_CH8_CFG Register

7	6	5	4	3	2	1	0
RESERVED	PASI_RX_CH8_CFG[1:0]		PASI_RX_CH8_SLOT_NUM[4:0]				
R-0b	R/W-00b		R/W-00111b				

表 7-44. PASI_RX_CH8_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved bit; Write only reset value
6-5	PASI_RX_CH8_CFG[1:0]	R/W	0x0	Primary ASI input channel 8 configuration. 0d = Primary ASI channel 8 input is disabled 1d = Primary ASI channel 8 input corresponds to DAC Channel 8 data 2d = Primary ASI channel 8 input corresponds to ADC Channel 4 output loopback 3d = Primary ASI channel 8 input corresponds to ICLA device 3 data
4-0	PASI_RX_CH8_SLOT_NUM[4:0]	R/W	0x7	Primary ASI input channel 8 slot assignment. 0d = TDM is slot 0 or I²S, LJ is left slot 0 1d = TDM is slot 1 or I²S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I²S, LJ is left slot 15 16d = TDM is slot 16 or I²S, LJ is right slot 0 17d = TDM is slot 17 or I²S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I²S, LJ is right slot 15

7.1.44 CLK_CFG0 Register (Address = 0x32) [Reset = 0x00]

CLK_CFG0 is shown in 図 7-44 and described in 表 7-45.

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This register is the clock configuration register 0.

図 7-44. CLK_CFG0 Register

7	6	5	4	3	2	1	0
PASI_SAMP_RATE[5:0]						PASI_FS_RATE_NO_LIM	CUSTOM_CLK_CFG
R/W-000000b						R/W-0b	R/W-0b

表 7-45. CLK_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	PASI_SAMP_RATE[5:0]	R/W	0x0	Primary ASI sample rate configuration. -Typical (Allowed Range) 0d = Primary ASI sampling rate auto detected in the device 1d = 768000 (670320-791040) 2d = 614400 (536256-632832) 3d = 512000 (446880-527360) 4d = 438857 (383040-452022) 5d = 384000 (335160-395520) 6d = 341333 (297920-351573) 7d = 307200 (268128-316416) 8d = 256000 (223440-263680) 9d = 219429 (191520-226011) 10d = 192000 (167580-197760) 11d = 170667 (148960-175786) 12d = 153600 (134064-158208) 13d = 128000 (111720-131840) 14d = 109714 (95760-113005) 15d = 96000 (83790-98880) 16d = 85333 (74480-87893) 17d = 76800 (67032-79104) 18d = 64000 (55860-65920) 19d = 54857 (47880-56502) 20d = 48000 (41895-49440) 21d = 42667 (37240-43946) 22d = 38400 (33516-39552) 23d = 32000 (27930-32960) 24d = 27429 (23940-28251) 25d = 24000 (20947-24720) 26d = 21333 (18620-21973) 27d = 19200 (16758-19776) 28d = 16000 (13965-16480) 29d = 13714 (11970-14125) 30d = 12000 (10473-12360) 31d = 10667 (9310-10986) 32d = 9600 (8379-9888) 33d = 8000 (6982-8240) 34d = 6857 (5985-7062) 35d = 6000 (5236-6180) 36d = 5333 (4655-5493) 37d = 4800 (4189-4944) 38d = 4000 (3491-4120) 39d = 3429 (2992-3531) 40d = 3000 (2618-3090) 41d-63d = Reserved
1	PASI_FS_RATE_NO_LIM	R/W	0x0	Limit sampling rate to standard audio sample rates only. 0d = Standard audio rates with 1% tolerance supported using auto mode 1d = Standard audio rates with 5% tolerance supported using auto mode
0	CUSTOM_CLK_CFG	R/W	0x0	Custom clock configuration enable, all dividers and mux selects need to be manually configured. 0d = Auto clock configuration 1d = Custom clock configuration

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7.1.45 CLK_CFG1 Register (Address = 0x33) [Reset = 0x00]

CLK_CFG1 is shown in 図 7-45 and described in 表 7-46.

Return to the Summary Table.

This register is the clock configuration register 1.

図 7-45. CLK_CFG1 Register

7	6	5	4	3	2	1	0
SASI_SAMP_RATE[5:0]						SASI_FS_RATE_NO_LIM	RESERVED
R/W-000000b						R/W-0b	R-0b

表 7-46. CLK_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	SASI_SAMP_RATE[5:0]	R/W	0x0	Secondary ASI sample rate configuration. -Typical (Range) 0d = Secondary ASI sampling rate auto detected in the device 1d = 768000 (670320-791040) 2d = 614400 (536256-632832) 3d = 512000 (446880-527360) 4d = 438857 (383040-452022) 5d = 384000 (335160-395520) 6d = 341333 (297920-351573) 7d = 307200 (268128-316416) 8d = 256000 (223440-263680) 9d = 219429 (191520-226011) 10d = 192000 (167580-197760) 11d = 170667 (148960-175786) 12d = 153600 (134064-158208) 13d = 128000 (111720-131840) 14d = 109714 (95760-113005) 15d = 96000 (83790-98880) 16d = 85333 (74480-87893) 17d = 76800 (67032-79104) 18d = 64000 (55860-65920) 19d = 54857 (47880-56502) 20d = 48000 (41895-49440) 21d = 42667 (37240-43946) 22d = 38400 (33516-39552) 23d = 32000 (27930-32960) 24d = 27429 (23940-28251) 25d = 24000 (20947-24720) 26d = 21333 (18620-21973) 27d = 19200 (16758-19776) 28d = 16000 (13965-16480) 29d = 13714 (11970-14125) 30d = 12000 (10473-12360) 31d = 10667 (9310-10986) 32d = 9600 (8379-9888) 33d = 8000 (6982-8240) 34d = 6857 (5985-7062) 35d = 6000 (5236-6180) 36d = 5333 (4655-5493) 37d = 4800 (4189-4944) 38d = 4000 (3491-4120) 39d = 3429 (2992-3531) 40d = 3000 (2618-3090) 41d-63d = Reserved
1	SASI_FS_RATE_NO_LIM	R/W	0x0	Limit sampling rate to standard audio sample rates only. 0d = Standard audio rates with 1% tolerance supported using auto mode 1d = Standard audio rates with 5% tolerance supported using auto mode

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表 7-46. CLK_CFG1 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
0	RESERVED	R	0x0	Reserved bit; Write only reset value

7.1.46 CLK_CFG2 Register (Address = 0x34) [Reset = 0x40]

CLK_CFG2 is shown in 図 7-46 and described in 表 7-47.

Return to the Summary Table.

This register is the clock configuration register 2.

図 7-46. CLK_CFG2 Register

7	6	5	4	3	2	1	0
PLL_DIS	AUTO_PLL_FR_ALLOW	RESERVED	RESERVED	CLK_SRC_SEL[2:0]			RATIO_CLK_EDGE
R/W-0b	R/W-1b	R-0b	R-0b	R/W-000b			R/W-0b

表 7-47. CLK_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PLL_DIS	R/W	0x0	Custom/Auto clock mode PLL setting. 0d = PLL is always enabled in custom clk mode/PLL is enabled based on DSP MIPS requirement in auto clock mode 1d = PLL is disabled
6	AUTO_PLL_FR_ALLOW	R/W	0x1	Allow the PLL to operate in fractional mode of operation. 0d = PLL fractional mode disabled 1d = PLL fractional mode allowed
5	RESERVED	R	0x0	Reserved bit; Write only reset value
4	RESERVED	R	0x0	Reserved bit; Write only reset value
3-1	CLK_SRC_SEL[2:0]	R/W	0x0	Input clock source select. 0d = Primary ASI BCLK is the input clock source 1d = cclk synchronized with Primary ASI FSYNC is the input clock source 2d = Secondary ASI BCLK is the input clock source 3d = cclk synchronized with Secondary ASI FSYNC is the input clock source 4d = Fixed cclk frequency (used only in controller mode configuration) 5d = Internal oscillator clock is the input clock source 6d to 7d = Reserved
0	RATIO_CLK_EDGE	R/W	0x0	Edge selection for clock source ratio detection. 0d = Use rising edge of clock source to check ratio with primary or secondary FSYNC 1d = Use falling edge of clock source to check ratio with primary or secondary FSYNC

7.1.47 CNT_CLK_CFG0 Register (Address = 0x35) [Reset = 0x00]

CNT_CLK_CFG0 is shown in 図 7-47 and described in 表 7-48.

Return to the Summary Table.

This register is the controller mode clock configuration register 0.

図 7-47. CNT_CLK_CFG0 Register

7	6	5	4	3	2	1	0
PDM_CLK_CFG[1:0]		CCLK_FS_RATIO_MSB[5:0]					

図 7-47. CNT_CLK_CFG0 Register (続き)

R/W-00b	R/W-000000b

表 7-48. CNT_CLK_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PDM_CLK_CFG[1:0]	R/W	0x0	PDM_CLK configurattion. 0d = PDM_CLK is 2.8224 MHz or 3.072 MHz 1d = PDM_CLK is 1.4112 MHz or 1.536 MHz 2d = PDM_CLK is 705.6 kHz or 768 kHz 3d = PDM_CLK is 5.6448 MHz or 6.144 MHz
5-0	CCLK_FS_RATIO_MSB[5:0]	R/W	0x0	Most significant bits for selecting the ratio between cclk and primary/secondary ASI FSYNC with which cclk is synchonized. 0d = Auto detect the ratio (assumption is cclk is synchronized with primary/secondary FSYNC) 1d to 16383d = Ratio as per configuration

7.1.48 CNT_CLK_CFG1 Register (Address = 0x36) [Reset = 0x00]

CNT_CLK_CFG1 is shown in 図 7-48 and described in 表 7-49.

Return to the Summary Table.

This register is the controller mode clock configuration register 1.

図 7-48. CNT_CLK_CFG1 Register

7	6	5	4	3	2	1	0
CCLK_FS_RATIO_LSB[7:0]							
R/W-00000000b							

表 7-49. CNT_CLK_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	CCLK_FS_RATIO_LSB[7:0]	R/W	0x0	Select the ratio between cclk and primary/secondary ASI FSYNC with which cclk is synchonized. 0d = Auto detect the ratio (assumption is cclk is synchronized with primary/secondary FSYNC) 1d to 16383d = Ratio as per configuration

7.1.49 CNT_CLK_CFG2 Register (Address = 0x37) [Reset = 0x20]

CNT_CLK_CFG2 is shown in 図 7-49 and described in 表 7-50.

Return to the Summary Table.

This register is the controller mode clock configuration register 2.

図 7-49. CNT_CLK_CFG2 Register

7	6	5	4	3	2	1	0
CCLK_FREQ_SEL[2:0]			PASI_CNT_CFG	SASI_CNT_CFG	RESERVED	RESERVED	FS_MODE
R/W-001b			R/W-0b	R/W-0b	R-0b	R-0b	R/W-0b

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表 7-50. CNT_CLK_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	CCLK_FREQ_SEL[2:0]	R/W	0x1	These bits select the CCLK input frequency (used only in controller mode configuration). 0d = 12 MHz 1d = 12.288 MHz 2d = 13 MHz 3d = 16 MHz 4d = 19.2 MHz 5d = 19.68 MHz 6d = 24 MHz 7d = 24.576 MHz
4	PASI_CNT_CFG	R/W	0x0	Primary ASI controller or target configuration 0d = Primary ASI in target configuration 1d = Primary ASI in controller configuration
3	SASI_CNT_CFG	R/W	0x0	Secondary ASI controller or target configuration 0d = Secondary ASI in target configuration 1d = Secondary ASI in controller configuration
2	RESERVED	R	0x0	Reserved bit; Write only reset value
1	RESERVED	R	0x0	Reserved bit; Write only reset value
0	FS_MODE	R/W	0x0	Sample rate setting (valid when the device is in controller mode). This is applicable for both PASI and SASI. 0d = sampling rate is a multiple (or submultiple) of 48 kHz 1d = sampling rate is a multiple (or submultiple) of 44.1 kHz

7.1.50 CNT_CLK_CFG3 Register (Address = 0x38) [Reset = 0x00]

CNT_CLK_CFG3 is shown in 図 7-50 and described in 表 7-51.

Return to the Summary Table.

This register is the controller mode clock configuration register 3.

図 7-50. CNT_CLK_CFG3 Register

7	6	5	4	3	2	1	0
PASI_USE_INT_BCLK_FOR_FSYNC	PASI_INV_BCLK_FOR_FSYNC	PASI_BCLK_FS_RATIO_MSB[5:0]					
R/W-0b	R/W-0b	R/W-000000b					

表 7-51. CNT_CLK_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PASI_USE_INT_BCLK_FOR_FSYNC	R/W	0x0	Use internal BCLK for FSYNC generation in PASI during controller mode configuration. 0d = Use external BCLK for FSYNC generation 1d = Use internal BCLK for FSYNC generation
6	PASI_INV_BCLK_FOR_FSYNC	R/W	0x0	Invert PASI BCLK polarity only for PASI FSYNC generation in controller mode configuration. 0d = Do not invert PASI BCLK polarity for PASI FSYNC generation 1d = Invert PASI BCLK polarity for PASI FSYNC generation
5-0	PASI_BCLK_FS_RATIO_MSB[5:0]	R/W	0x0	MSB bits for primary ASI BCLK to FSYNC ratio in controller mode.

7.1.51 CNT_CLK_CFG4 Register (Address = 0x39) [Reset = 0x00]

CNT_CLK_CFG4 is shown in 図 7-51 and described in 表 7-52.

Return to the Summary Table.

This register is the controller mode clock configuration register 4.

図 7-51. CNT_CLK_CFG4 Register

7	6	5	4	3	2	1	0
PASI_BCLK_FS_RATIO_LSB[7:0]							
R/W-00000000b							

表 7-52. CNT_CLK_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PASI_BCLK_FS_RATIO_LSB[7:0]	R/W	0x0	LSB byte for primary ASI BCLK to FSYNC ratio in controller mode.

7.1.52 CNT_CLK_CFG5 Register (Address = 0x3A) [Reset = 0x00]

CNT_CLK_CFG5 is shown in 図 7-52 and described in 表 7-53.

Return to the Summary Table.

This register is the controller mode clock configuration register 5.

図 7-52. CNT_CLK_CFG5 Register

7	6	5	4	3	2	1	0
SASI_USE_INT_BCLK_FOR_FSYNC	SASI_INV_BCLK_FOR_FSYNC	SASI_BCLK_FS_RATIO_MSB[5:0]					
R/W-0b	R/W-0b	R/W-000000b					

表 7-53. CNT_CLK_CFG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SASI_USE_INT_BCLK_FOR_FSYNC	R/W	0x0	Use internal BCLK for FSYNC generation in SASI during controller mode configuration. 0d = Use external BCLK for FSYNC generation 1d = Use internal BCLK for FSYNC generation
6	SASI_INV_BCLK_FOR_FSYNC	R/W	0x0	Invert SASI BCLK polarity only for SASI FSYNC generation in controller mode configuration. 0d = Do not invert SASI BCLK polarity for SASI FSYNC generation 1d = Invert SASI BCLK polarity for SASI FSYNC generation
5-0	SASI_BCLK_FS_RATIO_MSB[5:0]	R/W	0x0	MSB bits for secondary ASI BCLK to FSYNC ratio in controller mode.

7.1.53 CNT_CLK_CFG6 Register (Address = 0x3B) [Reset = 0x00]

CNT_CLK_CFG6 is shown in 図 7-53 and described in 表 7-54.

Return to the Summary Table.

This register is the controller mode clock configuration register 6.

図 7-53. CNT_CLK_CFG6 Register

7	6	5	4	3	2	1	0
SASI_BCLK_FS_RATIO_LSB[7:0]							
R/W-00000000b							

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表 7-54. CNT_CLK_CFG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SASI_BCLK_FS_RATIO_LSB[7:0]	R/W	0x0	LSB byte for secondary ASI BCLK to FSYNC ratio in controller mode.

7.1.54 CLK_ERR_STS0 Register (Address = 0x3C) [Reset = 0x00]

CLK_ERR_STS0 is shown in 図 7-54 and described in 表 7-55.

Return to the Summary Table.

This register is the clock error and status register 0.

図 7-54. CLK_ERR_STS0 Register

7	6	5	4	3	2	1	0
DSP_CLK_ERR	RESERVED	RESERVED	SRC_RATIO_ERR	DEM_RATE_ERR	PDM_CLK_ERR	RESET_ON_CLK_STOP_DET_STS	RESERVED
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 7-55. CLK_ERR_STS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DSP_CLK_ERR	R	0x0	Flag indicating ratio error between FSYNC and selected clock source. 0d = No ratio error 1d = Ratio error between primary or secondary ASI FSYNC and selected clock source
6	RESERVED	R	0x0	Reserved bit; Write only reset value
5	RESERVED	R	0x0	Reserved bit; Write only reset value
4	SRC_RATIO_ERR	R	0x0	Flag indicating that SRC m:n ratio is unsupported. (not valid for custom m/n ratio config). 0d = m:n ratio supported 1d = Unsupported m:n ratio error
3	DEM_RATE_ERR	R	0x0	Flag indicating that clock configuration does not allow valid DEM rate. 0d = No DEM clock rate error 1d = DEM clock rate error in selected clock configuration
2	PDM_CLK_ERR	R	0x0	Flag indicating that clock configuration does not allow valid PDM clock generation. 0d = No PDM clock generation error 1d = PDM clock generation error in selected clock configuration
1	RESET_ON_CLK_STOP_DET_STS	R	0x0	Flag indicating that audio clock source stopped for atleast 1ms. 0d = No audio clock source error 1d = Audio clock source stopped for atleast 1ms
0	RESERVED	R	0x0	Reserved bit; Write only reset value

7.1.55 CLK_ERR_STS1 Register (Address = 0x3D) [Reset = 0x00]

CLK_ERR_STS1 is shown in 図 7-55 and described in 表 7-56.

Return to the Summary Table.

This register is the clock error and status register 1.

図 7-55. CLK_ERR_STS1 Register

7	6	5	4	3	2	1	0

図 7-55. CLK_ERR_STS1 Register (続き)

PASI_BCLK_FS_RATIO_ERR	SASI_BCLK_FS_RATIO_ERR	CCLK_FS_RATIO_ERR	PASI_FS_ERR	SASI_FS_ERR	RESERVED
R-0b	R-0b	R-0b	R-0b	R-0b	R-000b

表 7-56. CLK_ERR_STS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PASI_BCLK_FS_RATIO_ERR	R	0x0	Flag indicating PASI bclk fsync ratio error. 0d = No PASI bclk fsync ratio error 1d = PASI bclk fsync ratio error in selected clock configuration
6	SASI_BCLK_FS_RATIO_ERR	R	0x0	Flag indicating SASI bclk fsync ratio error. 0d = No SASI bclk fsync ratio error 1d = SASI bclk fsync ratio error in selected clock configuration
5	CCLK_FS_RATIO_ERR	R	0x0	Flag indicating CCLK fsync ratio error. 0d = No CCLK fsync ratio error 1d = CCLK fsync ratio error
4	PASI_FS_ERR	R	0x0	Flag indicating PASI FS rate change or halt error. 0d = No PASI FS error 1d = PASI FS rate change or halt detected
3	SASI_FS_ERR	R	0x0	Flag indicating SASI FS rate change or halt error. 0d = No SASI FS error 1d = SASI FS rate change or halt detected
2-0	RESERVED	R	0x0	Reserved bits; Write only reset values

7.1.56 CLK_DET_STS0 Register (Address = 0x3E) [Reset = 0x00]

CLK_DET_STS0 is shown in 図 7-56 and described in 表 7-57.

Return to the Summary Table.

This register is the clock ratio detection register 0.

図 7-56. CLK_DET_STS0 Register

7	6	5	4	3	2	1	0
PASI_SAMP_RATE_STS[5:0]						PLL_MODE_STS[1:0]	
R-000000b						R-00b	

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表 7-57. CLK_DET_STS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	PASI_SAMP_RATE_STS[5:0]	R	0x0	Primary ASI Sample rate detected status. 0d = Reserved 1d = 768000 (670320-791040) 2d = 614400 (536256-632832) 3d = 512000 (446880-527360) 4d = 438857 (383040-452022) 5d = 384000 (335160-395520) 6d = 341333 (297920-351573) 7d = 307200 (268128-316416) 8d = 256000 (223440-263680) 9d = 219429 (191520-226011) 10d = 192000 (167580-197760) 11d = 170667 (148960-175786) 12d = 153600 (134064-158208) 13d = 128000 (111720-131840) 14d = 109714 (95760-113005) 15d = 96000 (83790-98880) 16d = 85333 (74480-87893) 17d = 76800 (67032-79104) 18d = 64000 (55860-65920) 19d = 54857 (47880-56502) 20d = 48000 (41895-49440) 21d = 42667 (37240-43946) 22d = 38400 (33516-39552) 23d = 32000 (27930-32960) 24d = 27429 (23940-28251) 25d = 24000 (20947-24720) 26d = 21333 (18620-21973) 27d = 19200 (16758-19776) 28d = 16000 (13965-16480) 29d = 13714 (11970-14125) 30d = 12000 (10473-12360) 31d = 10667 (9310-10986) 32d = 9600 (8379-9888) 33d = 8000 (6982-8240) 34d = 6857 (5985-7062) 35d = 6000 (5236-6180) 36d = 5333 (4655-5493) 37d = 4800 (4189-4944) 38d = 4000 (3491-4120) 39d = 3429 (2992-3531) 40d = 3000 (2618-3090) 41d-63d = Reserved
1-0	PLL_MODE_STS[1:0]	R	0x0	PLL usage status. 0d = PLL used in integer mode 1d = PLL used in fractional mode 2d = PLL not used 3d = Reserved

7.1.57 CLK_DET_STS1 Register (Address = 0x3F) [Reset = 0x00]

CLK_DET_STS1 is shown in 図 7-57 and described in 表 7-58.

Return to the Summary Table.

This register is the clock ratio detection register 1.

図 7-57. CLK_DET_STS1 Register

7	6	5	4	3	2	1	0
SASI_SAMP_RATE_STS[5:0]						RESERVED	
R-000000b						R-00b	

図 7-57. CLK_DET_STS1 Register (続き)

表 7-58. CLK_DET_STS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	SASI_SAMP_RATE_STS[5:0]	R	0x0	Secondary ASI Sample rate detected status. 0d = Reserved 1d = 768000 (670320-791040) 2d = 614400 (536256-632832) 3d = 512000 (446880-527360) 4d = 438857 (383040-452022) 5d = 384000 (335160-395520) 6d = 341333 (297920-351573) 7d = 307200 (268128-316416) 8d = 256000 (223440-263680) 9d = 219429 (191520-226011) 10d = 192000 (167580-197760) 11d = 170667 (148960-175786) 12d = 153600 (134064-158208) 13d = 128000 (111720-131840) 14d = 109714 (95760-113005) 15d = 96000 (83790-98880) 16d = 85333 (74480-87893) 17d = 76800 (67032-79104) 18d = 64000 (55860-65920) 19d = 54857 (47880-56502) 20d = 48000 (41895-49440) 21d = 42667 (37240-43946) 22d = 38400 (33516-39552) 23d = 32000 (27930-32960) 24d = 27429 (23940-28251) 25d = 24000 (20947-24720) 26d = 21333 (18620-21973) 27d = 19200 (16758-19776) 28d = 16000 (13965-16480) 29d = 13714 (11970-14125) 30d = 12000 (10473-12360) 31d = 10667 (9310-10986) 32d = 9600 (8379-9888) 33d = 8000 (6982-8240) 34d = 6857 (5985-7062) 35d = 6000 (5236-6180) 36d = 5333 (4655-5493) 37d = 4800 (4189-4944) 38d = 4000 (3491-4120) 39d = 3429 (2992-3531) 40d = 3000 (2618-3090) 41d-63d = Reserved
1-0	RESERVED	R	0x0	Reserved bits; Write only reset values

7.1.58 CLK_DET_STS2 Register (Address = 0x40) [Reset = 0x00]

CLK_DET_STS2 is shown in 図 7-58 and described in 表 7-59.

Return to the Summary Table.

This register is the clock ratio detection register 2.

図 7-58. CLK_DET_STS2 Register

7	6	5	4	3	2	1	0
RESERVED		FS_CLKSRC_RATIO_DET_MSB_STS[5:0]					
R-00b		R-000000b					

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表 7-59. CLK_DET_STS2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved bits; Write only reset values
5-0	FS_CLKSRC_RATIO_DET_MSB_STS[5:0]	R	0x0	MSB bits for primary ASI or secondary ASI FSYNC to clock source ratio detected.

7.1.59 CLK_DET_STS3 Register (Address = 0x41) [Reset = 0x00]

CLK_DET_STS3 is shown in 図 7-59 and described in 表 7-60.

Return to the Summary Table.

This register is the clock ratio detection register 3.

図 7-59. CLK_DET_STS3 Register

7	6	5	4	3	2	1	0
FS_CLKSRC_RATIO_DET_LSB_STS[7:0]							
R-00000000b							

表 7-60. CLK_DET_STS3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	FS_CLKSRC_RATIO_DET_LSB_STS[7:0]	R	0x0	LSB byte for primary ASI or secondary ASI FSYNC to clock source ratio detected.

7.1.60 INT_CFG Register (Address = 0x42) [Reset = 0x00]

INT_CFG is shown in 図 7-60 and described in 表 7-61.

Return to the Summary Table.

This regiser is the interrupt configuration register.

図 7-60. INT_CFG Register

7	6	5	4	3	2	1	0
INT_POL	INT_EVENT[1:0]		PD_ON_FLT_CFG[1:0]		LTCH_READ_CFG	PD_ON_FLT_RCV_CFG	LTCH_CLR_ON_READ
R/W-0b	R/W-00b		R/W-00b		R/W-0b	R/W-0b	R/W-0b

表 7-61. INT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_POL	R/W	0x0	Interrupt polarity. 0b = Active low (IRQZ) 1b = Active high (IRQ)
6-5	INT_EVENT[1:0]	R/W	0x0	Interrupt event configuration. 0d = INT asserts on any unmasked latched interrupts event 1d = INT asserts on any unmasked live interrupts event 2d = INT asserts for 2 ms (typical) for every 4-ms (typical) duration on any unmasked latched interrupts event 3d = INT asserts for 2 ms (typical) one time on each pulse for any unmasked interrupts event
4-3	PD_ON_FLT_CFG[1:0]	R/W	0x0	Powerdown configuration during fault for chx and micbias. 0d = Faults are not considered for power down 1d = Only unmasked faults are considered for power down 2d = All faults are considered for powerdown 3d = Reserved

表 7-61. INT_CFG Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
2	LTCH_READ_CFG	R/W	0x0	Interrupt latch registers readback configuration. 0b = All interrupts can be read through the LTCH registers 1b = Only unmasked interrupts can be read through the LTCH registers
1	PD_ON_FLT_RCV_CFG	R/W	0x0	Configuration for Powerdown ADC channels on fault 0b = Auto recovery, ADC channels are re-powered up when fault goes away 1b = Manual recovery, ADC channels are not re-powered up when fault goes away
0	LTCH_CLR_ON_READ	R/W	0x0	Cfgn for clearing LTCH register bits 0 = LTCH reg bits are cleared on reg read only if live status is zero 1 = LTCH reg bits are cleared on reg read irrespective of live status

7.1.61 DAC_FLT_CFG Register (Address = 0x43) [Reset = 0x50]

DAC_FLT_CFG is shown in 図 7-61 and described in 表 7-62.

Return to the Summary Table.

This regiser is the interrupt configuration register.

図 7-61. DAC_FLT_CFG Register

7	6	5	4	3	2	1	0
RESERVED	DAC_PD_ON_FLT_CFG[1:0]		DAC_PD_ON_FLT_RCV_CFG	OUT_CHx_PD_FLT_STS	DAC_DIS_PD_W_PU	DAC_FLT_DET_DIS	AREG_SC_FLAG_DET_DIS
R-0b	R/W-10b		R/W-1b	R-0b	R/W-0b	R/W-0b	R/W-0b

表 7-62. DAC_FLT_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved bit; Write only reset value
6-5	DAC_PD_ON_FLT_CFG[1:0]	R/W	0x2	Powerdown configuration during fault for DAC . 0d = Faults are not considered for power down 1d = Only unmasked faults are considered for power down 2d = All faults are considered for powerdown 3d = Reserved
4	DAC_PD_ON_FLT_RCV_CFG	R/W	0x1	Configuration for Powerdown DAC channels on fault 0b = Auto recovery, DAC channels are re-powered up when fault goes away 1b = Manual recovery, DAC channels are not re-powered up when fault goes away
3	OUT_CHx_PD_FLT_STS	R	0x0	Status for PD on OUTxx faults 0d = No DAC Channel is Powered Down due to fault/s 1d = Some DAC Channel is Powered Down due to fault/s
2	DAC_DIS_PD_W_PU	R/W	0x0	Disable power down on DRVR VG fault while powering up DAC 0b = Power down DAC on DRVR VG fault while power up 1b = Disable power down DAC on DRVR VG fault while power up
1	DAC_FLT_DET_DIS	R/W	0x0	DAC vg_fault/sc_fault detect config 0b = enable 1b = disable
0	AREG_SC_FLAG_DET_DIS	R/W	0x0	AREG short circuit detect config 0b = enable 1b = disable

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7.1.62 ADC_DAC_MISC_CFG Register (Address = 0x4B) [Reset = 0x00]

ADC_DAC_MISC_CFG is shown in 図 7-62 and described in 表 7-63.

Return to the Summary Table.

Option to Mute ADC Channel in Overload Recovery Phase

図 7-62. ADC_DAC_MISC_CFG Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	ADC_CH1_MUTE_ON_OVRLD	ADC_CH2_MUTE_ON_OVRLD	RESERVED		
R-0b	R-0b	R-0b	R/W-0b	R/W-0b	R-000b		

表 7-63. ADC_DAC_MISC_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved bit; Write only reset value
6	RESERVED	R	0x0	Reserved bit; Write only reset value
5	RESERVED	R	0x0	Reserved bit; Write only reset value
4	ADC_CH1_MUTE_ON_OVRLD	R/W	0x0	Mute ADC channel 1 while ADC1 is in Overload Recovery Phase 0b = Disable 1b = Enable
3	ADC_CH2_MUTE_ON_OVRLD	R/W	0x0	Mute ADC channel 2 while ADC2 is in Overload Recovery Phase 0b = Disable 1b = Enable
2-0	RESERVED	R	0x0	Reserved bits; Write only reset values

7.1.63 PWR_TUNE_CFG0 Register (Address = 0x4E) [Reset = 0x00]

PWR_TUNE_CFG0 is shown in 図 7-63 and described in 表 7-64.

Return to the Summary Table.

This register is configuration register for power tune configuration.

図 7-63. PWR_TUNE_CFG0 Register

7	6	5	4	3	2	1	0
ADC_CLK_BY2_MODE	ADC_CIC_ORDER	ADC_FIR_BYPASS	RESERVED		ADC_LOW_PWR_FILT	RESERVED	
R/W-0b	R/W-0b	R/W-0b	R-00b		R/W-0b	R-00b	

表 7-64. PWR_TUNE_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ADC_CLK_BY2_MODE	R/W	0x0	ADC MOD CLK select configuration. 0d = MOD CLK 3MHz 1d = MOD CLK 1.5MHz
6	ADC_CIC_ORDER	R/W	0x0	ADC CIC order configuratoin. 0d = 5th order CIC 1d = 4th order CIC
5	ADC_FIR_BYPASS	R/W	0x0	ADC FIR bypass configuration. 0d = Bypass disable 1d = Bypass enable
4-3	RESERVED	R	0x0	Reserved bits; Write only reset values

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表 7-64. PWR_TUNE_CFG0 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
2	ADC_LOW_PWR_FILT	R/W	0x0	Low Power filter configuration for ADC 0d = Disable 1d = Enable
1-0	RESERVED	R	0x0	Reserved bits; Write only reset values

7.1.64 PWR_TUNE_CFG1 Register (Address = 0x4F) [Reset = 0x00]

PWR_TUNE_CFG1 is shown in 図 7-64 and described in 表 7-65.

Return to the Summary Table.

This register is configuration register for power tune configuration.

図 7-64. PWR_TUNE_CFG1 Register

7	6	5	4	3	2	1	0
DAC_CLK_BY2_MODE	RESERVED	DAC_FIR_SEG_BYPASS	RESERVED		DAC_LOW_PWR_FILT	DAC_POWER_SCAL	RESERVED
R/W-0b	R-0b	R/W-0b	R-00b		R/W-0b	R/W-0b	R-0b

表 7-65. PWR_TUNE_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DAC_CLK_BY2_MODE	R/W	0x0	DAC MOD CLK select configuration. 0d = MOD CLK 3MHz 1d = MOD CLK 1.5MHz
6	RESERVED	R	0x0	Reserved bit; Write only reset value
5	DAC_FIR_SEG_BYPASS	R/W	0x0	DAC FIR and segmenter bypass configuration. 0d = Bypass disable 1d = Bypass enable
4-3	RESERVED	R	0x0	Reserved bits; Write only reset values
2	DAC_LOW_PWR_FILT	R/W	0x0	Low Power Filter configuration for DAC 0d = Disable 1d = Enable
1	DAC_POWER_SCAL	R/W	0x0	DAC IREF select configuration. 0d = Vref/R 1d = Vref/2R
0	RESERVED	R	0x0	Reserved bit; Write only reset value

7.1.65 ADC_CH1_CFG0 Register (Address = 0x50) [Reset = 0x00]

ADC_CH1_CFG0 is shown in 図 7-65 and described in 表 7-66.

Return to the Summary Table.

This register is configuration register 0 for ADC channel 1.

図 7-65. ADC_CH1_CFG0 Register

7	6	5	4	3	2	1	0
ADC_CH1_INSRC[1:0]		RESERVED		RESERVED		ADC_CH1_FULLSCALE_VAL	ADC_CH1_BW_MODE
R/W-00b		R-00b		R-00b		R/W-0b	R/W-0b

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表 7-66. ADC_CH1_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	ADC_CH1_INSRC[1:0]	R/W	0x0	ADC Channel 1 input configuration. 0d = Analog differential input 1d = Analog single-ended input Dont use Dont use
5-4	RESERVED	R	0x0	Reserved bits; Write only reset values
3-2	RESERVED	R	0x0	Reserved bits; Write only reset values
1	ADC_CH1_FULLSCALE_VAL	R/W	0x0	ADC Channel 1 Fullscale value for VREF=2.75 V (applicable for the analog input). 0d = 10 Vrms differential 1d = 5 Vrms differential
0	ADC_CH1_BW_MODE	R/W	0x0	ADC Channel 1 band-width selection. coupling (applicable for the analog input). 0d = audio band-width (24 kHz mode) 1d = wide band-width (96 kHz mode)

7.1.66 ADC_CH1_CFG2 Register (Address = 0x52) [Reset = 0xA1]

ADC_CH1_CFG2 is shown in 図 7-66 and described in 表 7-67.

Return to the Summary Table.

This register is configuration register 2 for ADC channel 1.

図 7-66. ADC_CH1_CFG2 Register

7	6	5	4	3	2	1	0
ADC_CH1_DVOL[7:0]							
R/W-10100001b							

表 7-67. ADC_CH1_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ADC_CH1_DVOL[7:0]	R/W	0xA1	Channel 1 digital volume control. 0d = Digital volume is muted 1d = Digital volume control is set to -80 dB 2d = Digital volume control is set to -79.5 dB 3d to 160d = Digital volume control is set as per configuration 161d = Digital volume control is set to 0 dB 162d = Digital volume control is set to 0.5 dB 163d to 253d = Digital volume control is set as per configuration 254d = Digital volume control is set to 46.5 dB 255d = Digital volume control is set to 47 dB

7.1.67 ADC_CH1_CFG3 Register (Address = 0x53) [Reset = 0x80]

ADC_CH1_CFG3 is shown in 図 7-67 and described in 表 7-68.

Return to the Summary Table.

This register is configuration register 3 for ADC channel 1.

図 7-67. ADC_CH1_CFG3 Register

7	6	5	4	3	2	1	0
ADC_CH1_FGAIN[3:0]				RESERVED			
R/W-1000b				R-0000b			

表 7-68. ADC_CH1_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	ADC_CH1_FGAIN[3:0]	R/W	0x8	ADC channel 1 fine gain calibration. 0d = Fine gain is set to -0.8 dB 1d = Fine gain is set to -0.7 dB 2d = Fine gain is set to -0.6 dB 3d to 7d = Fine gain is set as per configuration 8d = Fine gain is set to 0 dB 9d = Fine gain is set to 0.1 dB 10d to 13d = Fine gain is set as per configuration 14d = Fine gain is set to 0.6 dB 15d = Fine gain is set to 0.7 dB
3-0	RESERVED	R	0x0	Reserved bits; Write only reset value

7.1.68 ADC_CH1_CFG4 Register (Address = 0x54) [Reset = 0x00]

ADC_CH1_CFG4 is shown in 図 7-68 and described in 表 7-69.

Return to the Summary Table.

This register is configuration register 4 for ADC channel 1.

図 7-68. ADC_CH1_CFG4 Register

7	6	5	4	3	2	1	0
ADC_CH1_PCAL[5:0]						PCAL_ANA_DIG_SEL[1:0]	
R/W-000000b						R/W-00b	

表 7-69. ADC_CH1_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	ADC_CH1_PCAL[5:0]	R/W	0x0	ADC channel 1 phase calibration with modulator clock resolution. 0d = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 62d = Phase calibration delay as per configuration 63d = Phase calibration delay is set to 63 cycles of the modulator clock
1-0	PCAL_ANA_DIG_SEL[1:0]	R/W	0x0	PCAL support configuration. 0d = Pcal for both Ana-Dig supported 1d = Pcal for only Ana 2d = Pcal for only Dig 3d = Reserved

7.1.69 ADC_CH2_CFG0 Register (Address = 0x55) [Reset = 0x00]

ADC_CH2_CFG0 is shown in 図 7-69 and described in 表 7-70.

Return to the Summary Table.

This register is configuration register 0 for ADC channel 2.

図 7-69. ADC_CH2_CFG0 Register

7	6	5	4	3	2	1	0
ADC_CH2_INSRC[1:0]		RESERVED		ADC_CH2_CM_TOL[1:0]		ADC_CH2_FULLSCALE_VAL	ADC_CH2_BW_MODE
R/W-00b		R-00b		R/W-00b		R/W-0b	R/W-0b

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表 7-70. ADC_CH2_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	ADC_CH2_INSRC[1:0]	R/W	0x0	ADC Channel 2 input configuration. 0d = Analog differential input 1d = Analog single-ended input Dont use Dont use
5-4	RESERVED	R	0x0	Reserved bits; Write only reset values
3-2	ADC_CH2_CM_TOL[1:0]	R/W	0x0	ADC Channel 2 input coupling (applicable for the analog input). 0d = AC-coupled input with common mode variance tolerance supported 50 mVpp for single ended and 100 mVpp for differential configuration 1d = AC-coupled / DC-coupled input with common mode variance tolerance supported 500 mVpp for single ended and 1 Vpp for differential configuration (Expected SNR degradation of 1-2 dB) 2d = AC-coupled / DC-coupled input with common mode variance tolerance supported rail to rail (supply to ground) (Expected SNR degradation of 3-4 dB , High CMRR supported only in this case) 3d = Reserved
1	ADC_CH2_FULLSCALE_VAL	R/W	0x0	ADC Channel 2 Fullscale value for VREF=2.75 V (applicable for the analog input). 0d = 10 Vrms differential 1d = 5 Vrms differential
0	ADC_CH2_BW_MODE	R/W	0x0	ADC Channel 2 band-width selection. coupling (applicable for the analog input). 0d = audio band-width (24 kHz mode) 1d = wide band-width (96 kHz mode) (Supported only for 40-kΩ input impedance case)

7.1.70 ADC_CH2_CFG2 Register (Address = 0x57) [Reset = 0xA1]

ADC_CH2_CFG2 is shown in 図 7-70 and described in 表 7-71.

Return to the Summary Table.

This register is configuration register 2 for channel 2.

図 7-70. ADC_CH2_CFG2 Register

7	6	5	4	3	2	1	0
ADC_CH2_DVOL[7:0]							
R/W-10100001b							

表 7-71. ADC_CH2_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ADC_CH2_DVOL[7:0]	R/W	0xA1	Channel 1 digital volume control. 0d = Digital volume is muted 1d = Digital volume control is set to -80 dB 2d = Digital volume control is set to -79.5 dB 3d to 160d = Digital volume control is set as per configuration 161d = Digital volume control is set to 0 dB 162d = Digital volume control is set to 0.5 dB 163d to 253d = Digital volume control is set as per configuration 254d = Digital volume control is set to 46.5 dB 255d = Digital volume control is set to 47 dB

7.1.71 ADC_CH2_CFG3 Register (Address = 0x58) [Reset = 0x80]

ADC_CH2_CFG3 is shown in 図 7-71 and described in 表 7-72.

Return to the Summary Table.

This register is configuration register 3 for ADC Channel 2.

図 7-71. ADC_CH2_CFG3 Register

7	6	5	4	3	2	1	0
ADC_CH2_FGAIN[3:0]				RESERVED			
R/W-1000b				R-0000b			

表 7-72. ADC_CH2_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	ADC_CH2_FGAIN[3:0]	R/W	0x8	ADC Channel 2 fine gain calibration. 0d = Fine gain is set to -0.8 dB 1d = Fine gain is set to -0.7 dB 2d = Fine gain is set to -0.6 dB 3d to 7d = Fine gain is set as per configuration 8d = Fine gain is set to 0 dB 9d = Fine gain is set to 0.1 dB 10d to 13d = Fine gain is set as per configuration 14d = Fine gain is set to 0.6 dB 15d = Fine gain is set to 0.7 dB
3-0	RESERVED	R	0x0	Reserved bits; Write only reset value

7.1.72 ADC_CH2_CFG4 Register (Address = 0x59) [Reset = 0x00]

ADC_CH2_CFG4 is shown in 図 7-72 and described in 表 7-73.

Return to the Summary Table.

This register is configuration register 4 for ADC Channel 2.

図 7-72. ADC_CH2_CFG4 Register

7	6	5	4	3	2	1	0
ADC_CH2_PCAL[5:0]						RESERVED	
R/W-000000b						R-00b	

表 7-73. ADC_CH2_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	ADC_CH2_PCAL[5:0]	R/W	0x0	ADC Channel 2 phase calibration with modulator clock resolution. 0d = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 62d = Phase calibration delay as per configuration 63d = Phase calibration delay is set to 63 cycles of the modulator clock
1-0	RESERVED	R	0x0	Reserved bits; Write only reset value

7.1.73 ADC_CH3_CFG0 Register (Address = 0x5A) [Reset = 0x00]

ADC_CH3_CFG0 is shown in 図 7-73 and described in 表 7-74.

Return to the Summary Table.

This register is configuration register 0 for ADC channel 3.

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図 7-73. ADC_CH3_CFG0 Register

7	6	5	4	3	2	1	0
ADC_CH3_CLONE	RESERVED						
R/W-0b	R-0000000b						

表 7-74. ADC_CH3_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ADC_CH3_CLONE	R/W	0x0	ADC Channel 3 input configuration. 0d = clone disabled 1d = Channel 3 Digital Filter Input is generated same as Channel 1 Digital Filter Input (Cloned Input)
6-0	RESERVED	R	0x0	Reserved bits; Write only reset value

7.1.74 ADC_CH3_CFG2 Register (Address = 0x5B) [Reset = 0xA1]

ADC_CH3_CFG2 is shown in 図 7-74 and described in 表 7-75.

Return to the Summary Table.

This register is configuration register 2 for ADC channel 3.

図 7-74. ADC_CH3_CFG2 Register

7	6	5	4	3	2	1	0
ADC_CH3_DVOL[7:0]							
R/W-10100001b							

表 7-75. ADC_CH3_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ADC_CH3_DVOL[7:0]	R/W	0xA1	Channel 3 digital volume control. 0d = Digital volume is muted 1d = Digital volume control is set to -80 dB 2d = Digital volume control is set to -79.5 dB 3d to 160d = Digital volume control is set as per configuration 161d = Digital volume control is set to 0 dB 162d = Digital volume control is set to 0.5 dB 163d to 253d = Digital volume control is set as per configuration 254d = Digital volume control is set to 46.5 dB 255d = Digital volume control is set to 47 dB

7.1.75 ADC_CH3_CFG3 Register (Address = 0x5C) [Reset = 0x80]

ADC_CH3_CFG3 is shown in 図 7-75 and described in 表 7-76.

Return to the Summary Table.

This register is configuration register 3 for ADC channel 3.

図 7-75. ADC_CH3_CFG3 Register

7	6	5	4	3	2	1	0
ADC_CH3_FGAIN[3:0]				RESERVED			
R/W-1000b				R-0000b			

表 7-76. ADC_CH3_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	ADC_CH3_FGAIN[3:0]	R/W	0x8	ADC channel 3 fine gain calibration. 0d = Fine gain is set to -0.8 dB 1d = Fine gain is set to -0.7 dB 2d = Fine gain is set to -0.6 dB 3d to 7d = Fine gain is set as per configuration 8d = Fine gain is set to 0 dB 9d = Fine gain is set to 0.1 dB 10d to 13d = Fine gain is set as per configuration 14d = Fine gain is set to 0.6 dB 15d = Fine gain is set to 0.7 dB
3-0	RESERVED	R	0x0	Reserved bits; Write only reset value

7.1.76 ADC_CH3_CFG4 Register (Address = 0x5D) [Reset = 0x00]

ADC_CH3_CFG4 is shown in 図 7-76 and described in 表 7-77.

Return to the Summary Table.

This register is configuration register 4 for ADC channel 3.

図 7-76. ADC_CH3_CFG4 Register

7	6	5	4	3	2	1	0
ADC_CH3_PCAL[5:0]						RESERVED	
R/W-000000b						R-00b	

表 7-77. ADC_CH3_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	ADC_CH3_PCAL[5:0]	R/W	0x0	ADC channel 3 phase calibration with modulator clock resolution. 0d = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 62d = Phase calibration delay as per configuration 63d = Phase calibration delay is set to 63 cycles of the modulator clock
1-0	RESERVED	R	0x0	Reserved bits; Write only reset value

7.1.77 ADC_CH4_CFG0 Register (Address = 0x5E) [Reset = 0x00]

ADC_CH4_CFG0 is shown in 図 7-77 and described in 表 7-78.

Return to the Summary Table.

This register is configuration register 0 for ADC Channel 4.

図 7-77. ADC_CH4_CFG0 Register

7	6	5	4	3	2	1	0
ADC_CH4_CLONE	RESERVED						
R/W-0b	R-0000000b						

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表 7-78. ADC_CH4_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ADC_CH4_CLONE	R/W	0x0	ADC Channel 4 input configuration. 0d = clone disabled 1d = Channel 4 Digital Filter Input is generated same as Channel 2 Digital Filter Input (Cloned Input)
6-0	RESERVED	R	0x0	Reserved bits; Write only reset value

7.1.78 ADC_CH4_CFG2 Register (Address = 0x5F) [Reset = 0xA1]

ADC_CH4_CFG2 is shown in 図 7-78 and described in 表 7-79.

Return to the Summary Table.

This register is configuration register 2 for channel 4.

図 7-78. ADC_CH4_CFG2 Register

7	6	5	4	3	2	1	0
ADC_CH4_DVOL[7:0]							
R/W-10100001b							

表 7-79. ADC_CH4_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ADC_CH4_DVOL[7:0]	R/W	0xA1	Channel 4 digital volume control. 0d = Digital volume is muted 1d = Digital volume control is set to -80 dB 2d = Digital volume control is set to -79.5 dB 3d to 160d = Digital volume control is set as per configuration 161d = Digital volume control is set to 0 dB 162d = Digital volume control is set to 0.5 dB 163d to 253d = Digital volume control is set as per configuration 254d = Digital volume control is set to 46.5 dB 255d = Digital volume control is set to 47 dB

7.1.79 ADC_CH4_CFG3 Register (Address = 0x60) [Reset = 0x80]

ADC_CH4_CFG3 is shown in 図 7-79 and described in 表 7-80.

Return to the Summary Table.

This register is configuration register 3 for ADC Channel 4.

図 7-79. ADC_CH4_CFG3 Register

7	6	5	4	3	2	1	0
ADC_CH4_FGAIN[3:0]				RESERVED			
R/W-1000b				R-0000b			

表 7-80. ADC_CH4_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	ADC_CH4_FGAIN[3:0]	R/W	0x8	ADC Channel 4 fine gain calibration. 0d = Fine gain is set to -0.8 dB 1d = Fine gain is set to -0.7 dB 2d = Fine gain is set to -0.6 dB 3d to 7d = Fine gain is set as per configuration 8d = Fine gain is set to 0 dB 9d = Fine gain is set to 0.1 dB 10d to 13d = Fine gain is set as per configuration 14d = Fine gain is set to 0.6 dB 15d = Fine gain is set to 0.7 dB
3-0	RESERVED	R	0x0	Reserved bits; Write only reset value

7.1.80 ADC_CH4_CFG4 Register (Address = 0x61) [Reset = 0x00]

ADC_CH4_CFG4 is shown in 図 7-80 and described in 表 7-81.

Return to the Summary Table.

This register is configuration register 4 for ADC Channel 4.

図 7-80. ADC_CH4_CFG4 Register

7	6	5	4	3	2	1	0
ADC_CH4_PCAL[5:0]						RESERVED	
R/W-000000b						R-00b	

表 7-81. ADC_CH4_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	ADC_CH4_PCAL[5:0]	R/W	0x0	ADC Channel 4 phase calibration with modulator clock resolution. 0d = No phase calibration 1d = Phase calibration delay is set to one cycle of the modulator clock 2d = Phase calibration delay is set to two cycles of the modulator clock 3d to 62d = Phase calibration delay as per configuration 63d = Phase calibration delay is set to 63 cycles of the modulator clock
1-0	RESERVED	R	0x0	Reserved bits; Write only reset value

7.1.81 OUT1x_CFG0 Register (Address = 0x64) [Reset = 0x20]

OUT1x_CFG0 is shown in 図 7-81 and described in 表 7-82.

Return to the Summary Table.

This register is configuration register 0 for Channel OUT1x.

図 7-81. OUT1x_CFG0 Register

7	6	5	4	3	2	1	0
OUT1x_SRC[2:0]			OUT1x_CFG[2:0]			OUT1x_VCOM	OUT1x_LP_MODE
R/W-001b			R/W-000b			R/W-0b	R/W-0b

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表 7-82. OUT1x_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	OUT1x_SRC[2:0]	R/W	0x1	OUT1x Source Configuration. 0d = Output driver disabled 1d = Input from DAC signal chain 2d = Input from Analog bypass path 3d = Input from both DAC signal chain and Analog bypass path 4d = Independent input from both DAC signal chain and Analog bypass path (DAC -> OUT1P , IN1P -> OUT1M) 5d = Independent input from both DAC signal chain and Analog bypass path (IN1M -> OUT1P, DAC -> OUT1M) 6d-7d = Reserved; Don't use
4-2	OUT1x_CFG[2:0]	R/W	0x0	OUT1x DAC / Analog Bypass Routing Configuration. (Don't use if OUT1x_SRC configured 4d or 5d) 0d = Differential (DAC1AP + DAC1BP / IN1M -> OUT1P ; DAC1AM + DAC1BM / IN1P -> OUT1M) 1d = Stereo single-ended (DAC1A / IN1M -> OUT1P ; DAC1B / IN1P -> OUT1M) 2d = Mono single-ended with output at OUT1P only (DAC1A + DAC1B / IN1M-> OUT1P) 3d = Mono single-ended with output at OUT1M only (DAC1A + DAC1B / IN1P -> OUT1M) 4d = Pseudo differential with OUT1M as VCOM (DAC1A, DAC1B / IN1M -> OUT1P, VCOM -> OUT1M) 5d = Pseudo differential with OUT1M as VCOM and OUT2M for external sensing (DAC1A, DAC1B / IN1M -> OUT1P, VCOM -> OUT1M) 6d = Pseudo differential with OUT1P as VCOM (IN1P -> OUT1M, VCOM -> OUT1P) 7d = Reserved; Don't use
1	OUT1x_VCOM	R/W	0x0	Channel OUT1x VCOM configuration. 0d = 0.6 * Vref (for 1.375V VREF mode alone as 0.654*Vref) 1d = AVDD by 2
0	OUT1x_LP_MODE	R/W	0x0	Low power mode of OUT1x channel. (only valid for OUT1x_SRC configured as DAC signal chain) (not valid for OUT1x_CFG configured as Stereo SE) 0d = Low power mode is disabled (3 dB higher perf) 1d = Low power mode is enabled

7.1.82 OUT1x_CFG1 Register (Address = 0x65) [Reset = 0x20]

OUT1x_CFG1 is shown in 図 7-82 and described in 表 7-83.

Return to the Summary Table.

This register is configuration register 1 for Channel OUT1x.

図 7-82. OUT1x_CFG1 Register

7	6	5	4	3	2	1	0
OUT1P_DRIVE[1:0]		OUT1P_LVL_CTRL[2:0]			RESERVED	RESERVED	DAC_CH1_BW_MODE
R/W-00b		R/W-100b			R-0b	R-0b	R/W-0b

表 7-83. OUT1x_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	OUT1P_DRIVE[1:0]	R/W	0x0	Channel OUT1P drive configuration. 0d = Line out driver with minimum 300 Ω impedance 1d = Headphone driver with minimum 4 Ω impedance 2d = 4 Ω 3d = FD Receiver/Debug

表 7-83. OUT1x_CFG1 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
5-3	OUT1P_LVL_CTRL[2:0]	R/W	0x4	Channel OUT1P level control configuration Dont use Dont use Dont use Dont use 4d = -8 dB 5d = -14 dB 6d = -20 dB 7d = -26 dB
2	RESERVED	R	0x0	Reserved bit; Write only reset value
1	RESERVED	R	0x0	Reserved bit; Write only reset value
0	DAC_CH1_BW_MODE	R/W	0x0	DAC Channel 1 band-width selection. 0d = audio band-width (24 kHz mode) 1d = wide band-width (96 kHz mode)

7.1.83 OUT1x_CFG2 Register (Address = 0x66) [Reset = 0x20]

OUT1x_CFG2 is shown in 図 7-83 and described in 表 7-84.

Return to the Summary Table.

This register is configuration register 2 for Channel OUT2x.

図 7-83. OUT1x_CFG2 Register

7	6	5	4	3	2	1	0
OUT1M_DRIVE[1:0]		OUT1M_LVL_CTRL[2:0]			RESERVED	DAC_CH1_FULLSCALE_VAL	DAC_CH1_CM_TOL
R/W-00b		R/W-100b			R-0b	R/W-0b	R/W-0b

表 7-84. OUT1x_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	OUT1M_DRIVE[1:0]	R/W	0x0	Channel OUT1M drive configuration. 0d = Line out driver with minimum 300 Ω impedance 1d = Headphone driver with minimum 4 Ω impedance 2d = 4 Ω 3d = FD Receiver/Debug
5-3	OUT1M_LVL_CTRL[2:0]	R/W	0x4	Channel OUT1M level control configuration. Dont use Dont use Dont use Dont use 4d = -8 dB 5d = -14 dB 6d = -20 dB 7d = -26 dB
2	RESERVED	R	0x0	Reserved bit; Write only reset value
1	DAC_CH1_FULLSCALE_VAL	R/W	0x0	DAC Channel 1 Fullscale value for VREF=2.75 V 0d = 10 Vrms differential 1d = 5 Vrms differential
0	DAC_CH1_CM_TOL	R/W	0x0	DAC Channel 1 input coupling (applicable for the analog input). 0d = AC-coupled input with common mode variance tolerance supported 50 mVpp for single ended and 100 mVpp for differential configuration 1d = AC-coupled / DC-coupled input with common mode variance tolerance supported rail to rail (supply to ground) (Expected SNR degradation of 3-4 dB , High CMRR supported only in this case)

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7.1.84 DAC_CH1A_CFG0 Register (Address = 0x67) [Reset = 0xC9]

DAC_CH1A_CFG0 is shown in 図 7-84 and described in 表 7-85.

Return to the Summary Table.

This register is configuration register 0 for DAC channel 1A.

図 7-84. DAC_CH1A_CFG0 Register

7	6	5	4	3	2	1	0
DAC_CH1A_DVOL[7:0]							
R/W-11001001b							

表 7-85. DAC_CH1A_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DAC_CH1A_DVOL[7:0]	R/W	0xC9	Channel 1A digital volume control. 0d = Digtial Volume is muted 1d = Digital Volume Control set to -100 dB 2d = Digital Volume Control set to -99.5 dB 3d to 200d = Digital Volume Control set to as per configuration 201d = Digital Volume Control set to 0 dB 202d = Digital Volume Control set to +0.5 dB 203d to 253d = Digital Volume Control set to as per configuration 254d = Digital Volume Control set to +26.5 dB 255d = Digital Volume Control set to +27 dB

7.1.85 DAC_CH1A_CFG1 Register (Address = 0x68) [Reset = 0x80]

DAC_CH1A_CFG1 is shown in 図 7-85 and described in 表 7-86.

Return to the Summary Table.

This register is configuration register 1 for DAC channel 1A.

図 7-85. DAC_CH1A_CFG1 Register

7	6	5	4	3	2	1	0
DAC_CH1A_FGAIN[3:0]				RESERVED			
R/W-1000b				R-0000b			

表 7-86. DAC_CH1A_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DAC_CH1A_FGAIN[3:0]	R/W	0x8	DAC channel 1A fine gain calibration. 0d = Fine gain is set to -0.8 dB 1d = Fine gain is set to -0.7 dB 2d = Fine gain is set to -0.6 dB 3d to 7d = Fine gain is set as per configuration 8d = Fine gain is set to 0 dB 9d = Fine gain is set to 0.1 dB 10d to 13d = Fine gain is set as per configuration 14d = Fine gain is set to 0.6 dB 15d = Fine gain is set to 0.7 dB
3-0	RESERVED	R	0x0	Reserved bits; Write only reset value

7.1.86 DAC_CH1B_CFG0 Register (Address = 0x69) [Reset = 0xC9]

DAC_CH1B_CFG0 is shown in 図 7-86 and described in 表 7-87.

Return to the Summary Table.

This register is configuration register 0 for DAC channel 1B.

図 7-86. DAC_CH1B_CFG0 Register

7	6	5	4	3	2	1	0
DAC_CH1B_DVOL[7:0]							
R/W-11001001b							

表 7-87. DAC_CH1B_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DAC_CH1B_DVOL[7:0]	R/W	0xC9	Channel 1B digital volume control. 0d = Digtial Volume is muted 1d = Digital Volume Control set to -100 dB 2d = Digital Volume Control set to -99.5 dB 3d to 200d = Digital Volume Control set to as per configuration 201d = Digital Volume Control set to 0 dB 202d = Digital Volume Control set to +0.5 dB 203d to 253d = Digital Volume Control set to as per configuration 254d = Digital Volume Control set to +26.5 dB 255d = Digital Volume Control set to +27 dB

7.1.87 DAC_CH1B_CFG1 Register (Address = 0x6A) [Reset = 0x80]

DAC_CH1B_CFG1 is shown in 図 7-87 and described in 表 7-88.

Return to the Summary Table.

This register is configuration register 1 for DAC channel 1B.

図 7-87. DAC_CH1B_CFG1 Register

7	6	5	4	3	2	1	0
DAC_CH1B_FGAIN[3:0]				RESERVED			
R/W-1000b				R-0000b			

表 7-88. DAC_CH1B_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DAC_CH1B_FGAIN[3:0]	R/W	0x8	DAC channel 1B fine gain calibration. 0d = Fine gain is set to -0.8 dB 1d = Fine gain is set to -0.7 dB 2d = Fine gain is set to -0.6 dB 3d to 7d = Fine gain is set as per configuration 8d = Fine gain is set to 0 dB 9d = Fine gain is set to 0.1 dB 10d to 13d = Fine gain is set as per configuration 14d = Fine gain is set to 0.6 dB 15d = Fine gain is set to 0.7 dB
3-0	RESERVED	R	0x0	Reserved bits; Write only reset value

7.1.88 OUT2x_CFG0 Register (Address = 0x6B) [Reset = 0x20]

OUT2x_CFG0 is shown in 図 7-88 and described in 表 7-89.

Return to the Summary Table.

This register is configuration register 0 for Channel OUT2x.

図 7-88. OUT2x_CFG0 Register

7	6	5	4	3	2	1	0

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図 7-88. OUT2x_CFG0 Register (続き)

OUT2x_SRC[2:0]	OUT2x_CFG[2:0]	OUT2x_VCOM	OUT2x_LP_MODE
R/W-001b	R/W-000b	R/W-0b	R/W-0b

表 7-89. OUT2x_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	OUT2x_SRC[2:0]	R/W	0x1	OUT2x Source Configuration. 0d = Output driver disabled 1d = Input from DAC signal chain 2d = Input from Analog bypass path 3d = Input from both DAC signal chain and Analog bypass path 4d = Independent input from both DAC signal chain and Analog bypass path (DAC -> OUT2P , IN2P -> OUT2M) 5d = Independent input from both DAC signal chain and Analog bypass path (IN2M -> OUT2P, DAC -> OUT2M) 6d-7d = Reserved; Don't use
4-2	OUT2x_CFG[2:0]	R/W	0x0	OUT2x DAC / Analog Bypass Routing Configuration. (Don't use if OUT1x_SRC configured 4d or 5d) 0d = Differential (DAC2AP + DAC2BP / IN2M -> OUT2P ; DAC2AM + DAC2BM / IN2P -> OUT2M) 1d = Stereo single-ended (DAC2A / IN2M -> OUT2P ; DAC2B / IN2P -> OUT2M) 2d = Mono single-ended with output at OUT2P only (DAC2A + DAC2B / IN2M-> OUT2P) 3d = Mono single-ended with output at OUT2M only (DAC2A + DAC2B / IN2P -> OUT2M) 4d = Pseudo differential with OUT2M as VCOM (DAC2A, DAC2B / IN2M -> OUT2P, VCOM -> OUT2M) 5d =Reserved; Don't use 6d = Pseudo differential with OUT2P as VCOM (IN2P -> OUT2M, VCOM -> OUT2P) 7d = Reserved; Don't use
1	OUT2x_VCOM	R/W	0x0	Channel OUT2x VCOM configuration. 0d = 0.6 * Vref (for 1.375V VREF mode alone as 0.654*Vref) 2d = AVDD by 2
0	OUT2x_LP_MODE	R/W	0x0	Low power mode of OUT2x channel. (only valid for OUT2x_SRC configured as DAC signal chain) (not valid for OUT2x_CFG configured as Stereo SE) 0d = Low power mode is disabled (3 dB higher perf) 1d = Low power mode is enabled

7.1.89 OUT2x_CFG1 Register (Address = 0x6C) [Reset = 0x20]

OUT2x_CFG1 is shown in 図 7-89 and described in 表 7-90.

Return to the Summary Table.

This register is configuration register 1 for Channel OUT2x.

図 7-89. OUT2x_CFG1 Register

7	6	5	4	3	2	1	0
OUT2P_DRIVE[1:0]		OUT2P_LVL_CTRL[2:0]			RESERVED	RESERVED	DAC_CH2_BW_MODE
R/W-00b		R/W-100b			R-0b	R-0b	R/W-0b

表 7-90. OUT2x_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	OUT2P_DRIVE[1:0]	R/W	0x0	Channel OUT2P drive configuration. 0d = Line out driver with minimum 300 Ω impedance 1d = Headphone driver with minimum 4 Ω impedance 2d = 4 Ω 3d = FD Receiver/Debug
5-3	OUT2P_LVL_CTRL[2:0]	R/W	0x4	Channel OUT2P level control configuration. Dont use Dont use Dont use Dont use 4d = -8 dB 5d = -14 dB 6d = -20 dB 7d = -26 dB
2	RESERVED	R	0x0	Reserved bit; Write only reset value
1	RESERVED	R	0x0	Reserved bit; Write only reset value
0	DAC_CH2_BW_MODE	R/W	0x0	DAC Channel 2 band-width selection. 0d = audio band-width (24 kHz mode) 1d = wide band-width (96 kHz mode)

7.1.90 OUT2x_CFG2 Register (Address = 0x6D) [Reset = 0x20]

OUT2x_CFG2 is shown in 図 7-90 and described in 表 7-91.

Return to the Summary Table.

This register is configuration register 2 for Channel OUT2x.

図 7-90. OUT2x_CFG2 Register

7	6	5	4	3	2	1	0
OUT2M_DRIVE[1:0]		OUT2M_LVL_CTRL[2:0]			RESERVED	DAC_CH2_FULLSCALE_VAL	DAC_CH2_CM_TOL
R/W-00b		R/W-100b			R-0b	R/W-0b	R/W-0b

表 7-91. OUT2x_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	OUT2M_DRIVE[1:0]	R/W	0x0	Channel OUT2M drive configuration. 0d = Line out driver with minimum 300 Ω impedance 1d = Headphone driver with minimum 4 Ω impedance 2d = 4 Ω 3d = FD Receiver/Debug
5-3	OUT2M_LVL_CTRL[2:0]	R/W	0x4	Channel OUT2M level control configuration. Dont use Dont use Dont use Dont use 4d = -8 dB 5d = -14 dB 6d = -20 dB 7d = -26 dB
2	RESERVED	R	0x0	Reserved bit; Write only reset value
1	DAC_CH2_FULLSCALE_VAL	R/W	0x0	DAC Channel 2 Fullscale value for VREF=2.75 V 0d = 10 Vrms differential 1d = 5 Vrms differential

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表 7-91. OUT2x_CFG2 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
0	DAC_CH2_CM_TOL	R/W	0x0	DAC Channel 2 input coupling (applicable for the analog input). 0d = AC-coupled input with common mode variance tolerance supported 50 mVpp for single ended and 100 mVpp for differential configuration 1d = AC-coupled / DC-coupled input with common mode variance tolerance supported rail to rail (supply to ground) (Expected SNR degradation of 3-4 dB , High CMRR supported only in this case)

7.1.91 DAC_CH2A_CFG0 Register (Address = 0x6E) [Reset = 0xC9]

DAC_CH2A_CFG0 is shown in 図 7-91 and described in 表 7-92.

Return to the Summary Table.

This register is configuration register 0 for DAC channel 2A.

図 7-91. DAC_CH2A_CFG0 Register

7	6	5	4	3	2	1	0
DAC_CH2A_DVOL[7:0]							
R/W-11001001b							

表 7-92. DAC_CH2A_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DAC_CH2A_DVOL[7:0]	R/W	0xC9	Channel 2A digital volume control. 0d = Digtial Volume is muted 1d = Digital Volume Control set to -100 dB 2d = Digital Volume Control set to -99.5 dB 3d to 200d = Digital Volume Control set to as per configuration 201d = Digital Volume Control set to 0 dB 202d = Digital Volume Control set to +0.5 dB 203d to 253d = Digital Volume Control set to as per configuration 254d = Digital Volume Control set to +26.5 dB 255d = Digital Volume Control set to +27 dB

7.1.92 DAC_CH2A_CFG1 Register (Address = 0x6F) [Reset = 0x80]

DAC_CH2A_CFG1 is shown in 図 7-92 and described in 表 7-93.

Return to the Summary Table.

This register is configuration register 1 for DAC channel 2A.

図 7-92. DAC_CH2A_CFG1 Register

7	6	5	4	3	2	1	0
DAC_CH2A_FGAIN[3:0]				RESERVED			
R/W-1000b				R-0000b			

表 7-93. DAC_CH2A_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DAC_CH2A_FGAIN[3:0]	R/W	0x8	DAC channel 2A fine gain calibration. 0d = Fine gain is set to -0.8 dB 1d = Fine gain is set to -0.7 dB 2d = Fine gain is set to -0.6 dB 3d to 7d = Fine gain is set as per configuration 8d = Fine gain is set to 0 dB 9d = Fine gain is set to 0.1 dB 10d to 13d = Fine gain is set as per configuration 14d = Fine gain is set to 0.6 dB 15d = Fine gain is set to 0.7 dB
3-0	RESERVED	R	0x0	Reserved bits; Write only reset value

7.1.93 DAC_CH2B_CFG0 Register (Address = 0x70) [Reset = 0xC9]

DAC_CH2B_CFG0 is shown in 図 7-93 and described in 表 7-94.

Return to the Summary Table.

This register is configuration register 0 for DAC channel 2B.

図 7-93. DAC_CH2B_CFG0 Register

7	6	5	4	3	2	1	0
DAC_CH2B_DVOL[7:0]							
R/W-11001001b							

表 7-94. DAC_CH2B_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DAC_CH2B_DVOL[7:0]	R/W	0xC9	Channel 2B digital volume control. 0d = Digtial Volume is muted 1d = Digital Volume Control set to -100 dB 2d = Digital Volume Control set to -99.5 dB 3d to 200d = Digital Volume Control set to as per configuration 201d = Digital Volume Control set to 0 dB 202d = Digital Volume Control set to +0.5 dB 203d to 253d = Digital Volume Control set to as per configuration 254d = Digital Volume Control set to +26.5 dB 255d = Digital Volume Control set to +27 dB

7.1.94 DAC_CH2B_CFG1 Register (Address = 0x71) [Reset = 0x80]

DAC_CH2B_CFG1 is shown in 図 7-94 and described in 表 7-95.

Return to the Summary Table.

This register is configuration register 1 for DAC channel 2B.

図 7-94. DAC_CH2B_CFG1 Register

7	6	5	4	3	2	1	0
DAC_CH2B_FGAIN[3:0]				RESERVED			
R/W-1000b				R-0000b			

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表 7-95. DAC_CH2B_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DAC_CH2B_FGAIN[3:0]	R/W	0x8	DAC channel 2B fine gain calibration. 0d = Fine gain is set to -0.8 dB 1d = Fine gain is set to -0.7 dB 2d = Fine gain is set to -0.6 dB 3d to 7d = Fine gain is set as per configuration 8d = Fine gain is set to 0 dB 9d = Fine gain is set to 0.1 dB 10d to 13d = Fine gain is set as per configuration 14d = Fine gain is set to 0.6 dB 15d = Fine gain is set to 0.7 dB
3-0	RESERVED	R	0x0	Reserved bits; Write only reset value

7.1.95 DSP_CFG0 Register (Address = 0x72) [Reset = 0x18]

DSP_CFG0 is shown in 図 7-95 and described in 表 7-96.

Return to the Summary Table.

This register is the digital signal processor (DSP) configuration register 0.

図 7-95. DSP_CFG0 Register

7	6	5	4	3	2	1	0
ADC_DSP_DECI_FILT[1:0]		ADC_DSP_HPF_SEL[1:0]		ADC_DSP_BQ_CFG[1:0]		ADC_DSP_DISABLE_SOFT_STEP	ADC_DSP_DVOL_GANG
R/W-00b		R/W-01b		R/W-10b		R/W-0b	R/W-0b

表 7-96. DSP_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	ADC_DSP_DECI_FILT[1:0]	R/W	0x0	ADC channel decimation filter response. 0d = Linear phase 1d = Low latency 2d = Ultra-low latency 3d = Reserved; Don't use
5-4	ADC_DSP_HPF_SEL[1:0]	R/W	0x1	ADC channel high-pass filter (HPF) selection. 0d = Programmable first-order IIR filter for a custom HPF with default coefficient values in P10_R120-127 and P11_R8-11 set as the all-pass filter 1d = HPF with a cutoff of 0.00002 x f_S (1 Hz at f_S = 48 kHz) is selected 2d = HPF with a cutoff of 0.00025 x f_S (12 Hz at f_S = 48 kHz) is selected 3d = HPF with a cutoff of 0.002 x f_S (96 Hz at f_S = 48 kHz) is selected
3-2	ADC_DSP_BQ_CFG[1:0]	R/W	0x2	Number of biquads per ADC channel configuration. 0d = No biquads per channel; biquads are all disabled 1d = 1 biquad per channel 2d = 2 biquads per channel 3d = 3 biquads per channel
1	ADC_DSP_DISABLE_SOFT_STEP	R/W	0x0	ADC Soft-stepping disable during DVOL change, mute, and unmute. 0d = Soft-stepping enabled 1d = Soft-stepping disabled
0	ADC_DSP_DVOL_GANG	R/W	0x0	DVOL control ganged across ADC channels. 0d = Each channel has its own DVOL CTRL settings as programmed in the ADC_CHx_DVOL bits 1d = All active channels must use the channel 1 DVOL setting (ADC_CH1_DVOL) irrespective of whether channel 1 is turned on or not

7.1.96 DSP_CFG1 Register (Address = 0x73) [Reset = 0x18]

DSP_CFG1 is shown in 図 7-96 and described in 表 7-97.

Return to the Summary Table.

This register is the digital signal processor (DSP) configuration register 0.

図 7-96. DSP_CFG1 Register

7	6	5	4	3	2	1	0
DAC_DSP_INTX_FILT[1:0]		DAC_DSP_HPF_SEL[1:0]		DAC_DSP_BQ_CFG[1:0]		DAC_DSP_DISABLE_SOFT_STEP	DAC_DSP_DVOL_GANG
R/W-00b		R/W-01b		R/W-10b		R/W-0b	R/W-0b

表 7-97. DSP_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DAC_DSP_INTX_FILT[1:0]	R/W	0x0	DAC channel decimation filter response. 0d = Linear phase 1d = Low latency 2d = Ultra-low latency 3d = Reserved; Don't use
5-4	DAC_DSP_HPF_SEL[1:0]	R/W	0x1	DAC channel high-pass filter (HPF) selection. 0d = Programmable first-order IIR filter for a custom HPF with default coefficient values in P17_R120-127 and P18_R8-11 set as the all-pass filter 1d = HPF with a cutoff of 0.00002 x f_S (1 Hz at f_S = 48 kHz) is selected 2d = HPF with a cutoff of 0.00025 x f_S (12 Hz at f_S = 48 kHz) is selected 3d = HPF with a cutoff of 0.002 x f_S (96 Hz at f_S = 48 kHz) is selected
3-2	DAC_DSP_BQ_CFG[1:0]	R/W	0x2	Number of biquads per DAC channel configuration. 0d = No biquads per channel; biquads are all disabled 1d = 1 biquad per channel 2d = 2 biquads per channel 3d = 3 biquads per channel
1	DAC_DSP_DISABLE_SOFT_STEP	R/W	0x0	DAC Soft-stepping disable during DVOL change, mute, and unmute. 0d = Soft-stepping enabled 1d = Soft-stepping disabled
0	DAC_DSP_DVOL_GANG	R/W	0x0	DVOL control ganged across DAC channels. 0d = Each DAC channel has its own DVOL CTRL settings as programmed in the DAC_CHx_DVOL bits 1d = All active channels must use the channel 1 DVOL setting (DAC_CH1_DVOL) irrespective of whether channel 1 is turned on or not

7.1.97 CH_EN Register (Address = 0x76) [Reset = 0xCC]

CH_EN is shown in 図 7-97 and described in 表 7-98.

Return to the Summary Table.

This register is the channel enable configuration register.

図 7-97. CH_EN Register

7	6	5	4	3	2	1	0
IN_CH1_EN	IN_CH2_EN	IN_CH3_EN	IN_CH4_EN	OUT_CH1_EN	OUT_CH2_EN	OUT_CH3_EN	OUT_CH4_EN
R/W-1b	R/W-1b	R/W-0b	R/W-0b	R/W-1b	R/W-1b	R/W-0b	R/W-0b

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表 7-98. CH_EN Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IN_CH1_EN	R/W	0x1	Input channel 1 enable setting. 0d = Input channel 1 is disabled 1d = Input channel 1 is enabled
6	IN_CH2_EN	R/W	0x1	Input channel 2 enable setting. 0d = Input channel 2 is disabled 1d = Input channel 2 is enabled
5	IN_CH3_EN	R/W	0x0	Input channel 3 enable setting. 0d = Input channel 3 is disabled 1d = Input channel 3 is enabled
4	IN_CH4_EN	R/W	0x0	Input channel 4 enable setting. 0d = Input channel 4 is disabled 1d = Input channel 4 is enabled
3	OUT_CH1_EN	R/W	0x1	Output channel 1 enable setting. 0d = Output channel 1 is disabled 1d = Output channel 1 is enabled
2	OUT_CH2_EN	R/W	0x1	Output channel 2 enable setting. 0d = Output channel 2 is disabled 1d = Output channel 2 is enabled
1	OUT_CH3_EN	R/W	0x0	Output channel 3 enable setting. 0d = Output channel 3 is disabled 1d = Output channel 3 is enabled
0	OUT_CH4_EN	R/W	0x0	Output channel 4 enable setting. 0d = Output channel 4 is disabled 1d = Output channel 4 is enabled

7.1.98 DYN_PUPD_CFG Register (Address = 0x77) [Reset = 0x00]

DYN_PUPD_CFG is shown in 図 7-98 and described in 表 7-99.

Return to the Summary Table.

This register is the power-up configuration register.

図 7-98. DYN_PUPD_CFG Register

7	6	5	4	3	2	1	0
ADC_DYN_PUPD_EN	ADC_DYN_MAXCH_SEL	DAC_DYN_PUPD_EN	DAC_DYN_MAXCH_SEL	DYN_PUPD_ADC_PDM_DIFF_CLK	RESERVED		
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R-000b		

表 7-99. DYN_PUPD_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ADC_DYN_PUPD_EN	R/W	0x0	Dynamic channel power-up, power-down enable for record path. 0d = Channel power-up, power-down is not supported if any channel recording is on 1d = Channel can be powered up or down individually, even if channel recording is on
6	ADC_DYN_MAXCH_SEL	R/W	0x0	Dynamic mode maximum channel select configuration for record path. 0d = Channel 1 and channel 2 are used with dynamic channel power-up, power-down feature enabled 1d = Channel 1 to channel 4 are used with dynamic channel power-up, power-down feature enabled

表 7-99. DYN_PUPD_CFG Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
5	DAC_DYN_PUPD_EN	R/W	0x0	Dynamic channel power-up, power-down enable for playback path. 0d = Channel power-up, power-down is not supported if any channel playback is on 1d = Channel can be powered up or down individually, even if channel playback is on
4	DAC_DYN_MAXCH_SEL	R/W	0x0	Dynamic mode maximum channel select configuration for playback path. 0d = Channel 1 and channel 2 are used with dynamic channel power-up, power-down feature enabled 1d = Channel 1 to channel 4 are used with dynamic channel power-up, power-down feature enabled
3	DYN_PUPD_ADC_PDM_DIFF_CLK	R/W	0x0	Dynamic power-up power-down with different adc mod clock and pdm clock configuration. 0d = Same ADC MOD CLK and PDM CLK in dynamic pupd 1d = Different ADC MOD CLK and PDM CLK in dynamic pupd
2-0	RESERVED	R	0x0	Reserved bits; Write only reset value

7.1.99 PWR_CFG Register (Address = 0x78) [Reset = 0x00]

PWR_CFG is shown in 図 7-99 and described in 表 7-100.

Return to the Summary Table.

This register is the power-up configuration register.

図 7-99. PWR_CFG Register

7	6	5	4	3	2	1	0
ADC_PDZ	DAC_PDZ	MICBIAS_PDZ	RESERVED	UAD_EN	VAD_EN	UAG_EN	RESERVED
R/W-0b	R/W-0b	R/W-0b	R-0b	R/W-0b	R/W-0b	R/W-0b	R-0b

表 7-100. PWR_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ADC_PDZ	R/W	0x0	Power control for ADC and PDM channels. 0d = Power down all ADC and PDM channels 1d = Power up all enabled ADC and PDM channels
6	DAC_PDZ	R/W	0x0	Power control for DAC channels. 0d = Power down all DAC channels 1d = Power up all enabled DAC channels
5	MICBIAS_PDZ	R/W	0x0	Power control for MICBIAS. 0d = Power down MICBIAS 1d = Power up MICBIAS
4	RESERVED	R	0x0	Reserved bit; Write only reset value
3	UAD_EN	R/W	0x0	Enable ultrasound activity detection (UAD) algorithm. 0d = UAD is disabled 1d = UAD is enabled
2	VAD_EN	R/W	0x0	Enable voice activity detection (VAD) algorithm. 0d = VAD is disabled 1d = VAD is enabled
1	UAG_EN	R/W	0x0	Enable ultrasound activity detection (UAG) algorithm. 0d = UAG is disabled 1d = UAG is enabled
0	RESERVED	R	0x0	Reserved bit; Write only reset value

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7.1.100 DEV_STS0 Register (Address = 0x79) [Reset = 0x00]

DEV_STS0 is shown in 図 7-100 and described in 表 7-101.

Return to the Summary Table.

This register is the device status value register 0.

図 7-100. DEV_STS0 Register

7	6	5	4	3	2	1	0
IN_CH1_STATUS	IN_CH2_STATUS	IN_CH3_STATUS	IN_CH4_STATUS	OUT_CH1_STATUS	OUT_CH2_STATUS	OUT_CH3_STATUS	OUT_CH4_STATUS
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 7-101. DEV_STS0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IN_CH1_STATUS	R	0x0	ADC or PDM channel 1 power status. 0d = ADC or PDM channel is powered down 1d = ADC or PDM channel is powered up
6	IN_CH2_STATUS	R	0x0	ADC or PDM channel 2 power status. 0d = ADC or PDM channel is powered down 1d = ADC or PDM channel is powered up
5	IN_CH3_STATUS	R	0x0	ADC or PDM channel 1 power status. 0d = ADC or PDM channel is powered down 1d = ADC or PDM channel is powered up
4	IN_CH4_STATUS	R	0x0	ADC or PDM channel 2 power status. 0d = ADC or PDM channel is powered down 1d = ADC or PDM channel is powered up
3	OUT_CH1_STATUS	R	0x0	DAC channel 1 power status. 0d = DAC channel is powered down 1d = DAC channel is powered up
2	OUT_CH2_STATUS	R	0x0	DAC channel 2 power status. 0d = DAC channel is powered down 1d = DAC channel is powered up
1	OUT_CH3_STATUS	R	0x0	DAC channel 3 power status. 0d = DAC channel is powered down 1d = DAC channel is powered up
0	OUT_CH4_STATUS	R	0x0	DAC channel 4 power status. 0d = DAC channel is powered down 1d = DAC channel is powered up

7.1.101 DEV_STS1 Register (Address = 0x7A) [Reset = 0x80]

DEV_STS1 is shown in 図 7-101 and described in 表 7-102.

Return to the Summary Table.

This register is the device status value register 1.

図 7-101. DEV_STS1 Register

7	6	5	4	3	2	1	0
MODE_STS[2:0]			PLL_STS	MICBIAS_STS	BOOST_STS	CHx_PD_FLT_STS	ALL_CHx_PD_FLT_STS
R-100b			R-0b	R-0b	R-0b	R-0b	R-0b

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表 7-102. DEV_STS1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	MODE_STS[2:0]	R	0x4	Device mode status. 0-3d = Reserved 4d = Device is in sleep mode or software shutdown mode 5d = Reserved 6d = Device is in active mode with all record and playback channels turned off 7d = Device is in active mode with at least one record or playback channel turned on
4	PLL_STS	R	0x0	PLL status. 0d = PLL is not enabled 1d = PLL is enabled
3	MICBIAS_STS	R	0x0	MICBIAS status. 0d = MICBIAS is disabled 1d = MICBIAS is enabled
2	BOOST_STS	R	0x0	Boost status. 0d = Boost is disabled 1d = Boost is enabled
1	CHx_PD_FLT_STS	R	0x0	Status for PD on INxx Analog inputs faults 0d = No ADC Channel is Powered Down due to fault/s on Analog inputs INxx 1d = Some ADC Channel is Powered Down due to fault/s on Analog inputs INxx
0	ALL_CHx_PD_FLT_STS	R	0x0	Status for PD on Micbias faults 0d = No ADC Channel is Powered Down due to fault/s related to Micbias 1d = All ADC Channels are Powered Down due to fault/s related to Micbias

7.1.102 I2C_CKSUM Register (Address = 0x7E) [Reset = 0x00]

I2C_CKSUM is shown in 図 7-102 and described in 表 7-103.

Return to the Summary Table.

This register returns the I²C transactions checksum value.

図 7-102. I2C_CKSUM Register

7	6	5	4	3	2	1	0
I2C_CKSUM[7:0]							
R/W-00000000b							

表 7-103. I2C_CKSUM Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	I2C_CKSUM[7:0]	R/W	0x0	These bits return the I²C transactions checksum value. Writing to this register resets the checksum to the written value. This register is updated on writes to other registers on all pages.

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7.2 Page 1 Registers

表 7-104 lists the memory-mapped registers for the Page 1 registers. All register offset addresses not listed in 表 7-104 should be considered as reserved locations and the register contents should not be modified.

表 7-104. PAGE 1 Registers

Address	Acronym	Register Name	Reset Value	Section
0x0	PAGE_CFG	Device page register	0x00	セクション 7.2.1
0x3	DSP_CFG0		0x00	セクション 7.2.2
0xD	CLK_CFG0		0x00	セクション 7.2.3
0xE	CHANNEL_CFG1		0x00	セクション 7.2.4
0xF	CHANNEL_CFG2		0x00	セクション 7.2.5
0x17	SRC_CFG0	SRC configuration register 1	0x00	セクション 7.2.6
0x18	SRC_CFG1	SRC configuration register 2	0x00	セクション 7.2.7
0x19	JACK_DET_CFG0	JACK DET configuration register 0	0x00	セクション 7.2.8
0x1A	JACK_DET_CFG1	JACK DET configuration register 1	0x00	セクション 7.2.9
0x1B	JACK_DET_CFG2	JACK DET configuration register 2	0x00	セクション 7.2.10
0x1C	JACK_DET_CFG3	JACK DET configuration register 3	0x00	セクション 7.2.11
0x1E	LPAD_CFG1	LPAD	0x20	セクション 7.2.12
0x1F	LPSG_CFG1	LPSG	0x80	セクション 7.2.13
0x20	LPAD_LPSG_CFG1	LPAD and LPSG common configuration register 1	0x00	セクション 7.2.14
0x23	LIMITER_CFG	Limiter configuration register 2	0x00	セクション 7.2.15
0x24	AGC_DRC_CFG	AGC_DRC configuration register 2	0x00	セクション 7.2.16
0x2B	PLIM_CFG0	PLIM configuration register 0	0x00	セクション 7.2.17
0x2C	MIXER_CFG0	MISC configuration register 0	0x00	セクション 7.2.18
0x2D	MISC_CFG0	MISC configuration register 0	0x00	セクション 7.2.19
0x2E	BRWNOUT		0xBF	セクション 7.2.20
0x2F	INT_MASK0	Interrupt Mask Register-0	0xFF	セクション 7.2.21
0x30	INT_MASK1	Interrupt Mask Register-1	0x0F	セクション 7.2.22
0x31	INT_MASK2	Interrupt Mask Register-2	0x00	セクション 7.2.23
0x32	INT_MASK4	Interrupt Mask Register-3	0x00	セクション 7.2.24
0x33	INT_MASK5	Interrupt Mask Register-3	0x30	セクション 7.2.25
0x34	INT_LTCH0	Latched Interrupt Readback Register-0	0x00	セクション 7.2.26
0x35	CHx_LTCH	Summary of Diagnostics	0x00	セクション 7.2.27
0x36	IN_CH1_LTCH		0x00	セクション 7.2.28
0x37	IN_CH2_LTCH		0x00	セクション 7.2.29
0x38	OUT_CH1_LTCH		0x00	セクション 7.2.30
0x39	OUT_CH2_LTCH		0x00	セクション 7.2.31
0x3A	INT_LTCH1	Latched Interrupt Readback Register-0	0x00	セクション 7.2.32
0x3B	INT_LTCH2	Latched Interrupt Readback Register-3	0x00	セクション 7.2.33
0x3C	INT_LIVE0	Live Interrupt Readback Register-0	0x00	セクション 7.2.34
0x3D	CHx_LIVE	Summary of Diagnostics	0x00	セクション 7.2.35
0x3E	IN_CH1_LIVE		0x00	セクション 7.2.36
0x3F	IN_CH2_LIVE		0x00	セクション 7.2.37
0x40	OUT_CH1_LIVE		0x00	セクション 7.2.38
0x41	OUT_CH2_LIVE		0x00	セクション 7.2.39

表 7-104. PAGE 1 Registers (続き)

Address	Acronym	Register Name	Reset Value	Section
0x42	INT_LIVE1	Latched Interrupt Readback Register-0	0x00	セクション 7.2.40
0x43	INT_LIVE2	Latched Interrupt Readback Register-3	0x00	セクション 7.2.41
0x46	DIAG_CFG0		0x00	セクション 7.2.42
0x47	DIAG_CFG1		0x37	セクション 7.2.43
0x48	DIAG_CFG2		0x87	セクション 7.2.44
0x4A	DIAG_CFG4		0xB8	セクション 7.2.45
0x4B	DIAG_CFG5		0x00	セクション 7.2.46
0x4C	DIAG_CFG6		0xA2	セクション 7.2.47
0x4D	DIAG_CFG7		0x48	セクション 7.2.48
0x4E	DIAG_CFG8		0xBA	セクション 7.2.49
0x4F	DIAG_CFG9		0x4B	セクション 7.2.50
0x50	DIAG_CFG10		0x88	セクション 7.2.51
0x51	DIAG_CFG11		0x40	セクション 7.2.52
0x52	DIAG_CFG12		0x44	セクション 7.2.53
0x53	DIAG_CFG13		0x00	セクション 7.2.54
0x54	DIAG_CFG14		0x48	セクション 7.2.55
0x56	DIAG_MON_MSB_VBAT		0x00	セクション 7.2.56
0x57	DIAG_MON_LSB_VBAT		0x00	セクション 7.2.57
0x58	DIAG_MON_MSB_MBIAS		0x00	セクション 7.2.58
0x59	DIAG_MON_LSB_MBIAS		0x01	セクション 7.2.59
0x5A	DIAG_MON_MSB_IN1P		0x00	セクション 7.2.60
0x5B	DIAG_MON_LSB_IN1P		0x02	セクション 7.2.61
0x5C	DIAG_MON_MSB_IN1M		0x00	セクション 7.2.62
0x5D	DIAG_MON_LSB_IN1M		0x03	セクション 7.2.63
0x5E	DIAG_MON_MSB_IN2P		0x00	セクション 7.2.64
0x5F	DIAG_MON_LSB_IN2P		0x04	セクション 7.2.65
0x60	DIAG_MON_MSB_IN2M		0x00	セクション 7.2.66
0x61	DIAG_MON_LSB_IN2M		0x05	セクション 7.2.67
0x62	DIAG_MON_MSB_OUT1P		0x00	セクション 7.2.68
0x63	DIAG_MON_LSB_OUT1P		0x06	セクション 7.2.69
0x64	DIAG_MON_MSB_OUT1M		0x00	セクション 7.2.70
0x65	DIAG_MON_LSB_OUT1M		0x07	セクション 7.2.71
0x66	DIAG_MON_MSB_OUT2P		0x00	セクション 7.2.72
0x67	DIAG_MON_LSB_OUT2P		0x08	セクション 7.2.73
0x68	DIAG_MON_MSB_OUT2M		0x00	セクション 7.2.74
0x69	DIAG_MON_LSB_OUT2M		0x09	セクション 7.2.75
0x6A	DIAG_MON_MSB_TEMP		0x00	セクション 7.2.76
0x6B	DIAG_MON_LSB_TEMP		0x0A	セクション 7.2.77
0x6C	DIAG_MON_MSB_MBIAS_LOAD		0x00	セクション 7.2.78
0x6D	DIAG_MON_LSB_MBIAS_LOAD		0x0B	セクション 7.2.79
0x6E	DIAG_MON_MSB_AVDD		0x00	セクション 7.2.80

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表 7-104. PAGE 1 Registers (続き)

Address	Acronym	Register Name	Reset Value	Section
0x6F	DIAG_MON_LSB_AVDD		0x0C	セクション 7.2.81
0x70	DIAG_MON_MSB_GPA		0x00	セクション 7.2.82
0x71	DIAG_MON_LSB_GPA		0x0D	セクション 7.2.83
0x72	BOOST_CFG		0x00	セクション 7.2.84
0x73	MICBIAS_CFG		0xA0	セクション 7.2.85

7.2.1 PAGE_CFG Register (Address = 0x0) [Reset = 0x00]

PAGE_CFG is shown in 図 7-103 and described in 表 7-105.

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The device memory map is divided into pages. This register sets the page.

図 7-103. PAGE_CFG Register

7	6	5	4	3	2	1	0
PAGE[7:0]							
R/W-00000000b							

表 7-105. PAGE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	R/W	0x0	These bits set the device page. 0d = Page 0 1d = Page 1 2d to 254d = Page 2 to page 254 respectively 255d = Page 255

7.2.2 DSP_CFG0 Register (Address = 0x3) [Reset = 0x00]

DSP_CFG0 is shown in 図 7-104 and described in 表 7-106.

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図 7-104. DSP_CFG0 Register

7	6	5	4	3	2	1	0
RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	RESERVED	DIS_DVOL_OTF_CHG	EN_BQ_OTF_CHG
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R/W-0b	R/W-0b

表 7-106. DSP_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved bit; Write only reset value
6	RESERVED	R	0x0	Reserved bit; Write only reset value
5	RESERVED	R	0x0	Reserved bit; Write only reset value
4	RESERVED	R	0x0	Reserved bit; Write only reset value
3	RESERVED	R	0x0	Reserved bit; Write only reset value
2	RESERVED	R	0x0	Reserved bit; Write only reset value

表 7-106. DSP_CFG0 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
1	DIS_DVOL_OTF_CHG	R/W	0x0	Disable run-time changes to DVOL settings. 0d = Digital volume control changes supported while ADC is powered-on 1d = Digital volume control changes not supported while ADC is powered-on. This is useful for 384 kHz and higher sample rate if more than one channel processing is required.
0	EN_BQ_OTF_CHG	R/W	0x0	Enable run-time changes to Biquad settings. 0d = Disable on the fly biquad changes 1d = Enable on the fly biquad changes

7.2.3 CLK_CFG0 Register (Address = 0xD) [Reset = 0x00]

CLK_CFG0 is shown in 図 7-105 and described in 表 7-107.

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図 7-105. CLK_CFG0 Register

7	6	5	4	3	2	1	0
CNT_TGT_CFG_OVR_PASI	CNT_TGT_CFG_OVR_SASI	RESERVED	RESERVED		PASI_USE_INT_FSYNC	SASI_USE_INT_FSYNC	RESERVED
R/W-0b	R/W-0b	R-0b	R-00b		R/W-0b	R/W-0b	R-0b

表 7-107. CLK_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CNT_TGT_CFG_OVR_PASI	R/W	0x0	ASI controller target Config Override Register 0d = controller-target Config as per PASI_CNT_CFG bit. 1d = Override the standard behavior of the PASI_CNT_CFG. In this case the clock auto detect feature is not available. PASI_CNT_CFG = 0 : BCLK is input but FSYNC is output. PASI_CNT_CFG = 1 : BCLK is output but FSYNC in input.
6	CNT_TGT_CFG_OVR_SASI	R/W	0x0	ASI controller target Config Override Register 0d = controller-target Config as per SASI_CNT_CFG bit. 1d = Override the standard behavior of the SASI_CNT_CFG. In this case the clock auto detect feature is not available. SASI_CNT_CFG = 0 : BCLK is input but FSYNC is output. SASI_CNT_CFG = 1 : BCLK is output but FSYNC in input.
5	RESERVED	R	0x0	Reserved bit; Write only reset value
4-3	RESERVED	R	0x0	Reserved bits; Write only reset values
2	PASI_USE_INT_FSYNC	R/W	0x0	For Primary use internal FSYNC in controller mode configuration. 0d = Use external FSYNC 1d = Use internal FSYNC
1	SASI_USE_INT_FSYNC	R/W	0x0	For Secondary use internal FSYNC in controller mode configuration. 0d = Use external FSYNC 1d = Use internal FSYNC
0	RESERVED	R	0x0	Reserved bit; Write only reset value

7.2.4 CHANNEL_CFG1 Register (Address = 0xE) [Reset = 0x00]

CHANNEL_CFG1 is shown in 図 7-106 and described in 表 7-108.

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図 7-106. CHANNEL_CFG1 Register

7	6	5	4	3	2	1	0

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図 7-106. CHANNEL_CFG1 Register (続き)

FORCE_DYN_MODE_CUST_MAX_CH	DYN_MODE_CUST_MAX_CH[3:0]	RESERVED
R/W-0b	R/W-0000b	R-000b

表 7-108. CHANNEL_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	FORCE_DYN_MODE_CUST_MAX_CH	R/W	0x0	ADC Force dynamic mode custom max channel 0d = In Dynamic, Max channel is based on ADC_DYN_MAXCH_SEL 1d = In Dynamic mode, max channel is custom as DYN_MODE_CUST_MAX_CH
6-3	DYN_MODE_CUST_MAX_CH[3:0]	R/W	0x0	ADC Dynamic mode custom max channel configuration [3]->CH4_EN [2]->CH3_EN [1]->CH2_EN [0]->CH1_EN
2-0	RESERVED	R	0x0	Reserved bits; Write only reset values

7.2.5 CHANNEL_CFG2 Register (Address = 0xF) [Reset = 0x00]

CHANNEL_CFG2 is shown in 図 7-107 and described in 表 7-109.

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図 7-107. CHANNEL_CFG2 Register

7	6	5	4	3	2	1	0
DAC_FORCE_DYN_MODE_CUST_MAX_CH	DAC_DYN_MODE_CUST_MAX_CH[3:0]				RESERVED		
R/W-0b	R/W-0000b				R-000b		

表 7-109. CHANNEL_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DAC_FORCE_DYN_MODE_CUST_MAX_CH	R/W	0x0	DAC Force dynamic mode custom max channel 0d = In Dynamic, Max channel is based on DAC_DYN_MAXCH_SEL 1d = In Dynamic mode, max channel is custom as per DAC_DYN_MODE_CUST_MAX_CH
6-3	DAC_DYN_MODE_CUST_MAX_CH[3:0]	R/W	0x0	DAC Dynamic mode custom max channel configuration ([3]->CH4_EN, [2]->CH3_EN, [1]->CH2_EN, [0]->CH1_EN) [3]->CH4_EN [2]->CH3_EN [1]->CH2_EN [0]->CH1_EN
2-0	RESERVED	R	0x0	Reserved bits; Write only reset values

7.2.6 SRC_CFG0 Register (Address = 0x17) [Reset = 0x00]

SRC_CFG0 is shown in 図 7-108 and described in 表 7-110.

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This register is configuration register 1 for SRC.

図 7-108. SRC_CFG0 Register

7	6	5	4	3	2	1	0

図 7-108. SRC_CFG0 Register (続き)

7	6	5-0
SRC_EN	DIS_AUTO_SRC_DET	RESERVED
R/W-0b	R/W-0b	R-000000b

表 7-110. SRC_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SRC_EN	R/W	0x0	SRC enable config 0b = SRC disable 1b = SRC enable
6	DIS_AUTO_SRC_DET	R/W	0x0	SRC auto detect config 0b = SRC auto detect enabled 1b = SRC auto detect disabled
5-0	RESERVED	R	0x0	Reserved bits; Write only reset value

7.2.7 SRC_CFG1 Register (Address = 0x18) [Reset = 0x00]

SRC_CFG1 is shown in 図 7-109 and described in 表 7-111.

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This register is configuration register 2 for SRC.

図 7-109. SRC_CFG1 Register

7	6	5	4	3	2	1	0
MAIN_FS_CUSTOM_CFG	MAIN_FS_SELECT_CFG	MAIN_AUX_RATIO_M_CUSTOM_CFG[2:0]			MAIN_AUX_RATIO_N_CUSTOM_CFG[2:0]		
R/W-0b	R/W-0b	R/W-000b			R/W-000b		

表 7-111. SRC_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	MAIN_FS_CUSTOM_CFG	R/W	0x0	Main Fs custom config 0b = Main Fs is auto inferred 1b = Main Fs need to be selected from MAIN_FS_SELECT_CFG
6	MAIN_FS_SELECT_CFG	R/W	0x0	Main Fs select config 0b = PASI Fs shall be used as Main Fs 1b = SASI Fs shall be used as Main Fs
5-3	MAIN_AUX_RATIO_M_CUSTOM_CFG[2:0]	R/W	0x0	Main and Aux Fs Ratio m:n config 0d = m is auto inferred 1d = 1 2d = 2 3d = 3 4d = 4 5d = Reserved 6d = 6 7d = Reserved
2-0	MAIN_AUX_RATIO_N_CUSTOM_CFG[2:0]	R/W	0x0	Main and Aux Fs Ratio m:n config 0d = n is auto inferred 1d = 1 2d = 2 3d = 3 4d = 4 5d = Reserved 6d = 6 7d = Reserved

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7.2.8 JACK_DET_CFG0 Register (Address = 0x19) [Reset = 0x00]

JACK_DET_CFG0 is shown in 図 7-110 and described in 表 7-112.

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This register is the JACK DET configuration register 0.

図 7-110. JACK_DET_CFG0 Register

7	6	5	4	3	2	1	0
JACK_DET_MONITOR_FREQ[1:0]		JACK_DET_PULSE_WIDTH	RESERVED	RESERVED	HPDET_CLOCK_SEL[1:0]		RESERVED
R/W-00b		R/W-0b	R-0b	R-0b	R/W-00b		R-0b

表 7-112. JACK_DET_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	JACK_DET_MONITOR_FREQ[1:0]	R/W	0x0	Headset Detection Pulse Frequency 0d = 0.5 Hz 1d = 1 Hz 2d = 7.5 Hz 3d = 15 Hz
5	JACK_DET_PULSE_WIDTH	R/W	0x0	Detector Pulse High Width 0d = 4ms (MICBIAS PIN Cap = 1 uF) 1d = 32ms (MICBIAS PIN Cap = 10 uF)
4	RESERVED	R	0x0	Reserved bit; Write only reset value
3	RESERVED	R	0x0	Reserved bit; Write only reset value
2-1	HPDET_CLOCK_SEL[1:0]	R/W	0x0	Headphone Detection Clock Timeperiod Select 0d = 1ms 1d = 2ms 2d = 4ms 3d = Reserved
0	RESERVED	R	0x0	Reserved bit; Write only reset value

7.2.9 JACK_DET_CFG1 Register (Address = 0x1A) [Reset = 0x00]

JACK_DET_CFG1 is shown in 図 7-111 and described in 表 7-113.

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This register is the JACK DET configuration register 1.

図 7-111. JACK_DET_CFG1 Register

7	6	5	4	3	2	1	0
RESERVED	JACK_DET_COMP_CTRL2	JACK_DET_COMP_CTRL3[1:0]		HPDET_COUPLING	HPDET_USE_2x_CURR	JACK_DET_EN	RESERVED
R-0b	R/W-0b	R/W-00b		R/W-0b	R/W-0b	R/W-0b	R-0b

表 7-113. JACK_DET_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved bit; Write only reset value

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表 7-113. JACK_DET_CFG1 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
6	JACK_DET_COMP_CTRL2	R/W	0x0	Hook Press Threshold Control in Fixed External Resistance case, controls the choice of Lowest Microphone impedance to be supported or Highest Hook button Impedance to be supported 0d = Minimum Microphone resistance supported, R_Mic = 800 Ωs and Max Hook button impedance supported, R_Hook = 320 Ωs for AC coupled Headphones R26<3> = 0 (else, when R26<3> = 1, R_hook = 150 Ωs) 1d = Max Hook button impedance supported, R_hook = 680 Ωs and Minimum Microphone resistance supported, R_Mic = 1350 Ωs for AC coupled Headphones R26<3> = 0 (else, when R26<3> = 1, R_Mic = 1750 Ωs)
5-4	JACK_DET_COMP_CTRL3[1:0]	R/W	0x0	Hook Pressed Jack Insertion support, valid only for External Resistor Type P0_R25_D4 = 0 else Don't care. 0d = supports minimum Hook button impedance of 150 Ωs for Hook Pressed Jack Insertion detection 1d = supports minimum Hook button impedance of 100 Ωs for Hook Pressed Jack Insertion detection 2d = supports minimum Hook button impedance of 50 Ωs for Hook Pressed Jack Insertion detection 3d = Reserved
3	HPDET_COUPLING	R/W	0x0	Headphone detect coupling 0d = AC coupled 1d = DC coupled
2	HPDET_USE_2x_CURR	R/W	0x0	Headset detect current sel config 0d = 2x current for headphone detection disabled 1d = 2x current for headphone detection enabled
1	JACK_DET_EN	R/W	0x0	Headset Detection Enable 0d = Headset Detection Disabled 1d = Headset Detection Enabled
0	RESERVED	R	0x0	Reserved bit; Write only reset value

7.2.10 JACK_DET_CFG2 Register (Address = 0x1B) [Reset = 0x00]

JACK_DET_CFG2 is shown in 図 7-112 and described in 表 7-114.

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This register is the JACK DET configuration register 2.

図 7-112. JACK_DET_CFG2 Register

7	6	5	4	3	2	1	0
RESERVED	HPDET_DEB	JACK_DET_DEB_INSERT[2:0]			JACK_DET_DEB_REMOVAL	JACK_DET_DEB_HOOK_PRESS[1:0]	
R-0b	R/W-0b	R/W-000b			R/W-0b	R/W-00b	

表 7-114. JACK_DET_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved bit; Write only reset value
6	HPDET_DEB	R/W	0x0	Headphone Detection Debounce Programmability 0d = No Debounce 1d = Debounce of 3 detections

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表 7-114. JACK_DET_CFG2 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
5-3	JACK_DET_DEB_INSERT[2:0]	R/W	0x0	Headset Insert Detection Debounce Programmability 0d = Debounce Time = 16ms 1d = Debounce Time = 32ms 2d = Debounce Time = 64ms 3d = Debounce Time = 128ms 4d = Debounce Time = 256ms 5d = Debounce Time = 512ms 6d = Reserved. Don not use 7d = No Debounce
2	JACK_DET_DEB_REMOVAL	R/W	0x0	Headset Removal Detection Debounce Programmability 0d = Debounce of 5 detections 1d = Debounce of 3 detections
1-0	JACK_DET_DEB_HOOK_PRESS[1:0]	R/W	0x0	Hook Press Debounce config 0d = No Debounce 1d = No Debounce 2d = Debounce of 2 detections 3d = Debounce of 3 detections

7.2.11 JACK_DET_CFG3 Register (Address = 0x1C) [Reset = 0x00]

JACK_DET_CFG3 is shown in 図 7-113 and described in 表 7-115.

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This register is the JACK DET configuration register 3.

図 7-113. JACK_DET_CFG3 Register

7	6	5	4	3	2	1	0
JACK_TYPE_FLAG[1:0]		HEADSET_TYPE_DET[1:0]		RESERVED			
R-00b		R-00b		R-0000b			

表 7-115. JACK_DET_CFG3 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	JACK_TYPE_FLAG[1:0]	R	0x0	Headset Jack type flag 0d = Jack is not inserted 1d = Jack is inserted without Microphone 2d = Reserved. Do not use 3d = Jack is inserted with Microphone
5-4	HEADSET_TYPE_DET[1:0]	R	0x0	Headset type 0d = Headset is not inserted 1d = Jack is inserted with mono-HS (RIGHT) 2d = Jack is inserted with mono-HS (LEFT) 3d = Jack is inserted with stereo-HS
3-0	RESERVED	R	0x0	Reserved bits; Write only reset value

7.2.12 LPAD_CFG1 Register (Address = 0x1E) [Reset = 0x20]

LPAD_CFG1 is shown in 図 7-114 and described in 表 7-116.

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Low Power Activity Detection. Voice activity detection or Ultrasonic Activity detection configuration register 1

図 7-114. LPAD_CFG1 Register

7	6	5	4	3	2	1	0

図 7-114. LPAD_CFG1 Register (続き)

LPAD_MODE[1:0]		LPAD_CH_SEL[1:0]		LPAD_SDOUT_INT_CFG	RESERVED	LPAD_PD_DET_EN	RESERVED
R/W-00b		R/W-10b		R/W-0b	R-0b	R/W-0b	R-0b

表 7-116. LPAD_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	LPAD_MODE[1:0]	R/W	0x0	Auto ADC power up / power down configuration selection. 0d = User initiated ADC power-up and ADC power-down 1d = VAD/UAD interrupt based ADC power up and ADC power down 2d = VAD/UAD interrupt based ADC power up but user initiated ADC power down Dont use
5-4	LPAD_CH_SEL[1:0]	R/W	0x2	VAD channel select. 0d = Channel 1 is monitored for VAD/UAD activity 1d = Channel 2 is monitored for VAD/UAD activity 2d = Channel 3 is monitored for VAD/UAD activity 3d = Channel 4 is monitored for VAD/UAD activity
3	LPAD_SDOUT_INT_CFG	R/W	0x0	SDOUT interrupt configuration. 0d = SDOUT pin is not enabled for interrupt function 1d = SDOUT pin is enabled to support interrupt output when channel data in not being recorded
2	RESERVED	R	0x0	Reserved bit; Write only reset value
1	LPAD_PD_DET_EN	R/W	0x0	Enable ASI output data during VAD/UAD activity. 0d = VAD/UAD processing is not enabled during ADC recording 1d = VAD/UAD processing is enabled during ADC recording and VAD interrupts are generated as configured
0	RESERVED	R	0x0	Reserved bit; Write only reset value

7.2.13 LPSG_CFG1 Register (Address = 0x1F) [Reset = 0x80]

LPSG_CFG1 is shown in 図 7-115 and described in 表 7-117.

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Low Power Signal Generation configuration register 1

図 7-115. LPSG_CFG1 Register

7	6	5	4	3	2	1	0
LPSG_CH_SEL[1:0]		RESERVED	RESERVED				
R/W-10b		R-0b	R-00000b				

表 7-117. LPSG_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	LPSG_CH_SEL[1:0]	R/W	0x2	LPSG channel select.- UAG 0d = UAG activity is generated on channel 1 1d = UAG activity is generated on channel 2 2d = UAG activity is generated on channel 3 3d = UAG activity is generated on channel 4
5	RESERVED	R	0x0	Reserved bit; Write only reset value
4-0	RESERVED	R	0x0	Reserved bits; Write only reset values

7.2.14 LPAD_LPSG_CFG1 Register (Address = 0x20) [Reset = 0x00]

LPAD_LPSG_CFG1 is shown in 図 7-116 and described in 表 7-118.

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This register is configuration register 1 for VAD/UAD/UAG.

図 7-116. LPAD_LPSG_CFG1 Register

7	6	5	4	3	2	1	0
LPAD_LPSG_CLK_CFG[1:0]		LPAD_LPSG_EXT_CLK_CFG[1:0]		RESERVED	LPAD_PH1_EN	RESERVED	
R/W-00b		R/W-00b		R-0b	R/W-0b	R-00b	

表 7-118. LPAD_LPSG_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	LPAD_LPSG_CLK_CFG[1:0]	R/W	0x0	Clock select for VAD/UAD/UAG 0d = VAD/UAD/UAG processing using internal oscillator clock 1d = VAD/UAD/UAG processing using external clock on BCLK input 2d = VAD/UAD/UAG processing using external clock on CCLK input 3d = Custom clock configuration based on CNT_CFG, CLK_SRC and CLKGEN_CFG registers in page 0
5-4	LPAD_LPSG_EXT_CLK_CFG[1:0]	R/W	0x0	Clock configuration using external clock for VAD/UAD/UAG 0d = External clock is 24.576 MHz 1d = External clock is 6.144 MHz 2d = External clock is 12.288 MHz 3d = External clock is 18.432 MHz
3	RESERVED	R	0x0	Reserved bit; Write only reset value
2	LPAD_PH1_EN	R/W	0x0	Enable LPAD Phase 1 detection through Jack Detection comparator. 0d = LPAD phase 1 diabled 1d = LPAD phase 1 enabled
1-0	RESERVED	R	0x0	Reserved bits; Write only reset values

7.2.15 LIMITER_CFG Register (Address = 0x23) [Reset = 0x00]

LIMITER_CFG is shown in 図 7-117 and described in 表 7-119.

Return to the Summary Table.

This register is configuration register 2 for Limiter.

図 7-117. LIMITER_CFG Register

7	6	5	4	3	2	1	0
LIMITER_INP_SEL[1:0]		LIMITER_OUT_SEL[1:0]		RESERVED			
R/W-00b		R/W-00b		R-0000b			

表 7-119. LIMITER_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	LIMITER_INP_SEL[1:0]	R/W	0x0	Limiter input select config 0d = max(dacin_ch0, dacin_ch1) 1d = dacin_ch1 2d = dacin_ch0 3d = avg(dacin_ch0, dacin_ch1)
5-4	LIMITER_OUT_SEL[1:0]	R/W	0x0	Limiter output select config 0d = applied on both 1d = dacin_ch1 2d = dacin_ch0 3d = applied none
3-0	RESERVED	R	0x0	Reserved bits; Write only reset values

7.2.16 AGC_DRC_CFG Register (Address = 0x24) [Reset = 0x00]

AGC_DRC_CFG is shown in 図 7-118 and described in 表 7-120.

Return to the Summary Table.

This register is configuration register 2 for AGC_DRC.

図 7-118. AGC_DRC_CFG Register

7	6	5	4	3	2	1	0
AGC_CH1_EN	AGC_CH2_EN	AGC_CH3_EN	AGC_CH4_EN	DRC_CH1_EN	DRC_CH2_EN	DRC_CH3_EN	DRC_CH4_EN
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 7-120. AGC_DRC_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	AGC_CH1_EN	R/W	0x0	AGC Channel 1 enable config 0d = disable 1d = enable
6	AGC_CH2_EN	R/W	0x0	AGC Channel 2 enable config 0d = disable 1d = enable
5	AGC_CH3_EN	R/W	0x0	AGC Channel 3 enable config 0d = disable 1d = enable
4	AGC_CH4_EN	R/W	0x0	AGC Channel 4 enable config 0d = disable 1d = enable
3	DRC_CH1_EN	R/W	0x0	DRC Channel 1 enable config 0d = disable 1d = enable
2	DRC_CH2_EN	R/W	0x0	DRC Channel 2 enable config 0d = disable 1d = enable
1	DRC_CH3_EN	R/W	0x0	DRC Channel 3 enable config 0d = disable 1d = enable
0	DRC_CH4_EN	R/W	0x0	DRC Channel 4 enable config 0d = disable 1d = enable

7.2.17 PLIM_CFG0 Register (Address = 0x2B) [Reset = 0x00]

PLIM_CFG0 is shown in 図 7-119 and described in 表 7-121.

Return to the Summary Table.

This register is configuration register 0 for PLIM.

図 7-119. PLIM_CFG0 Register

7	6	5	4	3	2	1	0
EN_PLIM	PLIM_ATTN_VAL[2:0]			PLIM_BY_SAR_GPA	PLIM_RECOVERY	RESERVED	
R/W-0b	R/W-000b			R/W-0b	R/W-0b	R-00b	

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表 7-121. PLIM_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_PLIM	R/W	0x0	Enable PLIM 0d = Disable 1d = Enable
6-4	PLIM_ATTN_VAL[2:0]	R/W	0x0	PLIM attenuation factor 0d = 0dB 1d = -6dB 2d = -12dB 3d = -18dB 4d = -24dB 5d = -30dB 6d = -36dB 7d = -42dB
3	PLIM_BY_SAR_GPA	R/W	0x0	PLIM attenuation value source 0d = Plimit attentation based on GPIO and reg_plimi_attn_val 1d = Plimit attenuation based on GPA Analog voltage. LUT will map SAR ADC data to Attenuation factor
2	PLIM_RECOVERY	R/W	0x0	PLIM attenuation recovery 0d = Plimit func doesn't recover. It stays at same attenuation level or can apply more attenuation if required 1d = Plimit func recovers (reduces the attenuation) if "gpio_val=0" or "sar_adc_gpa" data suggest that Battery Voltage has recovered then we can reduce the attenuation being applied
1-0	RESERVED	R	0x0	Reserved bits; Write only reset value

7.2.18 MIXER_CFG0 Register (Address = 0x2C) [Reset = 0x00]

MIXER_CFG0 is shown in 図 7-120 and described in 表 7-122.

Return to the Summary Table.

This register is the MISC configuration register 0.

図 7-120. MIXER_CFG0 Register

7	6	5	4	3	2	1	0
EN_DAC_ASI_MIXER	EN_SIDE_CHAIN_MIXER	EN_ADC_CHANNEL_MIXER	EN_LOOPBACK_MIXER	RESERVED			
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R-0000b			

表 7-122. MIXER_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_DAC_ASI_MIXER	R/W	0x0	Enable DAC ASI Mixer 0b = Disabled 1b = Enabled
6	EN_SIDE_CHAIN_MIXER	R/W	0x0	Enable Side Chain Mixer 0b = Disabled 1b = Enabled
5	EN_ADC_CHANNEL_MIXER	R/W	0x0	Enable ADC Channel Mixer 0b = Disabled 1b = Enabled
4	EN_LOOPBACK_MIXER	R/W	0x0	Enable Loopback Mixer 0b = Disabled 1b = Enabled
3-0	RESERVED	R	0x0	Reserved bits; Write only reset value

7.2.19 MISC_CFG0 Register (Address = 0x2D) [Reset = 0x00]

MISC_CFG0 is shown in 図 7-121 and described in 表 7-123.

Return to the Summary Table.

This register is the MISC configuration register 0.

図 7-121. MISC_CFG0 Register

7	6	5	4	3	2	1	0
EN_DISTORTION	EN_BOP	EN_THERMAL_FOLDBACK	EN_DRC	DAC_SIGNAL_GENERATOR_1_ENABLE	DAC_SIGNAL_GENERATOR_2_ENABLE	DSP_VBAT_AVDD_SEL	BRWNOUT_EN
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 7-123. MISC_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	EN_DISTORTION	R/W	0x0	Distortion Limiter enable config 0b = Distortion Limiter disable 1b = Distortion Limiter enable
6	EN_BOP	R/W	0x0	BOP enable config 0b = BOP disable 1b = BOP enable
5	EN_THERMAL_FOLDBACK	R/W	0x0	Thermal Foldback enable config 0b = Thermal Foldback disable 1b = Thermal Foldback enable
4	EN_DRC	R/W	0x0	DRC enable config 0b = DRC disable 1b = DRC enable
3	DAC_SIGNAL_GENERATOR_1_ENABLE	R/W	0x0	DAC signal generator 1 enable config 0b = Signal generator disabled 1b = Signal generator enabled
2	DAC_SIGNAL_GENERATOR_2_ENABLE	R/W	0x0	DAC signal generator 2 enable config 0b = Signal generator disabled 1b = Signal generator enabled
1	DSP_VBAT_AVDD_SEL	R/W	0x0	SAR data source select for DSP Limiter, BOP, DRC 0b = SAR VBAT data to DSP 1b = SAR AVDD data to DSP
0	BRWNOUT_EN	R/W	0x0	Brownout enable config 0b = Brownout disable 1b = Brownout enable

7.2.20 BRWNOUT Register (Address = 0x2E) [Reset = 0xBF]

BRWNOUT is shown in 図 7-122 and described in 表 7-124.

Return to the Summary Table.

図 7-122. BRWNOUT Register

7	6	5	4	3	2	1	0
BRWNOUT_THRS[7:0]							
R/W-10111111b							

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表 7-124. BRWNOUT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	BRWNOUT_THRS[7:0]	R/W	0xBF	Threshold for brownout shutdown (IF P1_R45_D1->DSP_VBAT_AVDD_SEL=1) Default = 7.8V (~2.7V) Nd = ((0.9×(N*16)/4095)-0·211764)x17) (V) (((0.9×(N*16)/4095)-0·225)x6 (V))

7.2.21 INT_MASK0 Register (Address = 0x2F) [Reset = 0xFF]

INT_MASK0 is shown in 図 7-123 and described in 表 7-125.

Return to the Summary Table.

Interrupt masks.

図 7-123. INT_MASK0 Register

7	6	5	4	3	2	1	0
INT_MASK0	INT_MASK0	INT_MASK0	INT_MASK0	INT_MASK0	RESERVED	RESERVED	RESERVED
R/W-1b	R/W-1b	R/W-1b	R/W-1b	R/W-1b	R-0b	R-0b	R-0b

表 7-125. INT_MASK0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK0	R/W	0x1	Clock error interrupt mask. 0b = Don't Mask 1b = Mask
6	INT_MASK0	R/W	0x1	PLL Lock interrupt mask. 0b = Don't Mask 1b = Mask
5	INT_MASK0	R/W	0x1	Boost Over Temperature interrupt mask. 0b = Don't Mask 1b = Mask
4	INT_MASK0	R/W	0x1	Boost Over Current interrupt mask. 0b = Don't Mask 1b = Mask
3	INT_MASK0	R/W	0x1	Boost MO interrupt mask. 0b = Don't Mask 1b = Mask
2	RESERVED	R	0x0	Reserved bit; Write only reset value
1	RESERVED	R	0x0	Reserved bit; Write only reset value
0	RESERVED	R	0x0	Reserved bit; Write only reset value

7.2.22 INT_MASK1 Register (Address = 0x30) [Reset = 0x0F]

INT_MASK1 is shown in 図 7-124 and described in 表 7-126.

Return to the Summary Table.

Interrupt masks.

図 7-124. INT_MASK1 Register

7	6	5	4	3	2	1	0
INT_MASK1	INT_MASK1	INT_MASK1	INT_MASK1	INT_MASK1	RESERVED	RESERVED	RESERVED
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-1b	R-0b	R-0b	R-0b

表 7-126. INT_MASK1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK1	R/W	0x0	Channel-1 Input DC Faults Diagnostic Interrupt Mask. 0b = Don't Mask 1b = Mask
6	INT_MASK1	R/W	0x0	Channel-2 Input DC Faults Diagnostic Interrupt Mask. 0b = Don't Mask 1b = Mask
5	INT_MASK1	R/W	0x0	Channel-1 Output DC Faults Diagnostic Interrupt Mask. 0b = Don't Mask 1b = Mask
4	INT_MASK1	R/W	0x0	Channel-2 Output DC Faults Diagnostic Interrupt Mask. 0b = Don't Mask 1b = Mask
3	INT_MASK1	R/W	0x1	Input Faults Diagnostic Interrupt Mask for "Short to VBAT_IN" detect when VBAT_IN Voltage is less than MICBIAS Voltage. 0b = Don't Mask 1b = Mask
2	RESERVED	R	0x0	Reserved bit; Write only reset value
1	RESERVED	R	0x0	Reserved bit; Write only reset value
0	RESERVED	R	0x0	Reserved bit; Write only reset value

7.2.23 INT_MASK2 Register (Address = 0x31) [Reset = 0x00]

INT_MASK2 is shown in 図 7-125 and described in 表 7-127.

Return to the Summary Table.

Interrupt masks.

図 7-125. INT_MASK2 Register

7	6	5	4	3	2	1	0
INT_MASK2	INT_MASK2	INT_MASK2	INT_MASK2	INT_MASK2	INT_MASK2	INT_MASK2	INT_MASK2
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 7-127. INT_MASK2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK2	R/W	0x0	Input Diagnostics - Open Inputs Fault Interrupt Mask. 0b = Don't Mask 1b = Mask
6	INT_MASK2	R/W	0x0	Input Diagnostics - Inputs Shorted Fault Interrupt Mask. 0b = Don't Mask 1b = Mask
5	INT_MASK2	R/W	0x0	Input Diagnostics - INP Shorted to GND Fault Interrupt Mask. 0b = Don't Mask 1b = Mask
4	INT_MASK2	R/W	0x0	Input Diagnostics - INM Shorted to GND Fault Interrupt Mask. 0b = Don't Mask 1b = Mask
3	INT_MASK2	R/W	0x0	Input Diagnostics - INP Shorted to MICBIAS Fault Interrupt Mask. 0b = Don't Mask 1b = Mask
2	INT_MASK2	R/W	0x0	Input Diagnostics - INM Shorted to MICBIAS Fault Interrupt Mask. 0b = Don't Mask 1b = Mask

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表 7-127. INT_MASK2 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
1	INT_MASK2	R/W	0x0	Input Diagnostics - INP Shorted to VBAT_IN Fault Interrupt Mask. 0b = Don't Mask 1b = Mask
0	INT_MASK2	R/W	0x0	Input Diagnostics - INM Shorted to VBAT_IN Fault Interrupt Mask. 0b = Don't Mask 1b = Mask

7.2.24 INT_MASK4 Register (Address = 0x32) [Reset = 0x00]

INT_MASK4 is shown in 図 7-126 and described in 表 7-128.

Return to the Summary Table.

Interrupt masks.

図 7-126. INT_MASK4 Register

7	6	5	4	3	2	1	0
INT_MASK4	INT_MASK4	INT_MASK4	INT_MASK4	INT_MASK4	INT_MASK4	INT_MASK4	RESERVED
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R-0b

表 7-128. INT_MASK4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK4	R/W	0x0	INP overvoltage fault mask. 0b = Don't Mask 1b = Mask
6	INT_MASK4	R/W	0x0	INM overvoltage fault mask. 0b = Don't Mask 1b = Mask
5	INT_MASK4	R/W	0x0	OUT Short Circuit Fault Interrupt Mask. 0b = Don't Mask 1b = Mask
4	INT_MASK4	R/W	0x0	DRVR Virtual Ground Fault Interrupt Mask. 0b = Don't Mask 1b = Mask
3	INT_MASK4	R/W	0x0	Headset insert detection interrupt mask. 0b = Don't Mask 1b = Mask
2	INT_MASK4	R/W	0x0	Headset remove detection interrupt mask. 0b = Don't Mask 1b = Mask
1	INT_MASK4	R/W	0x0	Headset detection hook(button) interrupt mask. 0b = Don't Mask 1b = Mask
0	RESERVED	R	0x0	Reserved bit; Write only reset value

7.2.25 INT_MASK5 Register (Address = 0x33) [Reset = 0x30]

INT_MASK5 is shown in 図 7-127 and described in 表 7-129.

Return to the Summary Table.

Interrupt masks.

図 7-127. INT_MASK5 Register

7	6	5	4	3	2	1	0

図 7-127. INT_MASK5 Register (続き)

INT_MASK5	INT_MASK5	INT_MASK5	INT_MASK5	INT_MASK5	INT_MASK5	INT_MASK5	INT_MASK5
R/W-0b	R/W-0b	R/W-1b	R/W-1b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 7-129. INT_MASK5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_MASK5	R/W	0x0	GPA up threshold fault mask. 0b = Don't Mask 1b = Mask
6	INT_MASK5	R/W	0x0	GPA low threshold fault mask. 0b = Don't Mask 1b = Mask
5	INT_MASK5	R/W	0x1	VAD power up detect interrupt mask. 0b = Don't Mask 1b = Mask
4	INT_MASK5	R/W	0x1	VAD power down detect interrupt mask. 0b = Don't Mask 1b = Mask
3	INT_MASK5	R/W	0x0	Micbias short circuit fault mask. 0b = Don't Mask 1b = Mask
2	INT_MASK5	R/W	0x0	Micbias High current fault mask. 0b = Don't Mask 1b = Mask
1	INT_MASK5	R/W	0x0	Micbias Low current fault mask. 0b = Don't Mask 1b = Mask
0	INT_MASK5	R/W	0x0	Micbias Over voltage fault mask. 0b = Don't Mask 1b = Mask

7.2.26 INT_LTCH0 Register (Address = 0x34) [Reset = 0x00]

INT_LTCH0 is shown in 図 7-128 and described in 表 7-130.

Return to the Summary Table.

Latched interrupt readback.

図 7-128. INT_LTCH0 Register

7	6	5	4	3	2	1	0
INT_LTCH0	INT_LTCH0	INT_LTCH0	INT_LTCH0	INT_LTCH0	RESERVED	RESERVED	RESERVED
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 7-130. INT_LTCH0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH0	R	0x0	Interrupt due to clock error (self clearing bit). 0b = No interrupt 1b = Interrupt
6	INT_LTCH0	R	0x0	Interrupt due to PLL Lock (self clearing bit) 0b = No interrupt 1b = Interrupt
5	INT_LTCH0	R	0x0	Interrupt due to Boost Over Temperature (self clearing bit). 0b = No interrupt 1b = Interrupt

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表 7-130. INT_LTCH0 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
4	INT_LTCH0	R	0x0	Interrupt due to Boost Over Current.(self clearing bit). 0b = No interrupt 1b = Interrupt
3	INT_LTCH0	R	0x0	Interrupt due to Boost MO. (self clearing bit). 0b = No interrupt 1b = Interrupt
2	RESERVED	R	0x0	Reserved bit; Write only reset value
1	RESERVED	R	0x0	Reserved bit; Write only reset value
0	RESERVED	R	0x0	Reserved bit; Write only reset value

7.2.27 CHx_LTCH Register (Address = 0x35) [Reset = 0x00]

CHx_LTCH is shown in 図 7-129 and described in 表 7-131.

Return to the Summary Table.

Channel level Diagnostics Latched Status

図 7-129. CHx_LTCH Register

7	6	5	4	3	2	1	0
STS_CHx_LTCH	STS_CHx_LTCH	STS_CHx_LTCH	STS_CHx_LTCH	STS_CHx_LTCH	RESERVED	RESERVED	RESERVED
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 7-131. CHx_LTCH Register Field Descriptions

Bit	Field	Type	Reset	Description
7	STS_CHx_LTCH	R	0x0	Status of Input CH1_LTCH. 0b = No faults occurred in input channel 1 1b = Fault or Faults have occurred in input channel 1
6	STS_CHx_LTCH	R	0x0	Status of Input CH2_LTCH. 0b = No faults occurred in input channel 2 1b = Fault or Faults have occurred in input channel 2
5	STS_CHx_LTCH	R	0x0	Status of Output CH1_LTCH. 0b = No faults occurred in output channel 1 1b = Fault or Faults have occurred in output channel 1
4	STS_CHx_LTCH	R	0x0	Status of Output CH2_LTCH. 0b = No faults occurred in output channel 2 1b = Fault or Faults have occurred in output channel 2
3	STS_CHx_LTCH	R	0x0	Status on fault due "Short to VBAT_IN fault detected when VBAT_IN is less than MICBIAS" 0b = Short to VBAT_IN fault when VBAT_IN is less than MICBIAS did NOT occur in any channel 1b = Short to VBAT_IN fault when VBAT_IN is less than MICBIAS has occurred in atleast one channel
2	RESERVED	R	0x0	Reserved bit; Write only reset value
1	RESERVED	R	0x0	Reserved bit; Write only reset value
0	RESERVED	R	0x0	Reserved bit; Write only reset value

7.2.28 IN_CH1_LTCH Register (Address = 0x36) [Reset = 0x00]

IN_CH1_LTCH is shown in 図 7-130 and described in 表 7-132.

Return to the Summary Table.

図 7-130. IN_CH1_LTCH Register

7	6	5	4	3	2	1	0
IN_CH1_LTCH	IN_CH1_LTCH	IN_CH1_LTCH	IN_CH1_LTCH	IN_CH1_LTCH	IN_CH1_LTCH	IN_CH1_LTCH	IN_CH1_LTCH
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 7-132. IN_CH1_LTCH Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IN_CH1_LTCH	R	0x0	Input Channel-1 Open Inputs (self clearing bit). 0b = No Open Inputs 1b = Open Inputs
6	IN_CH1_LTCH	R	0x0	Input Channel-1 Inputs Shorted (self clearing bit). 0b = No Input Shorted 1b = Input Shorted each Other
5	IN_CH1_LTCH	R	0x0	Input Channel-1 INP Shorted to GND (self clearing bit). 0b = INP not shorted to GND 1b = INP shorted to GND
4	IN_CH1_LTCH	R	0x0	Input Channel-1 INM Shorted to GND (self clearing bit). 0b = INM not shorted to GND 1b = INM shorted to GND
3	IN_CH1_LTCH	R	0x0	Input Channel-1 INP Shorted to MICBIAS (self clearing bit). 0b = INP not shorted to MICBIAS 1b = INP shorted to MICBIAS
2	IN_CH1_LTCH	R	0x0	Input Channel-1 INM Shorted to MICBIAS (self clearing bit). 0b = INM not shorted to MICBIAS 1b = INM shorted to MICBIAS
1	IN_CH1_LTCH	R	0x0	Input Channel-1 INP Shorted to VBAT_IN (self clearing bit). 0b = INP not shorted to VBAT_IN 1b = INP shorted to VBAT_IN
0	IN_CH1_LTCH	R	0x0	Input Channel-1 INM Shorted to VBAT_IN (self clearing bit). 0b = INM not shorted to VBAT_IN 1b = INM shorted to VBAT_IN

7.2.29 IN_CH2_LTCH Register (Address = 0x37) [Reset = 0x00]

IN_CH2_LTCH is shown in 図 7-131 and described in 表 7-133.

Return to the Summary Table.

図 7-131. IN_CH2_LTCH Register

7	6	5	4	3	2	1	0
IN_CH2_LTCH	IN_CH2_LTCH	IN_CH2_LTCH	IN_CH2_LTCH	IN_CH2_LTCH	IN_CH2_LTCH	IN_CH2_LTCH	IN_CH2_LTCH
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 7-133. IN_CH2_LTCH Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IN_CH2_LTCH	R	0x0	Input Channel-2 Open Inputs (self clearing bit). 0b = No Open Inputs 1b = Open Inputs
6	IN_CH2_LTCH	R	0x0	Input Channel-2 Inputs Shorted (self clearing bit). 0b = No Input Shorted 1b = Input Shorted each Other
5	IN_CH2_LTCH	R	0x0	Input Channel-2 INP Shorted to GND (self clearing bit). 0b = INP not shorted to GND 1b = INP shorted to GND

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表 7-133. IN_CH2_LTCH Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
4	IN_CH2_LTCH	R	0x0	Input Channel-2 INM Shorted to GND (self clearing bit). 0b = INM not shorted to GND 1b = INM shorted to GND
3	IN_CH2_LTCH	R	0x0	Input Channel-2 INP Shorted to MICBIAS (self clearing bit). 0b = INP not shorted to MICBIAS 1b = INP shorted to MICBIAS
2	IN_CH2_LTCH	R	0x0	Input Channel-2 INM Shorted to MICBIAS (self clearing bit). 0b = INM not shorted to MICBIAS 1b = INM shorted to MICBIAS
1	IN_CH2_LTCH	R	0x0	Input Channel-2 INP Shorted to VBAT_IN (self clearing bit). 0b = INP not shorted to VBAT_IN 1b = INP shorted to VBAT_IN
0	IN_CH2_LTCH	R	0x0	Input Channel-2 INM Shorted to VBAT_IN (self clearing bit). 0b = INM not shorted to VBAT_IN 1b = INM shorted to VBAT_IN

7.2.30 OUT_CH1_LTCH Register (Address = 0x38) [Reset = 0x00]

OUT_CH1_LTCH is shown in 図 7-132 and described in 表 7-134.

Return to the Summary Table.

図 7-132. OUT_CH1_LTCH Register

7	6	5	4	3	2	1	0
OUT_CH1_LTCH	OUT_CH1_LTCH	OUT_CH1_LTCH	OUT_CH1_LTCH	MASK_ADC_CH1_OVRLD_FLAG	MASK_ADC_CH2_OVRLD_FLAG	RESERVED	
R-0b	R-0b	R-0b	R-0b	R/W-0b	R/W-0b	R-00b	

表 7-134. OUT_CH1_LTCH Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_CH1_LTCH	R	0x0	OUT1P Short Circuit Fault (self clearing bit). 0b = No short ciruit fault 1b = Short circuit fault
6	OUT_CH1_LTCH	R	0x0	OUT1M Short Circuit Fault (self clearing bit). 0b = No short ciruit fault 1b = Short circuit fault
5	OUT_CH1_LTCH	R	0x0	Channel 1 DRVRP Virtual Ground Fault (self clearing bit). 0b = No virtual ground fault 1b = Virtual ground fault
4	OUT_CH1_LTCH	R	0x0	Channel 1 DRVRM Virtual Ground Fault (self clearing bit). 0b = No virtual ground fault 1b = Virtual ground fault
3	MASK_ADC_CH1_OVRLD_FLAG	R/W	0x0	ADC CH1 OVRLD fault mask. 0b = Don't Mask 1b = Mask
2	MASK_ADC_CH2_OVRLD_FLAG	R/W	0x0	ADC CH2 OVRLD fault mask. 0b = Don't Mask 1b = Mask
1-0	RESERVED	R	0x0	Reserved bits; Write only reset value

7.2.31 OUT_CH2_LTCH Register (Address = 0x39) [Reset = 0x00]

OUT_CH2_LTCH is shown in 図 7-133 and described in 表 7-135.

Return to the Summary Table.

図 7-133. OUT_CH2_LTCH Register

7	6	5	4	3	2	1	0
OUT_CH2_LTCH	OUT_CH2_LTCH	OUT_CH2_LTCH	OUT_CH2_LTCH	RESERVED		MASK_AREG_SC_FLAG	AREG_SC_FLAG_LTCH
R-0b	R-0b	R-0b	R-0b	R-00b		R/W-0b	R-0b

表 7-135. OUT_CH2_LTCH Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_CH2_LTCH	R	0x0	OUT2P Short Circuit Fault (self clearing bit). 0b = No short ciruit fault 1b = Short circuit fault
6	OUT_CH2_LTCH	R	0x0	OUT2M Short Circuit Fault (self clearing bit). 0b = No short ciruit fault 1b = Short circuit fault
5	OUT_CH2_LTCH	R	0x0	Channel 2 DRVRP Virtual Ground Fault (self clearing bit). 0b = No virtual ground fault 1b = Virtual ground fault
4	OUT_CH2_LTCH	R	0x0	Channel 2 DRVRM Virtual Ground Fault (self clearing bit). 0b = No virtual ground fault 1b = Virtual ground fault
3-2	RESERVED	R	0x0	Reserved bits; Write only reset value
1	MASK_AREG_SC_FLAG	R/W	0x0	AREG SC fault mask. 0b = Don't Mask 1b = Mask
0	AREG_SC_FLAG_LTCH	R	0x0	AREG SC fault (self clearing bit). 0b = No AREG short circuit fault 1b = AREG short ciruit fault

7.2.32 INT_LTCH1 Register (Address = 0x3A) [Reset = 0x00]

INT_LTCH1 is shown in 図 7-134 and described in 表 7-136.

Return to the Summary Table.

Latched interrupt readback.

図 7-134. INT_LTCH1 Register

7	6	5	4	3	2	1	0
INT_LTCH1	INT_LTCH1	INT_LTCH1	INT_LTCH1	INT_LTCH1	INT_LTCH1	INT_LTCH1	INT_LTCH1
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 7-136. INT_LTCH1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH1	R	0x0	Channel-1 INP Over Voltage (self clearing bit). 0b = No INP Over Voltage fault 1b = INP Over Voltage fault has occured
6	INT_LTCH1	R	0x0	Channel-1 INM Over Voltage (self clearing bit). 0b = No INM Over Voltage fault 1b = INM Over Voltage fault has occured

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表 7-136. INT_LTCH1 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
5	INT_LTCH1	R	0x0	Channel-2 INP Over Voltage (self clearing bit). 0b = No INP Over Voltage fault 1b = INP Over Voltage fault has occured
4	INT_LTCH1	R	0x0	Channel-2 INM Over Voltage (self clearing bit). 0b = No INM Over Voltage fault 1b = INM Over Voltage fault has occured
3	INT_LTCH1	R	0x0	Interrupt due to Headset Insert Detection (self clearing bit). 0b = No interrupt 1b = Interrupt
2	INT_LTCH1	R	0x0	Interrupt due to Headset Remove Detection (self clearing bit). 0b = No interrupt 1b = Interrupt
1	INT_LTCH1	R	0x0	Interrupt due to Headset hook(button) (self clearing bit). 0b = No interrupt 1b = Interrupt
0	INT_LTCH1	R	0x0	Interrupt due to MIPS overload (self clearing bit) 0b = No interrupt 1b = Interrupt

7.2.33 INT_LTCH2 Register (Address = 0x3B) [Reset = 0x00]

INT_LTCH2 is shown in 図 7-135 and described in 表 7-137.

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Latched interrupt readback.

図 7-135. INT_LTCH2 Register

7	6	5	4	3	2	1	0
INT_LTCH2	INT_LTCH2	INT_LTCH2	INT_LTCH2	INT_LTCH2	INT_LTCH2	INT_LTCH2	INT_LTCH2
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 7-137. INT_LTCH2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LTCH2	R	0x0	Interrupt due to GPA up threshold fault (self clearing bit). 0b = No interrupt 1b = Interrupt
6	INT_LTCH2	R	0x0	Interrupt due to GPA low threshold fault (self clearing bit) 0b = No interrupt 1b = Interrupt
5	INT_LTCH2	R	0x0	Interrupt due to VAD power up detect (self clearing bit). 0b = No interrupt 1b = Interrupt
4	INT_LTCH2	R	0x0	Interrupt due to VAD power down detect (self clearing bit). 0b = No interrupt 1b = Interrupt
3	INT_LTCH2	R	0x0	Interrupt due to Micbias short circuit condition (self clearing bit) 0b = No interrupt 1b = Interrupt
2	INT_LTCH2	R	0x0	Interrupt due to Micbias High current fault (self clearing bit). 0b = No interrupt 1b = Interrupt
1	INT_LTCH2	R	0x0	Interrupt due to Micbias Low current fault (self clearing bit) 0b = No interrupt 1b = Interrupt

表 7-137. INT_LTCH2 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
0	INT_LTCH2	R	0x0	Interrupt due to Micbias Over voltage fault (self clearing bit). 0b = No interrupt 1b = Interrupt

7.2.34 INT_LIVE0 Register (Address = 0x3C) [Reset = 0x00]

INT_LIVE0 is shown in 図 7-136 and described in 表 7-138.

Return to the Summary Table.

Latched interrupt readback.

図 7-136. INT_LIVE0 Register

7	6	5	4	3	2	1	0
INT_LIVE0	INT_LIVE0	INT_LIVE0	INT_LIVE0	INT_LIVE0	RESERVED	RESERVED	RESERVED
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 7-138. INT_LIVE0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LIVE0	R	0x0	Interrupt due to clock error . 0b = No interrupt 1b = Interrupt
6	INT_LIVE0	R	0x0	Interrupt due to PLL Lock 0b = No interrupt 1b = Interrupt
5	INT_LIVE0	R	0x0	Interrupt due to Boost Over Temperature . 0b = No interrupt 1b = Interrupt
4	INT_LIVE0	R	0x0	Interrupt due to Boost Over Current.. 0b = No interrupt 1b = Interrupt
3	INT_LIVE0	R	0x0	Interrupt due to Boost MO. . 0b = No interrupt 1b = Interrupt
2	RESERVED	R	0x0	Reserved bit; Write only reset value
1	RESERVED	R	0x0	Reserved bit; Write only reset value
0	RESERVED	R	0x0	Reserved bit; Write only reset value

7.2.35 CHx_LIVE Register (Address = 0x3D) [Reset = 0x00]

CHx_LIVE is shown in 図 7-137 and described in 表 7-139.

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Channel level Diagnostics Live Status

図 7-137. CHx_LIVE Register

7	6	5	4	3	2	1	0
STS_CHx_LIVE	STS_CHx_LIVE	STS_CHx_LIVE	STS_CHx_LIVE	STS_CHx_LIVE	RESERVED	RESERVED	RESERVED
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

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表 7-139. CHx_LIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	STS_CHx_LIVE	R	0x0	Status of Input CH1_LIVE. 0b = No faults occurred in input channel 1 1b = Fault or Faults have occurred in input channel 1
6	STS_CHx_LIVE	R	0x0	Status of Input CH2_LIVE. 0b = No faults occurred in input channel 2 1b = Fault or Faults have occurred in input channel 2
5	STS_CHx_LIVE	R	0x0	Status of Output CH1_LIVE. 0b = No faults occurred in output channel 1 1b = Fault or Faults have occurred in output channel 1
4	STS_CHx_LIVE	R	0x0	Status of Output CH2_LIVE. 0b = No faults occurred in output channel 2 1b = Fault or Faults have occurred in output channel 2
3	STS_CHx_LIVE	R	0x0	Status on fault due "Short to VBAT_IN fault detected when VBAT_IN is less than MICBIAS" 0b = Short to VBAT_IN fault when VBAT_IN is less than MICBIAS did NOT occur in any channel 1b = Short to VBAT_IN fault when VBAT_IN is less than MICBIAS has occurred in atleast one channel
2	RESERVED	R	0x0	Reserved bit; Write only reset value
1	RESERVED	R	0x0	Reserved bit; Write only reset value
0	RESERVED	R	0x0	Reserved bit; Write only reset value

7.2.36 IN_CH1_LIVE Register (Address = 0x3E) [Reset = 0x00]

IN_CH1_LIVE is shown in 図 7-138 and described in 表 7-140.

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図 7-138. IN_CH1_LIVE Register

7	6	5	4	3	2	1	0
IN_CH1_LIVE	IN_CH1_LIVE	IN_CH1_LIVE	IN_CH1_LIVE	IN_CH1_LIVE	IN_CH1_LIVE	IN_CH1_LIVE	IN_CH1_LIVE
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 7-140. IN_CH1_LIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IN_CH1_LIVE	R	0x0	Input Channel-1 Open Inputs . 0b = No Open Inputs 1b = Open Inputs
6	IN_CH1_LIVE	R	0x0	Input Channel-1 Inputs Shorted . 0b = No Input Shorted 1b = Input Shorted each Other
5	IN_CH1_LIVE	R	0x0	Input Channel-1 INP Shorted to GND . 0b = INP not shorted to GND 1b = INP shorted to GND
4	IN_CH1_LIVE	R	0x0	Input Channel-1 INM Shorted to GND . 0b = INM not shorted to GND 1b = INM shorted to GND
3	IN_CH1_LIVE	R	0x0	Input Channel-1 INP Shorted to MICBIAS . 0b = INP not shorted to MICBIAS 1b = INP shorted to MICBIAS
2	IN_CH1_LIVE	R	0x0	Input Channel-1 INM Shorted to MICBIAS . 0b = INM not shorted to MICBIAS 1b = INM shorted to MICBIAS

表 7-140. IN_CH1_LIVE Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
1	IN_CH1_LIVE	R	0x0	Input Channel-1 INP Shorted to VBAT_IN . 0b = INP not shorted to VBAT_IN 1b = INP shorted to VBAT_IN
0	IN_CH1_LIVE	R	0x0	Input Channel-1 INM Shorted to VBAT_IN . 0b = INM not shorted to VBAT_IN 1b = INM shorted to VBAT_IN

7.2.37 IN_CH2_LIVE Register (Address = 0x3F) [Reset = 0x00]

IN_CH2_LIVE is shown in 図 7-139 and described in 表 7-141.

Return to the Summary Table.

図 7-139. IN_CH2_LIVE Register

7	6	5	4	3	2	1	0
IN_CH2_LIVE	IN_CH2_LIVE	IN_CH2_LIVE	IN_CH2_LIVE	IN_CH2_LIVE	IN_CH2_LIVE	IN_CH2_LIVE	IN_CH2_LIVE
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 7-141. IN_CH2_LIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IN_CH2_LIVE	R	0x0	Input Channel-2 Open Inputs . 0b = No Open Inputs 1b = Open Inputs
6	IN_CH2_LIVE	R	0x0	Input Channel-2 Inputs Shorted . 0b = No Input Shorted 1b = Input Shorted each Other
5	IN_CH2_LIVE	R	0x0	Input Channel-2 INP Shorted to GND . 0b = INP not shorted to GND 1b = INP shorted to GND
4	IN_CH2_LIVE	R	0x0	Input Channel-2 INM Shorted to GND . 0b = INM not shorted to GND 1b = INM shorted to GND
3	IN_CH2_LIVE	R	0x0	Input Channel-2 INP Shorted to MICBIAS . 0b = INP not shorted to MICBIAS 1b = INP shorted to MICBIAS
2	IN_CH2_LIVE	R	0x0	Input Channel-2 INM Shorted to MICBIAS . 0b = INM not shorted to MICBIAS 1b = INM shorted to MICBIAS
1	IN_CH2_LIVE	R	0x0	Input Channel-2 INP Shorted to VBAT_IN . 0b = INP not shorted to VBAT_IN 1b = INP shorted to VBAT_IN
0	IN_CH2_LIVE	R	0x0	Input Channel-2 INM Shorted to VBAT_IN . 0b = INM not shorted to VBAT_IN 1b = INM shorted to VBAT_IN

7.2.38 OUT_CH1_LIVE Register (Address = 0x40) [Reset = 0x00]

OUT_CH1_LIVE is shown in 図 7-140 and described in 表 7-142.

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図 7-140. OUT_CH1_LIVE Register

7	6	5	4	3	2	1	0

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図 7-140. OUT_CH1_LIVE Register (続き)

OUT_CH1_LIVE	OUT_CH1_LIVE	OUT_CH1_LIVE	OUT_CH1_LIVE	RESERVED
R-0b	R-0b	R-0b	R-0b	R-0000b

表 7-142. OUT_CH1_LIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_CH1_LIVE	R	0x0	OUT1P Short Circuit Fault . 0b = No short ciruit fault 1b = Short circuit fault
6	OUT_CH1_LIVE	R	0x0	OUT1M Short Circuit Fault . 0b = No short ciruit fault 1b = Short circuit fault
5	OUT_CH1_LIVE	R	0x0	Channel 1 DRVRP Virtual Ground Fault . 0b = No virtual ground fault 1b = Virtual ground fault
4	OUT_CH1_LIVE	R	0x0	Channel 1 DRVRM Virtual Ground Fault . 0b = No virtual ground fault 1b = Virtual ground fault
3-0	RESERVED	R	0x0	Reserved bits; Write only reset value

7.2.39 OUT_CH2_LIVE Register (Address = 0x41) [Reset = 0x00]

OUT_CH2_LIVE is shown in 図 7-141 and described in 表 7-143.

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図 7-141. OUT_CH2_LIVE Register

7	6	5	4	3	2	1	0
OUT_CH2_LIVE	OUT_CH2_LIVE	OUT_CH2_LIVE	OUT_CH2_LIVE	RESERVED			AREG_SC_FLAG_LIVE
R-0b	R-0b	R-0b	R-0b	R-000b			R-0b

表 7-143. OUT_CH2_LIVE Register Field Descriptions

Bit	Field	Type	Reset	Description
7	OUT_CH2_LIVE	R	0x0	OUT2P Short Circuit Fault . 0b = No short ciruit fault 1b = Short circuit fault
6	OUT_CH2_LIVE	R	0x0	OUT2M Short Circuit Fault . 0b = No short ciruit fault 1b = Short circuit fault
5	OUT_CH2_LIVE	R	0x0	Channel 2 DRVRP Virtual Ground Fault . 0b = No virtual ground fault 1b = Virtual ground fault
4	OUT_CH2_LIVE	R	0x0	Channel 2 DRVRM Virtual Ground Fault . 0b = No virtual ground fault 1b = Virtual ground fault
3-1	RESERVED	R	0x0	Reserved bits; Write only reset value
0	AREG_SC_FLAG_LIVE	R	0x0	AREG SC fault . 0b = No AREG short circuit fault 1b = AREG short ciruit fault

7.2.40 INT_LIVE1 Register (Address = 0x42) [Reset = 0x00]

INT_LIVE1 is shown in 図 7-142 and described in 表 7-144.

Return to the Summary Table.

Live interrupt readback.

図 7-142. INT_LIVE1 Register

7	6	5	4	3	2	1	0
INT_LIVE1	INT_LIVE1	INT_LIVE1	INT_LIVE1	INT_LIVE1	INT_LIVE1	INT_LIVE1	RESERVED
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 7-144. INT_LIVE1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LIVE1	R	0x0	Channel-1 INP Over Voltage . 0b = No INP Over Voltage fault 1b = INP Over Voltage fault has occured
6	INT_LIVE1	R	0x0	Channel-1 INM Over Voltage . 0b = No INM Over Voltage fault 1b = INM Over Voltage fault has occured
5	INT_LIVE1	R	0x0	Channel-2 INP Over Voltage . 0b = No INP Over Voltage fault 1b = INP Over Voltage fault has occured
4	INT_LIVE1	R	0x0	Channel-2 INM Over Voltage . 0b = No INM Over Voltage fault 1b = INM Over Voltage fault has occured
3	INT_LIVE1	R	0x0	Interrupt due to Headset Insert Detection . 0b = No interrupt 1b = Interrupt
2	INT_LIVE1	R	0x0	Interrupt due to Headset Remove Detection . 0b = No interrupt 1b = Interrupt
2	INT_LIVE1	R	0x0	Interrupt due to Headset hook(button) . 0b = No interrupt 1b = Interrupt
1	INT_LIVE1	R	0x0	Interrupt due to MIPS overload 0b = No interrupt 1b = Interrupt
0	RESERVED	R	0x0	

7.2.41 INT_LIVE2 Register (Address = 0x43) [Reset = 0x00]

INT_LIVE2 is shown in 図 7-143 and described in 表 7-145.

Return to the Summary Table.

Live interrupt readback.

図 7-143. INT_LIVE2 Register

7	6	5	4	3	2	1	0
INT_LIVE2	INT_LIVE2	INT_LIVE2	INT_LIVE2	INT_LIVE2	INT_LIVE2	INT_LIVE2	INT_LIVE2
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

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表 7-145. INT_LIVE2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	INT_LIVE2	R	0x0	Interrupt due to GPA up threshold fault . 0b = No interrupt 1b = Interrupt
6	INT_LIVE2	R	0x0	Interrupt due to GPA low threshold fault 0b = No interrupt 1b = Interrupt
5	INT_LIVE2	R	0x0	Interrupt due to VAD power up detect . 0b = No interrupt 1b = Interrupt
4	INT_LIVE2	R	0x0	Interrupt due to VAD power down detect . 0b = No interrupt 1b = Interrupt
3	INT_LIVE2	R	0x0	Interrupt due to Micbias short circuit condition 0b = No interrupt 1b = Interrupt
2	INT_LIVE2	R	0x0	Interrupt due to Micbias High current fault . 0b = No interrupt 1b = Interrupt
1	INT_LIVE2	R	0x0	Interrupt due to Micbias Low current fault 0b = No interrupt 1b = Interrupt
0	INT_LIVE2	R	0x0	Interrupt due to Micbias Over voltage fault . 0b = No interrupt 1b = Interrupt

7.2.42 DIAG_CFG0 Register (Address = 0x46) [Reset = 0x00]

DIAG_CFG0 is shown in 図 7-144 and described in 表 7-146.

Return to the Summary Table.

図 7-144. DIAG_CFG0 Register

7	6	5	4	3	2	1	0
IN_CH1_DIAG_EN	IN_CH2_DIAG_EN	INCL_SE_INM	INCL_AC_COUP	OUT1P_DIAG_EN	OUT1M_DIAG_EN	OUT2P_DIAG_EN	OUT2M_DIAG_EN
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 7-146. DIAG_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	IN_CH1_DIAG_EN	R/W	0x0	Channel-1 Input (IN1P and IN1M) Scan for Diagnostics 0b = Diagnostic Disabled 1b = Diagnostic Enabled
6	IN_CH2_DIAG_EN	R/W	0x0	Channel-2 Input (IN2P and IN2M) Scan for Diagnostics 0b = Diagnostic Disabled 1b = Diagnostic Enabled
5	INCL_SE_INM	R/W	0x0	INxM pin Diagnostics Scan Selection for Single Ended Configuration 0b = INxM pins of single ended channels are excluded for diagnosis 1b = INxM pins of single ended channels are included for diagnosis
4	INCL_AC_COUP	R/W	0x0	AC coupled channels pins Scan Selection for Diagnostics 0b = INxP and INxM pins of AC coupled channels are excluded for diagnosis 1b = INxP and INxM pins of AC coupled channels are included for diagnosis

表 7-146. DIAG_CFG0 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
3	OUT1P_DIAG_EN	R/W	0x0	Channel-1 Output OUT1P Scan for Diagnostics 0b = Diagnostic Disabled 1b = Diagnostic Enabled
2	OUT1M_DIAG_EN	R/W	0x0	Channel-1 Output OUT1M Scan for Diagnostics 0b = Diagnostic Disabled 1b = Diagnostic Enabled
1	OUT2P_DIAG_EN	R/W	0x0	Channel-2 Output OUT2P Scan for Diagnostics 0b = Diagnostic Disabled 1b = Diagnostic Enabled
0	OUT2M_DIAG_EN	R/W	0x0	Channel-2 Output OUT2M Scan for Diagnostics 0b = Diagnostic Disabled 1b = Diagnostic Enabled

7.2.43 DIAG_CFG1 Register (Address = 0x47) [Reset = 0x37]

DIAG_CFG1 is shown in 図 7-145 and described in 表 7-147.

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図 7-145. DIAG_CFG1 Register

7	6	5	4	3	2	1	0
DIAG_SHT_TERM[3:0]				DIAG_SHT_VBAT_IN[3:0]			
R/W-0011b				R/W-0111b			

表 7-147. DIAG_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_SHT_TERM[3:0]	R/W	0x3	INxP and INxM Terminal Short Detect Threshold 0d = INxP and INxM Terminal Short Detect Threshold Value is 0 mV 1d = INxP and INxM Terminal Short Detect Threshold Value is 30 mV 2d = INxP and INxM Terminal Short Detect Threshold Value is 60 mV 10d to 13d = INxP and INxM Terminal Short Detect Threshold Value is as per configuration 14d = INxP and INxM Terminal Short Detect Threshold Value is 420 mV 15d = INxP and INxM Terminal Short Detect Threshold Value is 450 mV
3-0	DIAG_SHT_VBAT_IN[3:0]	R/W	0x7	Short to VBAT_IN Detect Threshold 0d = Short to VBAT_IN Detect Threshold Value is 0 mV 1d = Short to VBAT_IN Detect Threshold Value is 30 mV 2d = Short to VBAT_IN Detect Threshold Value is 60 mV 10d to 13d = Short to VBAT_IN Detect Threshold Value is as per configuration 14d = Short to VBAT_IN Detect Threshold Value is 420 mV 15d = Short to VBAT_IN Detect Threshold Value is 450 mV

7.2.44 DIAG_CFG2 Register (Address = 0x48) [Reset = 0x87]

DIAG_CFG2 is shown in 図 7-146 and described in 表 7-148.

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図 7-146. DIAG_CFG2 Register

7	6	5	4	3	2	1	0
DIAG_SHT_GND[3:0]				DIAG_SHT_MICBIAS[3:0]			
R/W-1000b				R/W-0111b			

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図 7-146. DIAG_CFG2 Register (続き)

表 7-148. DIAG_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_SHT_GND[3:0]	R/W	0x8	Short to GND Detect Threshold 0d = Short to GND Detect Threshold Value is 0 mV 1d = Short to GND Detect Threshold Value is 60 mV 2d = Short to GND Detect Threshold Value is 120 mV 10d to 13d = Short to GND Detect Threshold Value is as per configuration 14d = Short to GND Detect Threshold Value is 840 mV 15d = Short to GND Detect Threshold Value is 900 mV
3-0	DIAG_SHT_MICBIAS[3:0]	R/W	0x7	Short to MICBIAS Detect Threshold 0d = Short to MICBIAS Detect Threshold Value is 0 mV 1d = Short to MICBIAS Detect Threshold Value is 30 mV 2d = Short to MICBIAS Detect Threshold Value is 60 mV 10d to 13d = Short to MICBIAS Detect Threshold Value is as per configuration 14d = Short to MICBIAS Detect Threshold Value is 420 mV 15d = Short to MICBIAS Detect Threshold Value is 450 mV

7.2.45 DIAG_CFG4 Register (Address = 0x4A) [Reset = 0xB8]

DIAG_CFG4 is shown in 図 7-147 and described in 表 7-149.

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図 7-147. DIAG_CFG4 Register

7	6	5	4	3	2	1	0
RESERVED		RESERVED		FAULT_DBNCE_SEL[1:0]		VSHORT_DBNCE	DIAG_2X_THRES
R-00b		R-00b		R/W-10b		R/W-0b	R/W-0b

表 7-149. DIAG_CFG4 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved bits; Write only reset values
5-4	RESERVED	R	0x0	Reserved bits; Write only reset values
3-2	FAULT_DBNCE_SEL[1:0]	R/W	0x2	Debounce conut for all the faults (except VBAT_IN short when VBAT_IN < MicBias) 0b = 16 counts for debounce to filter-out false faults detection 1b = 8 counts for debounce to filter-out false faults detection 2b = 4 counts for debounce to filter-out false faults detection 3b = No debounce count
1	VSHORT_DBNCE	R/W	0x0	VBAT_IN short debounce count 0b = 16 counts for debounce to filter-out false faults detection 1b = 8 counts for debounce to filter-out false faults detection
0	DIAG_2X_THRES	R/W	0x0	Diagostic thresholds range scale 0d = Thresholds same as configrued 1d = All the configruation thresholds gets scale by 2 times

7.2.46 DIAG_CFG5 Register (Address = 0x4B) [Reset = 0x00]

DIAG_CFG5 is shown in 図 7-148 and described in 表 7-150.

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図 7-148. DIAG_CFG5 Register

7	6	5	4	3	2	1	0
DIAG_MOV_AVG_CFG[1:0]		MOV_AVG_DIS_MBIAS_LOAD	MOV_AVG_DIS_TEMP_SENS	MOV_AVG_DIS_GPA	RESERVED		
R/W-00b		R/W-0b	R/W-0b	R/W-0b	R-000b		

表 7-150. DIAG_CFG5 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DIAG_MOV_AVG_CFG[1:0]	R/W	0x0	Moving average configuration 0d = Moving average disabled 1d = Moving average enabled with 0.5 weightage for new and old data 2d = Moving average enabled with 0.75 weightage for old data and 0.25 weightage for new data 3d = Reserved
5	MOV_AVG_DIS_MBIAS_LOAD	R/W	0x0	Moving average configuration for MicBias Load channel 0b = Moving average is enabled for Micbias Load channel 1b = Moving average is disabled for Micbias Load channel
4	MOV_AVG_DIS_TEMP_SENS	R/W	0x0	Moving average configuration for Temp sense channel 0b = Moving average is enabled for Temp sense channel 1b = Moving average is disabled for Temp sense channel
3	MOV_AVG_DIS_GPA	R/W	0x0	Moving average configuration for GPA channel 0b = Moving average is enabled for GPA channel 1b = Moving average is disabled for GPA channel
2-0	RESERVED	R	0x0	Reserved bits; Write only reset values

7.2.47 DIAG_CFG6 Register (Address = 0x4C) [Reset = 0xA2]

DIAG_CFG6 is shown in 図 7-149 and described in 表 7-151.

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図 7-149. DIAG_CFG6 Register

7	6	5	4	3	2	1	0
MBIAS_HIGH_CURR_THRS[7:0]							
R/W-10100010b							

表 7-151. DIAG_CFG6 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MBIAS_HIGH_CURR_THRS[7:0]	R/W	0xA2	Threshold for Micbias High current fault diagnostics Default = ~ 27mA Nd = ((0.9×(N*16)/4095)-0·2)x72.83237 (mA)

7.2.48 DIAG_CFG7 Register (Address = 0x4D) [Reset = 0x48]

DIAG_CFG7 is shown in 図 7-150 and described in 表 7-152.

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図 7-150. DIAG_CFG7 Register

7	6	5	4	3	2	1	0
MBIAS_LOW_CURR_THRS[7:0]							
R/W-01001000b							

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表 7-152. DIAG_CFG7 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MBIAS_LOW_CURR_THRS[7:0]	R/W	0x48	Threshold for Micbias Low current fault diagnostics Default = ~ 4mA Nd = ((0.9×(N*16)/4095)-0·2)x72.83237 (mA)

7.2.49 DIAG_CFG8 Register (Address = 0x4E) [Reset = 0xBA]

DIAG_CFG8 is shown in 図 7-151 and described in 表 7-153.

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図 7-151. DIAG_CFG8 Register

7	6	5	4	3	2	1	0
GPA_UP_THRS_FLT_THRES[7:0]							
R/W-10111010b							

表 7-153. DIAG_CFG8 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPA_UP_THRS_FLT_THRES[7:0]	R/W	0xBA	General Purpose Analog High Threshold Default = ~ 2.6V nd = ((0.9×(N*16)/4095)-0·225)x6 (V)

7.2.50 DIAG_CFG9 Register (Address = 0x4F) [Reset = 0x4B]

DIAG_CFG9 is shown in 図 7-152 and described in 表 7-154.

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図 7-152. DIAG_CFG9 Register

7	6	5	4	3	2	1	0
GPA_LOW_THRS_FLT_THRES[7:0]							
R/W-01001011b							

表 7-154. DIAG_CFG9 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GPA_LOW_THRS_FLT_THRES[7:0]	R/W	0x4B	General Purpose Analog Low Threshold Default = ~ 0.2V nd = ((0.9×(N*16)/4095)-0·225)x6 (V)

7.2.51 DIAG_CFG10 Register (Address = 0x50) [Reset = 0x88]

DIAG_CFG10 is shown in 図 7-153 and described in 表 7-155.

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図 7-153. DIAG_CFG10 Register

7	6	5	4	3	2	1	0
PD_MBIAS_SHRT_CKT_FLT	PD_MBIAS_HIGH_CURR_FLT	PD_MBIAS_LOW_CURR_FLT	PD_MBIAS_OV_FLT	PD_MBIAS_OT_FLT	MAN_RCV_PD_FLT_CHK	MBIAS_FLT_AUTO_REC_EN	MICBIAS_SHRT_CKT_DET_DIS
R/W-1b	R/W-0b	R/W-0b	R/W-0b	R/W-1b	R/W-0b	R/W-0b	R/W-0b

表 7-155. DIAG_CFG10 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PD_MBIAS_SHRT_CKT_FLT	R/W	0x1	Powerdown configuration of Micbias during Short Circuit fault 0b = No change when fault occurs 1b = Micbias is disabled when fault occurs
6	PD_MBIAS_HIGH_CURR_FLT	R/W	0x0	Powerdown configuration of Micbias during High current fault 0b = No change when fault occurs 1b = Micbias is disabled when fault occurs
5	PD_MBIAS_LOW_CURR_FLT	R/W	0x0	Powerdown configuration of Micbias during Low current fault 0b = No change when fault occurs 1b = Micbias is disabled when fault occurs
4	PD_MBIAS_OV_FLT	R/W	0x0	Powerdown configuration of Micbias during high voltage fault 0b = No change when fault occurs 1b = Micbias is disabled when fault occurs
3	PD_MBIAS_OT_FLT	R/W	0x1	Powerdown configuration of Micbias during over temperature fault 0b = No change when fault occurs 1b = Micbias is disabled when fault occurs
2	MAN_RCV_PD_FLT_CHK	R/W	0x0	Manual Recovery (self clear bit) 0b = No effect 1b = Recheck fault status and re-powerup channels if they do not have any faults
1	MBIAS_FLT_AUTO_REC_EN	R/W	0x0	Micbias PD on faults Auto-Recovery Enable 0d = Auto recovery from Micbias faults disabled 1d = Auto recovery enabled
0	MICBIAS_SHRT_CKT_DET_DIS	R/W	0x0	Micbias Short Circuit fault detect config 0b = enable 1b = disable

7.2.52 DIAG_CFG11 Register (Address = 0x51) [Reset = 0x40]

DIAG_CFG11 is shown in 図 7-154 and described in 表 7-156.

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図 7-154. DIAG_CFG11 Register

7	6	5	4	3	2	1	0
SAFEBAND_MBIAS_OV_FLT[2:0]			RESERVED				
R/W-010b			R-00000b				

表 7-156. DIAG_CFG11 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	SAFEBAND_MBIAS_OV_FLT[2:0]	R/W	0x2	Safeband cfgn for Mbias over voltage fault's lower boundary 0 = No safeband 1 = 30mV safeband (1LSb at 9b lvl) 2 = 60mV safeband (2LSb at 9b lvl) 3-7 = N*30mV
4-0	RESERVED	R	0x0	Reserved bits; Write only reset values

7.2.53 DIAG_CFG12 Register (Address = 0x52) [Reset = 0x44]

DIAG_CFG12 is shown in 図 7-155 and described in 表 7-157.

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図 7-155. DIAG_CFG12 Register

7	6	5	4	3	2	1	0

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図 7-155. DIAG_CFG12 Register (続き)

SAFEBAND_INx_MBIAS_FLT[2:0]	SAFEBAND_INx_OV_FLT[2:0]	RESERVED
R/W-010b	R/W-001b	R-00b

表 7-157. DIAG_CFG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	SAFEBAND_INx_MBIAS_FLT[2:0]	R/W	0x2	Safeband cfgn for INx Short to Mbias fault's upper boundary 0 = No safeband 1 = 30mV safeband (1LSb at 9b lvl) 2 = 60mV safeband (2LSb at 9b lvl) 3-7 = N*30mV
4-2	SAFEBAND_INx_OV_FLT[2:0]	R/W	0x1	Safeband cfgn for INx Overvoltage fault's lower boundary 0 = No safeband 1 = 30mV safeband (1LSb at 9b lvl) 2-7 = N*30mV Dont use
1-0	RESERVED	R	0x0	Reserved bits; Write only reset values

7.2.54 DIAG_CFG13 Register (Address = 0x53) [Reset = 0x00]

DIAG_CFG13 is shown in 図 7-156 and described in 表 7-158.

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図 7-156. DIAG_CFG13 Register

7	6	5	4	3	2	1	0
DIAG_FORCE_EN	DIAG_EN_MICBIAS_LOAD	DIAG_EN_MICBIAS	DIAG_EN_VBAT	DIAG_EN_TEMP_SENSE	DIAG_EN_AVDD	DIAG_EN_GPA	RESERVED
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R-0b

表 7-158. DIAG_CFG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DIAG_FORCE_EN	R/W	0x0	Configuration for auto/manual enable for diag vbat, micbias, micbias load, temp 0b = Auto enabled (auto enabled if atlease one of the input channel diagnostics is enabled in DIAG_CFG0) 1b = Manual en/disable based on DIAG_CFG13 Register
6	DIAG_EN_MICBIAS_LOAD	R/W	0x0	Micbias current/load channel enable for Diagnostics, valid if DIAG_FORCE_EN = 1 0b = Diagnostic Disabled 1b = Diagnostic Enabled
5	DIAG_EN_MICBIAS	R/W	0x0	Micbias channel enable for Diagnostics, valid if DIAG_FORCE_EN = 1 0b = Diagnostic Disabled 1b = Diagnostic Enabled
4	DIAG_EN_VBAT	R/W	0x0	VBAT channel enable for Diagnostics, valid if DIAG_FORCE_EN = 1 0b = Diagnostic Disabled 1b = Diagnostic Enabled
3	DIAG_EN_TEMP_SENSE	R/W	0x0	Temp sense channel enable for Diagnostics, valid if DIAG_FORCE_EN = 1 0b = Diagnostic Disabled 1b = Diagnostic Enabled
2	DIAG_EN_AVDD	R/W	0x0	AVDD channel enable for Diagnostics 0b = Diagnostic Disabled 1b = Diagnostic Enabled

表 7-158. DIAG_CFG13 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
1	DIAG_EN_GPA	R/W	0x0	GPA channel enable for Diagnostics 0b = Diagnostic Disabled 1b = Diagnostic Enabled
0	RESERVED	R	0x0	Reserved bit; Write only reset value

7.2.55 DIAG_CFG14 Register (Address = 0x54) [Reset = 0x48]

DIAG_CFG14 is shown in 図 7-157 and described in 表 7-159.

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図 7-157. DIAG_CFG14 Register

7	6	5	4	3	2	1	0
RESERVED	AVDD_FILT_SEL[1:0]		RESERVED	VBAT_FILT_SEL[1:0]		RESERVED	VBAT_SHRT_FLT
R-0b	R/W-10b		R-0b	R/W-10b		R-0b	R/W-0b

表 7-159. DIAG_CFG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved bit; Write only reset value
6-5	AVDD_FILT_SEL[1:0]	R/W	0x2	AVDD filter select 0d = 3.5MHz 1d = 200kHz 2d = 100kHz 3d = No filter
4	RESERVED	R	0x0	Reserved bit; Write only reset value
3-2	VBAT_FILT_SEL[1:0]	R/W	0x2	VBAT filter select 0d = 3.5MHz 1d = 200kHz 2d = 100kHz 3d = No filter
1	RESERVED	R	0x0	Reserved bit; Write only reset value
0	VBAT_SHRT_FLT	R/W	0x0	Cfgn on INx short to VBAT 0 = INx Overvoltage and INx short to VBAT are separate 1 = INx Overvoltage and INx short to VBAT are Ord together as VBAT short fault

7.2.56 DIAG_MON_MSB_VBAT Register (Address = 0x56) [Reset = 0x00]

DIAG_MON_MSB_VBAT is shown in 図 7-158 and described in 表 7-160.

Return to the Summary Table.

図 7-158. DIAG_MON_MSB_VBAT Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_VBAT[7:0]							
R-00000000b							

表 7-160. DIAG_MON_MSB_VBAT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_VBAT[7:0]	R	0x0	Diagnostic SAR Monitor Data MSB Byte

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7.2.57 DIAG_MON_LSB_VBAT Register (Address = 0x57) [Reset = 0x00]

DIAG_MON_LSB_VBAT is shown in 図 7-159 and described in 表 7-161.

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図 7-159. DIAG_MON_LSB_VBAT Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_VBAT[3:0]				Channel[3:0]			
R-0000b				R-0000b			

表 7-161. DIAG_MON_LSB_VBAT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_VBAT[3:0]	R	0x0	Diagnostic SAR Monitor Data LSB Nibble
3-0	Channel[3:0]	R	0x0	Channel ID

7.2.58 DIAG_MON_MSB_MBIAS Register (Address = 0x58) [Reset = 0x00]

DIAG_MON_MSB_MBIAS is shown in 図 7-160 and described in 表 7-162.

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図 7-160. DIAG_MON_MSB_MBIAS Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_MBIAS[7:0]							
R-00000000b							

表 7-162. DIAG_MON_MSB_MBIAS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_MBIAS[7:0]	R	0x0	Diagnostic SAR Monitor Data MSB Byte

7.2.59 DIAG_MON_LSB_MBIAS Register (Address = 0x59) [Reset = 0x01]

DIAG_MON_LSB_MBIAS is shown in 図 7-161 and described in 表 7-163.

Return to the Summary Table.

図 7-161. DIAG_MON_LSB_MBIAS Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_MBIAS[3:0]				Channel[3:0]			
R-0000b				R-0001b			

表 7-163. DIAG_MON_LSB_MBIAS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_MBIAS[3:0]	R	0x0	Diagnostic SAR Monitor Data LSB Nibble
3-0	Channel[3:0]	R	0x1	Channel ID

7.2.60 DIAG_MON_MSB_IN1P Register (Address = 0x5A) [Reset = 0x00]

DIAG_MON_MSB_IN1P is shown in 図 7-162 and described in 表 7-164.

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図 7-162. DIAG_MON_MSB_IN1P Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_IN_CH1P[7:0]							
R-00000000b							

表 7-164. DIAG_MON_MSB_IN1P Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_IN_CH1P[7:0]	R	0x0	Diagnostic SAR Monitor Data MSB Byte

7.2.61 DIAG_MON_LSB_IN1P Register (Address = 0x5B) [Reset = 0x02]

DIAG_MON_LSB_IN1P is shown in 図 7-163 and described in 表 7-165.

Return to the Summary Table.

図 7-163. DIAG_MON_LSB_IN1P Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_IN_CH1P[3:0]				Channel[3:0]			
R-0000b				R-0010b			

表 7-165. DIAG_MON_LSB_IN1P Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_IN_CH1P[3:0]	R	0x0	Diagnostic SAR Monitor Data LSB Nibble
3-0	Channel[3:0]	R	0x2	Channel ID

7.2.62 DIAG_MON_MSB_IN1M Register (Address = 0x5C) [Reset = 0x00]

DIAG_MON_MSB_IN1M is shown in 図 7-164 and described in 表 7-166.

Return to the Summary Table.

図 7-164. DIAG_MON_MSB_IN1M Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_IN_CH1N[7:0]							
R-00000000b							

表 7-166. DIAG_MON_MSB_IN1M Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_IN_CH1N[7:0]	R	0x0	Diagnostic SAR Monitor Data MSB Byte

7.2.63 DIAG_MON_LSB_IN1M Register (Address = 0x5D) [Reset = 0x03]

DIAG_MON_LSB_IN1M is shown in 図 7-165 and described in 表 7-167.

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図 7-165. DIAG_MON_LSB_IN1M Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_IN_CH1N[3:0]				Channel[3:0]			
R-0000b				R-0011b			

表 7-167. DIAG_MON_LSB_IN1M Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_IN_CH1N[3:0]	R	0x0	Diagnostic SAR Monitor Data LSB Nibble
3-0	Channel[3:0]	R	0x3	Channel ID

7.2.64 DIAG_MON_MSB_IN2P Register (Address = 0x5E) [Reset = 0x00]

DIAG_MON_MSB_IN2P is shown in 図 7-166 and described in 表 7-168.

Return to the Summary Table.

図 7-166. DIAG_MON_MSB_IN2P Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_IN_CH2P[7:0]							
R-00000000b							

表 7-168. DIAG_MON_MSB_IN2P Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_IN_CH2P[7:0]	R	0x0	Diagnostic SAR Monitor Data MSB Byte

7.2.65 DIAG_MON_LSB_IN2P Register (Address = 0x5F) [Reset = 0x04]

DIAG_MON_LSB_IN2P is shown in 図 7-167 and described in 表 7-169.

Return to the Summary Table.

図 7-167. DIAG_MON_LSB_IN2P Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_IN_CH2P[3:0]				Channel[3:0]			
R-0000b				R-0100b			

表 7-169. DIAG_MON_LSB_IN2P Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_IN_CH2P[3:0]	R	0x0	Diagnostic SAR Monitor Data LSB Nibble
3-0	Channel[3:0]	R	0x4	Channel ID

7.2.66 DIAG_MON_MSB_IN2M Register (Address = 0x60) [Reset = 0x00]

DIAG_MON_MSB_IN2M is shown in 図 7-168 and described in 表 7-170.

Return to the Summary Table.

図 7-168. DIAG_MON_MSB_IN2M Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_IN_CH2N[7:0]							
R-00000000b							

表 7-170. DIAG_MON_MSB_IN2M Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_IN_CH2N[7:0]	R	0x0	Diagnostic SAR Monitor Data MSB Byte

7.2.67 DIAG_MON_LSB_IN2M Register (Address = 0x61) [Reset = 0x05]

DIAG_MON_LSB_IN2M is shown in 図 7-169 and described in 表 7-171.

Return to the Summary Table.

図 7-169. DIAG_MON_LSB_IN2M Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_IN_CH2N[3:0]				Channel[3:0]			
R-0000b				R-0101b			

表 7-171. DIAG_MON_LSB_IN2M Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_IN_CH2N[3:0]	R	0x0	Diagnostic SAR Monitor Data LSB Nibble
3-0	Channel[3:0]	R	0x5	Channel ID

7.2.68 DIAG_MON_MSB_OUT1P Register (Address = 0x62) [Reset = 0x00]

DIAG_MON_MSB_OUT1P is shown in 図 7-170 and described in 表 7-172.

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図 7-170. DIAG_MON_MSB_OUT1P Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_OUT_CH1P[7:0]							
R-00000000b							

表 7-172. DIAG_MON_MSB_OUT1P Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_OUT_CH1P[7:0]	R	0x0	Diagnostic SAR Monitor Data MSB Byte

7.2.69 DIAG_MON_LSB_OUT1P Register (Address = 0x63) [Reset = 0x06]

DIAG_MON_LSB_OUT1P is shown in 図 7-171 and described in 表 7-173.

Return to the Summary Table.

図 7-171. DIAG_MON_LSB_OUT1P Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_OUT_CH1P[3:0]				Channel[3:0]			

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図 7-171. DIAG_MON_LSB_OUT1P Register (続き)

R-0000b	R-0110b

表 7-173. DIAG_MON_LSB_OUT1P Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_OUT_CH1P[3:0]	R	0x0	Diagnostic SAR Monitor Data LSB Nibble
3-0	Channel[3:0]	R	0x6	Channel ID

7.2.70 DIAG_MON_MSB_OUT1M Register (Address = 0x64) [Reset = 0x00]

DIAG_MON_MSB_OUT1M is shown in 図 7-172 and described in 表 7-174.

Return to the Summary Table.

図 7-172. DIAG_MON_MSB_OUT1M Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_OUT_CH1N[7:0]							
R-00000000b							

表 7-174. DIAG_MON_MSB_OUT1M Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_OUT_CH1N[7:0]	R	0x0	Diagnostic SAR Monitor Data MSB Byte

7.2.71 DIAG_MON_LSB_OUT1M Register (Address = 0x65) [Reset = 0x07]

DIAG_MON_LSB_OUT1M is shown in 図 7-173 and described in 表 7-175.

Return to the Summary Table.

図 7-173. DIAG_MON_LSB_OUT1M Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_OUT_CH1N[3:0]				Channel[3:0]			
R-0000b				R-0111b			

表 7-175. DIAG_MON_LSB_OUT1M Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_OUT_CH1N[3:0]	R	0x0	Diagnostic SAR Monitor Data LSB Nibble
3-0	Channel[3:0]	R	0x7	Channel ID

7.2.72 DIAG_MON_MSB_OUT2P Register (Address = 0x66) [Reset = 0x00]

DIAG_MON_MSB_OUT2P is shown in 図 7-174 and described in 表 7-176.

Return to the Summary Table.

図 7-174. DIAG_MON_MSB_OUT2P Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_OUT_CH2P[7:0]							
R-00000000b							

図 7-174. DIAG_MON_MSB_OUT2P Register (続き)

表 7-176. DIAG_MON_MSB_OUT2P Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_OUT_CH2P[7:0]	R	0x0	Diagnostic SAR Monitor Data MSB Byte

7.2.73 DIAG_MON_LSB_OUT2P Register (Address = 0x67) [Reset = 0x08]

DIAG_MON_LSB_OUT2P is shown in 図 7-175 and described in 表 7-177.

Return to the Summary Table.

図 7-175. DIAG_MON_LSB_OUT2P Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_OUT_CH2P[3:0]				Channel[3:0]			
R-0000b				R-1000b			

表 7-177. DIAG_MON_LSB_OUT2P Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_OUT_CH2P[3:0]	R	0x0	Diagnostic SAR Monitor Data LSB Nibble
3-0	Channel[3:0]	R	0x8	Channel ID

7.2.74 DIAG_MON_MSB_OUT2M Register (Address = 0x68) [Reset = 0x00]

DIAG_MON_MSB_OUT2M is shown in 図 7-176 and described in 表 7-178.

Return to the Summary Table.

図 7-176. DIAG_MON_MSB_OUT2M Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_OUT_CH2N[7:0]							
R-00000000b							

表 7-178. DIAG_MON_MSB_OUT2M Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_OUT_CH2N[7:0]	R	0x0	Diagnostic SAR Monitor Data MSB Byte

7.2.75 DIAG_MON_LSB_OUT2M Register (Address = 0x69) [Reset = 0x09]

DIAG_MON_LSB_OUT2M is shown in 図 7-177 and described in 表 7-179.

Return to the Summary Table.

図 7-177. DIAG_MON_LSB_OUT2M Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_OUT_CH2N[3:0]				Channel[3:0]			
R-0000b				R-1001b			

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表 7-179. DIAG_MON_LSB_OUT2M Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_OUT_CH2N[3:0]	R	0x0	Diagnostic SAR Monitor Data LSB Nibble
3-0	Channel[3:0]	R	0x9	Channel ID

7.2.76 DIAG_MON_MSB_TEMP Register (Address = 0x6A) [Reset = 0x00]

DIAG_MON_MSB_TEMP is shown in 図 7-178 and described in 表 7-180.

Return to the Summary Table.

図 7-178. DIAG_MON_MSB_TEMP Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_TEMP[7:0]							
R-00000000b							

表 7-180. DIAG_MON_MSB_TEMP Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_TEMP[7:0]	R	0x0	Diagnostic SAR Monitor Data MSB Byte

7.2.77 DIAG_MON_LSB_TEMP Register (Address = 0x6B) [Reset = 0x0A]

DIAG_MON_LSB_TEMP is shown in 図 7-179 and described in 表 7-181.

Return to the Summary Table.

図 7-179. DIAG_MON_LSB_TEMP Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_TEMP[3:0]				Channel[3:0]			
R-0000b				R-1010b			

表 7-181. DIAG_MON_LSB_TEMP Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_TEMP[3:0]	R	0x0	Diagnostic SAR Monitor Data LSB Nibble
3-0	Channel[3:0]	R	0xA	Channel ID

7.2.78 DIAG_MON_MSB_MBIAS_LOAD Register (Address = 0x6C) [Reset = 0x00]

DIAG_MON_MSB_MBIAS_LOAD is shown in 図 7-180 and described in 表 7-182.

Return to the Summary Table.

図 7-180. DIAG_MON_MSB_MBIAS_LOAD Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_MBIAS_LOAD[7:0]							
R-00000000b							

表 7-182. DIAG_MON_MSB_MBIAS_LOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_MBIAS_LOAD[7:0]	R	0x0	Diagnostic SAR Monitor Data MSB Byte

7.2.79 DIAG_MON_LSB_MBIAS_LOAD Register (Address = 0x6D) [Reset = 0x0B]

DIAG_MON_LSB_MBIAS_LOAD is shown in 図 7-181 and described in 表 7-183.

Return to the Summary Table.

図 7-181. DIAG_MON_LSB_MBIAS_LOAD Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_MBIAS_LOAD[3:0]				Channel[3:0]			
R-0000b				R-1011b			

表 7-183. DIAG_MON_LSB_MBIAS_LOAD Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_MBIAS_LOAD[3:0]	R	0x0	Diagnostic SAR Monitor Data LSB Nibble
3-0	Channel[3:0]	R	0xB	Channel ID

7.2.80 DIAG_MON_MSB_AVDD Register (Address = 0x6E) [Reset = 0x00]

DIAG_MON_MSB_AVDD is shown in 図 7-182 and described in 表 7-184.

Return to the Summary Table.

図 7-182. DIAG_MON_MSB_AVDD Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_AVDD[7:0]							
R-00000000b							

表 7-184. DIAG_MON_MSB_AVDD Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_AVDD[7:0]	R	0x0	Diagnostic SAR Monitor Data MSB Byte

7.2.81 DIAG_MON_LSB_AVDD Register (Address = 0x6F) [Reset = 0x0C]

DIAG_MON_LSB_AVDD is shown in 図 7-183 and described in 表 7-185.

Return to the Summary Table.

図 7-183. DIAG_MON_LSB_AVDD Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_AVDD[3:0]				Channel[3:0]			
R-0000b				R-1100b			

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表 7-185. DIAG_MON_LSB_AVDD Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_AVDD[3:0]	R	0x0	Diagnostic SAR Monitor Data LSB Nibble
3-0	Channel[3:0]	R	0xC	Channel ID

7.2.82 DIAG_MON_MSB_GPA Register (Address = 0x70) [Reset = 0x00]

DIAG_MON_MSB_GPA is shown in 図 7-184 and described in 表 7-186.

Return to the Summary Table.

図 7-184. DIAG_MON_MSB_GPA Register

7	6	5	4	3	2	1	0
DIAG_MON_MSB_GPA[7:0]							
R-00000000b							

表 7-186. DIAG_MON_MSB_GPA Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	DIAG_MON_MSB_GPA[7:0]	R	0x0	Diagnostic SAR Monitor Data MSB Byte

7.2.83 DIAG_MON_LSB_GPA Register (Address = 0x71) [Reset = 0x0D]

DIAG_MON_LSB_GPA is shown in 図 7-185 and described in 表 7-187.

Return to the Summary Table.

図 7-185. DIAG_MON_LSB_GPA Register

7	6	5	4	3	2	1	0
DIAG_MON_LSB_GPA[3:0]				Channel[3:0]			
R-0000b				R-1101b			

表 7-187. DIAG_MON_LSB_GPA Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	DIAG_MON_LSB_GPA[3:0]	R	0x0	Diagnostic SAR Monitor Data LSB Nibble
3-0	Channel[3:0]	R	0xD	Channel ID

7.2.84 BOOST_CFG Register (Address = 0x72) [Reset = 0x00]

BOOST_CFG is shown in 図 7-186 and described in 表 7-188.

Return to the Summary Table.

図 7-186. BOOST_CFG Register

7	6	5	4	3	2	1	0
BOOST_DIS	BOOST_OCPEN	BOOST_PDz_FLT	RESERVED	RESERVED	RESERVED		
R/W-0b	R/W-0b	R/W-0b	R-0b	R-0b	R-000b		

表 7-188. BOOST_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	BOOST_DIS	R/W	0x0	Boost Enable/Disable 0d = Internal Boost enable 1d = Internal Boost disable/bypass
6	BOOST_OCPEN	R/W	0x0	Boost Over Current Protection Enable/Disable 0d = Boost OCP is enable 1d = Boost OCP is disable
5	BOOST_PDz_FLT	R/W	0x0	Boost PD cfgn 0d = Boost is powered down if Micbias is powered down due to faults 1d = Boost is NOT powered down if Micbias is powered down due to faults
4	RESERVED	R	0x0	Reserved bit; Write only reset value
3	RESERVED	R	0x0	Reserved bit; Write only reset value
2-0	RESERVED	R	0x0	Reserved bits; Write only reset values

7.2.85 MICBIAS_CFG Register (Address = 0x73) [Reset = 0xA0]

MICBIAS_CFG is shown in 図 7-187 and described in 表 7-189.

Return to the Summary Table.

図 7-187. MICBIAS_CFG Register

7	6	5	4	3	2	1	0
MBIAS_VAL[3:0]				RESERVED			
R/W-1010b				R-0000b			

表 7-189. MICBIAS_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	MBIAS_VAL[3:0]	R/W	0xA	MicBias Value 0d = Microphone Bias output is bypassed to BSTOUT/HVDD 1d = Microphone Bias is set to 3.0 V 2d = Microphone Bias is set to 3.5 V 3d = Microphone Bias is set to 4.0 V 4d = Microphone Bias is set to 4.5 V 5d = Microphone Bias is set to 5 V 6d = Microphone Bias is set to 5.5 V 7d = Microphone Bias is set to 6 V 8d = Microphone Bias is set to 6.5 V 9d = Microphone Bias is set to 7 V 10d = Microphone Bias is set to 7.5 V 11d = Microphone Bias is set to 8 V 12d = Microphone Bias is set to 8.5 V 13d = Microphone Bias is set to 9 V 14d = Microphone Bias is set to 9.5 V 15d = Microphone Bias is set to 10 V
3-0	RESERVED	R	0x0	Reserved bits; Write only reset value

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7.3 Page_3 Registers

表 7-190 lists the memory-mapped registers for the Page_3 registers. All register offset addresses not listed in 表 7-190 should be considered as reserved locations and the register contents should not be modified.

表 7-190. PAGE_3 Registers

Address	Acronym	Register Name	Reset Value	Section
0x0	PAGE_CFG	Device page register	0x00	セクション 7.3.1
0x1A	SASI_CFG0	Secondary ASI configuration register 0	0x30	セクション 7.3.2
0x1B	SASI_TX_CFG0	SASI TX configuration register 0	0x00	セクション 7.3.3
0x1C	SASI_TX_CFG1	SASI TX configuration register 1	0x00	セクション 7.3.4
0x1D	SASI_TX_CFG2	SASI TX configuration register 2	0x00	セクション 7.3.5
0x1E	SASI_TX_CH1_CFG	SASI TX Channel 1 configuration register	0x00	セクション 7.3.6
0x1F	SASI_TX_CH2_CFG	SASI TX Channel 2 configuration register	0x01	セクション 7.3.7
0x20	SASI_TX_CH3_CFG	SASI TX Channel 3 configuration register	0x02	セクション 7.3.8
0x21	SASI_TX_CH4_CFG	SASI TX Channel 4 configuration register	0x03	セクション 7.3.9
0x22	SASI_TX_CH5_CFG	SASI TX Channel 5 configuration register	0x04	セクション 7.3.10
0x23	SASI_TX_CH6_CFG	SASI TX Channel 6 configuration register	0x05	セクション 7.3.11
0x24	SASI_TX_CH7_CFG	SASI TX Channel 7 configuration register	0x06	セクション 7.3.12
0x25	SASI_TX_CH8_CFG	SASI TX Channel 8 configuration register	0x07	セクション 7.3.13
0x26	SASI_RX_CFG0	SASI RX configuration register 0	0x00	セクション 7.3.14
0x27	SASI_RX_CFG1	SASI RX configuration register 1	0x00	セクション 7.3.15
0x28	SASI_RX_CH1_CFG	SASI RX Channel 1 configuration register	0x00	セクション 7.3.16
0x29	SASI_RX_CH2_CFG	SASI RX Channel 2 configuration register	0x01	セクション 7.3.17
0x2A	SASI_RX_CH3_CFG	SASI RX Channel 3 configuration register	0x02	セクション 7.3.18
0x2B	SASI_RX_CH4_CFG	SASI RX Channel 4 configuration register	0x03	セクション 7.3.19
0x2C	SASI_RX_CH5_CFG	SASI RX Channel 5 configuration register	0x04	セクション 7.3.20
0x2D	SASI_RX_CH6_CFG	SASI RX Channel 6 configuration register	0x05	セクション 7.3.21
0x2E	SASI_RX_CH7_CFG	SASI RX Channel 7 configuration register	0x06	セクション 7.3.22
0x2F	SASI_RX_CH8_CFG	SASI RX Channel 8 configuration register	0x07	セクション 7.3.23
0x32	CLK_CFG12	Clock configuration register 12	0x00	セクション 7.3.24
0x33	CLK_CFG13		0x00	セクション 7.3.25
0x34	CLK_CFG14	Clock configuration register 14	0x10	セクション 7.3.26
0x35	CLK_CFG15	Clock configuration register 15	0x01	セクション 7.3.27
0x36	CLK_CFG16	Clock configuration register 16	0x00	セクション 7.3.28
0x37	CLK_CFG17	Clock configuration register 17	0x00	セクション 7.3.29
0x38	CLK_CFG18	Clock configuration register 18	0x08	セクション 7.3.30
0x39	CLK_CFG19	Clock configuration register 19	0x20	セクション 7.3.31
0x3A	CLK_CFG20	Clock configuration register 20	0x04	セクション 7.3.32
0x3B	CLK_CFG21	Clock configuration register 21	0x00	セクション 7.3.33
0x3C	CLK_CFG22	Clock configuration register 18	0x01	セクション 7.3.34
0x3D	CLK_CFG23	Clock configuration register 18	0x01	セクション 7.3.35
0x3E	CLK_CFG24	Clock configuration register 21	0x01	セクション 7.3.36
0x44	CLK_CFG30		0x00	セクション 7.3.37
0x45	CLK_CFG31		0x00	セクション 7.3.38
0x46	CLKOUT_CFG1	CLKOUT configuration register 1	0x00	セクション 7.3.39

表 7-190. PAGE_3 Registers (続き)

Address	Acronym	Register Name	Reset Value	Section
0x47	CLKOUT_CFG2	CLKOUT configuration register 2	0x01	セクション 7.3.40
0x48	BSTCLK_CFG1	Boost clock configuration register 1	0x00	セクション 7.3.41
0x49	SARCLK_CFG1	SAR clock configuration register 1	0x00	セクション 7.3.42
0x5B	ADC_OVRLD_FLAG		0x00	セクション 7.3.43

7.3.1 PAGE_CFG Register (Address = 0x0) [Reset = 0x00]

PAGE_CFG is shown in 図 7-188 and described in 表 7-191.

Return to the Summary Table.

The device memory map is divided into pages. This register sets the page.

図 7-188. PAGE_CFG Register

7	6	5	4	3	2	1	0
PAGE[7:0]							
R/W-00000000b							

表 7-191. PAGE_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PAGE[7:0]	R/W	0x0	These bits set the device page. 0d = Page 0 1d = Page 1 2d to 254d = Page 2 to page 254 respectively 255d = Page 255

7.3.2 SASI_CFG0 Register (Address = 0x1A) [Reset = 0x30]

SASI_CFG0 is shown in 図 7-189 and described in 表 7-192.

Return to the Summary Table.

This register is the ASI configuration register 0.

図 7-189. SASI_CFG0 Register

7	6	5	4	3	2	1	0
SASI_FORMAT[1:0]		SASI_WLEN[1:0]		SASI_FSYNC_POL	SASI_BCLK_POL	SASI_BUS_ERR	SASI_BUS_ERR_RCOV
R/W-00b		R/W-11b		R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 7-192. SASI_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	SASI_FORMAT[1:0]	R/W	0x0	Secondary ASI protocol format. 0d = TDM mode 1d = I^2S mode 2d = LJ (left-justified) mode 3d = Reserved; Don't use
5-4	SASI_WLEN[1:0]	R/W	0x3	Secondary ASI word or slot length. 0d = 16 bits (Recommended this setting to be used with 10-kΩ input impedance configuration) 1d = 20 bits 2d = 24 bits 3d = 32 bits

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表 7-192. SASI_CFG0 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
3	SASI_FSYNC_POL	R/W	0x0	ASI FSYNC polarity (for SASI protocol only). 0d = Default polarity as per standard protocol 1d = Inverted polarity with respect to standard protocol
2	SASI_BCLK_POL	R/W	0x0	ASI BCLK polarity (for SASI protocol only). 0d = Default polarity as per standard protocol 1d = Inverted polarity with respect to standard protocol
1	SASI_BUS_ERR	R/W	0x0	ASI bus error detection. 0d = Enable bus error detection 1d = Disable bus error detection
0	SASI_BUS_ERR_RCOV	R/W	0x0	ASI bus error auto resume. 0d = Enable auto resume after bus error recovery 1d = Disable auto resume after bus error recovery and remain powered down until host configures the device

7.3.3 SASI_TX_CFG0 Register (Address = 0x1B) [Reset = 0x00]

SASI_TX_CFG0 is shown in 図 7-190 and described in 表 7-193.

Return to the Summary Table.

This register is the SASI TX configuration register 0.

図 7-190. SASI_TX_CFG0 Register

7	6	5	4	3	2	1	0
SASI_TX_EDGE	SASI_TX_FILL	SASI_TX_LSB	SASI_TX_KEEPER[1:0]		SASI_TX_USE_INT_FSYNC	SASI_TX_USE_INT_BCLK	SASI_TDM_PULSE_WIDTH
R/W-0b	R/W-0b	R/W-0b	R/W-00b		R/W-0b	R/W-0b	R/W-0b

表 7-193. SASI_TX_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SASI_TX_EDGE	R/W	0x0	Secondary ASI data output (on the primary and secondary data pin) transmit edge. 0d = Default edge as per the protocol configuration setting in SASI_BCLK_POL 1d = Inverted following edge (half cycle delay) with respect to the default edge setting
6	SASI_TX_FILL	R/W	0x0	Secondary ASI data output (on the primary and secondary data pin) for any unused cycles 0d = Always transmit 0 for unused cycles 1d = Always use Hi-Z for unused cycles
5	SASI_TX_LSB	R/W	0x0	Secondary ASI data output (on the primary and secondary data pin) for LSB transmissions. 0d = Transmit the LSB for a full cycle 1d = Transmit the LSB for the first half cycle and Hi-Z for the second half cycle
4-3	SASI_TX_KEEPER[1:0]	R/W	0x0	Secondary ASI data output (on the primary and secondary data pin) bus keeper. 0d = Bus keeper is always disabled 1d = Bus keeper is always enabled 2d = Bus keeper is enabled during LSB transmissions only for one cycle 3d = Bus keeper is enabled during LSB transmissions only for one and half cycles
2	SASI_TX_USE_INT_FSYNC	R/W	0x0	Secondary ASI uses internal FSYNC for output data generation in controller mode configuration as applicable. 0d = Use external FSYNC for ASI protocol data generation 1d = Use internal FSYNC for ASI protocol data generation

表 7-193. SASI_TX_CFG0 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
1	SASI_TX_USE_INT_BCLK	R/W	0x0	Secondary ASI uses internal BCLK for output data generation in controller mode configuration. 0d = Use external BCLK for ASI protocol data generation 1d = Use internal BCLK for ASI protocol data generation
0	SASI_TDM_PULSE_WIDTH	R/W	0x0	Secondary ASI fsync pulse width in TDM format. 0d = Fsync pulse is 1 bclk period wide 1d = Fsync pulse is 2 bclk period wide

7.3.4 SASI_TX_CFG1 Register (Address = 0x1C) [Reset = 0x00]

SASI_TX_CFG1 is shown in 図 7-191 and described in 表 7-194.

Return to the Summary Table.

This register is the SASI TX configuration register 1.

図 7-191. SASI_TX_CFG1 Register

7	6	5	4	3	2	1	0
RESERVED			SASI_TX_OFFSET[4:0]				
R-000b			R/W-00000b				

表 7-194. SASI_TX_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0x0	Reserved bits; Write only reset value
4-0	SASI_TX_OFFSET[4:0]	R/W	0x0	Secondary ASI output data MSB slot 0 offset (on the primary and secondary data pin). 0d = ASI data MSB location has no offset and is as per standard protocol 1d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset of one BCLK cycle with respect to standard protocol 2d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset of two BCLK cycles with respect to standard protocol 3d to 30d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset assigned as per configuration 31d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset of 31 BCLK cycles with respect to standard protocol

7.3.5 SASI_TX_CFG2 Register (Address = 0x1D) [Reset = 0x00]

SASI_TX_CFG2 is shown in 図 7-192 and described in 表 7-195.

Return to the Summary Table.

This register is the SASI TX configuration register 2.

図 7-192. SASI_TX_CFG2 Register

7	6	5	4	3	2	1	0
SASI_TX_CH8_SEL	SASI_TX_CH7_SEL	SASI_TX_CH6_SEL	SASI_TX_CH5_SEL	SASI_TX_CH4_SEL	SASI_TX_CH3_SEL	SASI_TX_CH2_SEL	SASI_TX_CH1_SEL
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

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表 7-195. SASI_TX_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SASI_TX_CH8_SEL	R/W	0x0	Secondary ASI output channel 8 select. 0d = Secondary ASI channel 8 output is on DOUT 1d = Secondary ASI channel 8 output is on DOUT2
6	SASI_TX_CH7_SEL	R/W	0x0	Secondary ASI output channel 7 select. 0d = Secondary ASI channel 7 output is on DOUT 1d = Secondary ASI channel 7 output is on DOUT2
5	SASI_TX_CH6_SEL	R/W	0x0	Secondary ASI output channel 6 select. 0d = Secondary ASI channel 6 output is on DOUT 1d = Secondary ASI channel 6 output is on DOUT2
4	SASI_TX_CH5_SEL	R/W	0x0	Secondary ASI output channel 5 select. 0d = Secondary ASI channel 5 output is on DOUT 1d = Secondary ASI channel 5 output is on DOUT2
3	SASI_TX_CH4_SEL	R/W	0x0	Secondary ASI output channel 4 select. 0d = Secondary ASI channel 4 output is on DOUT 1d = Secondary ASI channel 4 output is on DOUT2
2	SASI_TX_CH3_SEL	R/W	0x0	Secondary ASI output channel 3 select. 0d = Secondary ASI channel 3 output is on DOUT 1d = Secondary ASI channel 3 output is on DOUT2
1	SASI_TX_CH2_SEL	R/W	0x0	Secondary ASI output channel 2 select. 0d = Secondary ASI channel 2 output is on DOUT 1d = Secondary ASI channel 2 output is on DOUT2
0	SASI_TX_CH1_SEL	R/W	0x0	Secondary ASI output channel 1 select. 0d = Secondary ASI channel 1 output is on DOUT 1d = Secondary ASI channel 1 output is on DOUT2

7.3.6 SASI_TX_CH1_CFG Register (Address = 0x1E) [Reset = 0x00]

SASI_TX_CH1_CFG is shown in 図 7-193 and described in 表 7-196.

Return to the Summary Table.

This register is the SASI TX Channel 1 configuration register.

図 7-193. SASI_TX_CH1_CFG Register

7	6	5	4	3	2	1	0
RESERVED		SASI_TX_CH1_CFG	SASI_TX_CH1_SLOT_NUM[4:0]				
R-00b		R/W-0b	R/W-00000b				

表 7-196. SASI_TX_CH1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved bits; Write only reset value
5	SASI_TX_CH1_CFG	R/W	0x0	Secondary ASI output channel 1 configuration. 0d = Secondary ASI channel 1 output is in a tri-state condition 1d = Secondary ASI channel 1 output corresponds to ADC Channel 1 data
4-0	SASI_TX_CH1_SLOT_NUM[4:0]	R/W	0x0	Secondary ASI output channel 1 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^2S, LJ is left slot 15 16d = TDM is slot 16 or I^2S, LJ is right slot 0 17d = TDM is slot 17 or I^2S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is right slot 15

7.3.7 SASI_TX_CH2_CFG Register (Address = 0x1F) [Reset = 0x01]

SASI_TX_CH2_CFG is shown in 図 7-194 and described in 表 7-197.

Return to the Summary Table.

This register is the SASI TX Channel 2 configuration register.

図 7-194. SASI_TX_CH2_CFG Register

7	6	5	4	3	2	1	0
RESERVED		SASI_TX_CH2_CFG	SASI_TX_CH2_SLOT_NUM[4:0]				
R-00b		R/W-0b	R/W-00001b				

表 7-197. SASI_TX_CH2_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved bits; Write only reset value
5	SASI_TX_CH2_CFG	R/W	0x0	Secondary ASI output channel 2 configuration. 0d = Secondary ASI channel 2 output is in a tri-state condition 1d = Secondary ASI channel 2 output corresponds to ADC Channel 2 data
4-0	SASI_TX_CH2_SLOT_NUM[4:0]	R/W	0x1	Secondary ASI output channel 2 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^2S, LJ is left slot 15 16d = TDM is slot 16 or I^2S, LJ is right slot 0 17d = TDM is slot 17 or I^2S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is right slot 15

7.3.8 SASI_TX_CH3_CFG Register (Address = 0x20) [Reset = 0x02]

SASI_TX_CH3_CFG is shown in 図 7-195 and described in 表 7-198.

Return to the Summary Table.

This register is the SASI TX Channel 3 configuration register.

図 7-195. SASI_TX_CH3_CFG Register

7	6	5	4	3	2	1	0
RESERVED	SASI_TX_CH3_CFG[1:0]		SASI_TX_CH3_SLOT_NUM[4:0]				
R-0b	R/W-00b		R/W-00010b				

表 7-198. SASI_TX_CH3_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved bit; Write only reset value
6-5	SASI_TX_CH3_CFG[1:0]	R/W	0x0	Secondary ASI output channel 3 configuration. 0d = Secondary ASI channel 3 output is in a tri-state condition 1d = Secondary ASI channel 3 output corresponds to ADC Channel 3 data 2d = Secondary ASI channel 3 output corresponds to VBAT data 3d = Reserved

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表 7-198. SASI_TX_CH3_CFG Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
4-0	SASI_TX_CH3_SLOT_NUM[4:0]	R/W	0x2	Secondary ASI output channel 3 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^2S, LJ is left slot 15 16d = TDM is slot 16 or I^2S, LJ is right slot 0 17d = TDM is slot 17 or I^2S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is right slot 15

7.3.9 SASI_TX_CH4_CFG Register (Address = 0x21) [Reset = 0x03]

SASI_TX_CH4_CFG is shown in 図 7-196 and described in 表 7-199.

Return to the Summary Table.

This register is the SASI TX Channel 4 configuration register.

図 7-196. SASI_TX_CH4_CFG Register

7	6	5	4	3	2	1	0
RESERVED	SASI_TX_CH4_CFG[1:0]		SASI_TX_CH4_SLOT_NUM[4:0]				
R-0b	R/W-00b		R/W-00011b				

表 7-199. SASI_TX_CH4_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved bit; Write only reset value
6-5	SASI_TX_CH4_CFG[1:0]	R/W	0x0	Secondary ASI output channel 4 configuration. 0d = Secondary ASI channel 4 output is in a tri-state condition 1d = Secondary ASI channel 4 output corresponds to ADC Channel 4 data 2d = Secondary ASI channel 4 output corresponds to TEMP data 3d = Reserved
4-0	SASI_TX_CH4_SLOT_NUM[4:0]	R/W	0x3	Secondary ASI output channel 4 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^2S, LJ is left slot 15 16d = TDM is slot 16 or I^2S, LJ is right slot 0 17d = TDM is slot 17 or I^2S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is right slot 15

7.3.10 SASI_TX_CH5_CFG Register (Address = 0x22) [Reset = 0x04]

SASI_TX_CH5_CFG is shown in 図 7-197 and described in 表 7-200.

Return to the Summary Table.

This register is the SASI TX Channel 5 configuration register.

図 7-197. SASI_TX_CH5_CFG Register

7	6	5	4	3	2	1	0
RESERVED	SASI_TX_CH5_CFG[1:0]		SASI_TX_CH5_SLOT_NUM[4:0]				
R-0b	R/W-00b		R/W-00100b				

表 7-200. SASI_TX_CH5_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved bit; Write only reset value
6-5	SASI_TX_CH5_CFG[1:0]	R/W	0x0	Secondary ASI output channel 5 configuration. 0d = Secondary ASI channel 5 output is in a tri-state condition 1d = Secondary ASI channel 5 output corresponds to ASI Input Channel 1 loopback data 2d = Secondary ASI channel 5 output corresponds to echo reference channel 1 data 3d = Reserved
4-0	SASI_TX_CH5_SLOT_NUM[4:0]	R/W	0x4	Secondary ASI output channel 5 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^2S, LJ is left slot 15 16d = TDM is slot 16 or I^2S, LJ is right slot 0 17d = TDM is slot 17 or I^2S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is right slot 15

7.3.11 SASI_TX_CH6_CFG Register (Address = 0x23) [Reset = 0x05]

SASI_TX_CH6_CFG is shown in 図 7-198 and described in 表 7-201.

Return to the Summary Table.

This register is the SASI TX Channel 6 configuration register.

図 7-198. SASI_TX_CH6_CFG Register

7	6	5	4	3	2	1	0
RESERVED	SASI_TX_CH6_CFG[1:0]		SASI_TX_CH6_SLOT_NUM[4:0]				
R-0b	R/W-00b		R/W-00101b				

表 7-201. SASI_TX_CH6_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved bit; Write only reset value
6-5	SASI_TX_CH6_CFG[1:0]	R/W	0x0	Secondary ASI output channel 6 configuration. 0d = Secondary ASI channel 6 output is in a tri-state condition 1d = Secondary ASI channel 6 output corresponds to ASI Input Channel 2 loopback data 2d = Secondary ASI channel 6 output corresponds to echo reference channel 2 data 3d = Reserved
4-0	SASI_TX_CH6_SLOT_NUM[4:0]	R/W	0x5	Secondary ASI output channel 6 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^2S, LJ is left slot 15 16d = TDM is slot 16 or I^2S, LJ is right slot 0 17d = TDM is slot 17 or I^2S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is right slot 15

7.3.12 SASI_TX_CH7_CFG Register (Address = 0x24) [Reset = 0x06]

SASI_TX_CH7_CFG is shown in 図 7-199 and described in 表 7-202.

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This register is the SASI TX Channel 7 configuration register.

図 7-199. SASI_TX_CH7_CFG Register

7	6	5	4	3	2	1	0
RESERVED	SASI_TX_CH7_CFG[1:0]		SASI_TX_CH7_SLOT_NUM[4:0]				
R-0b	R/W-00b		R/W-00110b				

表 7-202. SASI_TX_CH7_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved bit; Write only reset value
6-5	SASI_TX_CH7_CFG[1:0]	R/W	0x0	Secondary ASI output channel 7 configuration. 0d = Secondary ASI channel 7 output is in a tri-state condition 1d = Secondary ASI channel 7 output corresponds to {VBAT_WLby2, TEMP_WLby2} 2d = Secondary ASI channel 7 output corresponds to {echo_ref_ch1_wlby2, echo_ref_ch2_wlby2} 3d = Reserved
4-0	SASI_TX_CH7_SLOT_NUM[4:0]	R/W	0x6	Secondary ASI output channel 7 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^2S, LJ is left slot 15 16d = TDM is slot 16 or I^2S, LJ is right slot 0 17d = TDM is slot 17 or I^2S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is right slot 15

7.3.13 SASI_TX_CH8_CFG Register (Address = 0x25) [Reset = 0x07]

SASI_TX_CH8_CFG is shown in 図 7-200 and described in 表 7-203.

Return to the Summary Table.

This register is the SASI TX Channel 8 configuration register.

図 7-200. SASI_TX_CH8_CFG Register

7	6	5	4	3	2	1	0
RESERVED		SASI_TX_CH8_CFG	SASI_TX_CH8_SLOT_NUM[4:0]				
R-00b		R/W-0b	R/W-00111b				

表 7-203. SASI_TX_CH8_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved bits; Write only reset value
5	SASI_TX_CH8_CFG	R/W	0x0	Secondary ASI output channel 8 configuration. 0d = Secondary ASI channel 8 output is in a tri-state condition 1d = Secondary ASI channel 8 output corresponds to ICLA data
4-0	SASI_TX_CH8_SLOT_NUM[4:0]	R/W	0x7	Secondary ASI output channel 8 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^2S, LJ is left slot 15 16d = TDM is slot 16 or I^2S, LJ is right slot 0 17d = TDM is slot 17 or I^2S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is right slot 15

7.3.14 SASI_RX_CFG0 Register (Address = 0x26) [Reset = 0x00]

SASI_RX_CFG0 is shown in 図 7-201 and described in 表 7-204.

Return to the Summary Table.

This register is the SASI RX configuration register 0.

図 7-201. SASI_RX_CFG0 Register

7	6	5	4	3	2	1	0
SASI_RX_EDGE	SASI_RX_USE_INT_FSYNC	SASI_RX_USE_INT_BCLK	SASI_RX_OFFSET[4:0]				
R/W-0b	R/W-0b	R/W-0b	R/W-00000b				

表 7-204. SASI_RX_CFG0 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SASI_RX_EDGE	R/W	0x0	Secondary ASI data input (on the primary and secondary data pin) receive edge. 0d = Default edge as per the protocol configuration setting in bit 2 (BCLK_POL) 1d = Inverted following edge (half cycle delay) with respect to the default edge setting
6	SASI_RX_USE_INT_FSYNC	R/W	0x0	Secondary ASI uses internal FSYNC for input data latching in controller mode configuration as applicable. 0d = Use external FSYNC for ASI protocol data latching 1d = Use internal FSYNC for ASI protocol data latching
5	SASI_RX_USE_INT_BCLK	R/W	0x0	Secondary ASI uses internal BCLK for input data latching in controller mode configuration. 0d = Use external BCLK for ASI protocol data latching 1d = Use internal BCLK for ASI protocol data latching
4-0	SASI_RX_OFFSET[4:0]	R/W	0x0	Secondary ASI data input MSB slot 0 offset (on the primary and secondary data pin). 0d = ASI data MSB location has no offset and is as per standard protocol 1d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset of one BCLK cycle with respect to standard protocol 2d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset of two BCLK cycles with respect to standard protocol 3d to 30d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset assigned as per configuration 31d = ASI data MSB location (TDM mode is slot 0 or I^2S, LJ mode is the left and right slot 0) offset of 31 BCLK cycles with respect to standard protocol

7.3.15 SASI_RX_CFG1 Register (Address = 0x27) [Reset = 0x00]

SASI_RX_CFG1 is shown in 図 7-202 and described in 表 7-205.

Return to the Summary Table.

This register is the SASI RX configuration register 1.

図 7-202. SASI_RX_CFG1 Register

7	6	5	4	3	2	1	0
SASI_RX_CH8_SEL	SASI_RX_CH7_SEL	SASI_RX_CH6_SEL	SASI_RX_CH5_SEL	SASI_RX_CH4_SEL	SASI_RX_CH3_SEL	SASI_RX_CH2_SEL	SASI_RX_CH1_SEL
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

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表 7-205. SASI_RX_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	SASI_RX_CH8_SEL	R/W	0x0	Secondary ASI input channel 8 select. 0d = Secondary ASI channel 8 input is on DIN 1d = Secondary ASI channel 8 input is on DIN2
6	SASI_RX_CH7_SEL	R/W	0x0	Secondary ASI input channel 7 select. 0d = Secondary ASI channel 7 input is on DIN 1d = Secondary ASI channel 7 input is on DIN2
5	SASI_RX_CH6_SEL	R/W	0x0	Secondary ASI input channel 6 select. 0d = Secondary ASI channel 6 input is on DIN 1d = Secondary ASI channel 6 input is on DIN2
4	SASI_RX_CH5_SEL	R/W	0x0	Secondary ASI input channel 5 select. 0d = Secondary ASI channel 5 input is on DIN 1d = Secondary ASI channel 5 input is on DIN2
3	SASI_RX_CH4_SEL	R/W	0x0	Secondary ASI input channel 4 select. 0d = Secondary ASI channel 4 input is on DIN 1d = Secondary ASI channel 4 input is on DIN2
2	SASI_RX_CH3_SEL	R/W	0x0	Secondary ASI input channel 3 select. 0d = Secondary ASI channel 3 input is on DIN 1d = Secondary ASI channel 3 input is on DIN2
1	SASI_RX_CH2_SEL	R/W	0x0	Secondary ASI input channel 2 select. 0d = Secondary ASI channel 2 input is on DIN 1d = Secondary ASI channel 2 input is on DIN2
0	SASI_RX_CH1_SEL	R/W	0x0	Secondary ASI input channel 1 select. 0d = Secondary ASI channel 1 input is on DIN 1d = Secondary ASI channel 1 input is on DIN2

7.3.16 SASI_RX_CH1_CFG Register (Address = 0x28) [Reset = 0x00]

SASI_RX_CH1_CFG is shown in 図 7-203 and described in 表 7-206.

Return to the Summary Table.

This register is the SASI RX Channel 1 configuration register.

図 7-203. SASI_RX_CH1_CFG Register

7	6	5	4	3	2	1	0
RESERVED		SASI_RX_CH1_CFG	SASI_RX_CH1_SLOT_NUM[4:0]				
R-00b		R/W-0b	R/W-00000b				

表 7-206. SASI_RX_CH1_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved bits; Write only reset value
5	SASI_RX_CH1_CFG	R/W	0x0	Secondary ASI input channel 1 configuration. 0d = Secondary ASI channel 1 input is disabled 1d = Secondary ASI channel 1 input corresponds to DAC Channel 1 data
4-0	SASI_RX_CH1_SLOT_NUM[4:0]	R/W	0x0	Secondary ASI input channel 1 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^2S, LJ is left slot 15 16d = TDM is slot 16 or I^2S, LJ is right slot 0 17d = TDM is slot 17 or I^2S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is right slot 15

7.3.17 SASI_RX_CH2_CFG Register (Address = 0x29) [Reset = 0x01]

SASI_RX_CH2_CFG is shown in 図 7-204 and described in 表 7-207.

Return to the Summary Table.

This register is the SASI RX Channel 2 configuration register.

図 7-204. SASI_RX_CH2_CFG Register

7	6	5	4	3	2	1	0
RESERVED		SASI_RX_CH2_CFG	SASI_RX_CH2_SLOT_NUM[4:0]				
R-00b		R/W-0b	R/W-00001b				

表 7-207. SASI_RX_CH2_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved bits; Write only reset value
5	SASI_RX_CH2_CFG	R/W	0x0	Secondary ASI input channel 2 configuration. 0d = Secondary ASI channel 2 input is disabled 1d = Secondary ASI channel 2 input corresponds to DAC Channel 2 data
4-0	SASI_RX_CH2_SLOT_NUM[4:0]	R/W	0x1	Secondary ASI input channel 2 slot assignment. 0d = TDM is slot 0 or I^{2}S, LJ is left slot 0 1d = TDM is slot 1 or I^{2}S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^{2}S, LJ is left slot 15 16d = TDM is slot 16 or I^{2}S, LJ is right slot 0 17d = TDM is slot 17 or I^{2}S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^{2}S, LJ is right slot 15

7.3.18 SASI_RX_CH3_CFG Register (Address = 0x2A) [Reset = 0x02]

SASI_RX_CH3_CFG is shown in 図 7-205 and described in 表 7-208.

Return to the Summary Table.

This register is the SASI RX Channel 3 configuration register.

図 7-205. SASI_RX_CH3_CFG Register

7	6	5	4	3	2	1	0
RESERVED		SASI_RX_CH3_CFG	SASI_RX_CH3_SLOT_NUM[4:0]				
R-00b		R/W-0b	R/W-00010b				

表 7-208. SASI_RX_CH3_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved bits; Write only reset value
5	SASI_RX_CH3_CFG	R/W	0x0	Secondary ASI input channel 3 configuration. 0d = Secondary ASI channel 3 input is disabled 1d = Secondary ASI channel 3 input corresponds to DAC Channel 3 data

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表 7-208. SASI_RX_CH3_CFG Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
4-0	SASI_RX_CH3_SLOT_NUM[4:0]	R/W	0x2	Secondary ASI input channel 3 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^2S, LJ is left slot 15 16d = TDM is slot 16 or I^2S, LJ is right slot 0 17d = TDM is slot 17 or I^2S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is right slot 15

7.3.19 SASI_RX_CH4_CFG Register (Address = 0x2B) [Reset = 0x03]

SASI_RX_CH4_CFG is shown in 図 7-206 and described in 表 7-209.

Return to the Summary Table.

This register is the SASI RX Channel 4 configuration register.

図 7-206. SASI_RX_CH4_CFG Register

7	6	5	4	3	2	1	0
RESERVED		SASI_RX_CH4_CFG	SASI_RX_CH4_SLOT_NUM[4:0]				
R-00b		R/W-0b	R/W-00011b				

表 7-209. SASI_RX_CH4_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved bits; Write only reset value
5	SASI_RX_CH4_CFG	R/W	0x0	Secondary ASI input channel 4 configuration. 0d = Secondary ASI channel 4 input is disabled 1d = Secondary ASI channel 4 input corresponds to DAC Channel 4 data
4-0	SASI_RX_CH4_SLOT_NUM[4:0]	R/W	0x3	Secondary ASI input channel 4 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^2S, LJ is left slot 15 16d = TDM is slot 16 or I^2S, LJ is right slot 0 17d = TDM is slot 17 or I^2S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is right slot 15

7.3.20 SASI_RX_CH5_CFG Register (Address = 0x2C) [Reset = 0x04]

SASI_RX_CH5_CFG is shown in 図 7-207 and described in 表 7-210.

Return to the Summary Table.

This register is the SASI RX Channel 5 configuration register.

図 7-207. SASI_RX_CH5_CFG Register

7	6	5	4	3	2	1	0
RESERVED	SASI_RX_CH5_CFG[1:0]		SASI_RX_CH5_SLOT_NUM[4:0]				
R-0b	R/W-00b		R/W-00100b				

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表 7-210. SASI_RX_CH5_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved bit; Write only reset value
6-5	SASI_RX_CH5_CFG[1:0]	R/W	0x0	Secondary ASI input channel 5 configuration. 0d = Secondary ASI channel 5 input is disabled 1d = Secondary ASI channel 5 input corresponds to DAC Channel 5 data 2d = Secondary ASI channel 5 input corresponds to ADC Channel 1 output loopback 3d = Reserved
4-0	SASI_RX_CH5_SLOT_NUM[4:0]	R/W	0x4	Secondary ASI input channel 5 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^2S, LJ is left slot 15 16d = TDM is slot 16 or I^2S, LJ is right slot 0 17d = TDM is slot 17 or I^2S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is right slot 15

7.3.21 SASI_RX_CH6_CFG Register (Address = 0x2D) [Reset = 0x05]

SASI_RX_CH6_CFG is shown in 図 7-208 and described in 表 7-211.

Return to the Summary Table.

This register is the SASI RX Channel 6 configuration register.

図 7-208. SASI_RX_CH6_CFG Register

7	6	5	4	3	2	1	0
RESERVED	SASI_RX_CH6_CFG[1:0]		SASI_RX_CH6_SLOT_NUM[4:0]				
R-0b	R/W-00b		R/W-00101b				

表 7-211. SASI_RX_CH6_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved bit; Write only reset value
6-5	SASI_RX_CH6_CFG[1:0]	R/W	0x0	Secondary ASI input channel 6 configuration. 0d = Secondary ASI channel 6 input is disabled 1d = Secondary ASI channel 6 input corresponds to DAC Channel 6 data 2d = Secondary ASI channel 6 input corresponds to ADC Channel 2 output loopback 3d = Secondary ASI channel 6 input corresponds to ICLA device 1 data
4-0	SASI_RX_CH6_SLOT_NUM[4:0]	R/W	0x5	Secondary ASI input channel 6 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^2S, LJ is left slot 15 16d = TDM is slot 16 or I^2S, LJ is right slot 0 17d = TDM is slot 17 or I^2S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is right slot 15

7.3.22 SASI_RX_CH7_CFG Register (Address = 0x2E) [Reset = 0x06]

SASI_RX_CH7_CFG is shown in 図 7-209 and described in 表 7-212.

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This register is the SASI RX Channel 7 configuration register.

図 7-209. SASI_RX_CH7_CFG Register

7	6	5	4	3	2	1	0
RESERVED	SASI_RX_CH7_CFG[1:0]		SASI_RX_CH7_SLOT_NUM[4:0]				
R-0b	R/W-00b		R/W-00110b				

表 7-212. SASI_RX_CH7_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved bit; Write only reset value
6-5	SASI_RX_CH7_CFG[1:0]	R/W	0x0	Secondary ASI input channel 7 configuration. 0d = Secondary ASI channel 7 input is disabled 1d = Secondary ASI channel 7 input corresponds to DAC Channel 7 data 2d = Secondary ASI channel 7 input corresponds to ADC Channel 3 output loopback 3d = Secondary ASI channel 7 input corresponds to ICLA device 2 data
4-0	SASI_RX_CH7_SLOT_NUM[4:0]	R/W	0x6	Secondary ASI input channel 7 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^2S, LJ is left slot 15 16d = TDM is slot 16 or I^2S, LJ is right slot 0 17d = TDM is slot 17 or I^2S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is right slot 15

7.3.23 SASI_RX_CH8_CFG Register (Address = 0x2F) [Reset = 0x07]

SASI_RX_CH8_CFG is shown in 図 7-210 and described in 表 7-213.

Return to the Summary Table.

This register is the SASI RX Channel 8 configuration register.

図 7-210. SASI_RX_CH8_CFG Register

7	6	5	4	3	2	1	0
RESERVED	SASI_RX_CH8_CFG[1:0]		SASI_RX_CH8_SLOT_NUM[4:0]				
R-0b	R/W-00b		R/W-00111b				

表 7-213. SASI_RX_CH8_CFG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved bit; Write only reset value
6-5	SASI_RX_CH8_CFG[1:0]	R/W	0x0	Secondary ASI input channel 8 configuration. 0d = Secondary ASI channel 8 input is disabled 1d = Secondary ASI channel 8 input corresponds to DAC Channel 8 data 2d = Secondary ASI channel 8 input corresponds to ADC Channel 4 output loopback 3d = Secondary ASI channel 8 input corresponds to ICLA device 3 data

表 7-213. SASI_RX_CH8_CFG Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
4-0	SASI_RX_CH8_SLOT_NUM[4:0]	R/W	0x7	Secondary ASI input channel 8 slot assignment. 0d = TDM is slot 0 or I^2S, LJ is left slot 0 1d = TDM is slot 1 or I^2S, LJ is left slot 1 2d to 14d = Slot assigned as per configuration 15d = TDM is slot 15 or I^2S, LJ is left slot 15 16d = TDM is slot 16 or I^2S, LJ is right slot 0 17d = TDM is slot 17 or I^2S, LJ is right slot 1 18d to 30d = Slot assigned as per configuration 31d = TDM is slot 31 or I^2S, LJ is right slot 15

7.3.24 CLK_CFG12 Register (Address = 0x32) [Reset = 0x00]

CLK_CFG12 is shown in 図 7-211 and described in 表 7-214.

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This register is the clock configuration register 12.

図 7-211. CLK_CFG12 Register

7	6	5	4	3	2	1	0
PDIV_CLKSRC_SEL[1:0]		PASI_BCLK_DIV_CLK_SEL[2:0]			RESERVED		
R/W-00b		R/W-000b			R-000b		

表 7-214. CLK_CFG12 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	PDIV_CLKSRC_SEL[1:0]	R/W	0x0	Source clock selection for PLL PDIV Divider. 0d = PLL_PDIV_IN_CLK is Primary ASI BCLK 1d = PLL_PDIV_IN_CLK is Secondary ASI BCLK 2d = PLL_PDIV_IN_CLK is CCLK 3d = PLL_PDIV_IN_CLK is internal Oscillator Clock
5-3	PASI_BCLK_DIV_CLK_SEL[2:0]	R/W	0x0	Primary ASI BCLK divider clock source selection. 0d = Primary ASI BCLK divider clock source is PLL output 1d = Reserved 2d = Primary ASI BCLK divider clock source is secondary ASI BCLK 3d = Primary ASI BCLK divider clock source is CCLK 4d = Primary ASI BCLK divider clock source is internal oscillator clock 5d = Primary ASI BCLK divider clock source is DSP clock 6d to 7d = Reserved
2-0	RESERVED	R	0x0	Reserved bits; Write only reset value

7.3.25 CLK_CFG13 Register (Address = 0x33) [Reset = 0x00]

CLK_CFG13 is shown in 図 7-212 and described in 表 7-215.

Return to the Summary Table.

図 7-212. CLK_CFG13 Register

7	6	5	4	3	2	1	0
RESERVED	SASI_BCLK_DIV_CLK_SEL[2:0]			RESERVED			
R-0b	R/W-000b			R-0000b			

表 7-215. CLK_CFG13 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved bit; Write only reset value

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表 7-215. CLK_CFG13 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
6-4	SASI_BCLK_DIV_CLK_SEL[2:0]	R/W	0x0	Secondaary ASI BCLK divider clock source selection. 0d = Secondaary ASI BCLK divider clock source is PLL output 1d = Secondaary ASI BCLK divider clock source is primary ASI BCLK 2d = Reserved 3d = Secondaary ASI BCLK divider clock source is CCLK 4d = Secondaary ASI BCLK divider clock source is internal oscillator clock 5d = Secondaary ASI BCLK divider clock source is DSP clock 6d to 7d = Reserved
3-0	RESERVED	R	0x0	Reserved bits; Write only reset value

7.3.26 CLK_CFG14 Register (Address = 0x34) [Reset = 0x10]

CLK_CFG14 is shown in 図 7-213 and described in 表 7-216.

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This register is the clock configuration register 14.

図 7-213. CLK_CFG14 Register

7	6	5	4	3	2	1	0
DIG_NM_DIV_CLK_SRC_SEL[1:0]		ANA_NM_DIV_CLK_SRC_SEL[1:0]		RESERVED		RESERVED	
R/W-00b		R/W-01b		R-00b		R-00b	

表 7-216. CLK_CFG14 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	DIG_NM_DIV_CLK_SRC_SEL[1:0]	R/W	0x0	Source clock selection for DIG NMDIV CLK clock. 0d = DIG NM divider input clock is Primary ASI BCLK 1d = DIG NM divider input clock is Secondary ASI BCLK 2d = DIG NM divider input clock is CCLK 3d = DIG NM divider input clock is internal oscillator clock
5-4	ANA_NM_DIV_CLK_SRC_SEL[1:0]	R/W	0x1	Source clock selection for NMDIV CLK clock. 0d = NM divider input clock is PLL Output 1d = NM divider input clock is PLL Output 2d = NM divider input clock is DIG NM Divider Clock Source 3d = NM divider input clock is Primary ASI BCLK (Low Jitter Path)
3-2	RESERVED	R	0x0	Reserved bits; Write only reset values
1-0	RESERVED	R	0x0	Reserved bits; Write only reset values

7.3.27 CLK_CFG15 Register (Address = 0x35) [Reset = 0x01]

CLK_CFG15 is shown in 図 7-214 and described in 表 7-217.

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This register is the clock configuration register 15.

図 7-214. CLK_CFG15 Register

7	6	5	4	3	2	1	0
PLL_PDIV[7:0]							
R/W-00000001b							

表 7-217. CLK_CFG15 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL_PDIV[7:0]	R/W	0x1	PLL pre-scaler P-divider value (Don't care when auto detection is enabled) 0d = PLL PDIV value is 256 1d = PLL PDIV value is 1 2d = PLL PDIV value is 2 3d to 254d = PLL PDIV value is as per configuration 255d = PLL PDIV value is 255

7.3.28 CLK_CFG16 Register (Address = 0x36) [Reset = 0x00]

CLK_CFG16 is shown in 図 7-215 and described in 表 7-218.

Return to the Summary Table.

This register is the clock configuration register 16.

図 7-215. CLK_CFG16 Register

7	6	5	4	3	2	1	0
PLL_JMUL_MSB	PLL_DIV_CLK_DIG_BY_2	PLL_DMUL_MSB[5:0]					
R/W-0b	R/W-0b	R/W-000000b					

表 7-218. CLK_CFG16 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	PLL_JMUL_MSB	R/W	0x0	PLL integer portion J-multiplier value MSB bit. (Don't care when auto detection is enabled)
6	PLL_DIV_CLK_DIG_BY_2	R/W	0x0	PLL DIV clock divide by 2 configuration 0d = No divide/2 inside PLL 1d = PLL does a divide/2
5-0	PLL_DMUL_MSB[5:0]	R/W	0x0	PLL fractional portion D-multiplier value MSB bits. (Don't care when auto detection is enabled)

7.3.29 CLK_CFG17 Register (Address = 0x37) [Reset = 0x00]

CLK_CFG17 is shown in 図 7-216 and described in 表 7-219.

Return to the Summary Table.

This register is the clock configuration register 17.

図 7-216. CLK_CFG17 Register

7	6	5	4	3	2	1	0
PLL_DMUL_LSB[7:0]							
R/W-00000000b							

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表 7-219. CLK_CFG17 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL_DMUL_LSB[7:0]	R/W	0x0	PLL fractional portion D-multiplier value LSB byte. Above D-multiplier value MSB bits (PLL_DMUL_MSB) along with this LSB byte (PLL_DMUL_LSB) is concatenated to determine final D-multiplier value. (Don't care when auto detection is enabled) 0d = PLL DMUL value is 0 1d = PLL DMUL value is 1 2d = PLL DMUL value is 2 3d to 9998d = PLL JMUL value is as per configuration 9999d = PLL JMUL value is 9999 10000d to 16383d = Reserved; Don't use

7.3.30 CLK_CFG18 Register (Address = 0x38) [Reset = 0x08]

CLK_CFG18 is shown in 図 7-217 and described in 表 7-220.

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This register is the clock configuration register 18.

図 7-217. CLK_CFG18 Register

7	6	5	4	3	2	1	0
PLL_JMUL_LSB[7:0]							
R/W-00001000b							

表 7-220. CLK_CFG18 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PLL_JMUL_LSB[7:0]	R/W	0x8	PLL integer portion J-multiplier value LSB byte. Above J-multiplier value MSB bit (PLL_JMUL_MSB) along with this LSB byte (PLL_JMUL_LSB) is concatenated to determine fianl J-multiplier value. (Don't care when auto detection is enabled) 0d = Reserved; Don't use 1d = PLL JMUL value is 1 2d = PLL JMUL value is 2 3d to 510d = PLL JMUL value is as per configuration 511d = PLL JMUL value is 511

7.3.31 CLK_CFG19 Register (Address = 0x39) [Reset = 0x20]

CLK_CFG19 is shown in 図 7-218 and described in 表 7-221.

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This register is the clock configuration register 19.

図 7-218. CLK_CFG19 Register

7	6	5	4	3	2	1	0
NDIV[2:0]			PDM_DIV[2:0]			RESERVED	
R/W-001b			R/W-000b			R-00b	

表 7-221. CLK_CFG19 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	NDIV[2:0]	R/W	0x1	NDIV divider value. (Don't care when auto detection is enabled) 0d = NDIV value is 8 1d = NDIV value is 1 2d = NDIV value is 2 3d to 6d = NDIV value is as per configuration 7d = NDIV value is 7
4-2	PDM_DIV[2:0]	R/W	0x0	PDM divider value. (Don't care when auto detection is enabled) 0d = PDM_DIV value is 1 1d = PDM_DIV value is 2 2d = PDM_DIV value is 4 3d = PDM_DIV value is 8 4d = PDM_DIV value is 16 5d-7d Reserved
1-0	RESERVED	R	0x0	Reserved bits; Write only reset values

7.3.32 CLK_CFG20 Register (Address = 0x3A) [Reset = 0x04]

CLK_CFG20 is shown in 図 7-219 and described in 表 7-222.

Return to the Summary Table.

This register is the clock configuration register 20.

図 7-219. CLK_CFG20 Register

7	6	5	4	3	2	1	0
MDIV[5:0]						DIG_ADC_MODCLK_DIV[1:0]	
R/W-000001b						R/W-00b	

表 7-222. CLK_CFG20 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	MDIV[5:0]	R/W	0x1	MDIV divider value. (Don't care when auto detection is enabled) 0d = MDIV value is 64 1d = MDIV value is 1 2d = MDIV value is 2 3d to 62d = MDIV value is as per configuration 63d = MDIV value is 63
1-0	DIG_ADC_MODCLK_DIV[1:0]	R/W	0x0	ADC modulator clock divider value. (Don't care when auto detection is enabled) 0d = DIG_ADC_MODCLK_DIV value is 1 1d = DIG_ADC_MODCLK_DIV value is 2 2d = DIG_ADC_MODCLK_DIV value is 4 3d = Reserved

7.3.33 CLK_CFG21 Register (Address = 0x3B) [Reset = 0x00]

CLK_CFG21 is shown in 図 7-220 and described in 表 7-223.

Return to the Summary Table.

This register is the clock configuration register 21.

図 7-220. CLK_CFG21 Register

7	6	5	4	3	2	1	0
RESERVED		DIG_DAC_MODCLK_DIV[1:0]		RESERVED	PASI_BDIV_MSB	SASI_BDIV_MSB	RESERVED
R-00b		R/W-00b		R-0b	R/W-0b	R/W-0b	R-0b

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図 7-220. CLK_CFG21 Register (続き)

表 7-223. CLK_CFG21 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved bits; Write only reset values
5-4	DIG_DAC_MODCLK_DIV[1:0]	R/W	0x0	DAC modulator clock divider value. (Don't care when auto detection is enabled) 0d = DIG_DAC_MODCLK_DIV value is 1 1d = DIG_DAC_MODCLK_DIV value is 2 2d = DIG_DAC_MODCLK_DIV value is 4 3d = Reserved
3	RESERVED	R	0x0	Reserved bit; Write only reset value
2	PASI_BDIV_MSB	R/W	0x0	Primary ASI BCLK divider value MSB bit. (Don't care when auto detection is enabled)
1	SASI_BDIV_MSB	R/W	0x0	Secondary ASI BCLK divider value MSB bit. (Don't care when auto detection is enabled)
0	RESERVED	R	0x0	Reserved bit; Write only reset value

7.3.34 CLK_CFG22 Register (Address = 0x3C) [Reset = 0x01]

CLK_CFG22 is shown in 図 7-221 and described in 表 7-224.

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This register is the clock configuration register 18.

図 7-221. CLK_CFG22 Register

7	6	5	4	3	2	1	0
PASI_BDIV_LSB[7:0]							
R/W-00000001b							

表 7-224. CLK_CFG22 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	PASI_BDIV_LSB[7:0]	R/W	0x1	Secondary ASI BCLK divider value. (Don't care when auto detection is enabled) 0d = SASI BCLK divider value is 512 1d = SASI BCLK divider value is 1 2d = SASI BCLK divider value is 2 3d to 62d = SASI BCLK divider value is as per configuration 63d = SASI BCLK divider value is 511

7.3.35 CLK_CFG23 Register (Address = 0x3D) [Reset = 0x01]

CLK_CFG23 is shown in 図 7-222 and described in 表 7-225.

Return to the Summary Table.

This register is the clock configuration register 18.

図 7-222. CLK_CFG23 Register

7	6	5	4	3	2	1	0
SASI_BDIV_LSB[7:0]							
R/W-00000001b							

表 7-225. CLK_CFG23 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	SASI_BDIV_LSB[7:0]	R/W	0x1	Secondary ASI BCLK divider value. (Don't care when auto detection is enabled) 0d = SASI BCLK divider value is 512 1d = SASI BCLK divider value is 1 2d = SASI BCLK divider value is 2 3d to 62d = SASI BCLK divider value is as per configuration 63d = SASI BCLK divider value is 511

7.3.36 CLK_CFG24 Register (Address = 0x3E) [Reset = 0x01]

CLK_CFG24 is shown in 図 7-223 and described in 表 7-226.

Return to the Summary Table.

This register is the clock configuration register 21.

図 7-223. CLK_CFG24 Register

7	6	5	4	3	2	1	0
RESERVED		ANA_NM_DIV[5:0]					
R-00b		R/W-000001b					

表 7-226. CLK_CFG24 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	RESERVED	R	0x0	Reserved bits; Write only reset value
5-0	ANA_NM_DIV[5:0]	R/W	0x1	Analog N-M DIV divider value. (Don't care when auto detection is enabled) 0d = ANA_NM_DIV value is 64 1d = ANA_NM_DIV value is 1 2d = ANA_NM_DIV value is 2 3d to 62d = ANA_NM_DIV value is as per configuration 63d = NDIV value is 63

7.3.37 CLK_CFG30 Register (Address = 0x44) [Reset = 0x00]

CLK_CFG30 is shown in 図 7-224 and described in 表 7-227.

Return to the Summary Table.

図 7-224. CLK_CFG30 Register

7	6	5	4	3	2	1	0
RESERVED					NDIV_EN	MDIV_EN	PDM_DIV_EN
R-00000b					R/W-0b	R/W-0b	R/W-0b

表 7-227. CLK_CFG30 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0x0	Reserved bits; Write only reset value
2	NDIV_EN	R/W	0x0	NDIV divider enable 0d = divider disabled 1d = divider enabled
1	MDIV_EN	R/W	0x0	MDIV divider enable 0d = divider disabled 1d = divider enabled

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表 7-227. CLK_CFG30 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
0	PDM_DIV_EN	R/W	0x0	PDM divider enable 0d = divider disabled 1d = divider enabled

7.3.38 CLK_CFG31 Register (Address = 0x45) [Reset = 0x00]

CLK_CFG31 is shown in 図 7-225 and described in 表 7-228.

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図 7-225. CLK_CFG31 Register

7	6	5	4	3	2	1	0
DIG_ADC_DEM_DIV_EN	DIG_ADC_MODCLK_DIV_EN	DIG_DAC_DEM_DIV_EN	DIG_DAC_MODCLK_DIV_EN	PASI_BDIV_EN	SASI_BDIV_EN	PASI_FSYNC_DIV_EN	SASI_FSYNC_DIV_EN
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 7-228. CLK_CFG31 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	DIG_ADC_DEM_DIV_EN	R/W	0x0	ADC DEM divider enable 0d = divider disabled 1d = divider enabled
6	DIG_ADC_MODCLK_DIV_EN	R/W	0x0	ADC MODCLK divider enable 0d = divider disabled 1d = divider enabled
5	DIG_DAC_DEM_DIV_EN	R/W	0x0	DAC DEM divider enable 0d = divider disabled 1d = divider enabled
4	DIG_DAC_MODCLK_DIV_EN	R/W	0x0	DAC MODCLK divider enable 0d = divider disabled 1d = divider enabled
3	PASI_BDIV_EN	R/W	0x0	PASI BDIV divider enable 0d = divider disabled 1d = divider enabled
2	SASI_BDIV_EN	R/W	0x0	SASI BDIV divider enable 0d = divider disabled 1d = divider enabled
1	PASI_FSYNC_DIV_EN	R/W	0x0	PASI FSYNC DIV divider enable 0d = divider disabled 1d = divider enabled
0	SASI_FSYNC_DIV_EN	R/W	0x0	SASI FSYNC DIV divider enable 0d = divider disabled 1d = divider enabled

7.3.39 CLKOUT_CFG1 Register (Address = 0x46) [Reset = 0x00]

CLKOUT_CFG1 is shown in 図 7-226 and described in 表 7-229.

Return to the Summary Table.

This register is the CLKOUT configuration register 1.

図 7-226. CLKOUT_CFG1 Register

7	6	5	4	3	2	1	0
RESERVED					CLKOUT_CLK_SEL[2:0]		

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図 7-226. CLKOUT_CFG1 Register (続き)

R-00000b	R/W-000b

表 7-229. CLKOUT_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-3	RESERVED	R	0x0	Reserved bits; Write only reset value
2-0	CLKOUT_CLK_SEL[2:0]	R/W	0x0	General Purpose CLKOUT divider clock source selection. 0d = Source clock is PLL output 1d = Source clock is primary ASI BCLK 2d = Source clock is secondary ASI BCLK 3d = Source clock is CCLK 4d = Source clock is internal oscillator clock 5d = Source clock is DSP clock 6d to 7d = Reserved

7.3.40 CLKOUT_CFG2 Register (Address = 0x47) [Reset = 0x01]

CLKOUT_CFG2 is shown in 図 7-227 and described in 表 7-230.

Return to the Summary Table.

This register is the CLKOUT configuration register 2.

図 7-227. CLKOUT_CFG2 Register

7	6	5	4	3	2	1	0
CLKOUT_DIV_EN	CLKOUT_DIV[6:0]						
R/W-0b	R/W-0000001b						

表 7-230. CLKOUT_CFG2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CLKOUT_DIV_EN	R/W	0x0	CLKOUT divider enable. 0d = CLKOUT divider disabled 1d = CLKOUT divider enabled
6-0	CLKOUT_DIV[6:0]	R/W	0x1	CLKOUT DIV divider value. 0d = CLKOUT_DIV value is 128 1d = CLKOUT_DIV value is 1 2d = CLKOUT_DIV value is 2 3d to 126d = CLKOUT_DIV value is as per configuration 127d = CLKOUT_DIV value is 127

7.3.41 BSTCLK_CFG1 Register (Address = 0x48) [Reset = 0x00]

BSTCLK_CFG1 is shown in 図 7-228 and described in 表 7-231.

Return to the Summary Table.

This register is the Boost clock configuration register 1

図 7-228. BSTCLK_CFG1 Register

7	6	5	4	3	2	1	0
RESERVED	BST_CLK_FREQ_SEL	BST_CLK_SRC_AUTO_DIS	BST_CLK_SRC_MANUAL_SEL	BST_CLK_EN_AUTO_DIS	BST_CLK_MANUAL_EN	BST_CLK_MANUAL_DIV[1:0]	
R-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-00b	

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表 7-231. BSTCLK_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0x0	Reserved bit; Write only reset value
6	BST_CLK_FREQ_SEL	R/W	0x0	Boost clock frequency mode 0d = Boost clock frequency is ~6MHz 1d = Boost clock frequency is ~3MHz
5	BST_CLK_SRC_AUTO_DIS	R/W	0x0	Boost divider source clock auto selection disable 0d = Boost divider source clock auto-selection based on clock detection scheme 1d = Boost divider source clock auto-selection disabled and selected based on BST_CLK_SRC_SEL
4	BST_CLK_SRC_MANUAL_SEL	R/W	0x0	Boost clock source manual selection (don't care in auto mode) 0d = Boost clock generated based on Audio clock available for ADC/DAC 1d = Boost clock generated based on internal oscillator clock
3	BST_CLK_EN_AUTO_DIS	R/W	0x0	Boost divider source clock auto selection disable 0d = Boost divider auto-enabled 1d = Boost divider enabled/disabled based on manual control using BST_CLK_MANUAL_EN
2	BST_CLK_MANUAL_EN	R/W	0x0	Boost divider manual enable (don't care in auto mode) 0d = Boost divider disabled 1d = Boost divider enabled
1-0	BST_CLK_MANUAL_DIV[1:0]	R/W	0x0	Boost divider value (don't care in auto mode) 0d = Boost divider value is 1 1d = Boost divider value is 2 2d = Boost divider value is 4 3d = Boost divider value is 8

7.3.42 SARCLK_CFG1 Register (Address = 0x49) [Reset = 0x00]

SARCLK_CFG1 is shown in 図 7-229 and described in 表 7-232.

Return to the Summary Table.

This register is the SAR clock configuration register 1

図 7-229. SARCLK_CFG1 Register

7	6	5	4	3	2	1	0
SAR_CLK_FREQ_SEL[1:0]		SAR_CLK_SRC_AUTO_DIS	SAR_CLK_SRC_MANUAL_SEL	SAR_CLK_EN_AUTO_DIS	SAR_CLK_MANUAL_EN	SAR_CLK_MANUAL_DIV[1:0]	
R/W-00b		R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-00b	

表 7-232. SARCLK_CFG1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-6	SAR_CLK_FREQ_SEL[1:0]	R/W	0x0	SAR clock frequency mode 0d = SAR clock frequency is ~6MHz 1d = SAR clock frequency is ~3MHz 2d = SAR clock frequency is ~1.5MHz 3d = SAR clock frequency is ~12MHz (valid only when SAR clock is generated directly using internal oscilator clock
5	SAR_CLK_SRC_AUTO_DIS	R/W	0x0	SAR divider source clock auto selection disable 0d = SAR divider source clock auto-selection based on clock detection scheme 1d = SAR divider source clock auto-selection disabled and selected based on BST_CLK_SRC_SEL
4	SAR_CLK_SRC_MANUAL_SEL	R/W	0x0	SAR clock source manual selection (don't care in auto mode) 0d = SAR clock generated based on Audio clock available for ADC/DAC 1d = SAR clock generated based on internal oscillator clock

表 7-232. SARCLK_CFG1 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
3	SAR_CLK_EN_AUTO_DIS	R/W	0x0	SAR divider source clock auto selection disable 0d = SAR divider auto-enabled 1d = SAR divider enabled/disabled based on manual control using BST_CLK_EN
2	SAR_CLK_MANUAL_EN	R/W	0x0	SAR divider manual enable (don't care in auto mode) 0d = SAR divider disabled 1d = SAR divider enabled
1-0	SAR_CLK_MANUAL_DIV[1:0]	R/W	0x0	SAR divider value (don't care in auto mode) 0d = SAR divider value is 1 1d = SAR divider value is 2 2d = SAR divider value is 4 3d = SAR divider value is 8

7.3.43 ADC_OVRLD_FLAG Register (Address = 0x5B) [Reset = 0x00]

ADC_OVRLD_FLAG is shown in 図 7-230 and described in 表 7-233.

Return to the Summary Table.

図 7-230. ADC_OVRLD_FLAG Register

7	6	5	4	3	2	1	0
ADC_CH1_OVRLD_LTCH	ADC_CH2_OVRLD_LTCH	ADC_CH1_OVRLD_LIVE	ADC_CH2_OVRLD_LIVE	RESERVED			
R-0b	R-0b	R-0b	R-0b	R-0000b			

表 7-233. ADC_OVRLD_FLAG Register Field Descriptions

Bit	Field	Type	Reset	Description
7	ADC_CH1_OVRLD_LTCH	R	0x0	ADC CH1 OVRLD fault (self clearing bit). 0b = No ADC CH1 OVRLD fault 1b = ADC CH1 OVRLD fault
6	ADC_CH2_OVRLD_LTCH	R	0x0	ADC CH2 OVRLD fault (self clearing bit). 0b = No ADC CH2 OVRLD fault 1b = ADC CH2 OVRLD fault
5	ADC_CH1_OVRLD_LIVE	R	0x0	ADC CH1 OVRLD fault (self clearing bit). 0b = No ADC CH1 OVRLD fault 1b = ADC CH1 OVRLD fault
4	ADC_CH2_OVRLD_LIVE	R	0x0	ADC CH2 OVRLD fault (self clearing bit). 0b = No ADC CH2 OVRLD fault 1b = ADC CH2 OVRLD fault
3-0	RESERVED	R	0x0	Reserved bits; Write only reset value

ADVANCE INFORMATION

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8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TAC5312-Q1 is a stereo, high-performance audio codec that supports sample rates of up to 768 kHz. The device supports up to a total of 4 microphones for simultaneous recording which can be selected from up to 2 analog microphones or 4 digital pulse density modulation (PDM) microphones. The device also supports up to 4 channel simultaneous playback which can be configured as a 2 channel differential or psuedo differential output or up to 4 channel single-ended output with options for headphone and lineout drive capabilities.

Communication to the TAC5312-Q1 for configuration of the control registers is supported using an I^2C or SPI interface. The device supports a highly flexible, audio serial interface (TDM, I^2S, and LJ) to transmit audio data seamlessly in the system across devices.

8.2 Typical Application

8.2.1 Application

図 8-1 shows a typical configuration of the TAC5312-Q1 for an application using two analog ECM microphones for simultaneous recording and two channel lineout operation with an I^2C control interface and a time-division multiplexing (TDM) audio data target interface. For best distortion performance, use input AC-coupling capacitors with a low-voltage coefficient.

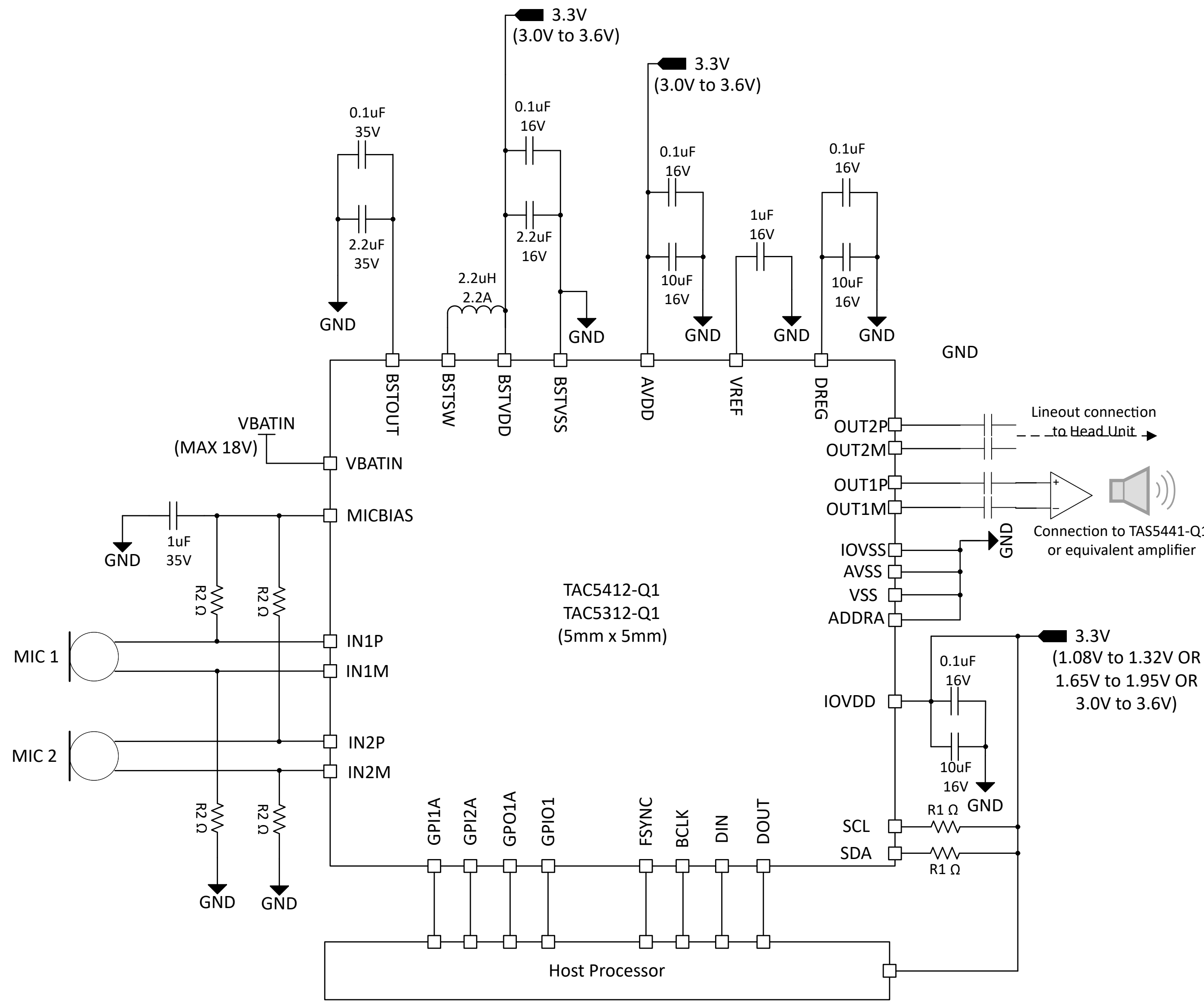

図 8-1. Stereo Microphone with Stereo Lineout Block Diagram

8.2.2 Design Requirements

表 8-1 lists the design parameters for this application.

表 8-1. Design Parameters

PARAMETER	VALUE
AVDD	3.3V
BSTVDD	3.3V
IOVDD	1.2V or 1.8V or 3.3V
AVDD supply current consumption	TBD
BSTVDD supply current consumption	TBD
IOVDD supply current consumption	TBD
Maximum MICBIAS current	30mA
Load on OUT1M, OUT1P, OUT2M, OUT2P	>600 ohms

8.2.3 Detailed Design Procedure

This section describes the necessary steps to configure the TAC5312-Q1 for this specific application. The following steps provide a sequence of items that must be executed in the time between powering the device up and reading data from the device or transitioning from one mode to another mode of operation.

1. Apply power to the device:
   a. Power up the IOVDD, BSTVDD and AVDD power supplies
   b. Wait for at least 1ms to allow the device to initialize the internal registers.
   c. The device now goes into sleep mode (low-power mode < 10 µA)
2. Transition from sleep mode to active mode whenever required for the operation:
   a. Wake up the device by writing to P0_R2 to disable sleep mode
   b. Wait for at least 1 ms to allow the device to complete the internal wake-up sequence
   c. Override the default configuration registers or programmable coefficients value as required (this step is optional)
   d. Enable all desired input channels by writing to P0_R118
   e. Enable all desired audio serial interface input/output channels by writing to P0_R40 to P0_R47 for DAC and P0_R30 to P0_R37 for ADC
   f. Power-up the ADC, DAC and MICBIAS by writing to P0_R120
   g. Apply FSYNC and BCLK with the desired output sample rates and the BCLK to FSYNC ratio

      This specific step can be done at any point in the sequence after step a.

      See the *セクション 6.3.3* section for supported sample rates and the BCLK to FSYNC ratio.
   h. The device recording data is now sent to the host processor using the TDM audio serial data bus and playback data from TDM is now played on the lineout
3. Transition from active mode to sleep mode (again) as required in the system for low-power operation:
   a. Enter sleep mode by writing to P0_R2 to enable sleep mode
   b. Wait at least 6 ms (when FSYNC = 48 kHz) for the volume to ramp down and for all blocks to power down
   c. Read P0_R122 to check the device shutdown and sleep mode status
   d. If the device P0_R122_D[7:5] status bit is 3'b100 then stop FSYNC and BCLK in the system
   e. The device now goes into sleep mode (low-power mode < 10 µA) and retains all register values
4. Transition from sleep mode to active mode (again) as required for the recording operation:
   a. Wake up the device by writing to P0_R2 to disable sleep mode
   b. Wait at least 1 ms to allow the device to complete the internal wake-up sequence
   c. Apply FSYNC and BCLK with the desired output sample rates and the BCLK to FSYNC ratio
   d. The device recording data is now sent to the host processor using the TDM audio serial data bus and playback data from TDM is now played on the lineout
5. Repeat step 4 and step 5 as required for mode transitions

9 Power Supply Recommendations

The power-supply sequence between the IOVDD, BSTVDD and AVDD rails can be applied in any order. However, after all supplies are stable, then only initiate the I^2C or SPI transactions to initialize the device.

For the supply power-up requirement, t_1, t_2 and t_3 must be at least 2 ms to allow the device to initialize the internal registers. For the supply power-down requirement, t_4, t_5 and t_6 must be at least 10 ms. This timing (as shown in 図 9-1) allows the device to ramp down the volume on the record data, power down the analog and digital blocks, and put the device into shutdown mode. The device can also be immediately put into shutdown mode by ramping down power supplies, but doing so causes an abrupt shutdown.

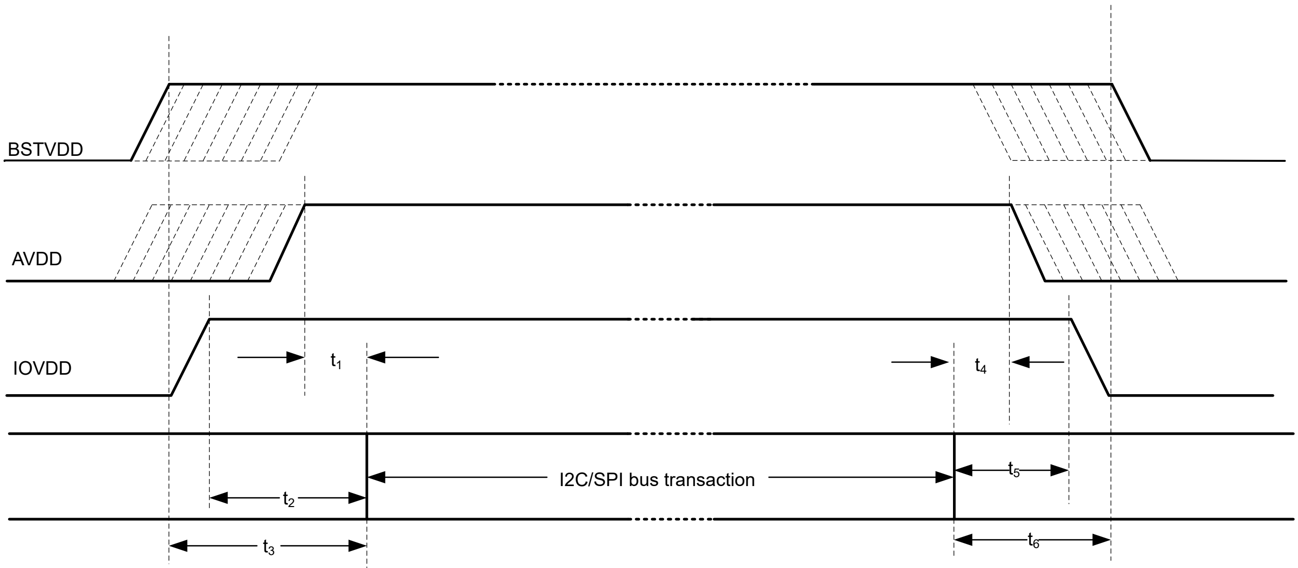

図 9-1. Power-Supply Sequencing Requirement Timing Diagram

Make sure that the supply ramp rate is slower than 0.1V/µs and that the wait time between a power-down and a power-up event is at least 100 ms. For supply ramp rate slower than 0.1 V/ms, host device must apply a software reset as first transaction before doing any device configuration. Make sure all digital input pins are at valid input levels and not toggling during supply sequencing.

The TAC5312-Q1 supports a single AVDD supply operation by integrating an on-chip digital regulator, DREG, and an analog regulator, AREG.

ADVANCE INFORMATION

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Documentation Support

10.1.1 Related Documentation

10.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。 変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

10.3 サポート・リソース

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10.4 Trademarks

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10.5 静電気放電に関する注意事項

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10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

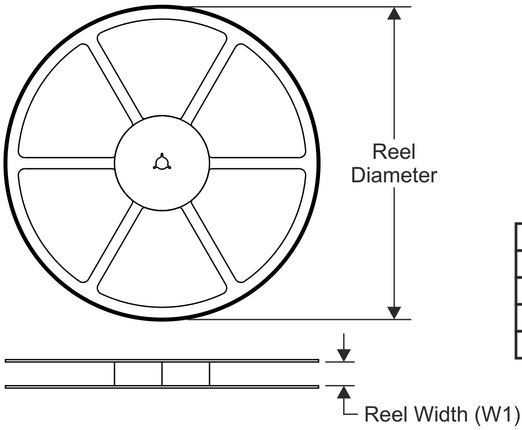
DATE	REVISION	NOTES
January 2024	*	Initial Release

12 Mechanical, Packaging, and Orderable Information

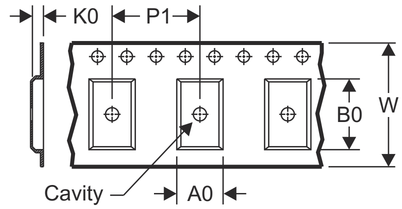
The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

12.1 Tape and Reel Information

REEL DIMENSIONS

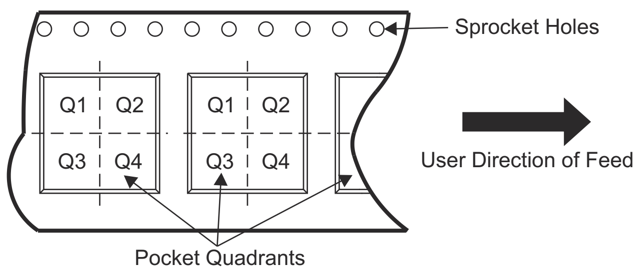


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

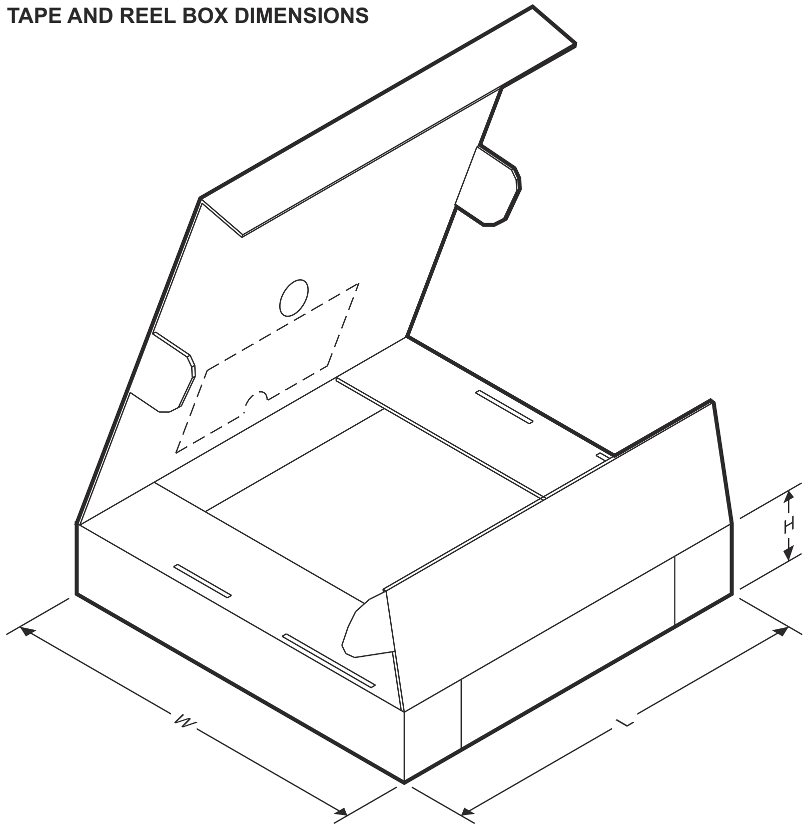


Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
XC5312WQRTVRQ1	WQFN	RTV	32	3000	330.0	12.4	5.3	5.3	1.1	8.0	12.0	Q1

ADVANCE INFORMATION

ADVANCE INFORMATION

TAPE AND REEL BOX DIMENSIONS



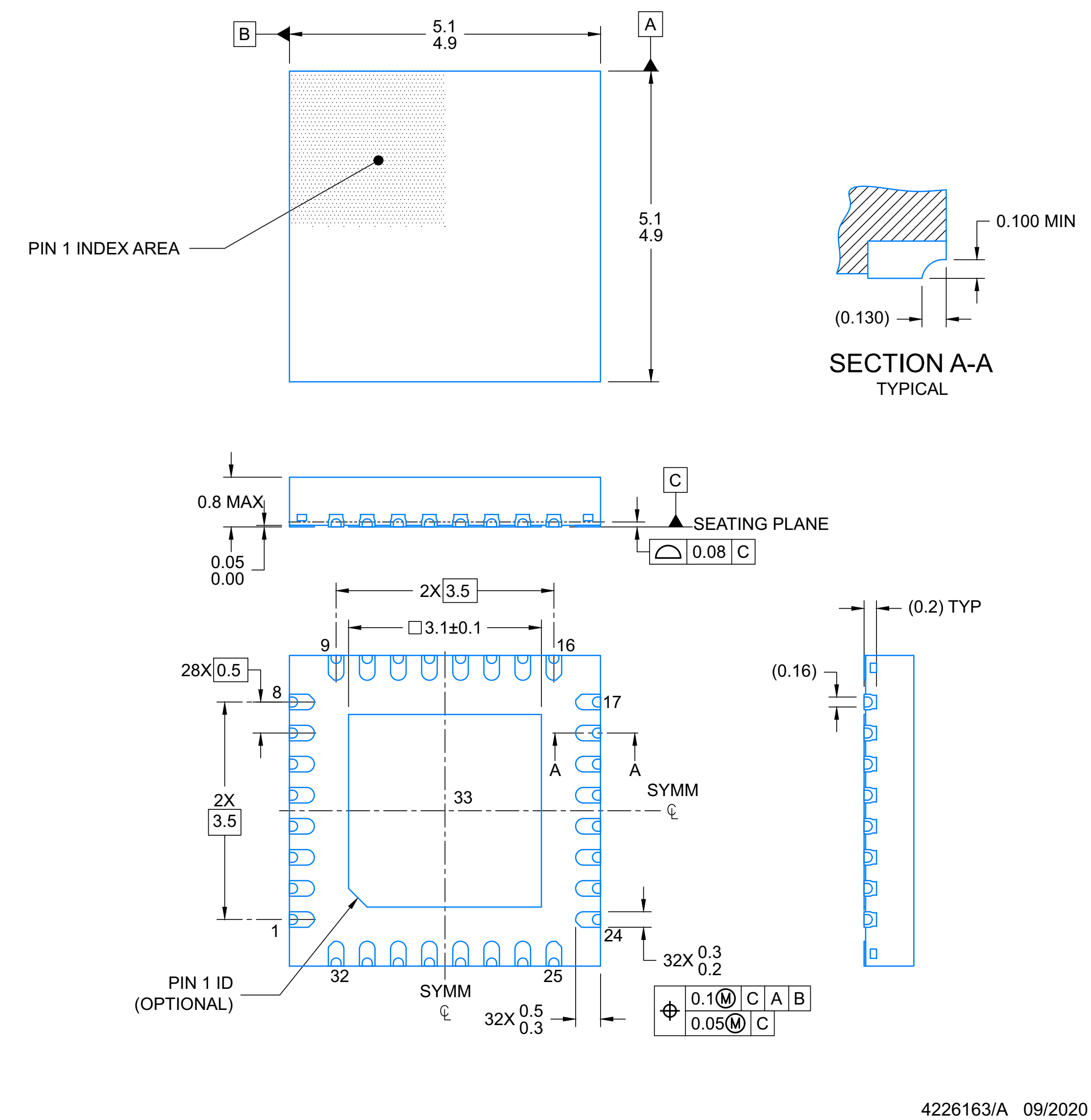
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
XC5312WQRTVRQ1	WQFN	RTV	32	3000	367.0	367.0	35.0

PACKAGE OUTLINE

RTV0032U

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for optimal thermal and mechanical performance.

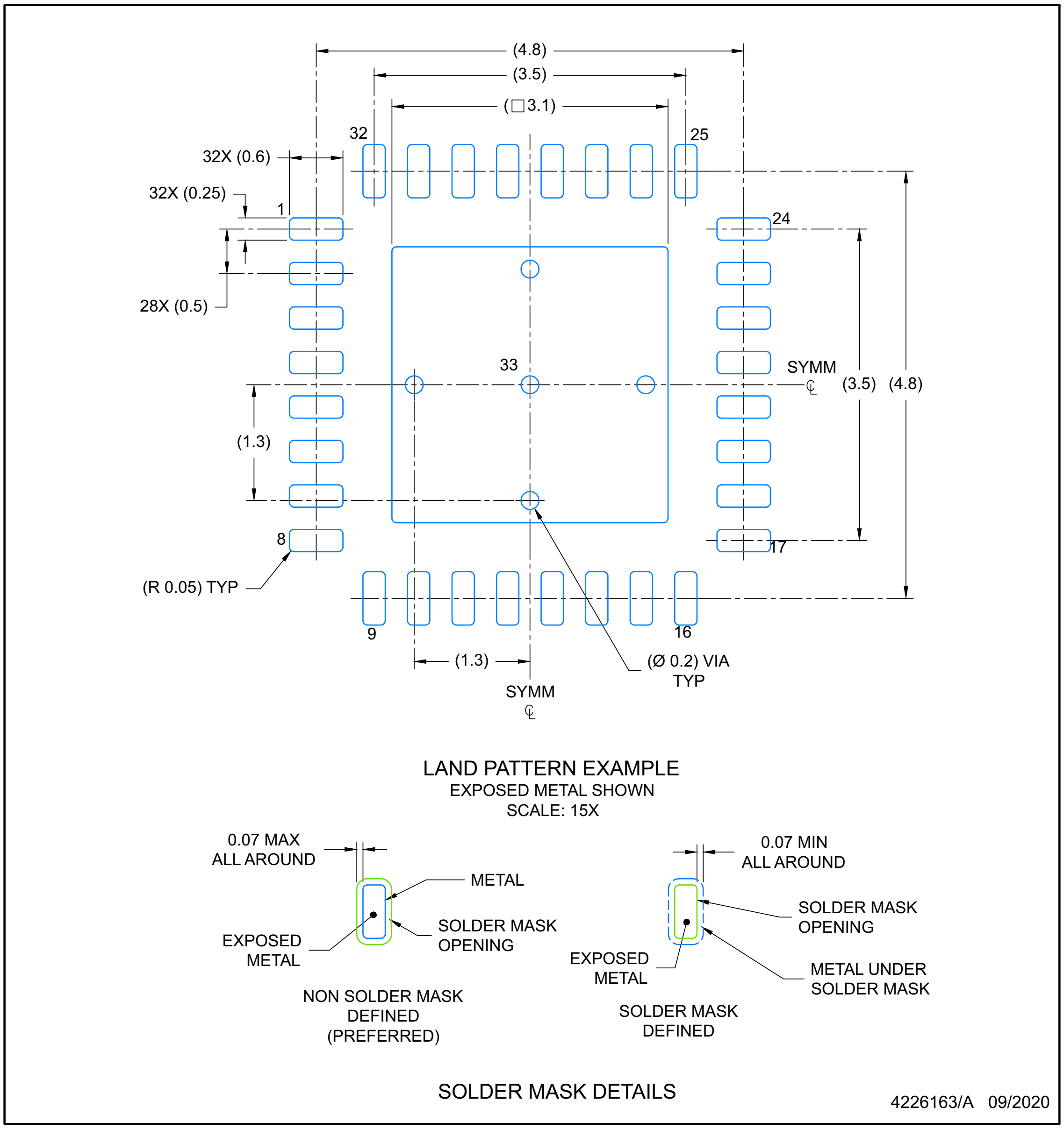
ADVANCE INFORMATION

EXAMPLE BOARD LAYOUT

RTV0032U

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271) .
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

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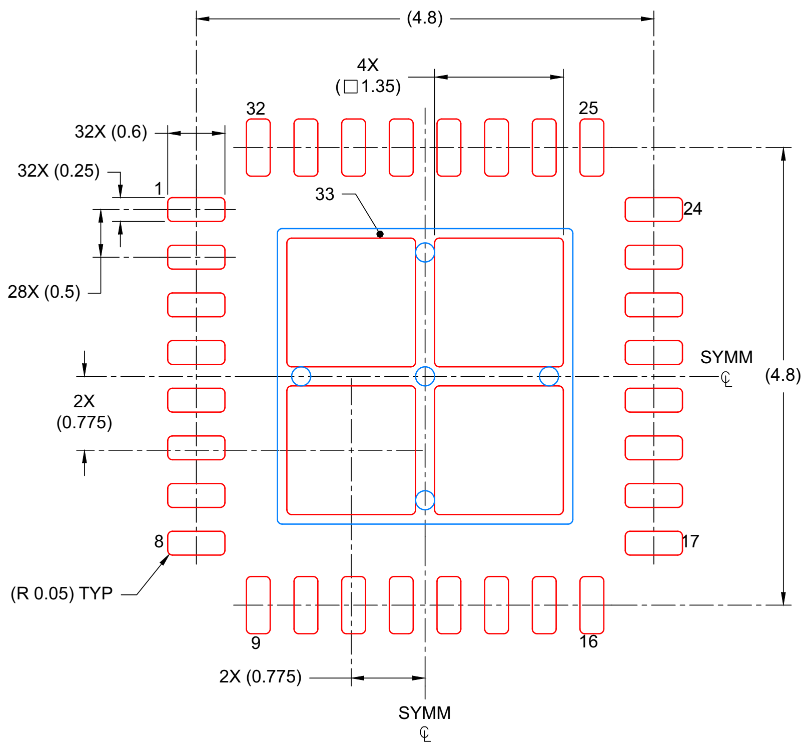
EXAMPLE STENCIL DESIGN

RTV0032U

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK-NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
76% PRINTED COVERAGE BY AREA
SCALE: 15X

4226163/A 09/2020

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
XC5312QRGERQ1	ACTIVE	VQFN	RGE	24	3000	TBD	Call TI	Call TI	-40 to 125		Samples
XC5312WQRTVRQ1	ACTIVE	WQFN	RTV	32	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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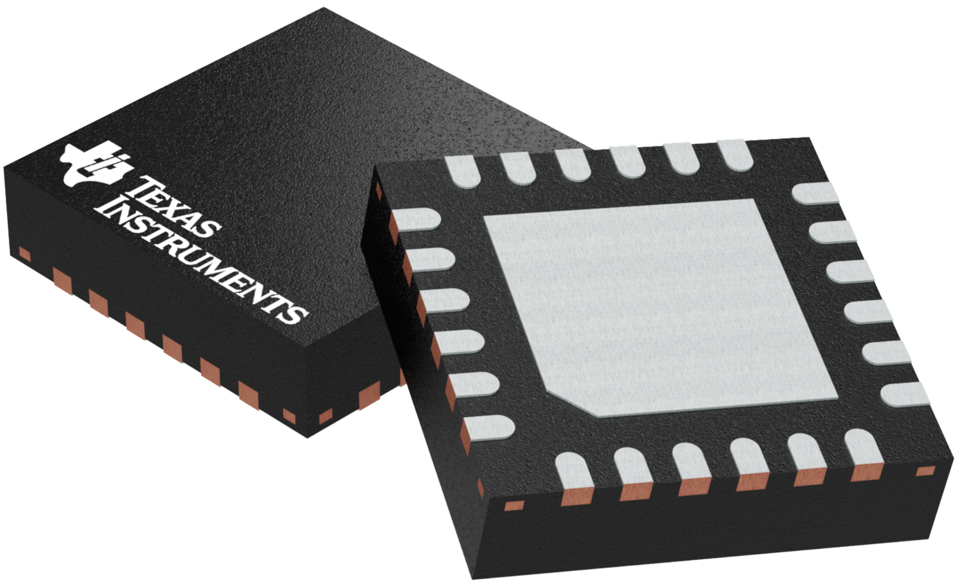
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

RGE 24 VQFN - 1 mm max height

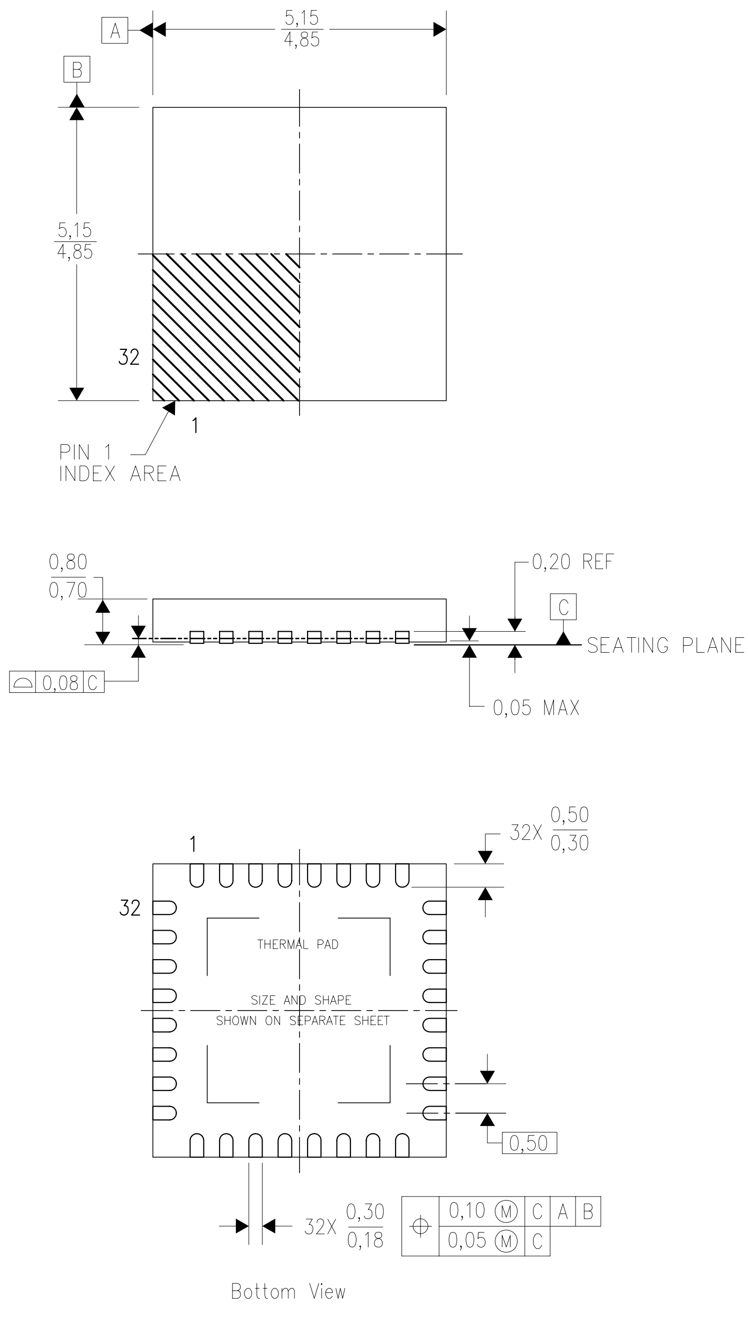
PLASTIC QUAD FLATPACK - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4204104/H

RTV (S-PWQFN-N32) PLASTIC QUAD FLATPACK NO-LEAD



NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
- B. This drawing is subject to change without notice.
- C. Quad Flatpack, No-Leads (QFN) package configuration.
- D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-220.

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