TLV906xS 低コスト・システム用の10MHz、RRIO、CMOSオペアンプ

1 特長

- レール・ツー・レールの入出力
- 低い入力オフセット電圧：±0.3mV
- ユニティ・ゲイン帯域幅：10MHz
- 低い広帯域ノイズ：10nV/√Hz
- 低い入力バイアス電流：0.5pA
- 低い静止電流：538µA
- ユニティ・ゲイン安定
- 内部 RFI および EMI フィルタ
- 最低 1.8V の電源電圧で動作
- 抵抗性の開ループ出力インピーダンスにより、大きな容量性負荷で簡単に安定
- シャットダウン・バージョン：TLV906xS
- 拡張温度範囲 -40°C～125°C

2 アプリケーション

- 電動アシスト自転車
- 煙感知器
- HVAC：暖房、換気、空調
- モーター制御：AC 誘導
- 冷蔵庫
- ウェアラブル機器
- ノート PC
- 洗濯機
- センサ信号コンディショニング
- パワー・モジュール
- バーコード・スキャナ
- アクティブ・フィルタ
- ローサイド電流センシング

3 概要

TLV9061 (シングル)、TLV9062 (デュアル)、TLV9064 (クワッド)は、シングル、デュアル、クワッドの低電圧 (1.8V～5.5V)オペアンプで、レール・ツー・レールの入力および出力機能があります。これらのデバイスは、低電圧での動作、小さな占有面積、大きな容量性負荷の駆動が必要なアプリケーション向けの、コスト効率の優れたソリューションです。TLV906x の容量性負荷駆動能力は 100pF ですが、開ループ出力インピーダンスは抵抗性なので、これより大きい容量性負荷も容易に安定化できます。これらのオペアンプは低電圧(1.8V～5.5V)で動作し、OPAx316およびTLVx316デバイスと同様の性能仕様を満たすよう、特別に設計されています。

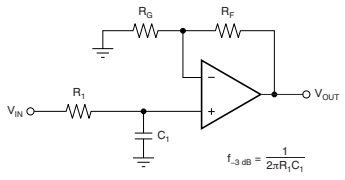
製品情報(1)

型番	パッケージ	本体サイズ(公称)
TLV9061	SOT-23 (5)	1.60mm×2.90mm
	SC70 (5)	1.25mm×2.00mm
	SOT553 (5)(2)	1.65mm×1.20mm
	X2SON (5)	0.80mm×0.80mm
TLV9061S	SOT-23 (6)	1.60mm×2.90mm
TLV9062	SOIC (8)	3.91mm×4.90mm
	TSSOP (8)	3.00mm×4.40mm
	VSSOP (8)	3.00mm×3.00mm
	SOT-23 (8)	1.60mm×2.90mm
	WSON (8)	2.00mm×2.00mm
TLV9062S	VSSOP (10)	3.00mm×3.00mm
	X2QFN (10)	1.50mm×2.00mm
TLV9064	SOIC (14)	8.65mm×3.91mm
	TSSOP (14)	4.40mm×5.00mm
	WQFN (16)	3.00mm×3.00mm
	X2QFN (14)	2.00mm×2.00mm
TLV9064S	WQFN (16)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

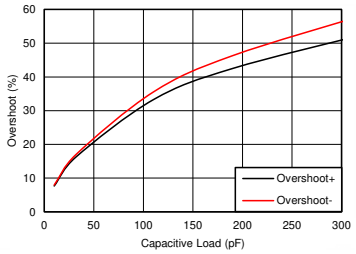
(2) このパッケージはプレビューのみです。

単極ローパス・フィルタ



$$\frac{V_{OUT}}{V_{IN}} = \left(1 + \frac{R_F}{R_G}\right)\left(\frac{1}{1 + sR_1C_1}\right)$$

小信号のオーバーシュートと負荷容量との関係



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision I (May 2019) から Revision J に変更 **Page**

- データシート全体で TLV9062IDDFR (SOT-23 (8)) パッケージのプレビュー注記を 削除 ... 1
- Added industry standard package names to *Device Comparison Table* ... 5
- Added note to packages with thermal pads, specifying that the thermal pads need to be connected to V– ... 7
- Added link to *Shutdown Function* section in $\overline{\text{SHDN}}$ pin function rows ... 11
- 追加 *EMI Rejection* section to the *Feature Description* section ... 24
- 変更 *Shutdown Function* section to add more clarification ... 25

Revision H (April 2019) から Revision I に変更 **Page**

- Added DDF (SOT-23) thermal information to replace TBDs ... 13

Revision G (December 2018) から Revision H に変更 **Page**

- 「*製品情報*」に SOT-23 (8) の情報を 追加 ... 1
- Added DDF package column to *Device Comparison Table* ... 5
- Added DDF (SOT-23) package to *Pin Functions* ... 7
- Added DDF (SOT-23) package to *Thermal Information* ... 13
- Added TLV9062 RUG (X2QFN) thermal information to replace TBDs ... 14

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Revision F (September 2018) から Revision G に変更 **Page**

- 「*製品情報*」表で、TLV9064 の RUC パッケージ名を「WQFN (14)」から「X2QFN (14)」に 変更 ... 1
- Added TLV9064 RUC (X2QFN) pinout drawing to *Pin Configuration and Functions* section ... 9
- Added RUC (X2QFN) package pinout information to Pin Functions: TLV9064 table ... 9
- Added RUC (X2QFN) to Thermal Information: TLV9064 table ... 14

Revision E (July 2018) から Revision F に変更 **Page**

- データシートのヘッダーからシャットダウン型番を 削除 ... 1
- TLV9062 の「製品情報」表から X2QFN (10) パッケージを 削除 ... 1
- シャットダウン型番への参照を「概要」セクションに 追加 ... 5
- データシート全体で、「TLV906xS シリーズ」を「TLV906xS ファミリ」に 変更 ... 5
- Added Shutdown devices to Device Comparison Table ... 5
- Changed pin namings for all pinout drawings to reflect updated nomenclature ... 6
- Added TLV9061S Thermal Information Table ... 13
- Added TLV9064S Thermal Information Table ... 14
- Deleted Partial Shutdown Amplifer Enable Time ... 16
- 追加 clarification on selecting resistors for a current sensing application in the Typical Applications Section ... 27
- 変更 wording of third bullet in Layout Guidelines ... 29

Revision D (June 2018) から Revision E に変更 **Page**

- 「*製品情報*」表に TLV9061S デバイスを 追加 ... 1
- 「*製品情報*」表に TLV9064S デバイスを 追加 ... 1
- Added RUC and RUG packages to the *Device Comparison* table ... 5
- Added TLV9061S DBV (SOT-23) pinout drawing to *Pin Configuration and Functions* section ... 7
- Added TLV9061S DBV (SOT-23) package pinout information to *Pin Functions: TLV9061S* table ... 7
- Added TLV9062S RUG (VSSOP) package pinout drawing to *Pin Configuration and Functions* section ... 8
- Added TLV9062S RUG (VSSOP) package pinout information to *Pin Functions: TLV9062S* table ... 8
- Added TLV9064 RTE (WQFN) pinout drawing to *Pin Configuration and Functions* section ... 9
- Added TLV9064 RTE pinout information to *Pin Functions: TLV9064* table ... 9
- Added TLV9064S RTE (WQFN) pinout drawing to *Pin Configuration and Functions* section ... 11

Revision C (March 2018) から Revision D に変更 **Page**

- ドキュメントのタイトルの"TLV906x"にシャットダウン接尾辞を 追加 ... 1
- 「*特長*」の箇条書き一覧に「シャットダウン・バージョン」項目を 追加 ... 1
- 「*製品情報*」表に TLV9062S デバイスを 追加 ... 1
- 「*概要 (続き)*」セクションのテキストにシャットダウンの説明を 追加 ... 5
- Added "(V_S = [V+] – [V–]) supply voltage parameter in *Absolute Maximum Ratings* table ... 12
- Added "input voltage range" and "output voltage range" parameters and values to *Recommended Operating Conditions* table ... 12
- Added shutdown pin recommended operating conditions in *Recommended Operating Conditions* table ... 12
- Added "T_A" symbol to "specified temperature" parameter to *Recommended Operating Conditions* table ... 12
- Added *Thermal Information: TLV9062S* thermal table data ... 14
- Added *Thermal Information: TLV9062S* thermal table data ... 14
- Added shutdown section to *Electrical Characteristics: V_S (Total Supply Voltage) = (V+) – (V–) = 1.8 V to 5.5 V* table ... 16

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- 追加 *Shutdown Function* section 25

Revision B (October 2017) から **Revision C** に変更 **Page**

- 製品ステータスを量産データ*/*混在ステータスから量産データに 変更 1
- 「*製品情報*」表で、TLV9061 DPW (X2SON) パッケージからパッケージのプレビュー版の注記を 削除 1
- Deleted package preview note from TLV9061 DPW (X2SON) package pinout drawing 6
- Changed formatting of *ESD Ratings* table to show different results for all packages 12
- Deleted package preview note from DPW (X2SON) package in *Thermal Information: TLV9061* table 13
- Deleted package preview note from DPW (X2SON) package in *Thermal Information: TLV9061* table 13

Revision A (June 2017) から **Revision B** に変更 **Page**

- Added 8-pin PW package to *Pin Configuration and Functions* section 7
- Added DSG (WSON) package to *Thermal Information* table 13
- Added PW (TSSOP) to TLV9062 *Thermal Information* table 13
- Changed maximum input offset voltage value from ±1.6 mV to 2 mV 15
- Changed maximum input offset voltage value from ±1.5 to ±1.6 mV 15
- Changed minimum common-mode rejection ratio input voltage range from 86 dB to 80 dB 15
- Changed typical input current noise density value from 10 to 23 fA/$\sqrt{\text{Hz}}$ 15
- Changed THD + N test conditions from V_S = 5 V to V_S = 5.5 V 15
- Added V_{CM} = 2.5 V test condition to THD + N parameter in *Electrical Characteristics* table 15
- Added maximum output voltage swing value from 25 mV to 60 mV 15
- Changed maximum output voltage swing value from 15 mV to 20 mV 15

2017年**3**月発行のものから更新 **Page**

- デバイスのステータスを「事前情報」から「量産データ」に 変更 1

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5 概要（続き）

TLV906xS デバイスにはシャットダウン・モードが搭載されており、アンプをオフにしてスタンバイ・モードに移行すると、消費電流は標準値で 1µA 未満になります。

TLV906xS ファミリはユニティ・ゲイン安定で、RFI および EMI 除去フィルタが内蔵されており、オーバードライブ状況でも位相反転が発生しないため、システム設計を簡素化できます。

すべてのチャネル・バリエーション (シングル、デュアル、クワッド) で、X2SON、X2QFN などのマイクロサイズ・パッケージと、SOIC、MSOP、SOT-23、TSSOP などの業界標準パッケージが利用可能です。

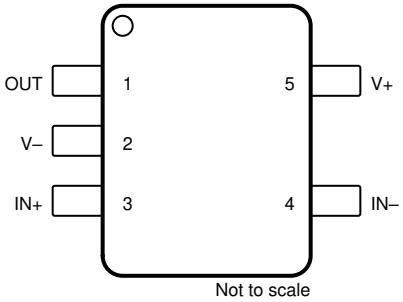
6 Device Comparison Table

DEVICE	NO. OF CHANNELS	PACKAGE LEADS												
		SOIC D	SOT-23 DBV	SC-70 DCK	VSSOP DGK	VSSOP DGS	X2SON DPW	SOT-553 DRL	WSON DSG	TSSOP PW	SOT-23 DDF	WQFN RTE	X2QFN RUC	X2QFN RUG
TLV9061	1	8	5	5	—	—	5	5	—	—	—	—	—	—
TLV9061S		—	6	—	—	—	—	—	—	—	—	—	—	—
TLV9062	2	8	—	—	8	10	—	—	8	8	8	—	—	—
TLV9062S		—	—	—	—	10	—	—	—	—	—	—	—	10
TLV9064	4	14	—	—	—	—	—	—	—	14	—	16	14	—
TLV9064S		—	—	—	—	—	—	—	—	—	—	16	—	—

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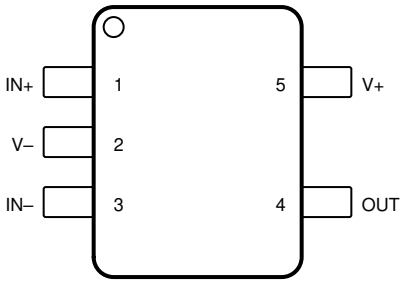
7 Pin Configuration and Functions

TLV9061 DBV, DRL Packages
5-Pin SOT-23, SOT-553
Top View



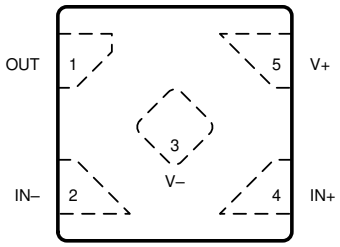
Not to scale

TLV9061 DCK Package
5-Pin SC70
Top View



Not to scale

TLV9061 DPW Package
5-Pin X2SON
Top View



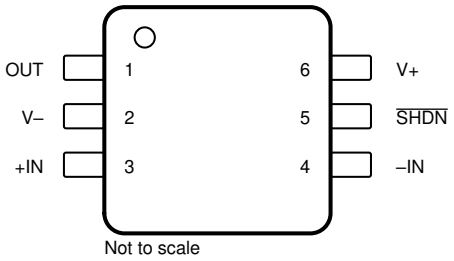
Not to scale

Pin Functions: TLV9061

PIN				I/O	DESCRIPTION
NAME	SOT-23, SOT-553	SC70	X2SON		
IN–	4	3	2	I	Inverting input
IN+	3	1	4	I	Noninverting input
OUT	1	4	1	O	Output
V–	2	2	3	I or —	Negative (low) supply or ground (for single-supply operation)
V+	5	5	5	I	Positive (high) supply

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TLV9061S DBV Package
6-Pin SOT-23
Top View

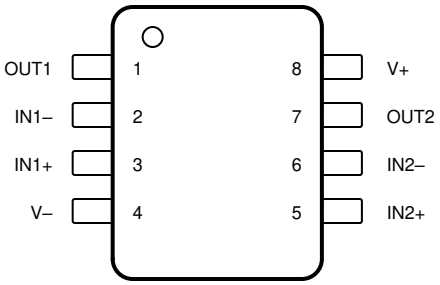


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Pin Functions: TLV9061S

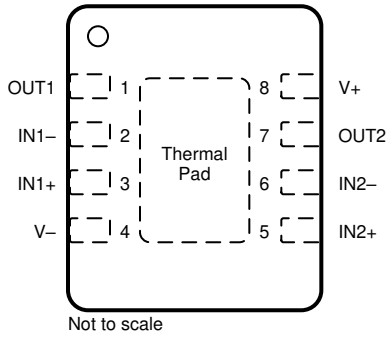
PIN		I/O	DESCRIPTION
NAME	NO.		
IN–	4	I	Inverting input
IN+	3	I	Noninverting input
OUT	1	O	Output
$\overline{\text{SHDN}}$	5	I	Shutdown: low = amp disabled, high = amp enabled. See *Shutdown Function* section for more information.
V–	2	I or —	Negative (low) supply or ground (for single-supply operation)
V+	6	I	Positive (high) supply

TLV9062 D, DGK, PW, DDF Packages
8-Pin SOIC, VSSOP, TSSOP, SOT-23
Top View



Not to scale

TLV9062 DSG Package
8-Pin WSON With Exposed Thermal Pad
Top View



Not to scale

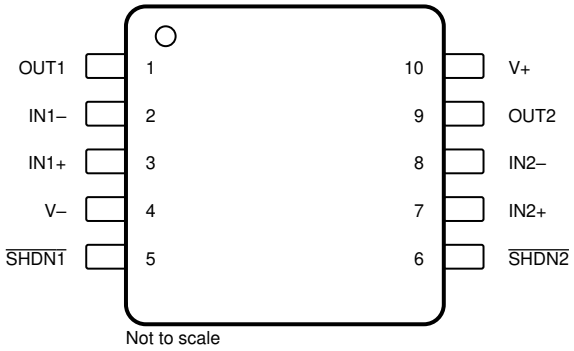
(1) Connect thermal pad to V–

Pin Functions: TLV9062

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1–	2	I	Inverting input, channel 1
IN1+	3	I	Noninverting input, channel 1
IN2–	6	I	Inverting input, channel 2
IN2+	5	I	Noninverting input, channel 2
OUT1	1	O	Output, channel 1
OUT2	7	O	Output, channel 2
V–	4	—	Negative (lowest) supply or ground (for single-supply operation)
V+	8	—	Positive (highest) supply

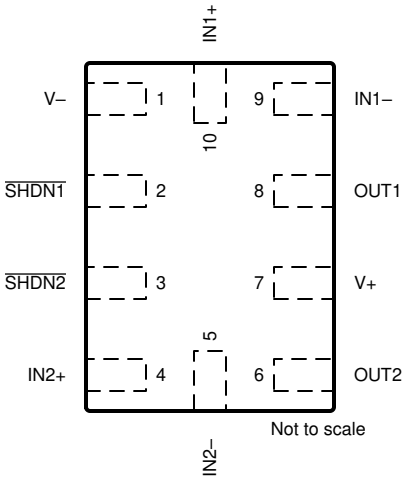
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TLV9062S DGS Package
10-Pin VSSOP
Top View



Not to scale

TLV9062S RUG Package
10-Pin X2QFN
Top View



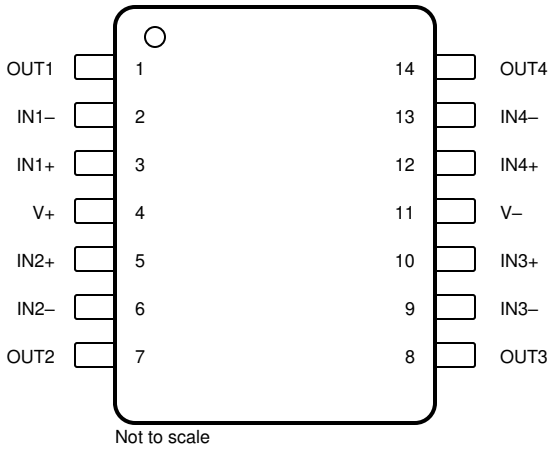
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Pin Functions: TLV9062S

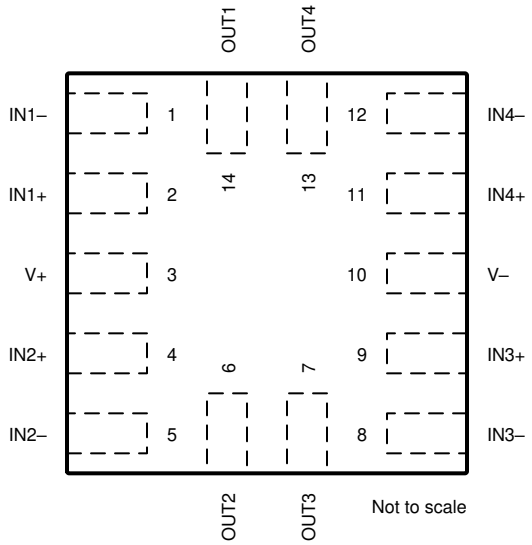
PIN			I/O	DESCRIPTION
NAME	VSSOP	X2QFN		
IN1–	2	9	I	Inverting input, channel 1
IN1+	3	10	I	Noninverting input, channel 1
IN2–	8	5	I	Inverting input, channel 2
IN2+	7	4	I	Noninverting input, channel 2
OUT1	1	8	O	Output, channel 1
OUT2	9	6	O	Output, channel 2
$\overline{\text{SHDN1}}$	5	2	I	Shutdown: low = amp disabled, high = amp enabled. Channel 1. See *Shutdown Function* section for more information.
$\overline{\text{SHDN2}}$	6	3	I	Shutdown: low = amp disabled, high = amp enabled. Channel 2. See *Shutdown Function* section for more information.
V–	4	1	I or —	Negative (low) supply or ground (for single-supply operation)
V+	10	7	I	Positive (high) supply

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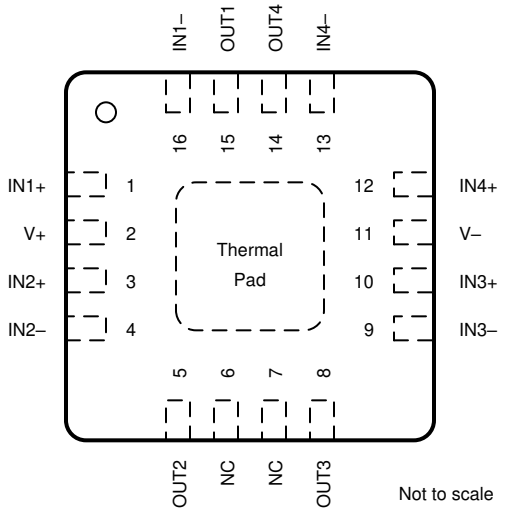
TLV9064 D, PW Packages
14-Pin SOIC, TSSOP
Top View



TLV9064 RUC Package
14-Pin X2QFN
Top View



TLV9064 RTE Package
16-Pin WQFN With Exposed Thermal Pad
Top View



(1) Connect thermal pad to V–

Pin Functions: TLV9064

PIN				I/O	DESCRIPTION
NAME	SOIC, TSSOP	WQFN	X2QFN		
IN1–	2	16	1	I	Inverting input, channel 1
IN1+	3	1	2	I	Noninverting input, channel 1
IN2–	6	4	5	I	Inverting input, channel 2
IN2+	5	3	4	I	Noninverting input, channel 2
IN3–	9	9	8	I	Inverting input, channel 3
IN3+	10	10	9	I	Noninverting input, channel 3
IN4–	13	13	12	I	Inverting input, channel 4
IN4+	12	12	11	I	Noninverting input, channel 4

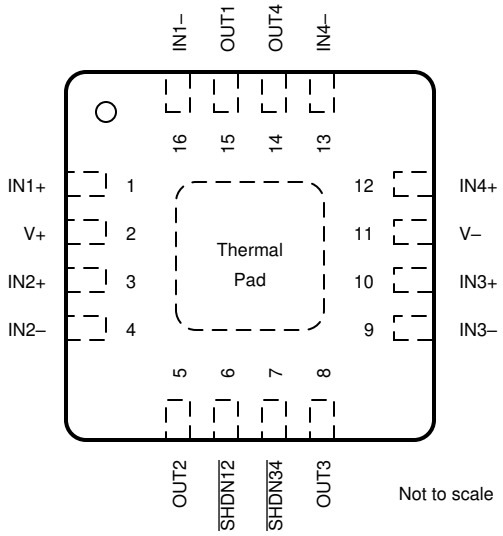
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Pin Functions: TLV9064 (continued)

PIN				I/O	DESCRIPTION
NAME	SOIC, TSSOP	WQFN	X2QFN		
NC	—	6, 7	—	—	No internal connection
OUT1	1	15	14	O	Output, channel 1
OUT2	7	5	6	O	Output, channel 2
OUT3	8	8	7	O	Output, channel 3
OUT4	14	14	13	O	Output, channel 4
V–	11	11	10	I or —	Negative (low) supply or ground (for single-supply operation)
V+	4	2	3	I	Positive (high) supply

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TLV9064S RTE Package
16-Pin WQFN With Exposed Thermal Pad
Top View



(1) Connect thermal pad to V–

Pin Functions: TLV9064S

PIN		I/O	DESCRIPTION
NAME	NO.		
IN1–	16	I	Inverting input, channel 1
IN1+	1	I	Noninverting input, channel 1
IN2–	4	I	Inverting input, channel 2
IN2+	3	I	Noninverting input, channel 2
IN3–	9	I	Inverting input, channel 3
IN3+	10	I	Noninverting input, channel 3
IN4–	13	I	Inverting input, channel 4
IN4+	12	I	Noninverting input, channel 4
OUT1	15	O	Output, channel 1
OUT2	5	O	Output, channel 2
OUT3	8	O	Output, channel 3
OUT4	14	O	Output, channel 4
$\overline{\text{SHDN12}}$	6	I	Shutdown: low = amp disabled, high = amp enabled. Channel 1. See *Shutdown Function* section for more information.
$\overline{\text{SHDN34}}$	7	I	Shutdown: low = amp disabled, high = amp enabled. Channel 1. See *Shutdown Function* section for more information.
V–	11	I or —	Negative (low) supply or ground (for single-supply operation)
V+	2	I	Positive (high) supply

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8 Specifications

8.1 Absolute Maximum Ratings

over operating ambient temperature (unless otherwise noted)(1)

			MIN	MAX	UNIT
Supply voltage [(V+) – (V–)]			0	6	V
Signal input pins	Voltage(2)	Common-mode	(V–) – 0.5	(V+) + 0.5	V
		Differential		(V+) – (V–) + 0.2	V
	Current(2)		–10	10	mA
Output short-circuit(3)			Continuous		mA
Temperature	Specified, T_A		–40	125	°C
	Junction, T_J			150	
	Storage, T_{stg}		–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input pins are diode-clamped to the power-supply rails. Current limit input signals that can swing more than 0.5 V beyond the supply rails to 10 mA or less.
(3) Short-circuit to ground, one amplifier per package.

8.2 ESD Ratings

		VALUE	UNIT
TLV9061 PACKAGES			
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	
ALL OTHER PACKAGES			
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_S	Supply voltage (V_S = [V+] – [V–])	1.8	5.5	V
V_I	Input voltage range	(V–) – 0.1	(V+) + 0.1	V
V_O	Output voltage range	V–	V+	V
V_{SHDN_IH}	High level input voltage at shutdown pin (amplifier enabled)	1.1	V+	V
V_{SHDN_IL}	Low level input voltage at shutdown pin (amplifier disabled)	V–	0.2	V
T_A	Specified temperature	–40	125	°C

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8.4 Thermal Information: TLV9061

THERMAL METRIC[1]		TLV9061			UNIT
		DBV (SOT-23)	DCK (SC70)	DPW (X2SON)	
		5 PINS	5 PINS	5 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	221.7	263.3	467	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	144.7	75.5	211.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	49.7	51	332.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	26.1	1	29.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	49	50.3	330.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	125	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

8.5 Thermal Information: TLV9061S

THERMAL METRIC[1]		TLV9061S	UNIT
		DBV (SOT-23)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	216.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	155.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	96.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	80.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	95.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics*.

8.6 Thermal Information: TLV9062

THERMAL METRIC[1]		TLV9062					UNIT
		D (SOIC)	DGK (VSSOP)	DSG (WSON)	PW (TSSOP)	DDF (SOT-23)	
		8 PINS	8 PINS	8 PINS	8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	157.6	201.2	94.4	205.8	184.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	104.6	85.7	116.5	106.7	112.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	99.7	122.9	61.3	133.9	99.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	55.6	21.2	13	34.4	18.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	99.2	121.4	61.7	132.6	99.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	34.4	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

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8.7 Thermal Information: TLV9062S

THERMAL METRIC(1)		TLV9062S		UNIT
		DGS (VSSOP)	RUG (X2QFN)	
		10 PINS	10 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	170.4	197.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	84.9	93.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	113.5	123.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	16.4	3.7	°C/W
ψ_{JB}	Junction-to-board characterization parameter	112.3	120.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

8.8 Thermal Information: TLV9064

THERMAL METRIC(1)		TLV9064				UNIT
		PW (TSSOP)	D (SOIC)	RTE (WQFN)	RUC (X2QFN)	
		14 PINS	14 PINS	16 PINS	14 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	135.8	106.9	65.1	205.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64	64	67.9	72.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	79	63	40.4	150.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.7	25.9	5.5	3.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	78.4	62.7	40.2	149.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	23.8	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

8.9 Thermal Information: TLV9064S

THERMAL METRIC(1)		TLV9064S	UNIT
		RTE (WQFN)	
		16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	65.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case(top) thermal resistance	67.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	40.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	40.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case(bottom) thermal resistance	23.8	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

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8.10 Electrical Characteristics

For V_S (Total Supply Voltage) = (V+) – (V–) = 1.8 V to 5.5 V at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OFFSET VOLTAGE						
V_{OS}	Input offset voltage	V_S = 5 V		±0.3	±1.6	mV
		V_S = 5 V, T_A = –40°C to 125°C			±2	
dV_{OS}/dT	Drift	V_S = 5 V, T_A = –40°C to 125°C		±0.53		µV/°C
PSRR	Power-supply rejection ratio	V_S = 1.8 V – 5.5 V, V_{CM} = (V–)		±7	±80	µV/V
	Channel separation, DC	At DC		100		dB
INPUT VOLTAGE RANGE						
V_{CM}	Common-mode voltage range	V_S = 1.8 V to 5.5 V	(V–) – 0.1		(V+) + 0.1	V
CMRR	Common-mode rejection ratio	V_S = 5.5 V, (V–) – 0.1 V < V_{CM} < (V+) – 1.4 V, T_A = –40°C to 125°C	80	103		dB
		V_S = 5.5 V, V_{CM} = –0.1 V to 5.6 V, T_A = –40°C to 125°C	57	87		
		V_S = 1.8 V, (V–) – 0.1 V < V_{CM} < (V+) – 1.4 V, T_A = –40°C to 125°C		88		
		V_S = 1.8 V, V_{CM} = –0.1 V to 1.9 V, T_A = –40°C to 125°C		81		
INPUT BIAS CURRENT						
I_B	Input bias current			±0.5		pA
I_{OS}	Input offset current			±0.05		pA
NOISE						
E_n	Input voltage noise (peak-to-peak)	V_S = 5 V, f = 0.1 Hz to 10 Hz		4.77		μV_{PP}
e_n	Input voltage noise density	V_S = 5 V, f = 10 kHz		10		nV/√Hz
		V_S = 5 V, f = 1 kHz		16		
i_n	Input current noise density	f = 1 kHz		23		fA/√Hz
INPUT CAPACITANCE						
C_{ID}	Differential			2		pF
C_{IC}	Common-mode			4		pF
OPEN-LOOP GAIN						
A_{OL}	Open-loop voltage gain	V_S = 1.8 V, (V–) + 0.04 V < V_O < (V+) – 0.04 V, R_L = 10 kΩ		100		dB
		V_S = 5.5 V, (V–) + 0.05 V < V_O < (V+) – 0.05 V, R_L = 10 kΩ	104	130		
		V_S = 1.8 V, (V–) + 0.06 V < V_O < (V+) – 0.06 V, R_L = 2 kΩ		100		
		V_S = 5.5 V, (V–) + 0.15 V < V_O < (V+) – 0.15 V, R_L = 2 kΩ		130		
FREQUENCY RESPONSE						
GBP	Gain bandwidth product	V_S = 5 V, G = +1		10		MHz
φ_m	Phase margin	V_S = 5 V, G = +1		55		°
SR	Slew rate	V_S = 5 V, G = +1		6.5		V/µs
t_S	Settling time	To 0.1%, V_S = 5 V, 2-V step , G = +1, C_L = 100 pF		0.5		µs
		To 0.01%, V_S = 5 V, 2-V step, G = +1, C_L = 100 pF		1		
t_{OR}	Overload recovery time	V_S = 5 V, V_{IN} × gain > V_S		0.2		µs
THD + N	Total harmonic distortion + noise(1)	V_S = 5.5 V, V_{CM} = 2.5 V, V_O = 1 V_{RMS}, G = +1, f = 1 kHz		0.0008%		
OUTPUT						
V_O	Voltage output swing from supply rails	V_S = 5.5 V, R_L = 10 kΩ			20	mV
		V_S = 5.5 V, R_L = 2 kΩ			60	
I_{SC}	Short-circuit current	V_S = 5 V		±50		mA
Z_O	Open-loop output impedance	V_S = 5 V, f = 10 MHz		100		Ω

(1) Third-order filter; bandwidth = 80 kHz at –3 dB.

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Electrical Characteristics (continued)

For V_S (Total Supply Voltage) = (V+) – (V–) = 1.8 V to 5.5 V at T_A = 25°C, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLY						
I_Q	Quiescent current per amplifier	V_S = 5.5 V, I_O = 0 mA		538	750	µA
		V_S = 5.5 V, I_O = 0 mA, T_A = –40°C to 125°C			800	
SHUTDOWN						
I_{QSD}	Quiescent current per amplifier	V_S = 1.8 V to 5.5 V, all amplifiers disabled, $\overline{SHDN}$ = Low		0.5	1.5	µA
Z_{SHDN}	Output impedance during shutdown	V_S = 1.8 V to 5.5 V, amplifier disabled		10 || 8		GΩ || pF
$V_{SHDN_THR_HI}$	High level voltage shutdown threshold (amplifier enabled)	V_S = 1.8 V to 5.5 V		(V–) + 0.9 V	(V–) + 1.1 V	V
$V_{SDHN_THR_LO}$	Low level voltage shutdown threshold (amplifier disabled)	V_S = 1.8 V to 5.5 V	(V–) + 0.2 V	(V–) + 0.7 V		V
t_{ON}	Amplifier enable time (shutdown)(2)	V_S = 1.8 V to 5.5 V, full shutdown; G = 1, V_{OUT} = 0.9 × V_S / 2, R_L connected to V–		10		µs
t_{OFF}	Amplifier disable time(2)	V_S = 1.8 V to 5.5 V, G = 1, V_{OUT} = 0.1 × V_S / 2, R_L connected to V–		0.6		µs
	$\overline{SHDN}$ pin input bias current (per pin)	V_S = 1.8 V to 5.5 V, V+ ≥ $\overline{SHDN}$ ≥ (V+) – 0.8 V		130		pA
		V_S = 1.8 V to 5.5 V, V– ≤ $\overline{SHDN}$ ≤ V– + 0.8 V		40		

(2) Disable time (t_{OFF}) and enable time (t_{ON}) are defined as the time interval between the 50% point of the signal applied to the $\overline{SHDN}$ pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.

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8.11 Typical Characteristics

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

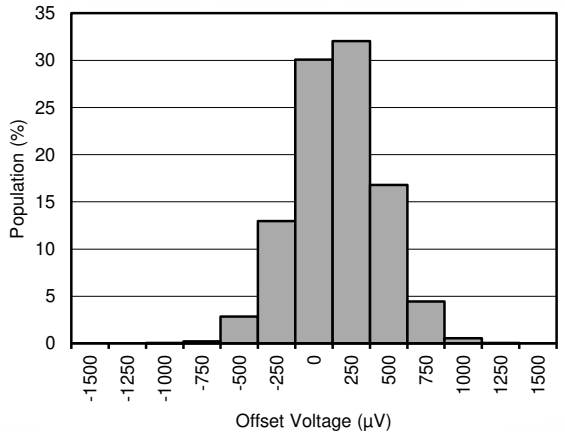
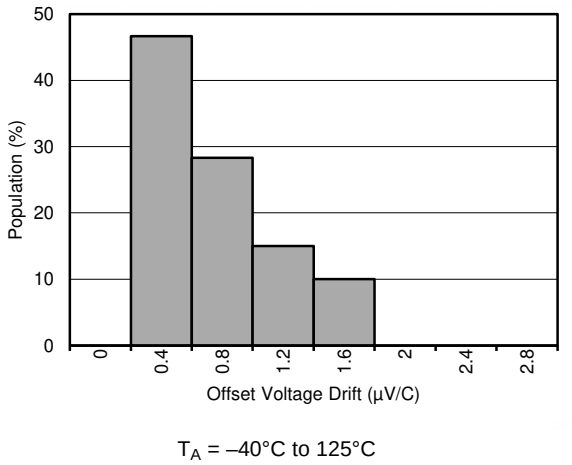


図 1. Offset Voltage Production Distribution



T_A = –40°C to 125°C

図 2. Offset Voltage Drift Distribution

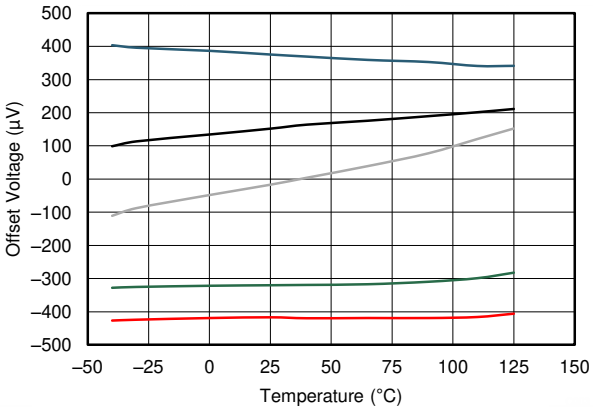
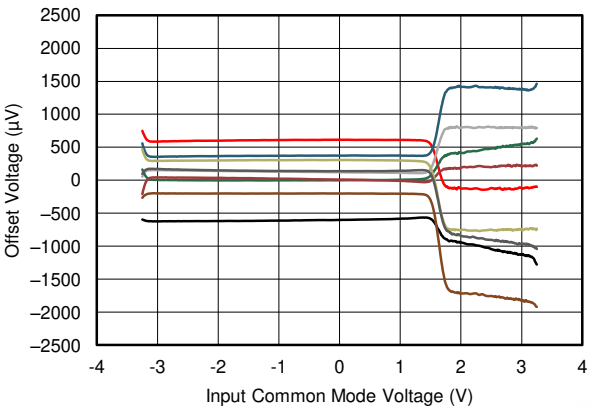
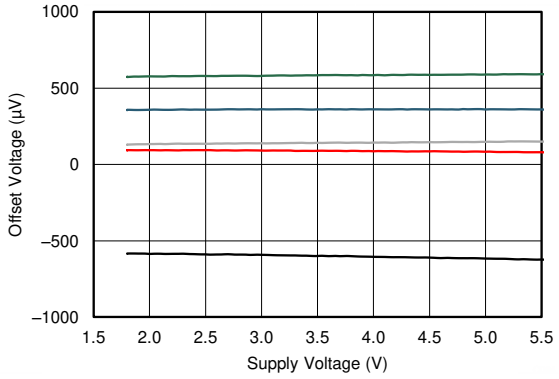


図 3. Offset Voltage vs Temperature



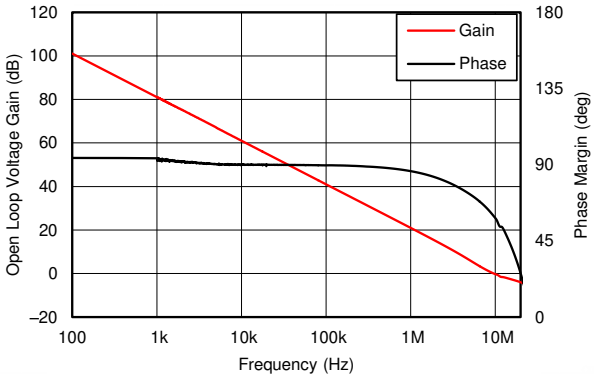
V+ = 2.75 V V– = –2.75 V

図 4. Offset Voltage vs Common-Mode Voltage



V_S = 1.8 V to 5.5 V

図 5. Offset Voltage vs Power Supply



C_L = 10 pF

図 6. Open-Loop Gain and Phase vs Frequency

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

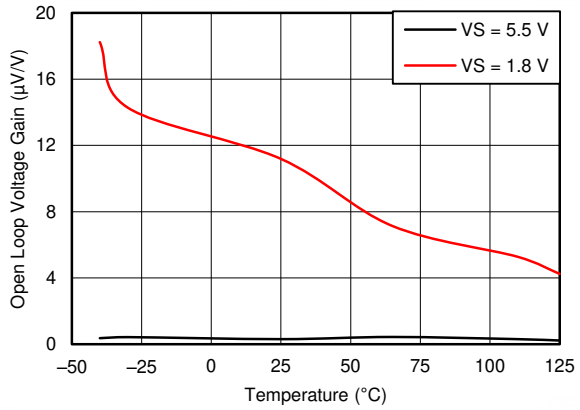


図 7. Open-Loop Gain vs Temperature

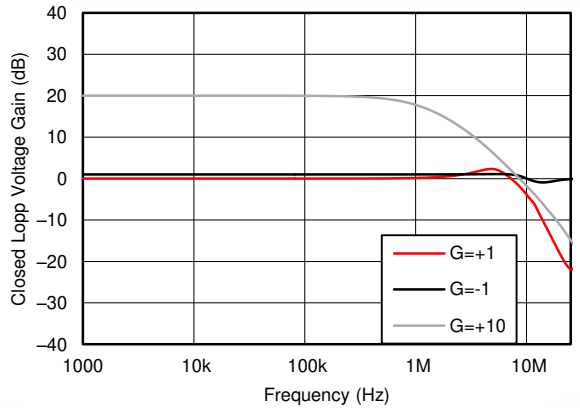


図 8. Closed-Loop Gain vs Frequency

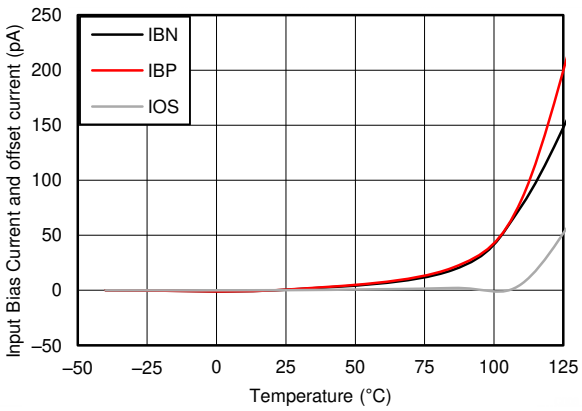


図 9. Input Bias Current vs Temperature

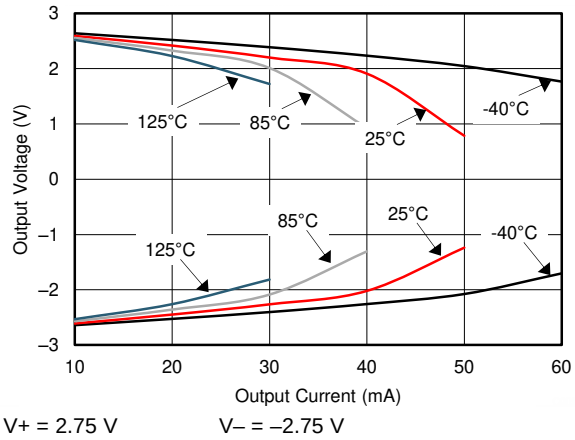


図 10. Output Voltage Swing vs Output Current

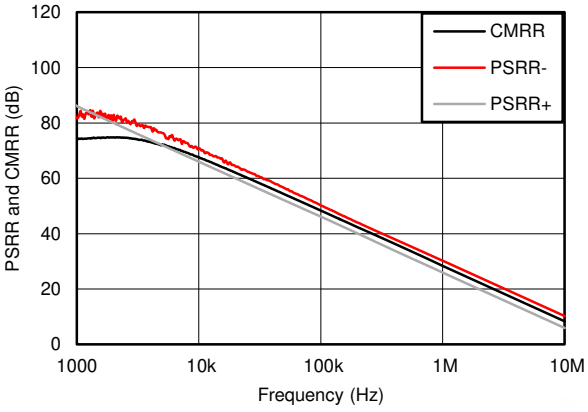


図 11. CMRR and PSRR vs Frequency (Referred to Input)

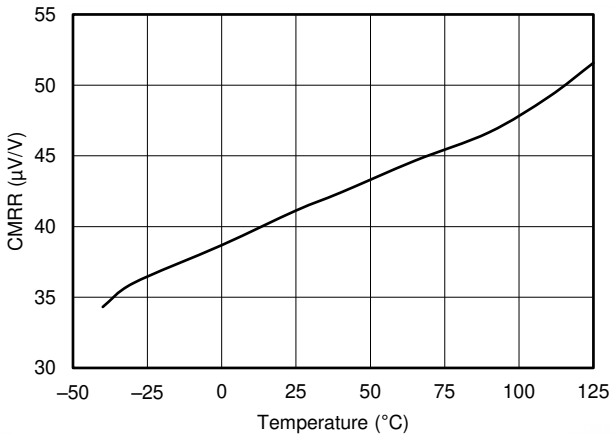
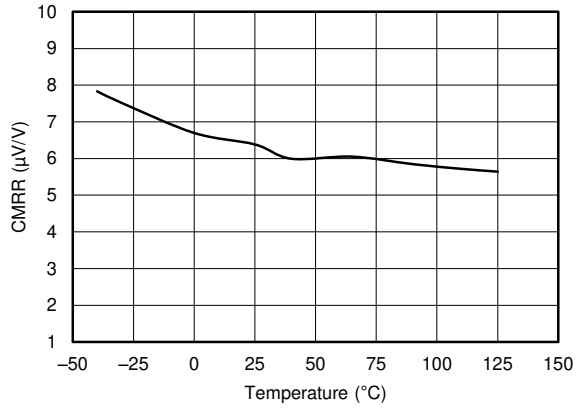


図 12. CMRR vs Temperature

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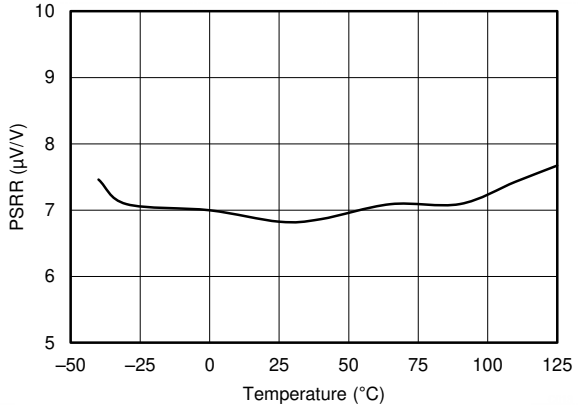
Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



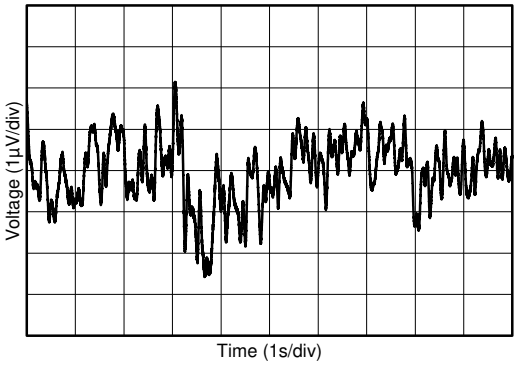
V_{CM} = (V–) – 0.1 V to (V+) – 1.4 V
T_A = –40°C to 125°C R_L = 10 kΩ V_S = 5.5 V

図 13. CMRR vs Temperature



V_S = 1.8 V to 5.5 V

図 14. PSRR vs Temperature



V_S = 1.8 V to 5.5 V

図 15. 0.1-Hz to 10-Hz Input Voltage Noise

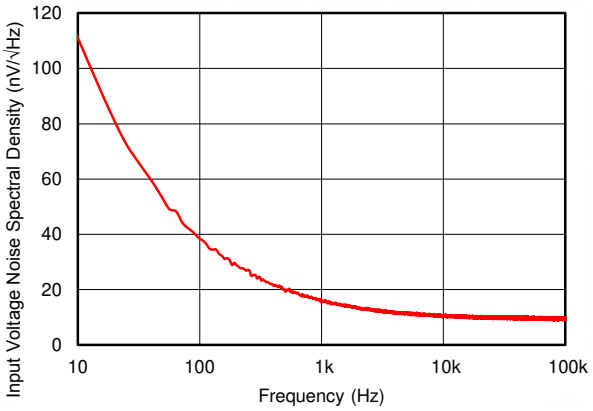
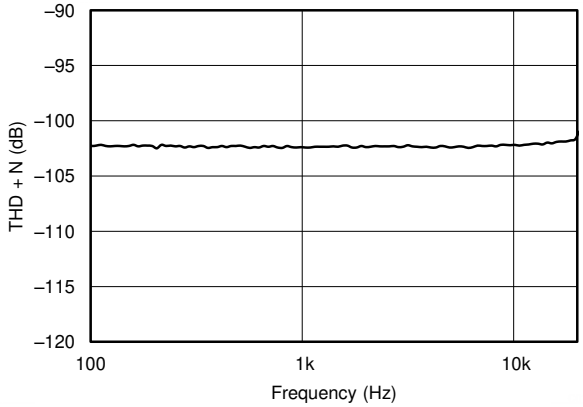
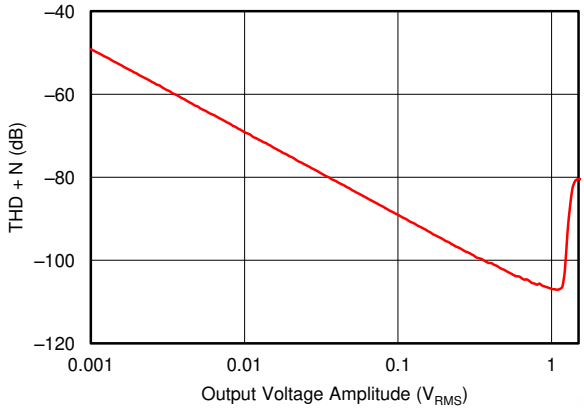


図 16. Input Voltage Noise Spectral Density vs Frequency



V_S = 5.5 V V_{CM} = 2.5 V R_L = 2 kΩ
V_{OUT} = 0.5 V_{RMS} BW = 80 kHz G = +1

図 17. THD + N vs Frequency



V_S = 5.5 V R_L = 2 kΩ G = +1
V_{CM} = 2.5 V BW = 80 kHz f = 1 kHz

図 18. THD + N vs Amplitude

Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

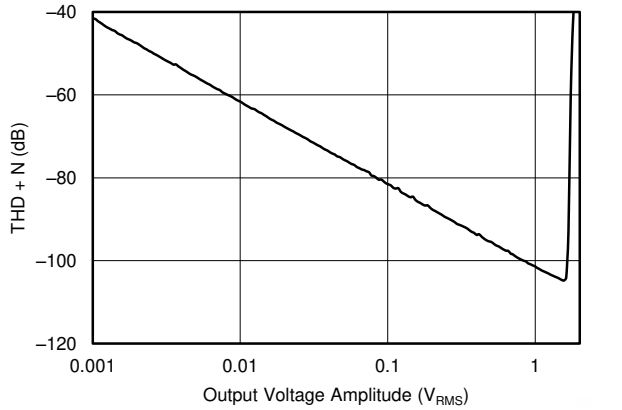


図 19. THD + N vs Amplitude

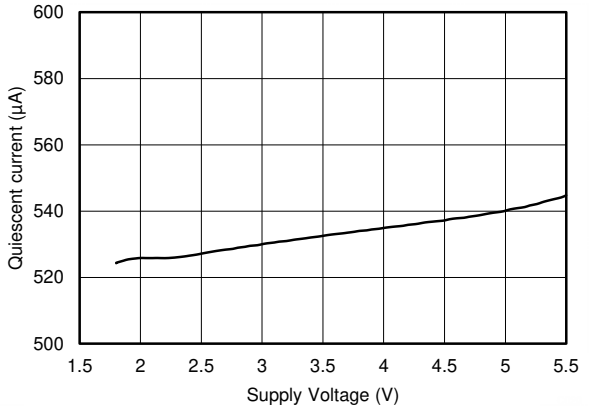


図 20. Quiescent Current vs Supply Voltage

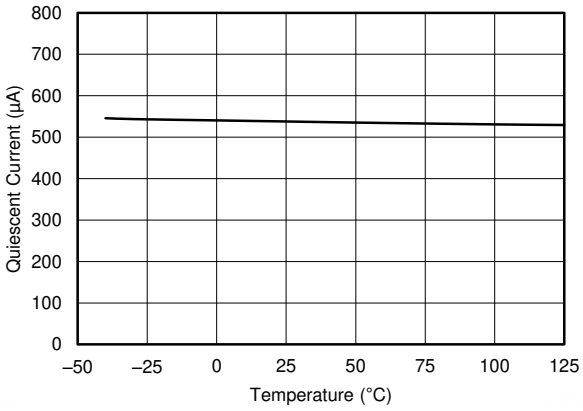


図 21. Quiescent Current vs Temperature

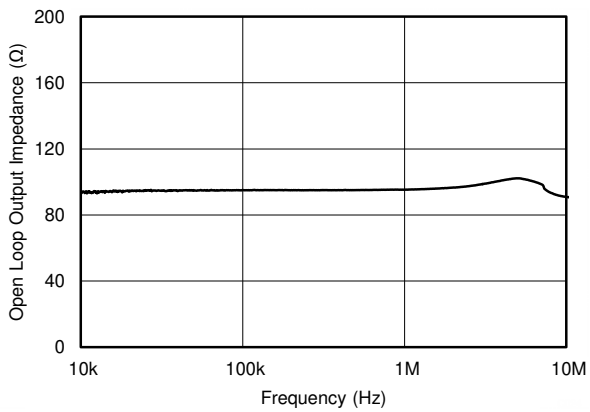


図 22. Open-Loop Output Impedance vs Frequency

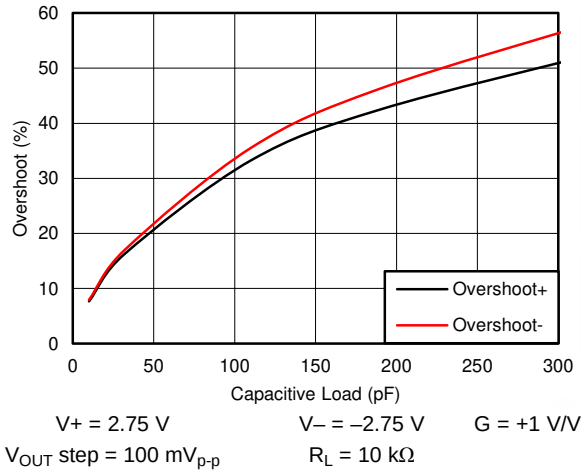


図 23. Small-Signal Overshoot vs Load Capacitance

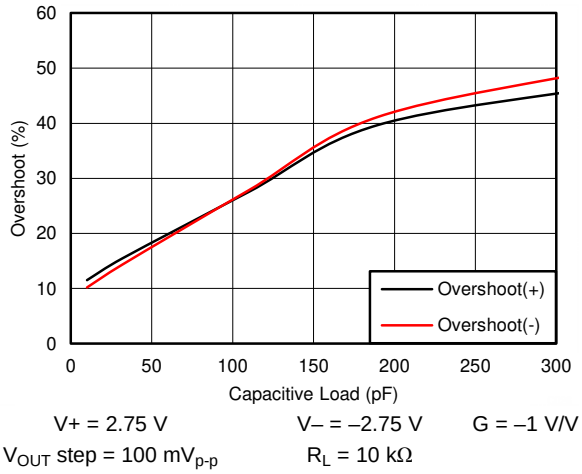
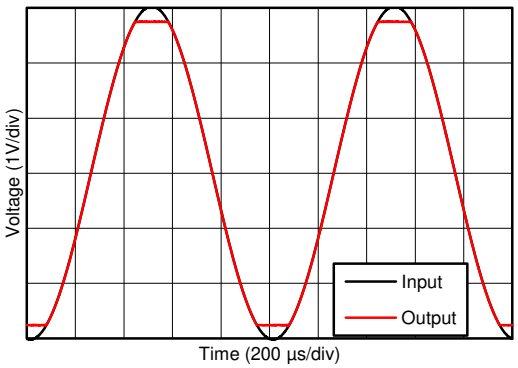


図 24. Small-Signal Overshoot vs Load Capacitance

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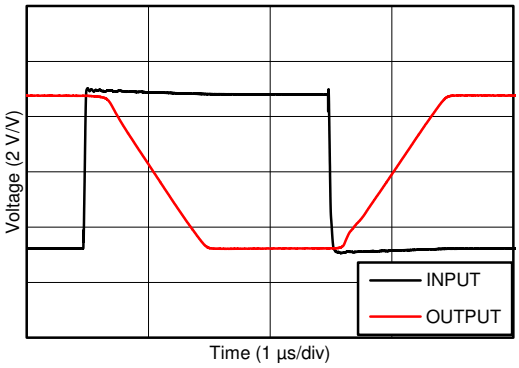
Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)



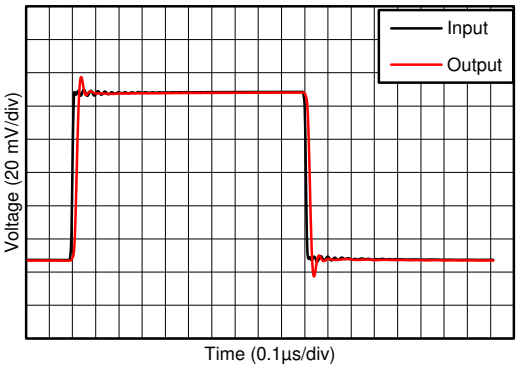
V+ = 2.75 V V– = –2.75 V

図 25. No Phase Reversal



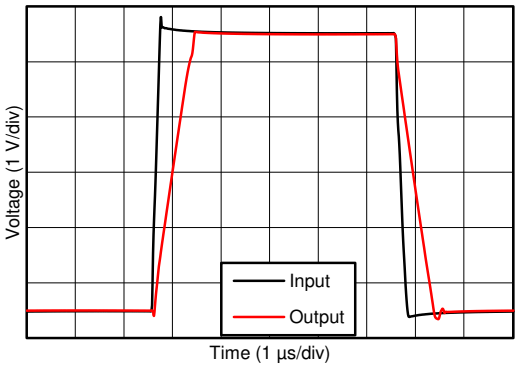
V+ = 2.75 V V– = –2.75 V G = –10 V/V

図 26. Overload Recovery



V+ = 2.75 V V– = –2.75 V G = 1 V/V

図 27. Small-Signal Step Response



V+ = 2.75 V V– = –2.75 V C_L = 100 pF
G = 1 V/V

図 28. Large-Signal Step Response

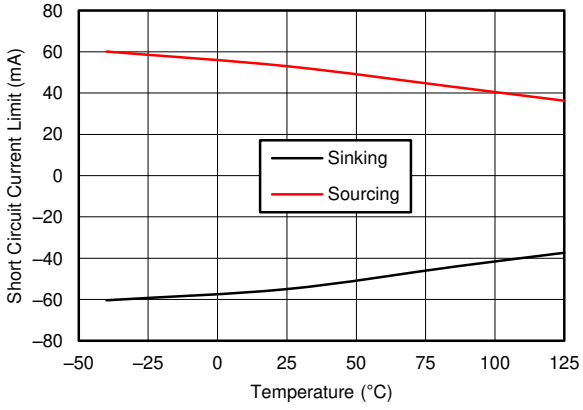
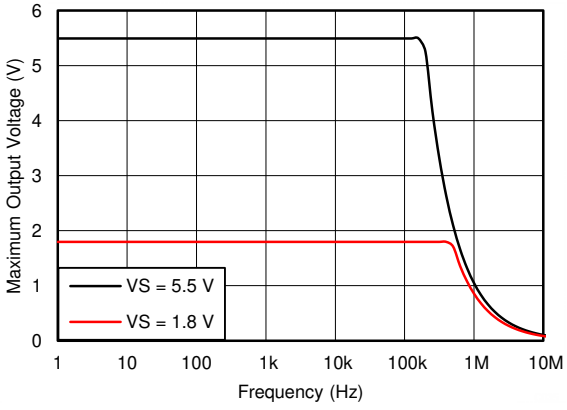


図 29. Short-Circuit Current vs Temperature



R_L = 10 kΩ C_L = 10 pF

図 30. Maximum Output Voltage vs Frequency and Supply Voltage

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Typical Characteristics (continued)

at T_A = 25°C, V_S = 5.5 V, R_L = 10 kΩ connected to V_S / 2, V_{CM} = V_S / 2, and V_{OUT} = V_S / 2 (unless otherwise noted)

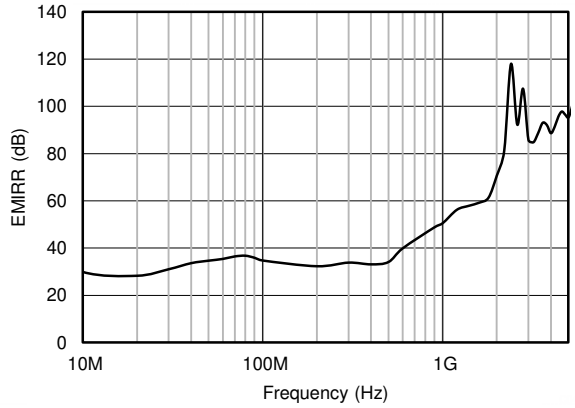


図 31. Electromagnetic Interference Rejection Ratio Referred to Noninverting Input (EMIRR+) vs Frequency

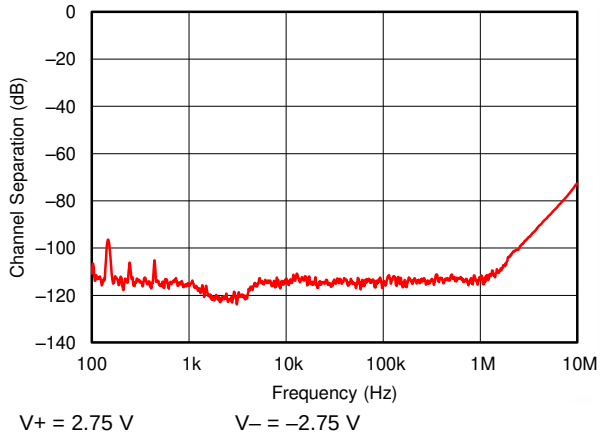


図 32. Channel Separation vs Frequency

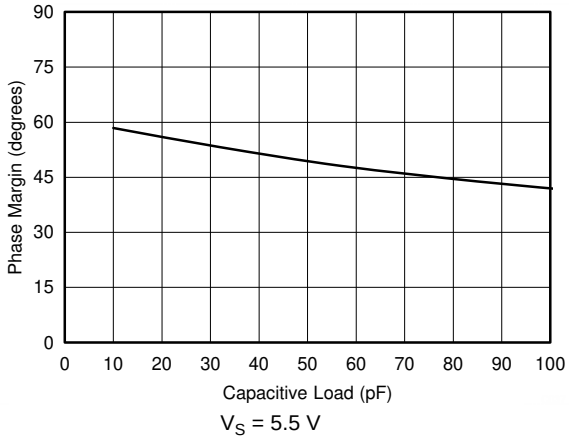


図 33. Phase Margin vs Capacitive Load

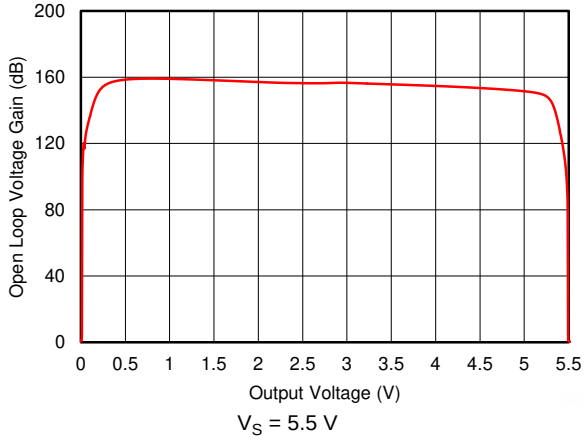


図 34. Open Loop Voltage Gain vs Output Voltage

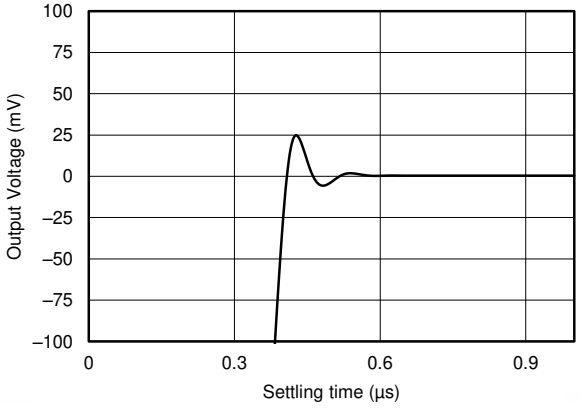


図 35. Large Signal Settling Time (Positive)

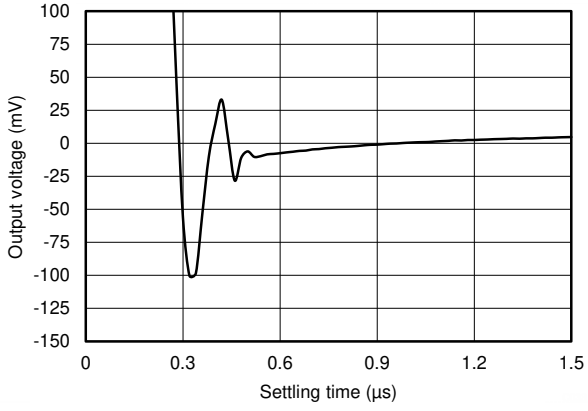


図 36. Large Signal Settling Time (Negative)

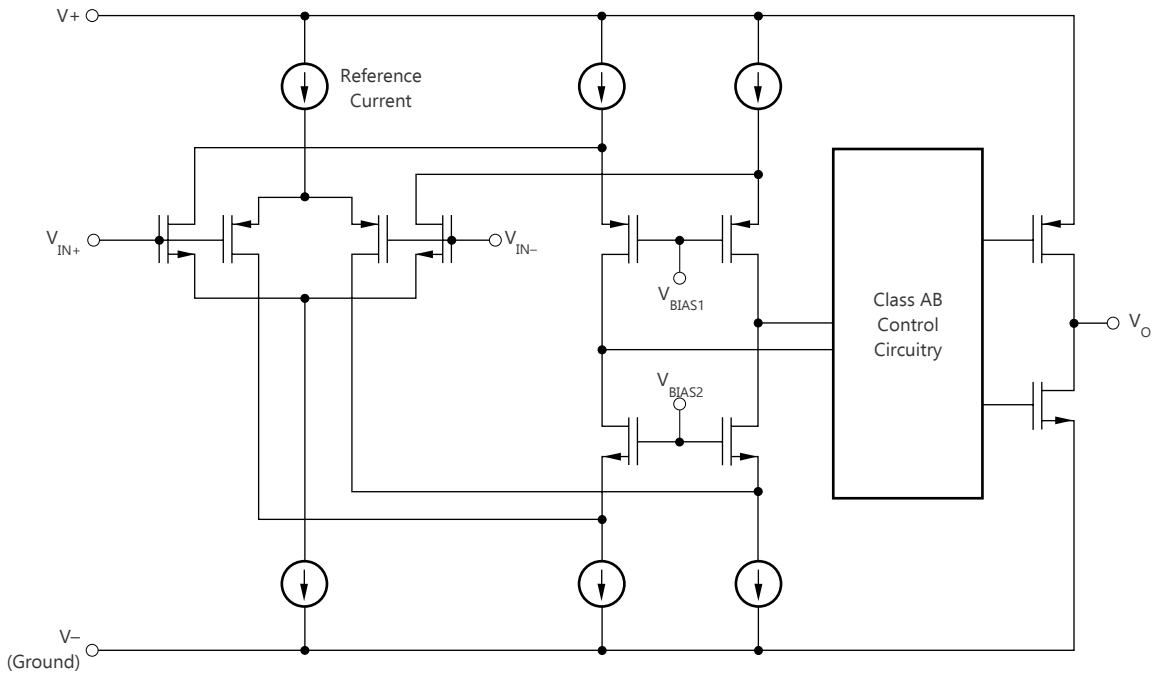
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9 Detailed Description

9.1 Overview

The TLV906x devices are a family of low-power, rail-to-rail input and output op amps. These devices operate from 1.8 V to 5.5 V, are unity-gain stable, and are designed for a wide range of general-purpose applications. The input common-mode voltage range includes both rails and allows the TLV906x series to be used in virtually any single-supply application. Rail-to-rail input and output swing significantly increases dynamic range, especially in low-supply applications. The high bandwidth enables this family to drive the sample-hold circuitry of analog-to-digital converters (ADCs).

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Rail-to-Rail Input

The input common-mode voltage range of the TLV906x family extends 100 mV beyond the supply rails for the full supply voltage range of 1.8 V to 5.5 V. This performance is achieved with a complementary input stage: an N-channel input differential pair in parallel with a P-channel differential pair, as shown in the *Functional Block Diagram*. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1.4 V to 200 mV above the positive supply, whereas the P-channel pair is active for inputs from 200 mV below the negative supply to approximately (V+) – 1.4 V. There is a small transition region, typically (V+) – 1.2 V to (V+) – 1 V, in which both pairs are on. This 200-mV transition region can vary up to 200 mV with process variation. Thus, the transition region (with both stages on) can range from (V+) – 1.4 V to (V+) – 1.2 V on the low end, and up to (V+) – 1 V to (V+) – 0.8 V on the high end. Within this transition region, PSRR, CMRR, offset voltage, offset drift, and THD can degrade compared to device operation outside this region.

9.3.2 Rail-to-Rail Output

Designed as a low-power, low-voltage operational amplifier, the TLV906x series delivers a robust output drive capability. A class AB output stage with common-source transistors achieves full rail-to-rail output swing capability. For resistive loads of 10 kΩ, the output swings to within 15 mV of either supply rail, regardless of the applied power-supply voltage. Different load conditions change the ability of the amplifier to swing close to the rails.

9.3.3 EMI Rejection

The TLV906x uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the TLV906x benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. 図 37 shows the results of this testing on the TLV906x. 表 1 shows the EMIRR IN+ values for the TLV906x at particular frequencies commonly encountered in real-world applications. The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.

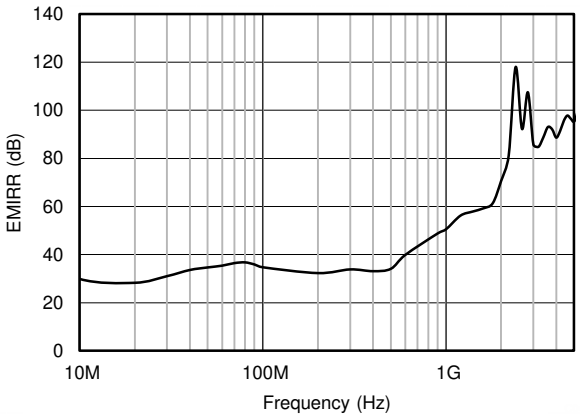


図 37. EMIRR Testing

表 1. TLV906x EMIRR IN+ For Frequencies of Interest

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
400 MHz	Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications	59.5 dB
900 MHz	Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications	68.9 dB
1.8 GHz	GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz)	77.8 dB

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Feature Description (continued)

表 1. TLV906x EMIRR IN+ For Frequencies of Interest (continued)

FREQUENCY	APPLICATION OR ALLOCATION	EMIRR IN+
2.4 GHz	802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz)	78.0 dB
3.6 GHz	Radiolocation, aero communication and navigation, satellite, mobile, S-band	88.8 dB
5 GHz	802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz)	87.6 dB

9.3.4 Overload Recovery

Overload recovery is defined as the time required for the operational amplifier output to recover from a saturated state to a linear state. The output devices of the operational amplifier enter a saturation region when the output voltage exceeds the rated operating voltage, because of the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return to the linear state. After the charge carriers return to the linear state, the device begins to slew at the specified slew rate. Therefore, the propagation delay (in case of an overload condition) is the sum of the overload recovery time and the slew time. The overload recovery time for the TLV906x family is approximately 200 ns.

9.3.5 Shutdown Function

The TLV906xS devices feature $\overline{\text{SHDN}}$ pins that disable the op amp, placing it into a low-power standby mode. In this mode, the op amp typically consumes less than 1 µA. The $\overline{\text{SHDN}}$ pins are active-low, meaning that shutdown mode is enabled when the input to the $\overline{\text{SHDN}}$ pin is a valid logic low.

The $\overline{\text{SHDN}}$ pins are referenced to the negative supply voltage of the op amp. The threshold of the shutdown feature lies around 800 mV (typical) and does not change with respect to the supply voltage. Hysteresis has been included in the switching threshold to ensure smooth switching characteristics. To ensure optimal shutdown behavior, the $\overline{\text{SHDN}}$ pins should be driven with valid logic signals. A valid logic low is defined as a voltage between V– and V– + 0.2 V. A valid logic high is defined as a voltage between V– + 1.2 V and V+. The shutdown pin must either be connected to a valid high or a low voltage or driven, and not left as an open circuit. There is ***no*** internal pull-up to enable the amplifier.

The $\overline{\text{SHDN}}$ pins are high-impedance CMOS inputs. Dual op amp versions are independently controlled, and quad op amp versions are controlled in pairs with logic inputs. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The enable time is 10 µs for full shutdown of all channels; disable time is 6 µs. When disabled, the output assumes a high-impedance state. This architecture allows the TLV906xS to be operated as a gated amplifier (or to have the device output multiplexed onto a common analog output bus). Shutdown time (t_{OFF}) depends on loading conditions and increases as load resistance increases. To ensure shutdown (disable) within a specific shutdown time, the specified 10-kΩ load to midsupply (V_S / 2) is required. If using the TLV906xS without a load, the resulting turnoff time is significantly increased.

9.4 Device Functional Modes

The TLV906x family are operational when the power-supply voltage is between 1.8 V (±0.9 V) and 5.5 V (±2.75 V). The TLV906xS devices feature a shutdown mode and are shut down when a valid logic low is applied to the shutdown pin.

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10 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The TLV906x family features 10-MHz bandwidth and 6.5-V/µs slew rate with only 538 µA of supply current per channel, providing good AC-performance at very low power consumption. DC applications are well served with a very low input noise voltage of 10 nV/√Hz at 10 kHz, low input bias current, and a typical input offset voltage of 0.3 mV.

10.2 Typical Applications

10.2.1 Typical Low-Side Current Sense Application

図 38 shows the TLV906x configured in a low-side current-sensing application.

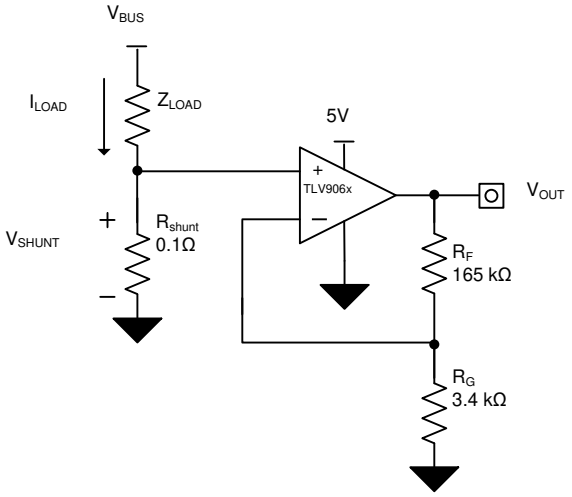


図 38. TLV906x in a Low-Side, Current-Sensing Application

10.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.95 V
- Maximum shunt voltage: 100 mV

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Typical Applications (continued)

10.2.1.2 Detailed Design Procedure

The transfer function of the circuit in 図 38 is given in 式 1.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \tag{1}$$

The load current (I_{LOAD}) produces a voltage drop across the shunt resistor (R_{SHUNT}). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using 式 2.

$$R_{SHUNT} = \frac{V_{SHUNT_MAX}}{I_{LOAD_MAX}} = \frac{100mV}{1A} = 100m\Omega \tag{2}$$

Using 式 2, R_{SHUNT} equals 100 mΩ. The voltage drop produced by I_{LOAD} and R_{SHUNT} is amplified by the TLV906x to produce an output voltage of approximately 0 V to 4.95 V. 式 3 calculates the gain required for the TLV906x to produce the required output voltage.

$$Gain = \frac{\left(V_{OUT_MAX} - V_{OUT_MIN}\right)}{\left(V_{IN_MAX} - V_{IN_MIN}\right)} \tag{3}$$

Using 式 3, the required gain equals 49.5 V/V, which is set with the R_F and R_G resistors. 式 4 sizes the R_F and R_G, resistors to set the gain of the TLV906x to 49.5 V/V.

$$Gain = 1 + \frac{\left(R_F\right)}{\left(R_G\right)} \tag{4}$$

Selecting R_F to equal 165 kΩ and R_G to equal 3.4 kΩ provides a combination that equals approximately 49.5 V/V. 図 39 shows the measured transfer function of the circuit shown in 図 38. Notice that the gain is only a function of the feedback and gain resistors. This gain is adjusted by varying the ratio of the resistors and the actual resistor values are determined by the impedance levels that the designer wants to establish. The impedance level determines the current drain, the effect that stray capacitance has, and a few other behaviors. There is no optimal impedance selection that works for every system, you must choose an impedance that is ideal for your system parameters.

10.2.1.3 Application Curve

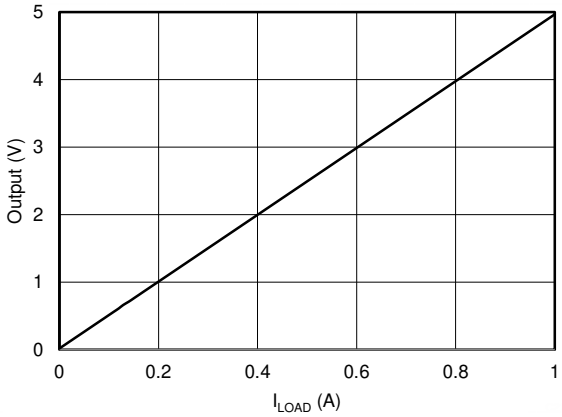


図 39. Low-Side, Current-Sense, Transfer Function

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11 Power Supply Recommendations

The TLV906x series is specified for operation from 1.8 V to 5.5 V (±0.9 V to ±2.75 V); many specifications apply from –40°C to 125°C. The *Typical Characteristics* section presents parameters that can exhibit significant variance with regard to operating voltage or temperature.

> **注意**
>
> Supply voltages larger than 6 V can permanently damage the device; see the *Absolute Maximum Ratings* table.

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, see the *Layout* section.

11.1 Input and ESD Protection

The TLV906x series incorporates internal ESD protection circuits on all pins. For input and output pins, this protection primarily consists of current-steering diodes connected between the input and power-supply pins. These ESD protection diodes provide in-circuit, input overdrive protection, as long as the current is limited to 10 mA, as shown in the *Absolute Maximum Ratings* table. 図 40 shows how a series input resistor can be added to the driven input to limit the input current. The added resistor contributes thermal noise at the amplifier input and the value must be kept to a minimum in noise-sensitive applications.

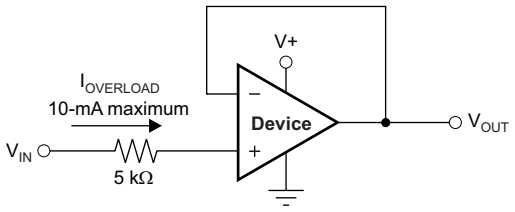


図 40. Input Current Protection

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12 Layout

12.1 Layout Guidelines

For best operational performance of the device, use good printed circuit board (PCB) layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and of the op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is adequate for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces electromagnetic interference (EMI) noise pickup. Take care to physically separate digital and analog grounds, paying attention to the flow of the ground current. For more detailed information, see *Circuit Board Layout Techniques*.
- In order to reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace at a 90 degree angle is much better as opposed to running the traces in parallel with the noisy trace.
- Place the external components as close to the device as possible. As illustrated in 図 42, keeping R_F and R_G close to the inverting input minimizes parasitic capacitance on the inverting input.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit can experience performance shifts resulting from moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low-temperature, post-cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

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12.2 Layout Example

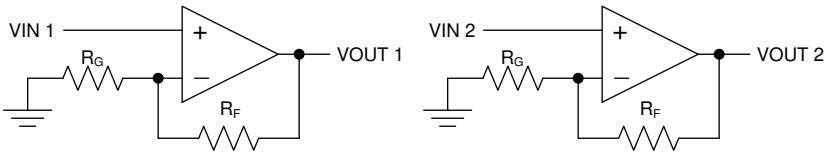


図 41. Schematic Representation for 図 42

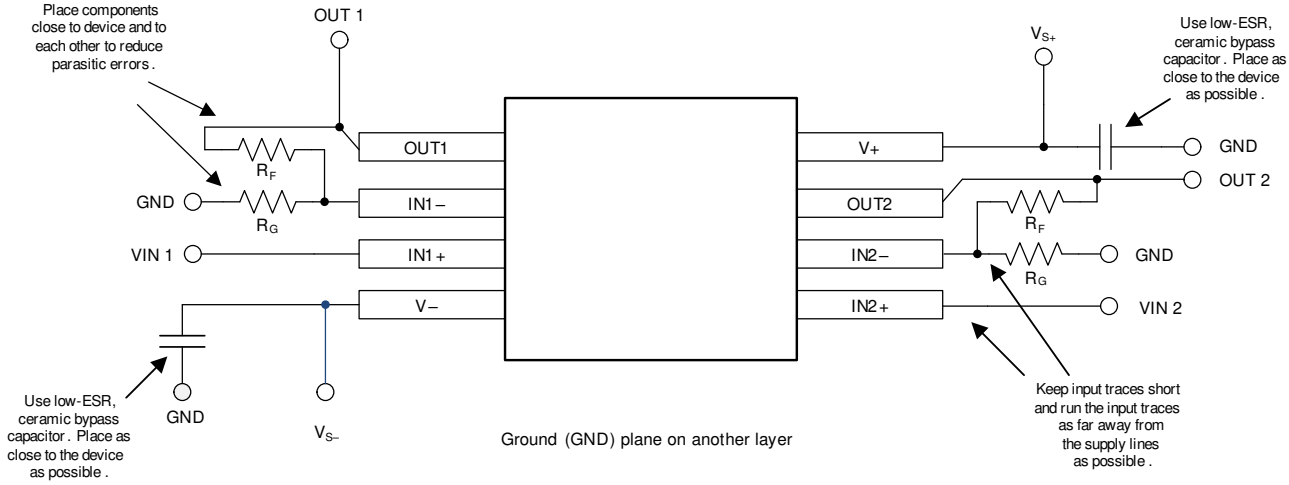


図 42. Layout Example

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13 デバイスおよびドキュメントのサポート

13.1 ドキュメントのサポート

13.1.1 関連資料

テキサス・インスツルメンツ、*『TLVx313 低電力、レール・ツー・レール入出力、オフセット標準値 500µV、1MHz オペアンプ、低コスト・システム用』*

テキサス・インスツルメンツ、*『TLVx314 3MHz、低消費電力、EMIフィルタ内蔵、RRIOオペアンプ』*

テキサス・インスツルメンツ、*『オペアンプのEMI除去率』*

テキサス・インスツルメンツ、*『QFN/SONのPCB実装』*

テキサス・インスツルメンツ、*『クワッド・フラットパック・リード端子なしロジック・パッケージ』*

テキサス・インスツルメンツ、*『回路基板のレイアウト技法』*

テキサス・インスツルメンツ、*『シングル・エンド入力から差動出力への変換回路のリファレンス・デザイン』*

13.2 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 2. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
TLV9061	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TLV9062	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TLV9064	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

13.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

13.4 コミュニティ・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

13.5 商標

E2E is a trademark of Texas Instruments.
Bluetooth is a registered trademark of Bluetooth SIG, Inc.
All other trademarks are the property of their respective owners.

13.6 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TLV9061IDBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	1OAF	Samples
TLV9061IDCKR	ACTIVE	SC70	DCK	5	3000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	1CA	Samples
TLV9061IDPWR	ACTIVE	X2SON	DPW	5	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	CG	Samples
TLV9061SIDBVR	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	1OEF	Samples
TLV9062IDDFR	ACTIVE	SOT-23-THIN	DDF	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T062	Samples
TLV9062IDGKR	ACTIVE	VSSOP	DGK	8	2500	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	T062	Samples
TLV9062IDGKT	ACTIVE	VSSOP	DGK	8	250	RoHS & Green	NIPDAU | SN | NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	T062	Samples
TLV9062IDR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	TL9062	Samples
TLV9062IDSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T062	Samples
TLV9062IDSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T062	Samples
TLV9062IPWR	ACTIVE	TSSOP	PW	8	2000	RoHS & Green	NIPDAU | SN	Level-2-260C-1 YEAR	-40 to 125	TL9062	Samples
TLV9062SIDGSR	ACTIVE	VSSOP	DGS	10	2500	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	1TDX	Samples
TLV9062SIRUGR	ACTIVE	X2QFN	RUG	10	3000	RoHS & Green	NIPDAUAG	Level-2-260C-1 YEAR	-40 to 125	EOF	Samples
TLV9064IDR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TLV9064D	Samples
TLV9064IPWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	TLV9064	Samples
TLV9064IPWT	ACTIVE	TSSOP	PW	14	250	RoHS & Green	SN	Level-2-260C-1 YEAR	-40 to 125	TLV9064	Samples
TLV9064IRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9064	Samples
TLV9064IRUCR	ACTIVE	QFN	RUC	14	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	1DD	Samples
TLV9064SIRTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	T9064S	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TLV9061, TLV9062, TLV9064 :

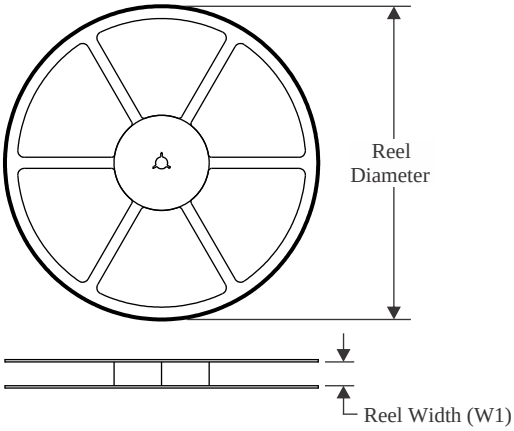
- Automotive : TLV9061-Q1, TLV9062-Q1, TLV9064-Q1

NOTE: Qualified Version Definitions:

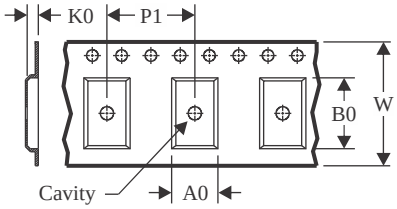
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

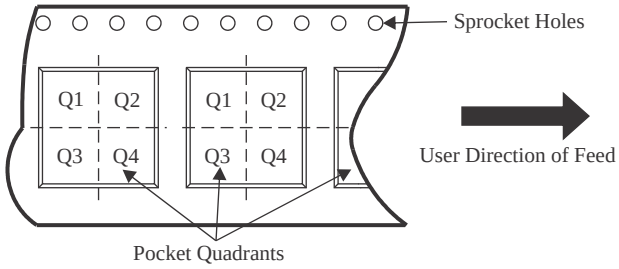


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

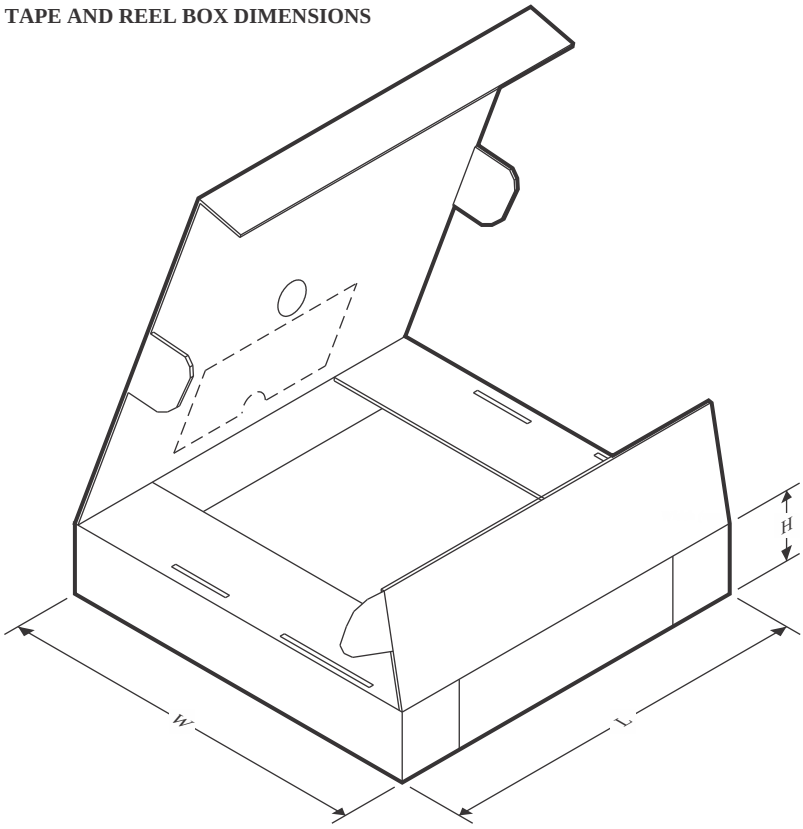


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9061IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9061IDBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9061IDCKR	SC70	DCK	5	3000	180.0	8.4	2.3	2.5	1.2	4.0	8.0	Q3
TLV9061IDPWR	X2SON	DPW	5	3000	178.0	8.4	0.91	0.91	0.5	2.0	8.0	Q2
TLV9061SIDBVR	SOT-23	DBV	6	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9062IDDFR	SOT-23-THIN	DDF	8	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TLV9062IDGKR	VSSOP	DGK	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9062IDGKT	VSSOP	DGK	8	250	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9062IDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TLV9062IDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV9062IDSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TLV9062IPWR	TSSOP	PW	8	2000	330.0	12.4	7.0	3.6	1.6	8.0	12.0	Q1
TLV9062SIDGSR	VSSOP	DGS	10	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TLV9062SIRUGR	X2QFN	RUG	10	3000	178.0	8.4	1.75	2.25	0.56	4.0	8.0	Q1
TLV9064IDR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TLV9064IPWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV9064IPWT	TSSOP	PW	14	250	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TLV9064IRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TLV9064IRUCR	QFN	RUC	14	3000	180.0	9.5	2.16	2.16	0.5	4.0	8.0	Q2
TLV9064SIRTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9061IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV9061IDBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TLV9061IDCKR	SC70	DCK	5	3000	210.0	185.0	35.0
TLV9061IDPWR	X2SON	DPW	5	3000	205.0	200.0	33.0
TLV9061SIDBVR	SOT-23	DBV	6	3000	210.0	185.0	35.0
TLV9062IDDFR	SOT-23-THIN	DDF	8	3000	210.0	185.0	35.0
TLV9062IDGKR	VSSOP	DGK	8	2500	356.0	356.0	35.0
TLV9062IDGKT	VSSOP	DGK	8	250	356.0	356.0	35.0
TLV9062IDR	SOIC	D	8	2500	356.0	356.0	35.0
TLV9062IDSGR	WSON	DSG	8	3000	210.0	185.0	35.0
TLV9062IDSGT	WSON	DSG	8	250	210.0	185.0	35.0
TLV9062IPWR	TSSOP	PW	8	2000	356.0	356.0	35.0
TLV9062SIDGSR	VSSOP	DGS	10	2500	366.0	364.0	50.0
TLV9062SIRUGR	X2QFN	RUG	10	3000	205.0	200.0	33.0
TLV9064IDR	SOIC	D	14	2500	356.0	356.0	35.0
TLV9064IPWR	TSSOP	PW	14	2000	366.0	364.0	50.0
TLV9064IPWT	TSSOP	PW	14	250	366.0	364.0	50.0
TLV9064IRTER	WQFN	RTE	16	3000	367.0	367.0	35.0

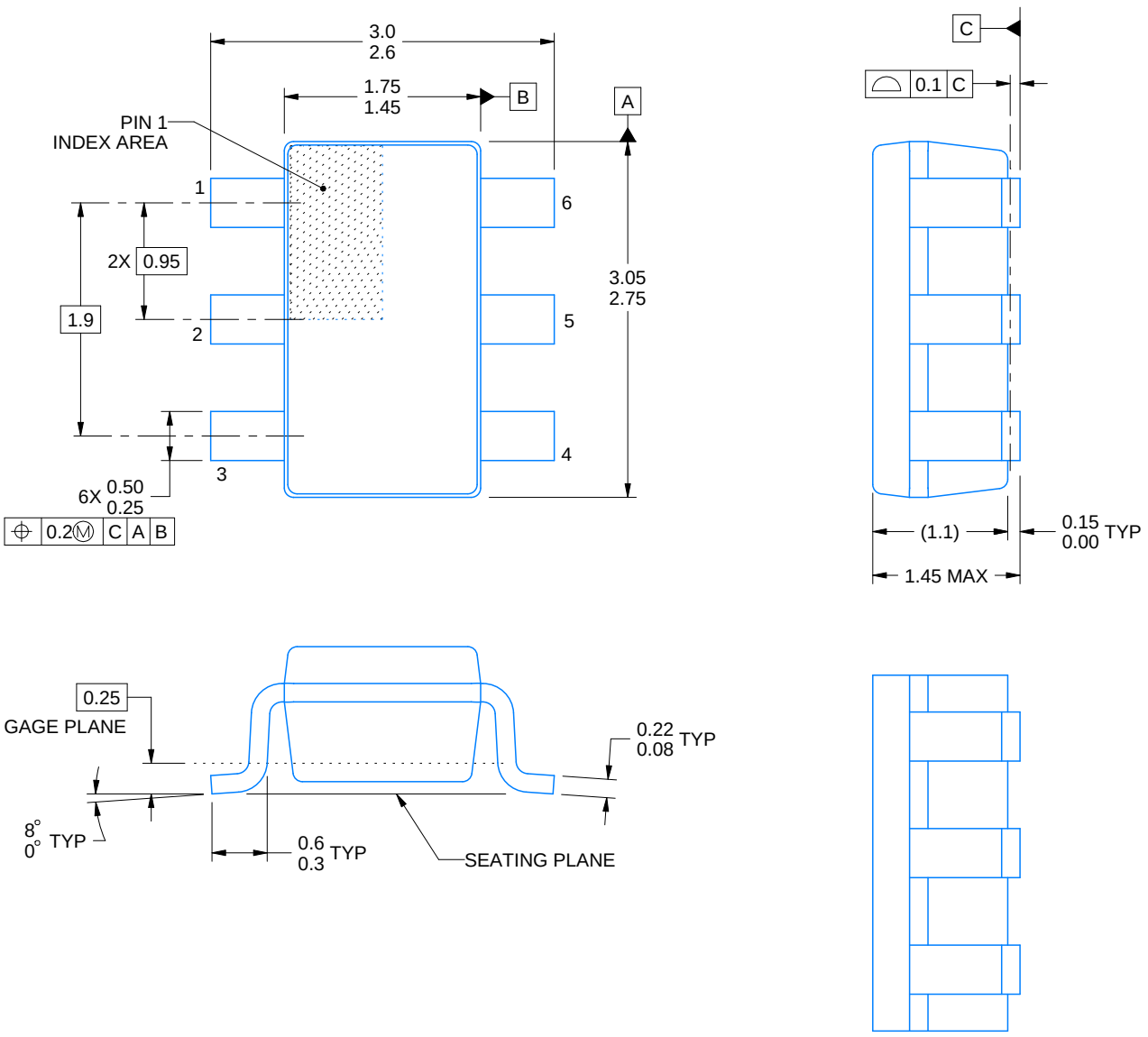
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TLV9064IRUCR	QFN	RUC	14	3000	205.0	200.0	30.0
TLV9064SIRTER	WQFN	RTE	16	3000	367.0	367.0	35.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

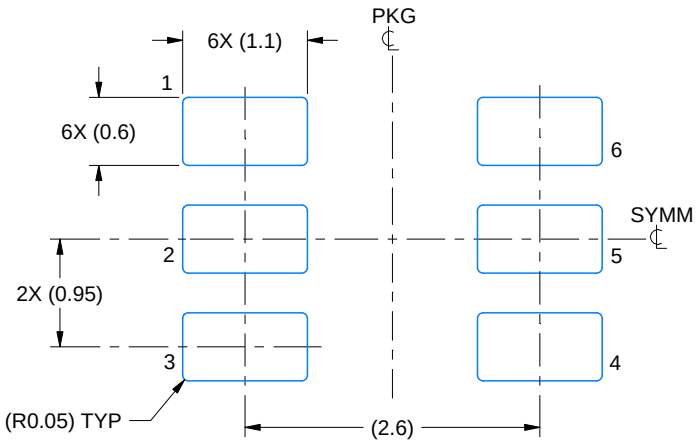


ALTERNATIVE PACKAGE SINGULATION VIEW

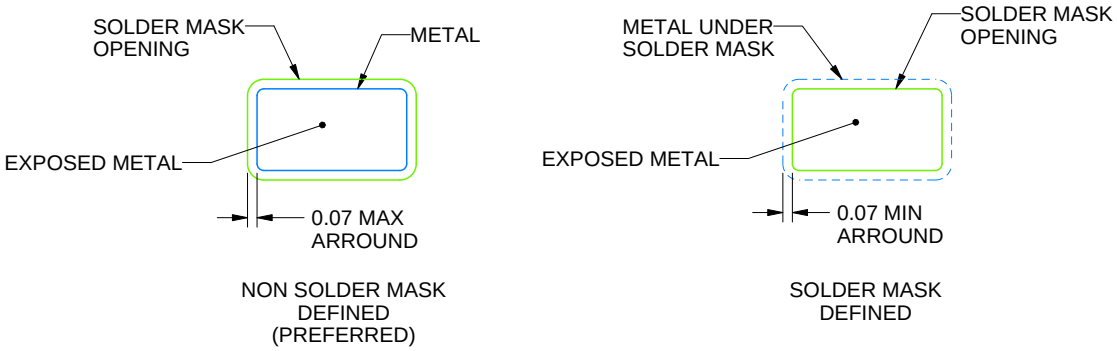
4214840/E 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

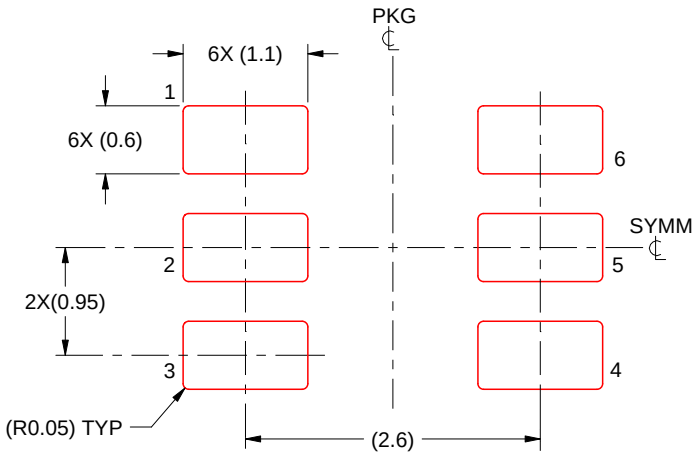


SOLDER MASK DETAILS

4214840/E 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/E 02/2024

NOTES: (continued)

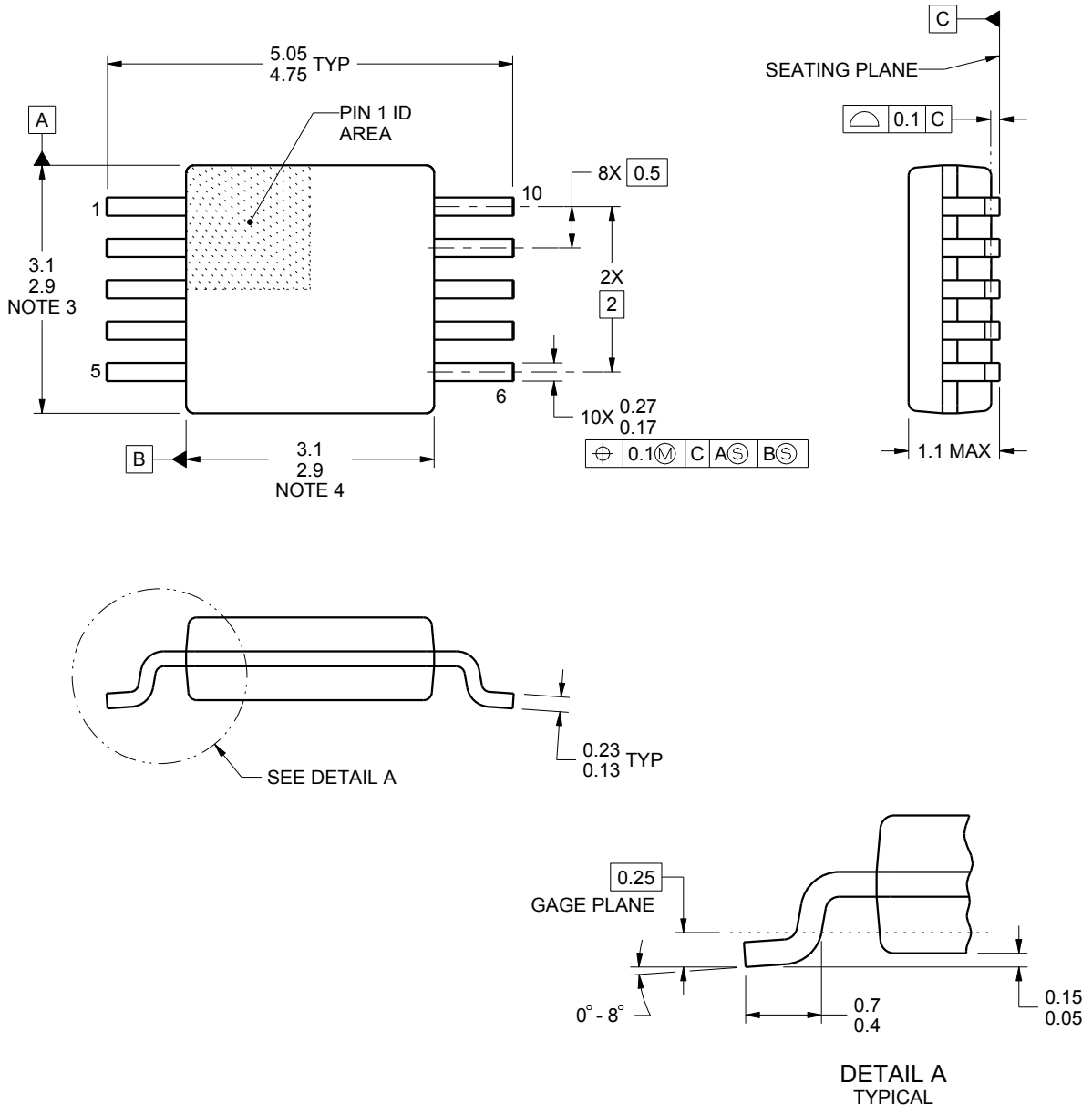
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DGS0010A

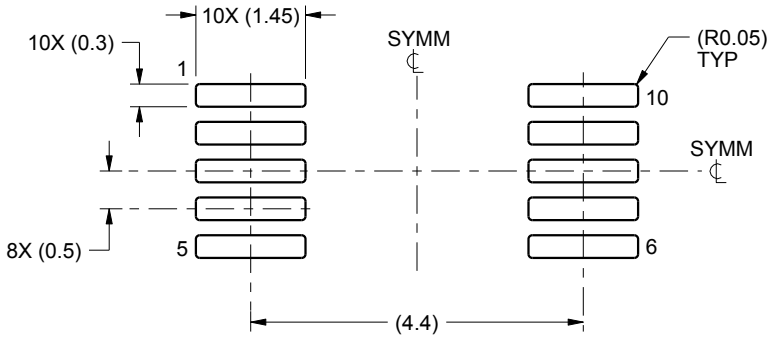
VSSOP - 1.1 mm max height

SMALL OUTLINE PACKAGE

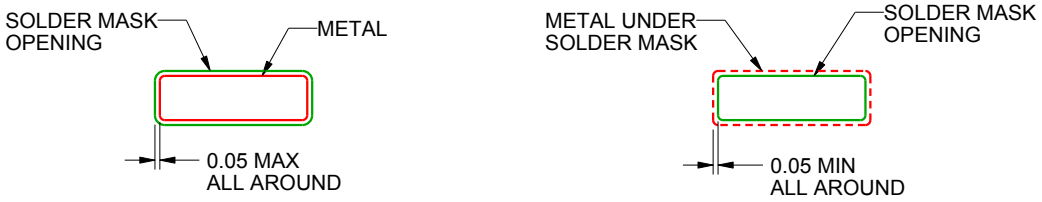


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187, variation BA.



LAND PATTERN EXAMPLE
SCALE:10X

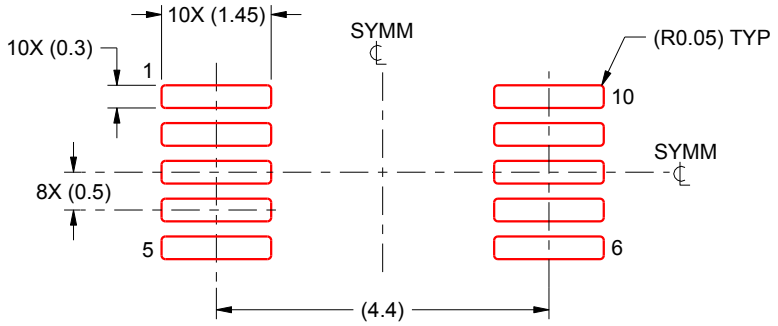


SOLDER MASK DETAILS
NOT TO SCALE

4221984/A 05/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221984/A 05/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DPW 5 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

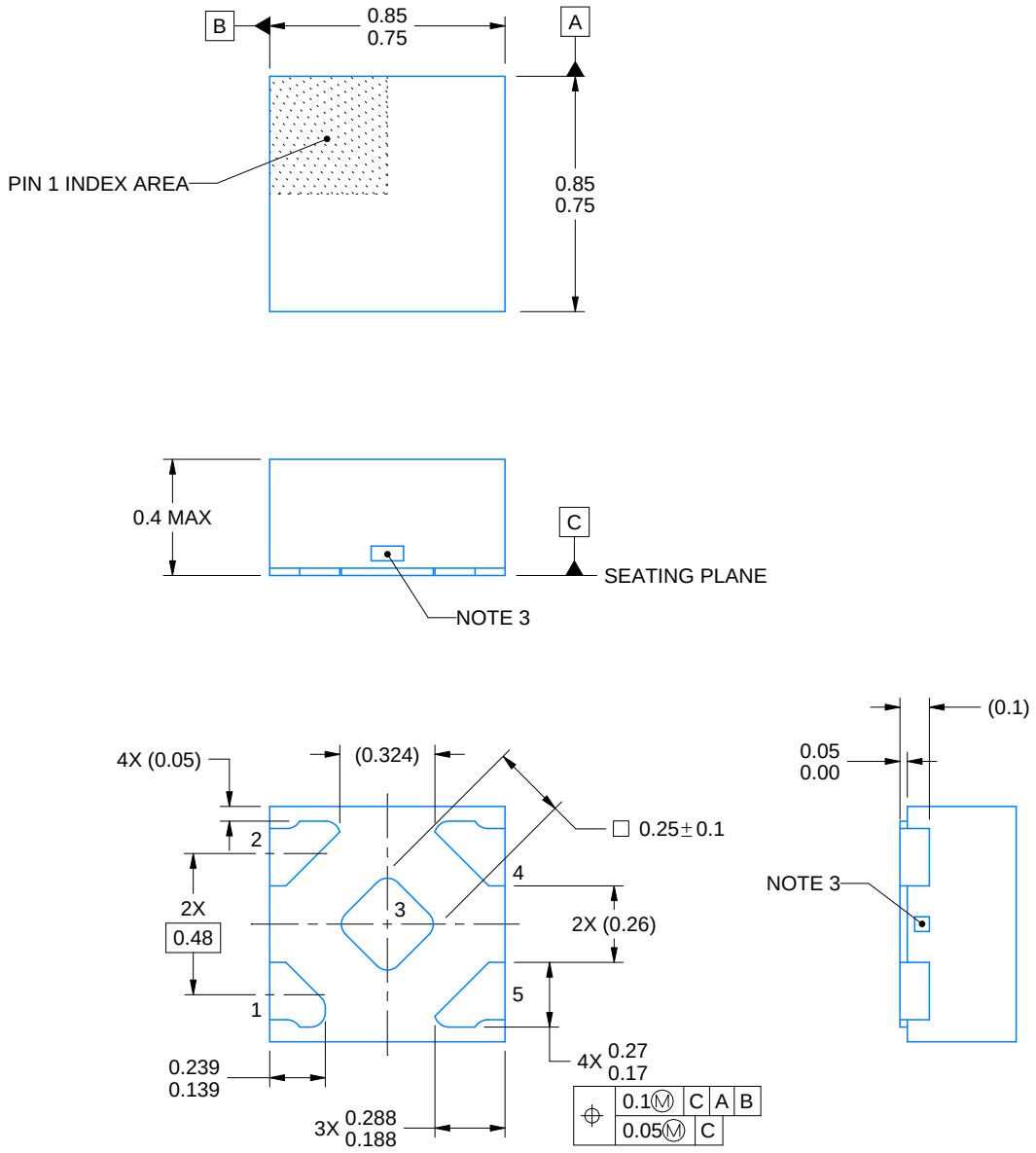
4211218-3/D

PACKAGE OUTLINE

DPW0005A

X2SON - 0.4 mm max height

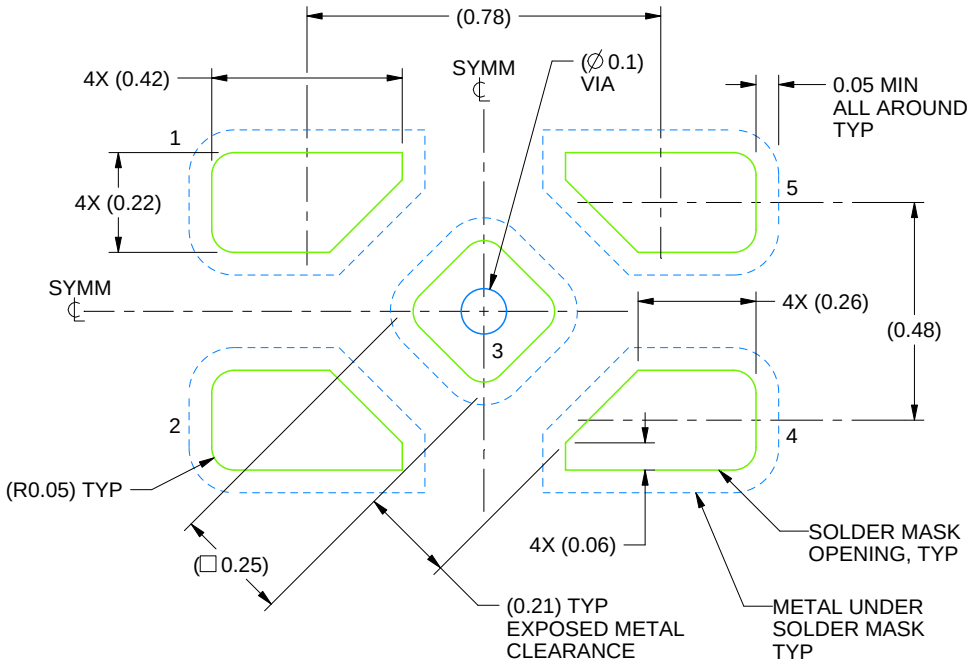
PLASTIC SMALL OUTLINE - NO LEAD



4223102/D 03/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The size and shape of this feature may vary.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

4223102/D 03/2022

NOTES: (continued)

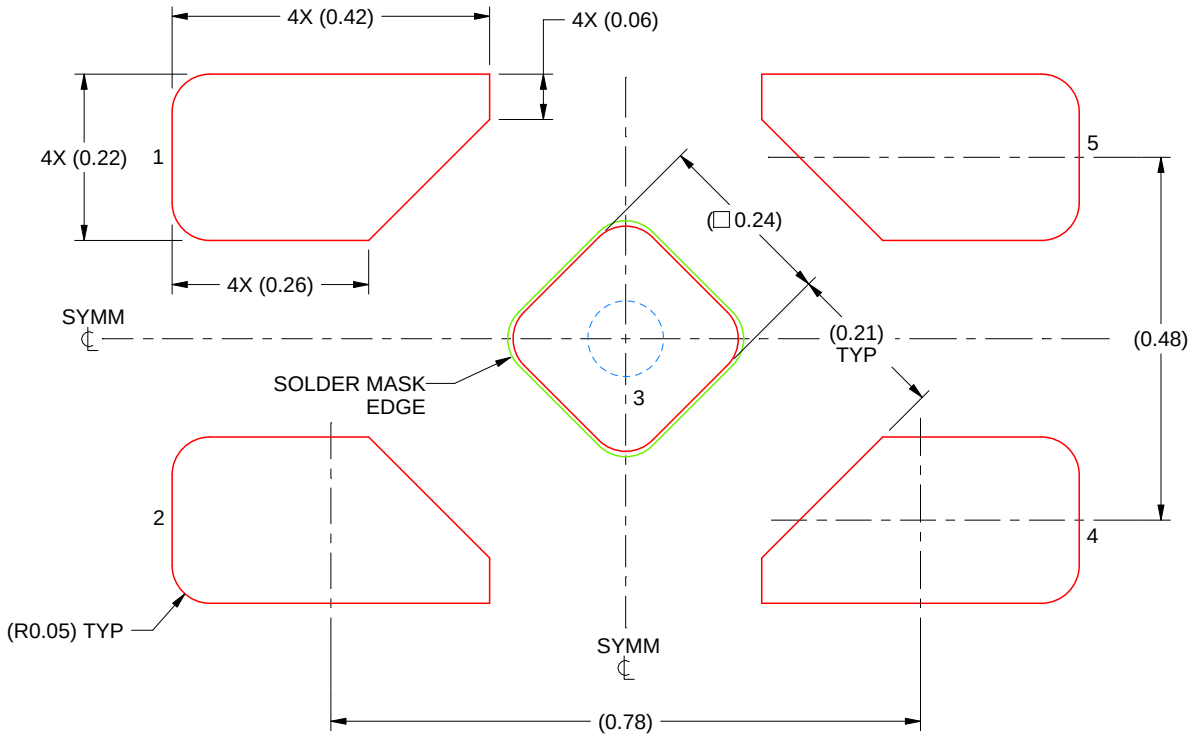
4. This package is designed to be soldered to a thermal pad on the board. For more information, refer to QFN/SON PCB application note in literature No. SLUA271 (www.ti.com/lit/slua271).

EXAMPLE STENCIL DESIGN

DPW0005A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 3
92% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:100X

4223102/D 03/2022

NOTES: (continued)

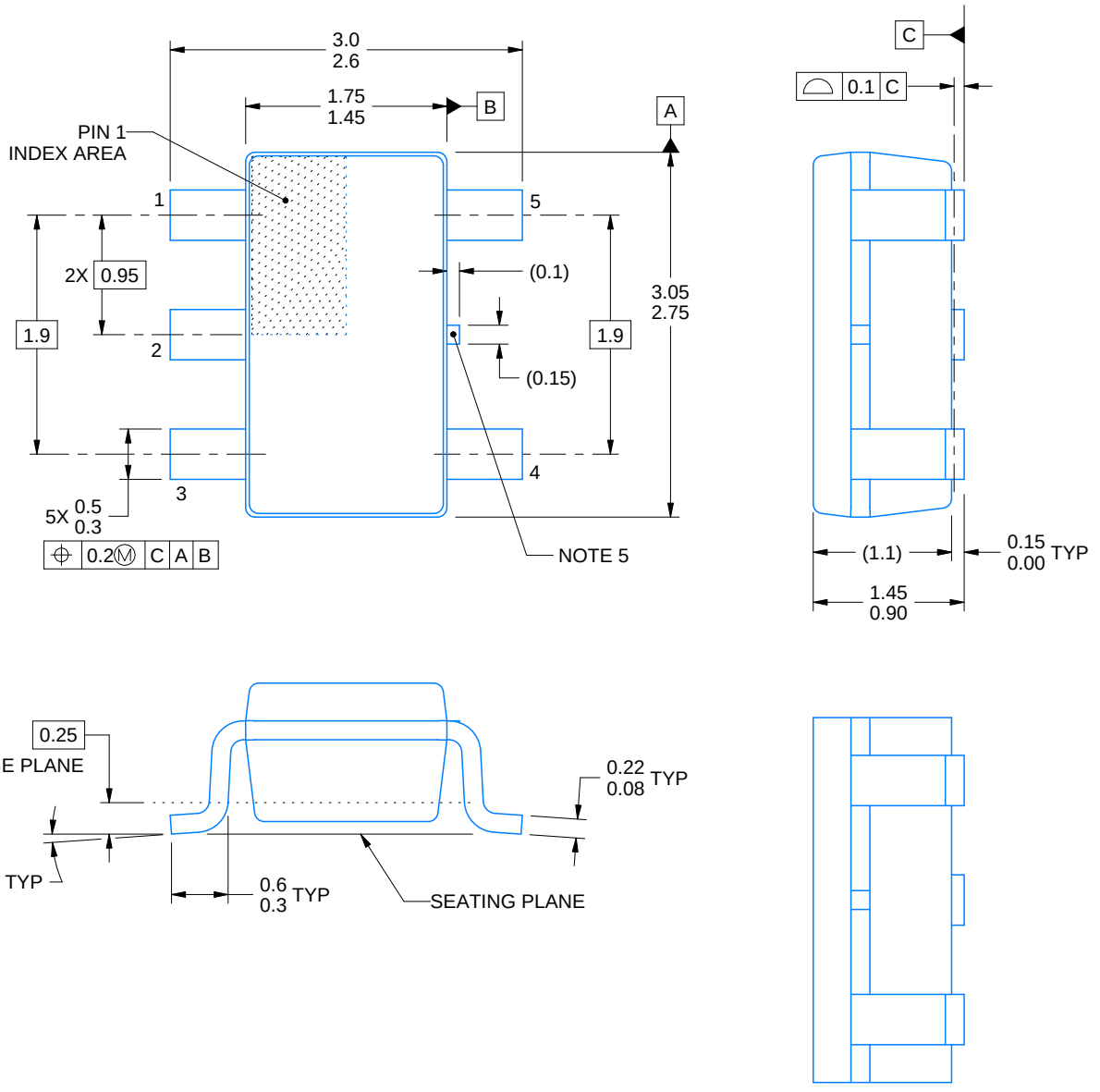
5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

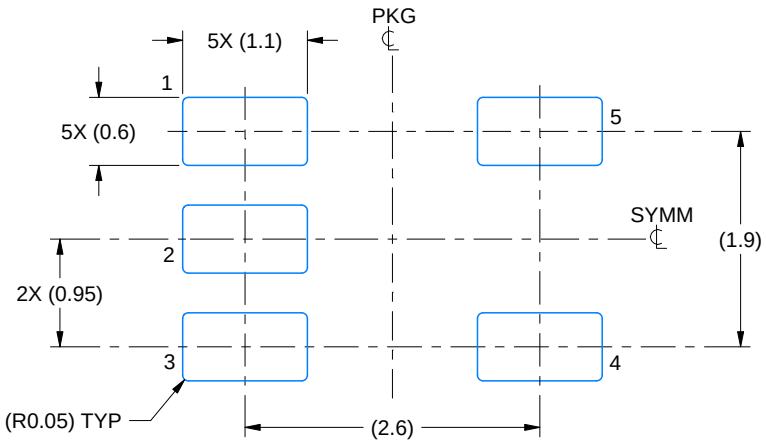


ALTERNATIVE PACKAGE SINGULATION VIEW

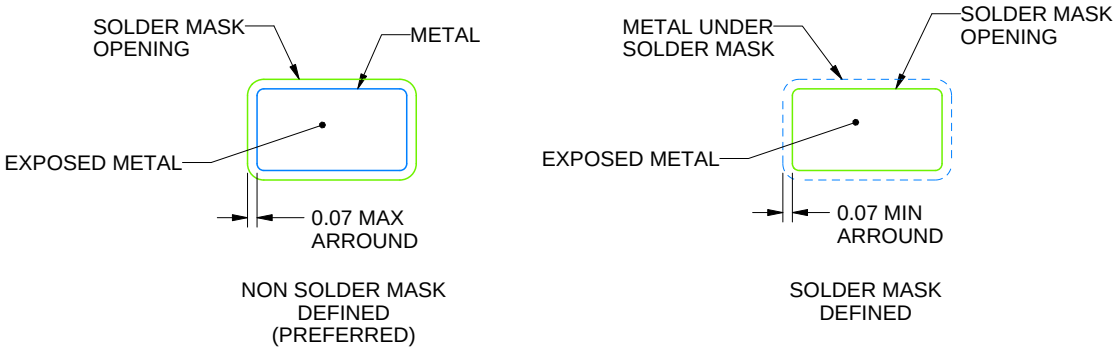
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

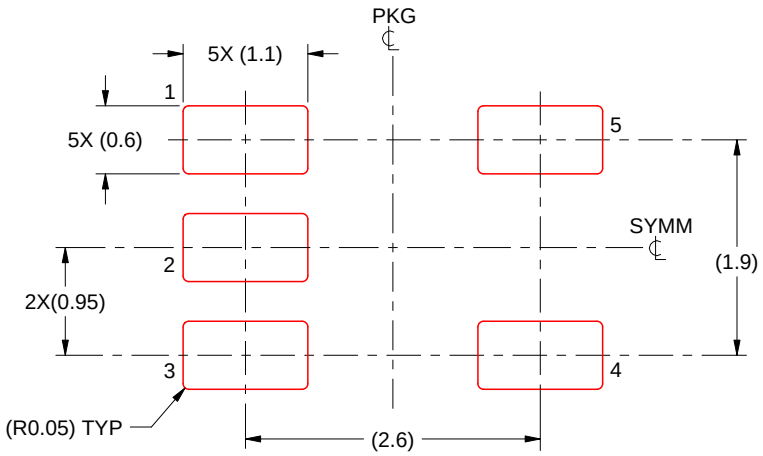


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

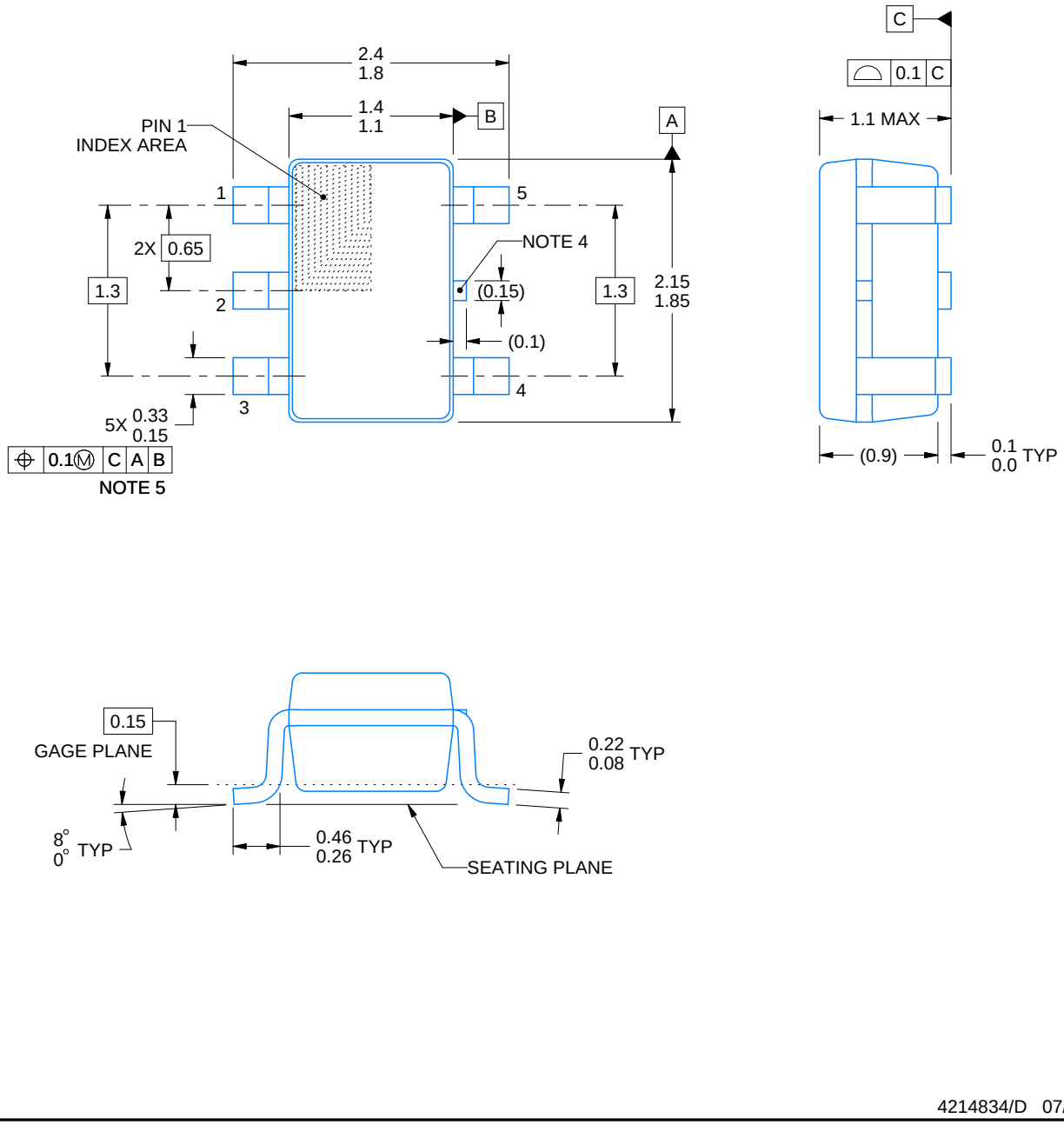
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

DCK0005A

SOT - 1.1 max height

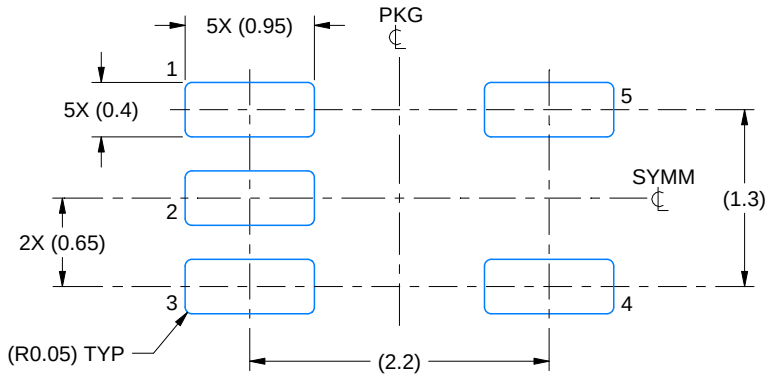
SMALL OUTLINE TRANSISTOR



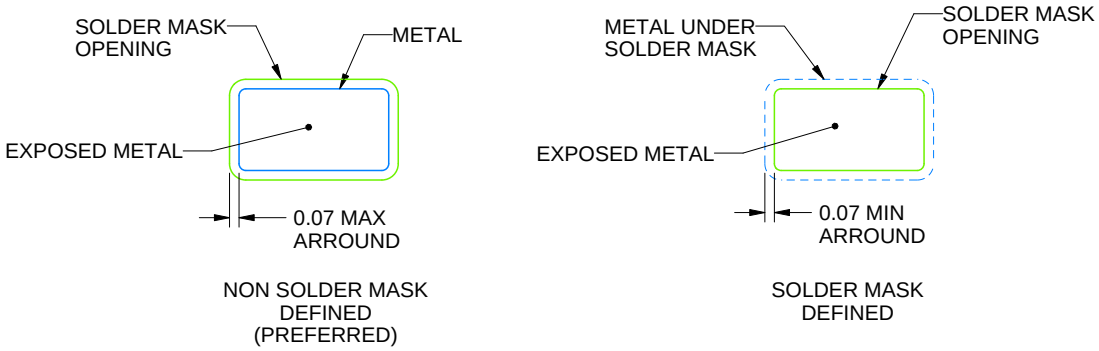
4214834/D 07/2023

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

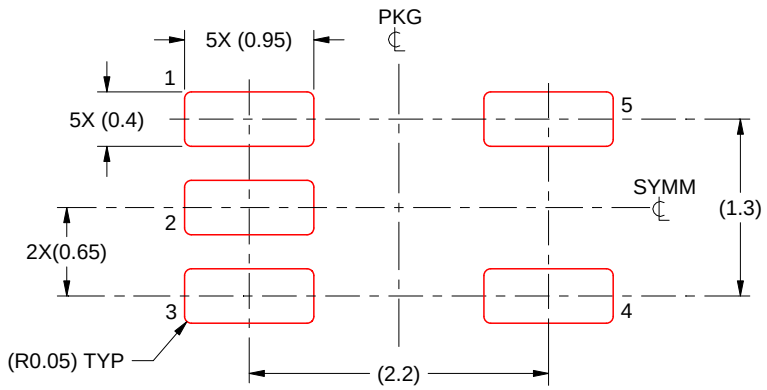


SOLDER MASK DETAILS

4214834/D 07/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



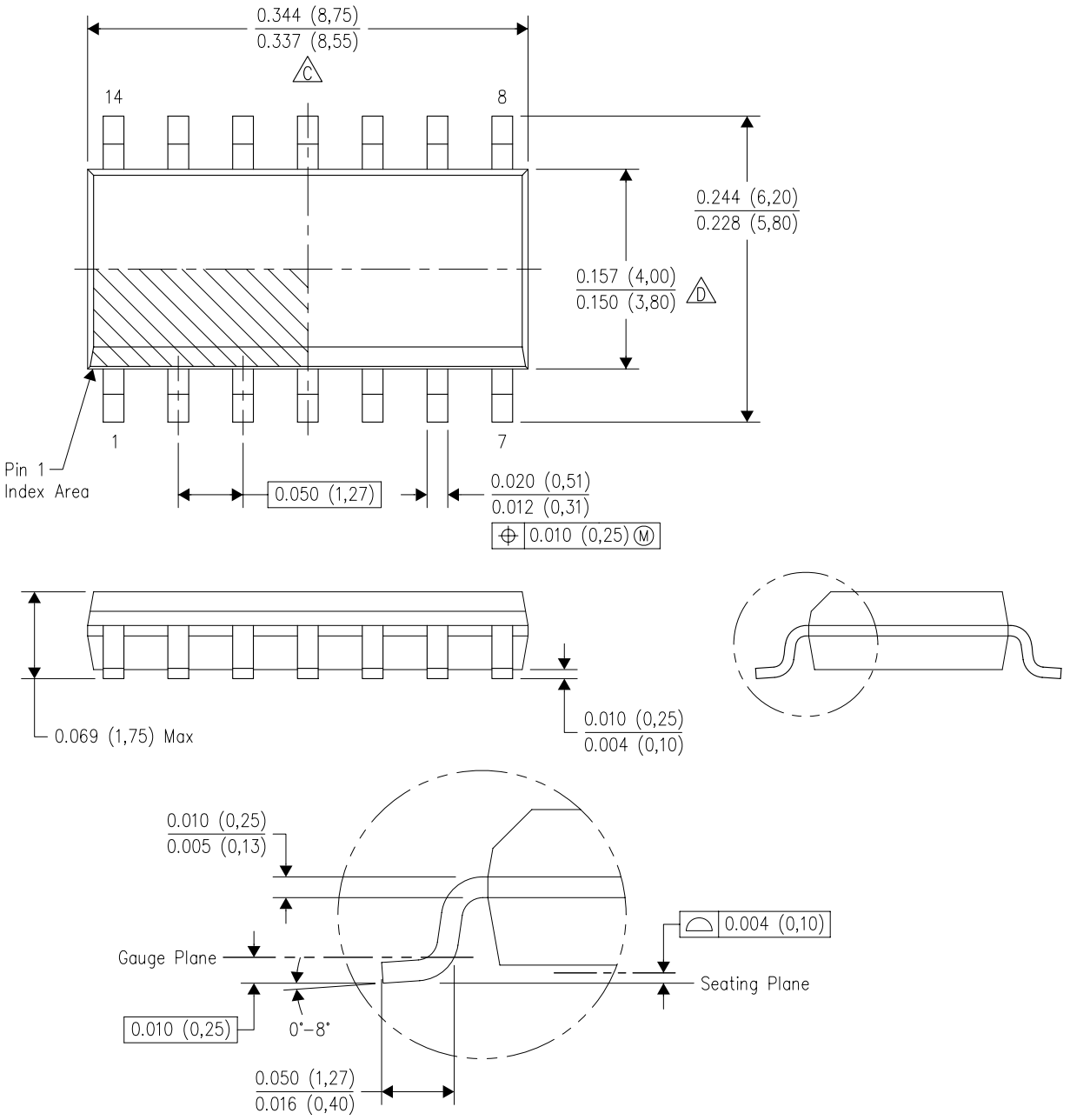
SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/D 07/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

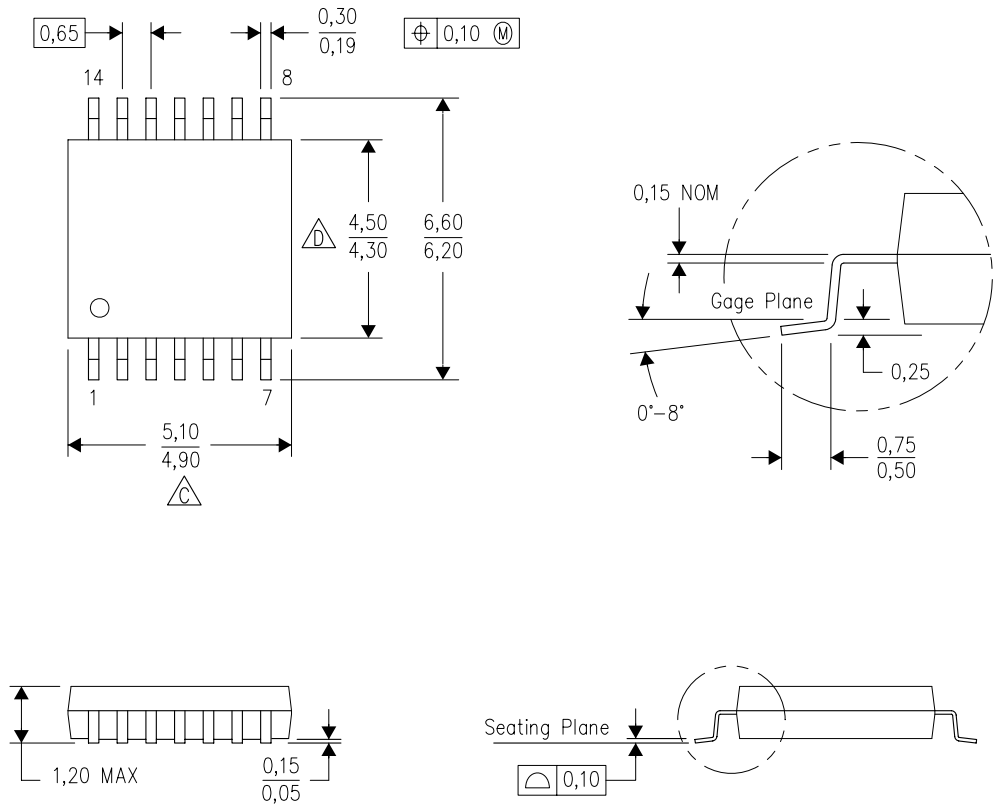
D (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040047–5/M 06/11

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AB.

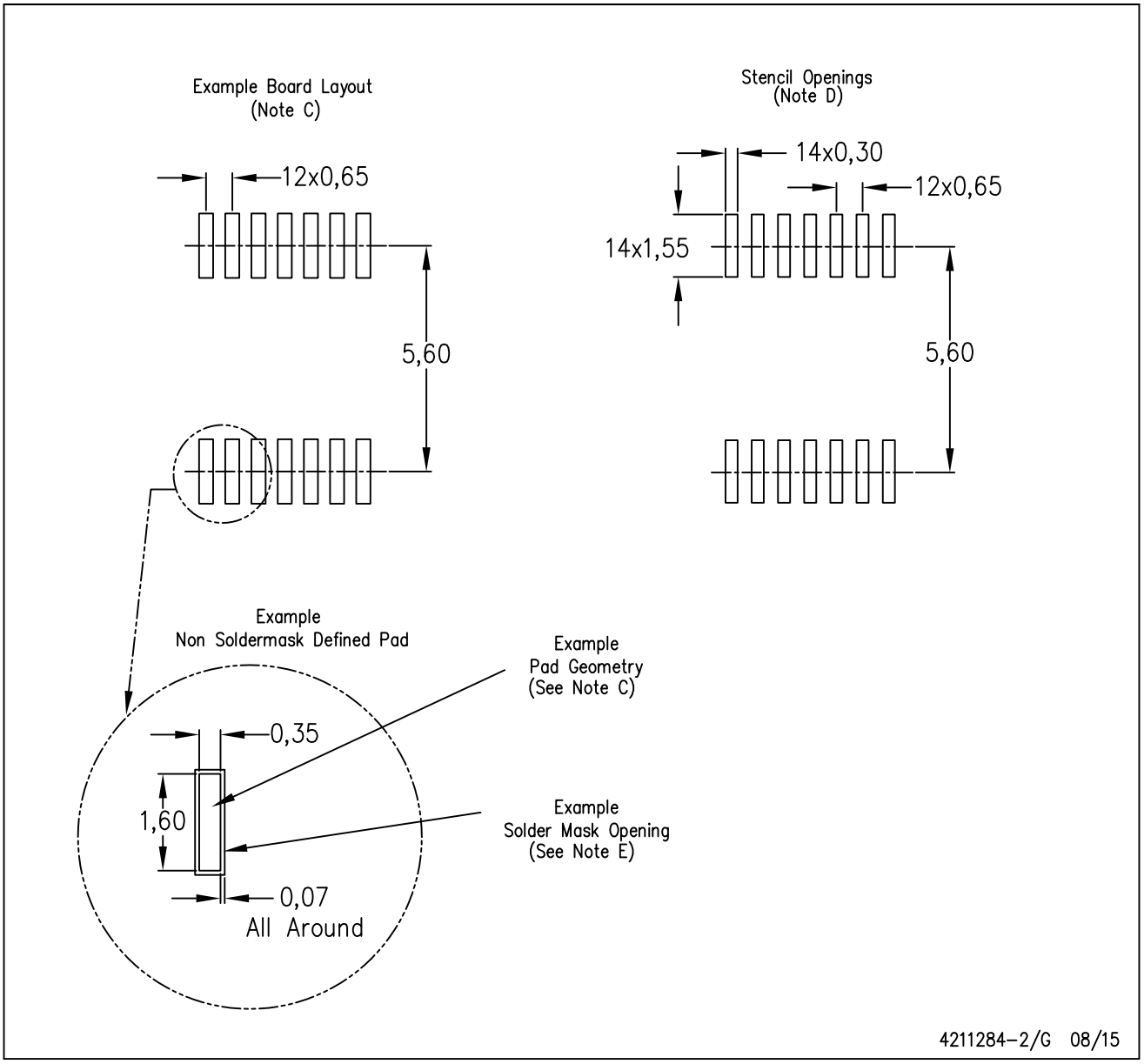
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

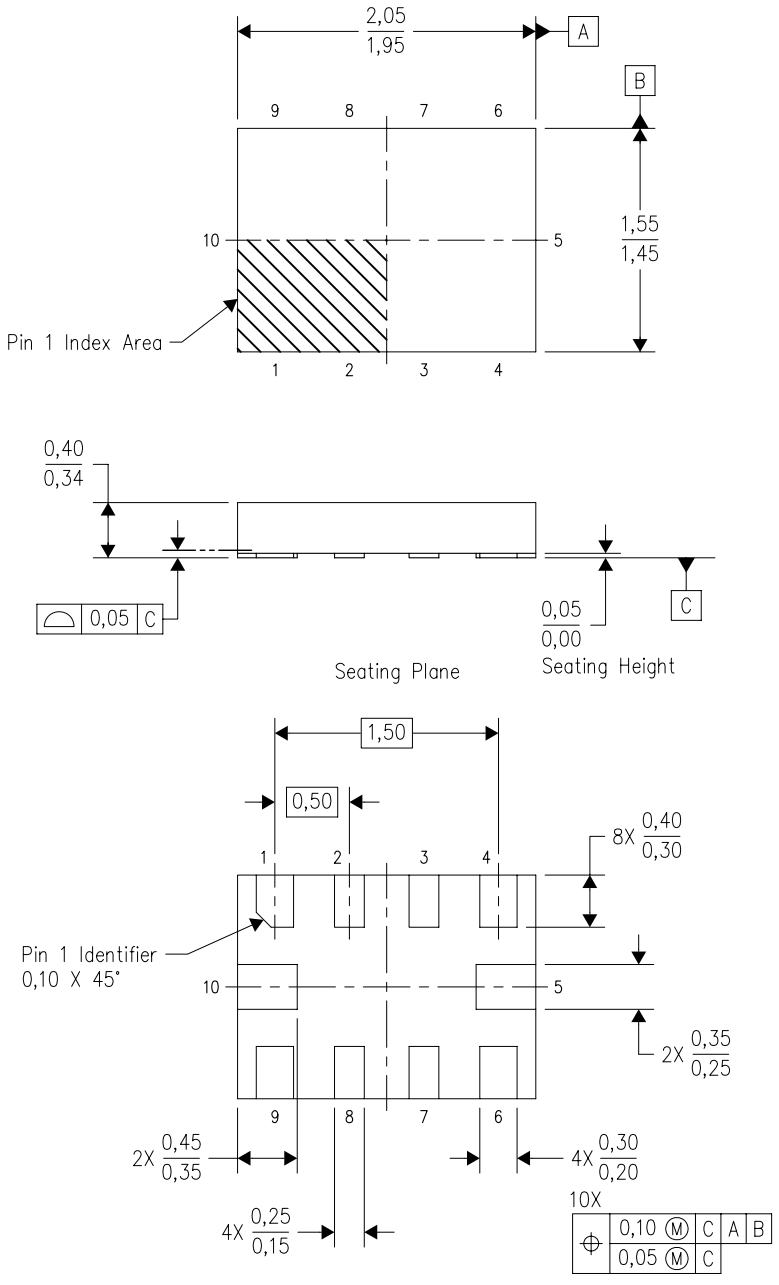
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

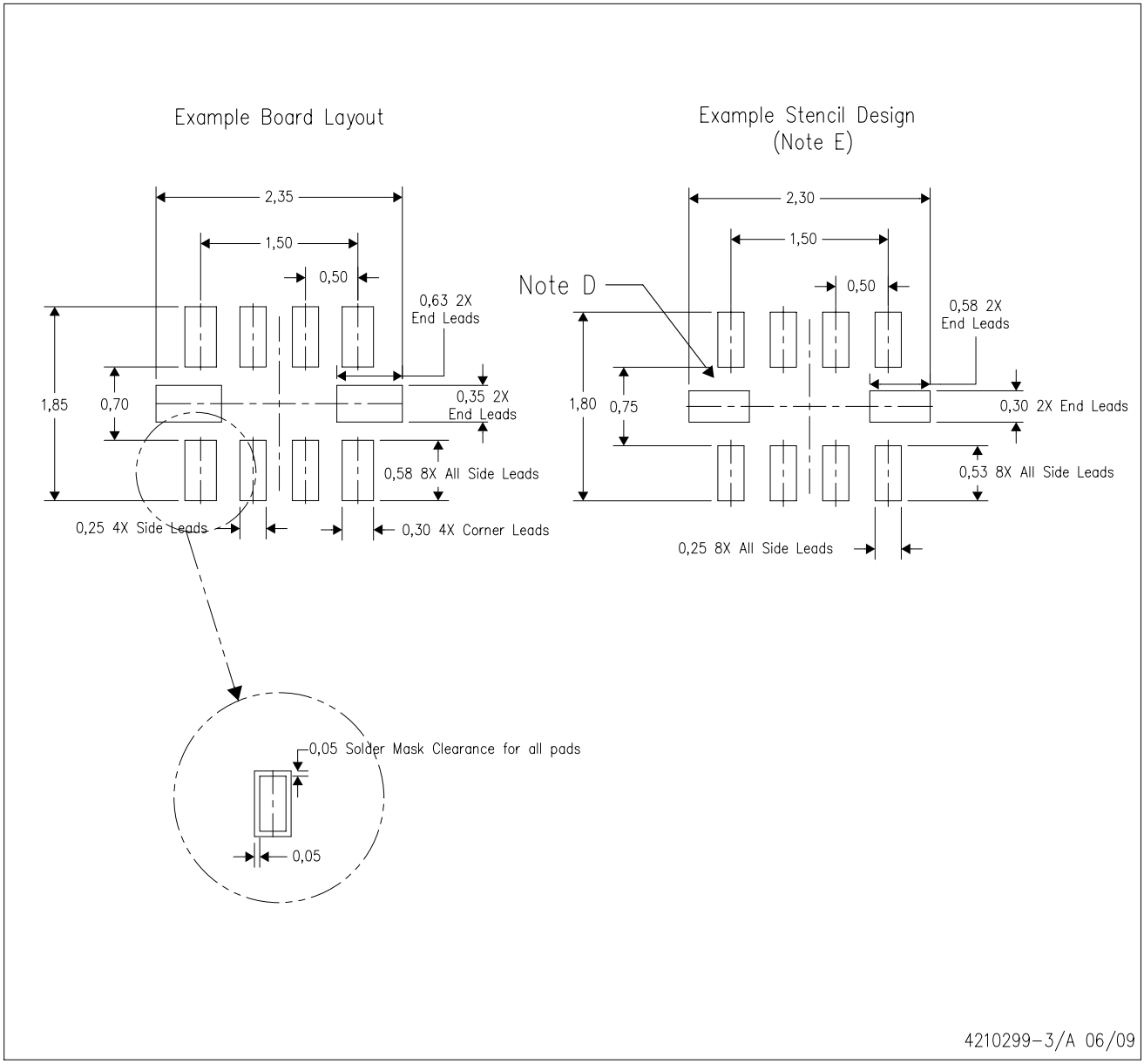
RUG (R–PQFP–N10) PLASTIC QUAD FLATPACK



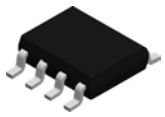
4208528–3/B 04/2008

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–Lead) package configuration.
D. This package complies to JEDEC MO–288 variation X2EFD.

RUG (R–PQFP–N10)



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

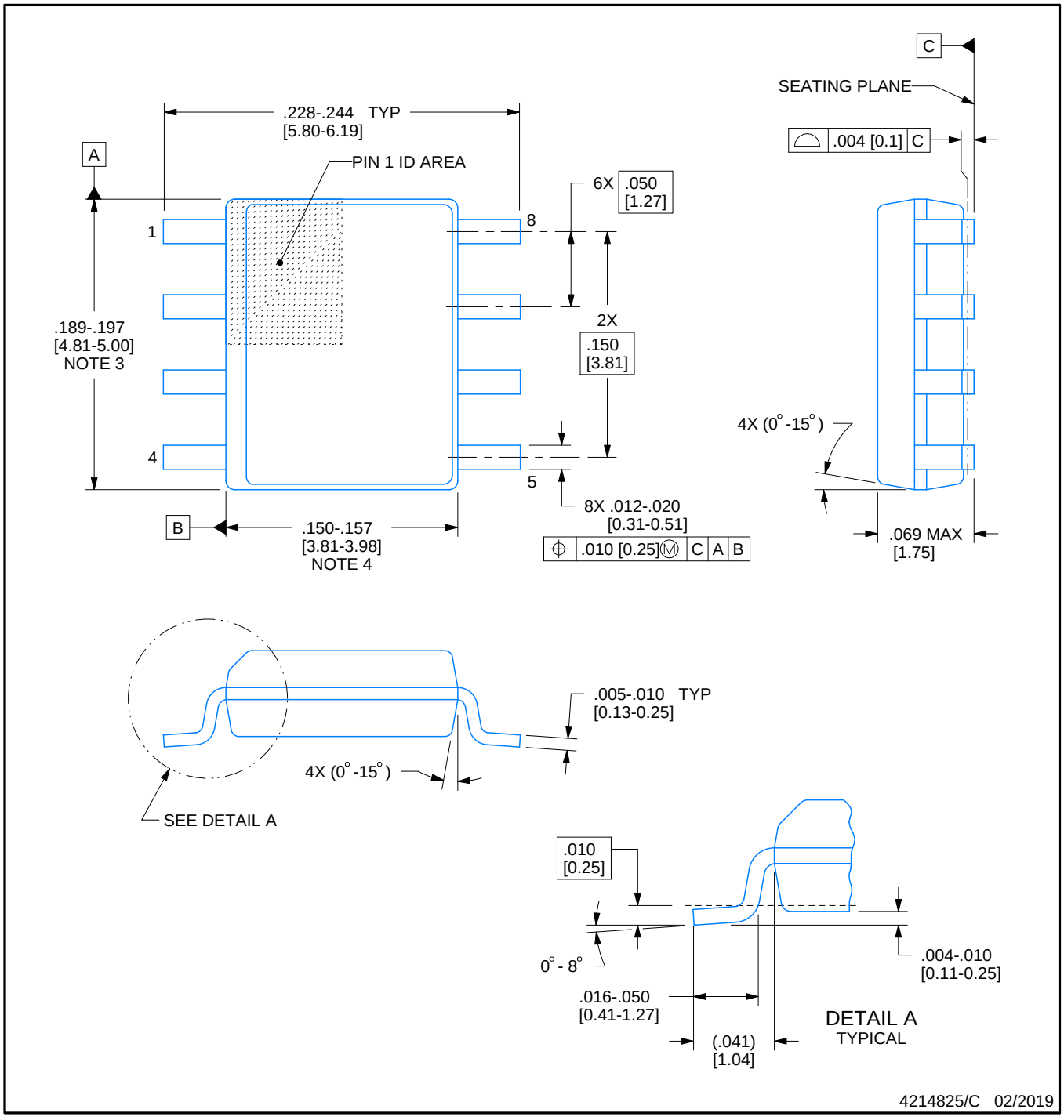


PACKAGE OUTLINE

D0008A

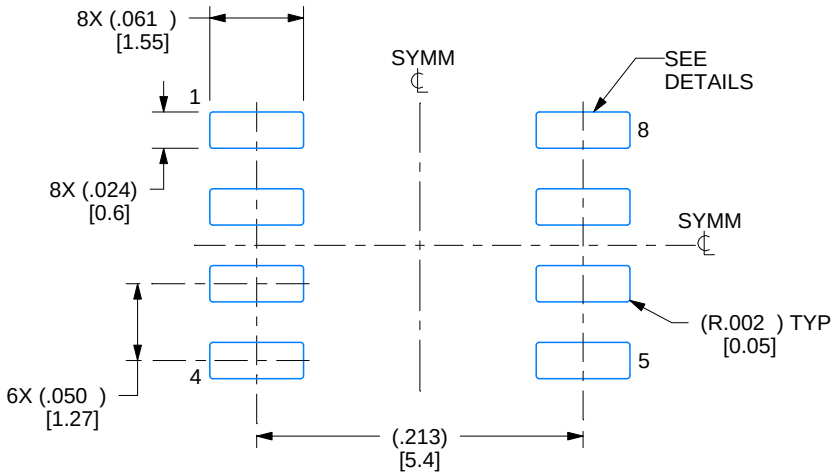
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

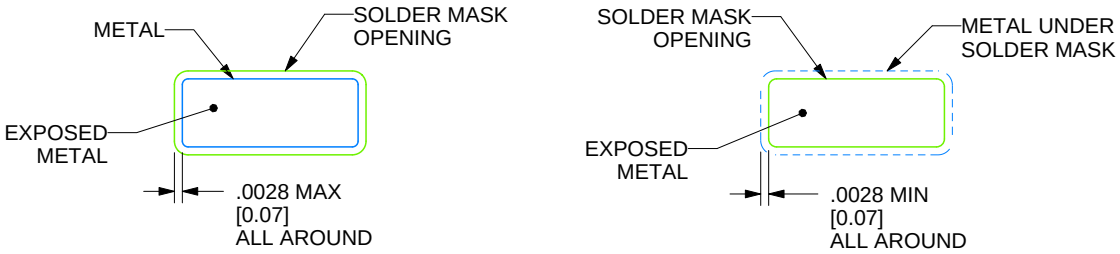


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

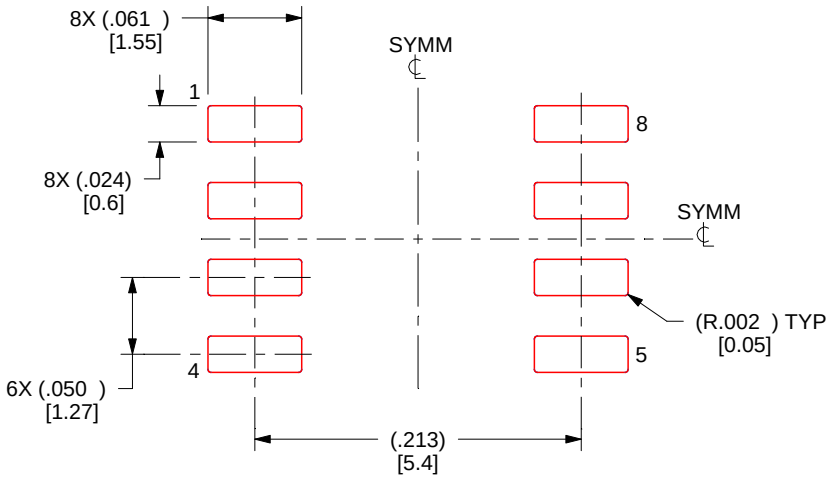
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



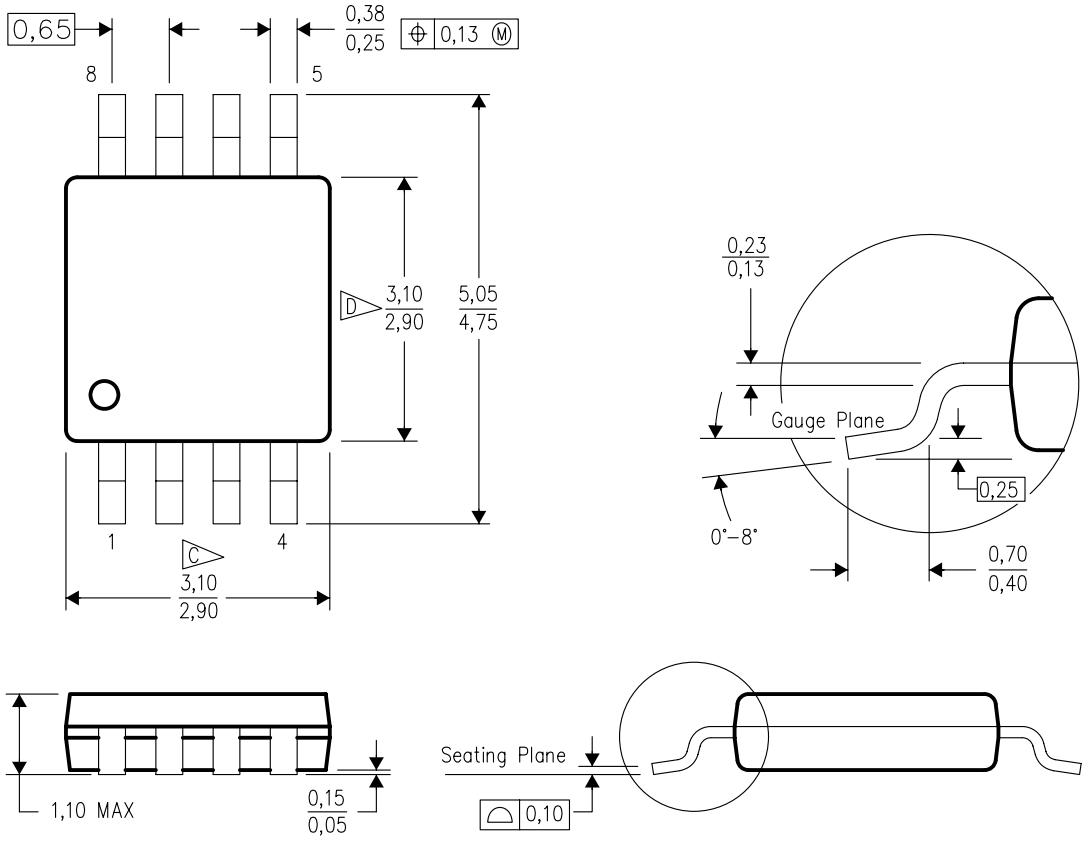
SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

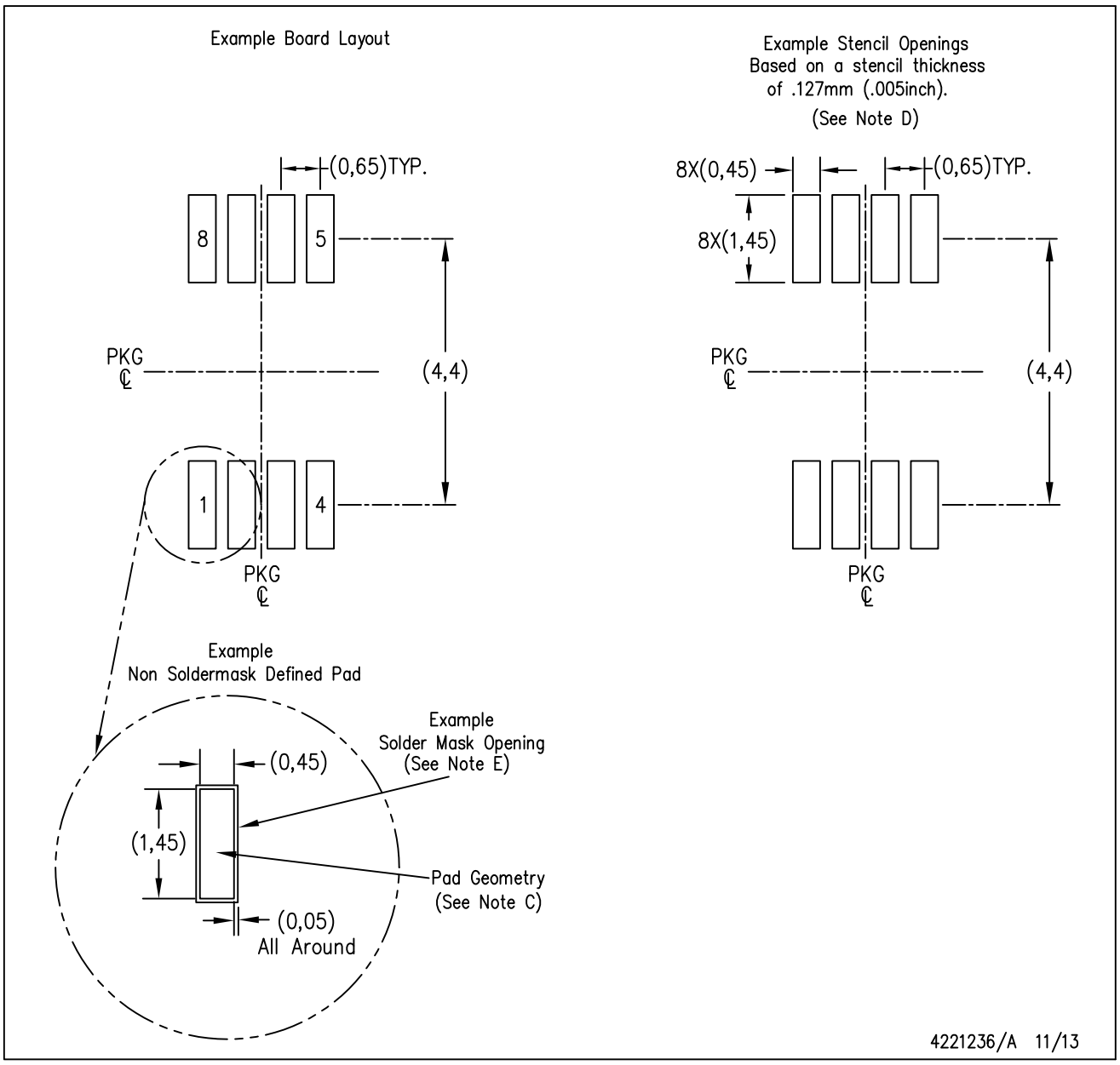
DGK (S–PDSO–G8) PLASTIC SMALL–OUTLINE PACKAGE



4073329/E 05/06

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per end.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
E. Falls within JEDEC MO–187 variation AA, except interlead flash.

DGK (S–PDSO–G8) PLASTIC SMALL OUTLINE PACKAGE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

GENERIC PACKAGE VIEW

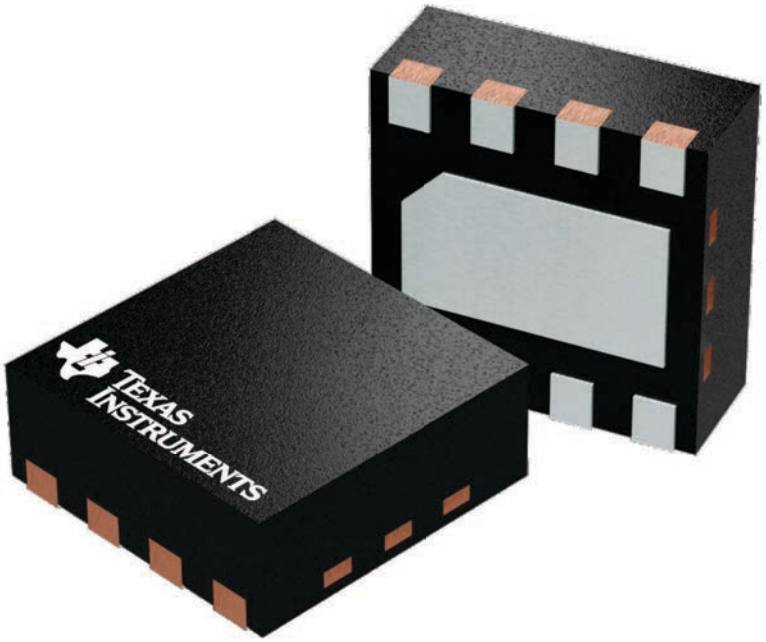
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



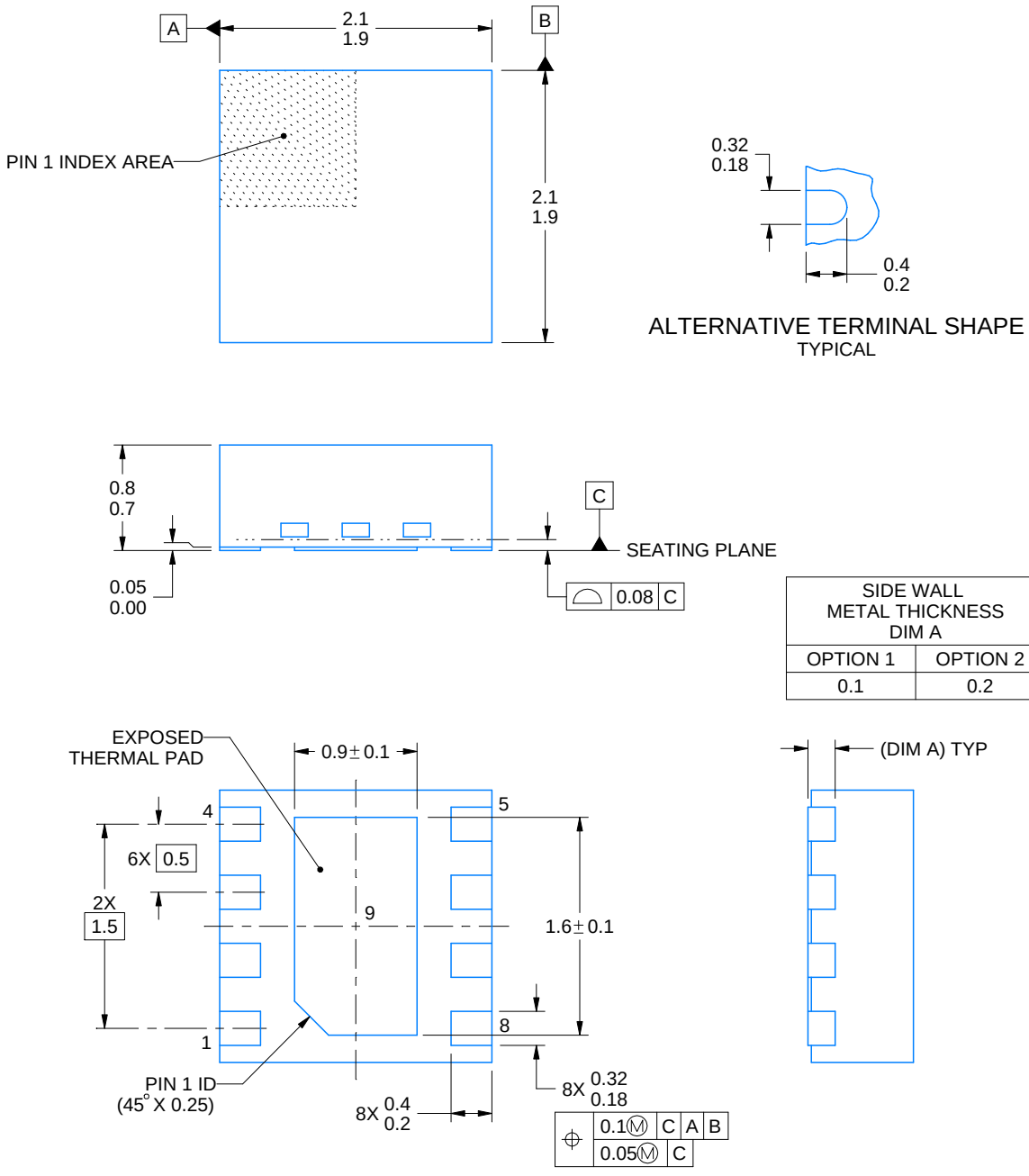
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

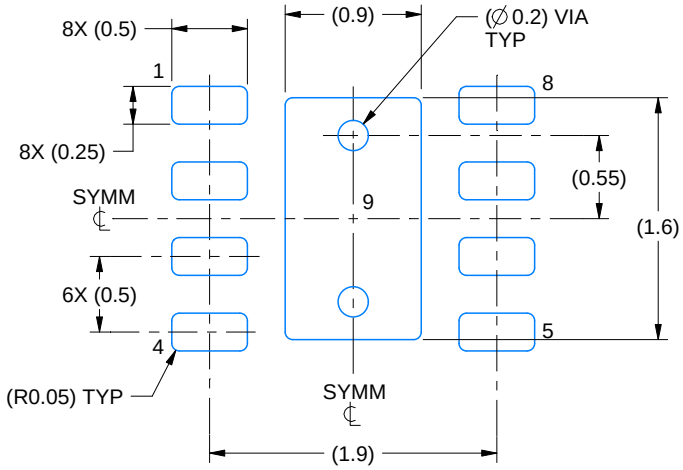
PLASTIC SMALL OUTLINE - NO LEAD



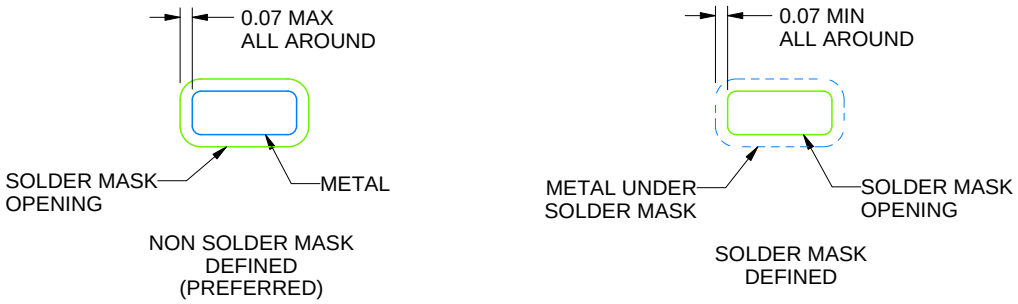
4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

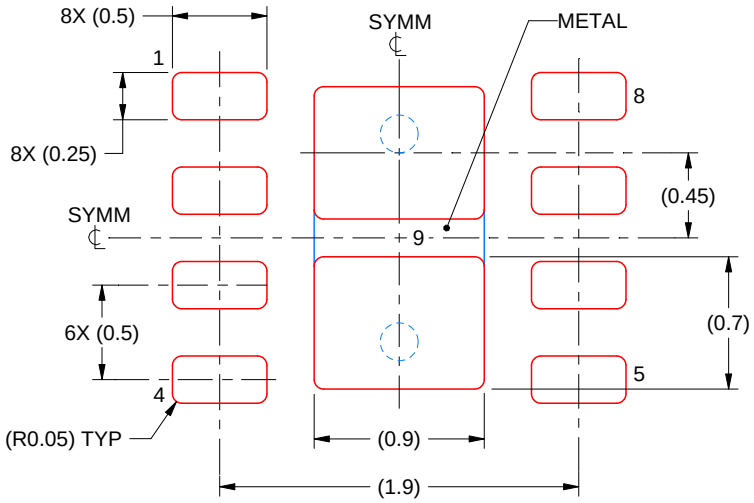


SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

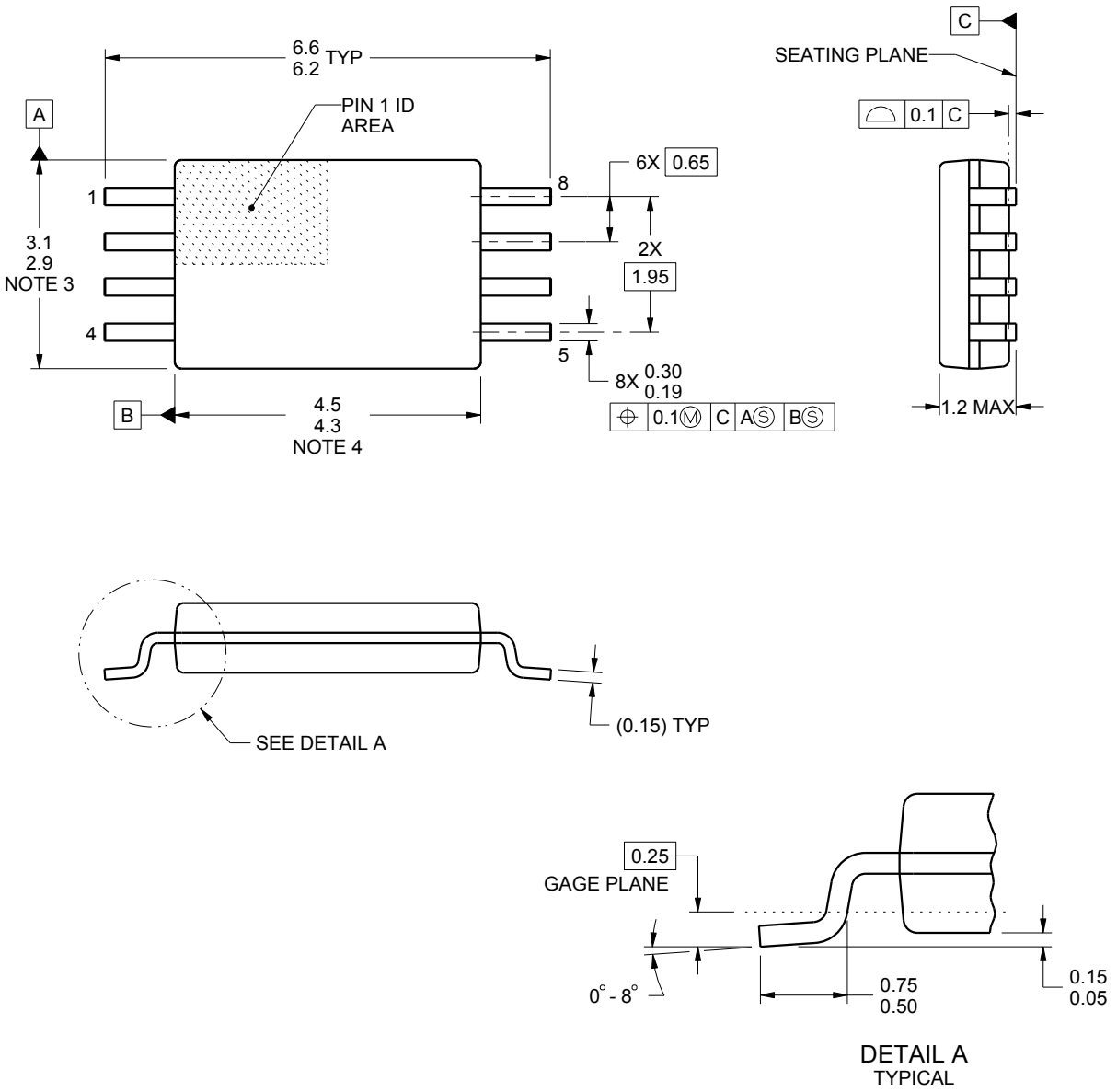
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

PW0008A

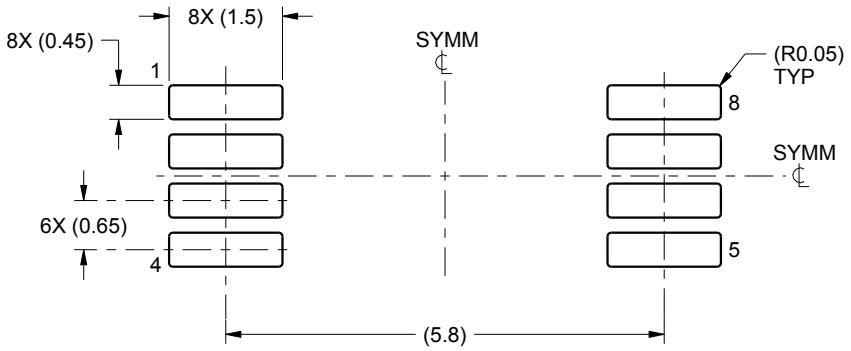
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

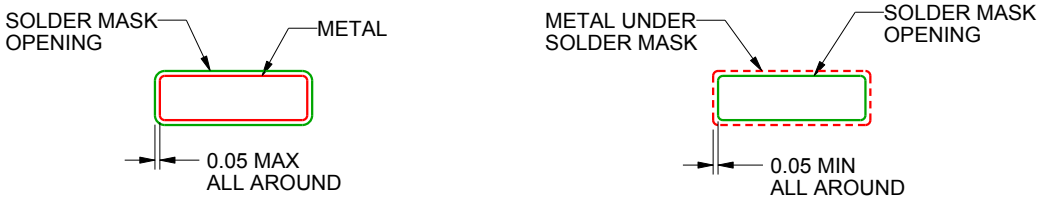


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.



LAND PATTERN EXAMPLE
SCALE:10X

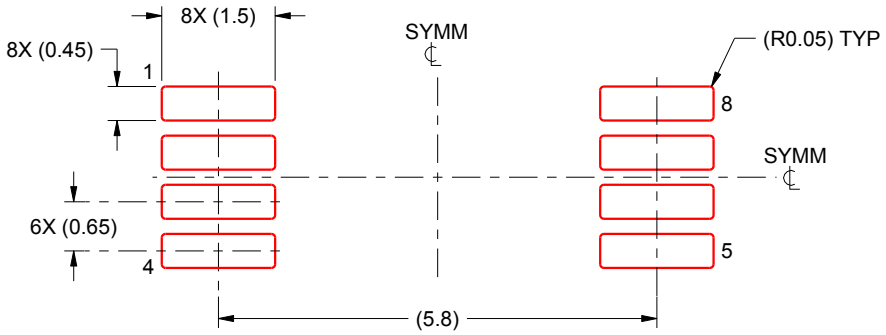


SOLDER MASK DETAILS
NOT TO SCALE

4221848/A 02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A 02/2015

NOTES: (continued)

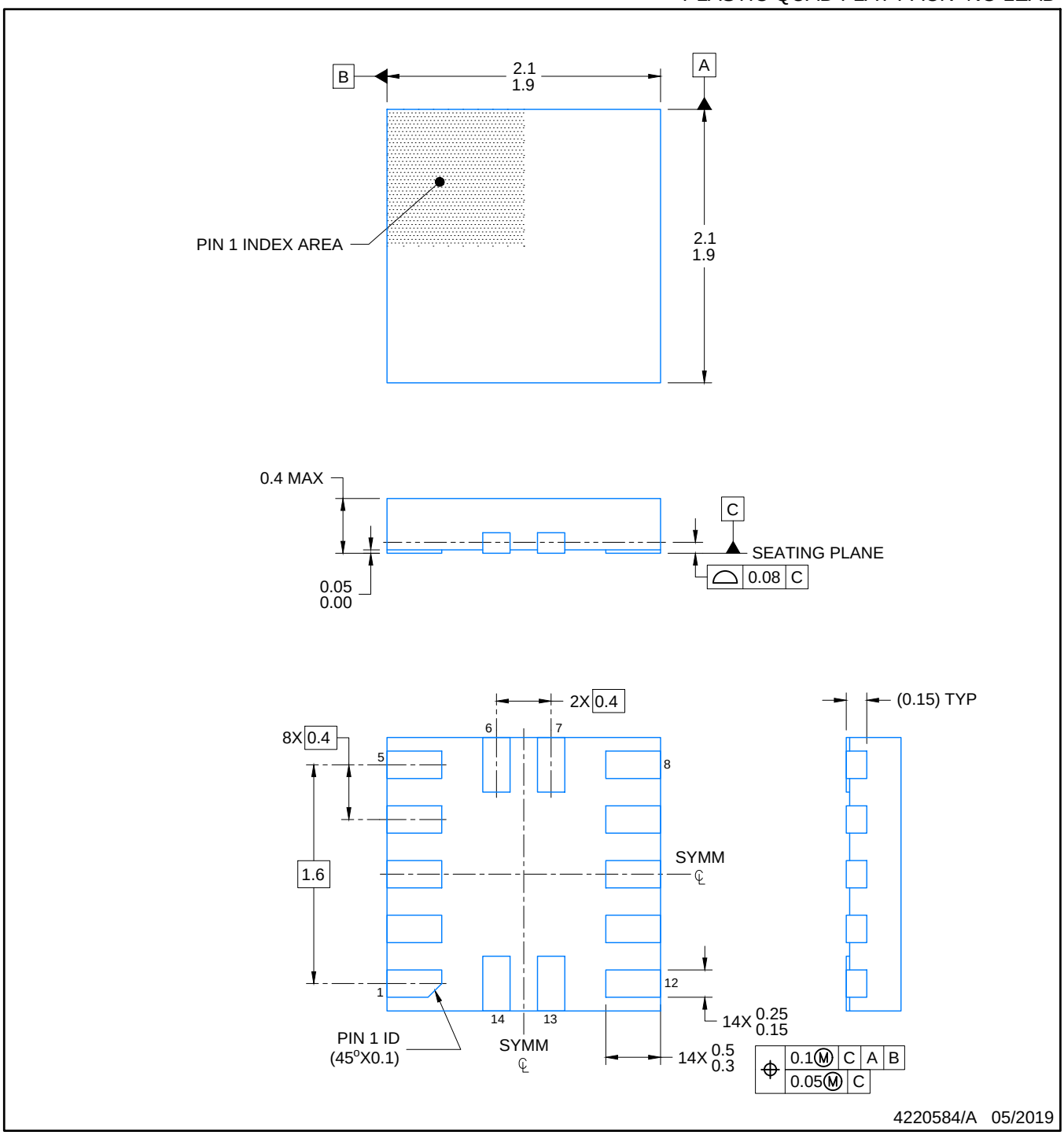
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

RUC0014A

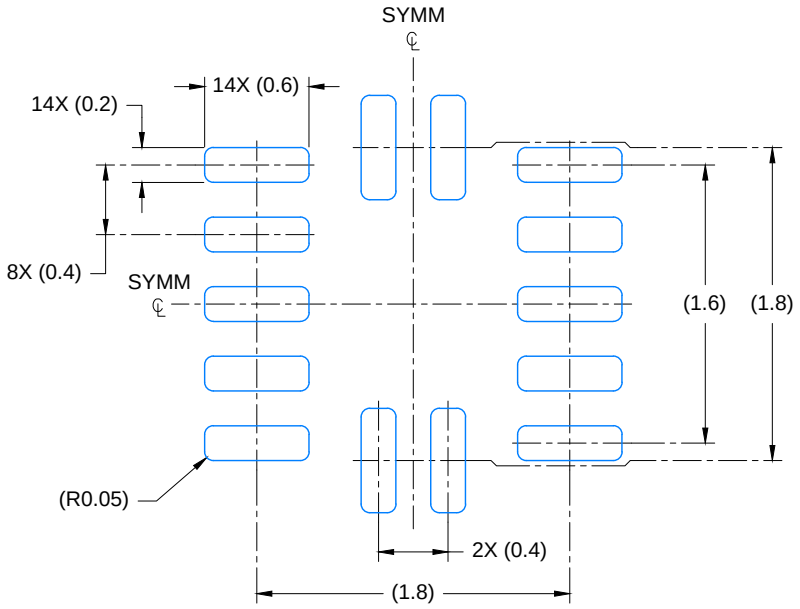
X2QFN - 0.4 mm max height

PLASTIC QUAD FLAT PACK- NO LEAD

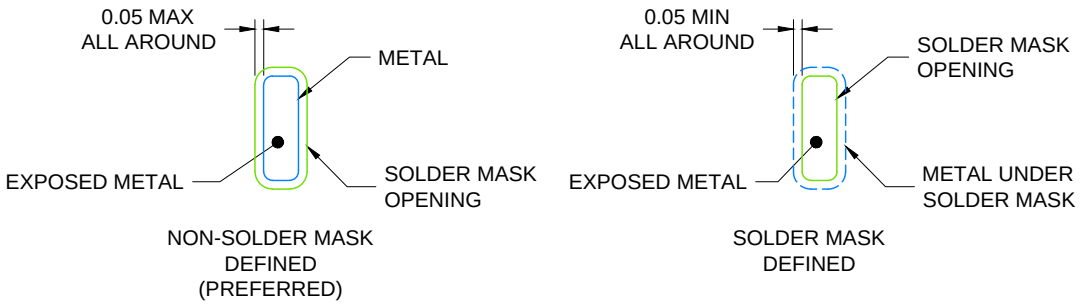


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 23X

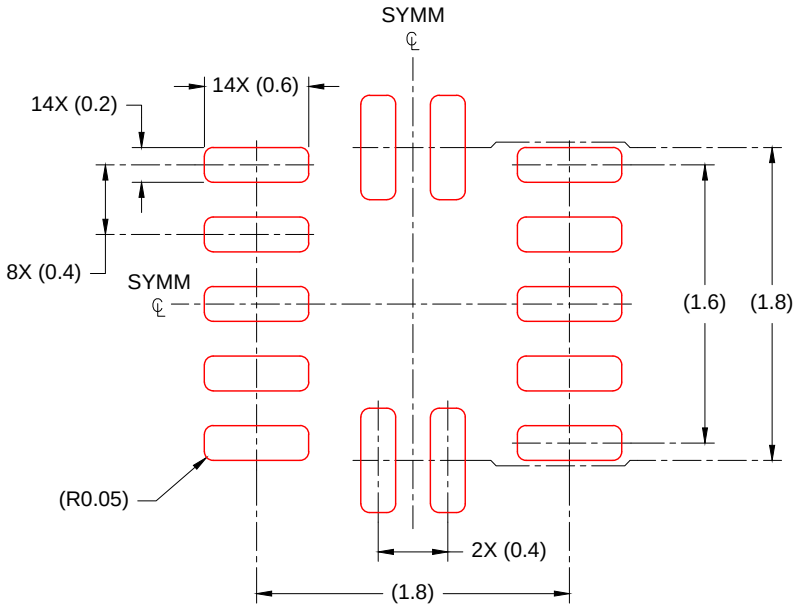


SOLDER MASK DETAILS

4220584/A 05/2019

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.100mm THICK STENCIL
SCALE: 23X

4220584/A 05/2019

NOTES: (continued)

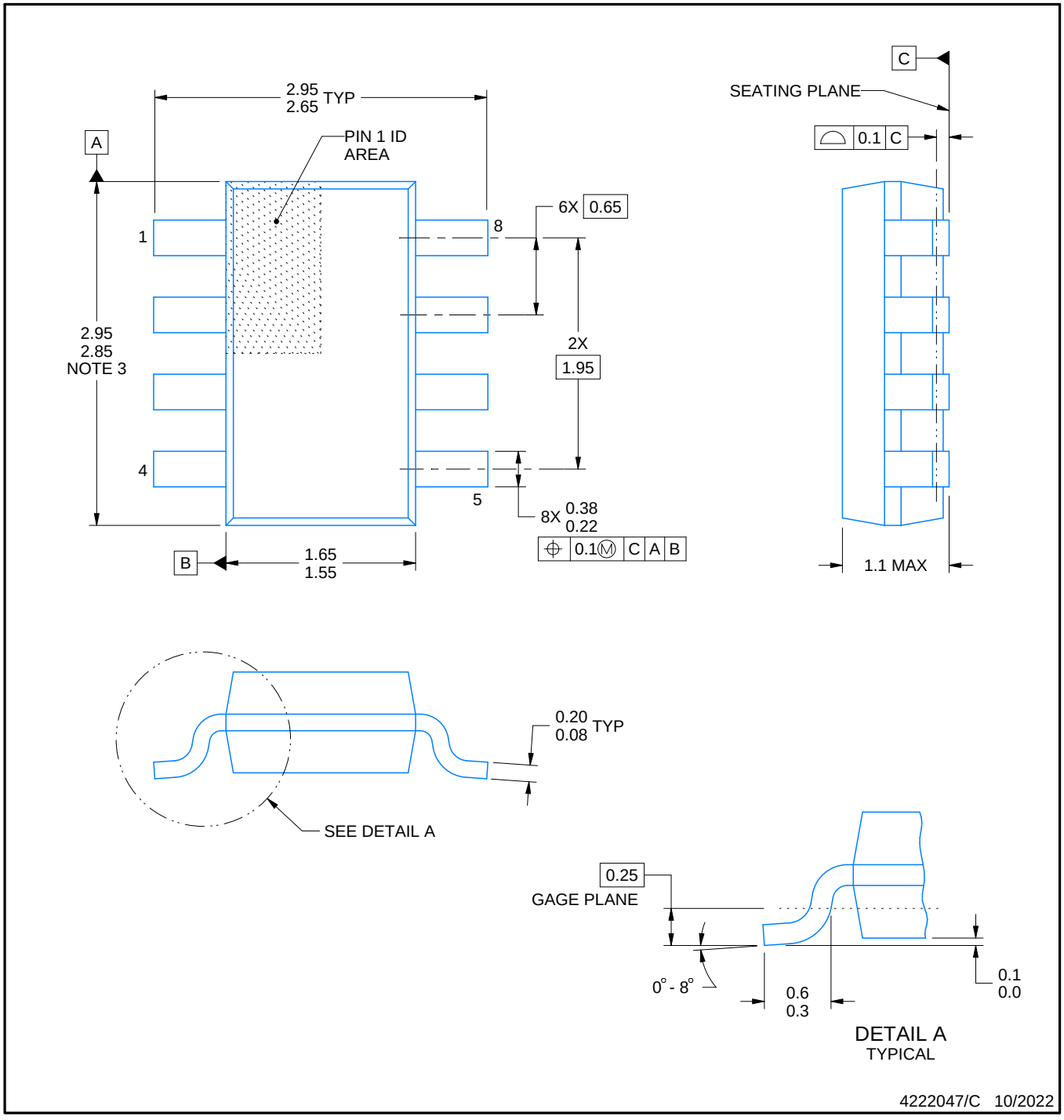
4. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DDF0008A

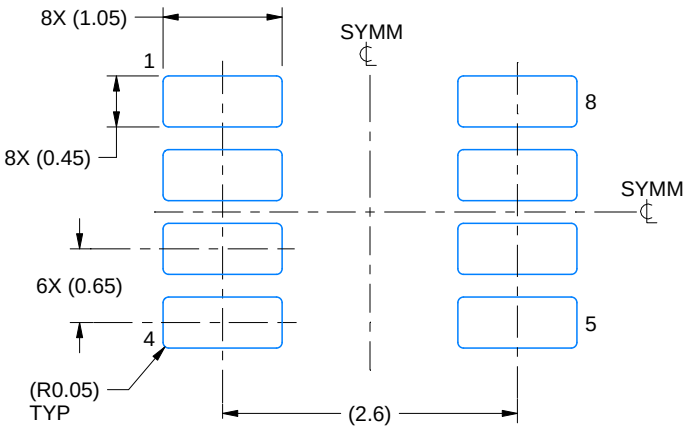
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X



NON SOLDER MASK
DEFINED

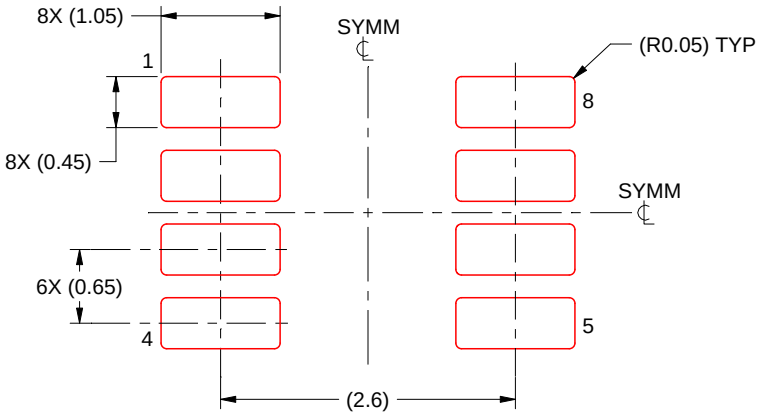
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/C 10/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/C 10/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

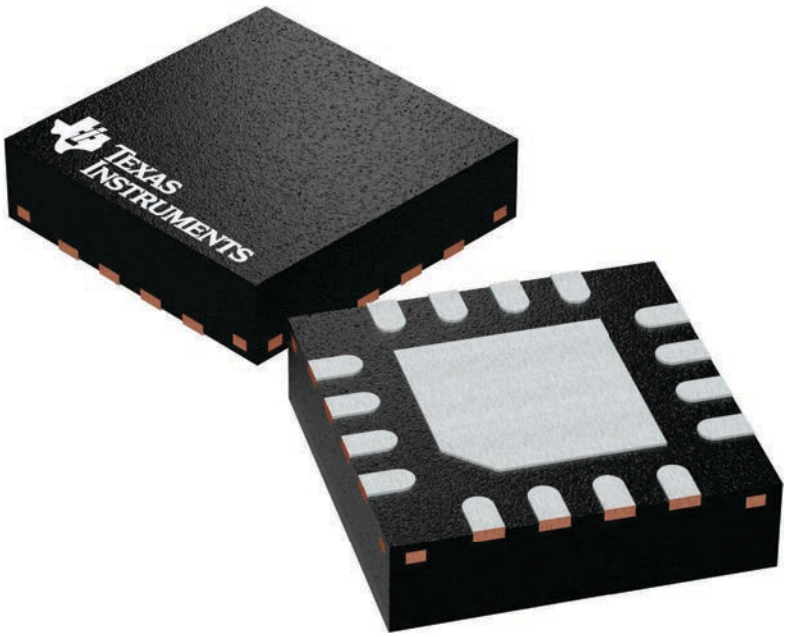
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

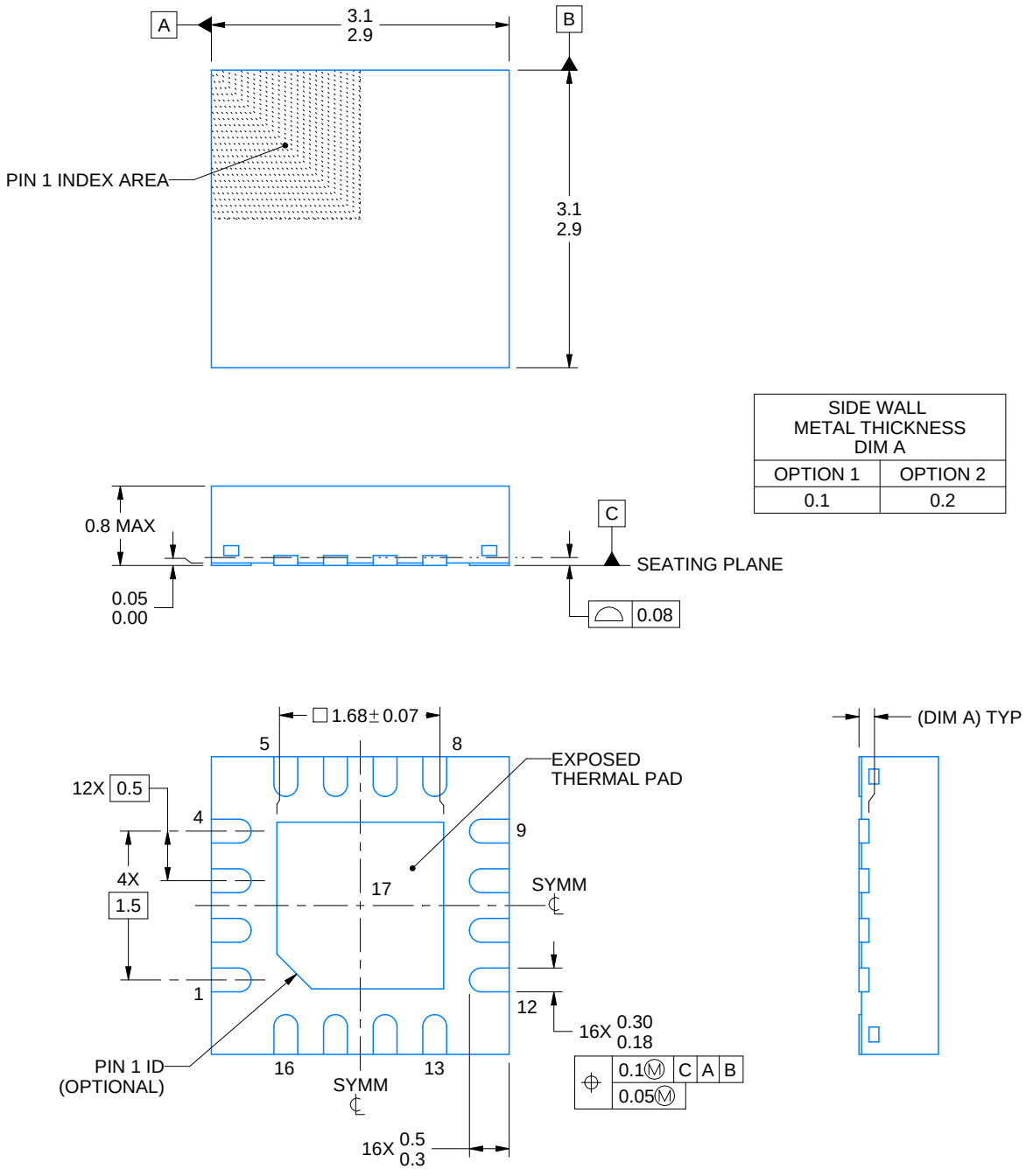


RTE0016C

PACKAGE OUTLINE

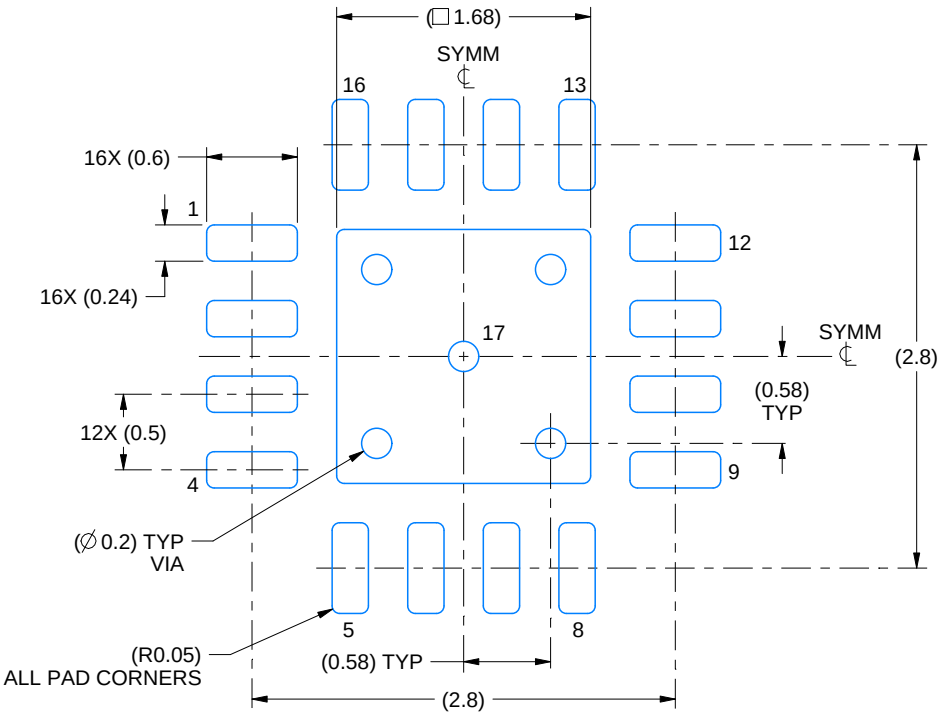
WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

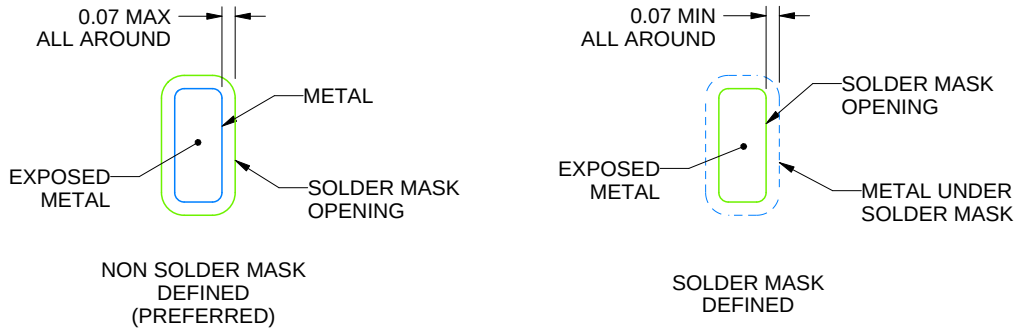


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

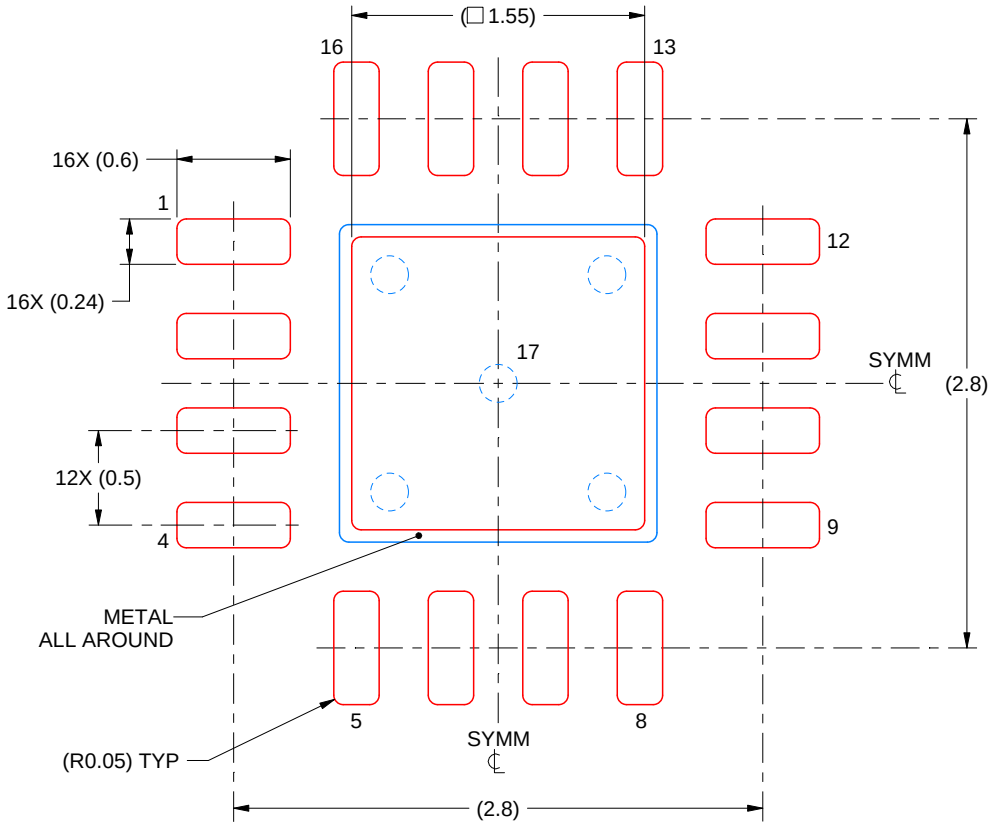


SOLDER MASK DETAILS

4219117/B 04/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4219117/B 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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