TEXAS INSTRUMENTS
TMAG5173-Q1
JAJSP27A – SEPTEMBER 2022 – REVISED SEPTEMBER 2023

TMAG5173-Q1 I²C インターフェイス搭載、高精度 3D ホール・エフェクト・センサ

1 特長

- 位置センシング速度と精度を最適化する高精度リニア 3D ホール効果センサ:
  - 感度室温誤差、X、Y、Z 軸:±2.5% (最大値)
  - 感度ミスマッチの温度ドリフト X-Y 軸:±2% (最大値)
  - X-Y 角度測定室温誤差:±1.1°(最大値)
  - X-Y 角度の測定温度ドリフト:±1.2°(最大値)
  - 1 軸で 20kSPS の変換レート
- 機能安全準拠:
  - 機能安全アプリケーション向けに開発
  - ISO 26262 システムの設計に役立つ資料を利用可能
  - ASIL D までの決定論的能力
  - ASIL B または SIL 2 までのハードウェア完全性
- 車載アプリケーション用に AEC-Q100 認定済み:
  - 温度グレード 1:–40℃～125℃
- 超低消費電力モード:
  - 8nA (代表値) のスリープ・モード電流
- X、Y、Z 軸で線形磁気感度範囲を選択可能:
  - TMAG5173x1-Q1:±40mT、±80mT
  - TMAG5173x2-Q1:±133mT、±266mT
- ユーザー定義の磁気および温度スレッショルド通過からの割り込み信号
- ユニポーラおよびオムニポーラ・スイッチ機能を構成可能
- ゲインおよびオフセット調整付き角度 CORDIC 計算機能を内蔵
- ノイズ低減のための平均化フィルタを構成可能
- 巡回冗長検査 (CRC) 機能を持つ I²C インターフェイス:
  - 最大 1MHz の I²C クロック速度
- I²C または専用 $\overline{\text{INT}}$ ピンにより変換をトリガ
- 各種磁石タイプに対応する温度補償機能を内蔵
- 温度センサ内蔵
- 2.3V～3.6V の電源電圧範囲
- I²C および $\overline{\text{INT}}$ ピンの公差:5.5V (最大値)

2 アプリケーション

- ステアリング・コラム制御
- ステアリング・ホイール制御
- シフタ・システム
- 電動アシスト自転車
- アクチュエータ
- ドア・モジュール
- パワー・シート
- 磁気近接スイッチ

3 概要

TMAG5173-Q1 は、幅広い車載用および産業用アプリケーション向けに設計された高精度リニア 3D ホール効果センサです。このデバイスは、X、Y、Z 軸に 3 つの独立したホール効果センサを内蔵しています。高精度アナログ・シグナル・チェーンは、狭い設計公差が必要なアプリケーションをサポートします。内蔵安全性メカニズムにより、堅牢な機能安全システム設計が可能になります。このデバイスは、1D 線形測定、2D 角度測定、3D ジョイスティック測定、磁気スレッショルドのクロス検出、およびユーザーが構成可能なさまざまなスイッチ機能アプリケーションに適しています。デジタル・フィルタ・オプションを使用すると、最大 32 倍のセンサ・データを統合し、ノイズ性能を向上させることができます。I²C インターフェイスは、多様な動作 V_{CC} 範囲に対応すると同時に、マイクロコントローラとのシームレスなデータ通信を確保します。このデバイスには温度センサが内蔵されており、特定の磁界における熱履歴の確認または温度補償の計算など、各種システム機能に利用できます。

TMAG5173-Q1 は、システムの消費電力と動作速度を最適化するため、複数の動作モードに対応しています。アクティブ・モードでは、デバイスは連続変換を自律的に実行します。スタンバイ・モードでは、マイクロコントローラは $\overline{\text{INT}}$ ピンまたは I²C 通信を使用して、新しい変換をトリガできます。スリープ・モード中、デバイスの消費電力は非常に低く、構成レジスタの値は保持されます。

内蔵の角度計算エンジン (CORDIC) は、軸上と軸外の両方のトポロジについて、角度分解能が 1/16°で 360°の全角度位置情報を提供します。角度の計算は、ユーザー構成レジスタの選択に基づいて、X-Y、Y-Z、または Z-X プレーンのいずれかに対して実行されます。このデバイスは磁気ゲインとオフセット補正機能を搭載しており、システムの機械的誤差の原因による影響を緩和します。

TMAG5173-Q1 はユーザー・レジスタを介して構成することにより、磁気軸と温度チャネル変換を自由に組み合わせて使用できます。このデバイスは、複数の I²C 読み取りフレームをサポートし、巡回冗長性検査と診断ステータス通信にも対応しています。

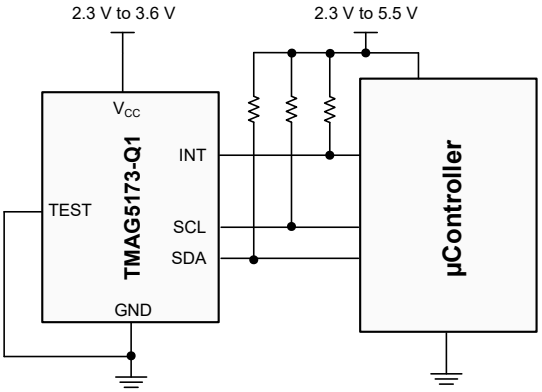
TMAG5173-Q1 は、出荷時にプログラムされた 4 つの異なる I²C アドレスで供給されます。また、このデバイスは、ユーザーが構成可能な I²C アドレス・レジスタを変更することにより、追加の I²C アドレスにも対応できます。各製品バリアントは、システム・キャリブレーション時の磁石の強さおよび部品の配置に適した 2 つの磁界範囲のうちの 1 つを選択するように構成できます。

このデバイスは、-40℃～+125℃の広い周囲温度範囲で正常に動作します。

パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)
TMAG5173-Q1	DBV (SOT-23、6)	2.9mm × 2.8mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にあるパッケージ・オプションについての付録を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



アプリケーションのブロック図

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4 Revision History

Changes from Revision * (September 2022) to Revision A (September 2023)	Page
• データシート・ステータスを「事前情報」から「量産データ」に変更	1

5 Pin Configuration and Functions

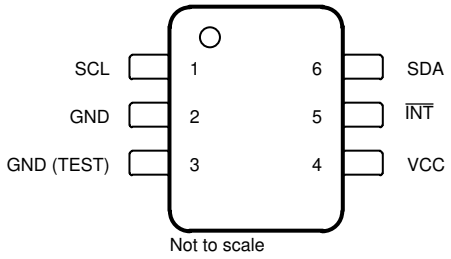


図 5-1. DBV Package, 6-Pin SOT-23 (Top View)

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NO.	NAME		
1	SCL	IO	Serial clock.
2	GND	GND	Ground
3	GND (TEST)	I	TI Test Pin. Connect to ground in application.
4	VCC	P	Supply voltage
5	$\overline{\text{INT}}$	IO	Interrupt input/ output. If not used and connected to ground, set MASK_INTB = 1b.
6	SDA	IO	Serial data.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{CC}	Main supply voltage	–0.3	4	V
I_{OUT}	Output current, SDA, $\overline{INT}$	0	10	mA
V_{OUT}	Output voltage, SDA, $\overline{INT}$	–0.3	7	V
V_{IN}	Input voltage, SCL, SDA, , $\overline{INT}$	–0.3	7	V
B_{MAX}	Magnetic flux density		Unlimited	T
T_J	Junction temperature	–40	150	°C
T_{stg}	Storage temperature	–65	170	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)		±2000	V
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 6, 3, and 4)	±700	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)
over recommended V_{Vcc} range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VCC}	Main supply voltage	2.3		3.6	V
V_{OUT}	Output voltage, SDA, $\overline{INT}$	0		5.5	V
I_{OUT}	Output current, SDA, $\overline{INT}$			2	mA
V_{IH}	Input HIGH voltage, SCL, SDA, $\overline{INT}$	0.7			V_{VCC}
V_{IL}	Input LOW voltage, SCL, SDA, $\overline{INT}$			0.3	V_{VCC}
T_A	Operating free air temperature	–40		125	C

6.4 Thermal Information

THERMAL METRIC(1)		TMAG5173-Q1 DBV (6-SOT23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	162	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	81.6	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	50.1	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	30.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	49.8	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)
over recommended V_{Vcc} range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SDA, $\overline{INT}$						
V_{OL}	Output LOW voltage, SDA, $\overline{INT}$ pin	I_{OUT} = 2 mA	0		0.4	V
I_{OZ}	Output leakage current, SDA, $\overline{INT}$ pin	Output disabled V_{OZ} = 5.5V			±100	nA
tFALL_$\overline{INT}$	$\overline{INT}$ output fall time	R_{PU} = 10 kΩ C_L = 20pF V_{PU} = 1.7 V to 5.5 V		6		ns
tINT ($\overline{INT}$)	$\overline{INT}$ Interrupt time duration during pulse mode	INT_MODE = 001b or 010b		10		µs
tINT (SCL)	SCL Interrupt time duration	INT_MODE = 011b or 100b		10		µs
DC POWER SECTION						
VCC_{UV}	Under voltage threshold at V_{CC}		1.9	2.1	2.2	V
I_{ACTIVE}	Active mode current	X, Y, Z, or thermal sensor active conversion, LP_LN = 0b		2.4		mA
I_{ACTIVE}	Active mode current	X, Y, Z, or thermal sensor active conversion, LP_LN = 1b		3.0		mA
$I_{STANDBY}$	Standby mode current	Device in trigger mode, no conversion started		0.45		mA
I_{SLEEP}	Sleep mode current			8		nA

6.6 Temperature Sensor

over operating free-air temperature range (unless otherwise noted)
over recommended V_{Vcc} range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
T_{SENS_RANGE}	Temperature sensing range		–40		150	℃
T_{SENS}	Temperature output(1)	T_A = 25°C	23	25	27	℃
T_{SENS_RES}	Temperature sensing resolution (in 16-bit format)			58		LSB/℃
T_{SENS_T0}	Reference temperature for T_{ADC_T0}			25		℃
T_{ADC_T0}	Temperature result in decimal value for T_{SENS_T0}			17508		
T_{SENS_ER}	Temperature error(1)	T_A = –40℃ to 125℃		±0.5	±3.5	℃
NRMS_T	RMS (1 Sigma) temperature noise	CONV_AVG = 101b		0.05		℃
NRMS_T	RMS (1 Sigma) temperature noise	CONV_AVG = 000b		0.3		℃

(1) The temperature data is collected with T_CH_EN =1h and at least one magnetic channel enabled

6.7 Magnetic Characteristics For A1, B1, C1, D1

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$B_{IN\_A1\_X\_Y}$	Linear magnetic range[1]	x_y_RANGE = 0b		±40		mT
$B_{IN\_A1\_X\_Y}$		x_y_RANGE = 1b		±80		mT
$B_{IN\_A1\_Z}$		z_RANGE = 0b		±40		mT
$B_{IN\_A1\_Z}$		z_RANGE = 1b		±80		mT
$SENS_{40\_A1}$	Sensitivity, X, Y, or Z axis	±40 mT range		844		LSB/mT
$SENS_{80\_A1}$		±80 mT range		425		LSB/mT
$SENS_{ER\_PC\_25C\_A1}$	Sensitivity error, X, Y, Z axis	T_A = 25°C		±0.4%	±2.5%	
$SENS_{ER\_PC\_TEMP\_A1}$	Sensitivity temperature drift from 25°C value; X, Y, Z axis[2]			±2.0%	±4.8%	
$SENS_{LER\_XY\_A1}$	Sensitivity linearity error, X, Y-axis	T_A = 25°C		±0.10%		
$SENS_{LER\_Z\_A1}$	Sensitivity linearity error, Z axis	T_A = 25°C		±0.10%		
$SENS_{MS\_XY\_A1}$	Sensitivity mismatch among X-Y axes	T_A = 25°C		±0.40%	±2.1%	
$SENS_{MS\_Z\_A1}$	Sensitivity mismatch among Y-Z, or X-Z axes	T_A = 25°C		±0.40%	±2.0%	
$SENS_{MS\_DR\_XY\_A1}$	Sensitivity mismatch temperature drift from 25°C value; X-Y axes[2]			±0.4%	±2.0%	
$SENS_{MS\_DR\_Z\_A1}$	Sensitivity mismatch temperature drift from 25°C value; Y-Z, or X-Z axes[2]			±0.4%	±5.4%	
$SENS_{LDR\_A1}$	Sensitivity lifetime drift, X, Y, Z axis	T_A = 25°C		±1.0%	±3.74%	
B_{off_A1}	Offset	T_A = 25°C		±100	±700	µT
$B_{off\_TC\_A1}$	Offset temperature drift from 25°C value[2]			±1.2	±7.85	µT/°C
$B_{off\_DR\_A1}$	Offset lifetime drift	T_A = 25°C		±100		µT
$N_{RMS\_XY\_00\_000\_A1}$	RMS (1 sigma) magnetic noise (X or Y-axis) T_A = 25°C	LP_LN = 0b CONV_AVG = 000b		92		µT
$N_{RMS\_XY\_01\_000\_A1}$		LP_LN = 1b CONV_AVG = 000b		82.5		µT
$N_{RMS\_XY\_00\_101\_A1}$		LP_LN = 0b CONV_AVG = 101b		16.75		µT
$N_{RMS\_XY\_01\_101\_A1}$		LP_LN = 1b CONV_AVG = 101b		15		µT
$N_{RMS\_Z\_00\_000\_A1}$	RMS (1 sigma) magnetic noise (Z axis) T_A = 25°C	LP_LN = 0b CONV_AVG = 000b		53		µT
$N_{RMS\_Z\_01\_000\_A1}$		LP_LN = 1b CONV_AVG = 000b		48.8		µT
$N_{RMS\_Z\_00\_101\_A1}$		LP_LN = 0b CONV_AVG = 101b		9.4		µT
$N_{RMS\_Z\_01\_101\_A1}$		LP_LN = 1b CONV_AVG = 101b		8.6		µT
$A_{ERR\_X\_Z\_101\_A1}$	X-Z or Y-Z angle error in full 360-degree rotation, 40-mT range, TEMPCO = 0h, T_A = 25°C[3]	CONV_AVG = 101b		±0.4	±1.2	Degree
$A_{ERR\_X\_Y\_101\_A1}$	X-Y angle error in full 360-degree rotation, 80-mT range, TEMPCO = 0h, T_A = 25°C[3]	CONV_AVG = 101b		±0.35	±1.1	Degree
$A_{DR\_X\_Z\_101\_A1}$	X-Z or Y-Z angle temperature drift from 25°C value in full 360-degree rotation; 40-mT range, TEMPCO = 0h[3]	CONV_AVG = 101b		±0.9	±2.5	Degree

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$A_{DR\_X\_Y\_101\_A1}$	X-Y angle temperature drift from 25°C value in full 360-degree rotation; 80-mT range, TEMPCO = 0h(3)	CONV_AVG = 101b		±0.4	±1.2	Degree

(1) Use only up to 90% of the linear magnetic range in the application
(2) Temperature drift is specified for full operating temperature range of –40°C to 125°C. Drift at an intermediate temperature can be estimated using the following examples: drift at 85°C = ((85 – 25) / (125 – 25)) × (drift); similarly, drift at –20°C = ((25 – (–20)) / (25 – (–40))) × (drift).
(3) Angle calculation is performed on-axis after calibrating system mechanical errors including magnet tilt and magnet misalignment.

6.8 Magnetic Characteristics For A2, B2, C2, D2

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$B_{IN\_A2\_X\_Y}$	Linear magnetic range(1)	x_y_RANGE = 0b		±133		mT
$B_{IN\_A2\_X\_Y}$		x_y_RANGE = 1b		±266		mT
$B_{IN\_A2\_Z}$		z_RANGE = 0b		±133		mT
$B_{IN\_A2\_Z}$		z_RANGE = 1b		±266		mT
$SENS_{133\_A2}$	Sensitivity, X, Y, or Z axis	±133 mT range		263		LSB/mT
$SENS_{266\_A2}$		±266 mT range		132		LSB/mT
$SENS_{ER\_PC\_25C\_A2}$	Sensitivity error, X, Y, Z axis	T_A = 25°C		±0.8%	±3.3%	
$SENS_{ER\_PC\_TEMP\_A2}$	Sensitivity temperature drift from 25°C value; X, Y, Z axis(1)			±3.0%	±5.5%	
$SENS_{LER\_XY\_A2}$	Sensitivity linearity error, X, Y-axis	T_A = 25°C		±0.10%		
$SENS_{LER\_Z\_A2}$	Sensitivity linearity error, Z axis	T_A = 25°C		±0.10%		
$SENS_{MS\_XY\_A2}$	Sensitivity mismatch among X-Y axes	T_A = 25°C		±0.5%	±2.3%	
$SENS_{MS\_Z\_A2}$	Sensitivity mismatch among Y-Z, or X-Z axes	T_A = 25°C		±1.50%	±4.3%	
$SENS_{MS\_DR\_XY\_A2}$	Sensitivity mismatch temperature drift from 25°C value; X-Y axes(2)			±0.5%	±2.0%	
$SENS_{MS\_DR\_Z\_A2}$	Sensitivity mismatch temperature drift from 25°C value; Y-Z, or X-Z axes(2)			±4.5%	±8.0%	
$SENS_{LDR\_A2}$	Sensitivity lifetime drift, X, Y, Z axis	T_A = 25°C		±1.5%	±4.9%	
B_{off_A2}	Offset	T_A = 25°C		±100	±700	µT
$B_{off\_TC\_A2}$	Offset temperature drift from 25°C value(2)			±1.2	±7.0	µT/°C
$B_{off\_DR\_A2}$	Offset lifetime drift	T_A = 25°C		±100		µT
$N_{RMS\_XY\_00\_000\_A2}$	RMS (1 sigma) magnetic noise (X or Y-axis)	LP_LN =0 b CONV_AVG = 000b		113		µT
$N_{RMS\_XY\_01\_000\_A2}$		LP_LN = 1b CONV_AVG = 000b		105		µT
$N_{RMS\_XY\_00\_010\_A2}$		LP_LN = 0b CONV_AVG = 101b		20		µT
$N_{RMS\_XY\_10\_010\_A2}$		LP_LN = 1b CONV_AVG = 101b		18.6		µT
$N_{RMS\_Z\_00\_000\_A2}$	RMS (1 sigma) magnetic noise (Z axis)	LP_LN = 0b CONV_AVG = 000b		81.7		µT
$N_{RMS\_Z\_10\_000\_A2}$		LP_LN = 1b CONV_AVG = 000b		78.4		µT
$N_{RMS\_Z\_00\_101\_A2}$		LP_LN = 0b CONV_AVG = 101b		13.9		µT
$N_{RMS\_Z\_10\_101\_A2}$		LP_LN = 1b CONV_AVG = 101b		14		µT

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$A_{ERR\_X\_Z\_101\_A2}$	X-Z or Y-Z angle error in full 360-degree rotation; TEMPCO = 0h, T_A = 25°C(3)	CONV_AVG = 101b		±0.25	±1.0	Degree
$A_{ERR\_X\_Y\_101\_A2}$	X-Y angle error in full 360-degree rotation; 133-mT range, TEMPCO = 0h,T_A = 25°C(3)	CONV_AVG = 101b		±0.4	±1.6	Degree
$A_{DR\_X\_Z\_101\_A2}$	X-Z or Y-Z angle temperature drift from 25°C value in full 360-degree rotation; 133-mT range, TEMPCO = 0h(3)	CONV_AVG = 101b		±1.6	±2.9	Degree
$A_{DR\_X\_Y\_101\_A2}$	X-Y angle temperature drift from 25°C value in full 360-degree rotation; 133-mT range, TEMPCO = 0h(3)	CONV_AVG = 101b		±0.4	±1.4	Degree

(1) Use only up to 90% of the linear magnetic range in the application
(2) Temperature drift is specified for full operating temperature range of –40°C to 125°C. Drift at an intermediate temperature can be estimated using the following examples: drift at 85°C = ((85 – 25) / (125 – 25)) × (drift); similarly, drift at –20°C = ((25 – (–20)) / (25 – (–40))) × (drift).
(3) Angle calculation is performed on-axis after calibrating system mechanical errors including magnet tilt and magnet misalignment.

6.9 Magnetic Temp Compensation Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$TC_{\_00}$	Temperature compensation (X, Y, Z-axes)	TEMPCO = 00b		0		%/°C
$TC_{\_12}$		TEMPCO = 01b		0.12		%/°C
$TC_{\_03}$		TEMPCO = 10b		0.03		%/°C
$TC_{\_20}$		TEMPCO = 11b		0.2		%/°C

6.10 I²C Interface Timing

minimum and maximum specifications are over –40°C to 125°C and V_{CC} = 2.3 V to 3.6 V (unless otherwise noted)(1)

		FAST MODE		FAST MODE PLUS		UNIT
		MIN	MAX	MIN	MAX	
$f_{(SCL)}$	SCL operating frequency	1	400	1	1000	kHz
$t_{(BUF)}$	Bus-free time between STOP and START conditions	1.3		0.5		µs
$t_{(SUSTA)}$	Repeated START condition setup time	0.6		0.26		µs
$t_{(HDSTA)}$	Hold time after repeated START condition. After this period, the first clock is generated.	0		0		µs
$t_{(SUSTO)}$	STOP condition setup time	0.6		0.26		µs
$t_{(HDDAT)}$	Data hold time(2)	0	900	0	150	ns
$t_{(SUDAT)}$	Data setup time	100		50		ns
$t_{(LOW)}$	SCL clock low period	1.3		0.5		µs
$t_{(HIGH)}$	SCL clock high period	0.6		0.26		µs
t_R	SDA, SCL fall time	20	300		120	ns
t_F	SDA, SCL fall time	20 x (V_{CC} / 5.5 V)	300	20 x (V_{CC} / 5.5 V)	120	ns
t_{LPF}	Glitch suppression filter	50		50		ns

(1) The host and device have the same V_{CC} value. Values are based on statistical analysis of samples tested during initial release.
(2) The maximum $t_{(HDDAT)}$ can be 0.9 µs for fast mode, and is less than the maximum $t_{(VDAT)}$ by a transition time.

6.11 Power up Timing

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{start\_power\_up}$	Time to go to standby mode after V_{CC} supply voltage crossing V_{CC_MIN}			270		µs
t_{start_sleep}	Time to go to standby mode from sleep mode(1)			50		µs
$t_{start\_measure}$	Time to go into continuous measure mode from standby mode			70		µs
$t_{measure}$	Conversion time	CONV_AVG = 000b, OPERATING_MODE =10b, only one channel enabled		50		µs
$t_{measure}$	Conversion time	CONV_AVG = 101b, OPERATING_MODE =10b, only one channel enabled		825		µs
t_{go_sleep}	Time to go into sleep mode after SCL goes high			20		µs

(1) The device will recognize the I2C communication from a primary only during standby or continuous measure modes. While the device is in sleep mode, a valid secondary address will wake up the device but no acknowledge will be sent to the primary. Start up time need to be considered before addressing the device after wake up.

6.12 Timing Diagram

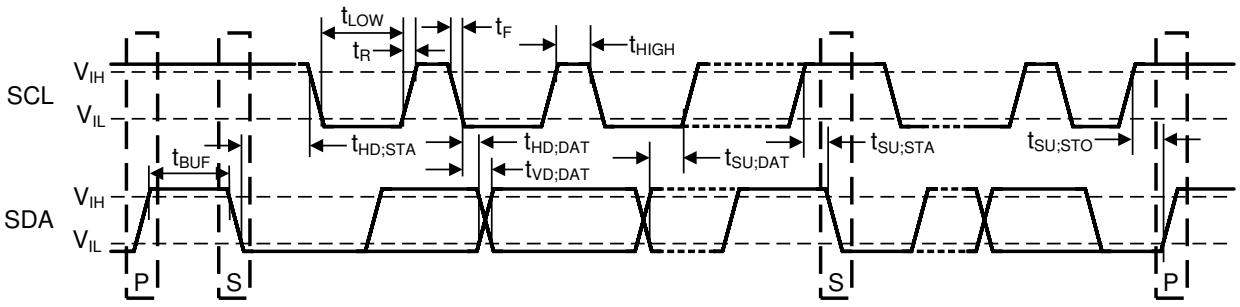


図 6-1. I2C Timing Diagram

6.13 Typical Characteristics

at T_A = 25°C typical (unless otherwise noted)

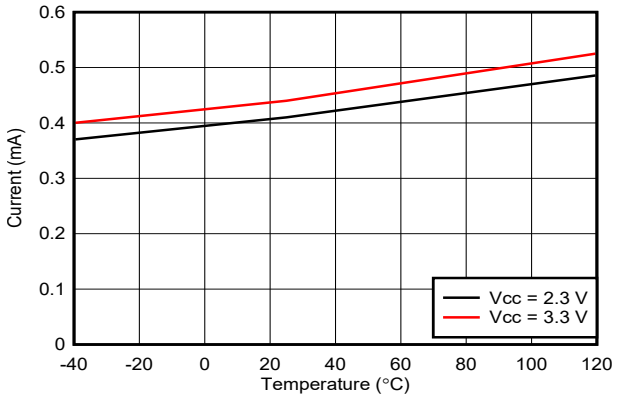
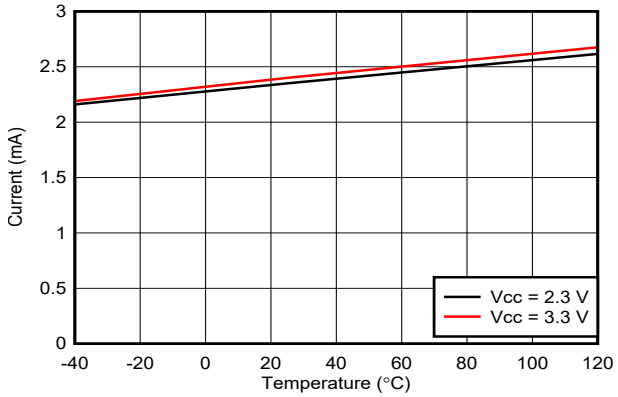


図 6-2. Standby Mode ICC vs Temperature

図 6-3. Active Mode ICC vs Temperature



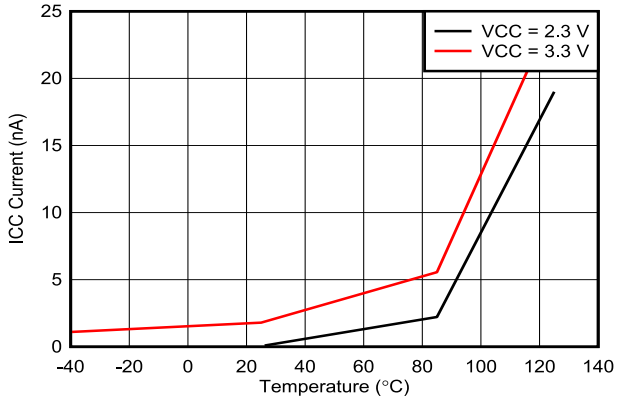


図 6-4. Sleep Mode ICC vs Temperature

7 Detailed Description

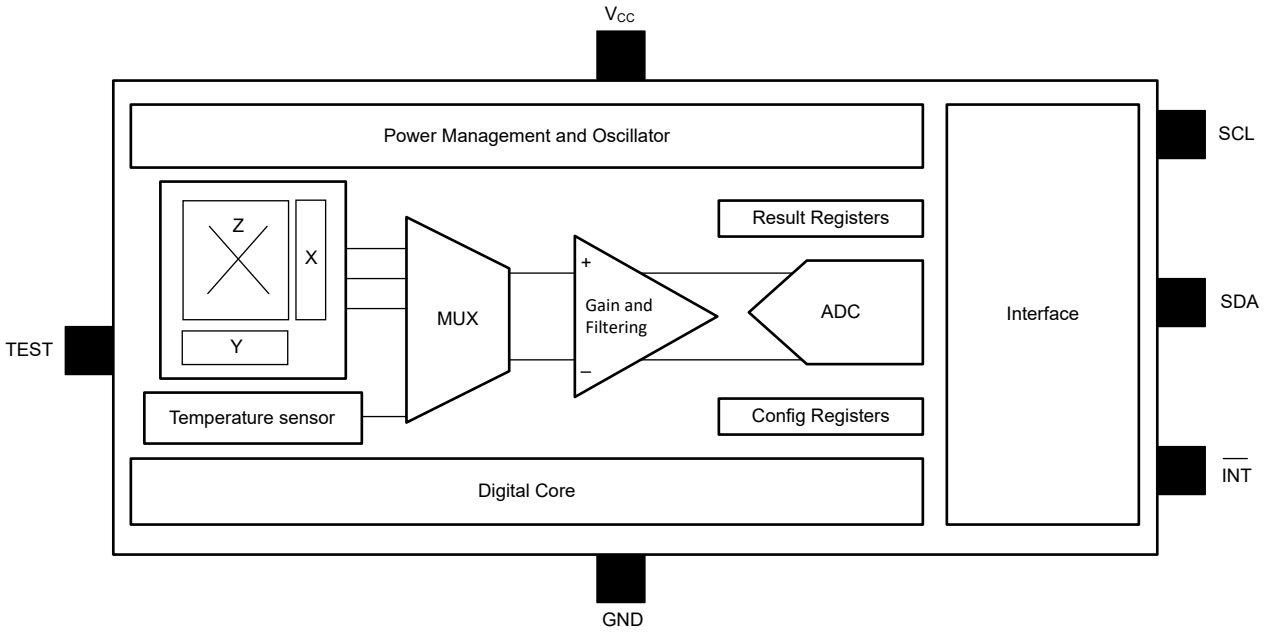
7.1 Overview

The TMAG5173-Q1 IC is based on the Hall-effect technology and precision mixed signal circuitry from Texas Instruments. The output signals (raw X, Y, Z magnetic data and temperature data) are accessible through the I^2C interface.

The IC consists of the following functional and building blocks:

- The Power Management & Oscillator block contain a low-power oscillator, biasing circuitry, undervoltage detection circuitry, and a fast oscillator.
- The sensing and temperature measurement block contains the Hall biasing, Hall sensors with multiplexers, noise filters, integrator circuit, temperature sensor, and the ADC. The Hall-effect sensor data and temperature data are multiplexed through the same ADC.
- The Interface block contains the I^2C control circuitry, ESD protection circuits, and all the I/O circuits. The TMAG5173-Q1 supports multiple I^2C read frames along with integrated cyclic redundancy check (CRC).

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Magnetic Flux Direction

As shown in 図 7-1, the TMAG5173-Q1 will generate positive ADC codes in response to a magnetic north pole in the proximity. Similarly, the TMAG5173-Q1 will generate negative ADC codes if magnetic south poles approach from the same directions.

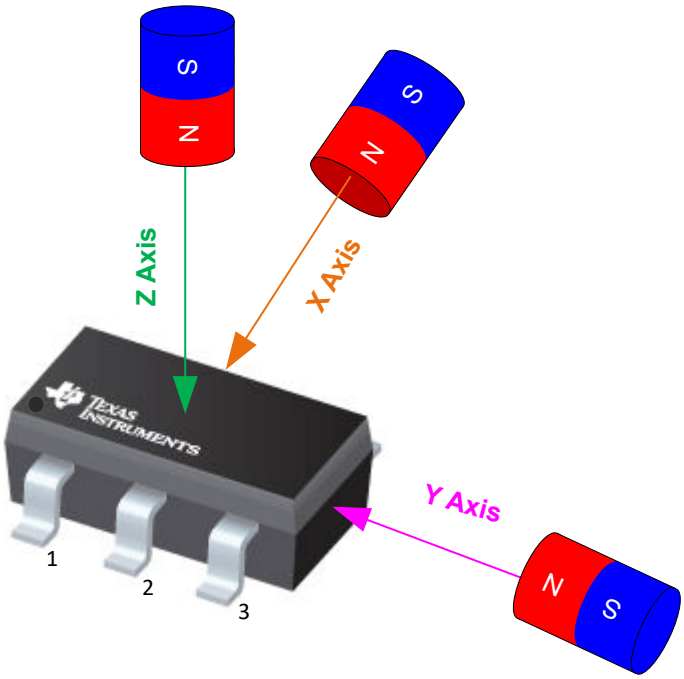


図 7-1. Direction of Sensitivity

7.3.2 Sensor Location

図 7-2 shows the location of X, Y, Z hall elements inside the TMAG5173-Q1.

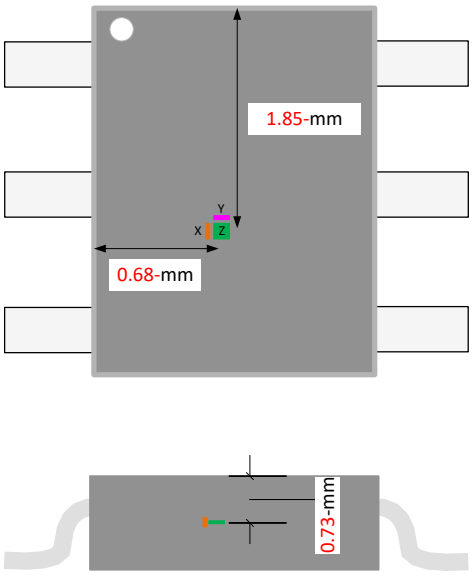


図 7-2. Location of X, Y, Z Hall Elements

7.3.3 Interrupt Function

The TMAG5173-Q1 supports flexible and configurable interrupt functions through either the $\overline{INT}$ or the SCL pin. 表 7-1 shows different conversion completion events where result registers and SET_COUNT bits update, and where they do not.

表 7-1. Result Register & SET_COUNT Update After Conversion Completion

INT_MODE	MODE DESCRIPTION	I²C BUS BUSY, NOT TALKING TO DEVICE		I²C BUS BUSY & TALKING TO DEVICE		I²C BUS NOT BUSY	
		RESULT UPDATE?	SET_COUNT UPDATE?	RESULT UPDATE?	SET_COUNT UPDATE?	RESULT UPDATE?	SET_COUNT UPDATE?
000b	No interrupt	Yes	Yes	No	No	Yes	Yes
001b	Interrupt through $\overline{INT}$	Yes	Yes	No	No	Yes	Yes
010b	Interrupt through $\overline{INT}$ except when I²C busy	Yes	Yes	No	No	Yes	Yes
011b	Interrupt through SCL	Yes	Yes	No	No	Yes	Yes
100b	Interrupt through SCL except when I²C busy	No	No	No	No	Yes	Yes

注

TI does not recommend sharing the same I²C bus with multiple secondary devices when using the SCL pin for interrupt function. The SCL interrupt may corrupt transactions with other secondary devices if present in the same I²C bus.

7.3.3.1 Interrupt Through SCL

図 7-3 shows an example for interrupt function through the SCL pin with the device programmed to generate interrupt at magnetic threshold cross event. When the magnetic threshold cross is detected, the device asserts a fixed width interrupt signal through the SCL pin.

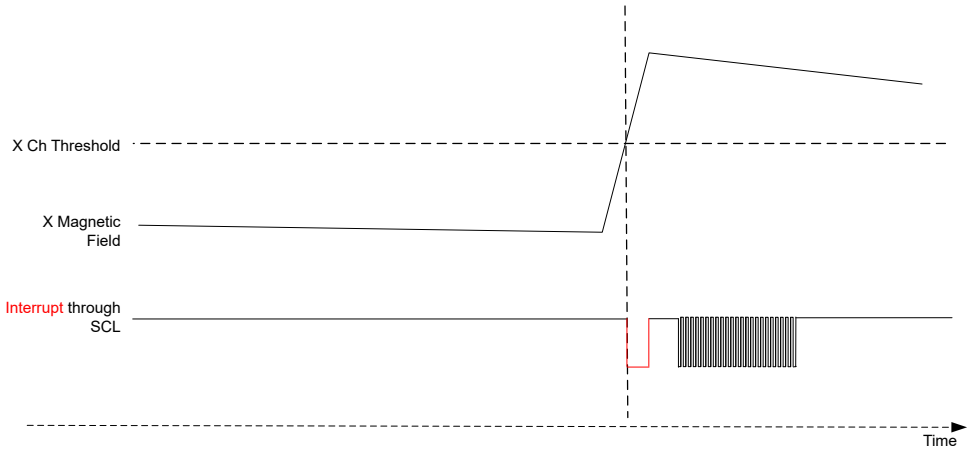


図 7-3. Interrupt Through SCL

7.3.3.2 Fixed Width Interrupt Through $\overline{\text{INT}}$

図 7-4 shows an example for fixed-width interrupt function through the $\overline{\text{INT}}$ pin. The device is programmed to generate interrupt at magnetic threshold cross event. The INT_STATE register bit is set 1b. When the magnetic threshold cross is detected, the device asserts a fixed width interrupt signal through the $\overline{\text{INT}}$ pin.

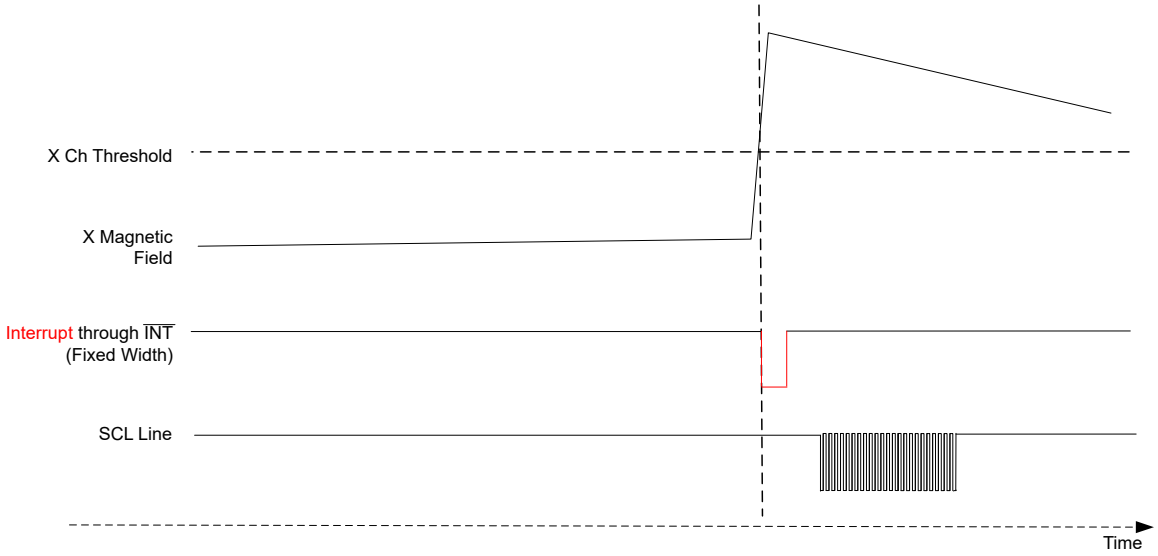


図 7-4. Fixed Width Interrupt Through $\overline{\text{INT}}$

7.3.3.3 Latched Interrupt Through $\overline{\text{INT}}$

図 7-5 shows an example for latched interrupt function through the $\overline{\text{INT}}$ pin. The device is programmed to generate interrupt at magnetic threshold cross event. The INT_STATE register bit is set 0b. When the magnetic threshold cross is detected, the device asserts a latched interrupt signal through the $\overline{\text{INT}}$ pin. The latched interrupt is cleared only after the device receives a valid address through the SCL line.

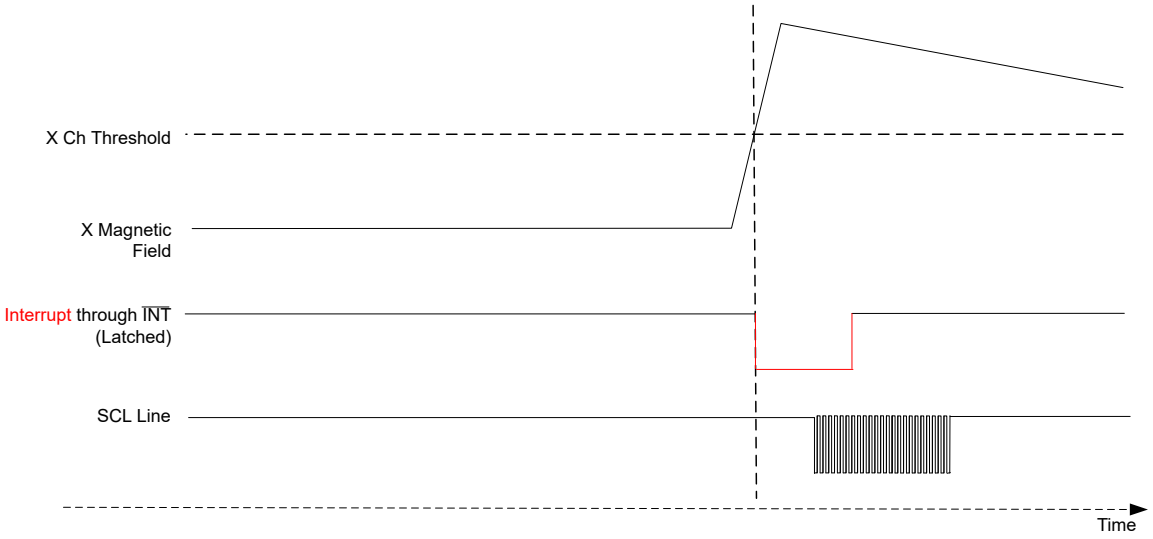


図 7-5. Latched Interrupt Through $\overline{INT}$

7.3.4 Device I²C Address

表 7-2 shows the default factory programmed I²C addresses of the TMAG5173-Q1. The device needs to be addressed with the factory default I²C address after power up. If required, a primary can assign a new I²C address through the I2C_ADDRESS register bits after power up.

表 7-2. I²C Default Address

DEVICE VERSION	MAGNETIC RANGE	I²C ADDRESS (7 MSB BITS)	I²C WRITE ADDRESS (8-BIT)	I²C READ ADDRESS (8-BIT)
TMAG5173A1	±40 mT, ±80 mT	35h	6Ah	6Bh
TMAG5173B1		22h	44h	45h
TMAG5173C1		78h	F0h	F1h
TMAG5173D1		44h	88h	89h
TMAG5173A2	±133 mT, ±266 mT	35h	6Ah	6Bh
TMAG5173B2		22h	44h	45h
TMAG5173C2		78h	F0h	F1h
TMAG5173D2		44h	88h	89h

7.3.5 Magnetic Range Selection

表 7-3 shows the magnetic range selection for the TMAG5173-Q1 device. The X, Y, and Z axes range can be selected with the X_Y_RANGE and Z_RANGE register bits.

表 7-3. Magnetic Range Selection

	RANGE REGISTER SETTING	TMAG5173A1	TMAG5173A2	COMMENT
X, Y Axis Field	X_Y_RANGE = 0b	±40 mT	±133 mT	
	X_Y_RANGE = 1b	±80 mT	±266 mT	Better SNR performance
Z Axis Field	Z_RANGE = 0b	±40 mT	±133 mT	
	Z_RANGE = 1b	±80 mT	±266 mT	Better SNR performance

7.3.6 Update Rate Settings

The TMAG5173-Q1 offers multiple update rates to offer design flexibility to system designers. The different update rates can be selected with the CONV_AVG register bits. 表 7-4 shows different update rate settings for the TMAG5173-Q1.

表 7-4. Update Rate Settings

OPERATING MODE	REGISTER SETTING	UPDATE RATE			COMMENT
		SINGLE AXIS	TWO AXES	THREE AXES	
X, Y, Z Axis	CONV_AVG = 000b	20.0 kSPS	13.3 kSPS	10.0 kSPS	Fastest update rate
X, Y, Z Axis	CONV_AVG = 001b	13.3 kSPS	8.0 kSPS	5.7 kSPS	
X, Y, Z Axis	CONV_AVG = 010b	8.0 kSPS	4.4 kSPS	3.1 kSPS	
X, Y, Z Axis	CONV_AVG = 011b	4.4 kSPS	2.4 kSPS	1.6 kSPS	
X, Y, Z Axis	CONV_AVG = 100b	2.4 kSPS	1.2 kSPS	0.8 kSPS	
X, Y, Z Axis	CONV_AVG = 101b	1.2 kSPS	0.6 kSPS	0.4 kSPS	Best SNR case

7.4 Device Functional Modes

The TMAG5173-Q1 supports multiple functional modes for wide array of applications as explained in 図 7-6. A specific functional mode is selected by setting the corresponding value in the OPERATING_MODE register bits. The device starts powering up after VCC supply crosses the minimum threshold as specified in the *Recommended Operating Conditions* (ROC) table.

7.4.1 Standby (Trigger) Mode

The TMAG5173-Q1 goes to standby mode after power up. During this mode the digital circuitry and oscillators are on and the device is ready to accept commands from the microcontroller. Based off the commands the device can start a new conversion, go to power saving mode, or the start data transfer through I^2C interface. A new conversion can be triggered through I^2C command or through $\overline{INT}$ pin. In this mode the device retains the immediate past conversion result data in the corresponding result registers. The time it takes for the device to go to standby mode from power up is denoted by $T_{start\_power\_up}$. The $\overline{INT}$ pin can be used to a trigger a new conversion or generate interrupt for the microcontroller. It is not recommended to use both functions through $\overline{INT}$ pin simultaneously.

7.4.2 Sleep Mode

The TMAG5173-Q1 supports an ultra-low power sleep mode where it retains the critical user configuration settings. In this mode the device doesn't retain the conversion result data. A microcontroller can wake up the device from sleep mode to standby mode through I^2C communications or the $\overline{INT}$ pin. The time it takes for the device to go to standby mode from sleep mode is denoted by T_{start_sleep}.

7.4.3 Continuous Measure Mode

In this mode the TMAG5173-Q1 continuously measures the sensor data per SENSOR_CONFIG & DEVICE_CONFIG register settings. In this mode the result registers can be accessed through the I2C lines. The time it takes for the device to go from standby mode to continuous measure mode is denoted by $T_{start\_measure}$.

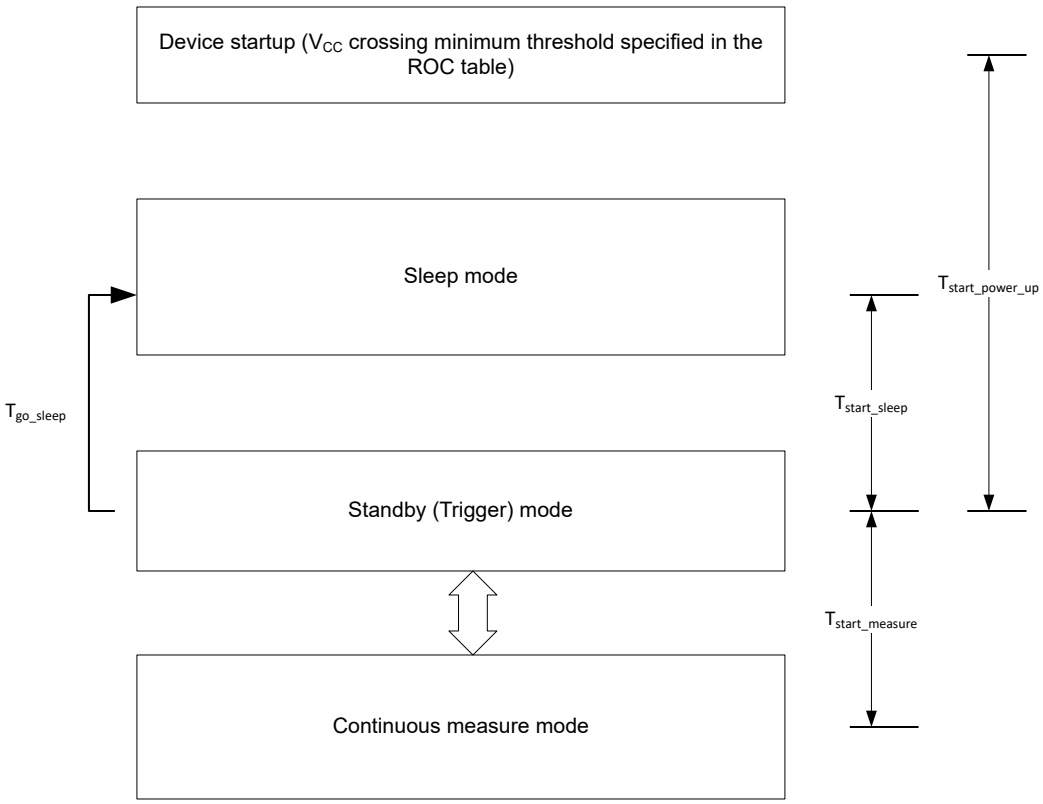


図 7-6. TMAG5173-Q1 Operating Modes

図 7-6 shows TMAG5173-Q1 operating modes and time references to transition from one mode to another.

表 7-5. Operating Modes

OPERATING MODE	DEVICE FUNCTION	ACCESS TO USER REGISTERS	RETAIN USER CONFIGURATION
Continuous measure mode	Continuously measuring X, Y, Z axes, or temperature data	Yes	Yes
Standby mode	Device is ready to accept I^2C commands and start active conversion	Yes	Yes
Sleep mode	Device retains key configuration settings, but doesn't retain the measurement data	No	Yes

7.5 Programming

7.5.1 I²C Interface

The TMAG5173-Q1 offers I²C interface, a two-wire interface to connect low-speed devices like microcontrollers, A/D and D/A converters, I/O interfaces and other similar peripherals in embedded systems.

7.5.1.1 SCL

The SCL is the clock line used to synchronize all data transfers over the I²C bus.

7.5.1.2 SDA

SDA is the bidirectional data line for the I²C interface.

7.5.1.3 I²C Read/Write

The TMAG5173-Q1 supports multiple I²C read and write frames targeting different applications. I2C_RD and CRC_EN bits offers multiple read frames to optimize the read time, data resolution, and data integrity for a select application.

7.5.1.3.1 Standard I²C Write

図 7-7 shows an example of standard I²C two byte write command supported by TMAG5173-Q1. The starting byte contains 7-bit secondary device address and a '0' at the R/$\overline{W}$ command bit. The MSB of the second byte contains the conversion trigger bit. Writing '1' at this trigger bit will start a new conversion after the register address decoding is completed. The 7 LSB bits of the second byte contains the starting register address for the write command. After the two command bytes, the primary device starts to send the data to be written at the corresponding register address. Each successive write byte will send the data for the successive register address in the secondary device.

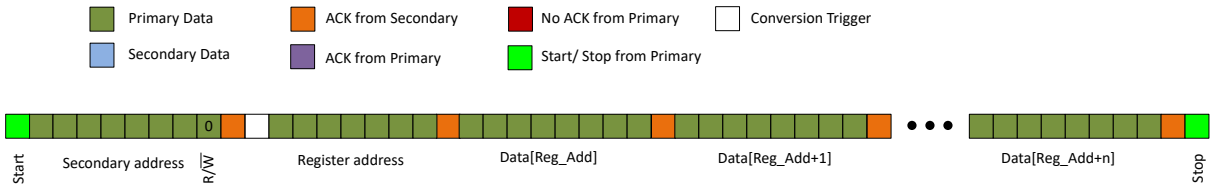


図 7-7. Standard I²C Write

7.5.1.3.2 General Call Write

図 7-8 shows an example of the general call I²C write command supported by the TMAG5173-Q1. This command is useful to configure multiple I²C devices in a I²C bus simultaneously. The starting byte contains 8-bit '0's. The MSB of the second byte contains the conversion trigger bit. Writing '1' at this trigger bit will start a new conversion after the register address decoding is completed. The 7 LSB bits of the second byte contains the starting register address for the write command. After the two command bytes, the primary device starts to send the data to be written at the corresponding register address of all the secondary devices in the I²C bus. Each successive write byte will send the data for the successive register address in the secondary devices.

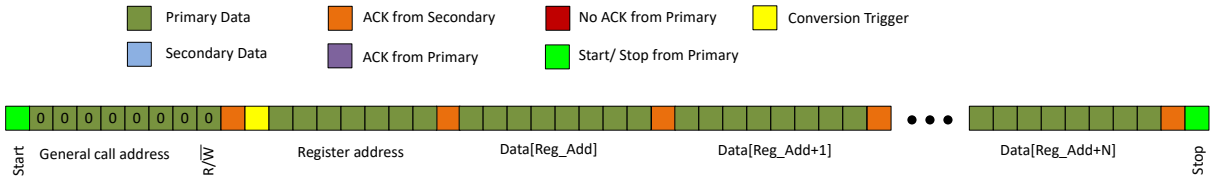


図 7-8. General Call I²C Write

7.5.1.3.3 Standard 3-Byte I²C Read

図 7-9 and 図 7-10 show examples of standard I²C three byte read command supported by the TMAG5173-Q1. The starting byte contains 7-bit secondary device address and the R/$\overline{W}$ command bit '0'. The MSB of the second byte contains the conversion trigger command bit. Writing '1' at this trigger bit will start a new conversion after the register address decoding is completed. The 7 LSB bits of the second byte contains the starting register address for the write command. After receiving ACK signal from secondary, the primary send the secondary address once again with R/$\overline{W}$ command bit as '1'. The secondary starts to send the corresponding register data. It will send successive register data with each successive ACK from primary. If CRC is enabled, the secondary will send the fifth CRC byte based off the CRC calculation of immediate past 4 register bytes.

注

In the standard 3-byte read command the TMAG5173-Q1 doesn't support CRC if the data length is more than 4 byte. Initiate successive read commands for larger data stream requiring CRC.

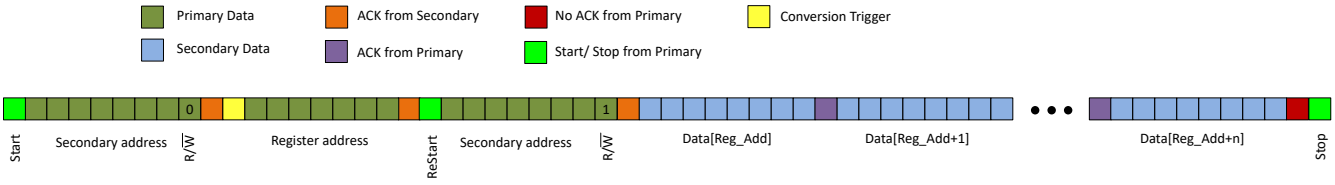


図 7-9. Standard 3-Byte I²C Read With CRC Disabled, CRC_EN = 0b

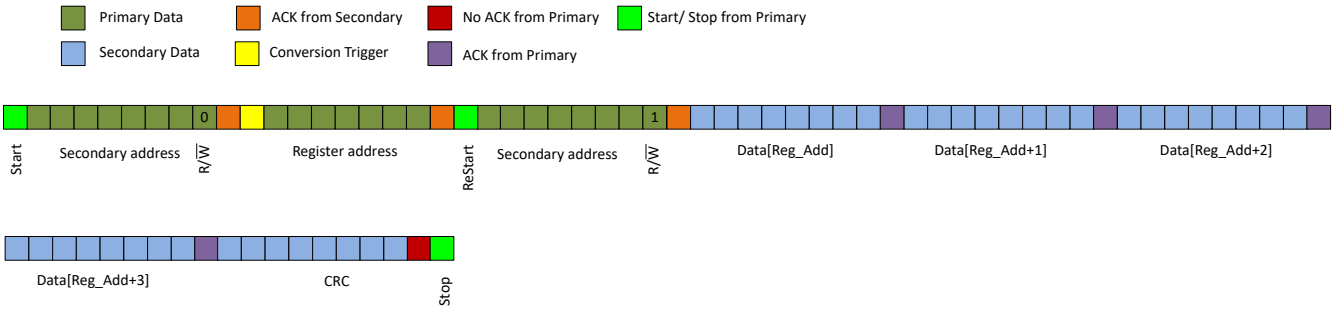


図 7-10. Standard 3-Byte I²C Read With CRC Enabled, CRC_EN = 1b

7.5.1.3.4 1-Byte I2C Read Command for 16-Bit Data

図 7-11 and 図 7-12 show examples of 1-byte I²C read command supported by the TMAG5173-Q1. Select I2C_RD =01b to enable this mode. The command byte contains 7-bit secondary device address and a '1' at the R/$\overline{W}$ bit. In this mode, per MAG_CH_EN and T_CH_EN bits setting, the device will send 16-bit data of the enabled channels and the CONV_STATUS register data byte. If CRC is enabled, the device will send an additional CRC byte based off the CRC calculation of the command byte and the data sent in the current packet. When multiple channels are enabled, the sent data follows the T, X, Y, and Z sequence in the successive data bytes.

図 7-11. 1-Byte I²C Read Command for 16-Bit Data With CRC Disabled, CRC_EN = 0b

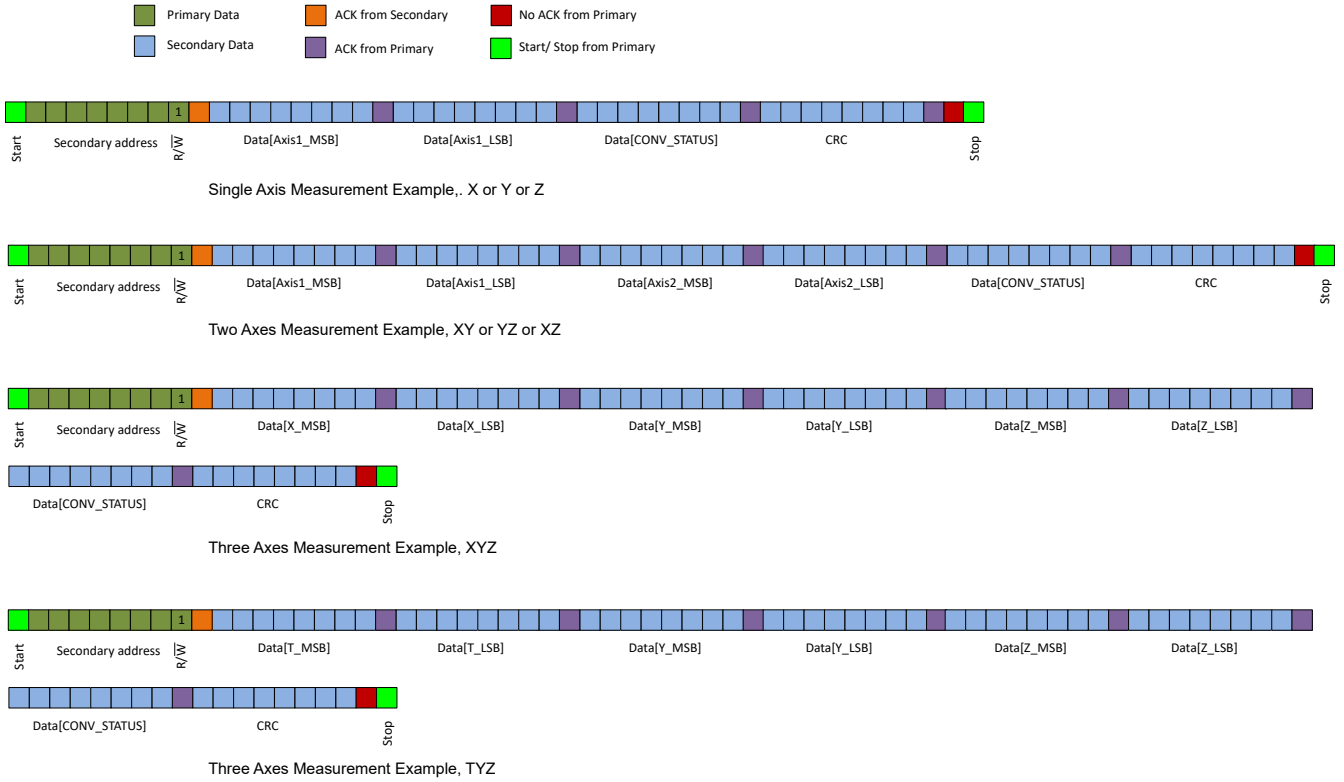


図 7-12. 1-Byte I²C Read Command for 16-Bit Data With CRC Enabled, CRC_EN = 1b

注

In the 1-byte read command for 16-bit data only up to 3 channels data can be sent when CRC is enabled. This restriction doesn't apply if CRC is disabled.

7.5.1.3.5 1-Byte I²C Read Command for 8-Bit Data

図 7-13 and 図 7-14 show examples of 1-byte I²C read command supported by the TMAG5173-Q1. Select I2C_RD =10b to enable this mode. The command byte contains 7-bit secondary device address and a '1' at the R/$\overline{W}$ bit. In this mode, per MAG_CH_EN and T_CH_EN bits setting, the device will send 8-bit data of the enabled channels and the CONV_STATUS register data byte. If CRC is enabled, the device will send an additional CRC byte based off the CRC calculation of the command byte and the data sent in the current packet. When multiple channels are enabled, the sent data follows the T, X, Y, and Z sequence in the successive data bytes.

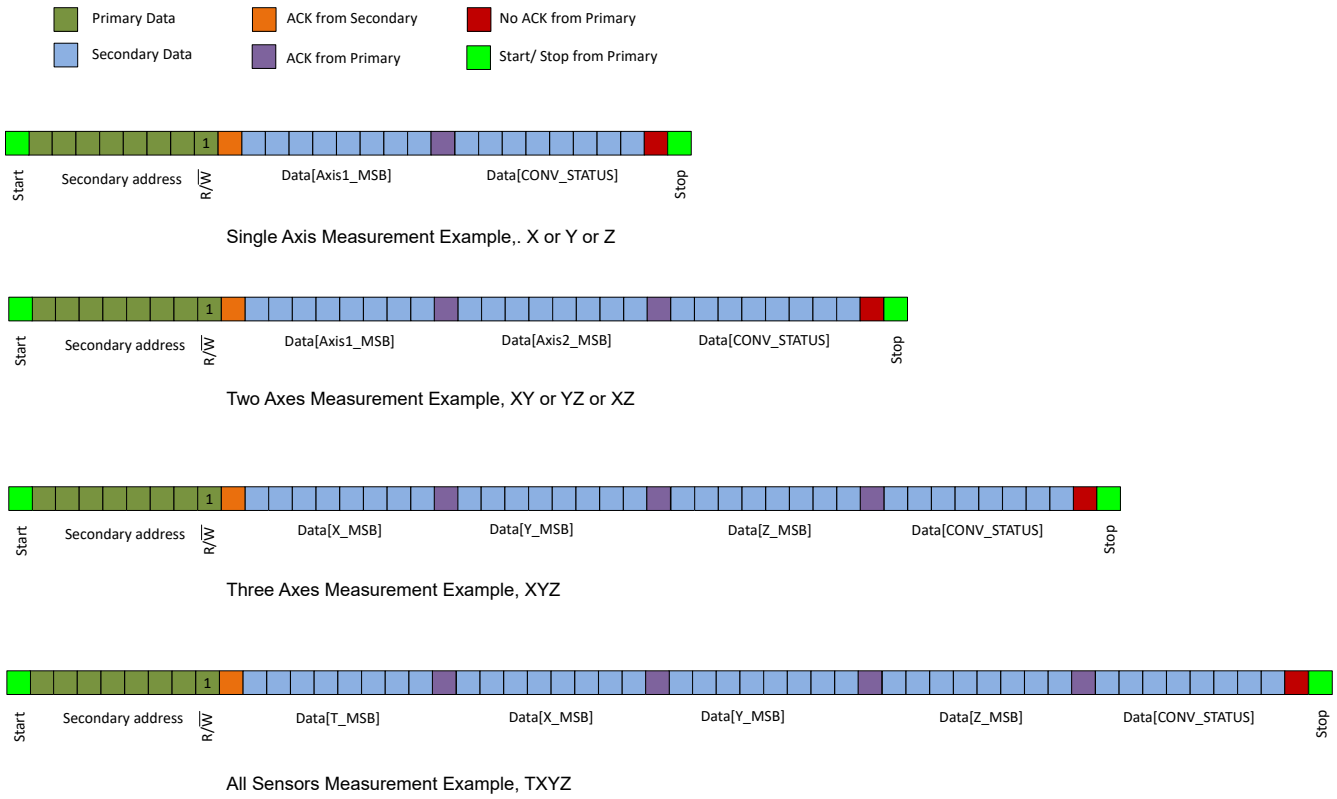


図 7-13. 1-Byte I²C Read Command for 8-Bit Data With CRC Disabled, CRC_EN = 0b

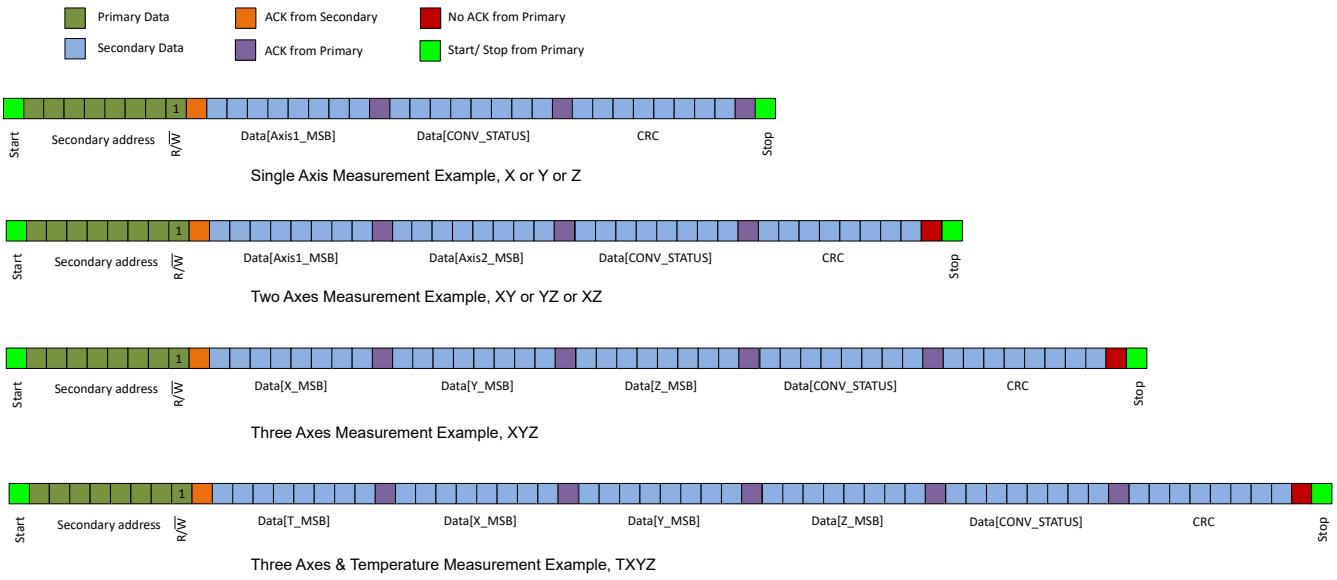


図 7-14. 1-Byte I²C Read Command for 8-Bit Data With CRC Enabled, CRC_EN = 1b

注

In the 1-byte read command for 8-bit data any combinations of channels can be sent without restrictions.

7.5.1.3.6 I²C Read CRC

The TMAG5173-Q1 supports optional CRC during I²C read. The CRC can be enabled through the CRC_EN register bit. The CRC is performed on a data string that is determined by the I²C read type. The CRC information is sent as a single byte after the data bytes. The code is generated by the polynomial $x^8 + x^2 + x + 1$. Initial CRC bits are FFh.

The following equations can be employed to calculate CRC:

d = Data Input, c = Initial CRC (FFh) (1)

newcrc[0] = d[7] ^ d[6] ^ d[0] ^ c[0] ^ c[6] ^ c[7] (2)

newcrc[1] = d[6] ^ d[1] ^ d[0] ^ c[0] ^ c[1] ^ c[6] (3)

newcrc[2] = d[6] ^ d[2] ^ d[1] ^ d[0] ^ c[0] ^ c[1] ^ c[2] ^ c[6] (4)

newcrc[3] = d[7] ^ d[3] ^ d[2] ^ d[1] ^ c[1] ^ c[2] ^ c[3] ^ c[7] (5)

newcrc[4] = d[4] ^ d[3] ^ d[2] ^ c[2] ^ c[3] ^ c[4] (6)

newcrc[5] = d[5] ^ d[4] ^ d[3] ^ c[3] ^ c[4] ^ c[5] (7)

newcrc[6] = d[6] ^ d[5] ^ d[4] ^ c[4] ^ c[5] ^ c[6] (8)

newcrc[7] = d[7] ^ d[6] ^ d[5] ^ c[5] ^ c[6] ^ c[7] (9)

The following examples show calculated CRC byte based off various input data:

I2C Data 00h : CRC = F3h

I2C Data FFh : CRC = 00h

I2C Data 80h : CRC = 7Ah

I2C Data 4Ch : CRC = 10h

I2C Data E0h : CRC = 5Dh

I2C Data 00000000h : CRC = D1h

I2C Data FFFFFFFFh : CRC = 0Fh

7.5.2 Data Definition

7.5.2.1 Magnetic Sensor Data

The X, Y, and Z magnetic sensor data are stored in x_MSB_RESULT and x_LSB_RESULT registers. 図 7-15 shows that each sensor output stored in a 16-bit 2's complement format in two 8-bit registers. The data can be retrieved as 16-bit format combining both MSB and LSB registers, or as 8-bit format through the MSB register.

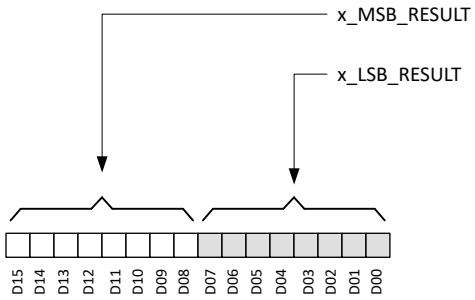


図 7-15. Magnetic Sensor Data Definition

The measured magnetic field can be calculated using 式 10 for 16-bit data, and using 式 11 for 8-bit data.

$$B = \frac{-\left(D_{15} \times 2^{15}\right) + \sum_{i=0}^{14} D_i \times 2^i}{2^{16}} \times 2\left|B_R\right| \tag{10}$$

where

- B is magnetic field in mT.
- D_i is the data bit shown in 図 7-15.
- B_R is the magnetic range in mT for the corresponding channel.

$$B = \frac{-\left(D_{15} \times 2^{7}\right) + \sum_{i=0}^{6} D_i + 8 \times 2^i}{2^{8}} \times 2\left|B_R\right| \tag{11}$$

7.5.2.2 Temperature Sensor Data

The TMAG5173-Q1 will measure temperature from –40°C to 170°C. The temperature sensor data are stored in T_MSB_RESULT and T_LSB_RESULT registers. 図 7-16 shows the sensor output stored in a 16-bit 2's complement format in two 8-bit registers. The data can be retrieved as 16-bit format combining both MSB and LSB registers, or as 8-bit format through the MSB register.

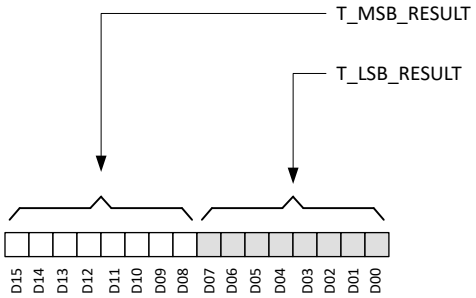


図 7-16. Temperature Sensor Data Definition

Use 式 12 to calculate the measured temperature in degree Celsius for 16-bit data, and use 式 13 to calculate the measured temperature for 8-bit data.

$$T = T_{SENS\_T0} + \frac{T_{ADC\_T} - T_{ADC\_T0}}{T_{ADC\_RES}} \quad (12)$$

$$T = T_{SENS\_T0} + \frac{256 \times \left(T_{ADC\_T} - \frac{T_{ADC\_T0}}{256}\right)}{T_{ADC\_RES}} \quad (13)$$

where

- T is the measured temperature in degree Celsius.
- T_{SENS_T0} as listed in the *Electrical Characteristics* table.
- T_{ADC_RES} is the change in ADC code per degree Celsius.
- T_{ADC_T0} as listed in the *Electrical Characteristics* table.
- T_{ADC_T} is the measured ADC code for temperature T.

7.5.2.3 Angle and Magnitude Data Definition

The TMAG5173-Q1 calculates the angle from a pair of magnetic axes based off the ANGLE_EN register bits setting. 図 7-17 shows the angle information stored in the ANGLE_RESULT_MSB and ANGLE_RESULT_LSB registers. Bits D04-D12 store angle integer value from 0 to 360 degree. Bits D00-D03 store fractional angle value. The 3-MSB bits are always populated as b000. Use 式 14 to calculate the angle value.

$$A = \sum_{i=4}^{12} D_i \times 2^{i-4} + \frac{\sum_{i=0}^{3} D_i \times 2^i}{16} \quad (14)$$

where

- A is the angle measured in degree.
- D_i is the data bit as shown in 図 7-17.

For example: a 354.50 degree is populated as 0001 0110 0010 1000b and a 17.25 degree is populated as 000 0001 0001 0100b.

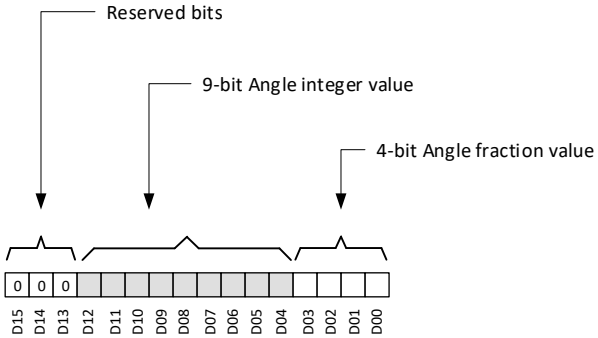


図 7-17. Angle Data Definition

During the angle calculation, use 式 15 to calculate the resultant vector magnitude.

$$M = \sqrt{MADC_{Ch1}{}^2 + MADC_{Ch2}{}^2} \tag{15}$$

where

- $MADC_{Ch1}$, $MADC_{Ch2}$ are the ADC codes of the two magnetic channels selected for the angle calculation.

図 7-18 shows the magnitude value stored in the MAGNITUDE_RESULT register. For on-axis angular measurement the magnitude value should remain constant across the full 360° measurement.

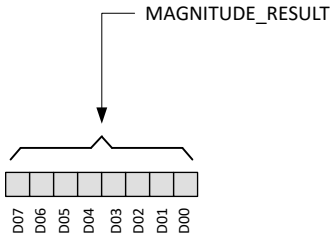


図 7-18. Magnitude Result Data Definition

7.5.2.4 Magnetic Sensor Offset Correction

The TMAG5173-Q1 enables offset correction for a pair of magnetic axes (see 図 7-19). The MAG_OFFSET_CONFIG_1 and MAG_OFFSET_CONFIG_2 registers store the offset values to be corrected in 2's complement data format. As an example, if the uncorrected waveform for a particular axis has a value that is +2 mT too high, the offset correction value of –2 mT should be entered in the corresponding offset correction register. The selection and order of the sensors are defined in the ANGLE_EN register bits setting. The default value of these offset correction registers are set as zero.

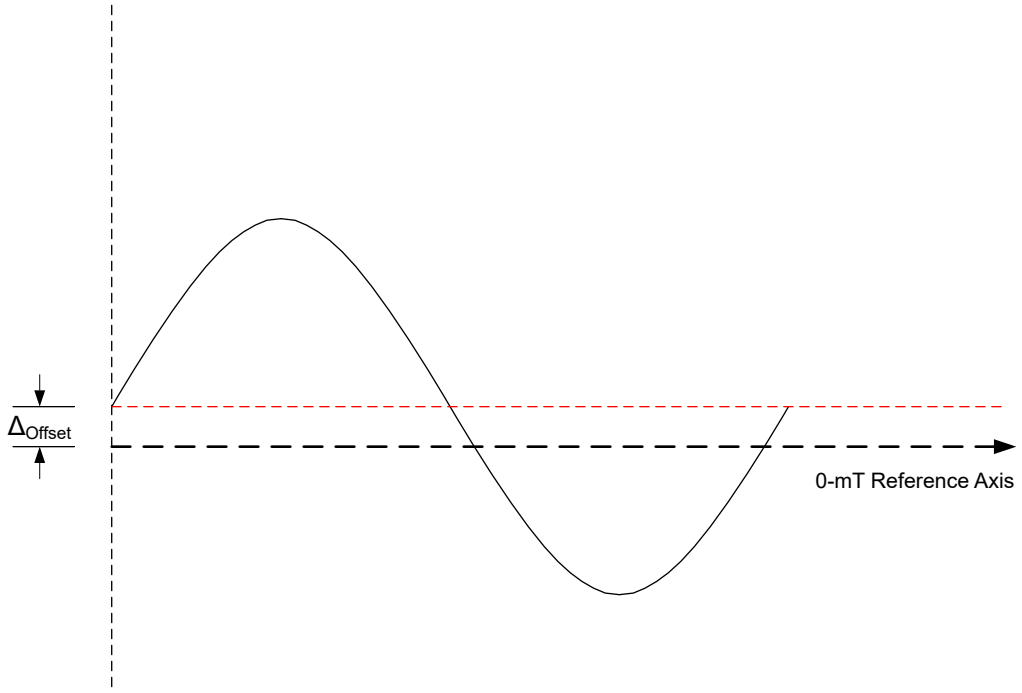


図 7-19. Magnetic Sensor Data Offset Correction

Use 式 16 to calculate the amount of offset for each axis. As an example, with a ±40 mT range, MAG_OFFSET_CONFIG_1 set at 1000 0000b, and MAG_OFFSET_CONFIG_2 set at 0001 0000b, the offset correction for the first axis is −2.5 mT and second axis is 0.312 mT.

$$\Delta_{Offset} = \frac{-\left(D_7 \times 2^7\right) + \sum_{i=0}^{6} D_i \times 2^i}{2^{12}} \times 2|B_R| \tag{16}$$

where

- Δ_{Offset} is the amount of offset correction to be applied in mT.
- D_i is the data bit in the MAG_OFFSET_CONFIG_1 or MAG_OFFSET_CONFIG_2 register.
- B_R is the magnetic range in mT for the corresponding channel.

Alternately, you can use 式 17 to calculate the values for MAG_OFFSET_CONFIG_1 or MAG_OFFSET_CONFIG_2 for a target offset correction.

$$\text{MAG\_OFFSET} = \frac{2^{12} \times \Delta_{Offset}}{2|B_R|} \tag{17}$$

where

- MAG_OFFSET is the decimal value to be entered in the MAG_OFFSET_CONFIG_1 or MAG_OFFSET_CONFIG_2 register.
- Δ_{Offset} is the amount of offset correction to be applied in mT.
- B_R is the magnetic range in mT for the corresponding channel.

7.6 TMAG5173-Q1 Registers

表 7-6 lists the memory-mapped registers for the TMAG5173-Q1 registers. All register offset addresses not listed in 表 7-6 should be considered as reserved locations and the register contents should not be modified.

表 7-6. TMAG5173-Q1 Registers

Offset	Acronym	Register Name	Section
0h	DEVICE_CONFIG_1	Configure Device Operation Modes	セクション 7.6.1
1h	DEVICE_CONFIG_2	Configure Device Operation Modes	セクション 7.6.2
2h	SENSOR_CONFIG_1	Sensor Device Operation Modes	セクション 7.6.3
3h	SENSOR_CONFIG_2	Sensor Device Operation Modes	セクション 7.6.4
4h	X_THR_CONFIG	X Threshold Configuration	セクション 7.6.5
5h	Y_THR_CONFIG	Y Threshold Configuration	セクション 7.6.6
6h	Z_THR_CONFIG	Z Threshold Configuration	セクション 7.6.7
7h	T_CONFIG	Temp Sensor Configuration	セクション 7.6.8
8h	INT_CONFIG_1	Configure Device Operation Modes	セクション 7.6.9
9h	MAG_GAIN_CONFIG	Configure Device Operation Modes	セクション 7.6.10
Ah	MAG_OFFSET_CONFIG_1	Configure Device Operation Modes	セクション 7.6.11
Bh	MAG_OFFSET_CONFIG_2	Configure Device Operation Modes	セクション 7.6.12
Ch	I2C_ADDRESS	I2C Address Register	セクション 7.6.13
Dh	DEVICE_ID	ID for the device die	セクション 7.6.14
Eh	MANUFACTURER_ID_LSB	Manufacturer ID lower byte	セクション 7.6.15
Fh	MANUFACTURER_ID_MSB	Manufacturer ID upper byte	セクション 7.6.16
10h	T_MSB_RESULT	Conversion Result Register	セクション 7.6.17
11h	T_LSB_RESULT	Conversion Result Register	セクション 7.6.18
12h	X_MSB_RESULT	Conversion Result Register	セクション 7.6.19
13h	X_LSB_RESULT	Conversion Result Register	セクション 7.6.20
14h	Y_MSB_RESULT	Conversion Result Register	セクション 7.6.21
15h	Y_LSB_RESULT	Conversion Result Register	セクション 7.6.22
16h	Z_MSB_RESULT	Conversion Result Register	セクション 7.6.23
17h	Z_LSB_RESULT	Conversion Result Register	セクション 7.6.24
18h	CONV_STATUS	Conversion Satus Register	セクション 7.6.25
19h	ANGLE_RESULT_MSB	Conversion Result Register	セクション 7.6.26
1Ah	ANGLE_RESULT_LSB	Conversion Result Register	セクション 7.6.27
1Bh	MAGNITUDE_RESULT	Conversion Result Register	セクション 7.6.28
1Ch	DEVICE_STATUS	Device_Diag Status Register	セクション 7.6.29

Complex bit access types are encoded to fit into small table cells. 表 7-7 shows the codes that are used for access types in this section.

表 7-7. TMAG5173-Q1 Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write

表 7-7. TMAG5173-Q1 Access Type Codes (続き)

Access Type	Code	Description
W1CP	W 1C P	Write 1 to clear Requires privileged access
Reset or Default Value		
-n		Value after reset or the default value

7.6.1 DEVICE_CONFIG_1 Register (Offset = 0h) [Reset = 00h]

DEVICE_CONFIG_1 is shown in 表 7-8.

Return to the Summary Table.

表 7-8. DEVICE_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	CRC_EN	R/W	0h	Enables I2C CRC byte to be sent. 0h = CRC disabled 1h = CRC enabled
6-5	MAG_TEMPCO	R/W	0h	Temperature coefficient of the magnet. 0h = 0 %/°C (No temperature compensation) 1h = 0.12 %/°C (NdBFe) 2h = 0.03 %/°C (SmCo) 3h = 0.20 %/°C (Ceramic)
4-2	CONV_AVG	R/W	0h	Enables additional sampling of the sensor data to reduce the noise effect (or to increase resolution). 0h = 1x average, 10.0-kSPS (3-axes) or 20-kSPS (1 axis) 1h = 2x average, 5.7-kSPS (3-axes) or 13.3-kSPS (1 axis) 2h = 4x average, 3.1-kSPS (3-axes) or 8.0-kSPS (1 axis) 3h = 8x average, 1.6-kSPS (3-axes) or 4.4-kSPS (1 axis) 4h = 16x average, 0.8-kSPS (3-axes) or 2.4-kSPS (1 axis) 5h = 32x average, 0.4-kSPS (3-axes) or 1.2-kSPS (1 axis)
1-0	I2C_RD	R/W	0h	Defines the I2C read mode. 0h = Standard I2C 3-byte read command 1h = 1-byte I2C read command for 16bit sensor data and conversion status 2h = 1-byte I2C read command for 8 bit sensor MSB data and conversion status 3h = Reserved

7.6.2 DEVICE_CONFIG_2 Register (Offset = 1h) [Reset = 00h]

DEVICE_CONFIG_2 is shown in 表 7-9.

Return to the Summary Table.

表 7-9. DEVICE_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	THR_HYST	R/W	0h	Select threshold band for the interrupt function, or hysteresis for the switch function. As an example, with 40-mT range the threshold band or hysteresis value, when THR_HYST set at 2h, ((40/(2^{11}))*8 = 0.156 mT. 0h = Takes the 2's complement value of each x_THR_CONFIG register to create a magnetic threshold of the corresponding axis 1h = Takes the 7 LSB bits of the x_THR_CONFIG register to create two opposite magnetic thresholds (one north, and another south) of equal magnitude. 2h = 8 LSB threshold band, 12 bit resolution 3h = 16 LSB threshold band, 12 bit resolution 4h = 32 LSB threshold, band 12 bit resolution 5h = 64 LSB threshold band, 12 bit resolution 6h = 128 LSB threshold band, 12 bit resolution 7h = 256 LSB threshold band, 12 bit resolution
4	LP_LN	R/W	0h	Selects the modes between low active current or low-noise modes. 0h = Low active current mode 1h = Low noise mode
3	I2C_GLITCH_FILTER	R/W	0h	I2C glitch filter. 0h = Glitch filter on 1h = Glitch filter off
2	TRIGGER_MODE	R/W	0h	Selects a condition which initiates a single conversion based off already configured registers. A running conversion completes before executing a trigger. Redundant triggers are ignored. TRIGGER_MODE is available only during the mode explicitly mentioned in OPERATING_MODE. 0h = Conversion starts at I2C command bits, default 1h = Conversion starts through a trigger signal at the $\overline{\text{INT}}$ pin
1-0	OPERATING_MODE	R/W	0h	Selects the device operating mode. 0h = Standby mode (starts new conversion at trigger event) 1h = Sleep mode 2h = Continuous measure mode 3h = Reserved

7.6.3 SENSOR_CONFIG_1 Register (Offset = 2h) [Reset = 00h]

SENSOR_CONFIG_1 is shown in 表 7-10.

Return to the Summary Table.

表 7-10. SENSOR_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-4	MAG_CH_EN	R/W	0h	Enables data acquisition of the magnetic channel(s). 0h = All magnetic channels of off, default 1h = X channel enabled 2h = Y channel enabled 3h = X, Y channel enabled 4h = Z channel enabled 5h = Z, X channel enabled 6h = Y, Z channel enabled 7h = X, Y, Z channel enabled 8h = XYX channel enabled 9h = YXY channel enabled Ah = YZY channel enabled Bh = XZX channel enabled Ch = X, Y, Z with positive AFE diagnostic check Dh = X, Y, Z with negative AFE diagnostic check Eh = Hall resistance check + ADC check Fh = Hall offset check +ADC check

表 7-10. SENSOR_CONFIG_1 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
3-0	RESERVED	R	0h	Reserved

7.6.4 SENSOR_CONFIG_2 Register (Offset = 3h) [Reset = 00h]

SENSOR_CONFIG_2 is shown in 表 7-11.

Return to the Summary Table.

表 7-11. SENSOR_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RESERVED	R	0h	Reserved
6	THRX_COUNT	R/W	0h	Number of threshold crossings before the interrupt is asserted. 0h = 1 threshold crossing 1h = 4 threshold crossing
5	MAG_THR_DIR	R/W	0h	Selects the direction of threshold check. This bit is ignored when THR_HYST > 001b. 0h = sets interrupt for field above the threshold 1h = sets interrupt for field below the threshold
4	MAG_GAIN_CH	R/W	0h	Selects the axis for magnitude gain correction value entered in MAG_GAIN_CONFIG register. 0h = 1st channel is selected for gain adjustment 1h = 2nd channel is selected for gain adjustment
3-2	ANGLE_EN	R/W	0h	Enables angle calculation, magnetic gain, and offset corrections between two selected magnetic channels. 0h = No angle calculation, magnitude gain, and offset correction enabled 1h = X 1st, Y 2nd 2h = Y 1st, Z 2nd 3h = X 1st, Z 2nd
1	X_Y_RANGE	R/W	0h	Select the X and Y axes magnetic range from 2 different options. 0h = ±40mT (TMAG5173A1) or ±133mT (TMAG5173A2), default 1h = ±80mT (TMAG5173A1) or ±266mT (TMAG5173A2)
0	Z_RANGE	R/W	0h	Select the Z axis magnetic range from 2 different options. 0h = ±40mT (TMAG5173A1) or ±133mT (TMAG5173A2), default 1h = ±80mT (TMAG5173A1) or ±266mT (TMAG5173A2)

7.6.5 X_THR_CONFIG Register (Offset = 4h) [Reset = 00h]

X_THR_CONFIG is shown in 表 7-12.

Return to the Summary Table.

表 7-12. X_THR_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	X_THR_CONFIG	R/W	0h	8-bit, 2's complement X axis threshold code for limit check. The range of possible threshold entrees can be from -128 to 127. The threshold value in mT is calculated for A1 as (40(1+X_Y_RANGE)/128)*X_THR_CONFIG, for A2 as (133(1+X_Y_RANGE)/128)*X_THR_CONFIG. Default 0h means no threshold comparison.

7.6.6 Y_THR_CONFIG Register (Offset = 5h) [Reset = 00h]

Y_THR_CONFIG is shown in 表 7-13.

Return to the Summary Table.

表 7-13. Y_THR_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Y_THR_CONFIG	R/W	0h	8-bit, 2's complement Y axis threshold code for limit check. The range of possible threshold entrees can be from -128 to 127. The threshold value in mT is calculated for A1 as (40(1+X_Y_RANGE)/128)*Y_THR_CONFIG, for A2 as (133(1+X_Y_RANGE)/128)*Y_THR_CONFIG. Default 0h means no threshold comparison.

7.6.7 Z_THR_CONFIG Register (Offset = 6h) [Reset = 00h]

Z_THR_CONFIG is shown in 表 7-14.

Return to the Summary Table.

表 7-14. Z_THR_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Z_THR_CONFIG	R/W	0h	8-bit, 2's complement Z axis threshold code for limit check. The range of possible threshold entrees can be from -128 to 127. The threshold value in mT is calculated for A1 as (40(1+Z_RANGE)/ 128)*Z_THR_CONFIG, for A2 as (133(1+Z_RANGE)/ 128)*Z_THR_CONFIG. Default 0h means no threshold comparison.

7.6.8 T_CONFIG Register (Offset = 7h) [Reset = 00h]

T_CONFIG is shown in 表 7-15.

Return to the Summary Table.

表 7-15. T_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	T_THR_CONFIG	R/W	0h	Temperature threshold code entered by user. The valid temperature threshold ranges are -41C to 170C with the threshold codes for -41C = 1Ah, and 170C = 34h. Resolution is 8-degree C/ LSB. Default 0h means no threshold comparison.
0	T_CH_EN	R/W	0h	Enables data acquisition of the temperature channel. 0h = Temp channel disabled 1h = Temp channel enabled

7.6.9 INT_CONFIG_1 Register (Offset = 8h) [Reset = 00h]

INT_CONFIG_1 is shown in 表 7-16.

Return to the Summary Table.

表 7-16. INT_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7	RSLT_INT	R/W	0h	Enable interrupt response when conversion result is complete. 0h = Interrupt is not asserted when the configured set of conversions are complete 1h = Interrupt is asserted when the configured set of conversions are complete
6	THRSLD_INT	R/W	0h	Enable interrupt response on a predefined threshold cross. 0h = Interrupt is not asserted when a threshold is crossed 1h = Interrupt is asserted when a threshold is crossed
5	INT_STATE	R/W	0h	$\overline{\text{INT}}$ interrupt latched or pulsed. 0h = $\overline{\text{INT}}$ interrupt latched until clear by a primary addressing the device 1h = $\overline{\text{INT}}$ interrupt pulse for 10 us

表 7-16. INT_CONFIG_1 Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
4-2	INT_MODE	R/W	0h	Interrupt mode select. 0h = No interrupt 1h = Interrupt through $\overline{INT}$ 2h = Interrupt through $\overline{INT}$ except when I2C bus is busy. 3h = Interrupt through SCL 4h = Interrupt through SCL except when I2C bus is busy. 5h = Unipolar switch function during continuous measure mode (only one magnetic field conversion support, selects the first magnetic field in X, Y, Z order if multiple thresholds are enabled). This mode overrides any interrupt function (INT trigger is also disabled), and only implements a Hall switch function based off the x_THRX_CONFIG and THR_HYST settings. Select THR_HYST >001b for this mode. 6h = Omnipolar switch function during continuous measure mode (only one magnetic field conversion support, selects the first magnetic field in X, Y, Z order if multiple thresholds are enabled). This mode overrides any interrupt function (INT trigger is also disabled), and only implements a Hall switch function based off the x_THRX_CONFIG and THR_HYST settings. Select THR_HYST >001b for this mode. 7h = Not valid- defaults to 000b mode
1	RESERVED	R	0h	Reserved
0	MASK_INTB	R/W	0h	Mask $\overline{INT}$ pin when $\overline{INT}$ connected to GND. 0h = $\overline{INT}$ pin is enabled 1h = $\overline{INT}$ pin is disabled (for wake-up and trigger functions)

7.6.10 MAG_GAIN_CONFIG Register (Offset = 9h) [Reset = 00h]

MAG_GAIN_CONFIG is shown in 表 7-17.

Return to the Summary Table.

表 7-17. MAG_GAIN_CONFIG Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	GAIN_VALUE	R/W	0h	8-bit gain value determined by a primary to adjust a Hall axis gain. The particular axis is selected based off the settings of MAG_GAIN_CH and ANGLE_EN register bits. The binary 8-bit input is interpreted as a fractional value in between 0 and 1 based off the formula, 'user entered value in decimal/256'. Gain value of 0 is interpreted by the device as 1.

7.6.11 MAG_OFFSET_CONFIG_1 Register (Offset = Ah) [Reset = 00h]

MAG_OFFSET_CONFIG_1 is shown in 表 7-18.

Return to the Summary Table.

表 7-18. MAG_OFFSET_CONFIG_1 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OFFSET_VALUE_1ST	R/W	0h	8-bit, 2's complement number entered by a primary to adjust the 1st axis offset during angle calculation. The 1st axis is defined in ANGLE_EN register bits. The range of possible valid entrees in decimal numbers can be -128 to 127. The offset value is calculated by multiplying bit resolution (uT/ LSB) with the entered value.

7.6.12 MAG_OFFSET_CONFIG_2 Register (Offset = Bh) [Reset = 00h]

MAG_OFFSET_CONFIG_2 is shown in 表 7-19.

Return to the Summary Table.

表 7-19. MAG_OFFSET_CONFIG_2 Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	OFFSET_VALUE_2ND	R/W	0h	8-bit, 2's complement number entered by a primary to adjust the 2nd axis offset during angle calculation. The 2nd axis is defined in ANGLE_EN register bits. The range of possible valid entrees in decimal numbers can be -128 to 127. The offset value is calculated by multiplying bit resolution (uT/ LSB) with the entered value.

7.6.13 I2C_ADDRESS Register (Offset = Ch) [Reset = 6Ah]

I2C_ADDRESS is shown in 表 7-20.

Return to the Summary Table.

表 7-20. I2C_ADDRESS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-1	I2C_ADDRESS	R/W	35h	7-bit default factory I2C address is loaded from OTP during first power up. Change these bits to a new setting if a new I2C address is required (at each power cycle these bits need to be written again to avoid going back to default factory address).
0	I2C_ADDRESS_UPDATE_EN	R/W	0h	Enable a new user defined I2C address. 0h = Disable update of I2C address 1h = Enable update of I2C address with bits (7:1)

7.6.14 DEVICE_ID Register (Offset = Dh) [Reset = 04h]

DEVICE_ID is shown in 表 7-21.

Return to the Summary Table.

表 7-21. DEVICE_ID Register Field Descriptions

Bit	Field	Type	Reset	Description
7-2	RESERVED	R	1h	Reserved
1-0	VER	R	0h	Device version indicator. Reset value of DEVICE_ID depends on the orderable part number. 0h = ±40-mT and ±80-mT range 1h = Reserved 2h = ±133-mT and ±266-mT range 3h = Reserved

7.6.15 MANUFACTURER_ID_LSB Register (Offset = Eh) [Reset = 49h]

MANUFACTURER_ID_LSB is shown in 表 7-22.

Return to the Summary Table.

表 7-22. MANUFACTURER_ID_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MANUFACTURER_ID_[7:0]	R	49h	Unique manufacturer ID LSB bits.

7.6.16 MANUFACTURER_ID_MSB Register (Offset = Fh) [Reset = 54h]

MANUFACTURER_ID_MSB is shown in 表 7-23.

Return to the Summary Table.

表 7-23. MANUFACTURER_ID_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MANUFACTURER_ID_[15:8]	R	54h	Unique manufacturer ID MSB bits.

7.6.17 T_MSB_RESULT Register (Offset = 10h) [Reset = 00h]

T_MSB_RESULT is shown in 表 7-24.

Return to the Summary Table.

表 7-24. T_MSB_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	T_CH_RESULT [15:8]	R	0h	T-channel data conversion results, MSB 8 bits.

7.6.18 T_LSB_RESULT Register (Offset = 11h) [Reset = 00h]

T_LSB_RESULT is shown in 表 7-25.

Return to the Summary Table.

表 7-25. T_LSB_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	T_CH_RESULT [7:0]	R	0h	T-channel data conversion results, LSB 8 bits.

7.6.19 X_MSB_RESULT Register (Offset = 12h) [Reset = 00h]

X_MSB_RESULT is shown in 表 7-26.

Return to the Summary Table.

表 7-26. X_MSB_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	X_CH_RESULT [15:8]	R	0h	X-channel data conversion results, MSB 8 bits.

7.6.20 X_LSB_RESULT Register (Offset = 13h) [Reset = 00h]

X_LSB_RESULT is shown in 表 7-27.

Return to the Summary Table.

表 7-27. X_LSB_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	X_CH_RESULT [7:0]	R	0h	X-channel data conversion results, LSB 8 bits.

7.6.21 Y_MSB_RESULT Register (Offset = 14h) [Reset = 00h]

Y_MSB_RESULT is shown in 表 7-28.

Return to the Summary Table.

表 7-28. Y_MSB_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Y_CH_RESULT [15:8]	R	0h	Y-channel data conversion results, MSB 8 bits.

7.6.22 Y_LSB_RESULT Register (Offset = 15h) [Reset = 00h]

Y_LSB_RESULT is shown in 表 7-29.

Return to the Summary Table.

表 7-29. Y_LSB_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Y_CH_RESULT [7:0]	R	0h	Y-channel data conversion results, LSB 8 bits.

7.6.23 Z_MSB_RESULT Register (Offset = 16h) [Reset = 00h]

Z_MSB_RESULT is shown in 表 7-30.

Return to the Summary Table.

表 7-30. Z_MSB_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Z_CH_RESULT [15:8]	R	0h	Z-channel data conversion results, MSB 8 bits.

7.6.24 Z_LSB_RESULT Register (Offset = 17h) [Reset = 00h]

Z_LSB_RESULT is shown in 表 7-31.

Return to the Summary Table.

表 7-31. Z_LSB_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	Z_CH_RESULT [7:0]	R	0h	Z-channel data conversion results, LSB 8 bits.

7.6.25 CONV_STATUS Register (Offset = 18h) [Reset = 10h]

CONV_STATUS is shown in 表 7-32.

Return to the Summary Table.

表 7-32. CONV_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	SET_COUNT	R	0h	Rolling count of conversion data sets.
4	POR	R/W1CP	1h	Device powered up, or experienced power-on-reset. Bit is clear when host writes back '1'. 0h = No POR 1h = POR occurred
3-2	RESERVED	R	0h	Reserved

表 7-32. CONV_STATUS Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
1	DIAG_STATUS	R	0h	Detect any internal diagnostics fail which include VCC UV, internal memory CRC error, $\overline{INT}$ pin error and internal clock error. 0h = No diagnostic fail 1h = Diagnostic fail detected
0	RESULT_STATUS	R	0h	Conversion data buffer is ready to be read. 0h = Conversion data not complete 1h = Conversion data complete

7.6.26 ANGLE_RESULT_MSB Register (Offset = 19h) [Reset = 00h]

ANGLE_RESULT_MSB is shown in 表 7-33.

Return to the Summary Table.

表 7-33. ANGLE_RESULT_MSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ANGLE_RESULT_MSB	R	0h	Angle measurement result in degree. The data is displayed from 0 to 360 degree in 13 LSB bits after combining the ANGLE_RESULT_MSB and _LSB bits. The 4 LSB bits allocated for fraction of an angle in the format (xxxx/16).

7.6.27 ANGLE_RESULT_LSB Register (Offset = 1Ah) [Reset = 00h]

ANGLE_RESULT_LSB is shown in 表 7-34.

Return to the Summary Table.

表 7-34. ANGLE_RESULT_LSB Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	ANGLE_RESULT_LSB	R	0h	Angle measurement result in degree. The data is displayed from 0 to 360 degree in 13 LSB bits after combining the ANGLE_RESULT_MSB and _LSB bits. The 4 LSB bits allocated for fraction of an angle in the format (xxxx/16).

7.6.28 MAGNITUDE_RESULT Register (Offset = 1Bh) [Reset = 00h]

MAGNITUDE_RESULT is shown in 表 7-35.

Return to the Summary Table.

表 7-35. MAGNITUDE_RESULT Register Field Descriptions

Bit	Field	Type	Reset	Description
7-0	MAGNITUDE_RESULT	R	0h	Resultant vector magnitude during angle measurement. This value should be constant during 360-degree on-axis angle measurement. The magnitude in mT can be calculated as (MAGNITUDE_RESULT*256)/(LSB/mT) where the LSB/mT is calculated in 16-bit format as specified in the magnetic characteristics table.

7.6.29 DEVICE_STATUS Register (Offset = 1Ch) [Reset = 10h]

DEVICE_STATUS is shown in 表 7-36.

Return to the Summary Table.

表 7-36. DEVICE_STATUS Register Field Descriptions

Bit	Field	Type	Reset	Description
7-5	RESERVED	R	0h	Reserved
4	INTB_RB	R	1h	Indicates the level that the device is reading back from $\overline{\text{INT}}$ pin. The reset value of DEVICE_STATUS depends on the status of the $\overline{\text{INT}}$ pin at power-up. 0h = $\overline{\text{INT}}$ pin driven low 1h = $\overline{\text{INT}}$ pin status high

表 7-36. DEVICE_STATUS Register Field Descriptions (続き)

Bit	Field	Type	Reset	Description
3	OSC_ER	R/W1CP	0h	Indicates if Oscillator error is detected. Bit is clear when host writes back '1'. 0h = No oscillator error detected 1h = Oscillator error detected
2	INT_ER	R/W1CP	0h	Indicates if $\overline{\text{INT}}$ pin error is detected. Bit is clear when host writes back '1'. 0h = No $\overline{\text{INT}}$ error detected 1h = $\overline{\text{INT}}$ error detected
1	OTP_CRC_ER	R/W1CP	0h	Indicates if OTP CRC error is detected. Bit is clear when host writes back '1'. 0h = No OTP CRC error detected 1h = OTP CRC error detected
0	VCC_UV_ER	R/W1CP	0h	Indicates if VCC undervoltage was detected. Bit is clear when host writes back '1'. 0h = No VCC UV detected 1h = VCC UV detected

8 Application and Implementation

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

8.1.1 Select the Sensitivity Option

Select the highest TMAG5173-Q1 sensitivity option that can measure the required range of magnetic flux density so that the ADC input range is maximized.

Larger-sized magnets and farther sensing distances can generally enable better positional accuracy than very small magnets at close distances, because magnetic flux density increases exponentially with the proximity to a magnet. TI created an online tool to help with simple magnet calculations under the TMAG5173-Q1 product folder on ti.com.

8.1.2 Temperature Compensation for Magnets

The TMAG5173-Q1 temperature compensation is designed to directly compensate the average temperature drift of several magnets as specified in the MAG_TEMPCO register bits. The residual induction (B_r) of a magnet typically reduces by 0.12%/°C for NdFeB, and 0.20%/°C for ferrite magnets as the temperature increases. Set the MAG_TEMPCO bit to default 00b if the device temperature compensation is not needed.

8.1.3 Sensor Conversion

Multiple conversion schemes can be adopted based off the MAG_CH_EN and CONV_AVG register bits settings.

8.1.3.1 Continuous Conversion

The TMAG5173-Q1 can be set in continuous conversion mode when OPERATING_MODE is set to 10b. 図 8-1 shows a few examples of continuous conversion. The input magnetic field is processed in two steps. In the first step, the device spins the Hall sensor elements and integrates the sampled data. In the second step, the ADC block converts the analog signal into digital bits and stores in the corresponding result register. While the ADC starts processing the first magnetic sample, the spin block can start processing another magnetic sample. In this mode, the temperature data is taken at the beginning of each new conversion. This temperature data is used to compensate for the magnetic thermal drift.

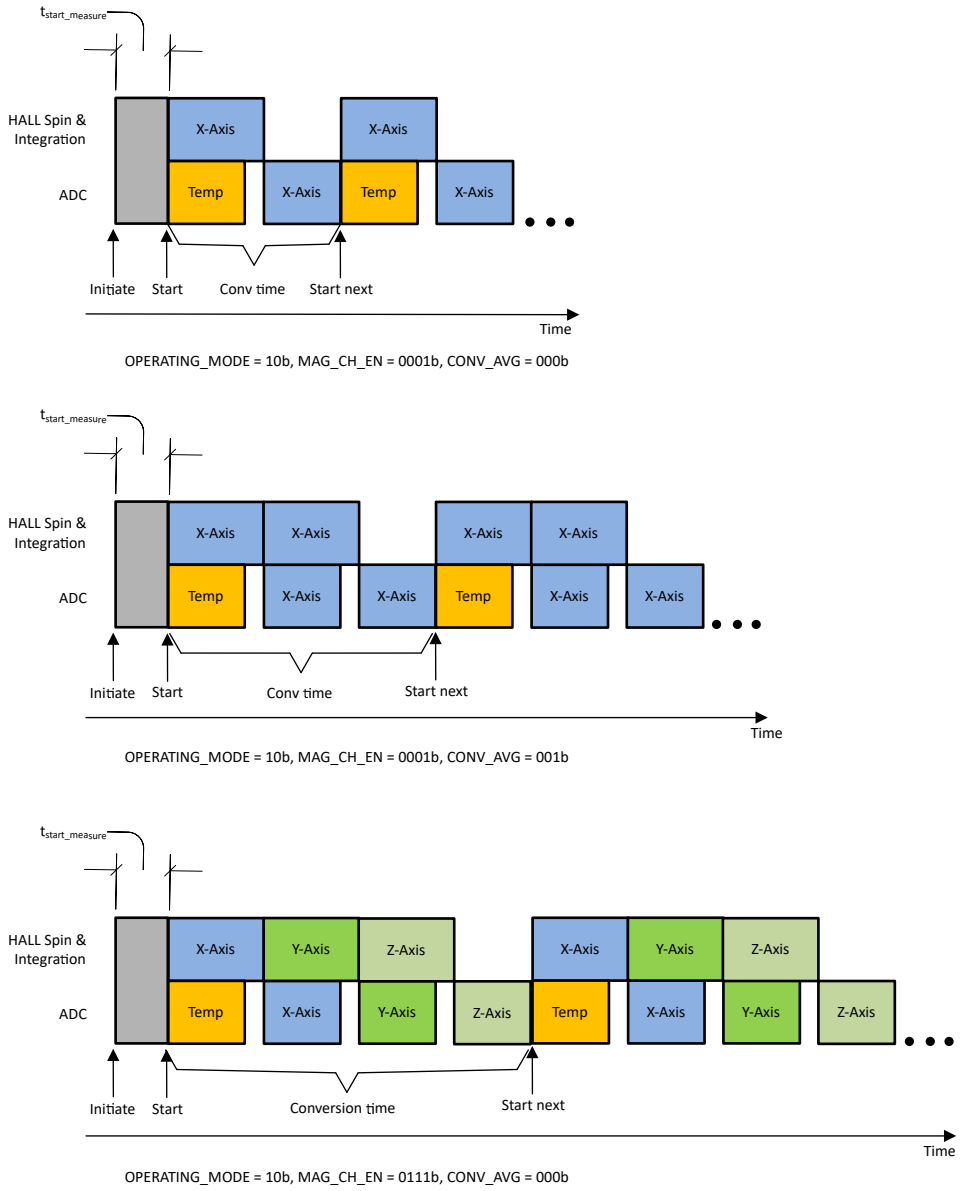


図 8-1. Continuous Conversion Examples

8.1.3.2 Trigger Conversion

The TMAG5173-Q1 supports trigger conversion with OPERATING_MODE set to 00b. The trigger event can be initiated through I^2C command or $\overline{INT}$ signal. 図 8-2 shows an example of trigger conversion with temperature, X, Y, and Z sensors activated.

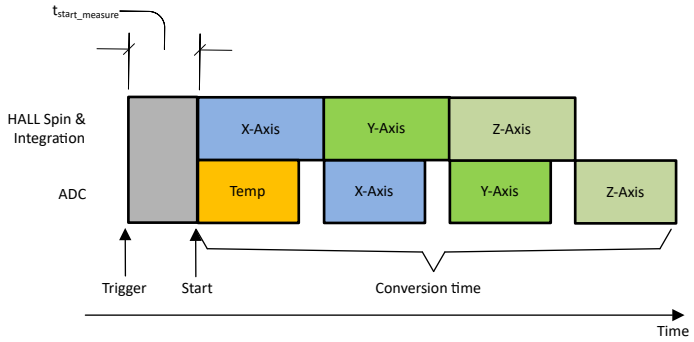


図 8-2. Trigger Conversion for Temperature, X, Y, & Z Sensors

8.1.3.3 Pseudo-Simultaneous Sampling

In absolute angle measurement, application sensor data from multiple axes are required to calculate an accurate angle. The magnetic field data collected at different times through the same signal chain introduces error in angle calculation. The TMAG5173-Q1 offers pseudo-simultaneous sampling data collection modes to eliminate this error. 図 8-3 shows an example where MAG_CH_EN is set at 1011b to collect XZX data. 式 18 shows that the time stamps for the X and Z sensor data are the same.

$$t_Z = \frac{t_{X1} + t_{X2}}{2} \tag{18}$$

where

- t_{X1}, t_Z, t_{X2} are time stamps for X, Z, X sensor data completion as defined in 図 8-3.

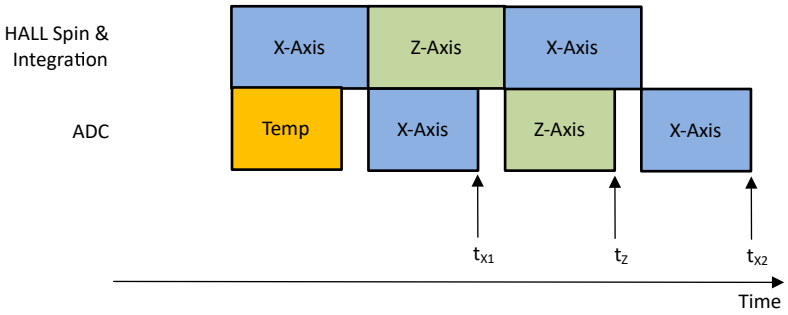


図 8-3. XZX Magnetic Field Conversion

The vertical X, Y sensors of the TMAG5173-Q1 exhibit more noise than the horizontal Z sensor. The pseudo-simultaneous sampling can be used to equalize the noise floor when two set of vertical sensor data are collected against one set of horizontal sensor data, as in examples of XZX or YZY modes.

8.1.4 Magnetic Limit Check

The TMAG5173-Q1 enables magnetic limit checks for single or multiple axes at the same time. 図 8-4 to 図 8-7 show examples of magnetic limit cross detection events while the field going above, below, exiting a magnetic band, and entering a magnetic band. The device will keep generating interrupt with each new conversion if the magnetic fields remain in the shaded regions in the figures. The MAG_THR_DIR and THR_HYST register bits help select different limit cross modes.

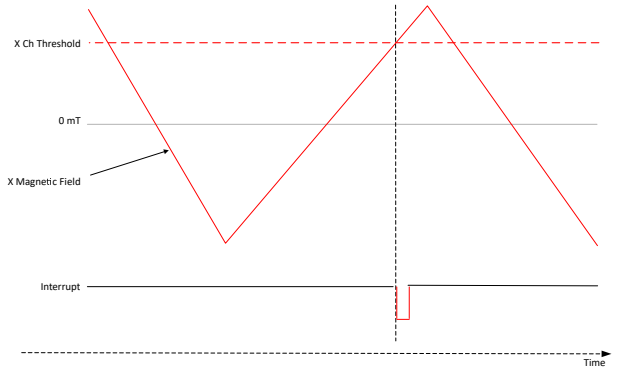


図 8-4. Magnetic Upper Limit Cross Check With MAG_THR_DIR =0b, THR_HYST = 000b

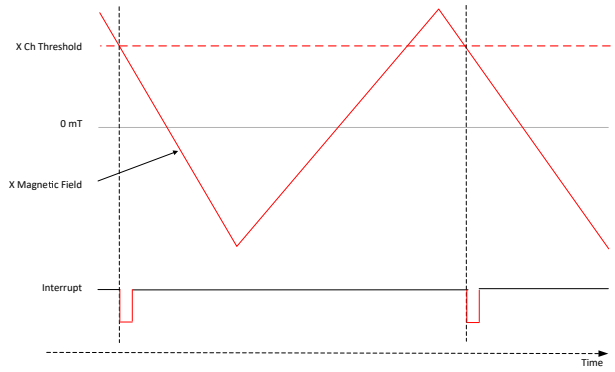


図 8-5. Magnetic Lower Limit Cross Check With MAG_THR_DIR =1b, THR_HYST = 000b

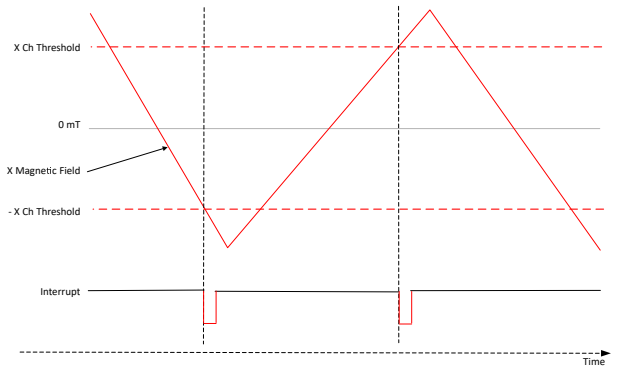


図 8-6. Magnetic Field Going Out of Band Check With MAG_THR_DIR =0b, THR_HYST = 001b

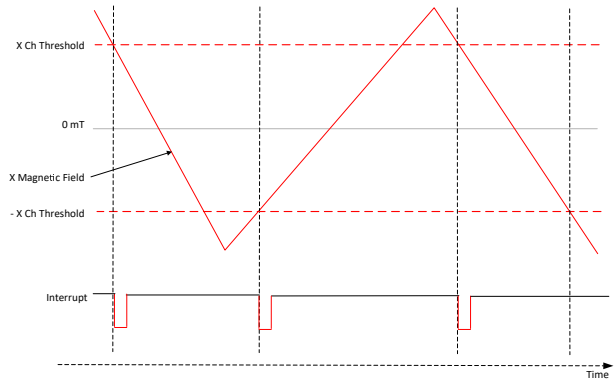


図 8-7. Magnetic Field Entering a Band Check With MAG_THR_DIR =1b, THR_HYST = 001b

8.1.5 Magnetic Threshold Band Cross Detection

表 8-1 shows different threshold band width options supported by the TMAG5173-Q1. For larger threshold band use the A2 orderable. The magnetic threshold band is useful to create programmable magnetic switch and latch hysteresis.

表 8-1. Threshold Band Width (Upper Threshold- Lower Threshold) in mT

THR_HYST Codes	±40-mT Option	±80-mT Option	±133-mT Option	±266-mT Option
	A1/ B1/ C1/ D1 Orderable		A2/ B2/ C2/ D2 Orderable	
010b	0.156	0.312	0.52	1.04
011b	0.312	0.625	1.04	2.08
100b	0.625	1.25	2.08	4.15
101b	1.25	2.5	4.16	8.30
110b	2.5	5.0	8.30	16.63
111b	5.0	10.0	16.63	33.25

8.1.6 Error Calculation During Linear Measurement

The TMAG5173-Q1 offers independent configurations to perform linear position measurements in X, Y, and Z axes. To calculate the expected error during linear measurement, the contributions from each of the individual error sources must be understood. The relevant error sources include sensitivity error, offset, noise, cross axis sensitivity, hysteresis, nonlinearity, drift across temperature, drift across life time, and so forth. For a 3-axis Hall

solution like the TMAG5173-Q1, the cross-axis sensitivity and hysteresis error sources are insignificant. Use 式 19 to estimate the linear measurement error calculation at room temperature.

$$Error_{LM\_25C} = \frac{\sqrt{(B \times SENS_{ER})^2 + B_{off}^2 + N_{RMS\_25}^2}}{B} \times 100\% \quad (19)$$

where

- $Error_{LM\_25C}$ is total error in % during linear measurement at 25°C.
- B is input magnetic field.
- $SENS_{ER}$ is sensitivity error in decimal number at 25°C. As an example, enter 0.05 for sensitivity error of 5%.
- B_{off} is offset error at 25°C.
- N_{RMS_25} is RMS noise at 25°C.

In many applications, system level calibration at room temperature can nullify the offset and sensitivity errors at 25°C. The noise errors can be reduced by internally averaging by up to 32x on the device in addition to the averaging that could be done in the microcontroller. Use 式 20 to estimate the linear measurement error across temperature after calibration at room temperature.

$$Error_{LM\_Temp} = \frac{\sqrt{(B \times SENS_{DR})^2 + B_{off\_DR}^2 + N_{RMS\_Temp}^2}}{B} \times 100\% \quad (20)$$

where

- $Error_{LM\_Temp}$ is total error in % during linear measurement across temperature after room temperature calibration.
- B is input magnetic field.
- $SENS_{DR}$ is sensitivity drift in decimal number from value at 25°C. As an example, enter 0.05 for sensitivity drift of 5%.
- B_{off_DR} is offset drift from value at 25°C.
- N_{RMS_Temp} is RMS noise across temperature.

If room temperature calibration is not performed, sensitivity and offset errors at room temperature must also account for total error calculation across temperature (see 式 21).

$$Error_{LM\_Temp\_NCal} = \frac{\sqrt{(B \times SENS_{ER})^2 + (B \times SENS_{DR})^2 + B_{off}^2 + B_{off\_DR}^2 + N_{RMS\_Temp}^2}}{B} \times 100\% \quad (21)$$

where

- $Error_{LM\_Temp\_NCal}$ is total error in % during linear measurement across temperature without room temperature calibration.

注

In this section, error sources such as system mechanical vibration, magnet temperature gradient, earth magnetic field, nonlinearity, lifetime drift, and so forth, are not considered. The user must take these additional error sources into account while calculating overall system error budgets.

8.1.7 Error Calculation During Angular Measurement

The TMAG5173-Q1 offers on-chip CORDIC to measure angle data from any of the two magnetic axes. The linear magnetic axis data can be used to calculate the angle using an external CORDIC as well. To calculate the expected error during angular measurement, the contributions from each individual error source must be understood. The relevant error sources include sensitivity error, offset, noise, axis-axis mismatch, nonlinearity, drift across temperature, drift across life time, and so forth. Use the Angle Error Calculation Tool to estimate the total error during angular measurement.

8.2 Typical Applications

Magnetic 3D sensors are very popular due to contactless and reliable measurements, especially in applications requiring long-term measurements in rugged environments. The TMAG5173-Q1 offers design flexibility in wide range of industrial and personal electronics applications. In this section three common application examples are discussed in details.

8.2.1 Angle Measurement

Magnetic angle sensors are very popular due to contactless and reliable measurements, especially in applications requiring long-term measurements in rugged environments. The TMAG5173-Q1 offers an on-chip angle calculator providing angular measurement based off any two of the magnetic axes. The two axes of interest can be selected in the ANGLE_EN register bits. The device offers angle output in complete 360 degree scale. Take several error sources into account for angle calculation, including sensitivity error, offset error, linearity error, noise, mechanical vibration, temperature drift, and so forth.

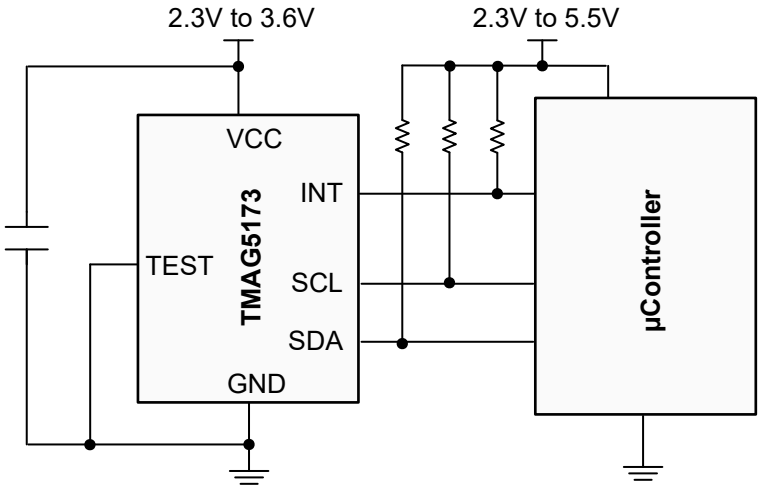


図 8-8. TMAG5173-Q1 Application Diagram for Angle Measurement

8.2.1.1 Design Requirements

Use the parameters listed in 表 8-2 for this design example.

表 8-2. Design Parameters

DESIGN PARAMETERS	ON-AXIS MEASUREMENT	OFF-AXIS MEASUREMENT
Device	TMAG5173A1-Q1	TMAG5173A1-Q1
VCC	3.3 V	3.3 V
Device Position	Directly under the magnet	At the adjacent side of the magnet
Magnet	Cylinder: 4.7625-mm diameter, 12.7-mm thick, neodymium N52, Br = 1480	Cylinder: 4.7625-mm diameter, 12.7-mm thick, neodymium N52, Br = 1480
Magnetic Range Selection	Select the same range for both axes based off the highest possible magnetic field seen by the sensor	Select the same range for both axes based off the highest possible magnetic field seen by the sensor
RPM	<600	<600
Desired Accuracy	<2° for 360° rotation	<2° for 360° rotation

8.2.1.2 Detailed Design Procedure

For accurate angle measurement, the two axes amplitudes must be normalized by selecting the proper gain adjustment value in the MAG_GAIN_CONFIG register. The gain adjustment value is a fractional decimal number between 0 and 1. The following steps must be followed to calculate this fractional value:

- Set the device at 32x average mode and rotate the shaft full 360 degree.
- Record the two axes sensor ADC codes for the full 360 degree rotation.
- A normalized plot for the full 360 degree rotations are represented in 図 8-10 or 図 8-11.
- Measure the maximum peak-peak ADC code delta for each axis, A_X and A_Y.
- If $A_X > A_Y$, set the MAG_GAIN_CH register bit to 0b. Calculate the gain adjustment value for X axis: $G_X = \frac{A_Y}{A_X}$
- If $A_X < A_Y$, set the MAG_GAIN_CH register bit to 1b. Calculate the gain adjustment value for Y axis: $G_Y = \frac{1}{G_X}$
- The target binary gain setting at the GAIN VALUE register bits are calculated from the equation, G_X or G_Y = $GAIN\_VALUE_{decimal}$/ 256.

Example 1: If $A_X = A_Y$ = 60,000, the GAIN_VALUE register bits are set at default 0000 0000b.

Example 2: If A_X= 60,000, A_Y = 45,000, the G_X = 45,000/60,000 =0.75. Set MAG_GAIN_CH to 0b and GAIN_VALUE to 1100 0000b.

Example 3: If A_X= 45,000, A_Y = 60,000, the G_X = (60,000/45,000) =1.33. Since G_X >1, the gain adjustment needs to be applied to Y axis with $G_Y = 1/G_X$. Set MAG_GAIN_CH to 1b and GAIN_VALUE to 1100 0000b.

8.2.1.2.1 Gain Adjustment for Angle Measurement

Common measurement topology include angular position measurements in on-axis or off-axis angular measurements shown in 図 8-9. Select the on-axis measurement topology whenever possible as this offers the best optimization of magnetic field and the device measurement ranges. The TMAG5173-Q1 offers on-chip gain adjustment option to account for mechanical position misalignments.

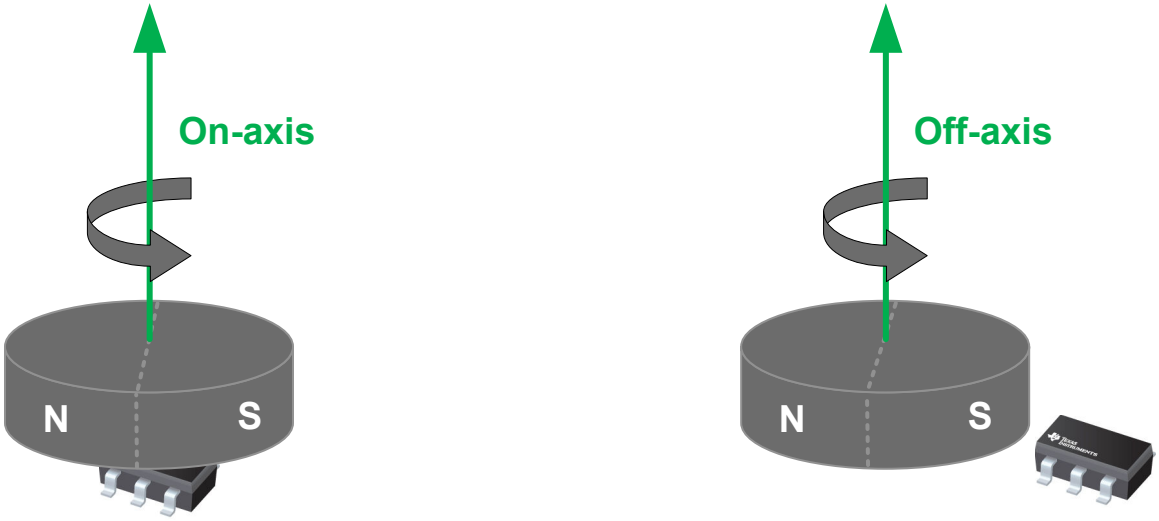


図 8-9. On-Axis vs Off-Axis Angle Measurements

8.2.1.3 Application Curves

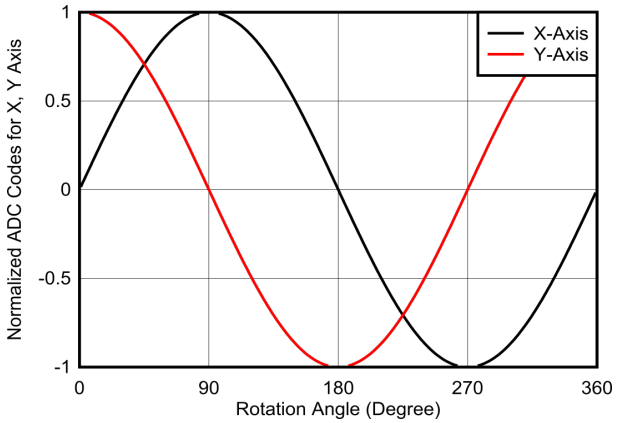


図 8-10. X and Y Sensor Data for Full 360 Degree Rotation for On-Axis Measurement

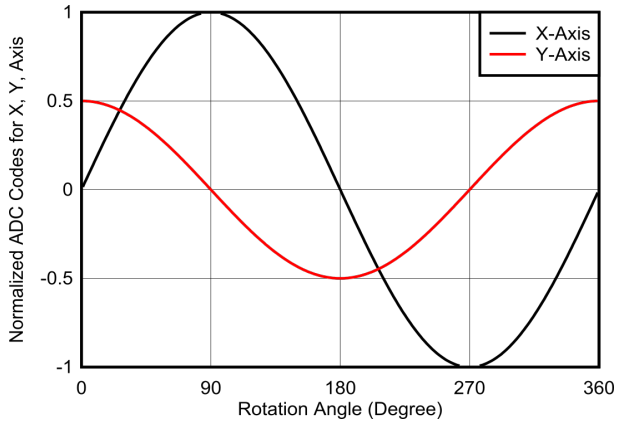


図 8-11. X and Y Sensor Data for Full 360 Degree Rotation for Off-Axis Measurement

8.2.2 I²C Address Expansion

The TMAG5173-Q1 is offered in four different factory-programmed I²C addresses. The device also supports additional I²C addresses through the configuration of the I2C_ADDRESS register. There are 7 bits to select 128 different addresses. Take system limitations like bus loading, maximum clock frequency, available GPIOs from a microcontroller, and so forth, in account before selecting maximum number of sensors in a single I²C bus.

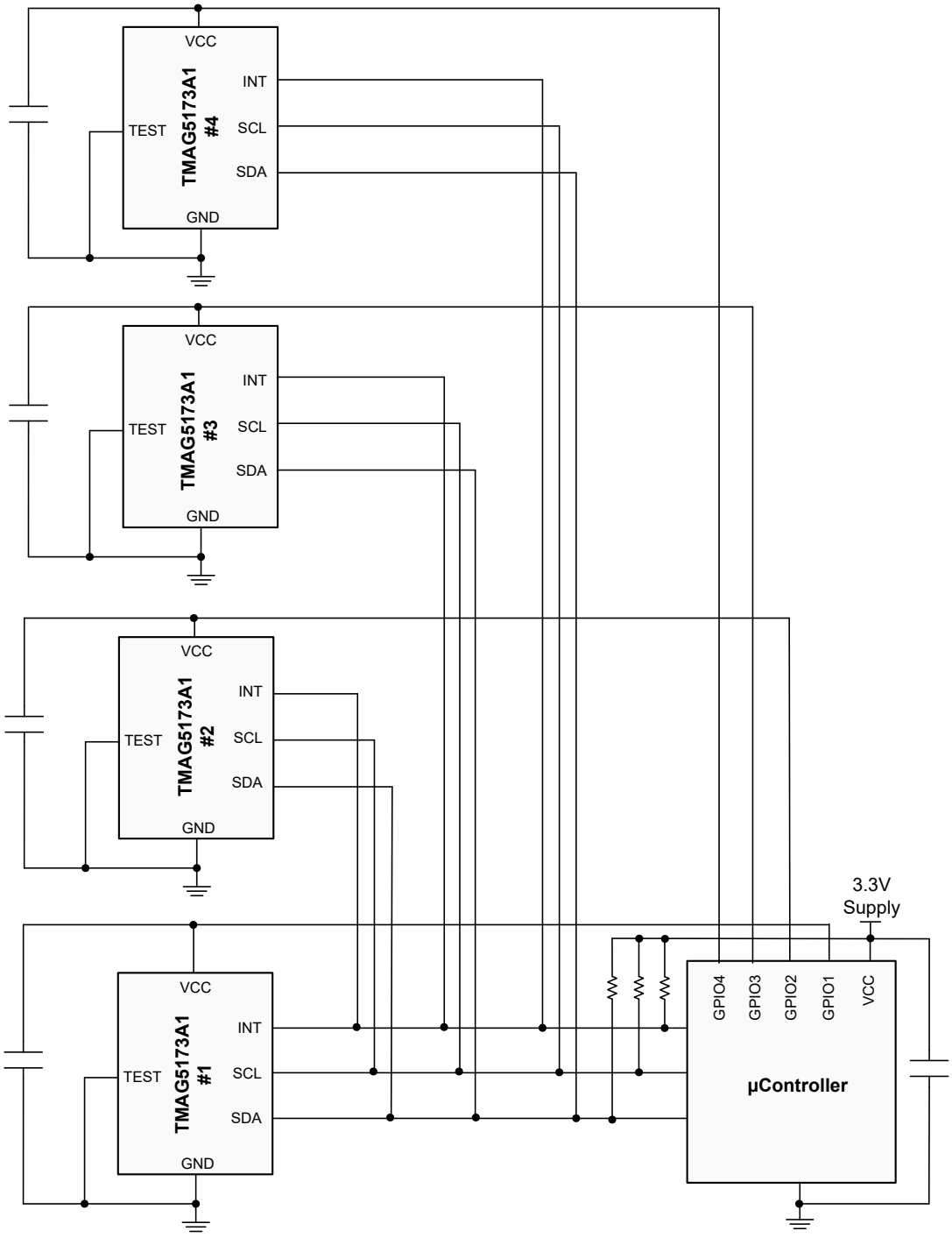


図 8-12. TMAG5173-Q1 Application Diagram for I²C Address Expansion

8.2.2.1 Design Requirements

Use the parameters listed in 表 8-2 for this design example.

表 8-3. Design Parameters

PARAMETERS	DESIGN TARGET
Device orderable	TMAG5173A1-Q1
VCC	3.3 V

表 8-3. Design Parameters (続き)

PARAMETERS	DESIGN TARGET
# of Devices in same bus	4 (same method can be used to expand the number of sensors in the I²C bus)
Design objective	Optimize the # GPIO and component count
Current supply per sensor	5-mA, supplied by a microcontroller GPIO

8.2.2.2 Detailed Design Procedure

Select GPIO with current supply capability of 5 mA. 図 8-12 shows that the SCL, SDA lines and $\overline{INT}$ pin can be shared. However, the function of the $\overline{INT}$ pin must be analyzed when shared by multiple sensors. As an example, if the sensors are configured to generate interrupt through the $\overline{INT}$ pin, the microcontroller needs to read all the sensors to determine which specific one sending the interrupt. Take the following steps sequentially to assign new I²C addresses to the four TMAG5173-Q1 shown in 図 8-13:

- Turn on the GPIO#1 and wait until $t_{start\_power\_up}$ time is elapsed.
- Address the device#1 with factory programmed address. Write to the I2C_ADDRESS register to assign a new address.
- Turn on the GPIO#2 and wait until $t_{start\_power\_up}$ time is elapsed.
- Address the device#2 with factory programmed address. Write to the I2C_ADDRESS register to assign a new unique address.
- Turn on the GPIO#3 and wait until $t_{start\_power\_up}$ time is elapsed.
- Address the device#3 with factory programmed address. Write to the I2C_ADDRESS register to assign a new unique address.
- Turn on the GPIO#4 and wait until $t_{start\_power\_up}$ time is elapsed.
- Address the device#4 with factory programmed address. Write to the I2C_ADDRESS register to assign a new unique address.

Repeat the above steps if there is a power outage or power-up reset condition.

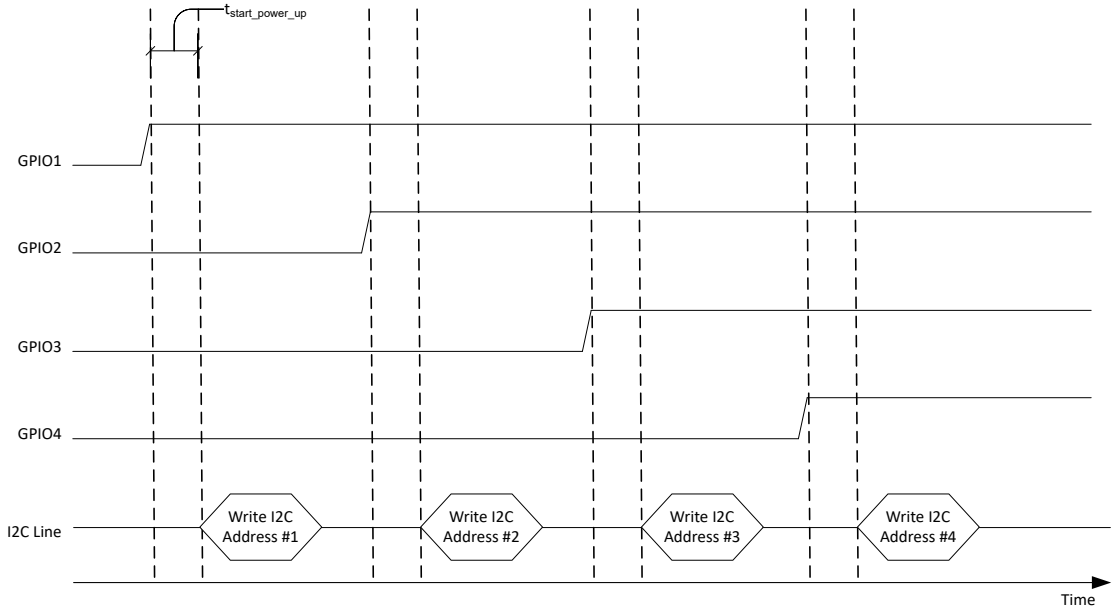


図 8-13. Power-Up Timing and I²C Address Allocation for the Four Sensors

8.3 Best Design Practices

The TMAG5173-Q1 updates the result registers at the end of a conversion. I²C read of the result register must be synchronized with the conversion update time to avoid reading a result data while the result register is being

updated. For applications with a tight timing budget, use the $\overline{\text{INT}}$ signal to notify the primary when a conversion is complete.

8.4 Power Supply Recommendations

A decoupling capacitor close to the device must be used to provide local energy with minimal inductance. TI recommends using a ceramic capacitor with a value of at least 0.01 µF. Connect the TEST pin to ground.

8.5 Layout

8.5.1 Layout Guidelines

Magnetic fields pass through most nonferromagnetic materials with no significant disturbance. Embedding Hall effect sensors within plastic or aluminum enclosures and sensing magnets on the outside is common practice. Magnetic fields also easily pass through most printed circuit boards (PCBs), which makes placing the magnet on the opposite side of the PCB possible.

8.5.2 Layout Example

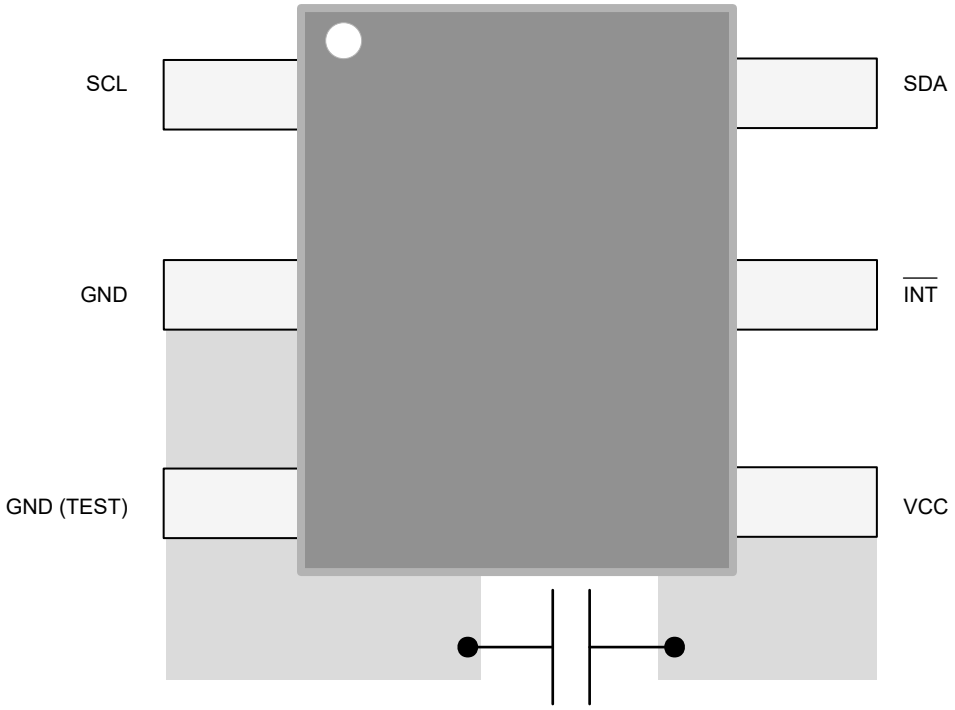


図 8-14. Layout Example With TMAG5173-Q1

9 デバイスおよびドキュメントのサポート

9.1 ドキュメントのサポート

9.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *HALL-ADAPTER-EVM User's Guide* (SLYU043)
- Texas Instruments, *TMAG5173 Evaluation Manual user's guide* (SLYU058)
- Texas Instruments, *Angle Measurement With Multi-Axis Linear Hall-Effect Sensors* application note (SBAA463)
- Texas Instruments, *Absolute Angle Measurements for Rotational Motion Using Hall-Effect Sensors* application brief (SBAA503)
- Texas Instruments, *Limit Detection for Tamper and End-of-Travel Detection Using Hall-Effect Sensors* application brief (SBOA514)

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

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9.4 商標

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9.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMAG5173A1QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125		Samples
TMAG5173A2QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125		Samples
TMAG5173B1QDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

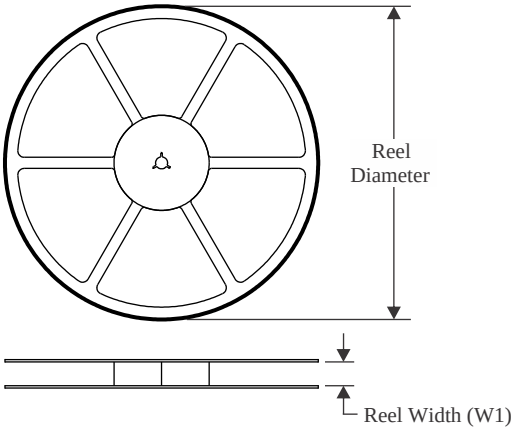
(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

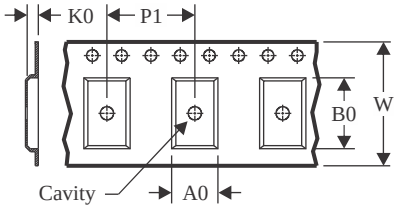
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

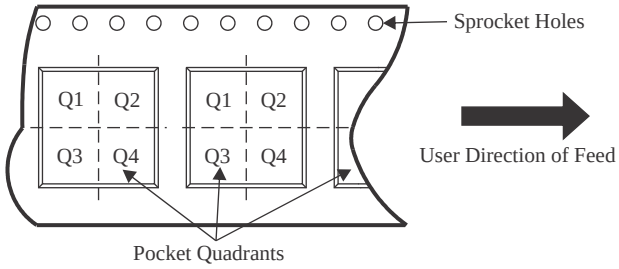


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

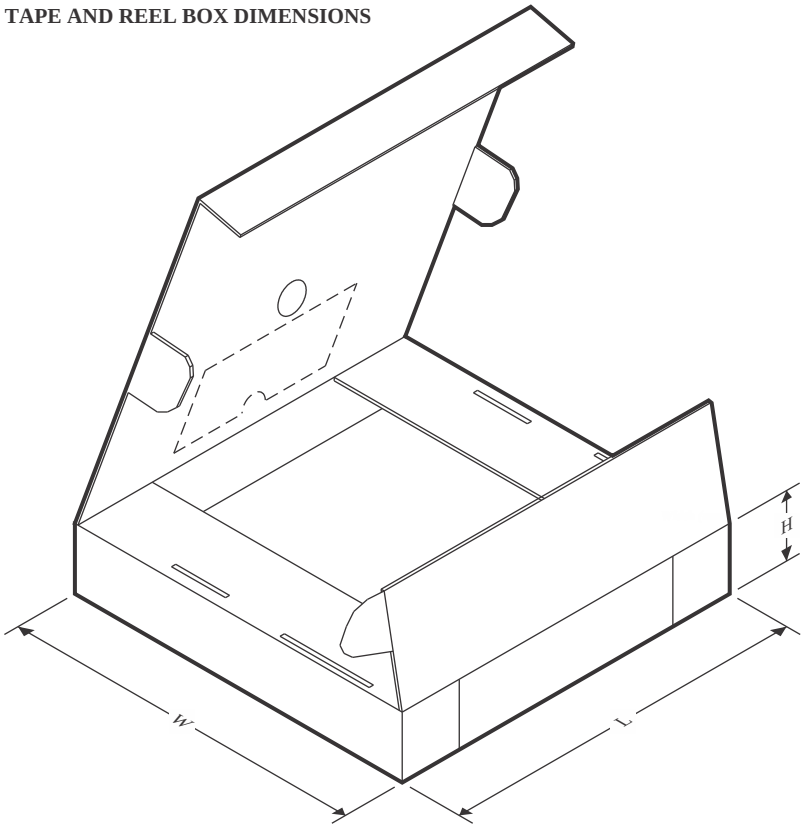
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMAG5173A1QDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TMAG5173A2QDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TMAG5173B1QDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

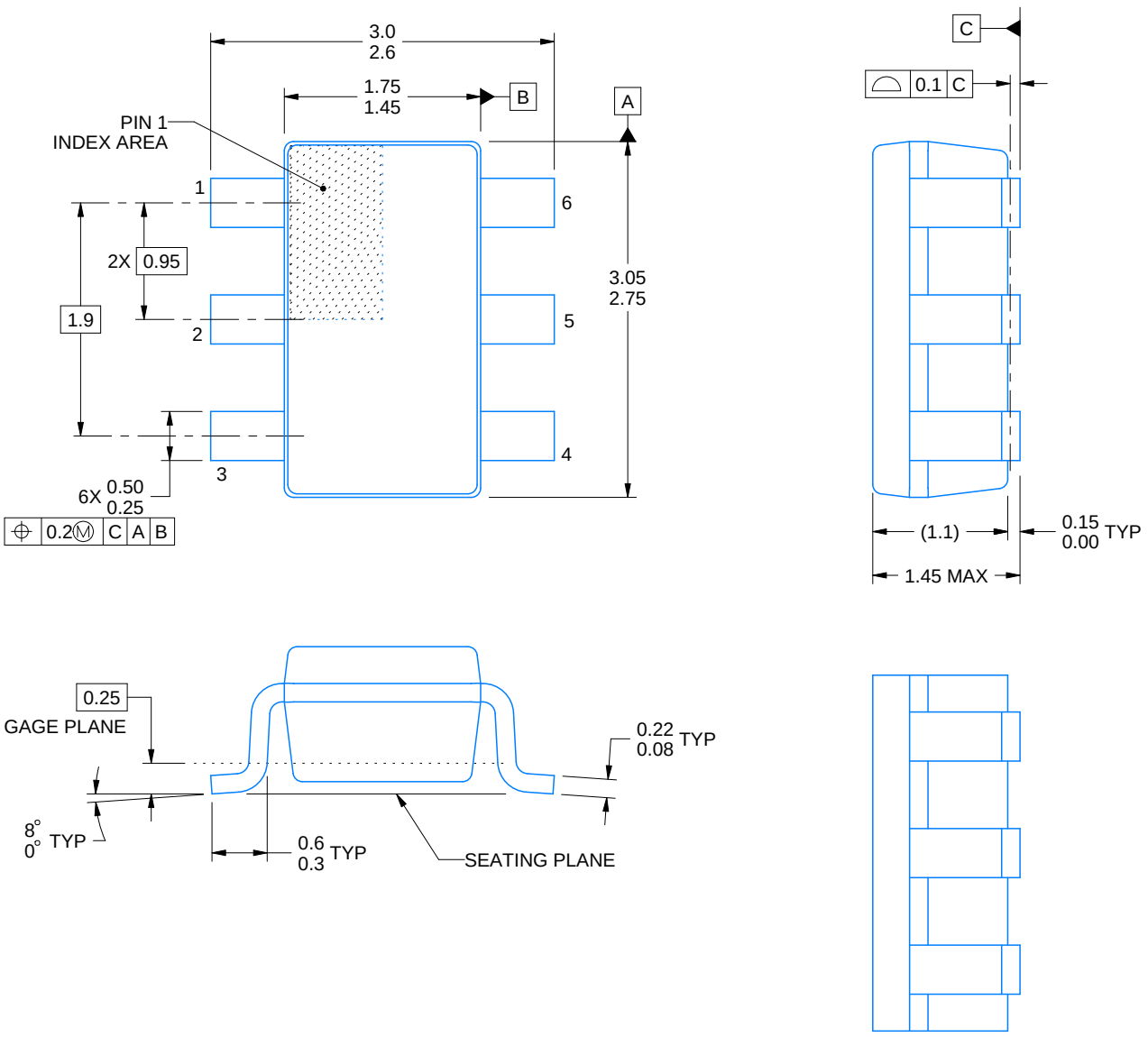
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMAG5173A1QDBVRQ1	SOT-23	DBV	6	3000	190.0	190.0	30.0
TMAG5173A2QDBVRQ1	SOT-23	DBV	6	3000	190.0	190.0	30.0
TMAG5173B1QDBVRQ1	SOT-23	DBV	6	3000	190.0	190.0	30.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



ALTERNATIVE PACKAGE SINGULATION VIEW

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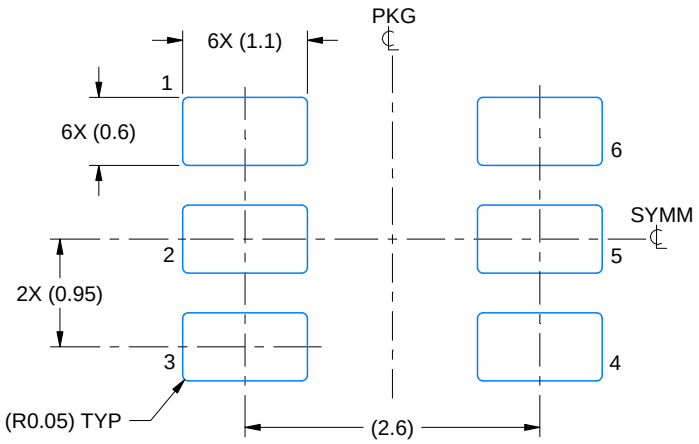
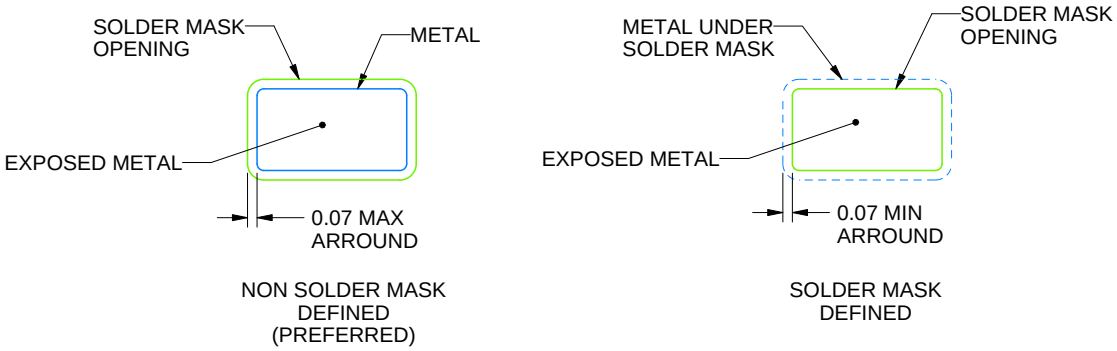
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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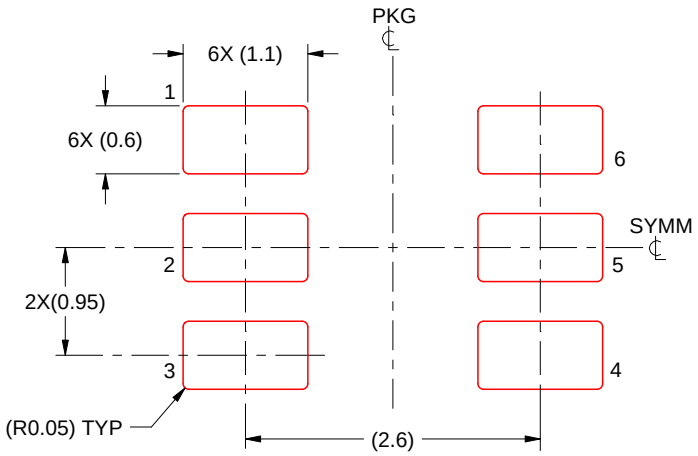
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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