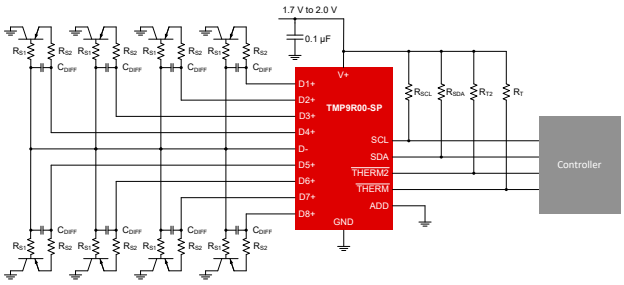
TMP9R00-SP 9 チャネル (リモート×8、ローカル×1) 高精度温度センサ

1 特長

- QMLV 認定済み:5962R2021401VXC
  - 10mrad/s の低線量率 (LDR) において、総照射線量 (TID) 100krad(Si) までの放射線耐性保証 (RHA)
  - 125℃において 76MeV-cm2/mg のシングル・イベント・ラッチアップ (SEL) 耐性
  - 熱的に強化された 16 リードのセラミック HKT パッケージ
- 8 チャネルのリモート・ダイオード温度センサの精度:±1.5℃
- ローカル温度センサの精度:±1.5℃
- 温度分解能:0.0625℃
- ロジック電圧範囲:1.7V～3.6V
- 電源電圧範囲:1.7V～2.0V
- 動作電流:67µA (1SPS、全チャネルがアクティブ)
- 0.3µA のシャットダウン電流
- リモート・ダイオード:直列抵抗のキャンセル、η-係数補正、オフセット補正、ダイオードの障害検出
- レジスタ・ロック機能により主要レジスタを保護
- I²C または SMBus™ 互換の 2 線式インターフェイス、アドレスはピンによりプログラム可能

2 アプリケーション

- 衛星
- 航空
- 宇宙船での FPGA、ADC、DAC、ASIC の温度監視
- 宇宙船の室内整備およびテレメトリー



代表的なアプリケーション回路図

3 概要

TMP9R00-SP デバイスは、放射線耐性強化、マルチゾーン、高精度、低消費電力の温度センサで、2 線式の SMBus または I²C 互換インターフェイスを使用します。最大 8 つのリモートおよび 1 つのローカル温度ゾーンを同時に監視でき、システム内で温度測定を集約することにより、設計の複雑性を低減できます。代表的な使用例として、MCU、GPU、ADC、DAC、FPGA など、さまざまな高消費電力デバイスの温度監視があります。直列抵抗のキャンセル、プログラム可能な理想係数、温度オフセット補正、温度制限などの高度な機能が搭載されているため、堅牢な熱監視ソリューションを実現できます。

各リモート・チャネルとローカル・チャネルには、個別にプログラム可能な 2 つのスレッショルドがあり、対応する温度が制限を超えたときにトリガされます。スレッショルド付近での頻繁な切り替わりを回避するため、ヒステリシス設定をプログラム可能です。

TMP9R00-SP は、高精度 (±1.5℃)、高分解能 (0.0625℃) の測定能力を備えています。このデバイスは、低電圧レール (1.7V～2.0V)、一般的な 2 線式インターフェイス (1.7V～3.6V)、-55℃～125℃の動作温度範囲、-55℃～150℃のリモート接合部温度範囲に対応しています。

パッケージ情報(1)

型番	グレード	パッケージ	本体サイズ (公称)
5962R2021401VXC	QMLV RHA	CFP (16)	10.16mm × 7.10mm
TMP9R00HKT/EM	エンジニアリング・サンプル(2)	CFP (16)	10.16mm × 7.10mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

(2) これらのユニットは、技術的な評価のみを目的としています。標準とは異なるフローに従って処理されています。これらのユニットは、認定、量産、放射線テスト、航空での使用には適していません。これらの部品は、MIL に規定されている温度範囲 -55℃～125℃、または動作寿命の全体にわたる性能を保証されていません。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (December 2021) to Revision A (August 2022)	Page
• 「パッケージ情報」表から 5962R2021401VXC QMLV グレード・オプションを削除	1
• Added a maximum value for the input capacitance parameter	5
• Moved the *Power Supply Recommendations* and *Layout* sections to the *Application and Implementation* section	31

5 Pin Configuration and Functions

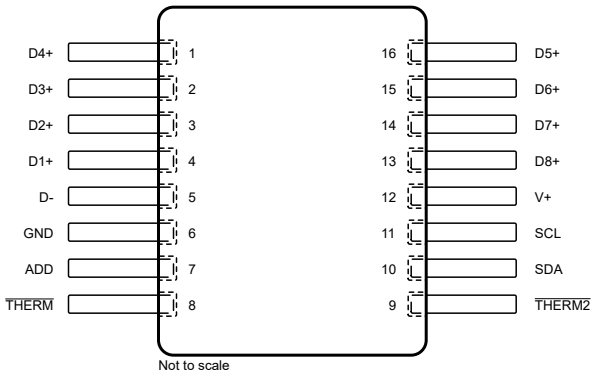


図 5-1. TMP9R00-SP HKT Package 16-Pin CFP Top View

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
D4+	1	Analog input	Positive connection to remote temperature sensors. A total of 8 remote channels are supported. An unused channel must be connected to D–.
D3+	2	Analog input	Positive connection to remote temperature sensors. A total of 8 remote channels are supported. An unused channel must be connected to D–.
D2+	3	Analog input	Positive connection to remote temperature sensors. A total of 8 remote channels are supported. An unused channel must be connected to D–.
D1+	4	Analog input	Positive connection to remote temperature sensors. A total of 8 remote channels are supported. An unused channel must be connected to D–.
D-	5	Analog input	Negative connection to remote temperature sensors. Common for 8 remote channels.
GND	6	Ground	Supply ground connection
ADD	7	Digital input	Address select. Connect to GND, V+, SDA, or SCL.
$\overline{\text{THERM}}$	8	Digital output	Thermal shutdown or fan-control pin. Active low; open-drain; requires a pullup resistor to a voltage between 1.7 V and 3.6 V, not necessarily V+. If this pin is not used it may be left open or grounded.
$\overline{\text{THERM2}}$	9	Digital output	Second $\overline{\text{THERM}}$ output. Active low; open-drain; requires a pullup resistor to a voltage between 1.7 V and 3.6V, not necessarily V+. If this pin is not used it may be left open or grounded.
SDA	10	Bidirectional digital input/output	Serial data line for I^2C or SMBus compatible two-wire interface. Open-drain; requires a pullup resistor to a voltage between 1.7 V and 3.6V, not necessarily V+.
SCL	11	Digital input	Serial clock line for I^2C- or SMBus compatible two-wire interface. Requires a pullup resistor to a voltage between 1.7 V and 3.6V (not necessarily V+) if driven by an open-drain output.
V+	12	Power Supply	Positive supply voltage, 1.7 V to 2.0V; requires 0.1-µF bypass capacitor to ground.
D8+	13	Analog input	Positive connection to remote temperature sensors. A total of 8 remote channels are supported. An unused channel must be connected to D–.
D7+	14	Analog input	Positive connection to remote temperature sensors. A total of 8 remote channels are supported. An unused channel must be connected to D–.
D6+	15	Analog input	Positive connection to remote temperature sensors. A total of 8 remote channels are supported. An unused channel must be connected to D–.
D5+	16	Analog input	Positive connection to remote temperature sensors. A total of 8 remote channels are supported. An unused channel must be connected to D–.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Power supply	V+	–0.3	2.3	V
Input voltage	$\overline{\text{THERM}}$, $\overline{\text{THERM2}}$, SDA, SCL and ADD only	–0.3	6	V
	D+1 through D+8	–0.3	((V+) + 0.3) and ≤6.0V	
	D- only	–0.3	0.3	
Input current	SDA Sink	-25		mA
	All other pins	-10	10	
Operating temperature		–55	150	°C
Junction temperature (T_J max)			150	°C
Storage temperature, T_{stg}		–60	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute maximum ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If briefly operating outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not sustain damage, but it may not be fully functional. Operating the device in this manner may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V+	Supply voltage	1.7		2.0	V
T_A	Operating free-air temperature	–55		125	°C
T_D	Remote junction temperature	-55		150	°C
V_{IO}	IO Voltage (SCL,SDA, $\overline{\text{THERM}}$, $\overline{\text{THERM2}}$)	1.7		3.6	V

6.4 Thermal Information

THERMAL METRIC		TMP9R00-SP HKT (CFP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	52.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	36.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	31.0	°C/W
ψ_{JB}	Junction-to-board characterization parameter	36.2	°C/W

6.5 Electrical Characteristics

At T_A = –55 °C to 125 °C and V+ = 1.7 V to 2.0 V, unless otherwise noted.

PARAMETER			CONDITIONS	MIN	TYP	MAX	UNIT
TEMPERATURE MEASUREMENT							
T_{LOCAL}	Local temperature sensor accuracy		T_A = –55 °C to 125 °C	-1.5	±0.5	1.5	°C
T_{REMOTE}	Remote temperature sensor accuracy		T_A = –55 °C to 125 °C T_D = –55 °C to 150 °C	-2	±0.5	2	°C
	Local Temperature Error Supply Sensitivity			-0.25	±0.05	0.25	°C/V
	Remote Temperature Error Supply Sensitivity			-0.5	±0.1	0.5	°C/V
	Temperature resolution (local and remote)				0.0625		°C
	ADC conversion time		One-shot mode, per channel (local or remote)		16	17	ms
	ADC resolution				13		Bits
	Remote sensor source current	High	Series resistance 1 kΩ (max)		120		µA
		Medium			45		
		Low			7.5		
η	Remote transistor ideality factor		η-Factor Correction registers = 0000h		1.008		
SERIAL INTERFACE							
V_{IH}	High-level input voltage			0.7×(V+)			V
V_{IL}	Low-level input voltage					0.3×(V+)	V
	Hysteresis				200		mV
	SDA output-low sink current			20			mA
V_{OL}	Low-level output voltage		I_O = –15 mA; V+ < 2V			0.2×(V+)	V
	Serial bus input leakage current		0 V ≤ V_{IN} ≤ 3.6 V	–1		1	µA
	Serial bus input capacitance				11	20	pF
DIGITAL INPUTS							
V_{IH}	High-level input voltage			0.7×(V+)			V
V_{IL}	Low-level input voltage			–0.3		0.3×(V+)	V
	Input leakage current		0 V ≤ V_{IN} ≤ 3.6 V	–1		1	µA
	Input capacitance				4	10	pF
DIGITAL OUTPUTS							
	Output-low sink current		V_{OL} = 0.4V	6			mA
V_{OL}	Low-level output voltage		I_O = –6 mA		0.15	0.4	V
I_{OH}	High-level output leakage current		V_O = V+			1	µA
POWER SUPPLY							
V+	Specified supply voltage range			1.7		2.0	V
I_Q	Quiescent current		Active conversion, local sensor		240	375	µA
			Active conversion, remote sensors		400	600	
			Standby mode (between conversions)		15	21	
			Shutdown mode, serial bus inactive		0.3	4	
			Shutdown mode, serial bus active, f_S = 400 kHz		120		
			Shutdown mode, serial bus active, f_S = 2.56 MHz		300		
POR	Power-on reset threshold		Rising edge		1.5	1.65	V
			Falling edge	1.0	1.2	1.35	
POH	Power-on reset hysteresis				0.2		V

6.6 Two-Wire Timing Requirements

At –55°C to 125°C and V+ = 1.7 V to 2.0 V, unless otherwise noted. With controller and target at same V+. Values are based on statistical analysis of samples tested during initial release.

		FAST-MODE		HIGH-SPEED MODE		UNIT
		MIN	MAX	MIN	MAX	
f_{SCL}	SCL operating frequency	0.001	0.4	0.001	2.56	MHz
t_{BUF}	Bus free time between stop and start condition	1300		160		ns
$t_{HD;STA}$	Hold time after repeated start condition. After this period, the first clock is generated.	600		160		ns
$t_{SU;STA}$	Repeated start condition setup time	600		160		ns
$t_{SU;STO}$	Stop condition setup time	600		160		ns
$t_{HD;DAT}$	Data hold time when SDA	0	-(1)	0	130	ns
$t_{VD;DAT}$	Data valid time (2)	0	900	–	–	ns
$t_{SU;DAT}$	Data setup time	100		20		ns
t_{LOW}	SCL clock low period	1300		250		ns
t_{HIGH}	SCL clock high period	600		60		ns
t_F – SDA	Data fall time	20 × (V+/5.5)	300		100	ns
t_F, t_R – SCL	Clock fall and rise time		300		40	ns
t_R	Rise time for SCL ≤ 100 kHz		1000			ns
	Serial bus timeout	15	20	15	20	ms

(1) The maximum t_{HDDAT} could be 0.9 µs for Fast-Mode, and is less than the maximum t_{VDDAT} by a transition time.
(2) t_{VDDATA} = time for data signal from SCL LOW to SDA output (HIGH to LOW, depending on which is worse).

6.6.1 Timing Diagrams

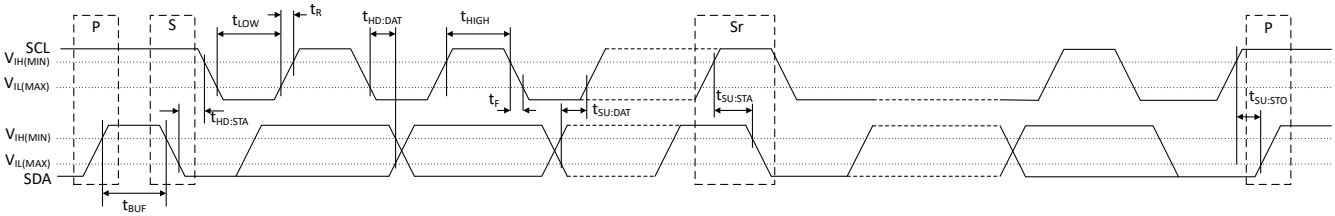


図 6-1. Two-Wire Timing Diagram

6.7 Typical Characteristics

at T_A = 25°C and V+ = 1.8 V (unless otherwise noted)

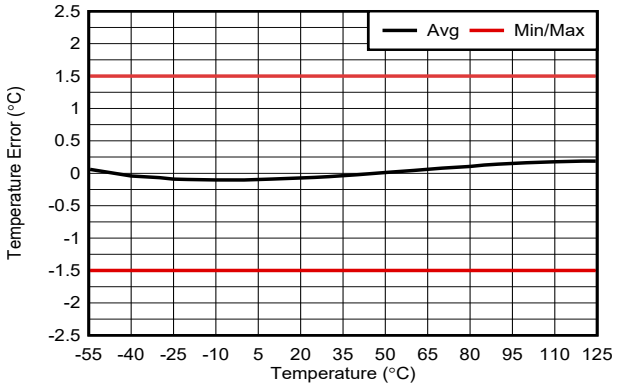


図 6-2. Local Temperature Error vs Ambient Temperature

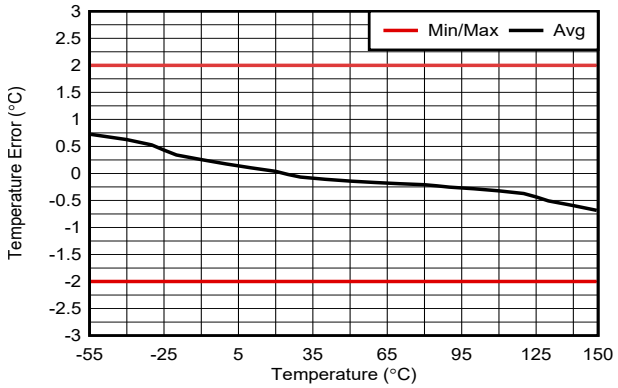


図 6-3. Remote Temperature Error vs Device Junction Temperature

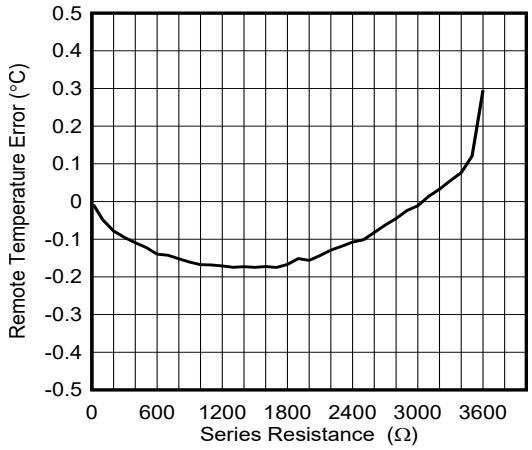
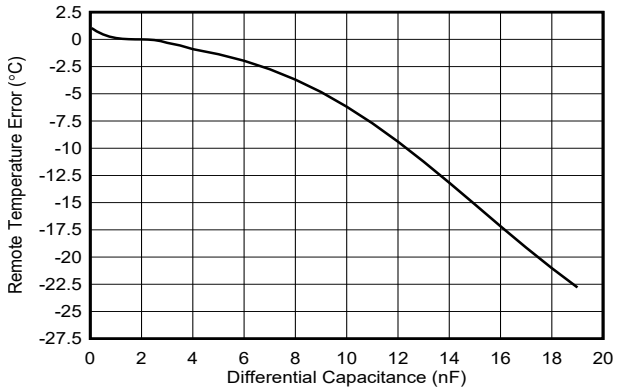


図 6-4. Remote Temperature Error vs Series Resistance



No physical series resistance on D+, D– pins during measurement

図 6-5. Remote Temperature Error vs Differential Capacitance

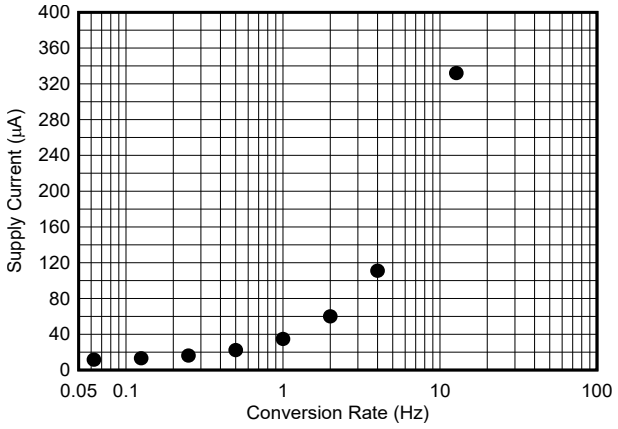


図 6-6. Quiescent Current vs Conversion Rate

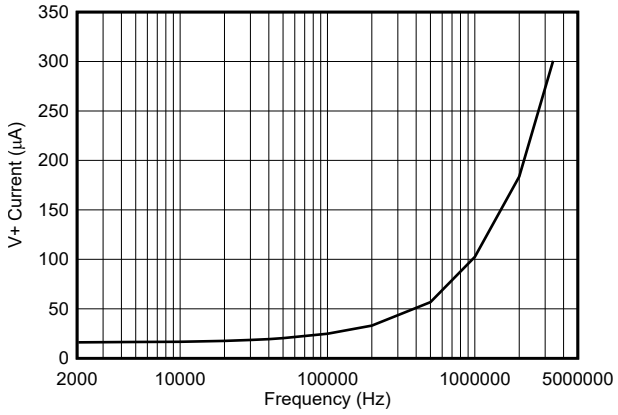


図 6-7. Shutdown Quiescent Current vs SCL Clock Frequency

6.7 Typical Characteristics (continued)

at T_A = 25°C and V+ = 1.8 V (unless otherwise noted)

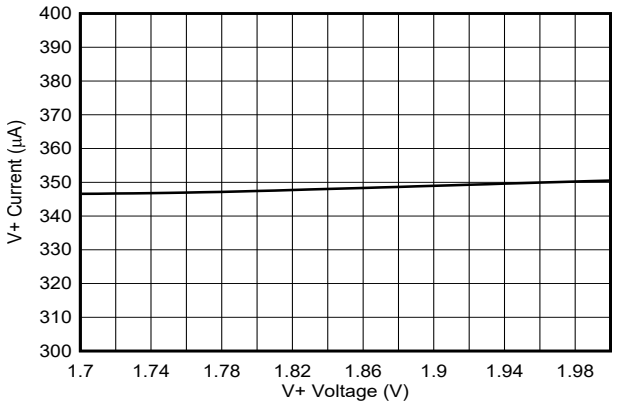


図 6-8. Quiescent Current vs Supply Voltage (at Default Conversion Rate of 16 Conversions Per Second)

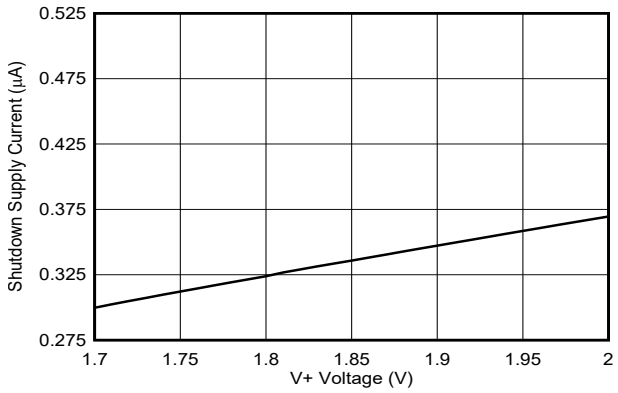


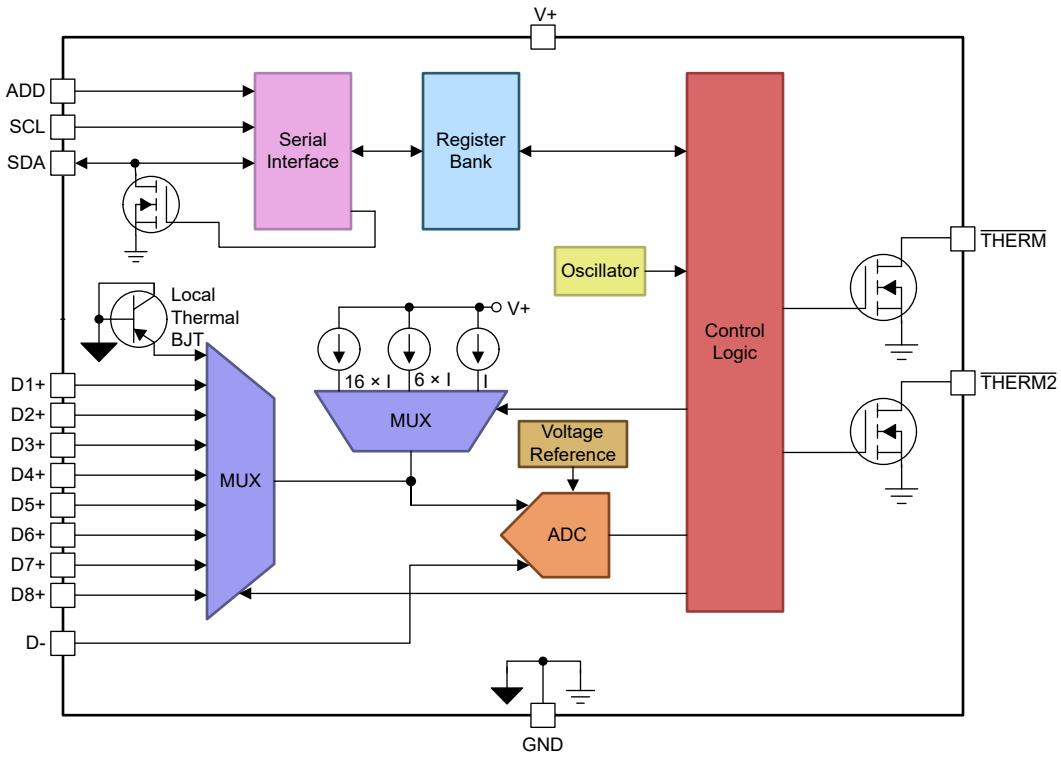
図 6-9. Shutdown Quiescent Current vs Supply Voltage

7 Detailed Description

7.1 Overview

The TMP9R00-SP device is a digital temperature sensor that combines a local temperature measurement channel and eight remote-junction temperature measurement channels in a CFP-16 package. The device has a two-wire-interface that is compatible with I^2C or SMBus interfaces and includes four pin-programmable bus address options. The TMP9R00-SP is specified over a local device temperature range from –55°C to 125°C. The TMP9R00-SP device also contains multiple registers for programming and holding configuration settings, temperature limits, and temperature measurement results. The TMP9R00-SP pinout includes $\overline{\text{THERM}}$ and $\overline{\text{THERM2}}$ outputs that signal overtemperature events based on the settings of temperature limit registers.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Temperature Measurement Data

The local and remote temperature sensors have a resolution of 13 bits (0.0625°C). Temperature data that result from conversions within the default measurement range are represented in binary form, as shown in the *Standard Binary* column of 表 7-1. Negative numbers are represented in two's-complement format. The resolution of the temperature registers extends to 255.9375°C and down to –256°C, but the actual device is limited to ranges as specified in the *Electrical Characteristics* table to meet the accuracy specifications. The TMP9R00-SP device is specified for ambient temperatures ranging from –55°C to 125°C; parameters in the *Absolute Maximum Ratings* table must be observed to prevent damage to the device.

表 7-1. Temperature Data Format (Local and Remote Temperature)

TEMPERATURE (°C)	LOCAL OR REMOTE TEMPERATURE REGISTER VALUE (0.0625°C RESOLUTION)	
	STANDARD BINARY(1)	
	BINARY	HEX
–64	1110 0000 0000 0000	E0 00
–50	1110 0111 0000 0000	E7 00
–25	1111 0011 1000 0000	F3 80
–0.1250	1111 1111 1111 0000	FF F0
–0.0625	1111 1111 1111 1000	FF F8
0	0000 0000 0000 0000	00 00
0.0625	0000 0000 0000 1000	00 08
0.1250	0000 0000 0001 0000	00 10
0.1875	0000 0000 0001 1000	00 18
0.2500	0000 0000 0010 0000	00 20
0.3125	0000 0000 0010 1000	00 28
0.3750	0000 0000 0011 0000	00 30
0.4375	0000 0000 0011 1000	00 38
0.5000	0000 0000 0100 0000	00 40
0.5625	0000 0000 0100 1000	00 48
0.6250	0000 0000 0101 0000	00 50
0.6875	0000 0000 0101 1000	00 58
0.7500	0000 0000 0110 0000	00 60
0.8125	0000 0000 0110 1000	00 68
0.8750	0000 0000 0111 0000	00 70
0.9375	0000 0000 0111 1000	00 78
1	0000 0000 1000 0000	00 80
5	0000 0010 1000 0000	02 80
10	0000 0101 0000 0000	05 00
25	0000 1100 1000 0000	0C 80
50	0001 1001 0000 0000	19 00
75	0010 0101 1000 0000	25 80
100	0011 0010 0000 0000	32 00
125	0011 1110 1000 0000	3E 80
127	0011 1111 1000 0000	3F 80
150	0100 1011 0000 0000	4B 00

(1) Resolution is 0.0625°C per count. Negative numbers are represented in two's-complement format.

Both local and remote temperature data use two bytes for data storage with a two's-complement format for negative numbers. The high byte stores the temperature with 2.0°C resolution. The second or low byte stores the decimal fraction value of the temperature and allows a higher measurement resolution (see 表 7-1). The measurement resolution for both the local and the remote channels is 0.0625 °C.

7.3.2 Series Resistance Cancellation

Series resistance cancellation automatically eliminates the temperature error caused by the resistance of the routing to the remote transistor or by the resistors of the optional external low-pass filter. A total up to 1-kΩ series resistance can be cancelled by the TMP9R00-SP device, which eliminates the need for additional characterization and temperature offset correction.

7.3.3 Differential Input Capacitance

The TMP9R00-SP device tolerates differential input capacitance of up to 1000 pF with minimal change in temperature error. 図 6-5 shows the effect of capacitance on the sensed remote temperature error.

7.3.4 Sensor Fault

The TMP9R00-SP device can sense a fault at the D+ resulting from an incorrect diode connection. The TMP9R00-SP device can also sense an open circuit. Short-circuit conditions return a value of –256°C. The detection circuitry consists of a voltage comparator that trips when the voltage at D+ exceeds (V+) – 0.3 V (typical). The comparator output is continuously checked during a conversion. If a fault is detected, then the RxOP bit in the Remote Channel Status register is set to 1.

When not using the remote sensor with the TMP9R00-SP device, the corresponding D+ and D– inputs must be connected together to prevent meaningless fault warnings.

7.3.5 $\overline{\text{THERM}}$ Functions

図 7-1 shows the operation of the $\overline{\text{THERM}}$ and $\overline{\text{THERM2}}$ interrupt pins.

The hysteresis value is stored in the $\overline{\text{THERM}}$ Hysteresis register and applies to both the $\overline{\text{THERM}}$ and $\overline{\text{THERM2}}$ interrupts.

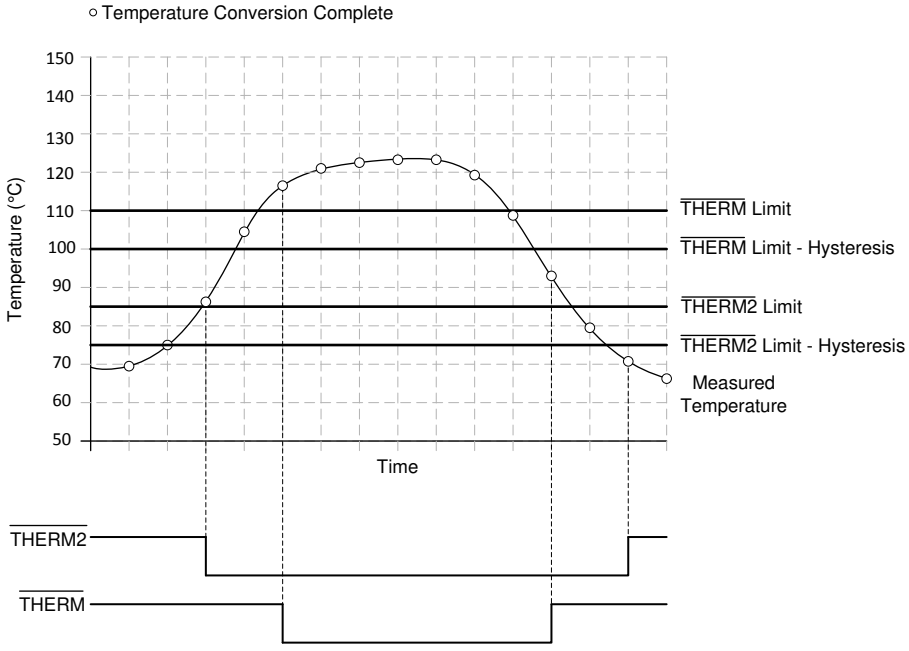


図 7-1. $\overline{\text{THERM}}$ and $\overline{\text{THERM2}}$ Interrupt Operation

7.4 Device Functional Modes

7.4.1 Shutdown Mode (SD)

The TMP9R00-SP shutdown mode enables the user to save maximum power by shutting down all device circuitry other than the serial interface, and reducing current consumption to typically less than 0.3 µA (see 図 6-9). Shutdown mode is enabled when the shutdown bit (SD, bit 5) of the Configuration Register is HIGH; the

device shuts down immediately once the current conversion is complete. When the SD bit is LOW, the device maintains a continuous-conversion state.

7.5 Programming

7.5.1 Serial Interface

The TMP9R00-SP device operates only as a target device on the two-wire bus (I^2C or SMBus). Connections to either bus are made using the open-drain I/O lines, SDA, and SCL. The SDA and SCL pins feature integrated spike suppression filters and Schmitt triggers to minimize the effects of input spikes and bus noise. The TMP9R00-SP device supports the transmission protocol for fast (1 kHz to 400 kHz) and high-speed (1 kHz to 2.56 MHz) modes. All data bytes are transmitted MSB first.

While the TMP9R00-SP device is unpowered bus traffic on SDA and SCL may continue without any adverse effects to the communication or to the TMP9R00-SP device itself. As the TMP9R00-SP device is powering up, the device does not load the bus, and as a result the bus traffic may continue undisturbed.

7.5.1.1 Bus Overview

The TMP9R00-SP device is compatible with the I^2C or SMBus interface. In I^2C or SMBus protocol, the device that initiates the transfer is called a *controller*, and the devices controlled by the controller are *targets*. The bus must be controlled by a controller device that generates the serial clock (SCL), controls the bus access, and generates the start and stop conditions.

To address a specific device, a start condition is initiated. A start condition is indicated by pulling the data line (SDA) from a high-to-low logic level when SCL is high. All target on the bus shift in the target address byte, with the last bit indicating whether a read or write operation is intended. During the ninth clock pulse, the addressed target responds to the controller by generating an *acknowledge* (ACK) bit and pulling SDA low.

Data transfer is then initiated and sent over eight clock pulses followed by an acknowledge bit (ACK). During data transfer, SDA must remain stable when SCL is high. A change in SDA when SCL is high is interpreted as a control signal. The TMP9R00-SP device has a word register structure (16-bit wide), with data writes always requiring two bytes. Data transfer occurs during the ACK at the end of the second byte.

After all data are transferred, the controller generates a stop condition. A stop condition is indicated by pulling SDA from low to high when SCL is high.

7.5.1.2 Bus Definitions

The TMP9R00-SP device has a two-wire interface that is compatible with the I²C or SMBus interface. 図 7-2 through 図 7-7 illustrate the timing for various operations on the TMP9R00-SP device. The bus definitions are as follows:

Bus Idle: Both SDA and SCL lines remain high.

Start Data Transfer: A change in the state of the SDA line (from high to low) when the SCL line is high defines a start condition. Each data transfer initiates with a start condition.

Stop Data Transfer: A change in the state of the SDA line (from low to high) when the SCL line is high defines a stop condition. Each data transfer terminates with a repeated start or stop condition.

Data Transfer: The number of data bytes transferred between a start and stop condition is not limited and is determined by the controller device. The target acknowledges the data transfer.

Acknowledge: Each receiving device, when addressed, is obliged to generate an acknowledge bit. A device that acknowledges must pull down the SDA line during the acknowledge clock pulse in such a way that the SDA line is stable low during the high period of the acknowledge clock pulse. Take setup and hold times into account. On a controller receive, data transfer termination can be signaled by the controller generating a not-acknowledge on the last byte that is transmitted by the target.

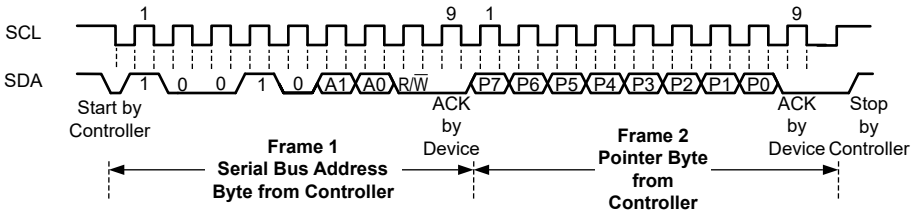


図 7-2. Two-Wire Timing Diagram for Write Pointer Byte

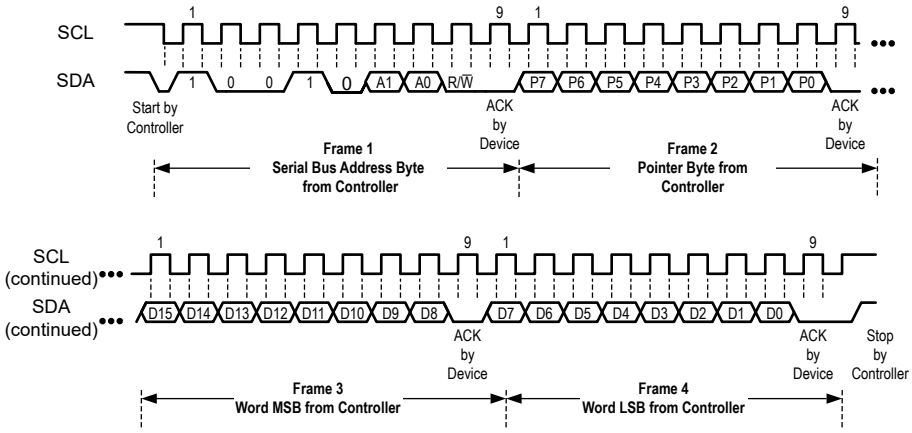
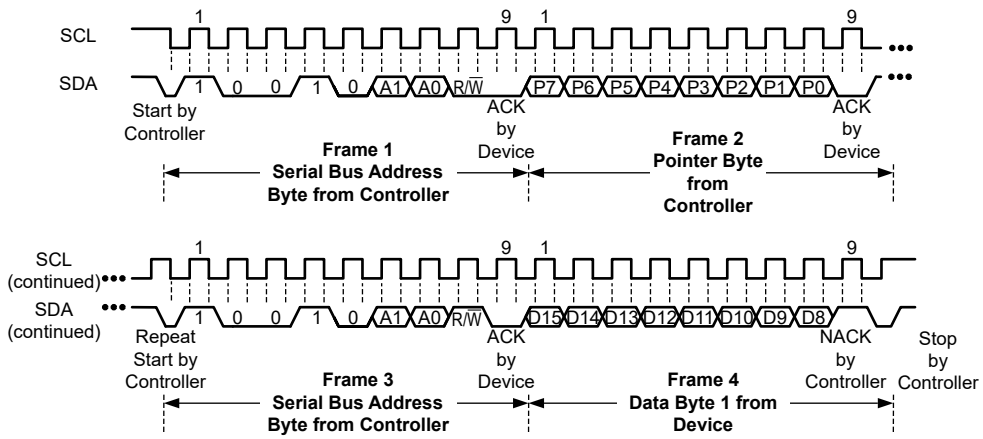


図 7-3. Two-Wire Timing Diagram for Write Pointer Byte and Value Word



A. The controller must leave SDA high to terminate a single-byte read operation.

図 7-4. Two-Wire Timing Diagram for Pointer Set Followed by a Repeat Start and Single-Byte Read Format

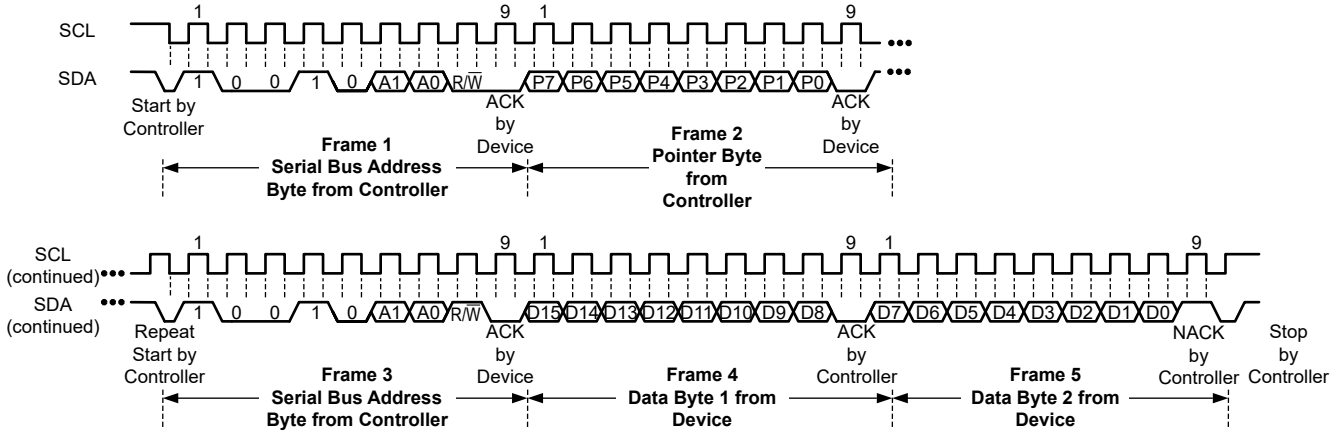


図 7-5. Two-Wire Timing Diagram for Pointer Byte Set Followed by a Repeat Start and Word (Two-Byte) Read

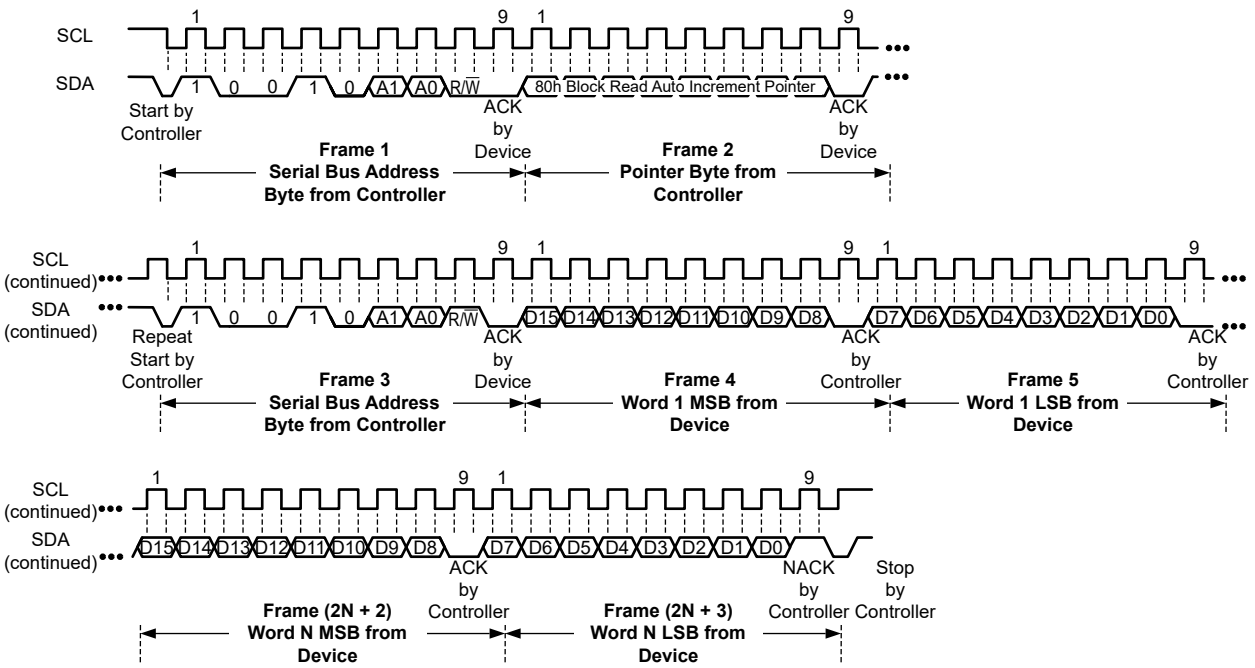


図 7-6. Two-Wire Timing Diagram for Pointer Byte Set Followed by a Repeat Start and Multiple-Word (N-Word) Read

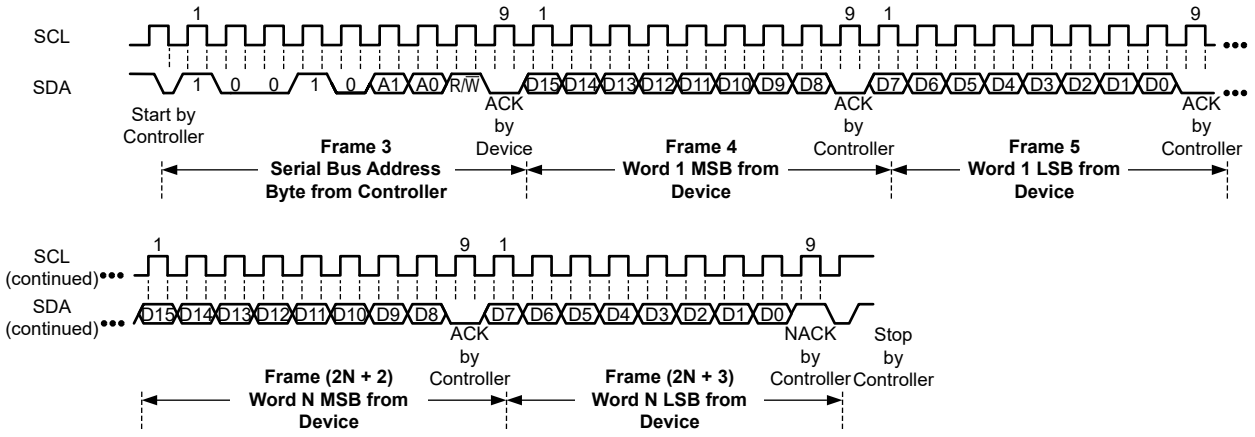


図 7-7. Two-Wire Timing Diagram for Multiple-Word (N-Word) Read Without a Pointer Byte Set

7.5.1.3 Serial Bus Address

To communicate with the TMP9R00-SP device, the controller must first address target devices using a target address byte. The target address byte consists of seven address bits and a direction bit indicating the intent of executing a read or write operation. The TMP9R00-SP device allows up to four devices to be addressed on a single bus. The assigned device address depends on the ADD pin connection (see 表 7-2).

表 7-2. TMP9R00-SP Target Address Options

ADD PIN CONNECTION	TARGET ADDRESS	
	BINARY	HEX
GND	1001000	48
V+	1001001	49
SDA	1001010	4A
SCL	1001011	4B

7.5.1.4 Read and Write Operations

Accessing a particular register on the TMP9R00-SP device is accomplished by writing the appropriate value to the pointer register. The value for the pointer register is the first byte transferred after the target address byte with the R/ $\overline{W}$ bit low. Every write operation to the TMP9R00-SP device requires a value for the pointer register (see 図 7-3).

The TMP9R00-SP registers can be accessed with block or single register reads. Block reads are only supported for pointer values 80h to 88h. Registers at 80h through 88h mirror the Remote and Local Temperature registers (00h to 08h). Pointer values 00h to 08h are for single register reads.

7.5.1.4.1 Single Register Reads

When reading from the TMP9R00-SP device, the last value stored in the pointer register by a write operation is used to determine which register is read by a read operation. To change which register is read for a read operation, a new value must be written to the pointer register. This transaction is accomplished by issuing a target address byte with the R/ $\overline{W}$ bit low, followed by the pointer register byte; no additional data are required. The controller can then generate a start condition and send the target address byte with the R/ $\overline{W}$ bit high to initiate the read command. See 図 7-4 through 図 7-6 for details of this sequence.

If repeated reads from the same register are desired, continually sending the pointer register bytes is not necessary because the TMP9R00-SP device retains the pointer register value until the value is changed by the next write operation. The register bytes are sent by the MSB first, followed by the LSB. If only one byte is read (MSB), a consecutive read of TMP9R00-SP device results in the MSB being transmitted first. The LSB can only be accessed through two-byte reads.

The controller terminates a read operation by issuing a *not-acknowledge* (NACK) command at the end of the last byte to be read or transmitting a stop condition. For a single-byte operation, the controller must leave the SDA line high during the acknowledge time of the first byte that is read from the target

The TMP9R00-SP register structure has a word (two-byte) length, so every write transaction must have an even number of bytes (MSB and LSB) following the pointer register value (see 図 7-3). Data transfers occur during the ACK at the end of the second byte or LSB. If the transaction does not finish, signaled by the ACK at the end of the second byte, then the data is ignored and not loaded into the TMP9R00-SP register. Read transactions do not have the same restrictions and may be terminated at the end of the last MSB.

7.5.1.4.2 Block Register Reads

The TMP9R00-SP supports block mode reads at address 80h through 88h for temperature results alone. Setting the pointer register to 80h signals to the TMP9R00-SP device that a block of more than two bytes must be transmitted before a stop is issued. In this mode, the TMP9R00-SP device auto increments the internal pointer. After the 18 bytes of temperature data are transmitted, the internal pointer resets to 80h. If the transmission is terminated before register 88h is read, the pointer increments so a consecutive read (without a pointer set) can access the next register.

7.5.1.5 Timeout Function

The TMP9R00-SP device resets the serial interface if either SCL or SDA are held low for 17.5 ms (typical) between a start and stop condition. If the TMP9R00-SP device is holding the bus low, the device releases the bus and waits for a start condition. To avoid activating the timeout function, maintain a communication speed of at least 1 kHz for the SCL operating frequency.

7.5.1.6 High-Speed Mode

For the two-wire bus to operate at frequencies above 1 MHz, the controller device must issue a high-speed mode (HS-mode) controller code (0000 1xxx) as the first byte after a start condition to switch the bus to high-speed operation. The TMP9R00-SP device does not acknowledge the controller code byte, but switches the input filters on SDA and SCL and the output filter on SDA to operate in HS-mode, allowing transfers up to 2.56 MHz. After the HS-mode controller code is issued, the controller transmits a two-wire target address to initiate a data transfer operation. The bus continues to operate in HS-mode until a stop condition occurs on the bus. Upon receiving the stop condition, the TMP9R00-SP device switches the input and output filters back to fast mode.

7.5.2 TMP9R00-SP Register Reset

The TMP9R00-SP registers can be software reset by setting bit 15 of the Software Reset register (20h) to 1. This software reset restores the power-on-reset state to all TMP9R00-SP registers and aborts any conversion in progress.

7.5.3 Lock Register

All of the configuration and limit registers may be locked for writes (making the registers write-protected), which decreases the chance of software runaway from issuing false changes to these registers. The *Lock* column in 表 7-3 identifies which registers may be locked. Lock mode does not effect read operations. To activate the lock mode, Lock Register C4h must be set to 0x5CA6. The lock only remains active while the TMP9R00-SP device is powered up. Because the TMP9R00-SP device does not contain nonvolatile memory, the settings of the configuration and limit registers are lost once a power cycle occurs regardless if the registers are locked or unlocked.

In lock mode, the TMP9R00-SP device ignores a write operation to configuration and limit registers except for Lock Register C4h. The TMP9R00-SP device does not acknowledge the data bytes during a write operation to a locked register. To unlock the TMP9R00-SP registers, write 0xEB19 to register C4h. The TMP9R00-SP device powers up in locked mode, so the registers must be unlocked before the registers accept writes of new data.

7.6 Register Maps

表 7-3. TMP9R00-SP Register Map

PTR	POR	LOCK	TMP9R00-SP FUNCTIONAL REGISTER - BIT DESCRIPTION																REGISTER DESCRIPTION
(HEX)	(HEX)	(Y/N)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
00	0000	N/A	LT12	LT11	LT10	LT9	LT8	LT7	LT6	LT5	LT4	LT3	LT2	LT1	LT0	0[1]	0	0	Local Temperature
01	0000	N/A	RT12	RT11	RT10	RT9	RT8	RT7	RT6	RT5	RT4	RT3	RT2	RT1	RT0	0	0	0	Remote Temperature 1
02	0000	N/A	RT12	RT11	RT10	RT9	RT8	RT7	RT6	RT5	RT4	RT3	RT2	RT1	RT0	0	0	0	Remote Temperature 2
03	0000	N/A	RT12	RT11	RT10	RT9	RT8	RT7	RT6	RT5	RT4	RT3	RT2	RT1	RT0	0	0	0	Remote Temperature 3
04	0000	N/A	RT12	RT11	RT10	RT9	RT8	RT7	RT6	RT5	RT4	RT3	RT2	RT1	RT0	0	0	0	Remote Temperature 4
05	0000	N/A	RT12	RT11	RT10	RT9	RT8	RT7	RT6	RT5	RT4	RT3	RT2	RT1	RT0	0	0	0	Remote Temperature 5
06	0000	N/A	RT12	RT11	RT10	RT9	RT8	RT7	RT6	RT5	RT4	RT3	RT2	RT1	RT0	0	0	0	Remote Temperature 6
07	0000	N/A	RT12	RT11	RT10	RT9	RT8	RT7	RT6	RT5	RT4	RT3	RT2	RT1	RT0	0	0	0	Remote Temperature 7
08	0000	N/A	RT12	RT11	RT10	RT9	RT8	RT7	RT6	RT5	RT4	RT3	RT2	RT1	RT0	0	0	0	Remote Temperature 8
20	0000	N/A	RST	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	Software Reset Register
21	N/A	N/A	R8TH	R7TH	R6TH	R5TH	R4TH	R3TH	R2TH	R1TH	LTH	0	0	0	0	0	0	0	$\overline{\text{THERM}}$ Status
22	N/A	N/A	R8TH2	R7TH2	R6TH2	R5TH2	R4TH2	R3TH2	R2TH2	R1TH2	LTH2	0	0	0	0	0	0	0	$\overline{\text{THERM2}}$ Status
23	N/A	N/A	R8OPN	R7OPN	R6OPN	R5OPN	R4OPN	R3OPN	R2OPN	R1OPN	0	0	0	0	0	0	0	0	Remote Channel OPEN Status
30	FF9C	Y	REN8	REN7	REN6	REN5	REN4	REN3	REN2	REN1	LEN	OS	SD	CR2	CR1	CR0	BUSY	0	Configuration Register (Enables, OneShot, ShutDown, ConvRate, BUSY)
38	0500	Y	0	HYS11	HYS10	HYS9	HYS8	HYS7	HYS6	HYS5	HYS4	0	0	0	0	0	0	0	$\overline{\text{THERM}}$ Hysteresis
39	7FC0	Y	LTH1_12	LTH1_11	LTH1_10	LTH1_09	LTH1_08	LTH1_07	LTH1_06	LTH1_05	LTH1_04	LTH1_03	0	0	0	0	0	0	Local Temperature $\overline{\text{THERM}}$ Limit
3A	7FC0	Y	LTH2_12	LTH2_11	LTH2_10	LTH2_09	LTH2_08	LTH2_07	LTH2_06	LTH2_05	LTH2_04	LTH2_03	0	0	0	0	0	0	Local Temperature $\overline{\text{THERM2}}$ Limit
40	0000	Y	ROS12	ROS12[2]	ROS10	ROS9	ROS8	ROS7	ROS6	ROS5	ROS4	ROS3	ROS2	ROS1	ROS0	0	0	0	Remote Temperature 1 Offset
41	0000	Y	RNC7	RNC6	RNC5	RNC4	RNC3	RNC2	RNC1	RNC0	0	0	0	0	0	0	0	0	Remote Temperature 1 η-Factor Correction
42	7FC0	Y	RTH1_12	RTH1_11	RTH1_10	RTH1_09	RTH1_08	RTH1_07	RTH1_06	RTH1_05	RTH1_04	RTH1_03	0	0	0	0	0	0	Remote Temperature 1 $\overline{\text{THERM}}$ Limit
43	7FC0	Y	RTH2_12	RTH2_11	RTH2_10	RTH2_09	RTH2_08	RTH2_07	RTH2_06	RTH2_05	RTH2_04	RTH2_03	0	0	0	0	0	0	Remote Temperature 1 $\overline{\text{THERM2}}$ Limit
48	0000	Y	ROS12	ROS12	ROS10	ROS9	ROS8	ROS7	ROS6	ROS5	ROS4	ROS3	ROS2	ROS1	ROS0	0	0	0	Remote Temperature 2 Offset
49	0000	Y	RNC7	RNC6	RNC5	RNC4	RNC3	RNC2	RNC1	RNC0	0	0	0	0	0	0	0	0	Remote Temperature 2 η-Factor Correction
4A	7FC0	Y	RTH1_12	RTH1_11	RTH1_10	RTH1_09	RTH1_08	RTH1_07	RTH1_06	RTH1_05	RTH1_04	RTH1_03	0	0	0	0	0	0	Remote Temperature 2 $\overline{\text{THERM}}$ Limit
4B	7FC0	Y	RTH2_12	RTH2_11	RTH2_10	RTH2_09	RTH2_08	RTH2_07	RTH2_06	RTH2_05	RTH2_04	RTH2_03	0	0	0	0	0	0	Remote Temperature 2 $\overline{\text{THERM2}}$ Limit
50	0000	Y	ROS12	ROS12	ROS10	ROS9	ROS8	ROS7	ROS6	ROS5	ROS4	ROS3	ROS2	ROS1	ROS0	0	0	0	Remote Temperature 3 Offset
51	0000	Y	RNC7	RNC6	RNC5	RNC4	RNC3	RNC2	RNC1	RNC0	0	0	0	0	0	0	0	0	Remote Temperature 3 η-Factor Correction
52	7FC0	Y	RTH1_12	RTH1_11	RTH1_10	RTH1_09	RTH1_08	RTH1_07	RTH1_06	RTH1_05	RTH1_04	RTH1_03	0	0	0	0	0	0	Remote Temperature 3 $\overline{\text{THERM}}$ Limit
53	7FC0	Y	RTH2_12	RTH2_11	RTH2_10	RTH2_09	RTH2_08	RTH2_07	RTH2_06	RTH2_05	RTH2_04	RTH2_03	0	0	0	0	0	0	Remote Temperature 3 $\overline{\text{THERM2}}$ limit
58	0000	Y	ROS12	ROS12	ROS10	ROS9	ROS8	ROS7	ROS6	ROS5	ROS4	ROS3	ROS2	ROS1	ROS0	0	0	0	Remote temperature 4 Offset
59	0000	Y	RNC7	RNC6	RNC5	RNC4	RNC3	RNC2	RNC1	RNC0	0	0	0	0	0	0	0	0	Remote Temperature 4 η-Factor Correction
5A	7FC0	Y	RTH1_12	RTH1_11	RTH1_10	RTH1_09	RTH1_08	RTH1_07	RTH1_06	RTH1_05	RTH1_04	RTH1_03	0	0	0	0	0	0	Remote Temperature 4 $\overline{\text{THERM}}$ Limit
5B	7FC0	Y	RTH2_12	RTH2_11	RTH2_10	RTH2_09	RTH2_08	RTH2_07	RTH2_06	RTH2_05	RTH2_04	RTH2_03	0	0	0	0	0	0	Remote Temperature 4 $\overline{\text{THERM2}}$ Limit

表 7-3. TMP9R00-SP Register Map (continued)

PTR	POR	LOCK	TMP9R00-SP FUNCTIONAL REGISTER - BIT DESCRIPTION																REGISTER DESCRIPTION
(HEX)	(HEX)	(Y/N)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
60	0000	Y	ROS12	ROS12	ROS10	ROS9	ROS8	ROS7	ROS6	ROS5	ROS4	ROS3	ROS2	ROS1	ROS0	0	0	0	Remote Temperature 5 Offset
61	0000	Y	RNC7	RNC6	RNC5	RNC4	RNC3	RNC2	RNC1	RNC0	0	0	0	0	0	0	0	0	Remote Temperature 5 η-Factor Correction
62	7FC0	Y	RTH1_12	RTH1_11	RTH1_10	RTH1_09	RTH1_08	RTH1_07	RTH1_06	RTH1_05	RTH1_04	RTH1_03	0	0	0	0	0	0	Remote Temperature 5 $\overline{\text{THERM}}$ Limit
63	7FC0	Y	RTH2_12	RTH2_11	RTH2_10	RTH2_09	RTH2_08	RTH2_07	RTH2_06	RTH2_05	RTH2_04	RTH2_03	0	0	0	0	0	0	Remote Temperature 5 $\overline{\text{THERM2}}$ Limit
68	0000	Y	ROS12	ROS12	ROS10	ROS9	ROS8	ROS7	ROS6	ROS5	ROS4	ROS3	ROS2	ROS1	ROS0	0	0	0	Remote Temperature 6 Offset
69	0000	Y	RNC7	RNC6	RNC5	RNC4	RNC3	RNC2	RNC1	RNC0	0	0	0	0	0	0	0	0	Remote Temperature 6 η-Factor Correction
6A	7FC0	Y	RTH1_12	RTH1_11	RTH1_10	RTH1_09	RTH1_08	RTH1_07	RTH1_06	RTH1_05	RTH1_04	RTH1_03	0	0	0	0	0	0	Remote Temperature 6 $\overline{\text{THERM}}$ Limit
6B	7FC0	Y	RTH2_12	RTH2_11	RTH2_10	RTH2_09	RTH2_08	RTH2_07	RTH2_06	RTH2_05	RTH2_04	RTH2_03	0	0	0	0	0	0	Remote Temperature 6 $\overline{\text{THERM2}}$ Limit
70	0000	Y	ROS12	ROS12	ROS10	ROS9	ROS8	ROS7	ROS6	ROS5	ROS4	ROS3	ROS2	ROS1	ROS0	0	0	0	Remote Temperature 7 Offset
71	0000	Y	RNC7	RNC6	RNC5	RNC4	RNC3	RNC2	RNC1	RNC0	0	0	0	0	0	0	0	0	Remote Temperature 7 η-Factor Correction
72	7FC0	Y	RTH1_12	RTH1_11	RTH1_10	RTH1_09	RTH1_08	RTH1_07	RTH1_06	RTH1_05	RTH1_04	RTH1_03	0	0	0	0	0	0	Remote Temperature 7 $\overline{\text{THERM}}$ Limit
73	7FC0	Y	RTH2_12	RTH2_11	RTH2_10	RTH2_09	RTH2_08	RTH2_07	RTH2_06	RTH2_05	RTH2_04	RTH2_03	0	0	0	0	0	0	Remote Temperature 7 $\overline{\text{THERM2}}$ Limit
78	0000	Y	ROS12	ROS12	ROS10	ROS9	ROS8	ROS7	ROS6	ROS5	ROS4	ROS3	ROS2	ROS1	ROS0	0	0	0	Remote Temperature 8 Offset
79	0000	Y	RNC7	RNC6	RNC5	RNC4	RNC3	RNC2	RNC1	RNC0	0	0	0	0	0	0	0	0	Remote Temperature 8 η-Factor Correction
7A	7FC0	Y	RTH1_12	RTH1_11	RTH1_10	RTH1_09	RTH1_08	RTH1_07	RTH1_06	RTH1_05	RTH1_04	RTH1_03	0	0	0	0	0	0	Remote Temperature 8 $\overline{\text{THERM}}$ Limit
7B	7FC0	Y	RTH2_12	RTH2_11	RTH2_10	RTH2_09	RTH2_08	RTH2_07	RTH2_06	RTH2_05	RTH2_04	RTH2_03	0	0	0	0	0	0	Remote Temperature 8 $\overline{\text{THERM2}}$ Limit
80	0000	N/A	LT12	LT11	LT10	LT9	LT8	LT7	LT6	LT5	LT4	LT3	LT2	LT1	LT0	0	0	0	Local Temperature (Block Read Range - Auto Increment Pointer Register)
81	0000	N/A	RT12	RT11	RT10	RT9	RT8	RT7	RT6	RT5	RT4	RT3	RT2	RT1	RT0	0	0	0	Remote Temperature 1 (Block Read Range - Auto Increment Pointer Register)
82	0000	N/A	RT12	RT11	RT10	RT9	RT8	RT7	RT6	RT5	RT4	RT3	RT2	RT1	RT0	0	0	0	Remote Temperature 2 (Block Read Range - Auto Increment Pointer Register)
83	0000	N/A	RT12	RT11	RT10	RT9	RT8	RT7	RT6	RT5	RT4	RT3	RT2	RT1	RT0	0	0	0	Remote Temperature 3 (Block Read Range - Auto Increment Pointer Register)
84	0000	N/A	RT12	RT11	RT10	RT9	RT8	RT7	RT6	RT5	RT4	RT3	RT2	RT1	RT0	0	0	0	Remote Temperature 4 (Block Read Range - Auto Increment Pointer Register)
85	0000	N/A	RT12	RT11	RT10	RT9	RT8	RT7	RT6	RT5	RT4	RT3	RT2	RT1	RT0	0	0	0	Remote Temperature 5 (Block Read Range - Auto Increment Pointer Register)
86	0000	N/A	RT12	RT11	RT10	RT9	RT8	RT7	RT6	RT5	RT4	RT3	RT2	RT1	RT0	0	0	0	Remote Temperature 6 (Block Read Range - Auto Increment Pointer Register)
87	0000	N/A	RT12	RT11	RT10	RT9	RT8	RT7	RT6	RT5	RT4	RT3	RT2	RT1	RT0	0	0	0	Remote Temperature 7 (Block Read Range - Auto Increment Pointer Register)
88	0000	N/A	RT12	RT11	RT10	RT9	RT8	RT7	RT6	RT5	RT4	RT3	RT2	RT1	RT0	0	0	0	Remote Temperature 8 (Block Read Range - Auto Increment Pointer Register)

表 7-3. TMP9R00-SP Register Map (continued)

PTR	POR	LOCK	TMP9R00-SP FUNCTIONAL REGISTER - BIT DESCRIPTION																REGISTER DESCRIPTION
(HEX)	(HEX)	(Y/N)	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0	
C4	8000	N/A	Write 0x5CA6 to lock registers and 0xEB19 to unlock registers Read back: locked 0x8000; unlocked 0x0000																Lock Register. This locks the registers after initialization.
FE	5449	N/A	0	1	0	1	0	1	0	0	0	1	0	0	1	0	0	1	Manufacturers Identification Register
FF	0468	N/A	0	0	0	0	0	1	0	0	0	1	1	0	1	0	0	0	Device Identification/Revision Register

1. Register bits highlighted in purple are reserved for future use and always report 0; writes to these bits are ignored.
2. Register bits highlighted in green show sign extended values.

7.6.1 Register Information

The TMP9R00-SP device contains multiple registers for holding configuration information, temperature measurement results, and status information. These registers are described in 表 7-3.

7.6.1.1 Pointer Register

図 7-8 shows the internal register structure of the TMP9R00-SP device. The 8-bit pointer register addresses a given data register. The pointer register identifies which of the data registers must respond to a read or write command on the two-wire bus. This register is set with every write command. A write command must be issued to set the proper value in the pointer register before executing a read command. 表 7-3 describes the pointer register and the internal structure of the TMP9R00-SP registers. The power-on-reset (POR) value of the pointer register is 00h (0000 0000b). 表 7-3 lists a summary of the pointer values for the different registers. Writing data to unassigned pointer values are ignored and does not **affect** the operation of the device. Reading an unassigned register returns undefined data and is ACKed.

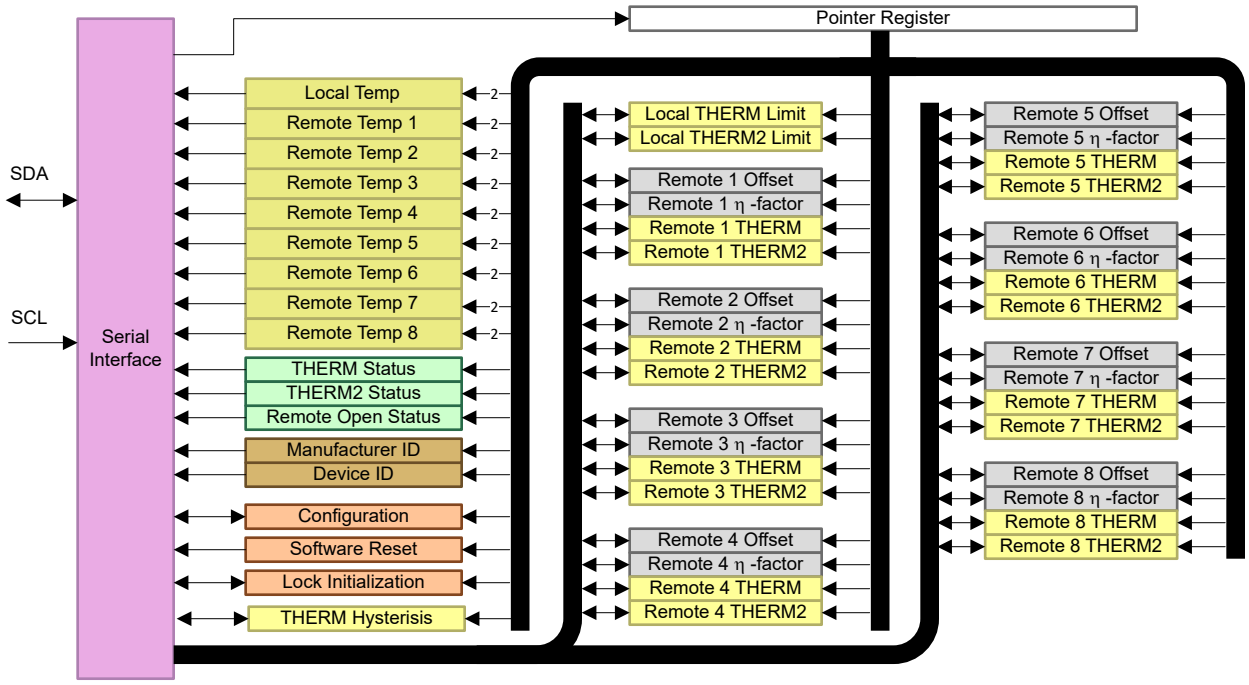


図 7-8. TMP9R00-SP Internal Register Structure

7.6.1.2 Local and Remote Temperature Value Registers

The TMP9R00-SP device has multiple 16-bit registers that hold 13-bit temperature measurement results. The 13 bits of the local temperature sensor result are stored in register 00h. The 13 bits of the eight remote temperature sensor results are stored in registers 01h through 08h. The four assigned LSBs of both the local (LT3:LT0) and remote (RT3:RT0) sensors indicate the temperature value after the decimal point (for example, if the temperature result is 10.0625°C, then the high byte is 0000 0101 and the low byte is 0000 1000). These registers are read-only and are updated by the ADC each time a temperature measurement is complete. Asynchronous reads are supported, so a read operation can occur at any time and results in valid conversion results being transmitted once the first conversion is complete after power up for the channel being accessed. If after power up a read is initiated before a conversion is complete, the read operation results in all zeros (0x0000).

7.6.1.3 Software Reset Register

The Software Reset Register allows the user to reset the TMP9R00-SP registers through software by setting the reset bit (RST, bit 15) to 1. The power-on-reset value for this register is 0x0000. Resets are ignored when the device is in lock mode, so writing a 1 to the RST bit does not reset any registers.

表 7-4. Software Reset Register Format

STATUS REGISTER (READ = 20h, WRITE = 20h, POR = 0x0000)		
BIT NUMBER	**BIT NAME**	**FUNCTION**
15	RST	1 software reset device; writing a value of 0 is ignored
14-0	0	Reserved for future use; always reports 0

7.6.1.4 THERM Status Register

The $\overline{\text{THERM}}$ Status register reports the state of the $\overline{\text{THERM}}$ limit comparators for local and eight remote temperatures. 表 7-5 lists the status register bits. The $\overline{\text{THERM}}$ Status register is read-only and is read by accessing pointer address 21h.

表 7-5. $\overline{\text{THERM}}$ Status Register Format

$\overline{\text{THERM}}$ STATUS REGISTER (READ = 21h, WRITE = N/A)		
BIT NUMBER	**BIT NAME**	**FUNCTION**
15	R8TH	1 when Remote 8 exceeds the $\overline{\text{THERM}}$ limit
14	R7TH	1 when Remote 7 exceeds the $\overline{\text{THERM}}$ limit
13	R6TH	1 when Remote 6 exceeds the $\overline{\text{THERM}}$ limit
12	R5TH	1 when Remote 5 exceeds the $\overline{\text{THERM}}$ limit
11	R4TH	1 when Remote 4 exceeds the $\overline{\text{THERM}}$ limit
10	R3TH	1 when Remote 3 exceeds the $\overline{\text{THERM}}$ limit
9	R2TH	1 when Remote 2 exceeds the $\overline{\text{THERM}}$ limit
8	R1TH	1 when Remote 1 exceeds the $\overline{\text{THERM}}$ limit
7	LTH	1 when Local sensor exceeds the $\overline{\text{THERM}}$ limit
6:0	0	Reserved for future use; always reports 0.

The R8TH:R1TH and LTH flags are set when the corresponding temperature exceeds the respective programmed $\overline{\text{THERM}}$ limit (39h, 42h, 4Ah, 52h, 5Ah, 62h, 6Ah, 72h, 7Ah). These flags are reset automatically when the temperature returns below the $\overline{\text{THERM}}$ limit minus the value set in the $\overline{\text{THERM}}$ Hysteresis register (38h). The $\overline{\text{THERM}}$ output goes low in the case of overtemperature on either the local or remote channels, and goes high as soon as the measurements are less than the $\overline{\text{THERM}}$ limit minus the value set in the $\overline{\text{THERM}}$ Hysteresis register. The $\overline{\text{THERM}}$ Hysteresis register (38h) allows hysteresis to be added so that the flag resets and the output goes high when the temperature returns to or goes below the limit value minus the hysteresis value.

7.6.1.5 $\overline{\text{THERM2}}$ Status Register

The $\overline{\text{THERM2}}$ Status register reports the state of the $\overline{\text{THERM2}}$ limit comparators for local and remote 1-8 temperatures. 表 7-6 lists the status register bits. The $\overline{\text{THERM2}}$ Status register is read-only and is read by accessing pointer address 22h.

表 7-6. $\overline{\text{THERM2}}$ Status Register Format

THERM2 STATUS REGISTER (READ = 22h, WRITE = N/A)		
BIT NUMBER	**BIT NAME**	**FUNCTION**
15	R8TH2	1 when Remote 8 exceeds the $\overline{\text{THERM2}}$ limit
14	R7TH2	1 when Remote 7 exceeds the $\overline{\text{THERM2}}$ limit
13	R6TH2	1 when Remote 6 exceeds the $\overline{\text{THERM2}}$ limit
12	R5TH2	1 when Remote 5 exceeds the $\overline{\text{THERM2}}$ limit
11	R4TH2	1 when Remote 4 exceeds the $\overline{\text{THERM2}}$ limit
10	R3TH2	1 when Remote 3 exceeds the $\overline{\text{THERM2}}$ limit
9	R2TH2	1 when Remote 2 exceeds the $\overline{\text{THERM2}}$ limit
8	R1TH2	1 when Remote 1 exceeds the $\overline{\text{THERM2}}$ limit
7	LTH2	1 when Local Sensor exceeds the $\overline{\text{THERM2}}$ limit
6:0	0	Reserved for future use; always reports 0.

The R8TH2:R1TH2 and LTH2 flags are set when the corresponding temperature exceeds the respective programmed $\overline{\text{THERM2}}$ limit (3Ah, 43h, 4Bh, 53h, 5Bh, 63h, 6Bh, 73h, 7Bh). These flags are reset automatically when the temperature returns below the $\overline{\text{THERM2}}$ limit minus the value set in the $\overline{\text{THERM}}$ Hysteresis register (38h). The $\overline{\text{THERM2}}$ output goes low in the case of overtemperature on either the local or remote channels, and goes high as soon as the measurements are less than the $\overline{\text{THERM2}}$ limit minus the value set in the $\overline{\text{THERM}}$ Hysteresis register. The $\overline{\text{THERM}}$ Hysteresis register (38h) allows hysteresis to be added so that the flag resets and the output goes high when the temperature returns to or goes below the limit value minus the hysteresis value.

7.6.1.6 Remote Channel Open Status Register

The Remote Channel Open Status register reports the state of the connection of remote channels one through eight. 表 7-7 lists the status register bits. The Remote Channel Open Status register is read-only and is read by accessing pointer address 23h.

表 7-7. Remote Channel Open Status Register Format

REMOTE CHANNEL OPEN STATUS REGISTER (READ = 23h, WRITE = N/A)		
BIT NUMBER	**BIT NAME**	**FUNCTION**
15	R8OPEN	1 when Remote 8 channel is an open circuit
14	R7OPEN	1 when Remote 7 channel is an open circuit
13	R6OPEN	1 when Remote 6 channel is an open circuit
12	R5OPEN	1 when Remote 5 channel is an open circuit
11	R4OPEN	1 when Remote 4 channel is an open circuit
10	R3OPEN	1 when Remote 3 channel is an open circuit
9	R2OPEN	1 when Remote 2 channel is an open circuit
8	R1OPEN	1 when Remote 1 channel is an open circuit
7:0	0	Reserved for future use; always reports 0.

The R8OPEN:R1OPEN bits indicate an open-circuit condition on remote sensors eight through one, respectively. The setting of these flags does not directly affect the state of the $\overline{\text{THERM}}$ or $\overline{\text{THERM2}}$ output pins. Indirectly, the temperature reading(s) may be erroneous and exceed the respective $\overline{\text{THERM}}$ and $\overline{\text{THERM2}}$ limits, activating the $\overline{\text{THERM}}$ or $\overline{\text{THERM2}}$ output pins.

7.6.1.7 Configuration Register

The Configuration Register sets the conversion rate, starts one-shot conversion of all enabled channels, enables conversion the temperature channels, controls the shutdown mode and reports when a conversion is in process. The Configuration Register is set by writing to pointer address 30h, and is read from pointer address 30h. 表 7-8 summarizes the bits of the Configuration Register.

表 7-8. Configuration Register Bit Descriptions

CONFIGURATION REGISTER (READ = 30h, WRITE = 30h, POR = 0F9Ch)			
BIT NUMBER	**NAME**	**FUNCTION**	**POWER-ON-RESET VALUE**
15:8	REN8:REN1	1 = enable respective remote channel 8 through 1 conversions	1111 1111
7	LEN	1 = enable local channel conversion	1
6	OS	1 = start one-shot conversion on enabled channels	0
5	SD	1 = enables device shutdown	0
4:2	CR2:CR0	Conversion rate control bits; control conversion rates for all enabled channels from 16 seconds to continuous conversion	111
1	BUSY	1 when the ADC is converting (read-only bit ignores writes)	0
0	Reserved	—	0

The Remote Enable eight through one (REN8:REN1, bits 15:8) bits enable conversions on the respective remote channels. The Local Enable (LEN, bit 7) bit enables conversions of the local temperature channel. If all LEN and REN are set to 1 (default), this enables the ADC to convert the local and all remote temperatures. If the LEN is set to 0, the local temperature conversion is skipped. Similarly if a REN is set to 0, that remote temperature conversion channel is skipped. The TMP9R00-SP device steps through each enabled channel in a round-robin fashion in the following order: LOC, REM1, REM2, REM8, LOC, REM1, and so on. All local and remote temperatures are converted by the internal ADC by default after power up. The configuration register LEN and REN bits can be configured to save power by reducing the total ADC conversion time for applications that do not require all of the eight remote and local temperature information. Note writing all zeros to REN8:REN1 and LEN has the same effect as SD = 1 and OS = 0.

The shutdown bit (SD, bit 5) enables or disables the temperature-measurement circuitry. If SD = 0 (default), the TMP9R00-SP device converts continuously at the rate set in the conversion rate register. When SD is set to 1, the TMP9R00-SP device immediately stops the conversion in progress and instantly enters shutdown mode. When SD is set to 0 again, the TMP9R00-SP device resumes continuous conversions starting with the local temperature.

The BUSY bit = 1 if the ADC is making a conversion. This bit is set to 0 if the ADC is not converting.

After the TMP9R00-SP device is in shutdown mode, writing a 1 to the one-shot (OS, bit 6) bit starts a single ADC conversion of all the enabled temperature channels. This write operation starts one conversion and comparison cycle on either the eight remote and one local sensor or any combination of sensors, depending on the LEN and REN values in the Configuration Register (read address 30h). The TMP9R00-SP device returns to shutdown mode when the cycle is complete. 表 7-9 details the interaction of the SD, OS, LEN, and REN bits.

表 7-9. Conversion Modes

WRITE			READ			FUNCTION
REN[8:1], LEN	**OS**	**SD**	**REN[8:1], LEN**	**OS**	**SD**	
All 0	—	—	All 0	0	1	Shutdown
At least 1 enabled	—	0	Written value	0	0	Continuous conversion

表 7-9. Conversion Modes (continued)

WRITE			READ			FUNCTION
REN[8:1], LEN	OS	SD	REN[8:1], LEN	OS	SD	
At least 1 enabled	0	1	Written value	0	1	Shutdown
At least 1 enabled	1	1	Written value	1	1	One-shot conversion

The conversion rate bits control the rate that the conversions occur (CR2:CR0, bits 4:2). The value of CR2:CR0 bits controls the idle time between conversions but not the conversion time itself, which allows the TMP9R00-SP device power dissipation to be balanced with the update rate of the temperature register. 表 7-10 describes the mapping for CR2:CR0 to the conversion rate or temperature register update rate.

表 7-10. Conversion Rate

CR2:CR0	DECIMAL VALUE	FREQUENCY (Hz)	TIME (s)
000	0	0.0625	16
001	1	0.125	8
010	2	0.25	4
011	3	0.5	2
100	4	1	1
101	5	2	0.5
110	6	4	0.25
111	7	Continuous conversion; depends on number of enabled channels; see 表 7-11 (default).	

表 7-11. Continuous Conversion Times

NUMBER OF REMOTE CHANNELS ENABLED	CONVERSION TIME (ms)	
	LOCAL DISABLED	LOCAL ENABLED
0	0	15.5
1	15.8	31.3
2	31.6	47.1
3	47.4	62.9
4	63.2	78.7
5	79	94.5
6	94.8	110.3
7	110.6	126.1
8	126.4	141.9

The remaining bits of the configuration register are reserved and must always be set to 0. The POR value for this register is 0x0F9C.

7.6.1.8 η-Factor Correction Register

The TMP9R00-SP device allows for a different η-factor value to be used for converting remote channel measurements to temperature for each temperature channel. There are eight η-Factor Correction registers assigned: one to each of the remote input channels (addresses 41h, 49h, 51h, 59h, 61h, 69h, 71h and 79h). Each remote channel uses sequential current excitation to extract a differential V_{BE} voltage measurement to determine the temperature of the remote transistor. 式 1 shows this voltage and temperature.

$$V_{BE2} - V_{BE1} = \frac{\eta k T}{q} \ln\left(\frac{I_2}{I_1}\right) \quad (1)$$

The value η in 式 1 is a characteristic of the particular transistor used for the remote channel. The POR value for the TMP9R00-SP device is η = 1.008. The value in the η-Factor Correction register can be used to adjust the effective η-factor, according to 式 2 and 式 3.

$$\eta_{eff} = \left(\frac{1.008 \times 2088}{2088 + N_{ADJUST}} \right) \tag{2}$$

$$N_{ADJUST} = \left(\frac{1.008 \times 2088}{\eta_{eff}} \right) - 2088 \tag{3}$$

The η-factor correction value must be stored in a two's-complement format, which yields an effective data range from –128 to +127. The POR value for each register is 0000h, which does not affect register values unless a different value is written to the register. The resolution of the η-factor register changes linearly as the code changes and has a range from 0.0004292 to 0.0005476, with an average of 0.0004848.

表 7-12. η-Factor Range

N_{ADJUST} ONLY BITS 15 TO 8 IN THE REGISTER ARE SHOWN			η
BINARY	HEX	DECIMAL	
0111 1111	7F	127	0.950205
0000 1010	0A	10	1.003195
0000 1000	08	8	1.004153
0000 0110	06	6	1.005112
0000 0100	04	4	1.006073
0000 0010	02	2	1.007035
0000 0001	01	1	1.007517
0000 0000	00	0	1.008
1111 1111	FF	–1	1.008483
1111 1110	FE	–2	1.008966
1111 1100	FC	–4	1.009935
1111 1010	FA	–6	1.010905
1111 1000	F8	–8	1.011877
1111 0110	F6	–10	1.012851
1000 0000	80	–128	1.073829

7.6.1.9 Remote Temperature Offset Register

The offset registers allow the TMP9R00-SP device to store any system offset compensation value that may result from precision calibration. The value in these registers is added to the remote temperature results upon every conversion. Each of the eight temperature channels have an independent assigned offset register (addresses 40h, 48h, 50h, 58h, 60h, 68h, 70h, and 78h). Combined with the independent η-factor corrections, this function allows for very accurate system calibration over the entire temperature range for each remote channel. The format of these registers is the same as the temperature value registers with a range from +127.9375 to –128. Take care to program this register with sign extension, as values above +127.9375 and below –128 are not supported.

7.6.1.10 $\overline{\text{THERM}}$ Hysteresis Register

The $\overline{\text{THERM}}$ Hysteresis register (address 38h) sets the value of the hysteresis used by the temperature comparison logic. All temperature reading comparisons have a common hysteresis. Hysteresis prevents oscillations from occurring on the $\overline{\text{THERM}}$ and $\overline{\text{THERM2}}$ outputs as the measured temperature approaches the comparator threshold (see *$\overline{\text{THERM}}$ Functions*). The resolution of the $\overline{\text{THERM}}$ Hysteresis register is 1°C and ranges from 0°C to 255°C.

7.6.1.11 Local and Remote $\overline{THERM}$ and $\overline{THERM2}$ Limit Registers

Each of the eight remote and the local temperature channels has associated independent $\overline{THERM}$ and $\overline{THERM2}$ Limit registers. There are nine $\overline{THERM}$ registers (addresses 39h, 42h, 4Ah, 52h, 5Ah, 62h, 6Ah, 72h, and 7Ah) and nine $\overline{THERM2}$ registers (addresses 39h, 43h, 4Bh, 53h, 5Bh, 63h, 6Bh, 73h, and 7Bh), 18 registers in total. The resolution of these registers is 0.5°C and ranges from +255.5°C to –255°C. See *$\overline{THERM}$ Functions* for more information.

Setting a $\overline{THERM}$ limit to 255.5°C disables the $\overline{THERM}$ limit comparison for that particular channel and disables the limit flag from being set in the $\overline{THERM}$ Status register. This prevents the associated channel from activating the $\overline{THERM}$ output. $\overline{THERM2}$ limits, status, and outputs function similarly.

7.6.1.12 Block Read - Auto Increment Pointer

Block reads can be initiated by setting the pointer register to 80h to 87h. The temperature results are mirrored at pointer addresses 80h to 88h; temperature results for all the channels can be read with one read transaction. Setting the pointer register to any address from 80h to 88h signals to the TMP9R00-SP device that a block of more than two bytes must be transmitted before a design stop is issued. In block read mode, the TMP9R00-SP device auto increments the pointer address. After 88h, the pointer resets to 80h. The controller must NACK the last byte read so the TMP9R00-SP device can discontinue driving the bus, which allows the controller to initiate a stop. In this mode, the pointer continuously loops in the address range from 80h to 88h, so the register may be easily read multiple times. Block read does not disrupt the conversion process.

7.6.1.13 Lock Register

Register C4h allows the device configuration and limit registers to lock, as shown by the *Lock* column in 表 7-3. To lock the registers, write 0x5CA6. To unlock the registers, write 0xEB19. When the lock function is enabled, reading the register yields 0x8000; when unlocked, 0x0000 is transmitted.

7.6.1.14 Manufacturer and Device Identification Plus Revision Registers

The TMP9R00-SP device allows the two-wire bus controller to query the device for manufacturer and device identifications (IDs) to enable software identification of the device at the particular two-wire bus address. The manufacturer ID is obtained by reading from pointer address FEh; the device ID is obtained from register FFh. Note that the most significant byte of the Device ID register identifies the TMP9R00-SP device revision level. The TMP9R00-SP device reads 0x5449 for the manufacturer code and 0x0468 for the device ID code for the first release.

8 Application and Implementation

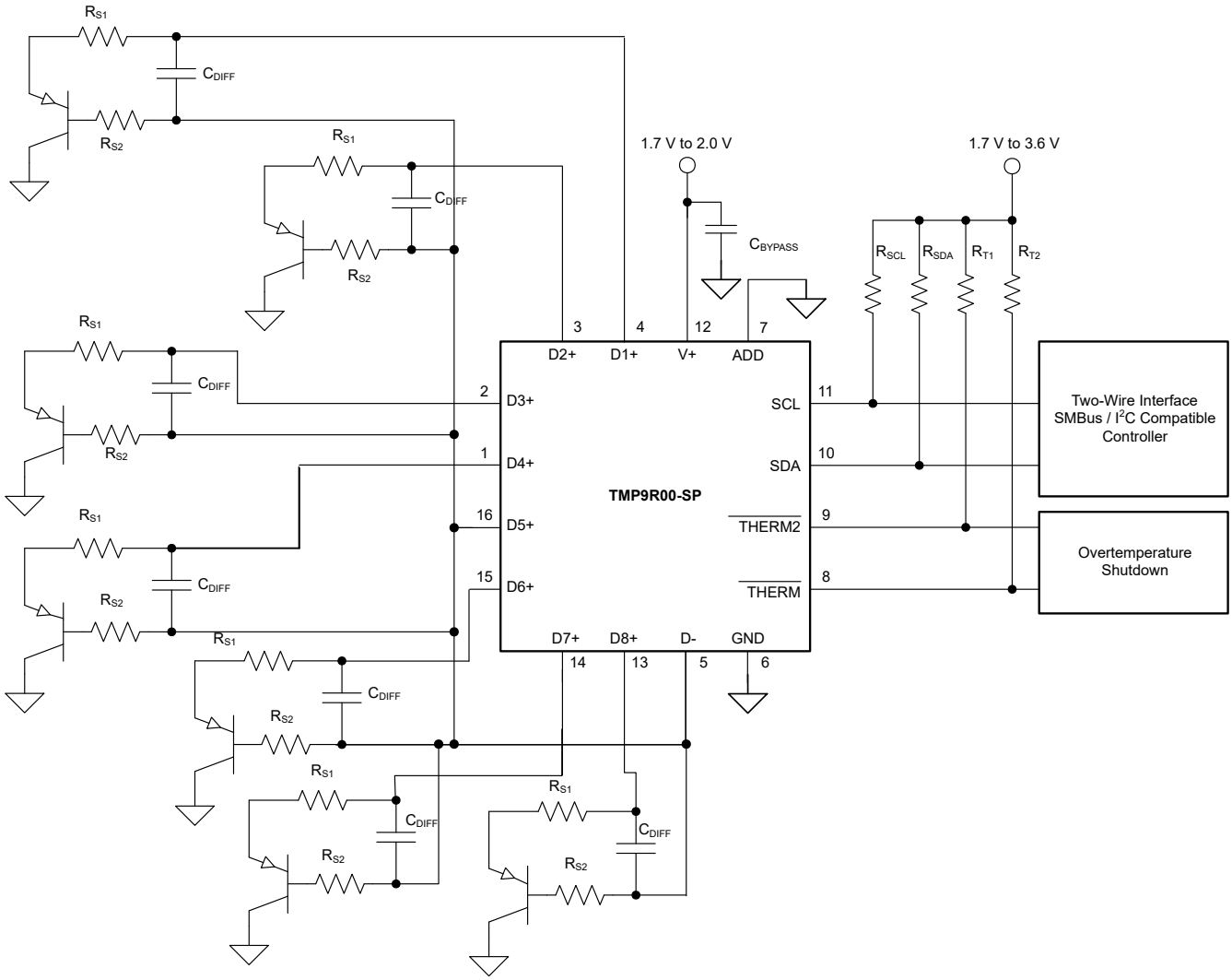
注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

8.1 Application Information

The TMP9R00-SP device requires a transistor connected between the D+ and D– pins for remote temperature measurement. Tie the D+ pin to D– if the remote channel is not used and only the local temperature is measured. The SDA, ALERT, and THERM pins (and SCL, if driven by an open-drain output) require pullup resistors as part of the communication bus. TI recommends a 0.1-µF power-supply decoupling capacitor for local bypassing. 図 8-1 and 図 8-2 illustrate the typical configurations for the TMP9R00-SP device.

8.2 Typical Application



A. The diode-connected configuration provides better settling time. The transistor-connected configuration provides better series resistance cancellation. TI recommends a MMBT3904 or MMBT3906 transistor with an η-factor of 1.008.

B. R_S (optional) is < 1 kΩ in most applications. R_S is the combined series resistance connected externally to the D+, D– pins. R_S selection depends on the application.

C. C_{DIFF} (optional) is < 1000 pF in most applications. C_{DIFF} selection depends on the application; see 図 6-5.

D. Unused diode channels must be tied to D– as shown for D5+.

図 8-1. TMP9R00-SP Basic Connections Using a Discrete Remote Transistors

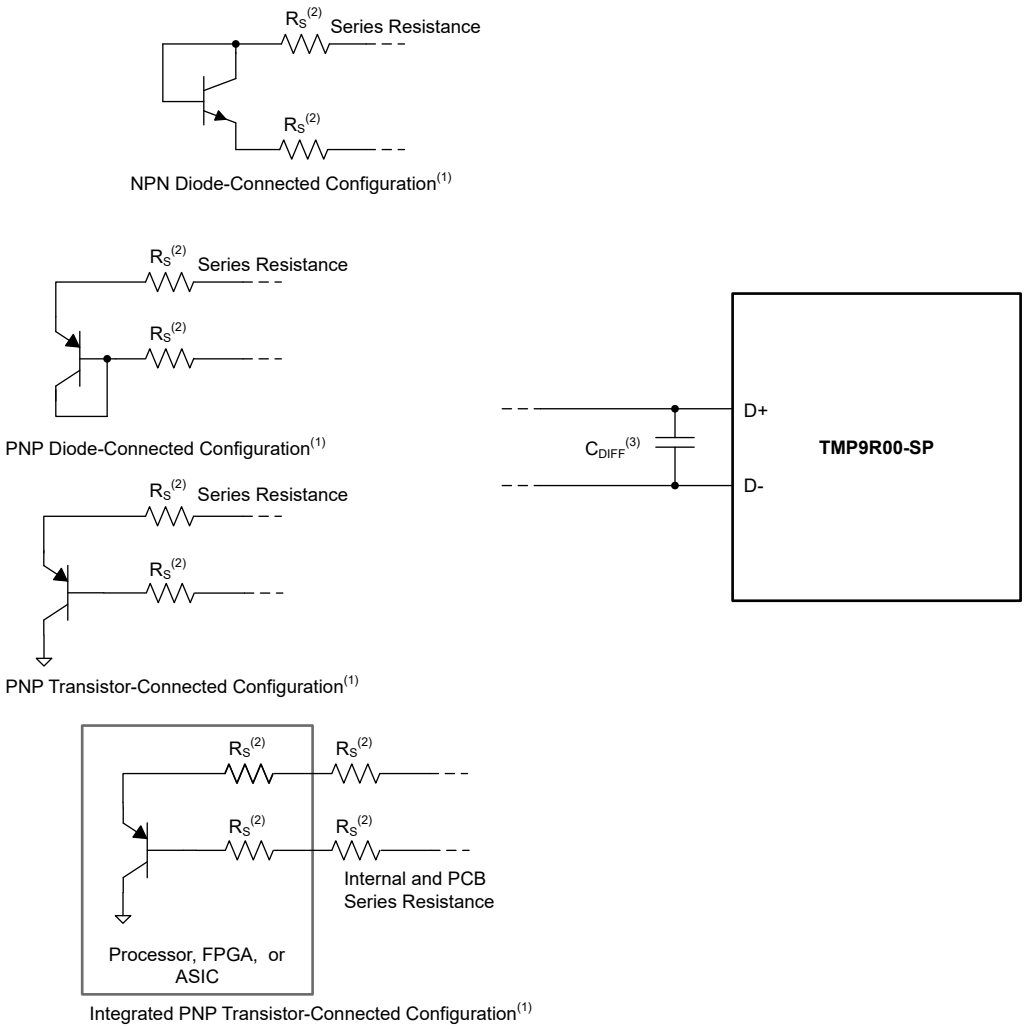


図 8-2. TMP9R00-SP Remote Transistor Configuration Options

8.2.1 Design Requirements

The TMP9R00-SP device is designed to be used with either discrete transistors or substrate transistors built into processor chips, field programmable gate arrays (FPGAs), and application-specific integrated circuits (ASICs). Either NPN or PNP transistors can be used, as long as the base-emitter junction is used as the remote temperature sensor. NPN transistors must be diode-connected, and PNP transistors can either be transistor- or diode-connected. See 図 8-2 for configuration options.

Errors in remote temperature sensor readings are typically the consequence of the ideality factor (η-factor) and current excitation used by the TMP9R00-SP device versus the manufacturer-specified operating current for a given transistor. Some manufacturers specify a high-level and low-level current for the temperature-sensing substrate transistors. The TMP9R00-SP uses 7.5 µA (typical) for I_{LOW} and 120 µA (typical) for I_{HIGH}.

The ideality factor (η-factor) is a measured characteristic of a remote temperature sensor diode as compared to an ideal diode. The TMP9R00-SP allows for different η-factor values. See *η-Factor Correction Register* for more information.

The η-factor for the TMP9R00-SP device is trimmed to 1.008. For transistors that have an ideality factor that does not match the TMP9R00-SP device, 式 4 can be used to calculate the temperature error.

注

For 式 4 to be used correctly, the actual temperature (°C) must be converted to Kelvin (K).

$$T_{ERR} = \left(\frac{\eta - 1.008}{1.008}\right) \times \left(273.15 + T(^{\circ}C)\right) \quad (4)$$

where

- T_{ERR} = error in the TMP9R00-SP device because η ≠ 1.008
- η = ideality factor of the remote temperature sensor
- T(°C) = actual temperature, and

In 式 4, the degree of delta is the same for°C and K.

For η = 1.004 and T(°C) = 100°C:

$$T_{ERR} = \left(\frac{1.004 - 1.008}{1.008}\right) \times \left(273.15 + 100^{\circ}C\right)$$
$$T_{ERR} = -1.48^{\circ}C \quad (5)$$

If a discrete transistor is used as the remote temperature sensor with the TMP9R00-SP device, then select the transistor according to the following criteria for best accuracy:

- Base-emitter voltage is > 0.25 V at 7.5 µA, at the highest-sensed temperature.
- Base-emitter voltage is < 0.95 V at 120 µA, at the lowest-sensed temperature.
- Base resistance is < 100 Ω.
- Tight control of V_{BE} characteristics indicated by small variations in h_{FE} (50 to 150).

Based on these criteria, TI recommends using a MMBT3904 (NPN) or a MMBT3906 (PNP) transistor.

8.2.2 Detailed Design Procedure

The internal power dissipation of the TMP9R00-SP device can cause the temperature to rise above the ambient or PCB temperature. The internal power is negligible because of the small current drawn by the TMP9R00-SP device. 式 6 can be used to calculate the average conversion current for power dissipation and self-heating based on the number of conversions per second and temperature sensor channel enabled. Use the *Electrical Characteristics* table to find typical values required for these calculations. For a 2.0-V supply and a conversion rate of 1 conversion per second, the TMP9R00-SP device dissipates 136 mW (PD_{IQ} = 2.0 V × 68 µA) when both the remote and local channels are enabled.

$$\text{Average Conversion Current} = (\text{Local Conversion Time}) \times (\text{Conversions Per Second}) \times (\text{Local Active IQ}) + (\text{Remote Conversion Time}) \times (\text{Conversions Per Second}) \times (\text{Remote Active } I_Q) \times (\text{Number of Active Channels} + (\text{Standby Mode}) \times [1 - ((\text{Local Conversion Time}) + (\text{Remote Conversion Time}) \times (\text{Number of Active Channels})) \times (\text{Conversions Per Second})] \quad (6)$$

The temperature measurement accuracy of the TMP9R00-SP device depends on the remote and local temperature sensor being at the same temperature as the monitored system point. If the temperature sensor is not in good thermal contact with the part of the monitored system, then there is a delay between the sensor response and the system changing temperature. This delay is usually not a concern for remote temperature-sensing applications that use a substrate transistor (or a small, SOT-23 transistor) placed close to the monitored device.

8.2.3 Application Curve

図 8-3 and 図 8-4 show the typical local and remote temperature error of the TMP9R00-SP device.

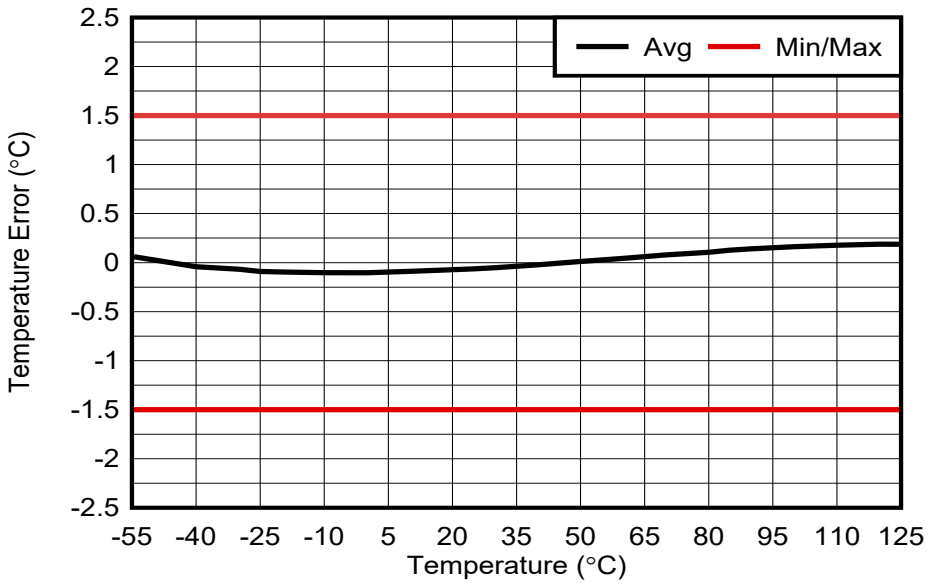


図 8-3. Local Temperature Error vs Ambient Temperature

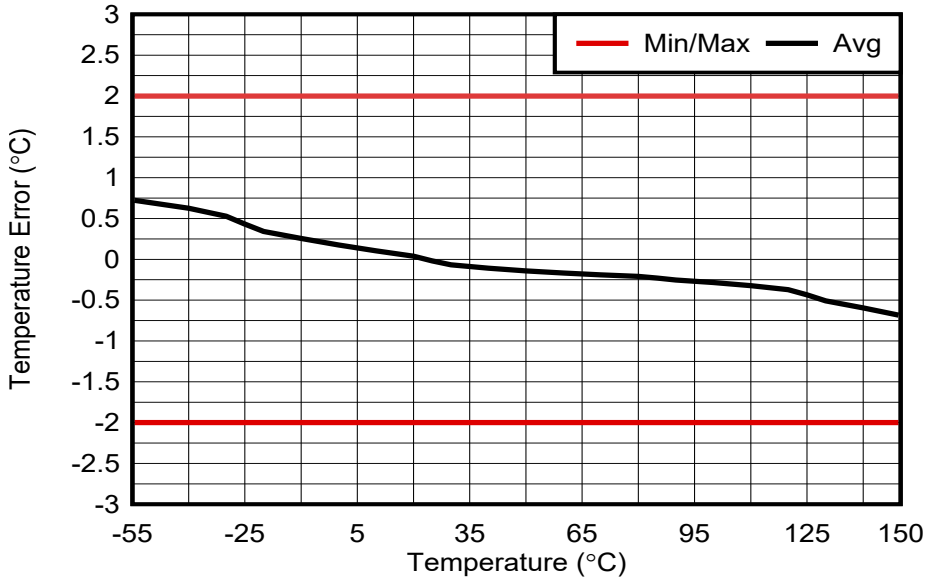


図 8-4. Remote Temperature Error vs Device Junction Temperature

8.3 Power Supply Recommendations

The TMP9R00-SP device operates with a power-supply range from 1.7 V to 2.0 V. The device is optimized for operation at a 1.8-V supply, but can measure temperature accurately in the full supply range.

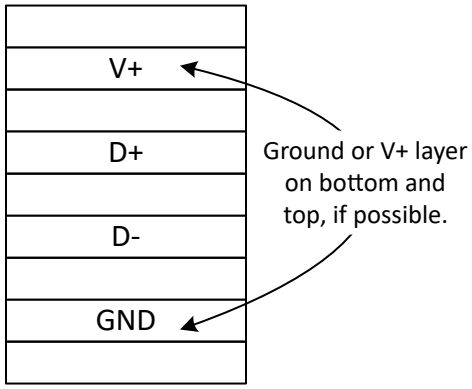
TI recommends a power-supply bypass capacitor. Place this capacitor as close as possible to the supply and ground pins of the device. A typical value for this supply bypass capacitor is 0.1 µF. Applications with noisy or high-impedance power supplies may require additional decoupling capacitors to reject power-supply noise.

8.4 Layout

8.4.1 Layout Guidelines

Remote temperature sensing on the TMP9R00-SP device measures very small voltages using very low currents; therefore, noise at the device inputs must be minimized. Most applications using the TMP9R00-SP device have high digital content, with several clocks and a multitude of logic-level transitions that create a noisy environment. Layout must adhere to the following guidelines:

1. Place the TMP9R00-SP device as close to the remote junction sensor as possible.
2. Route the D+ and D– traces next to each other and shield them from adjacent signals through the use of ground guard traces (see 図 8-5). If a multilayer PCB is used, bury these traces between the ground or V+ planes to shield them from extrinsic noise sources. TI recommends 5-mil (0.127 mm) PCB traces.
3. Minimize additional thermocouple junctions caused by copper-to-solder connections. If these junctions are used, make the same number and approximate locations of copper-to-solder connections in both the D+ and D– connections to cancel any thermocouple effects.
4. Use a 0.1-µF local bypass capacitor directly between the V+ and GND of the TMP9R00-SP. For optimum measurement performance, minimize filter capacitance between D+ and D– to 1000 pF or less. This capacitance includes any cable capacitance between the remote temperature sensor and the TMP9R00-SP.
5. If the connection between the remote temperature sensor and the TMP9R00-SP is wired and is less than eight inches (20.32 cm) long, use a twisted-wire pair connection. For lengths greater than eight inches, use a twisted, shielded pair with the shield grounded as close to the TMP9R00-SP device as possible. Leave the remote sensor connection end of the shield wire open to avoid ground loops and 60-Hz pickup.
6. Thoroughly clean and remove all flux residue in and around the pins of the device to avoid temperature offset readings as a result of leakage paths between D+ and GND, or between D+ and V+.



NOTE: Use a minimum of 5-mil (0.127 mm) traces with 5-mil spacing.

図 8-5. Suggested PCB Layer Cross-Section

8.4.2 Layout Example

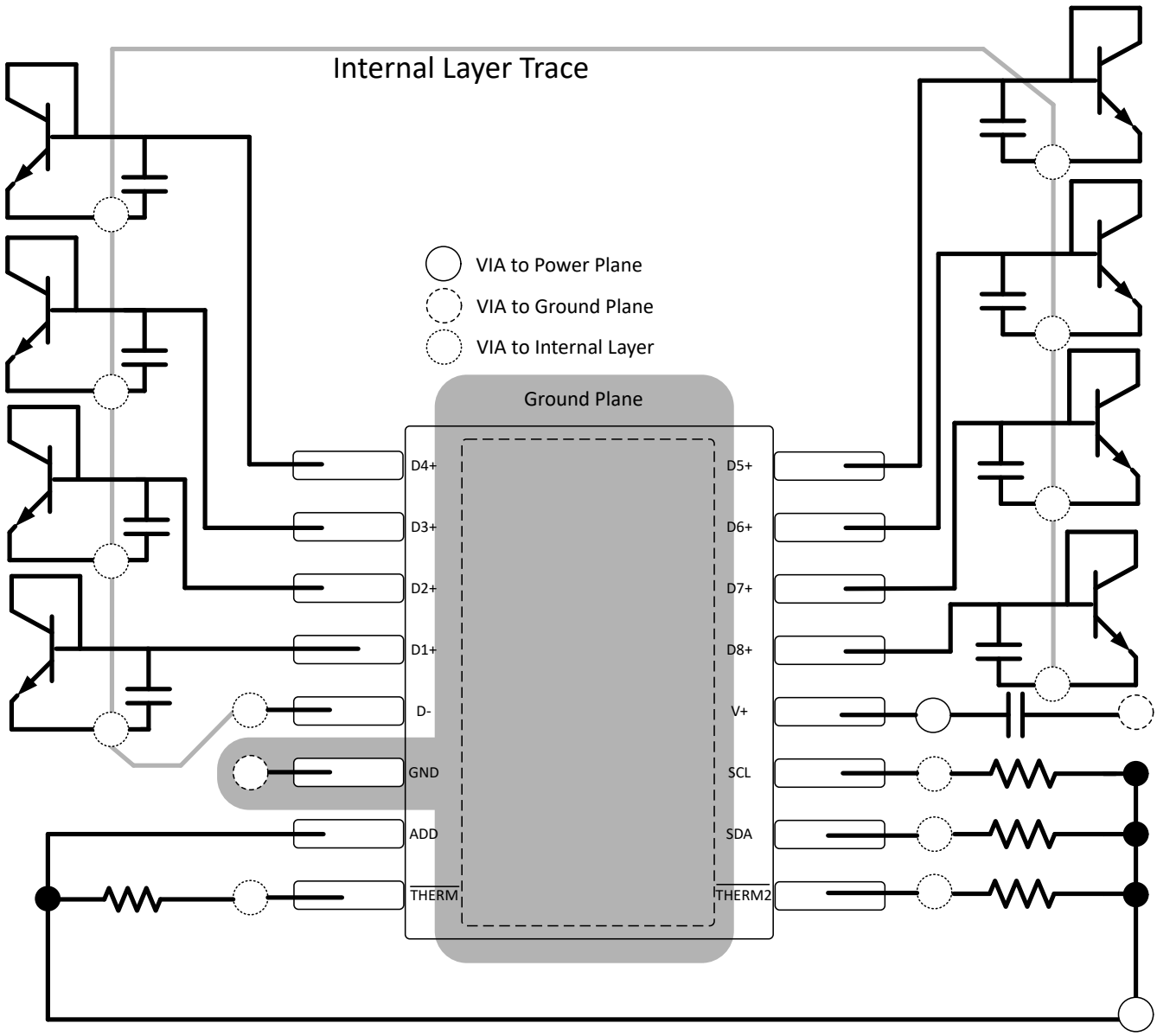


図 8-6. TMP9R00-SP HKT Example Layout

9 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

9.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

9.2 サポート・リソース

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9.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
5962R2021401VXC	ACTIVE	CFP	HKT	16	25	RoHS & Green	NIAU	N / A for Pkg Type	-55 to 125	5962R2021401 VXC TMP9R00-SP Q	Samples
TMP9R00HKT/EM	ACTIVE	CFP	HKT	16	25	RoHS & Green	NIAU	N / A for Pkg Type	-55 to 125	TMP9R00HKT/EM EVAL ONLY	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

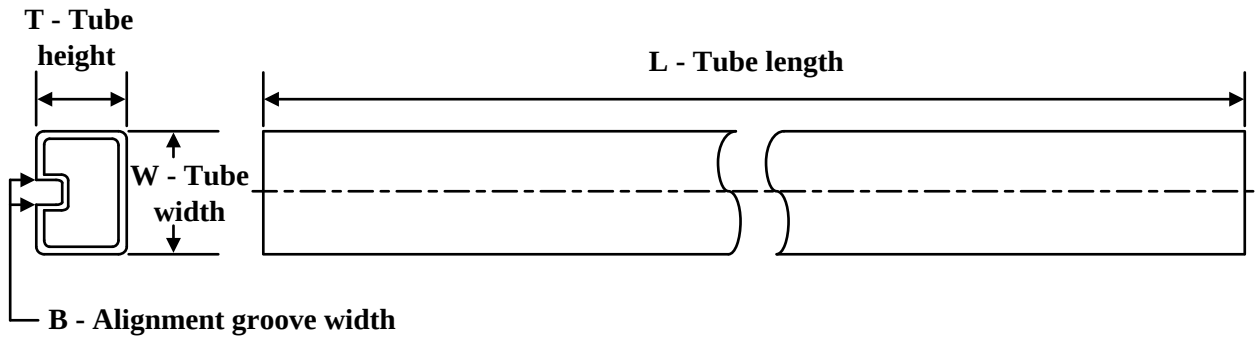
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TUBE



*All dimensions are nominal

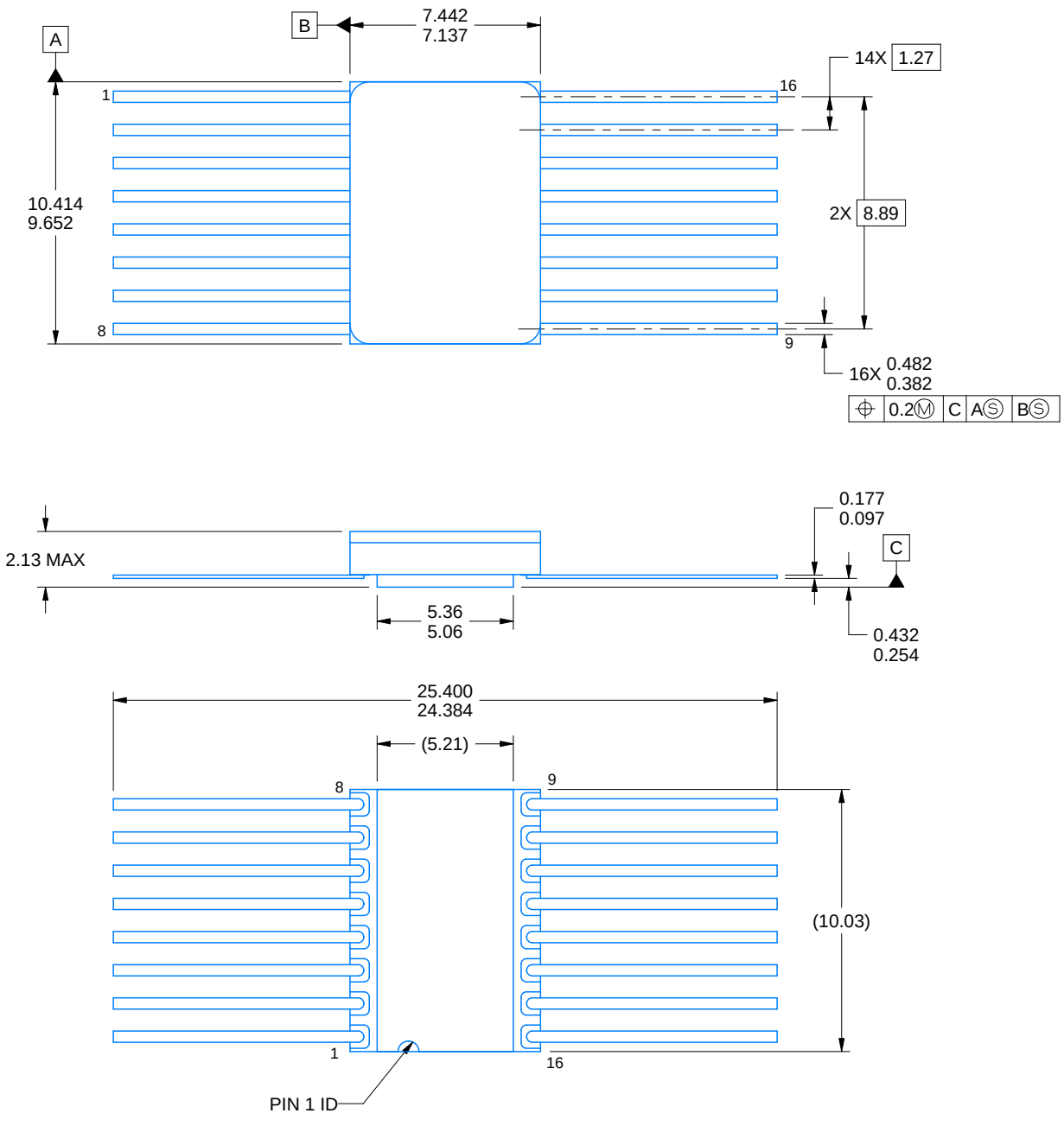
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
5962R2021401VXC	HKT	CFP (HSL)	16	25	506.98	26.16	6220	NA
TMP9R00HKT/EM	HKT	CFP (HSL)	16	25	506.98	26.16	6220	NA

PACKAGE OUTLINE

HKT0016A

CFP - 2.13 mm max height

CERAMIC DUAL FLATPACK



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a metal lid. Lid and cavity are electrically isolated
4. The terminals are gold plated.
5. Falls within MIL-STD-1835 CDFP-F11A.

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