TMS3705 トランスポンダ基地局 IC

1 特長

- TI-RFid™ RF 識別システム用基地局 IC
- アンテナを駆動
- 変調データをアンテナに送信
- トランスポンダの応答を検出および復調 (FSK)
- 短絡保護
- 診断
- スリープ・モード消費電流:0.2mA
- 車載要件に合わせて設計
- 16 ピン SOIC (D) パッケージ

2 アプリケーション

- カー・アクセス
- イモビライザ
- ビルディング・アクセス
- 家畜用リーダ

3 説明

TMS3705 トランスポンダ基地局 IC により、TI-RFid トランスポンダ・システムのアンテナを駆動し、変調データをアンテナ信号として送信し、トランスポンダの応答を検出および復調することができます。トランスポンダの応答は、周波数シフト・キーイング (FSK) 信号です。HIGH ビットまたは LOW ビットは、2 種類の高周波信号 (LOW ビットは公称 134.2kHz、HIGH ビットは公称 123kHz) でコード化されます。トランスポンダは、内蔵されたコードに従って、これらの信号をアンテナ・コイルに誘導します。トランスポンダがデータを送信するために必要な電力は、トランスポンダの蓄電コンデンサに蓄えられます。このコンデンサは、アンテナ電界により、先行する充電フェーズで充電されます。また、この IC は外部マイクロコントローラへのインターフェイスも備えています。

マイクロコントローラと基地局 IC へのクロック供給には、次の 2 つの構成があります。

1. マイクロコントローラと基地局 IC には 1 つの共振器から得られるクロック信号が供給されます。共振器はマイクロコントローラに接続されています。基地局 IC には、マイクロコントローラのデジタル・クロック出力で駆動されたクロック信号が供給されます。クロック周波数は、選択したマイクロコントローラのタイプに応じて 4MHz または 2MHz となります。
2. マイクロコントローラと基地局がそれぞれ共振器を備えている。

基地局 IC にはオンチップ PLL が搭載されており、内部クロック電源専用に 16MHz のクロック周波数を生成します。AES トランスポンダ製品 (TRPWS21GTEA または RF430F5xxx など) との組み合わせに推奨されるのは、TMS3705DDRQ1 および TMS3705GDRQ1 だけです。TMS3705EDRQ1 および TMS3705FDRQ1 は、DST40、DST80、MPT トランスポンダ (TMS37145TEAx、TMS37126xx、TMS37x128xx、TMS37x136xx、TMS37x158xx、RI-TRP-DR2B-xx、RI-TRP-BRHP-xx など) と組み合わせた場合に最高水準の性能を提供しますが、AES トランスポンダ製品と組み合わせることはできません。

製品情報 (1)

部品番号	パッケージ	本体サイズ (2)
TMS3705EDRQ1	SOIC (16)	9.9mm × 3.91mm
TMS3705DDRQ1	SOIC (16)	9.9mm × 3.91mm
TMS3705FDRQ1	SOIC (16)	9.9mm × 3.91mm
TMS3705GDRQ1	SOIC (16)	9.9mm × 3.91mm

(1) 提供中の全デバイスに関する最新の製品、パッケージ、および注文情報については セクション 12 の「付録:パッケージ・オプション」または www.ti.com のテキサス・インスツルメンツの Web サイトを参照してください。
(2) ここに記載されているサイズは概略です。許容公差を含めたパッケージの寸法については、セクション 12 の「メカニカル・データ」を参照してください。

注

- TMS3705FDRQ1 は TMS3705EDRQ1 に代わるものです
- TMS3705GDRQ1 は TMS3705DDRQ1 に代わるものです

4 Functional Block Diagram

図 4-1 shows the functional block diagram.

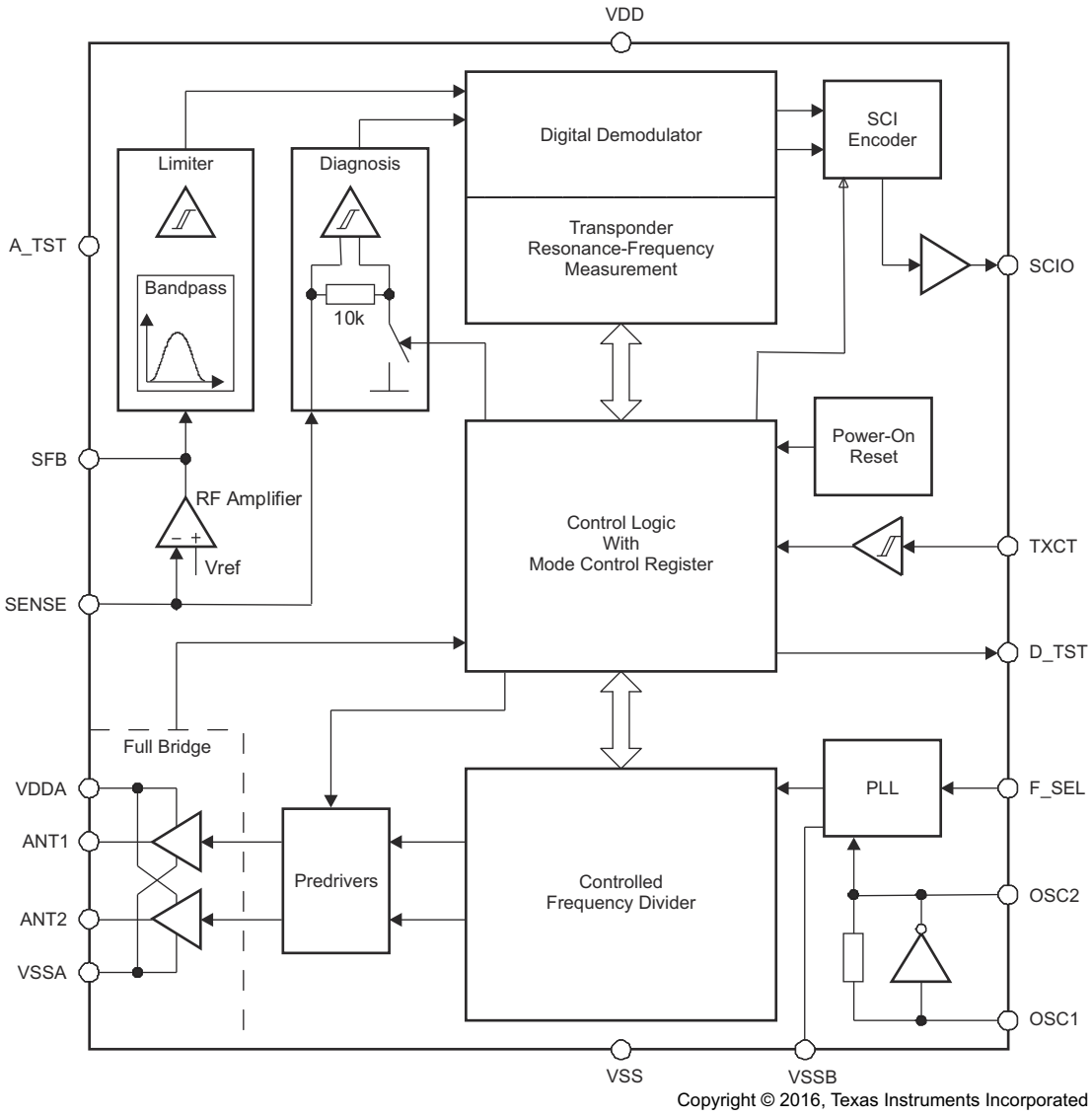

図 4-1. Functional Block Diagram

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5 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from November 1, 2018 to June 12, 2023	Page
• 文書全体にわたって表、図、相互参照の採番方法を更新	1
• セクション 3、「概要」で、「基地局 IC にはオンチップ PLL が搭載されています...」から始まる段落を更新	1
• 「説明」および「製品情報」表に TMS3705FDRQ1 および TMS3705GDRQ1 を追加	1
• Corrected typo in description of test condition of parameters GBW and φ_O	7
• Removed crystal from Detailed Description of Oscillator	11
• Corrected typo of phase shift to 180° in Detailed Description of Predriver	11
• Added TMS3705FDRQ1 in note (F) on 図 9-1, *Operational State Diagram for the Control Logic*	13
• Changed the note "Setting not allowed for..." on 表 9-1, *Mode Control Register (7-Bit Register)*	13
• Updated the paragraph that starts "The TMS3705EDRQ1..." in セクション 9.13, *Control Logic*	13
• Corrected typo of value C1 to 3.3 nF in 表 10-1 *Bill of Materials (BOM)*	17

6 Device Characteristics

表 6-1 lists the characteristics of the TMS3705.

表 6-1. Device Characteristics

Characteristic	TMS3705
Data rate (maximum)	8 kbps
Frequency	134.2 kHz
Required antenna inductance	100 to 1000 µH
Supply voltage	4.5 to 5.5 Vdc
Transmission principle	HDX, FSK

6.1 Related Products

For information about other devices in this family of products or related products, see the following links.

Products for wireless connectivity	Innovative, affordable wireless solutions for an ever-evolving connected world
Reference designs	Find reference designs leveraging the best in TI technology to solve your system-level challenges

7 Terminal Configuration and Functions

7.1 Pin Diagram

図 7-1 shows the pinout of the 16-pin D (SOIC) package.

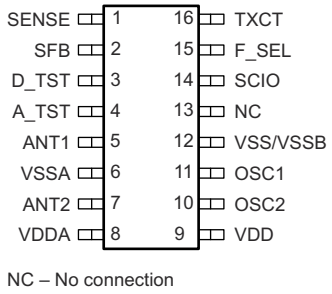


図 7-1. 16-Pin D Package (Top View)

7.2 Signal Descriptions

表 7-1 describes the device signals.

表 7-1. Signal Descriptions

TERMINAL		TYPE	DESCRIPTION
NO.	NAME		
1	SENSE	Analog input	Input of the RF amplifier
2	SFB	Analog output	Output of the RF amplifier
3	D_TST	Digital output	Test output for digital signals
4	A_TST	Analog output	Test output for analog signals
5	ANT1	Driver output	Antenna output 1
6	VSSA	Supply input	Ground for the full bridge drivers
7	ANT2	Driver output	Antenna output 2
8	VDDA	Supply input	Voltage supply for the full bridge drivers
9	VDD	Supply input	Voltage supply for nonpower blocks
10	OSC2	Analog output	Oscillator output
11	OSC1	Analog input	Oscillator input
12	VSS/VSSB	Supply input	Ground for nonpower blocks and PLL
13	NC		Not connected
14	SCIO	Digital output	Data output to the microcontroller
15	F_SEL	Digital input	Control input for frequency selection (default value is high)
16	TXCT	Digital input	Control input from the microcontroller (default value is high)

8 Specifications

8.1 Absolute Maximum Ratings(1)

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply voltage range	VDD, VSS/VSSB, VDDA, VSSA	–0.3	7	V
V_{OSC}	Voltage range	OSC1, OSC2	–0.3	V_{DD} + 0.3	V
V_{inout}	Voltage range	SCIO, TXCT, F_SEL, D_TST	–0.3	V_{DD} + 0.3	V
I_{inout}	Overload clamping current	SCIO, TXCT, F_SEL, D_TST	–5	5	mA
V_{ANT}	Output voltage	ANT1, ANT2	–0.3	V_{DD} + 0.3	V
I_{ANT}	Output peak current	ANT1, ANT2	–1.1	1.1	A
V_{analog}	Voltage range	SENSE, SFB, A_TST	–0.3	V_{DD} + 0.3	V
I_{SENSE}	SENSE input current	SENSE, SFB, A_TST	–5	5	mA
I_{SFB}	Input current in case of overvoltage	SFB	–5	5	mA
T_A	Operating ambient temperature		–40	85	°C
T_{stg}	Storage temperature		–55	150	°C
P_D	Total power dissipation at T_A = 85°C			0.5	W

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8.2 ESD Ratings

		VALUE	UNIT
V_{ESD}	ESD protection (MIL STD 883)	±2000	V

8.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{DD}	Supply voltage	VDD, VSS/VSSB, VDDA, VSSA	4.5	5	5.5	V
f_{osc}	Oscillator frequency	OSC1, OSC2		4		MHz
V_{IH}	High-level input voltage	F_SEL, TXCT, OSC1	0.7 V_{DD}			V
V_{IL}	Low-level input voltage	TXCT, OSC1			0.3 V_{DD}	V
		F_SEL			0.2 V_{DD}	
I_{OH}	High-level output current	SCIO, D_TST	–1			mA
I_{OL}	Low-level output current	SCIO, D_TST			1	mA

8.4 Electrical Characteristics

V_{DD} = 4.5 V to 5.5 V, f_{osc} = 4 MHz, F_SEL = high, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Power Supply (VDD, VSS/VSSB, VDDA, VSSA)						
I_{DD}	Supply current	Sum of supply currents in Charge phase, without antenna load		8	20	mA
I_{Sleep}	Supply current, Sleep state	Sum of supply currents in Sleep state, without I/O currents		0.015	0.2	mA
Oscillator (OSC1, OSC2)						
g_{osc}	Transconductance	f_{osc} = 4 MHz, 0.5 V_{pp} at OSC1	0.5	2	5	mA/V
C_{in}	Input capacitance at OSC1(1)				10	pF
C_{out}	Output capacitance at OSC2(1)				10	pF
Logic Inputs (TXCT, F_SEL, OSC1)						
R_{pullup}	Pullup resistance	TXCT	120		500	kΩ
		F_SEL	10		500	
Logic Outputs (SCIO, D_TST)						
V_{OH}	High-level output voltage		0.8 V_{DD}			V
V_{OL}	Low-level output voltage				0.2 V_{DD}	V
Full-Bridge Outputs (ANT1, ANT2)						
ΣR_{ds_on}	Sum of drain-source resistances	Full-bridge N-channel and P-channel MOSFETs at driver current I_{ant} = 50 mA		7	14	Ω
	Duty cycle	P-channel MOSFETs of full bridge	38%	40%	42%	
t_{on1}/t_{on2}	Symmetry of pulse durations for the P-channel MOSFETs of full bridge		96%		104.5%	
I_{oc}	Threshold for overcurrent protection		220		1100	mA
t_{oc}	Switch-off time of overcurrent protection	Short to ground with 3 Ω	0.25		10	µs
t_{doc}	Delay for switching on the full bridge after an overcurrent		2	2.05	2.1	ms
I_{leak}	Leakage current				1	µA
Analog Module (SENSE, SFB, A_TST)						
I_{SENSE}	Input current	SENSE, In charge phase	–2		2	mA
V_{DCREF}/V_{DD}	DC reference voltage of RF amplifier, related to VDD		9.25%	10%	11%	
GBW	Gain-bandwidth product of RF amplifier	At 500 kHz with external components to achieve a voltage gain of minimum 4 and 5-mV_{pp} input signal	2			MHz
φ_O	Phase shift of RF amplifier	At 134 kHz with external components to achieve a voltage gain of 5 and 20-mV_{pp} input signal			16	°
V_{sfb}	Peak-to-peak input voltage of band pass at which the limiter comparator should toggle(2)	At 134 kHz (corresponds to a minimal total gain of 1000)	5			mV
f_{low}	Lower cut-off frequency of band-pass filter(3)		24	60	100	kHz
f_{high}	Higher cut-off frequency of band-pass filter(3)		160	270	500	kHz
ΔV_{hys}	Hysteresis of limiter	A_TST pin used as input, D_TST pin as output, offset level determined by band-pass stage	25	50	135	mV
Diagnosis (SENSE)						
I_{diag}	Current threshold for operating antenna(4)		80		240	µA

8.4 Electrical Characteristics (continued)

V_{DD} = 4.5 V to 5.5 V, f_{osc} = 4 MHz, F_SEL = high, over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Phase-Locked Loop (D_TST)						
f_{pll}	PLL frequency		15.984	16	16.0166	MHz
$\Delta f/f_{pll}$	Jitter of the PLL frequency				6%	
Power-On Reset (POR)						
V_{por_r}	POR threshold voltage, rising	V_{DD} rising with low slope	1.9		3.5	V
V_{por_f}	POR threshold voltage, falling	V_{DD} falling with low slope	1.3		2.6	V

(1) Specified by design
(2) Specified by design; functional test done for input voltage of 90 mV_{pp}.
(3) Band-pass filter tested at three different frequencies: f_{mid} = 134 kHz and gain > 30 dB; f_{low} = 24 kHz; f_{high} = 500 kHz. Attenuation < –3 dB (reference = measured gain at f_{mid} = 134 kHz).
(4) Internal resistance switched on and much lower than external SENSE resistance.

8.5 Thermal Resistance Characteristics for D (SOIC) Package

PARAMETER		VALUE	UNIT
$R_{\theta JA}$	Thermal resistance, junction to ambient(1)	130	°C/W

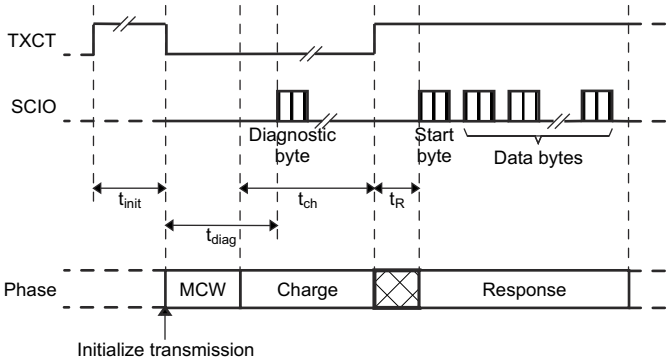
(1) The junction-to-ambient thermal resistance under natural convection is obtained in a simulation on a JEDEC-standard, High-K board, as specified in JESD51-7, in an environment described in JESD51-2a.

8.6 Switching Characteristics

V_{DD} = 4.5 V to 5.5 V, f_{osc} = 4 MHz, F_SEL = high, over operating free-air temperature range (unless otherwise noted)

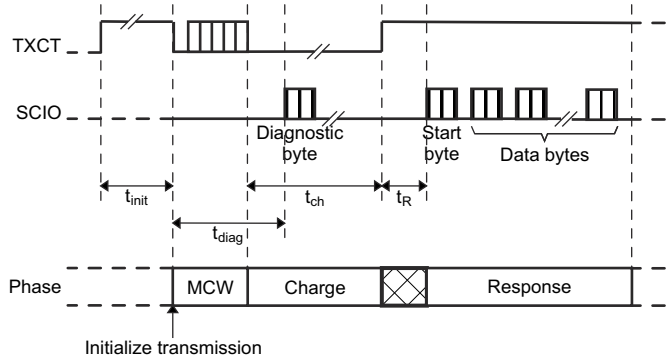
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{init\ min}$	Time for TXCT high to initialize a new transmission	From start of the oscillator after power on or waking up until reaching the Idle state (see 図 8-1, 図 8-2, 図 8-3)	2	2.05	2.2	ms
t_{diag}	Delay between leaving Idle state and start of diagnosis byte at SCIO	Normal operation (see 図 8-1, 図 8-2, 図 8-3)	2	2.12	2.2	ms
t_R	Delay between end of charge or end of program and start of transponder data transmit on SCIO	See 図 8-1, 図 8-2, 図 8-3.		3		ms
t_{off}	Write pulse pause	See 図 8-5.	0.1			ms
t_{dwrite}	Signal delay on TXCT for controlling the full bridge	Write mode	73	79	85	µs
t_{mcr}	NRZ bit duration for mode control register	See 図 8-4.	121	128	135	µs
t_{sci}	NRZ bit duration on SCIO	Asynchronous mode (see 図 8-6)	63	64	65	µs
t_{dstop}	Low signal delay on TXCT to stop	Synchronous mode	128		800	µs
t_{t_sync}	Total TXCT time for reading data on SCIO	Synchronous mode (see 図 8-7)			900	µs
t_{sync}	TXCT period for shifting data on SCIO	Synchronous mode (see 図 8-7)	4	64	100	µs
t_{L_sync}	Low phase on TXCT	Synchronous mode (see 図 8-7)	2	32	t_{sync} – 2	µs
t_{ready}	Data ready for output after SCIO goes high	Synchronous mode (see 図 8-7)	1		127	µs

8.7 Timing Diagrams



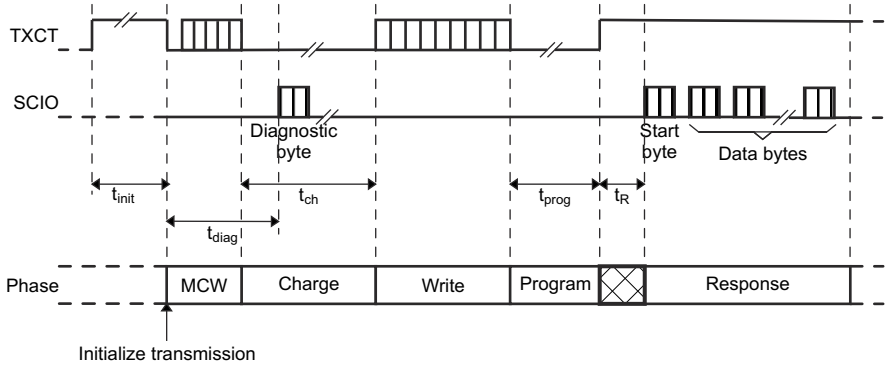
NOTE: MCW = Mode control write (to write into the mode control register)

図 8-1. Default Mode (Read Only, No Writing Into Mode Control Register)



NOTE: MCW = Mode control write (to write into the mode control register)

図 8-2. Read-Only Mode (Writing Into Mode Control Register)



NOTE: MCW = Mode control write (to write into the mode control register)

図 8-3. Write/Read Mode (Writing Into Mode Control Register)

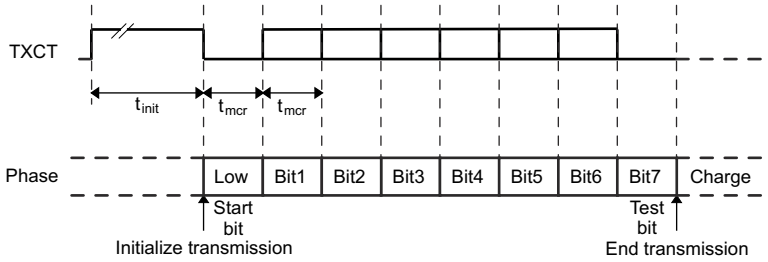


図 8-4. Mode Control Write Protocol (NRZ Coding)

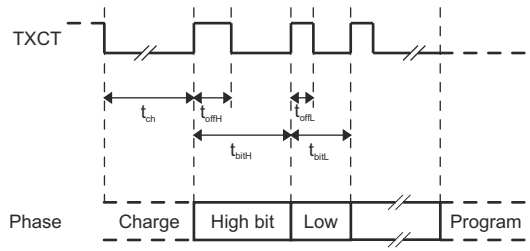


図 8-5. Transponder Write Protocol

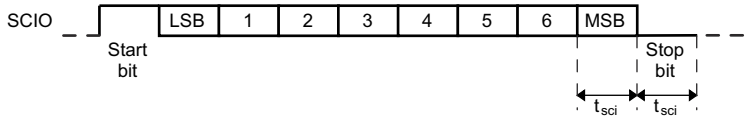


図 8-6. Transmission on SCIO in Asynchronous Mode (NRZ Coding)

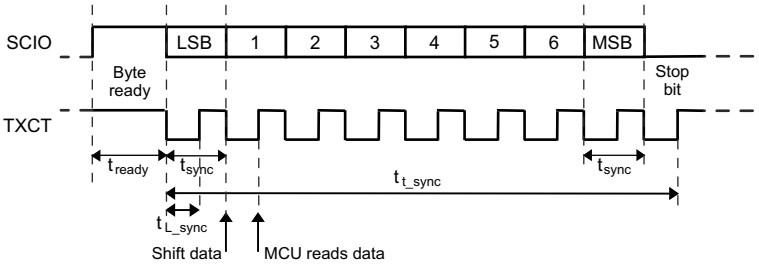


図 8-7. Transmission on SCIO in Synchronous Mode (NRZ Coding) (For Diagnosis Byte and Data Bytes)

9 Detailed Description

9.1 Power Supply

The device is supplied with 5 V by an external voltage regulator through two supply pins, one for providing the driver current for the antenna and the analog part in front of the digital demodulator and one for supplying the other blocks.

The power supply supplies a power-on reset that brings the control logic into Idle state as soon as the supply voltage drops under a certain value.

In Sleep state, the sum of both supply currents is reduced to 0.2 mA. The base station device falls into Sleep state 100 ms after TXCT has changed to high. When TXCT changes to low or is low, the base station IC immediately goes into and remains in normal operation.

9.2 Oscillator

The oscillator generates the clock of the base station IC of which all timing signals are derived. Between its input and output a ceramic resonator is connected that oscillates at a typical frequency of 4 MHz. If a digital clock signal with a frequency of 4 MHz or 2 MHz is supplied to pin OSC1, the signal can be used to generate the internal operation frequency of 16 MHz.

The oscillator block contains a PLL that generates the internal clock frequency of 16 MHz from the input clock signal. The PLL multiplies the input clock frequency depending on the logic state of the input pin F_SEL by a factor of 4 (F_SEL is high) or by a factor of 8 (F_SEL is low).

In the Sleep state, the oscillator is off.

9.3 Predrivers

The predrivers generate the signals for the four power transistors of the full bridge using the carrier frequency generated by the frequency divider. The gate signals of the P-channel power transistors (active low) have the same width (±1 cycle of the 16 MHz clock), the delay between one P-channel MOSFET being switched off and the other one being switched on is defined to be 12 cycles of the 16-MHz clock. In write mode the first activation of a gate signal after a bit pause is synchronized to the received transponder signal by a phase shift of 180°.

9.4 Full Bridge

The full bridge drives the antenna current at the carrier frequency during the charge phase and the active time of the write phase. The minimal load resistance the full bridge sees between its outputs in normal operation at the resonance frequency of the antenna is 43.3 Ω. When the full bridge is not active, the two driver outputs are switched to ground.

Both outputs of the full bridge are protected independently against short circuits to ground.

In case of an occurring short circuit, the full bridge is switched off in less than 10 µs to avoid a drop of the supply voltage. After a delay time of less than 10 ms the full bridge is switched on again to test if the short circuit is still there. An overcurrent due to a resistive short to ground that is higher than the maximum current in normal operation but lower than the current threshold for overcurrent protection does not need to be considered.

9.5 RF Amplifier

The RF amplifier is an operational amplifier with a fixed internal voltage reference and a voltage gain of 5 defined by external resistors. The RF amplifier has a high gain-bandwidth product of at least 2 MHz to show a phase shift of less than 16° for the desired signal and to give the possibility to use it as a low-pass filter by adapting additional external components.

The input signal of the RF amplifier is DC coupled to the antenna. The amplitude of the output signal of the RF amplifier is higher than 5 mV peak-to-peak.

9.6 Band-Pass Filter and Limiter

The band-pass filter provides amplification and filtering without external components. The lower cut-off frequency is approximately a factor of 2 lower than the average signal frequency of 130 kHz, the higher cut-off frequency is approximately a factor of 2 higher than 130 kHz.

The limiter converts the analog sine-wave signal to a digital signal. The limiter provides a hysteresis depending on the minimal amplitude of its input signal. The duty cycle of its digital output signal is between 40% and 60%. The band-pass filter and the limiter together have a high gain of at least 1000.

9.7 Diagnosis

The diagnosis is carried out during the charge phase to detect whether the full bridge and the antenna are working. When the full bridge drives the antenna, the voltage across the coil exceeds the supply voltage so that the voltage at the input of the RF amplifier is clamped by the ESD-protection diodes. For diagnosis, the SENSE pin is loaded on-chip with a switchable resistor to ground so that the internal switchable resistor and the external SENSE resistor form a voltage divider, while the internal resistor is switched off in read mode. When the voltage drop across the internal resistor exceeds a certain value, the diagnosis block passes the frequency of its input signal to the digital demodulator. The frequency of the diagnosis signal is accepted if eight subsequent times can be detected, all with their counter state within the range of 112 to 125, during the diagnosis time (at most 0.1 ms). The output signal is used only during the charge phase, otherwise it is ignored.

When the short-circuit protection switches off one of the full-bridge drivers, the diagnosis also indicates an improper operation of the antenna by sending the same diagnostic byte to the microcontroller as for the other failure mode.

During diagnosis, the antenna drivers are active. In synchronous mode the antenna drivers remain active up to 1 ms after the diagnosis is performed, without any respect to the logic state of the signal at TXCT (thus enabling the microcontroller to clock out the diagnosis byte).

9.8 Power-on Reset

The power-on reset generates an internal reset signal to allow the control logic to start up in the defined way.

9.9 Frequency Divider

The frequency divider is a programmable divider that generates the carrier frequency for the full-bridge antenna drivers. The default value for the division factor is the value 119 needed to provide the nominal carrier frequency of 134.45 kHz generated from 16 MHz. The resolution for programming the division factor is one divider step that corresponds to a frequency shift of approximately 1.1 kHz. The different division factors needed to cover the range of frequencies for meeting the resonance frequency of the transponder are 114 to 124.

9.10 Digital Demodulator

The input signal of the digital demodulator comes from the limiter and is frequency-coded according to the high- and low-bit sequence of the transmitted transponder code. The frequency of the input signal is measured by counting the oscillation clock for the time period of the input signal. As the high-bit and low-bit frequencies are specified with wide tolerances, the demodulator is designed to distinguish the high-bit and the low-bit frequency by the shift between the two frequencies and not by the absolute values. The threshold between the high-bit and the low-bit frequency is defined to be 6.5 kHz lower than the measured low-bit frequency and has a hysteresis of ±0.55 kHz.

The demodulator is controlled by the control logic. After the charge phase (that is during read or write phase) it measures the time period of its input signal and waits for the transponder resonance-frequency measurement to determine the counter state for the threshold between high-bit and low-bit frequency. Then the demodulator waits for the occurrence of the start bit. For that purpose, the results of the comparisons between the measured time periods and the threshold are shifted in a 12-bit shift register. The detection of the start bit comes into effect when the contents of the shift register matches a specific pattern, indicating 8 subsequent periods below the threshold immediately followed by 4 subsequent periods above the threshold. A 2-period digital filter is inserted

in front of the 12-bit shift register to make a start bit detection possible in case of a nonmonotonous progression of the time periods during a transition from low- to high-bit frequency.

The bit stream detected by the input stage of the digital demodulator passes a digital filter before being evaluated. After demodulation, the serial bit flow received from the transponder is buffered byte-wise before being sent to the microcontroller by SCI encoding.

9.11 Transponder Resonance-Frequency Measurement

During the prebit reception phase, the bits the transponder transmits show the low-bit frequency, which is the resonance frequency of the transponder. The time periods of the prebits are evaluated by the demodulator counter. Based on the counter states, an algorithm is implemented that ensures a correct measurement of the resonance frequency of the transponder:

1. A time period of the low-bit frequency has a counter state between 112 and 125.
2. The measurement of the low-bit frequency (the average of eight subsequent counter states) is accepted during the write mode, when the eight time periods have counter states in the defined range. The measurement during write mode is started with the falling edge at TXCT using the fixed delay time at which end the full bridge is switched on again.
3. The counter state of the measured low-bit frequency results in the average counter state of an accepted measurement and can be used to update the register of the programmable frequency divider.
4. The measurement of the low-bit frequency (the average of eight subsequent counter states) is accepted during the read mode, when the eight time periods have counter states in the defined range. The start of the measurement during read mode is delayed to use a stable input signal for the measurement.
5. The threshold to distinguish between high-bit and low-bit frequency is calculated to be by a value of 5 or 7 (see hysteresis in threshold) higher than the counter state of the measured low-bit frequency.

9.12 SCI Encoder

An SCI encoder performs the data transmission to the microcontroller. As the transmission rate of the transponder is lower than the SCI transmission rate, the serial bit flow received from the transponder is buffered after demodulation and before SCI encoding.

The SCI encoder uses an 8-bit shift register to send the received data byte-wise (least significant bit first) to the microcontroller with a transmission rate of 15.625 kbaud (±1.5 %), 1 start bit (high), 1 stop bit (low), and no parity bit (asynchronous mode indicated by the SYNC bit of the Mode Control register is permanently low). The data bits at the SCIO output are inverted with respect to the corresponding bits sent by the transponder.

The transmission starts after the reception of the start bit. The start byte detection is initialized with the first rising edge. Typical values for the start byte are 81_H or 01_H (at SCIO). The start byte is the first byte to be sent to the microcontroller. The transmission stops and the base station returns to the Idle state when TXCT becomes low or 20 ms after the beginning of the read phase. TXCT remains low for at least 128 µs to stop the read phase and less than 900 µs to avoid starting the next transmission cycle.

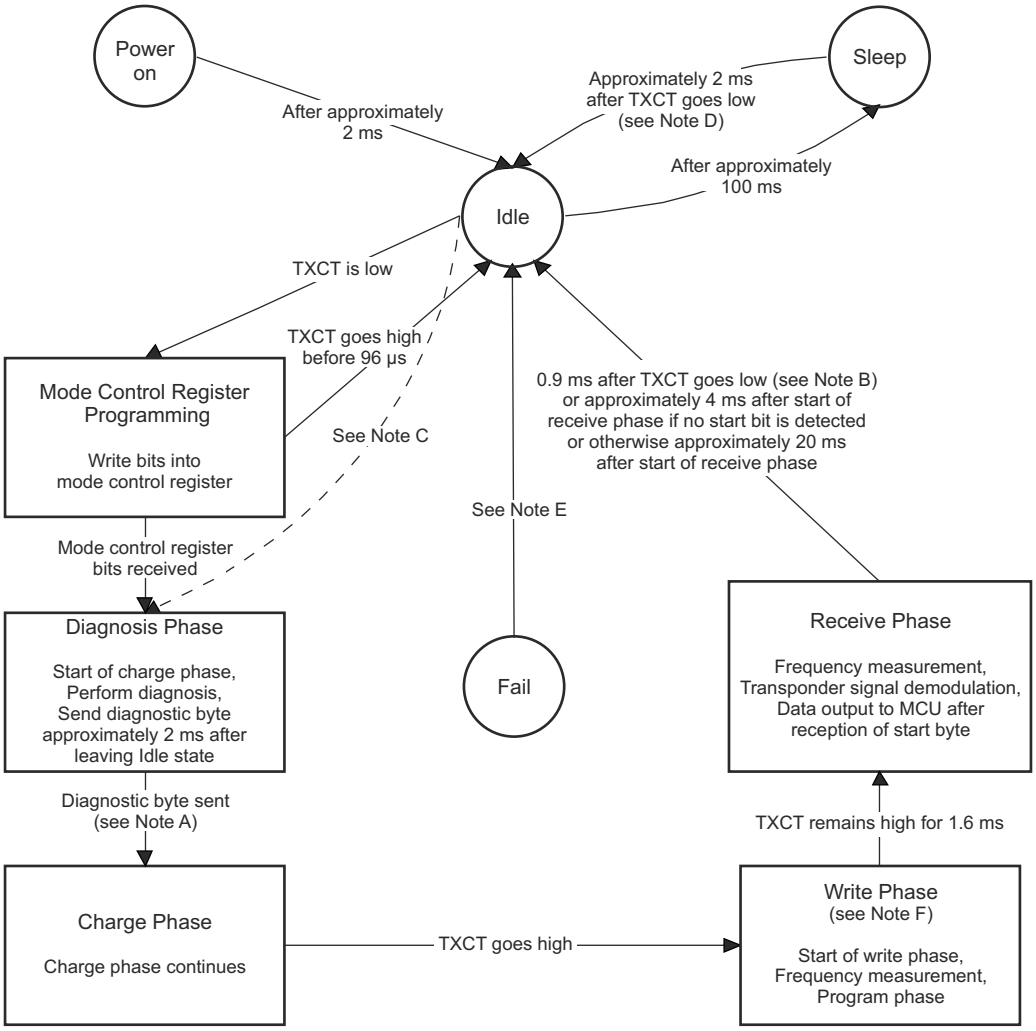
The SCI encoder also sends the diagnostic byte 2 ms after beginning of the charge phase. In case of a normal operation of the antenna, the diagnostic byte AF_H is sent. If no antenna oscillation can be measured or if at least one of the full-bridge drivers is switched off due to a detected short circuit, the diagnostic byte FF_H is sent to indicate the failure mode.

The SCI encoder can be switched into a synchronous data transmission mode by setting the mode control register bit SYNC to high. In this mode, the output SCIO indicates by a high state that a new byte is ready to be transmitted. The microcontroller can receive the 8 bits at SCIO when sending the eight clock signals (falling edge means active) for the synchronous data transmission through pin TXCT to the SCI encoder.

9.13 Control Logic

The control logic is the core of the TMS3705 circuit. This circuit contains a sequencer or a state machine that controls the global operations of the base station (see 図 9-1). This block has a default mode configuration but can also be controlled by the microcontroller through the TXCT serial input pin to change the configuration and

to control the programmable frequency divider. For that purpose a mode control register is implemented in this module that can be written by the microcontroller.



A. In SCI synchronous mode, this transition always occurs approximately 3 ms after leaving Idle state. Diagnostic byte transmission is complete before the transition.
B. A falling edge on TXCT interrupts the receive phase after a delay of 0.9 ms. TXCT must remain low for at least 128 µs. If TXCT is still low after the 0.9-ms delay, the base station enters the Idle state and then the Diagnosis phase one clock cycle later (see the dotted line marked with "See Note C"). No mode control register can be written, and only the default mode is fully supported in this case. Otherwise, if TXCT returns high and remains high during the delay, the base station stays in Idle state and waits for TXCT to go low (which properly starts a new mode control register programming operation) or waits for 100 ms to enter the Sleep state.
C. This transition occurs only in a special case, as described in Note B.
D. A falling edge on TXCT interrupts the Sleep state. Only the default mode is fully supported when starting an operation from the Sleep state with only one falling edge on TXCT, because of the 2-ms delay. For proper mode control register programming, TXCT must return to high and remain high during this delay.
E. Idle state is the next state in case of undefined states (fail-safe state machine).
F. Frequency measurement is available for the TMS3705EDRQ1 and TMS3705FDRQ1 only.

図 9-1. Operational State Diagram for the Control Logic

The default mode is a read-only mode that uses the default frequency as the carrier frequency for the full bridge. Therefore the mode control register does not need to be written (it is filled with low states), and the communication sequence between microcontroller and base station starts with TXCT being low for a fixed time

to initiate the charge phase. When TXCT becomes high again, the module enters the read phase and the data transmission through the SCIO pin to the microcontroller starts.

There is another read-only mode that differs from the default mode only in the writing of the mode control register before the start of the charge phase. The method to fill the mode control register and the meaning of its contents is described in the following paragraphs.

The write-read mode starts with the programming of the mode control register. Then the charge phase starts with TXCT being low for a fixed time. When TXCT becomes high again, the write phase begins in which the data are transmitted from the microcontroller to the transponder through the TXCT pin, the control logic, the predrivers, and the full bridge by amplitude modulation of 100% with a fixed delay time. After the write phase TXCT goes low again to start another charge or program phase. When TXCT becomes high again, the read phase begins.

The contents of the mode control register (see 表 9-1) define the mode and the way that the carrier frequency generated by the frequency divider is selected to meet the transponder resonance frequency as closely as possible.

表 9-1. Mode Control Register (7-Bit Register)

BIT		RESET VALUE	DESCRIPTION	
NAME	NO.			
START_BIT	Bit 0	0	START_BIT = 0	The start bit is always low and does not need to be stored.
DATA_BIT1	Bit 1	0	DATA_BIT[4:1] = 0000	Microcontroller selects division factor 119
			DATA_BIT[4:1] = 1111	Division factor is adapted automatically(1)
DATA_BIT2	Bit 2	0	DATA_BIT[4:1] = 0001	Microcontroller selects division factor 114
			DATA_BIT[4:1] = 0010	Microcontroller selects division factor 115
DATA_BIT3	Bit 3	0	...	...
			DATA_BIT[4:1] = 0110	Microcontroller selects division factor 119
DATA_BIT4	Bit 4	0	...	...
			DATA_BIT[4:1] = 1011	Microcontroller selects division factor 124
SCI_SYNC	Bit 5	0	SCI_SYNC = 0	Asynchronous data transmission to the microcontroller
			SCI_SYNC = 1	Synchronous data transmission to the microcontroller
RX_AFC	Bit 6	0	RX_AFC = 0	Demodulator threshold is adapted automatically
			RX_AFC = 1	Demodulator threshold is defined by DATA_BIT[4:1]
TEST_BIT	Bit 7	0	TEST_BIT = 0	No further test bytes
			TEST_BIT = 1	Further test byte follows for special test modes

(1) Setting is not allowed for TMS3705DDRQ1 and TMS3705GDRQ1.

The TMS3705EDRQ1 and TMS3705FDRQ1 can adjust the carrier frequency to the transponder resonance frequency automatically by giving the counter state of the transponder resonance-frequency measurement directly to the frequency divider by setting the first 4 bits in high state. The other combinations of the first 4 bits allow the microcontroller to select the default carrier frequency or to use another frequency. The division factor can be selected to be between 114 and 124.

Some bits are included for testability reasons. The default value of these test bits for normal operation is low. Bit 7 (TEST_BIT) is low for normal operation; otherwise, the base station may enter one of the test modes.

The control logic also controls the demodulator, the SCI encoder, the diagnosis, and the transmission of the diagnosis byte during the charge phase.

The state diagram in 図 9-1 shows the general behavior of the state machine (the state blocks drawn can contain more than one state). All given times are measured from the moment when the state is entered if not specified otherwise.

9.14 Test Pins

The IC has an analog test pin A_TST for the analog part of the receiver. The digital output pin D_TST is used for testing the internal logic. Connecting both pins is not required.

10 Applications, Implementation, and Layout

注

以下のアプリケーション情報は、TI の製品仕様に含まれるものではなく、TI ではその正確性または完全性を保証いたしません。個々の目的に対する製品の適合性については、お客様の責任で判断していただくことになります。お客様は自身の設計実装を検証しテストすることで、システムの機能を確認する必要があります。

10.1 Application Diagram

図 10-1 shows a typical application diagram.

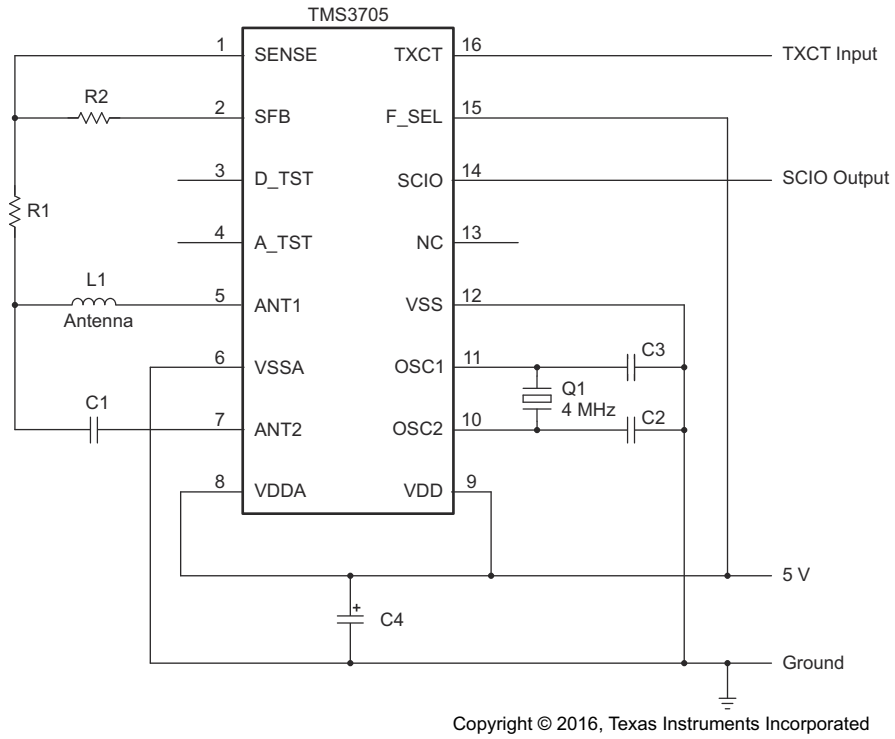


図 10-1. Application Diagram

表 10-1 lists the bill of materials for the application in 図 10-1.

表 10-1. Bill of Materials (BOM)

COMPONENT	VALUE	COMMENTS
R1	47 kΩ	
R2	150 kΩ	
L1	422 µH at 134 kHz	Sumida part number: Vogt 581 05 042 40
C1	3.3 nF	NPO , COG (high Q types). Voltage rating must be 100 V or higher depending on Q factor.
C2	220 pF	NPO
C3	220 pF	NPO
C4	22 µF	Low ESR
Q1	4-MHz resonator	muRata part number: CSTCR4M00G55B-R0. See resonator data sheet (load capacitance is important).

11 Device and Documentation Support

11.1 Getting Started and Next Steps

RFID products from TI provide the ultimate solution for a wide range of applications. With its patented HDX technology, TI RFID offers unmatched performance in read range, read rate and robustness. For more information, see Overview for NFC / RFID.

11.2 Device Nomenclature

To designate the stages in the product development cycle, TI assigns prefixes to the part numbers of devices. Each device has one of three prefixes: X, P, or null (no prefix) (for example, *TMS3705*).

Device development evolutionary flow:

X Experimental device that is not necessarily representative of the final device's electrical specifications and may not use production assembly flow.

P Prototype device that is not necessarily the final silicon die and may not necessarily meet final electrical specifications.

null Production version of the silicon die that is fully qualified.

X and P devices are shipped against the following disclaimer:

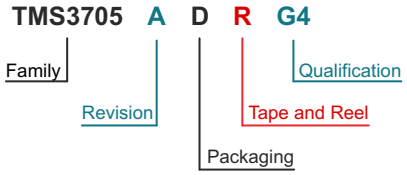
"Developmental product is intended for internal evaluation purposes."

Production devices have been characterized fully, and the quality and reliability of the device have been demonstrated fully. TI's standard warranty applies.

Predictions show that prototype devices (X or P) have a greater failure rate than the standard production devices. TI recommends that these devices not be used in any production system because their expected end-use failure rate still is undefined. Only qualified production devices are to be used.

TI device nomenclature also includes a suffix with the device family name. This suffix indicates the package type (for example, *D*). 図 11-1 provides a legend for reading the complete device name.

For orderable part numbers of *TMS3705* devices in the *D* package types, see the *Package Option Addendum* in セクション 12, the TI website, or contact your TI sales representative.



Family	TMS3705 = Transponder base station IC
Revision	A1, B, C, D = Silicon revision
Packaging	http://www.ti.com/packaging
Tape and Reel	R = Large reel
Qualification	G4 = Green (RoHS and no Sb, Br) Q1 = Q100 Qualified

図 11-1. Device Nomenclature

11.3 Tools and Software

Design Kits and Evaluation Modules

Low-Frequency Demo Reader	The ADR2 Evaluation Kit contains a low-frequency reader required to evaluate and operate the TI Car Access products. The kit comes with a reader base board, LF antenna, and a USB-RS232 adapter. Together with the PC software available online, all functions of the reader can be controlled and all automotive transponders, remote keyless entry, and passive entry devices can be addressed. Operation of transponder functions and also passive entry communication is supported by the same system without component changes.
PaLFI, Passive Low-Frequency Evaluation Kit TMS37157	The PaLFI Evaluation kit contains all components required to evaluate and operate the TMS37157. The kit comes with an eZ430 MSP430F1612 USB development stick, and an MSP430 target board including an MSP430F2274 plus the TMS37157 PaLFI. A battery board for active operation in addition to an RFID base station reader/writer provide the infrastructure for various evaluation setups.

11.4 Documentation Support

The following documentation describes the transponder, related peripherals, and other technical collateral.

Receiving Notification of Document Updates

To receive notification of documentation updates—including silicon errata—go to the TMS3705 product folder. In the upper right corner, click the "Alert me" button. This registers you to receive a weekly digest of product information that has changed (if any). For change details, check the revision history of any revised document.

Application Reports

Resonant Trimming Sequence	This application report presents an efficient and precise method on how to achieve the desired resonant frequency of configuring the trim array with only a few iterations and measuring the resonant frequency.
TMS3705 Range Extender Power Solution Using UCC27424-Q1	This application report provides supplementary information about the TI 134.2-kHz RFID Base Station IC TMS3705x in combination with an external driver IC. In particular, the document shows a low cost and easy-to-implement solution to improve the communication distance between the transaction processor (TRP) and the Reader unit.
TMS3705 Passive Antenna Solution	The TI low-frequency transponder technology provides the possibility to use a simple passive antenna in combination with various antenna cable lengths. This solution significantly reduces system costs because the active part of the transceiver can be added to the already existing host system; for example, the body control module (BCM) of a vehicle.
Integrated TIRIS RF Module TMS3705A Introduction to Low Frequency Reader	A TIRIS setup consists of one or more Transponders and a Reader. The Reader described in this application note normally contains the Reader Antenna, the RF Module and the Control Module.

More Literature

Wireless Connectivity Tri-fold Overview	At TI, we are committed to delivering a broad portfolio of wireless connectivity solutions which consume the lowest power and are the easiest to use. With TI innovation supporting your designs, you can share, monitor and manage data wirelessly for applications in wearables, home and building automation, manufacturing, smart cities, healthcare and automotive.

MSP430™ Ultra-Low-Power MCUs and TI-RFid Devices	The TI portfolio of MSP430 microcontrollers and TI-RFid devices is an ideal fit for low-power, robust RFID reader and transponder solutions. Together, MSP430 and TI-RFid devices help RF designers achieve low power consumption, best-in-class read range and reliable performance at a competitive price.

11.5 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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11.6 Trademarks

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11.7 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

11.8 用語集

テキサス・インスツルメンツ用語集	この用語集には、用語や略語の一覧および定義が記載されています。

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TMS3705EDRQ1	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-40 to 85	TMS3705EQ1
TMS3705FDRQ1	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TMS3705FQ1
TMS3705FDRQ1.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TMS3705FQ1
TMS3705GDRQ1	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TMS3705GQ1
TMS3705GDRQ1.A	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	TMS3705GQ1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

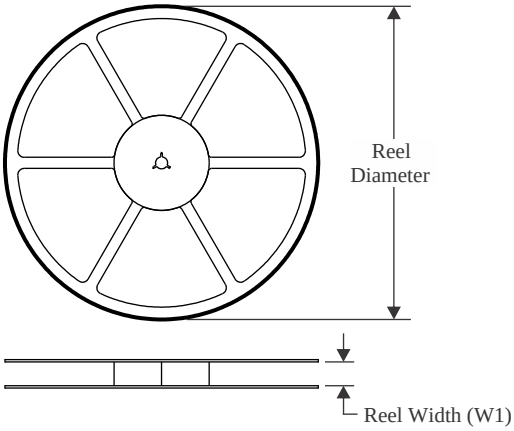
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

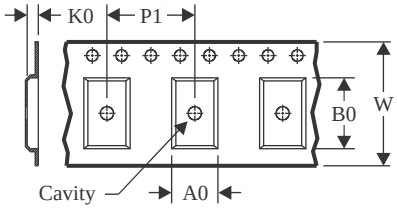
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

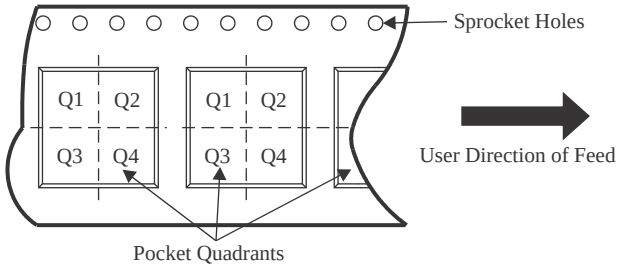


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

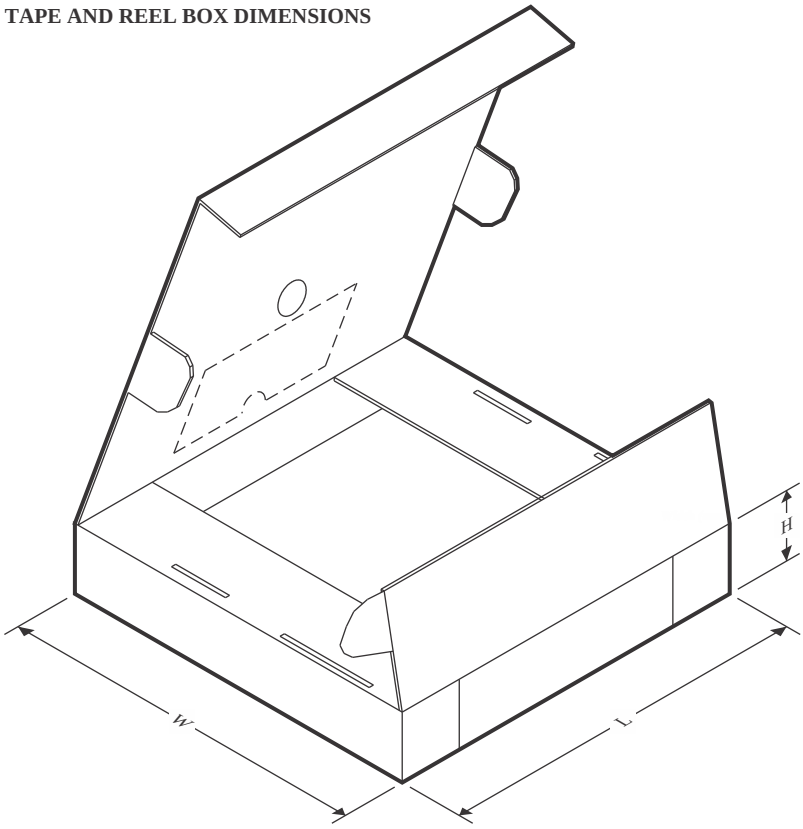
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMS3705FDRQ1	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
TMS3705GDRQ1	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

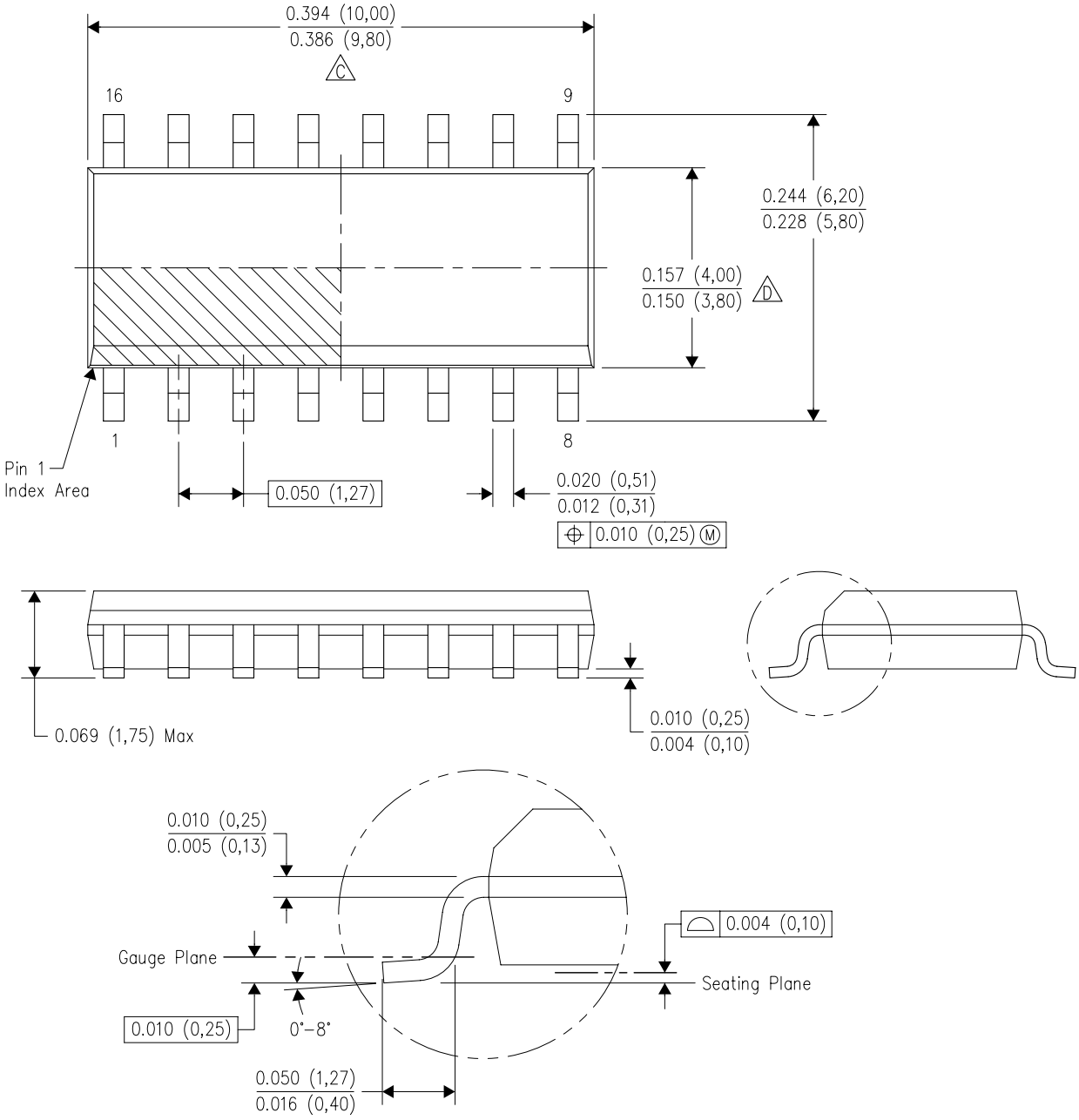
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMS3705FDRQ1	SOIC	D	16	2500	356.0	356.0	35.0
TMS3705GDRQ1	SOIC	D	16	2500	356.0	356.0	35.0

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265