TMUX131 4V、低静電容量、3：1 2 チャネル・マルチプレクサ

1 特長

- 高速 I3C 信号と互換
- V_{DD} 範囲：2.5V～4.3V
- 高性能スイッチ特性：
  - 帯域幅 (–3dB)：6.5GHz
  - R_{ON} (標準値)：5.5Ω
  - C_{ON} (標準値)：1.3pF
- 消費電流：28µA (標準値)
- ロジック・ピンにプルダウン抵抗を内蔵
- 特別な機能：
  - I_{OFF} 保護により、パワー・ダウン状態 (V_{DD} = 0V) での電流リークを防止
  - 1.8V 互換の制御入力 (SEL)
  - 外部部品なしで、すべての I/O ピンにおいて最大 5.5V の過電圧耐性 (OVT)
- ESD 性能：
  - 2kV、人体モデル (A114-B、Class II)
  - 1kV、デバイス帯電モデル (C101)
- パッケージ：
  - 12 ピンの VQFN パッケージ (1.8mm × 1.8mm、0.5mm 刻み)

2 アプリケーション

- I3C (SenseWire)
- I3C および I2C ペリフェラル・スイッチング
- サーバー
- 携帯電話：スマートフォン
- ノート PC
- タブレット：マルチメディア
- レジ用電子機器
- 現場用計測機器
- ポータブル・モニタ

3 概要

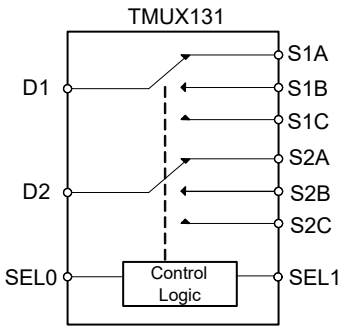
TMUX131 デバイスは、高性能双方向 2 チャネルの 3:1 マルチプレクサで、差動およびシングル・エンドの両方の信号をサポートします。TMUX131 は、電源オフ保護機能を備えたアナログ・パッシブ・マルチプレクサで、VDD ピンに電力が供給されていないときは、すべての I/O ピンが強制的に高インピーダンス・モードになります。TMUX131 の選択ピンは、1.8V および 3.3V 制御ロジックと互換性があるため、低電圧プロセッサからの汎用 I/O (GPIO) と直接インターフェイスが可能です。この TMUX131 はオン抵抗が低くオン静電容量が小さいため、I3C などの高速規格を含め、幅広いアナログ信号およびデジタル通信プロトコル規格のスイッチングをサポートするのに最適なデバイスです。

TMUX131 は、小型の 12 ピン VQFN パッケージで供給されており、そのサイズはわずか 1.8mm × 1.8 mm であることから、PCB 面積が限られている場合に便利です。

パッケージ情報

部品番号	パッケージ (1)	パッケージ・サイズ (2)
TMUX131	RMG (VQFN、12)	1.8mm × 1.8 mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



スイッチ図

Table of Contents

4 Revision History

DATE	REVISION	NOTES
August 2023	*	Initial Release

5 Pin Configuration and Functions

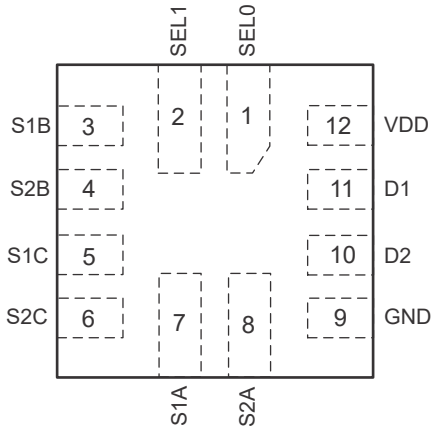


図 5-1. RMG Package, 12-Pin VQFN (Top View)

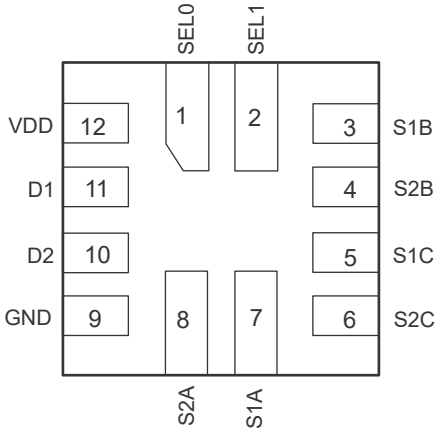


図 5-2. RMG Package, 12-Pin VQFN (Bottom View)

表 5-1. Pin Functions

PIN		TYPE(1)	DESCRIPTION
NAME	NO.		
SEL0	1	I	Switch logic control. Controls the switch connects as provided in 表 7-1
SEL1	2	I	Switch logic control. Controls the switch connects as provided in 表 7-1
S1B	3	I/O	Source pin 1B. Can be an input or output.
S2B	4	I/O	Source pin 2B. Can be an input or output.
S1C	5	I/O	Source pin 1C. Can be an input or output.
S2C	6	I/O	Source pin 2C. Can be an input or output.
S1A	7	I/O	Source pin 1A. Can be an input or output.
S2A	8	I/O	Source pin 2A. Can be an input or output.
GND	9	G	Ground
D2	10	I/O	Drain pin 2. Can be an input or output.
D1	11	I/O	Drain pin 1. Can be an input or output.
VDD	12	P	Power Supply

(1) G = Ground, I = Input, O = Output, P = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2)

		MIN	MAX	UNIT
V_{DD}	Supply voltage(3)	–0.3	5.5	V
$V_{S/D}$	Input/Output DC voltage(3)	–0.3	5.5	V
I_K	Input/Output port diode current ($V_{S/D}$ < 0)	–50		mA
V_I	Digital input voltage (SEL0, SEL1)	–0.3	5.5	
I_{IK}	Digital logic input clamp current (V_I < 0)(3)	–50		mA
$I_{I/O}$	Continuous switch DC output current		60	mA
T_{stg}	Storage temperature	–65	150	°C

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 500-V HBM is possible with the necessary precautions. Pins listed as ±2000 V may actually have higher performance.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process. Manufacturing with less than 250-V CDM is possible with the necessary precautions. Pins listed as ±1000 V may actually have higher performance.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{DD}	Supply voltage	2.5	4.3	V
$V_{S/D}$,	Analog voltage	0	3.6	V
V_{SEL}	Digital input voltage (SEL0, SEL1)	0	V_{DD}	V
$T_{RAMP\ (VDD)}$	Power supply ramp time requirement (VDD)	100	1000	µs/V
$I_{S/D,\ PEAK}$	Peak switch DC output current (1-ms duration pulse at <10% duty cycle)		150	mA
T_A	Operating free-air temperature	–40	85	°C

6.4 Thermal Information

THERMAL METRIC(1)		TMUX131 RMG (VQFN) 12 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	160.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	95.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	91.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	7.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	91.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_A = –40°C to 85°C, typical values are at V_{DD} = 3.3 V and T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{ON}	ON-state resistance	V_{DD} = 2.5 V, V_S = 1.5V, I_{ON} = –8 mA (see 図 7-1)		5.5	7	Ω
ΔR_{ON}	ON-state resistance match between channels	V_{DD} = 2.5 V, V_S = 1.5 V, I_{ON} = –8 mA		0.1		Ω
$R_{ON (FLAT)}$	ON-state resistance flatness	V_{DD} = 2.5 V, V_S = 1.5 V to 3.3 V, I_{ON} = –8 mA		1		Ω
I_{OZ}	OFF leakage current	V_{DD} = 4.3 V, Switch OFF, V_S = 1.5 V to 3.3 V, V_D= 0 V (see 図 7-2)	–2		2	µA
I_{OFF}	Power-off leakage current	V_{DD} = 0 V, Power off, V_S = 1.5 V to 3.3 V, V_D= NC	–10		10	µA
I_{ON}	ON leakage current	V_{DD} = 4.3 V, Switch ON, V_S = 1.5 V to 3.3 V, V_D= NC	–2		2	µA
DIGITAL CONTROL INPUTS (SEL)						
V_{IH}	Input logic high	V_{DD} = 2.5 V to 4.3 V	1.3			V
V_{IL}	Input logic low	V_{DD} = 2.5 V to 4.3 V			0.6	V
I_{IN}	Input leakage current	V_{DD} = 4.3 V, $V_{S/D}$ = 0 V to 3.6 V, V_{SEL} = 0 V to 4.3 V	–10		10	µA

6.6 Dynamic Characteristics

T_A = –40°C to 85°C, Typical values are at V_{DD} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{pd}	Propagation delay	R_L = 50 Ω, CL = 5 pF, V_{DD} = 2.5 V to 4.3 V, V_S = 0.4 V or 3.3 V		50		ps
t_{TRAN}	Switching time from control input	R_L = 50 Ω, CL = 5 pF, V_{DD} = 2.5 V to 4.3 V, V_S = 0.4 V or 3.3 V			400	ns
t_{ON}	Switch turnon time (from disabled to active mode)	R_L = 50 Ω, CL = 5 pF, V_{DD} = 2.5 V to 4.3 V, V_S = 0.4 V or 3.3 V			100	µs
t_{OFF}	Switch turnoff time (from active to disabled mode)	R_L = 50 Ω, CL = 5 pF, V_{DD} = 2.5 V to 4.3 V, V_S = 0.4 V or 3.3 V			100	µs
$C_{S(ON)}$ $C_{D(ON)}$	ON capacitance	V_{DD} = 3.3 V, V_S = 0 V or 3.3 V, f = 240 MHz, Switch ON		1.3		pF
$C_{S(OFF)}$	OFF capacitance	V_{DD} = 3.3 V, V_S = 0 V or 3.3 V, f = 240 MHz, Switch OFF		1		pF
C_I	Digital input capacitance	V_{DD} = 3.3 V, V_I = 0 V or 2 V		2.2		pF
O_{ISO}	Differential OFF isolation	V_S = –10 dBm, V_{DC_BIAS} = 2.4 V, RT = 50 Ω, f = 240 MHz (see 図 7-3), Switch OFF		–38		dB
X_{TALK}	Channel-to-Channel Crosstalk	V_S = –10 dBm, V_{DC_BIAS} = 0.2 V, RT = 50 Ω, f = 240 MHz (see 図 7-4), Switch ON		–38		dB
BW	–3-dB bandwidth	V_{DD} = 2.5 V to 4.3 V, R_L = 50 Ω (see 図 7-5), Switch ON		6.5		GHz
SUPPLY						
V_{DD}	Power supply voltage		2.5		4.3	V
I_{DD}	Positive supply current	V_{DD} = 4.3 V, V_{IN} = V_{DD} or GND, V_S = 0 V, Switch ON or OFF		28	40	µA

6.7 Typical Characteristics

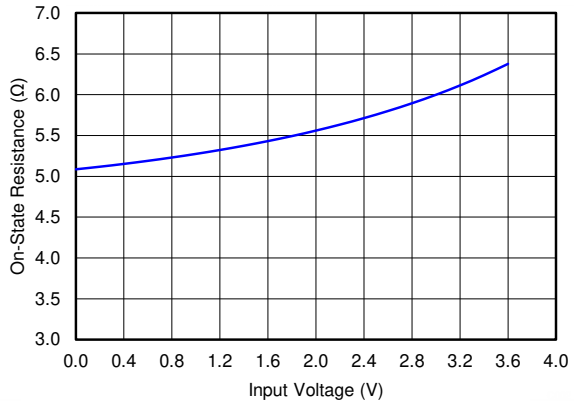


図 6-1. ON-Resistance vs V_S

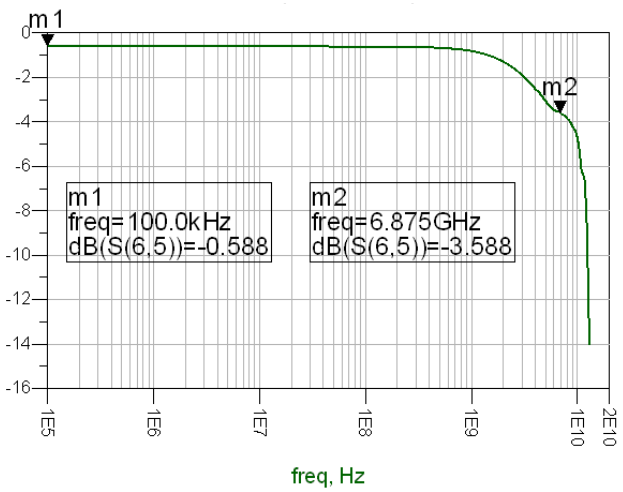


図 6-2. Typical Differential Bandwidth vs Frequency

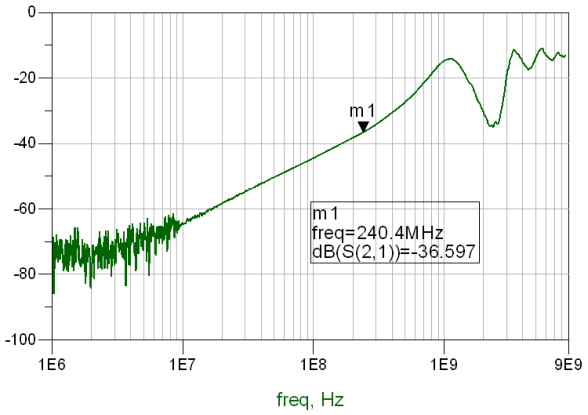


図 6-3. OFF Isolation vs Frequency

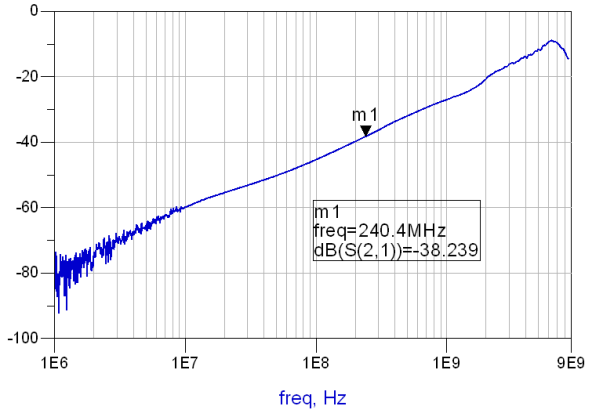


図 6-4. Cross Talk vs Frequency

Parameter Measurement Information

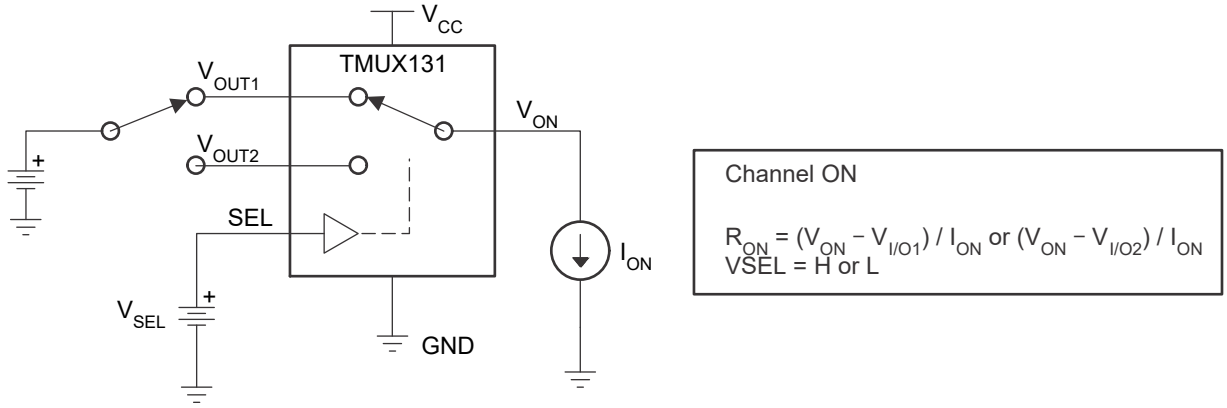


図 7-1. ON-State Resistance (R_{ON})

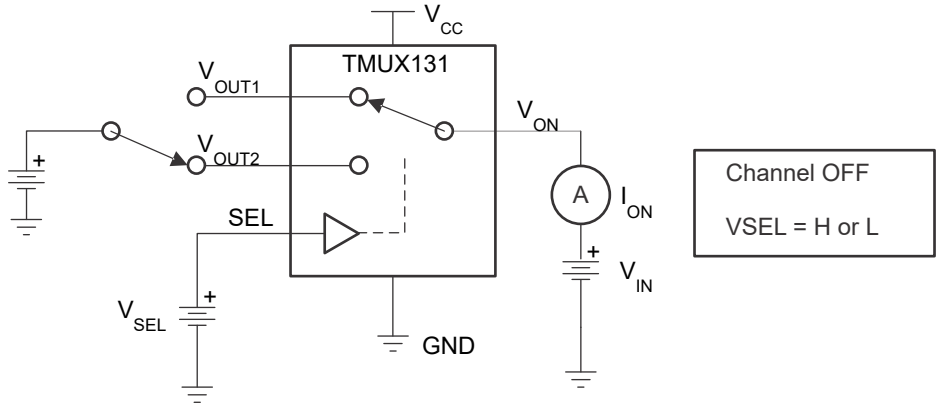


図 7-2. OFF Leakage Current (I_{OZ})

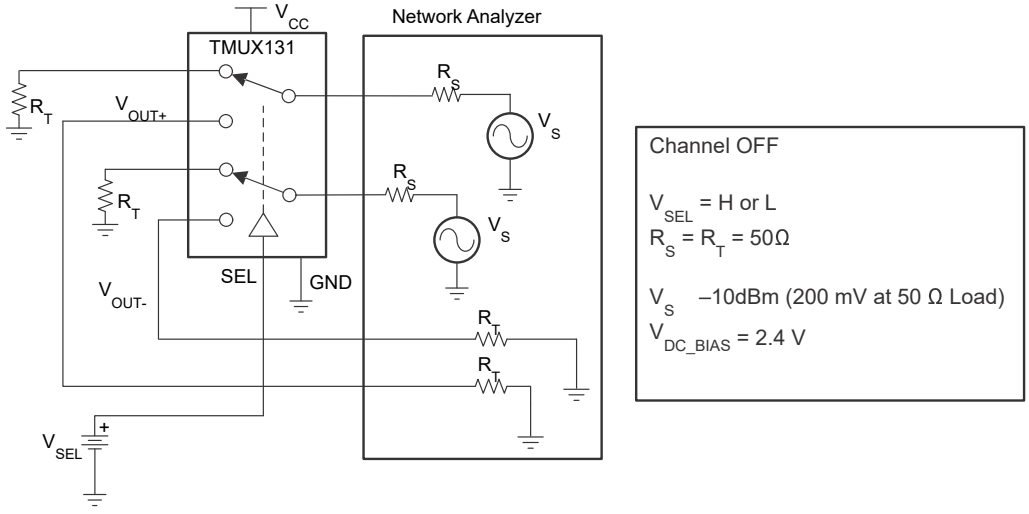


図 7-3. Differential Off-Isolation (O_{ISO})

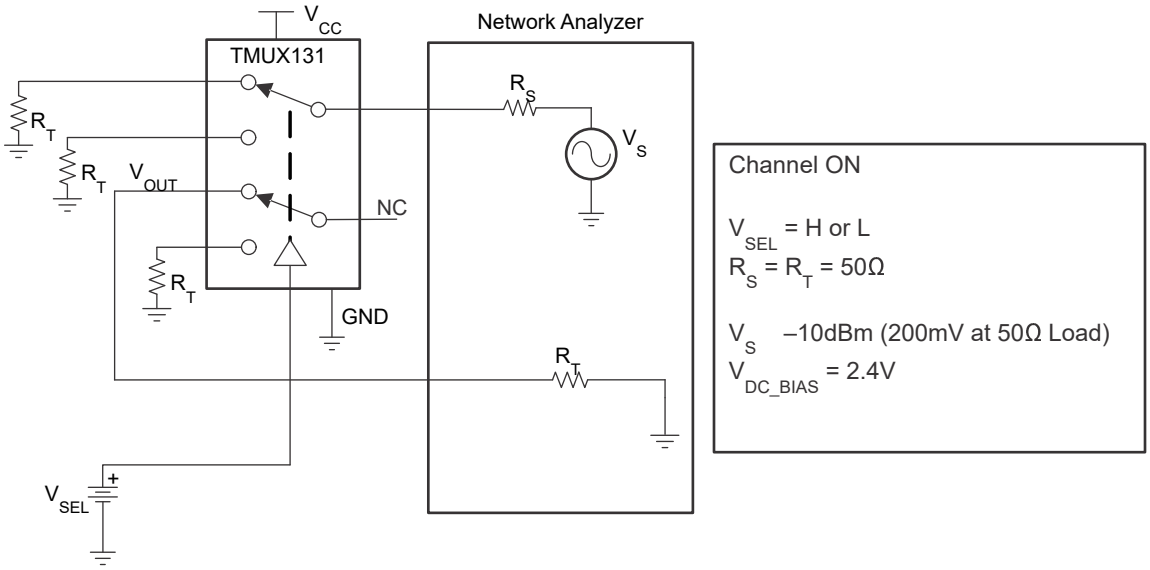


図 7-4. Crosstalk (Xtalk)

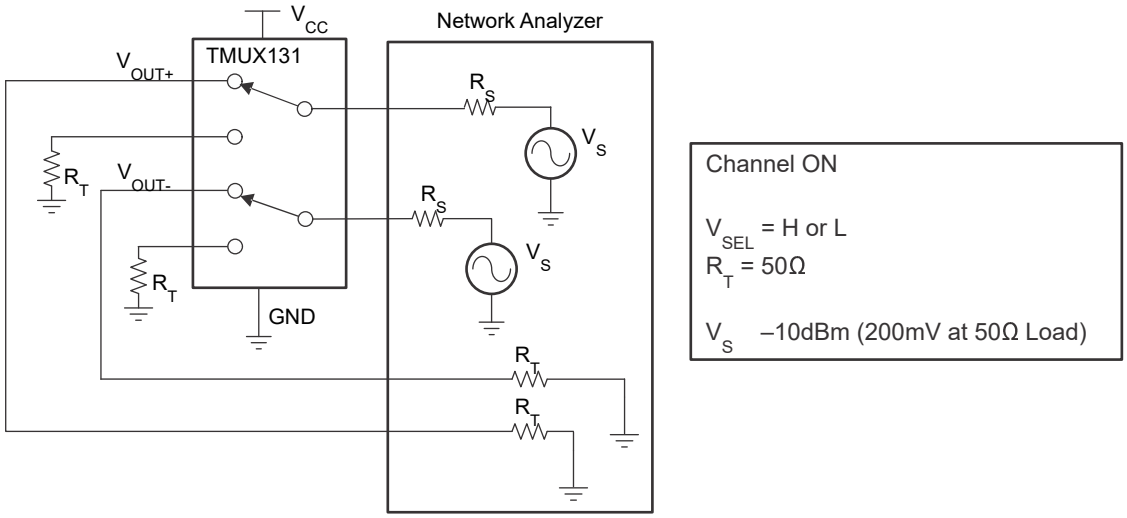


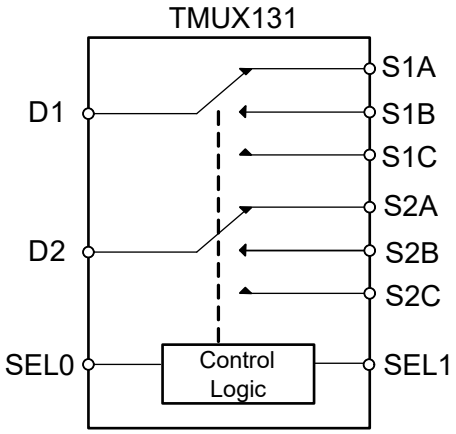
図 7-5. Differential Bandwidth (BW)

7 Detailed Description

7.1 Overview

The TMUX131 device is an analog passive 2 channel, 3:1 multiplexer that can work for any low-speed, high-speed, differential or single ended signals. Excellent low capacitance characteristics of the device allow signal switching with minimal attenuation and very little added jitter. The signals must be within the allowable voltage range of 0 to 3.6 V.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 I_{OFF} Protection

I_{OFF} protection percents current leakage through the device when V_{DD} = 0 V This allows signals to be present on the source and drain pins before the device is powered up without damaging the device or system.

7.3.2 1.8-V Compatible Logic

The TMUX131 device supports 1.8-V logic irrespective to the supply voltage applied to the IC.

7.3.3 Overvoltage Tolerant (OVT)

The source and drain pins of the device can support signals up to 5.5 V without damaging the device. This protects the TMUX131 in case of an overvoltage fault event with no extra components needed.

7.3.4 Integrated Pull-Down Resistors

The TMUX131 has internal weak pull-down resistors (6 MΩ) to GND so that the logic pins are not left floating. This feature integrates up to two external components and reduces system size and cost.

7.4 Device Functional Modes

表 7-1 lists the functional modes of the TMUX131.

表 7-1. Function Table

SEL1	SEL0	SWITCH STATUS
Low	Low	D1/D2 connected to S1B/S2B
Low	High	D1/D2 connected to S1C/S2C
High	Low	D1/D2 connected to S1A/S2A
High	High	All switches in High-Z

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TMUX131 is a passive, bidirectional, 2-channel 1:3 switch, which makes it versatile for many high speed 1:3 switching applications. This device can be used for general protocol switching applications such as I^3C, I^2C, UART, LVDS, and other analog signal applications.

8.2 Typical Application

8.2.1 Signal Expansion (I^3C and I^2C)

There are many applications in which microprocessors or controllers have a limited number of I/Os. The TMUX131 solution can effectively expand the limited I/Os by switching between multiple buses to interface them to a single microprocessor or controller. A common application where the TMUX131 is used as a I^3C 1:3 multiplexer. In this application, the TMUX131 is used to route communicating between different peripherals from a single controller or driver within a server, as shown in 図 8-1. The high bandwidth of the TMUX131 will preserve signal integrity at even the fastest communication protocols that may be used in server applications, such as I^3C. Also, because I^3C is backwards compatible, any of the peripherals can also be I^2C, and the TMUX131 will still support it.

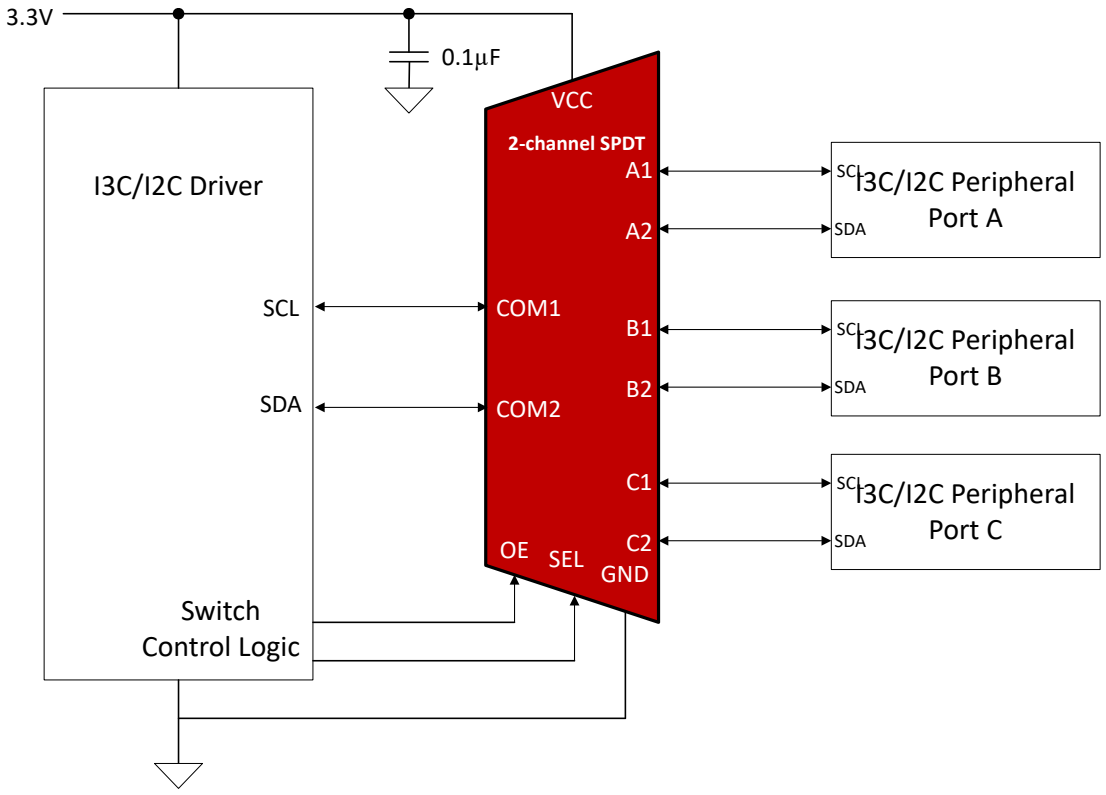


図 8-1. Typical TMUX131 Application

8.2.2 Design Requirements

The TMUX131 supports I^3C standard by maintaining signal integrity through the switch. 表 8-1 details how the TMUX131 specifications make this device optimal for switching I^3C signals.

表 8-1. TMUX131 I^3C Compatibility

	I^3C Requirements	TMUX131
Voltage	1.0 V, 1.2 V, 1.8 V, and 3.3 V	0 – 3.6 V
Frequency	Up to 12.5 MHz	6.5 GHz Bandwidth
Capacitance	50 pF maximum bus capacitance	< 2 pF On or Off Capacitance

8.2.3 Detailed Design Procedure

The TMUX131 can operate properly without any external components. However, TI recommends to connect unused signal I/O pins to ground through a 50-Ω resistor to prevent signal reflections back into the device.

8.2.4 Application Curves

図 8-2 shows TMUX131 bandwidth. This bandwidth can easily support the maximum data rate of the I^3C standard. A combination of low on-resistance, low capacitance, and low added jitter from the device allows it to be used for I^3C.

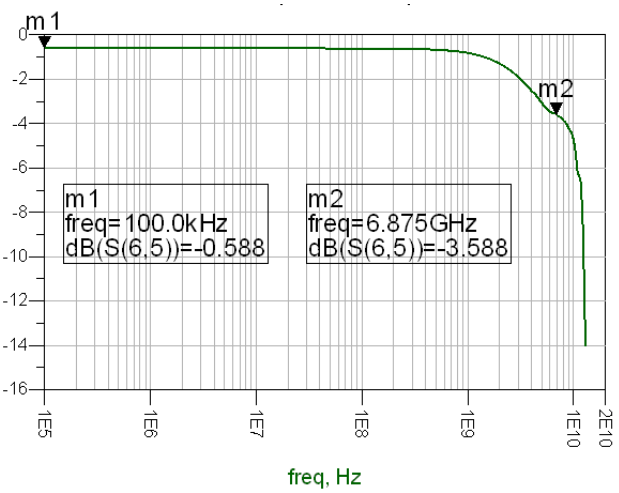


図 8-2. Typical Differential Bandwidth vs Frequency

8.3 Power Supply Recommendations

The TMUX131 does not require a power supply sequence. However, TI recommends to enable the device after VDD is stable and in specification. TI also recommends to place a bypass capacitor as close to the supply pin (VDD) as possible to help smooth out lower frequency noise and provide better load regulation across the frequency spectrum.

8.4 Layout

8.4.1 Layout Guidelines

Place supply bypass capacitors as close to VDD pin as possible and avoid placing the bypass capacitors near the high speed traces.

Route the high-speed signals using a minimum of vias and corners which reduces signal reflections and impedance changes. When a via must be used, increase the clearance size around it to minimize its capacitance. Each via introduces discontinuities in the signal's transmission line and increases the chance of picking up interference from the other layers of the board. Be careful when designing test points on twisted pair lines; through-hole pins are not recommended.

When it becomes necessary to turn 90°, use two 45° turns or an arc instead of making a single 90° turn. Doing this reduces reflections on the signal traces by minimizing impedance discontinuities. Avoid stubs on the high-speed signals because they cause signal reflections. Route all high-speed signal traces over continuous planes (VDD or GND) with no interruptions.

Due to high frequencies, a printed circuit board with at least four layers is recommended; two signal layers separated by a ground and power layer as shown in 図 8-3.

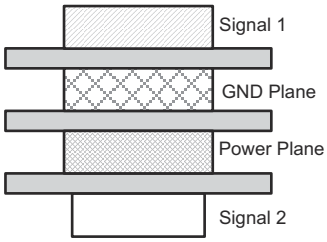


図 8-3. Four-Layer Board Stack-Up

The majority of signal traces must run on a single layer, preferably Signal 1. Immediately next to this layer must be the GND plane, which is solid with no cuts. Avoid running signal traces across a split in the ground or power plane. When running across split planes is unavoidable, sufficient decoupling must be used. Minimizing the number of signal vias reduces EMI by reducing inductance at high frequencies.

For high speed layout guidelines, refer to *High-Speed Layout Guidelines* application note.

8.4.2 Layout Example

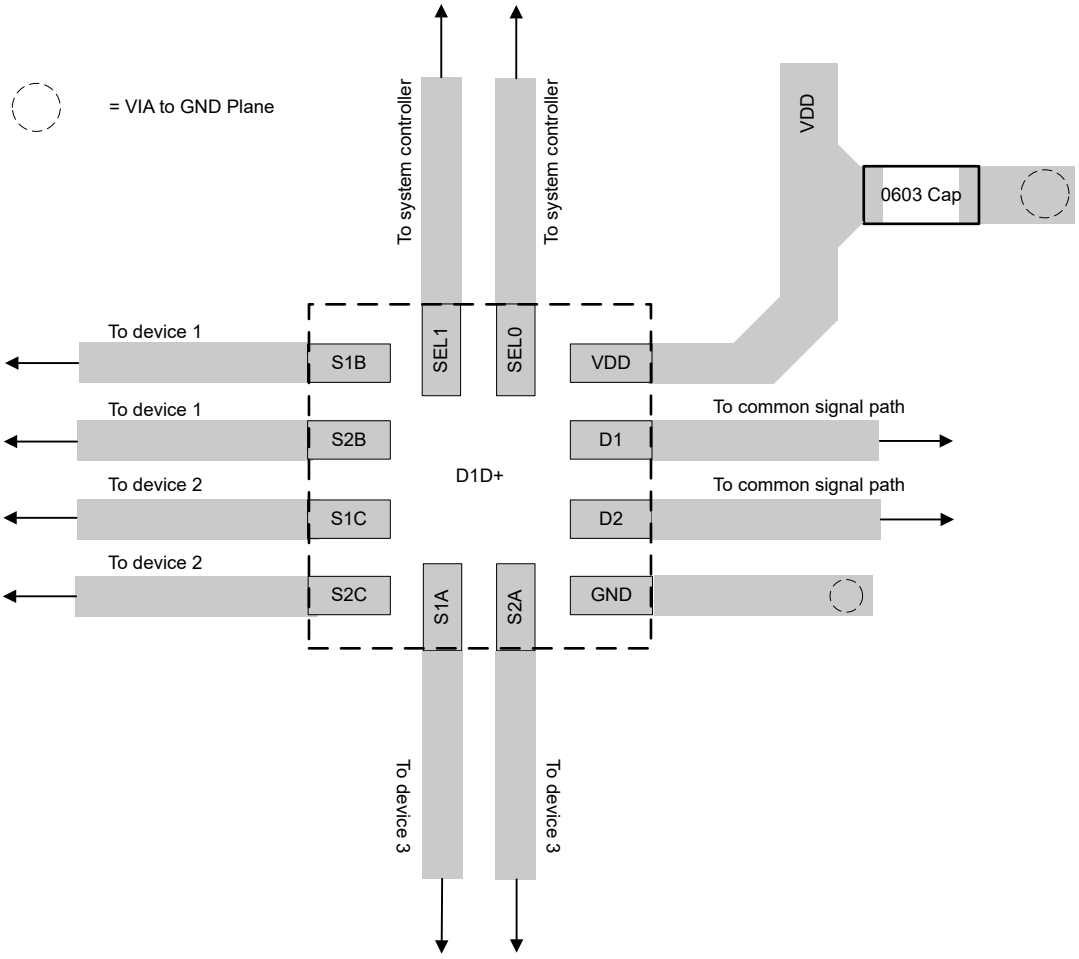


図 8-4. Layout Recommendation

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *High Speed Layout Guidelines*

9.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。「更新の通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

9.3 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の使用条件を参照してください。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

9.5 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUX131RMGR	ACTIVE	WQFN	RMG	12	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	OH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

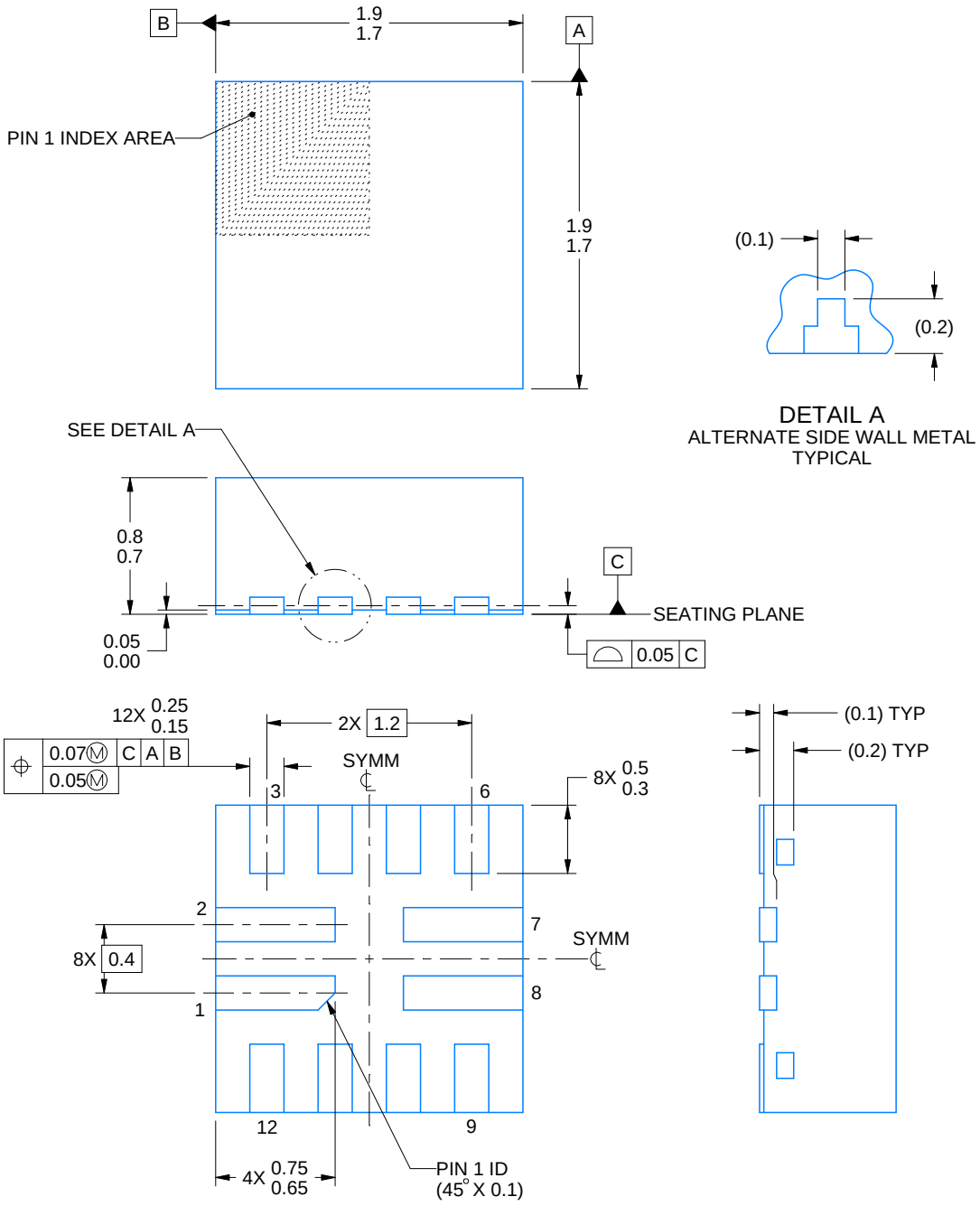
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

RMG0012A

PACKAGE OUTLINE

VQFN - 0.8 mm max height

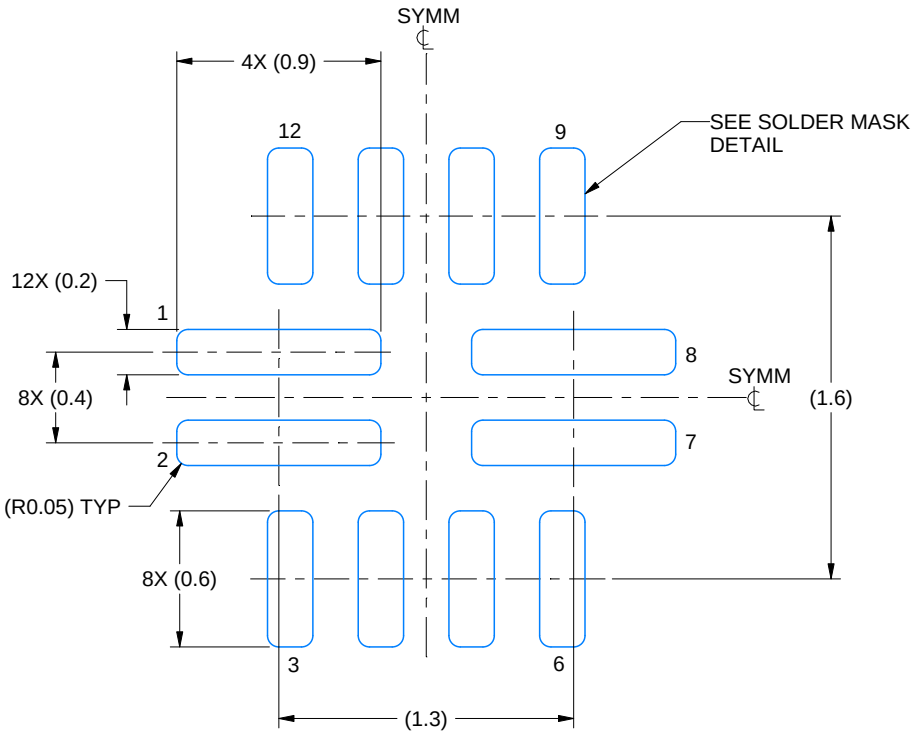
PLASTIC QUAD FLATPACK - NO LEAD



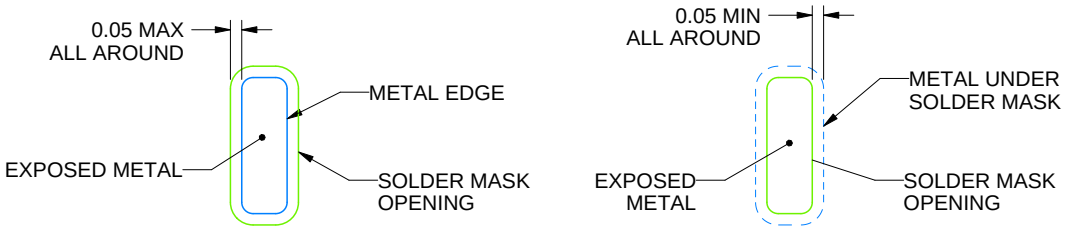
4226797/A 05/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 30X

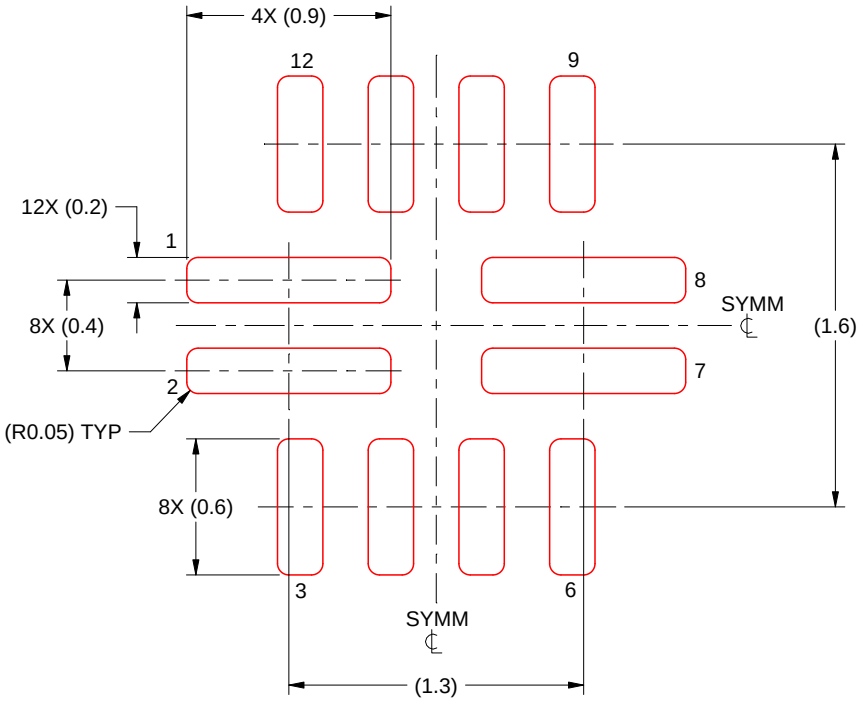


SOLDER MASK DETAILS

4226797/A 05/2021

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 30X

4226797/A 05/2021

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265