TMUX9616 ラッチアップ耐性付き、220V 高電圧 1:1、16 チャネル・スイッチ

1 特長

- 広い電源電圧範囲または入力信号範囲:
  - 両電源: ±20V～±110V、220V_{PP}
  - 240V_{PP} の絶対最大値
- 低いオフ容量:5pF
- 低いオン容量:10pF
- 低いオン抵抗 (R_{ONL}):12Ω
- 高速ターンオン時間:3µs (最大値)
- 最大 72MHz のデータ・シフト・クロック周波数
- ロジック・レベル:1.8V～5V
- 非常に優れたオフ絶縁性能:-70dB (5MHz 時)
- 出力にブリード抵抗を内蔵
- デバイス構造に基づくラッチアップ耐性
- 拡張温度
  範囲:–40℃～125℃
- 業界標準の 7mm × 7mm (本体サイズ) LQFP パッケージによるピン互換の実現

2 アプリケーション

- 医療用超音波画像処理
- 非破壊試験 (NDT) による金属の欠陥検出
- 圧電性のトランスデューサ・ドライバ
- 超音波流量トランスミッタ
- プリンタ
- 光 MEMS モジュール

3 概要

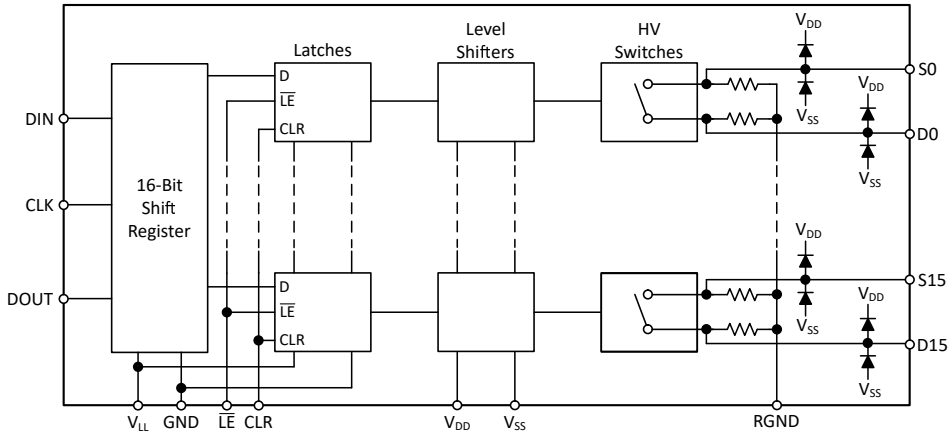
TMUX9616 は、ラッチアップ耐性を備えた、16 チャネル、低抵抗、低静電容量、高電圧のアナログ・スイッチ集積回路 (IC) です。各デバイスは、独立して選択可能な 16 個の 1:1 単極単投 (SPST) スイッチ・チャネルを備えています。このデバイスは、最大±110V の両電源で良好に動作します。推奨電源範囲内では、非対称の電源バイアスもサポートされています。TMUX9616 は、ソース (Sx) およびドレイン (Dx) ピンで、V_{SS} から V_{DD} までの範囲の双方向アナログおよびデジタル信号をサポートします。TMUX9616 また、ソース (Sx) ピンとドレイン (Dx) ピンにブリード抵抗を内蔵しており、圧電トランスデューサなどの容量性負荷を放電します。TMUX9616 医療用超音波イメージングやその他の圧電トランスデューサ・ドライバ・アプリケーション向けの優れた選択肢になります。

TMUX9616 カスケード接続可能な 16 ビット・シフト・レジスタを内蔵し、16 個の各スイッチを制御するためのラッチを搭載しています。デイジーチェーン機能により、デバイスごとに個別のチップ・セレクトを必要とせずに、多くの TMUX9616 デバイスを制御できます。潜在的なクロック・フィードスルーによる信号パスのノイズを低減するために、データがシフト・レジスタにロードされている間、アクティブ・ローのラッチ・イネーブルを High に保持することができます。16 ビット・シフト・レジスタは、1.8V～5V の電源で動作できます。16 ビット・シフト・レジスタは、最高 72MHz のクロック速度をサポートできます。

パッケージ情報

部品番号	パッケージ(1)	パッケージ・サイズ(2)
TMUX9616	PT (LQFP、48)	9mm × 9mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。



概略回路図

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4 Revision History

DATE	REVISION	NOTES
September 2023	*	Initial Release

5 Pin Configuration and Functions

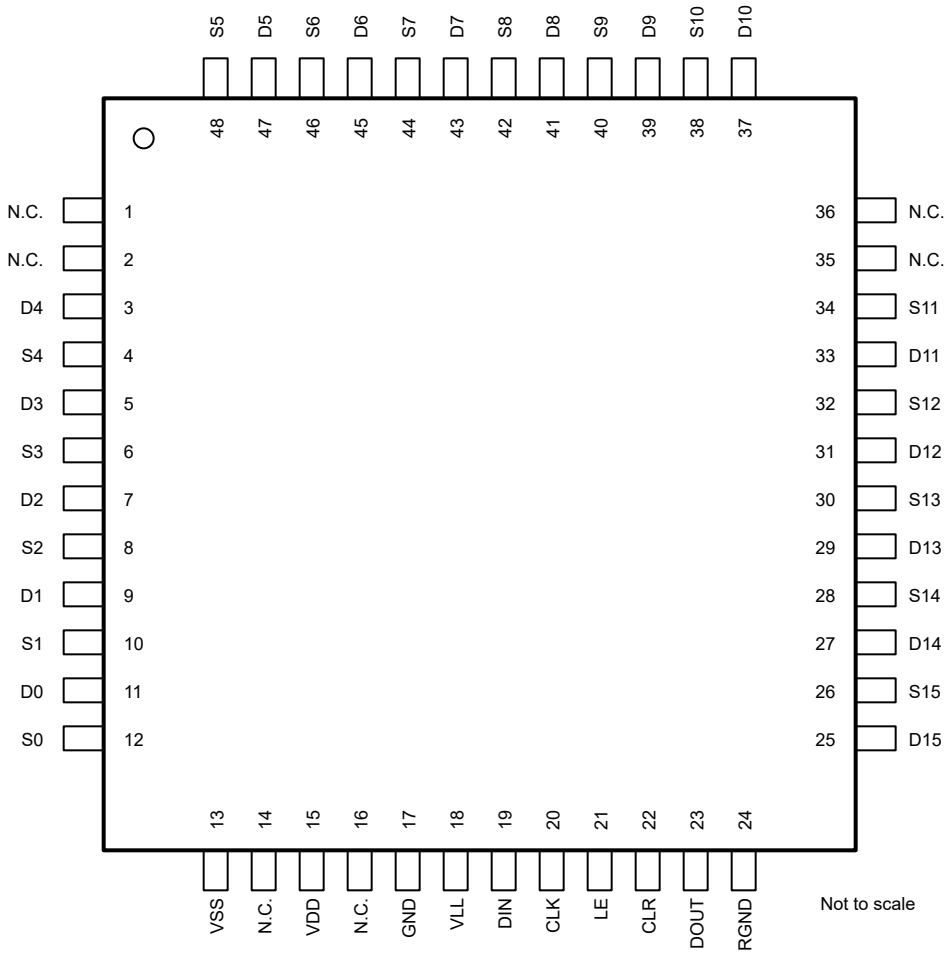


図 5-1. PT Package, 48-Pin LQFP (Top View)

表 5-1. Pin Functions

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
N.C.	1	—	No internal connection. Leave floating or connect to GND.
N.C.	2	—	No internal connection. Leave floating or connect to GND.
D4	3	I/O	Drain pin 4. Can be an input or an output.
S4	4	I/O	Source pin 4. Can be an input or an output.
D3	5	I/O	Drain pin 3. Can be an input or an output.
S3	6	I/O	Source pin 3. Can be an input or an output.
D2	7	I/O	Drain pin 2. Can be an input or an output.
S2	8	I/O	Source pin 2. Can be an input or an output.
D1	9	I/O	Drain pin 1. Can be an input or an output.
S1	10	I/O	Source pin 1. Can be an input or an output.
D0	11	I/O	Drain pin 0. Can be an input or an output.
S0	12	I/O	Source pin 0. Can be an input or an output.
V_{SS}	13	P	Negative power supply. This pin is the most negative power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND.
N.C.	14	—	No internal connection. Leave floating or connect to GND.

表 5-1. Pin Functions (続き)

PIN		TYPE[1]	DESCRIPTION
NAME	NO.		
V_{DD}	15	P	Positive power supply. This pin is the most positive power-supply potential. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND.
N.C.	16	—	No internal connection. Leave floating or connect to GND.
GND	17	P	Ground (0 V) reference.
V_{LL}	18	P	1.8 V – 5 V SPI power supply. For reliable operation, connect a decoupling capacitor ranging from 0.1 µF to 1 µF between V_{LL} and GND.
DIN	19	I	SPI (Daisy Chain) Data Input.
CLK	20	I	SPI (Daisy Chain) Clock Input.
$\overline{LE}$	21	I	Latch enable input, active low.
CLR	22	I	Latch clear input, active high.
DOUT	23	O	SPI (Daisy Chain) Data Output.
RGND	24	P	Bleed Resistor GND. Connect to ground (0 V) reference.
D15	25	I/O	Drain pin 15. Can be an input or an output.
S15	26	I/O	Source pin 15. Can be an input or an output.
D14	27	I/O	Drain pin 14. Can be an input or an output.
S14	28	I/O	Source pin 14. Can be an input or an output.
D13	29	I/O	Drain pin 13. Can be an input or an output.
S13	30	I/O	Source pin 13. Can be an input or an output.
D12	31	I/O	Drain pin 12. Can be an input or an output.
S12	32	I/O	Source pin 12. Can be an input or an output.
D11	33	I/O	Drain pin 11. Can be an input or an output.
S11	34	I/O	Source pin 11. Can be an input or an output.
N.C.	35	—	No internal connection. Leave floating or connect to GND.
N.C.	36	—	No internal connection. Leave floating or connect to GND.
D10	37	I/O	Drain pin 10. Can be an input or an output.
S10	38	I/O	Source pin 10. Can be an input or an output.
D9	39	I/O	Drain pin 9. Can be an input or an output.
S9	40	I/O	Source pin 9. Can be an input or an output.
D8	41	I/O	Drain pin 8. Can be an input or an output.
S8	42	I/O	Source pin 8. Can be an input or an output.
D7	43	I/O	Drain pin 7. Can be an input or an output.
S7	44	I/O	Source pin 7. Can be an input or an output.
D6	45	I/O	Drain pin 6. Can be an input or an output.
S6	46	I/O	Source pin 6. Can be an input or an output.
D5	47	I/O	Drain pin 5. Can be an input or an output.
S5	48	I/O	Source pin 5. Can be an input or an output.

(1) I = input, O = output, P = power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1) (2) (3)

		MIN	MAX	UNIT
V_{DD}–V_{SS}	Supply voltage		240	V
V_{DD}		–0.5	120	V
V_{SS}		–120	0.5	V
V_{LL}	SPI/Logic supply voltage	–0.5	6	V
V_L	Logic control pin voltage (DIN, DOUT, CLK, $\overline{LE}$, CLR)	–0.5	V_{LL}	V
I_L	Logic control pin current (DIN, DOUT, CLK, $\overline{LE}$, CLR)	–30	30	mA
V_S or V_D	Source or drain voltage (Sx, D)	V_{SS}	V_{DD}	V
I_{PK}	Analog Signal Peak Current/Channel		3	A
T_A	Ambient temperature	–40	125	°C
T_{stg}	Storage temperature	–65	150	°C
T_J	Junction temperature	–40	150	°C

(1) Operation outside the *Absolute Maximum Rating* may cause permanent device damage. *Absolute Maximum Rating* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Condition*. If used outside the *Recommended Operating Condition* but within the *Absolute Maximum Rating*, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±1000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC(1)		TMUX9616 PT (LQFP) 48 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	60.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	15.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	26.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	26.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
$V_{DD} – V_{SS}$	Power supply voltage differential	40	200	220	V
V_{DD}	Positive power supply voltage	20	100	110	V
V_{SS}	Negative power supply voltage	–110	–100	0	V
V_S or V_D	Signal path input/output voltage (source or drain pin) (Sx, D)(1)	V_{SS} + 10		V_{DD} – 10	V
V_{LL}	SPI/Logic power supply voltage	1.7		5.5	V
V_L	Logic control pin voltage (DIN, DOUT, CLK, $\overline{LE}$, CLR)	0		V_{LL}	V
V_{IH}	Logic control pin high-level input voltage (DIN, DOUT, CLK, $\overline{LE}$, CLR)	0.9 x V_{LL}			V
V_{IL}	Logic control pin low-level input voltage (DIN, DOUT, CLK, $\overline{LE}$, CLR)			0.1 x V_{LL}	V
T_A	Ambient temperature	–40		85	°C
T_J	Junction temperature	–40		125	°C

(1) V_S, V_D operation up to V_{SS} and V_{DD} is acceptable for recommended operation. $R_{ON\ FLAT}$ may increase when operating beyond V_{SS} + 10 V and V_{DD} – 10 V

6.5 Electrical Characteristics: TMUX9616

V_{DD} = +110 V, V_{SS} = –110 V, V_{LL} = 1.7 V - 5.5 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +110 V, V_{SS} = –110 V, V_{LL} = 3.3 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	mAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –100 V to +100 V I_D = –5 mA	25°C		14	19	Ω
			–40°C to +85°C			24	Ω
R_{ON}	On-resistance	V_S = –100 V to +100 V I_D = –200 mA	25°C		13	17	Ω
			–40°C to +85°C			19	Ω
ΔR_{ON}	On-resistance mis mAtch between channels	V_S = –100 V to +100 V I_D = –5 mA	25°C		2		%
			–40°C to +85°C			20	%
R_{ONL}	Large-Signal On-resistance	I_D = -1A	25°C		12		Ω
I_{SWPK}	Switch Peak Output Current	t_{PW} ≤100 ns, duty cycle ≤ 0.1%, current into source or drain.	25°C		3		A
I_{SWPK_DIODE}	Switch Peak Isolation Diode Current	t_{PW} ≤300 ns, duty cycle ≤ 2%	25°C		300		mA
V_{DC_OFFSET}	Switch DC Offset Voltage	Switch ON or OFF, R_L = No load (Integrated Bleed Resistors)	25°C		1.6		mV
			–40°C to +85°C	–60		30	mV
R_{INT}	Output Bleed Resistor	Source or Drain Output to GND, I_{RINT} = 20 µA. Switch is OFF	25°C	20	35	50	kΩ
$I_{S(OFF)}$	Source off leakage current(1)	V_{DD} = 110 V, V_{SS} = –110 V Switch state is off V_S = +100 V / –100 V V_D = –100 V / + 100 V	25°C		0.07		µA
			–40°C to +85°C	–4		4	µA
$I_{D(OFF)}$	Drain off leakage current(1)	V_{DD} = 110 V, V_{SS} = –110 V Switch state is off V_S = +100 V / –100 V V_D = –100 V / + 100 V	25°C		0.07		µA
			–40°C to +85°C	–4		4	µA
DIGITAL LOGIC (DIN, DOUT, CLK, $\overline{LE}$, CLR Pins)							
V_{IH}	Logic voltage high	V_{LL} = 1.7 V - 5.5 V	–40°C to +85°C	0.66 x V_{LL}			V
V_{IL}	Logic voltage low	V_{LL} = 1.7 V - 5.5 V	–40°C to +85°C			0.33 x V_{LL}	V
I_{IH}	Input leakage current		–40°C to +85°C			1.0	µA

6.5 Electrical Characteristics: TMUX9616 (続き)

V_{DD} = +110 V, V_{SS} = –110 V, V_{LL} = 1.7 V - 5.5 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +110 V, V_{SS} = –110 V, V_{LL} = 3.3 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	mAX	UNIT
I_{IL}	Input leakage current		–40°C to +85°C	–1.0			µA
C_{IN}	Logic input capacitance		–40°C to +85°C		3	10	pF
V_{OH}	Logic high output voltage	I_{SOURCE} = 1 mA	–40°C to +85°C	V_{LL} - 0.1			V
V_{OL}	Logic low output voltage	I_{SINK} = 1 mA, includes open drain /THERM pin	–40°C to +85°C			0.1	V
POWER SUPPLY							
I_{DDQ_OFF}	V_{DD} quiescent supply current	V_{DD} = 110 V, V_{SS} = –110 V I_D = -5 mA Switches OFF	25°C		15		µA
			–40°C to +85°C			23	µA
I_{DDQ_ON}	V_{DD} quiescent supply current	V_{DD} = 110 V, V_{SS} = –110 V I_D = -5 mA Switches ON	25°C		40		µA
			–40°C to +85°C			95	µA
I_{SSQ_OFF}	V_{SS} quiescent supply current	V_{DD} = 110 V, V_{SS} = –110 V I_D = -5 mA Switches OFF	25°C		10		µA
			–40°C to +85°C			65	µA
I_{SSQ_ON}	V_{SS} quiescent supply current	V_{DD} = 110 V, V_{SS} = –110 V I_D = -5 mA Switches ON	25°C		22		µA
			–40°C to +85°C			40	µA
I_{DD}	V_{DD} dynamic supply current	V_{DD} = 110 V, V_{SS} = –110 V All switches turned ON and OFF at f = 50 kHz	25°C		2.4		mA
			–40°C to +85°C			4	mA
I_{SS}	V_{SS} dynamic supply current	V_{DD} = 110 V, V_{SS} = –110 V All switches turned ON and OFF at f = 50 kHz	25°C		3.1		mA
			–40°C to +85°C			4	mA
I_{LLQ}	V_{LL} quiescent supply current		25°C		3.8		µA
			–40°C to +85°C			8	µA
I_{LL}	V_{LL} dynamic supply current	fCLK = 5 MHz, V_{LL} = 5 V	25°C		0.20		mA
			–40°C to +85°C			0.25	mA

(1) When V_S is positive, V_D is negative, or when V_S is negative, V_D is positive.

6.6 Switching Characteristics: TMUX9616

V_{DD} = +110 V, V_{SS} = –110 V, V_{LL} = 1.7V - 5.5 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +110 V, V_{SS} = –110 V, V_{LL} = 3.3 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{ON}	Turn-on time from enable	V_S = 100 V R_L = 10 kΩ	25°C		1.5		µs
			–40°C to +85°C			3	µs
t_{OFF}	Turn-off time from enable	V_S = 100 V R_L = 10 kΩ	25°C		0.8		µs
			–40°C to +85°C			2.5	µs
dV/dt_{MAX}	Maximum Analog Signal Slew Rate		–40°C to +85°C			20	V/ns
O_{ISO_TX}	Off-isolation TX	R_L = 50 Ω V_S = 0 V_{BIAS}, 10 V_{PP}, f = 5 MHz	25°C		–70		dB
O_{ISO_TX}	Off-isolation TX	R_L = 1 kΩ , C_L = 15 pF V_S = 0 V_{BIAS}, 10 V_{PP}, f = 5 MHz	25°C		–54		dB
O_{ISO_RX}	Off-isolation RX	R_L = 50 Ω V_D = 0 V_{BIAS}, 10 V_{PP}, f = 5 MHz	25°C		–70		dB

6.6 Switching Characteristics: TMUX9616 (続き)

V_{DD} = +110 V, V_{SS} = –110 V, V_{LL} = 1.7V - 5.5 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +110 V, V_{SS} = –110 V, V_{LL} = 3.3 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
O_{ISO_RX}	Off-isolation RX	R_L = 1 kΩ , C_L = 15 pF V_D = 0 V_{BIAS}, 10 V_{PP}, f = 5 MHz	25°C		–54		dB
X_{TALK_TX}	Crosstalk TX	R_L = 50 Ω V_S = 0 V_{BIAS}, 10 V_{PP}, f = 5 MHz	25°C		–75		dB
X_{TALK_RX}	Crosstalk RX	R_L = 50 Ω V_D = 0 V_{BIAS}, 10 V_{PP}, f = 5 MHz	25°C		–75		dB
BW_{SS_TX}	–3dB Bandwidth (Small Signal) TX	R_L = 50 Ω V_S = 0 V, Vpp = 200 mV	25°C		500		MHz
BW_{SS_RX}	–3dB Bandwidth (Small Signal) RX	R_L = 50 Ω V_D = 0 V, Vpp = 200 mV	25°C		500		MHz
HD2PC_LL_TX	Second Harmonic Distortion Pulse Cancellation (Large Signal) TX	V_{PP} = 200 V, V_S = 0 V R_L = 100 Ω || 100 pF f = 5 MHz, 2 Cycles, dv/dt: 7.1V/ns	25°C		54		dBc
$C_{S(OFF)}$	Source off capacitance	V_S = 0 V_{BIAS}, 100 mV_{PP}, f = 1 MHz	25°C		5		pF
$C_{D(OFF)}$	Drain off capacitance	V_D = 0 V_{BIAS}, 100 mV_{PP}, f = 1 MHz	25°C		5		pF
$C_{S(ON)}$, $C_{D(ON)}$	On capacitance	V_S/V_D = 0 V_{BIAS}, 100 mV_{PP}, f = 1 MHz	25°C		10		pF
V_{SPK}	Output voltage spike	R_{L_Source} = 1kΩ, R_{L_Drain} = 50Ω Enable and Disable Switch	25°C	-45		18	mV
V_{SPK}	Output voltage spike	R_{L_Source} = 1kΩ, R_{L_Drain} = 50Ω Enable and Disable Switch	–40°C to +85°C	-55		25	mV

6.7 Digital Timings: TMUX9616

V_{DD} = 4.5 V - 5.5 V, V_{LL} = 1.7V - 5.5 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = 5 V, V_{LL} = 3.3 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
f_{CLK_SPI}	SPI Clock Frequency (including daisy chain mode)	V_{LL} = 5 V	–40°C to +85°C			72	MHz
f_{CLK_SPI}	SPI Clock Frequency (including daisy chain mode)	V_{LL} = 3.3 V	–40°C to +85°C			54	MHz
f_{CLK_SPI}	SPI Clock Frequency (including daisy chain mode)	V_{LL} = 1.8 V	–40°C to +85°C			24	MHz
t_R, t_{F_SPI}	SPI Clock Rise and Fall Times		–40°C to +85°C			50	ns
t_{CLK_SPI}	CLK SPI Period	V_{LL} = 5 V	–40°C to +85°C	11.76			ns
t_{CLK_SPI}	CLK SPI Period	V_{LL} = 3.3 V	–40°C to +85°C	16.67			ns
t_{CLK_SPI}	CLK SPI Period	V_{LL} = 1.8 V	–40°C to +85°C	41.67			ns
$t_{CLK\_H\_SPI}$	CLK High Time SPI	V_{LL} = 5 V	–40°C to +85°C	5.29			ns
$t_{CLK\_H\_SPI}$	CLK High Time SPI	V_{LL} = 3.3 V	–40°C to +85°C	7.5			ns
$t_{CLK\_H\_SPI}$	CLK High Time SPI	V_{LL} = 1.8 V	–40°C to +85°C	18.75			ns
$t_{CLK\_L\_SPI}$	CLK Low Time SPI	V_{LL} = 5 V	–40°C to +85°C	5.29			ns
$t_{CLK\_L\_SPI}$	CLK Low Time SPI	V_{LL} = 3.3 V	–40°C to +85°C	7.5			ns
$t_{CLK\_L\_SPI}$	CLK Low Time SPI	V_{LL} = 1.8 V	–40°C to +85°C	18.75			ns
t_{SU_SPI}	Set Up Time Data to Clock SPI	V_{LL} = 5 V	–40°C to +85°C	1.0			ns
t_{SU_SPI}	Set Up Time Data to Clock SPI	V_{LL} = 3.3 V	–40°C to +85°C	2			ns
t_{SU_SPI}	Set Up Time Data to Clock SPI	V_{LL} = 1.8 V	–40°C to +85°C	5			ns

6.7 Digital Timings: TMUX9616 (続き)

V_{DD} = 4.5 V - 5.5 V, V_{LL} = 1.7V - 5.5 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = 5 V, V_{LL} = 3.3 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
t_{H_SPI}	Hold Time Data to Clock SPI	V_{LL} = 5 V	–40°C to +85°C	1.0			ns
t_{H_SPI}	Hold Time Data to Clock SPI	V_{LL} = 3.3 V	–40°C to +85°C	1.2			ns
t_{H_SPI}	Hold Time Data to Clock SPI	V_{LL} = 1.8 V	–40°C to +85°C	3			ns
t_{DO}	Clock Delay Time to Data Out	V_{LL} = 5 V	–40°C to +85°C	3		12.8	ns
t_{DO}	Clock Delay Time to Data Out	V_{LL} = 3.3 V	–40°C to +85°C	4		16.3	ns
t_{DO}	Clock Delay Time to Data Out	V_{LL} = 1.8 V	–40°C to +85°C	7		34	ns
$t_{S/LE}$	Set Up Time Before $\overline{LE}$ Rises		–40°C to +85°C	25			ns
$t_{W/LE}$	Time Width of $\overline{LE}$		–40°C to +85°C	12			ns
t_{WCLR}	Time Width of CLR		–40°C to +85°C	55			ns

6.8 Timing Diagrams

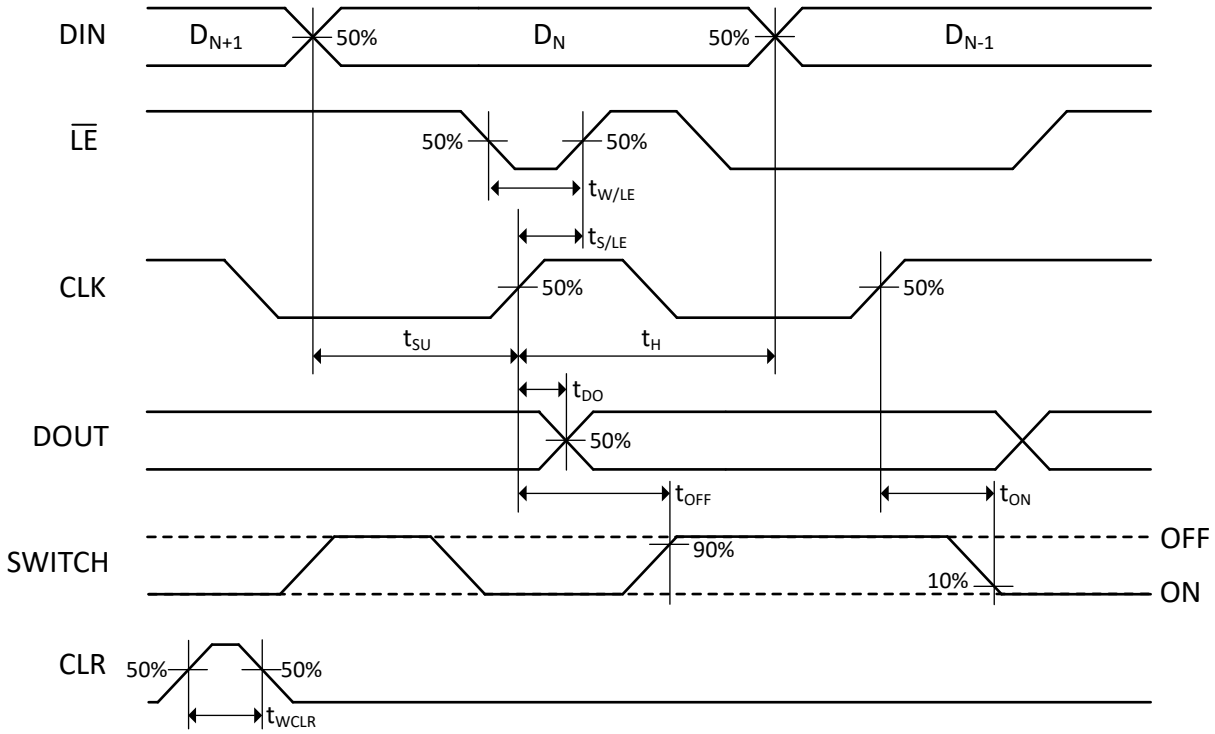


図 6-1. Logic Timing Diagram

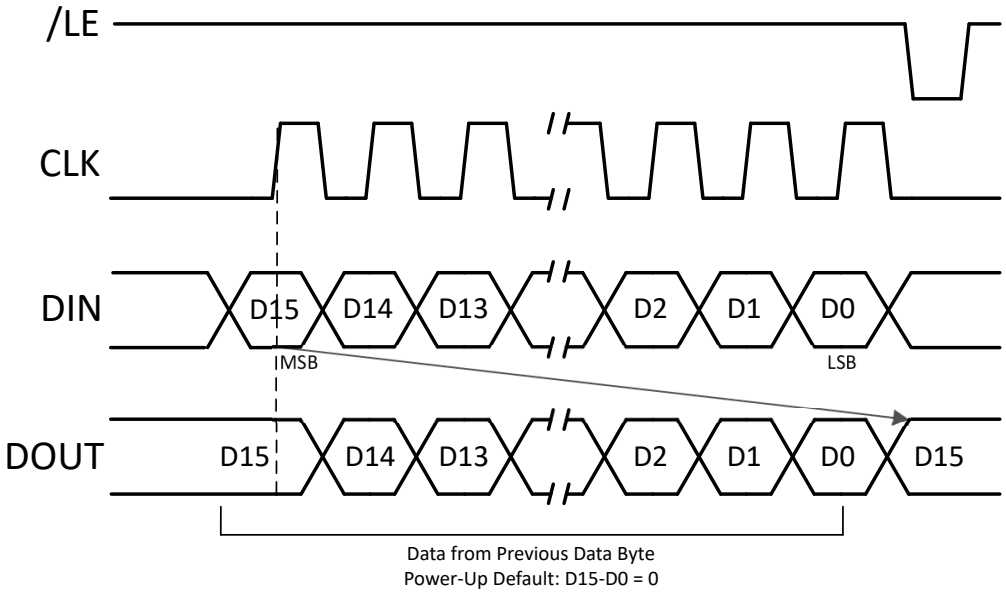


図 6-2. Latch Enable Timing Diagram

6.9 Typical Characteristics

at T_A = 25°C, V_{DD} = 110 V, V_{SS} = –110 V, and V_{LL} = 3.3V (unless otherwise noted)

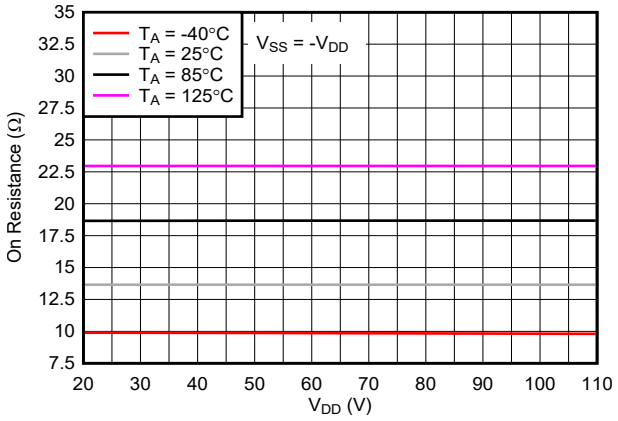


図 6-3. On-Resistance vs V_{DD}/V_{SS} Supply Voltage

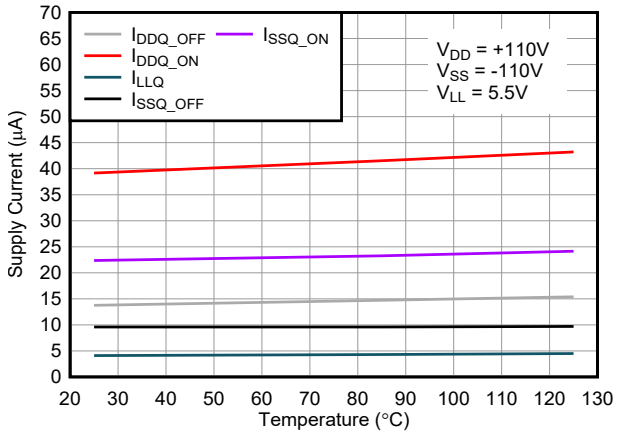


図 6-4. Supply Quiescent Current vs Temperature

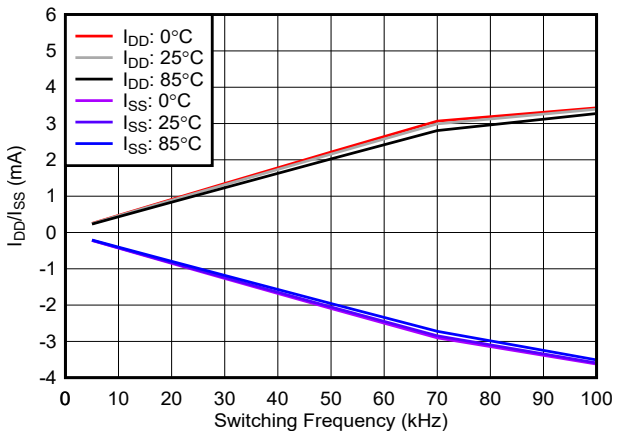


図 6-5. High Voltage Supply Current vs Switching Frequency

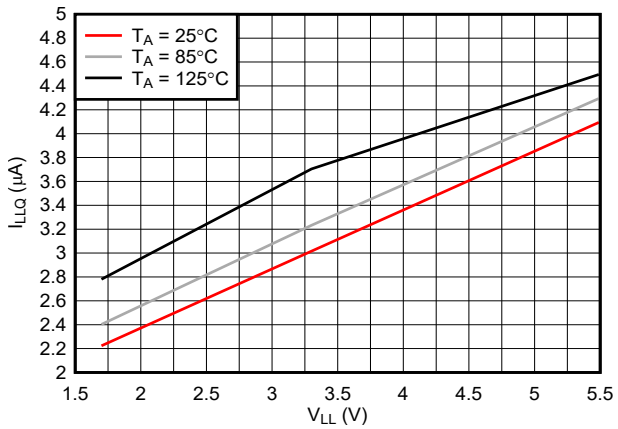


図 6-6. I_{LLQ} vs V_{LL}

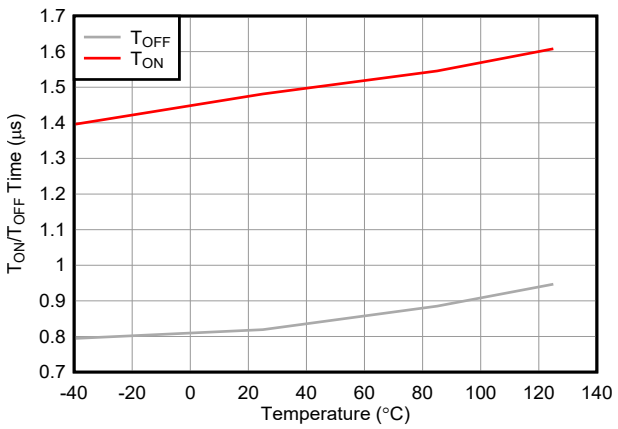


図 6-7. Turn ON and Turn OFF Time vs Temperature

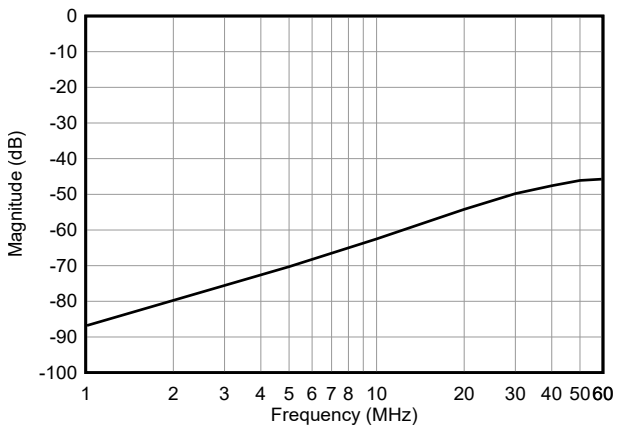


図 6-8. Large Signal Off Isolation vs Frequency

6.9 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 110 V, V_{SS} = –110 V, and V_{LL} = 3.3V (unless otherwise noted)

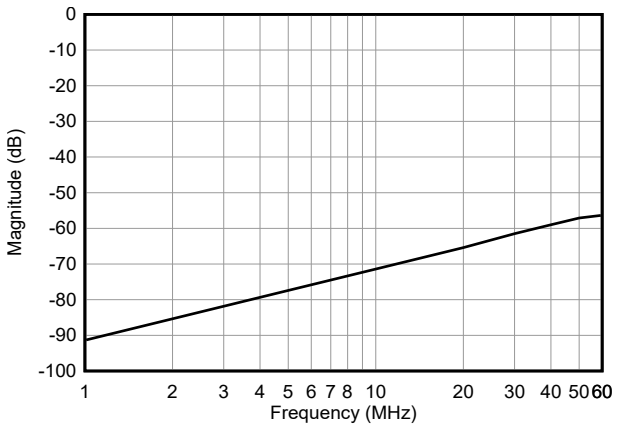


図 6-9. Large Signal Crosstalk vs Frequency

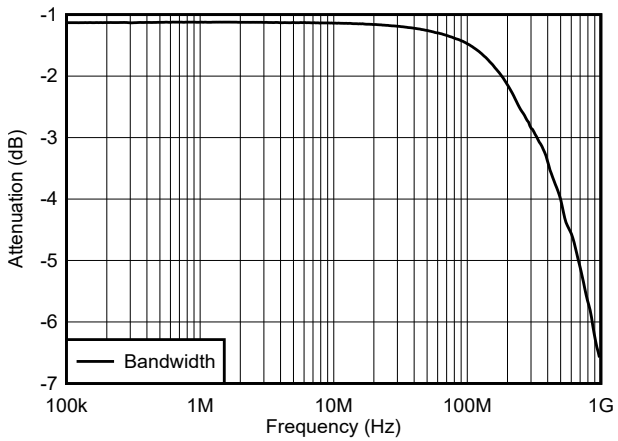


図 6-10. Small Signal Insertion Loss vs Frequency

7 Parameter Measurement Information

7.1 Off-Leakage Current

There are two types of leakage currents associated with a switch during the off state:

1. Source off-leakage current $I_{S(OFF)}$: the leakage current flowing into or out of the source pin when the switch is off.
2. Drain off-leakage current $I_{D(OFF)}$: the leakage current flowing into or out of the drain pin when the switch is off.

The setup used to measure both off-leakage currents is shown in 図 7-1.

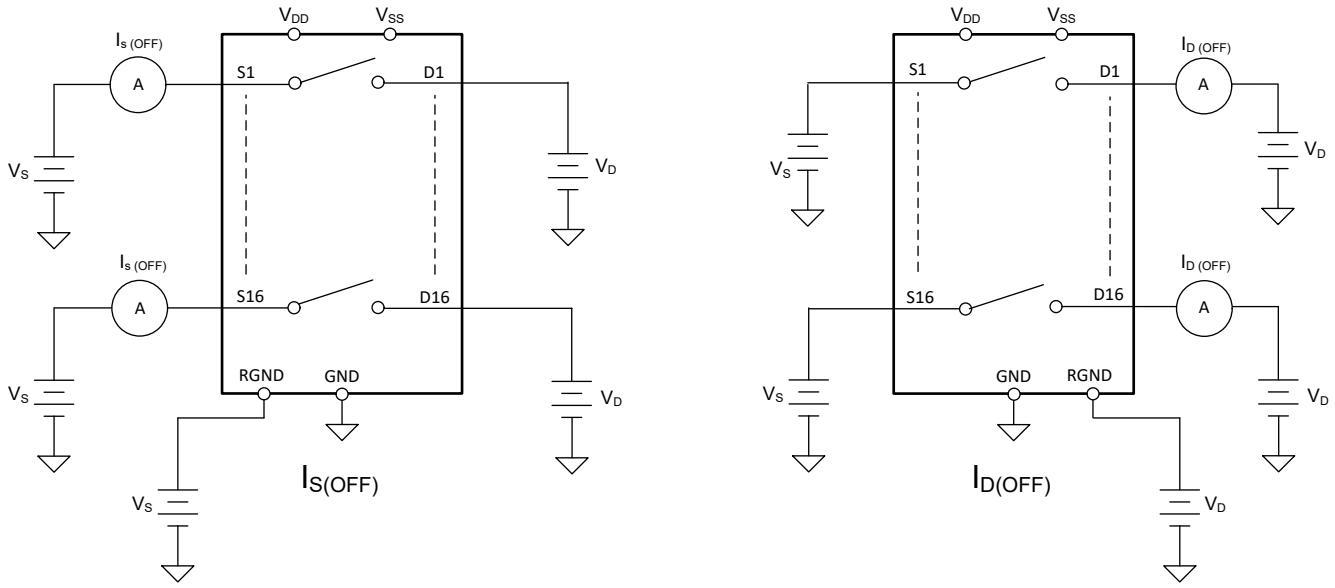


図 7-1. Off-Leakage Measurement Setup

7.2 Device Turn On/Off Time

Turn-off time (t_{OFF}) is defined as the time taken by the Sx pin of the TMUX9616 to rise to a 90% final value after the CLK signal has risen to 50% of its final value. Turn-on time (t_{ON}) is defined as the time taken by the output of the TMUX9616 to fall to a 10% initial value after the CLK signal has risen) to 50% of its final value. 図 7-2 shows the setup used to measure t_{ON} and t_{OFF}.

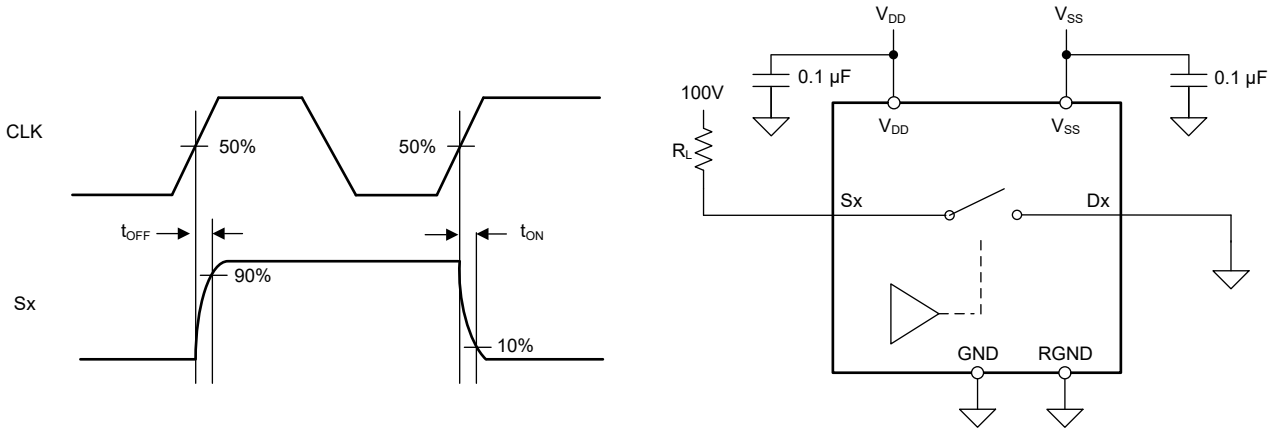
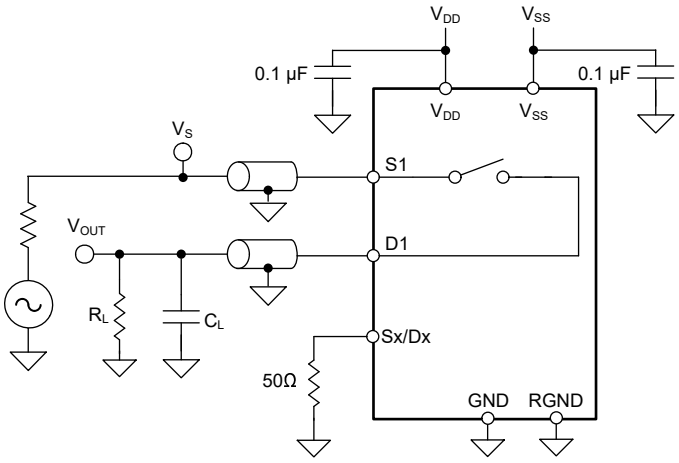


図 7-2. Turn-on/off Measurement Setup

7.3 Off Isolation

Off isolation is defined as the ratio of the signal at the drain pin (Dx) of the device when a signal is applied to the source pin (Sx) of an off-channel. 図 7-3 shows the setup used to measure off isolation.

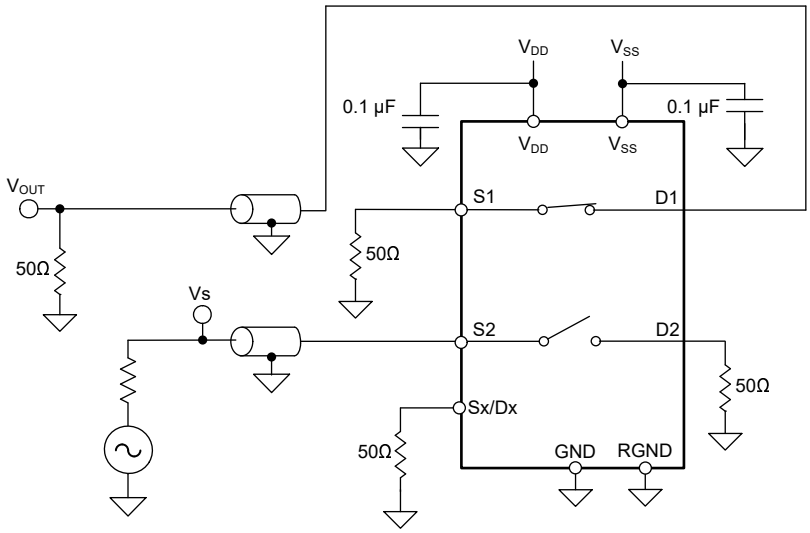


$$O_{ISO} = 20 * Log(\frac{V_{OUT}}{V_S})$$

図 7-3. Off Isolation Measurement Setup

7.4 Inter-Channel Crosstalk

Crosstalk (X_{TALK}) is defined as the ratio of the output signal at the Dx pin of an on-channel to the input signal at the Sx pin of an off-channel, as shown in 図 7-4.



$$X_{TALK} = 20 * Log(\frac{V_{OUT}}{V_S})$$

図 7-4. Crosstalk Measurement Setup

7.5 Output Voltage Spike

Output Voltage Spike (V_{SPIKE} or V_{SPK}) is the magnitude of the transient output voltage spike which occurs on an input or output pin when turning the switch channel ON or OFF. When measuring V_{SPK} on the Dx pin, 50 Ω is placed on the Dx pin and 1 kΩ is placed on the Sx pin. Likewise, when measuring V_{SPK} on the Sx pin, 50 Ω is placed on the Sx pin and 1 kΩ is placed on the Dx pin. 図 7-5 shows the setup used to measure the V_{SPK} of the switch.

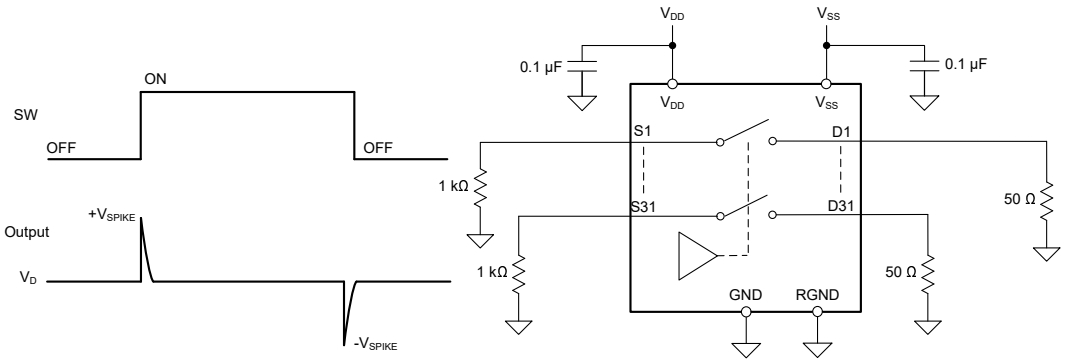


図 7-5. V_{SPK} Measurement Setup

7.6 Switch DC Offset Voltage

The switch DC offset voltage (V_{DC_OFFSET}) is the DC offset voltage that can be present on an Sx or Dx pin when the switch channel is ON or OFF. 図 7-6 shows the setup used to measure the V_{DC_OFFSET} voltage of the device.

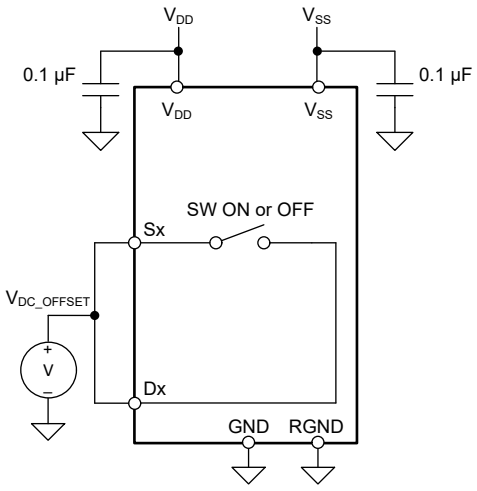


図 7-6. V_{DC_OFFSET} Measurement Setup

7.7 Isolation Diode Current

The switch peak isolation diode current (I_{SWPK_DIODE}) is the maximum peak current the isolation diodes on each channel can sustain. 図 7-7 shows the set-up used to measure I_{SWPK_DIODE}

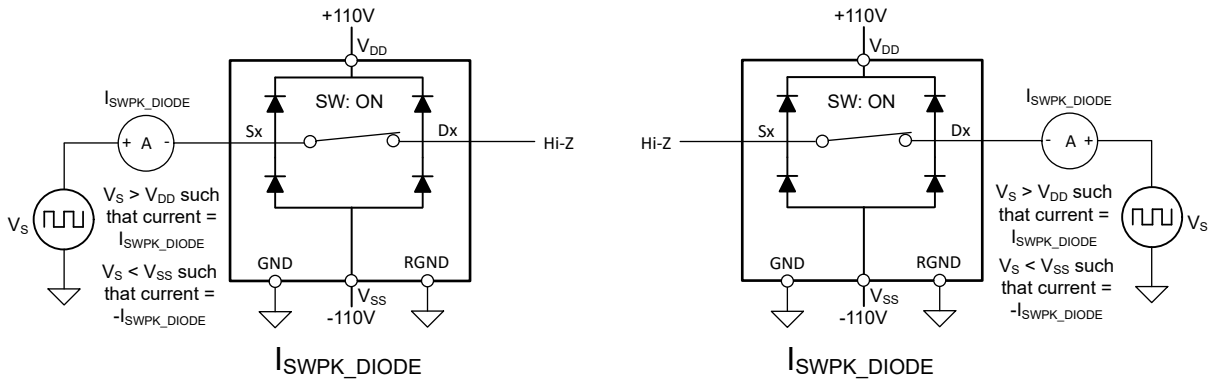


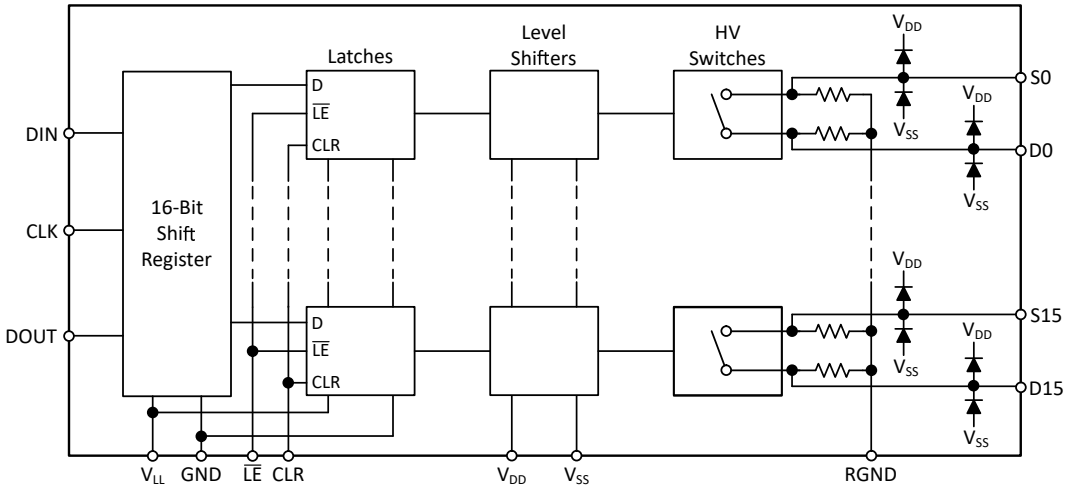
図 7-7. Isolation Diode Current Measurement Setup

8 Detailed Description

8.1 Overview

The TMUX9616 is a 16-channel low resistance, low capacitance high-voltage analog switch integrated circuit (IC) with latch-up immunity. Each device has 16 independently selectable 1:1, single-pole, single-throw (SPST) switch channels. The device works well with dual supplies up to ±110 V. Asymmetric supply biasing is also supported within the recommended supply range. The TMUX9616 supports bidirectional analog and digital signals on the source (Sx) and drain (Dx) pins ranging from V_{SS} to V_{DD}. TMUX9616 also integrates bleed resistors on its source (Sx) and drain (Dx) pins to discharge capacitive loads, like piezoelectric transducers.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Wide Input Signal Range (up to ±110 V, 220 V_{PP})

TMUX9616 can pass a wide input signal range, up to V_{DD}/V_{SS} of ±110 V (220 V_{PP}), which is very beneficial as many high voltage transmitters are designed to transmit up to ±100 V. The extra headroom above ±100 V that TMUX9616 provides is critical for operating the high voltage transmitters in systems up to ±100 V for a few reasons. First, with high voltage supply multiplexers (±110 V V_{DD}/V_{SS}), typically as the V_S pin approaches V_{DD} (V_S > V_{DD} - (5 V to 10 V)), the R_{ON} of the switch starts to rapidly increase. With a large change in R_{ON} when V_S is near V_{DD}, this can cause the harmonic distortion performance of the system to degrade (HD2PC, so fourth). Setting the high voltage supplies 10 V above the pulser operating voltage, allows V_S to stay ≤ (V_{DD} - 10 V), keeping the switch in its flat R_{ON} operating region for the intended TX signal, and therefore greatly improving system harmonic distortion performance.

Second, various system parasitics (or even intentionally added tuning inductors) and transmission line reflections in the system (due to cables, long PCB traces, and so forth) can cause some temporary peaking of the maximum voltage that the TMUX9616 receives above the ±100 V maximum output voltage of the high voltage transmitter. Having the high voltage multiplexer in the system have voltage tolerance above the high voltage transmitter (up to VDD = +110 V and VSS = -110 V per *Recommended Operating Conditions*) is crucial for being able to run the system at the high voltage transmitters maximum voltage output capability.

8.3.2 Bidirectional Operation

The devices conduct equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each signal path has very similar characteristics in both directions.

8.3.3 Device Digital Logic Control

The TMUX9616 is controlled by a SPI interface to a 16-bit shift register, and a CLR pin. The SPI interface can run at speeds up to 72 MHz. It can also be run with 1.8 V – 5 V logic levels (set by logic supply V_{LL}). The DIN pin will take in the data for the 16-bit register, and CLK will take in the clock signal. Data is shifted in on the DIN pin with the most-significant bit (MSB) first. After writing in 16 bits into the shift register using DIN and CLK, $\overline{LE}$ is then used to latch the state of the switches in the shift register to change the state of the switches in analog. The switches go to a state of retaining their present state on the rising edge of the $\overline{LE}$ pin. When $\overline{LE}$ is high, updates to the shift register does not change the condition of the 16 switches until $\overline{LE}$ is made low again. When $\overline{LE}$ is low, the shift register data flows through the latch and the condition of the 16 switches will be changed as the shift register is updated.

TMUX9616 16-bit shift register can be used in daisy chain mode. This is done by connecting the DOUT pin of the first TMUX9616 device to the DIN pin of the next TMUX9616 device in the chain. All TMUX9616 in the daisy chain will share the same source CLK signal (the CLK pin of each device in the daisy chain will be shorted together). DOUT is the data output pin of the 16th bit of the shift register, which is the data on DIN clock shifted by 16 clock cycles. The $\overline{LE}$ pin of each device in the chain will be shorted together, using the same $\overline{LE}$ source.

Assuming N number of TMUX9616 devices in the daisy chain, the standard method of writing to the shift registers is to write 16 * N bits of data, corresponding to each switch in the daisy chain, with $\overline{LE}$ set high. Once all 16 * N bits are written into the shift register, $\overline{LE}$ is pulsed low for at least $t_{W\overline{LE}}$ to update the condition of the 16 * N switches in the daisy chain to the new state recorded in the shift register. Then $\overline{LE}$ is set high again so that the state of the switches will not change until the next 16 * N bits are written into the shift register (and $\overline{LE}$ is pulsed low again following the 16 * N bit write).

The CLR pin, when asserted high, causes all the 16 switches in TMUX9616 to turn OFF, regardless of the state of the bits in the 16-bit shift register. When the CLR pin asserted low, the switches will then use the shift register again to set its values.

For more details on programming the shift register and the logic state of each switch, see the *Device Logic Table* section. For more details of programming the shift register with the correct digital timings, see the *Timing Diagrams* section and the *Digital Timings* table. For more details on the maximum speeds obtainable in daisy chain mode depending on device configuration, see the *Switching Characteristics* table. 図 8-1 shows more details on how to connect the TMUX9616 device's in daisy chain mode.

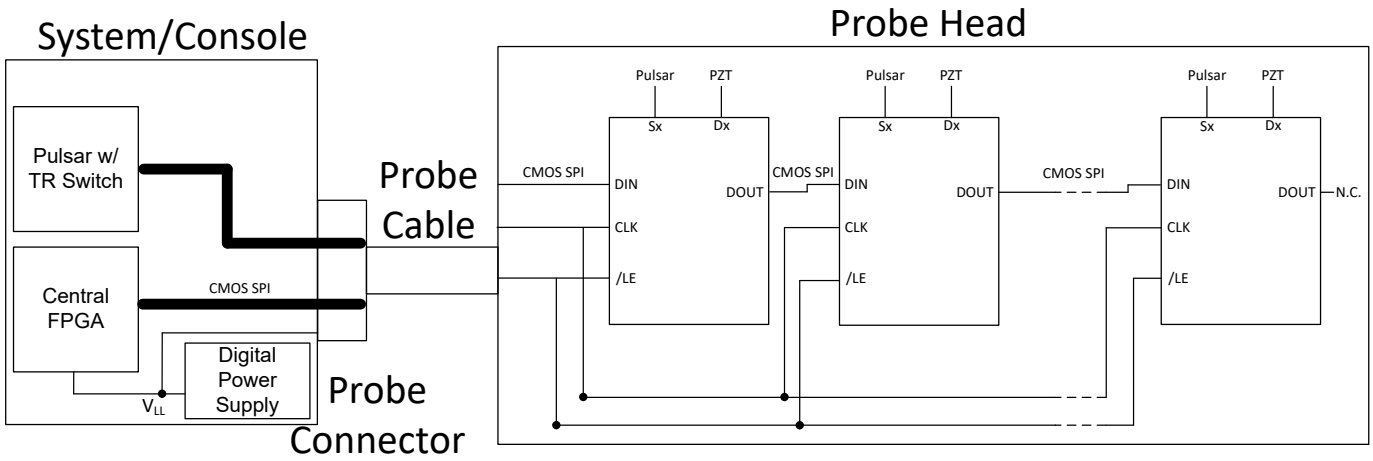


図 8-1. Daisy Chain System Block Diagram

8.3.4 Latch-Up Immunity by Device Construction

Latch-up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The latch-up condition typically requires a power cycle to eliminate the low impedance path.

The TMUX9616 is constructed on silicon on insulator (SOI) based process where an oxide layer is added between the PMOS and NMOS transistor of each CMOS switch to prevent parasitic structures from forming. The oxide layer is also known as an insulating trench and prevents triggering of latch up events due to overvoltage, fast voltage slew rates, and current injections. The latch-up immunity feature allows the TMUX9616 to be used in harsh environments. For more information on latch-up immunity, refer to *Using Latch Up Immune Multiplexers to Help Improve System Reliability*.

8.4 Device Functional Modes

8.4.1 Normal Mode

In normal mode operation, TMUX9616 is controlled by its digital logic, which is detailed in the *Device Digital Logic Control* section. In normal mode, switches are available to be used to pass high voltage ±110 V signals (signals from V_{SS} to V_{DD}). More details of the device operation in normal mode can be found in the *Feature Description* and *Device Logic Table* sections.

8.4.2 Device Power Up

TMUX9616 will be powered up once V_{LL}, V_{DD}, and V_{SS} reach their final voltage. V_{LL}, V_{DD}, and V_{SS} can be powered up in any order (there is no power sequencing requirement). The device digital logic control will not receive updates until both V_{LL}, V_{DD}, and V_{SS} are powered up. Additionally, after V_{LL}, V_{DD}, and V_{SS} are powered up, the system FPGA or controller should wait at least 500 µs until writing to the device digital logic control. For more details on the device digital logic control, see the *Device Digital Logic Control* section.

On power-up, all 16 switches in TMUX9616 will be in the OFF state.

8.5 Device Logic Table

表 8-1. Device Logic Table(1)(2)(3)(4)(5)(6)(7)

Inputs						Outputs			
D0	D1	...	D15	$\overline{LE}$	CLR	SW0	SW1	...	SW15
0	—	...	—	L	L	OFF	—	...	—
1	—		—	L	L	ON	—		—
—	0		—	L	L	—	OFF		—
—	1		—	L	L	—	ON		—
—	—		—	L	L	—	—		—
—	—		—	L	L	—	—		—
—	—		0	L	L	—	—		OFF
—	—		1	L	L	—	—		ON
X	X	X	X	H	L	HOLD PREVIOUS STATE			
X	X	X	X	X	H	OFF	OFF	OFF	OFF

(1) All 16 switches operate independently.
(2) Serial data is clocked in on the rising edge of CLK. Data is shifted in on the DIN pin with the most-significant bit (MSB) first.
(3) The switches go to a state of retaining their present state on the rising edge of the $\overline{LE}$ pin. Once the $\overline{LE}$ pin is high, updates to the shift register no longer change the condition of the 16 switches until the $\overline{LE}$ pin is made low again. When the $\overline{LE}$ is low, the shift register data flows through the latch.
(4) Shift register clocking has no effect on the switch states if the $\overline{LE}$ pin is high.
(5) DOUT is the data output pin of the 16 bit shift register for daisy chaining multiple muxes together. It is the data of the DIN clock shifted by the 16 clock cycles.
(6) The CLR input overrides all other inputs.
(7) While $\overline{LE}$ = H or CLR = H, if the CLK pin still receiving a valid clock signal, DIN will still function and input data into the shift register, and DOUT will still output the contents on the shift register. However, while $\overline{LE}$ = H or CLR = H, the state of the analog switches is no longer dependent on the contents of the shift register, but rather takes the state per this logic table.

9 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TMUX9616 is a 16-channel low harmonic distortion, low resistance, low capacitance, high-voltage analog switch integrated circuit (IC) with latch-up immunity. Each device has 16 independently selectable 1:1, single-pole, single-throw (SPST) switch channels. The device can support high voltage supplies and signals up to ±110V. It comes in popular, pin-to-pin (P2P) 48-pin QFP package for 16CH SPST multiplexers. This makes TMUX9616 a great replacement in an existing design with fixed foot print, where improvement is needed on harmonic distortion performance of the system. Also, TMUX9616 a great solution any time the application may require a leaded package.

9.2 Typical Application

図 9-1 shows a multiplexer configuration that is found in a variety of ultrasound applications. Two TX7516 are used to provide 32 TX/RX channels, and 8x TMUX9616 are used to multiplex the 32 TX/RX channels to 128 piezoelectric (PZT) elements, making a 4:1 multiplexer configuration. An FPGA controls both the TX7516 and TMUX9616 using SPI.

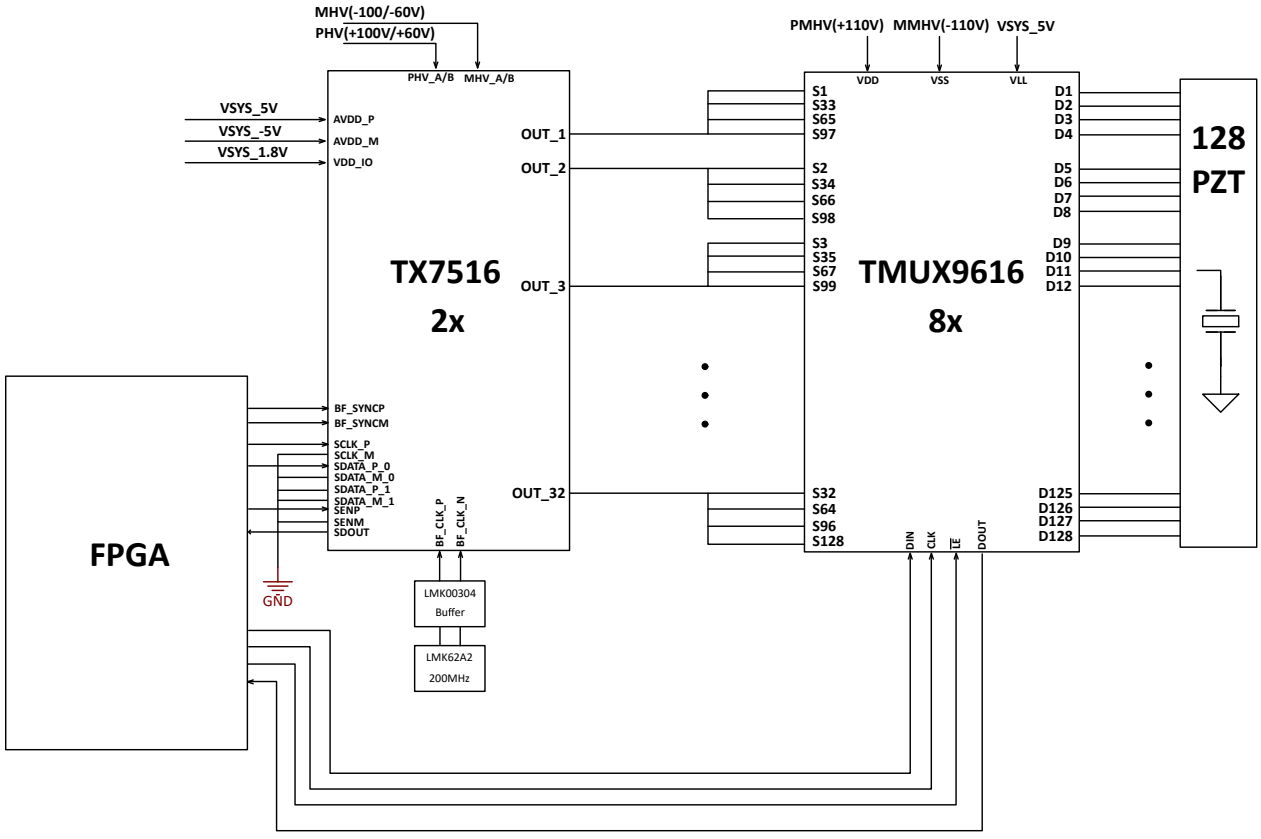

図 9-1. TMUX9616 Application Schematic

9.2.1 Design Requirements

表 9-1. Design Parameters

PARAMETERS	VALUES
Positive analog supply (V_{DD}) TMUX9616	+110 V
Negative analog supply (V_{SS}) TMUX9616	-110 V
Logic supply (V_{LL}) TMUX9616	5 V
Pulser supply A (PHV_A/MHV_A) TX7516	+100 V/-100 V
Pulser supply B (PHV_B/MHV_B) TX7516	+60 V/-60 V
Analog signal support TMUX9616	±110 V
Maximum SPI speed supported TMUX9616	72 MHz
System level HD2PC target requirement	≥40 dB
System level HD1PC target requirement	≥40 dB
System test load	100 Ω || 100 pF

9.2.2 Detailed Design Procedure

図 9-1 shows a system configuration found in a variety of ultrasound applications. The TX7516 has two supply rails A (PHV_A/MHV_A) and B (PHV_B/MHV_B) that enable switching between multiple TX levels for 3-Level mode, and also enable transmitting 5-Level mode. Each supply channel (A or B) can both provide up to 2 A output current, and the two channels can be operated in parallel for a 4 A output mode. Two TX7516 are used to provide 32 TX channels, and eight TMUX9616 are used to multiplex the 32 TX channels to the 128 PZT elements (4:1 mux configuration). Supply A will transmit at ±100 V, and supply B will transmit ±60 V.

A very important system level requirement for good image quality is to target ≥40 dB for both HD2PC and HD1PC (harmonic distortion pulse cancellation). The entire system, including both the TX7516 pulser and TMUX9616 mux, must output a TX signal at ≥40 dB. TX7516 is a pulser with excellent output signal performance, performing higher than the ≥40 dB target. Additionally, TMUX9616 is an excellent multiplexer, having minimal and in many cases negligible impact on the HD2PC/HD1PC performance, keeping the output signal performance high for good image quality while also allowing to increase the number of PZT elements in the system without increasing the number of pulser TX channels.

An example system use case using the TX7516EVM with the TMUX9616 EVM was performed first with the TMUX9616 removed and replaced with a pass through connection. Second, the same system level use case was performed by removing the pass through connection and adding the TMUX9616 back into the signal path. For a ±100 V pulser supply in this system use case, transmitting in 3-level mode with 5 cycles at 5 MHz with a 100 Ω || 100 pF test load, TX7516 alone performed with an HD2PC of 49 dB and an HD1PC of 67 dB. For the same use case, adding in TMUX9616 into the signal path, the system performed with an HD2PC of 54 dB and an HD1PC of 60 dB. Therefore, in this use case the TMUX9616 has negligible impact on the system level HD2PC/HD1PC performance; TX7516, by itself, and TX7516 with TMUX9616 in its signal path perform at an HD2PC/HD1PC performance level well above 40 dB.

For more details on the HD2PC and HD1PC performance of TX7516 and TMUX9616 across multiple supply levels, see the *Application Curves*. Additionally, some example use cases are plotted in the time domain and frequency domain for observation.

9.2.3 Application Curves

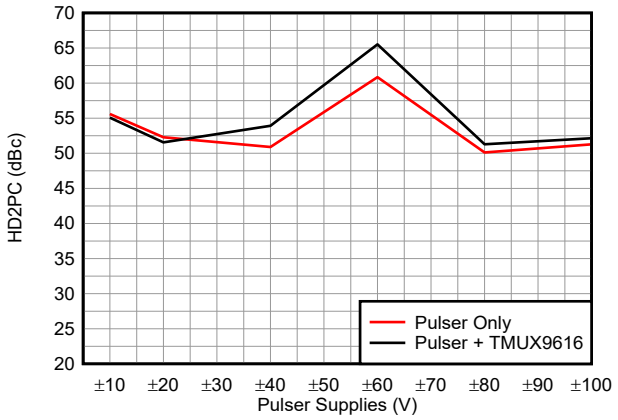

図 9-2. HD2PC TMUX9616 Input, 5 MHz, 5 Cycles, 100 Ω || 100 pF Load

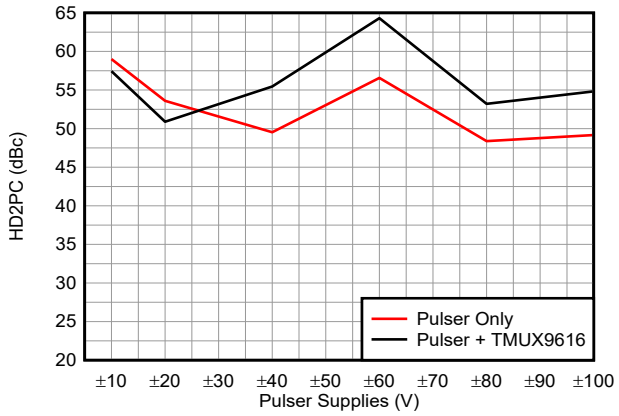

図 9-3. HD2PC TMUX9616 Output, 5 MHz, 5 Cycles, 100 Ω || 100 pF Load

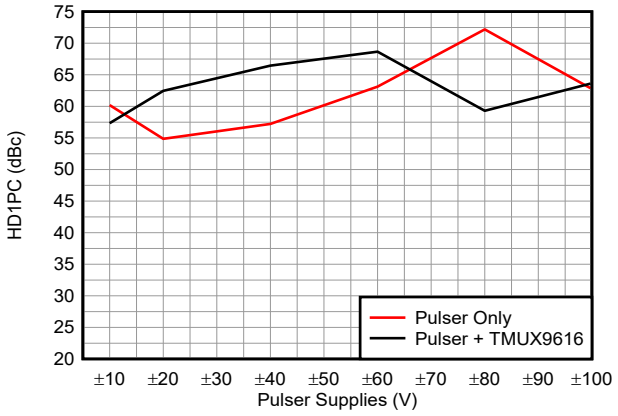

図 9-4. HD1PC TMUX9616 Input, 5 MHz, 5 Cycles, 100 Ω || 100 pF Load

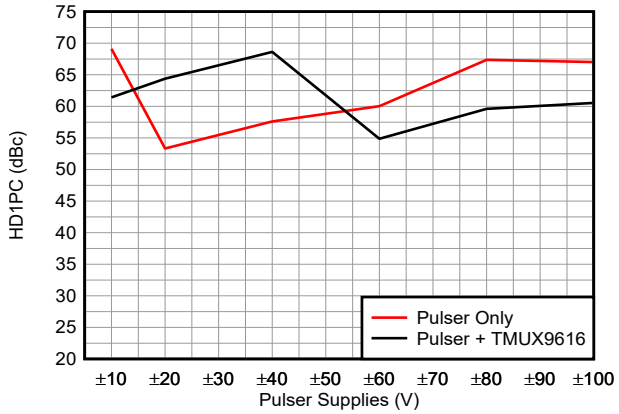

図 9-5. HD1PC TMUX9616 Output, 5 MHz, 5 Cycles, 100 Ω || 100 pF Load

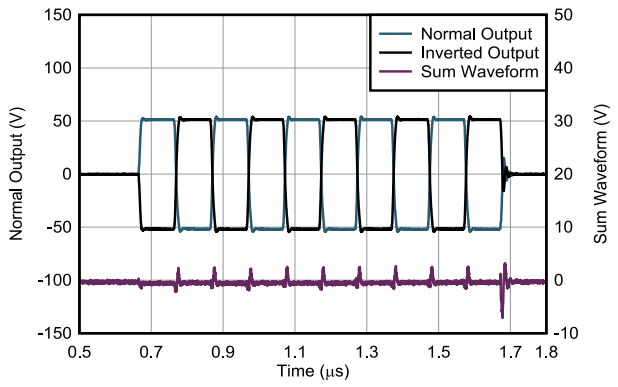

図 9-6. Pulser Only, Mux Input Side, ±60 V Pulser Supplies, 5 MHz, 5 Cycles, 100 Ω || 100 pF Load

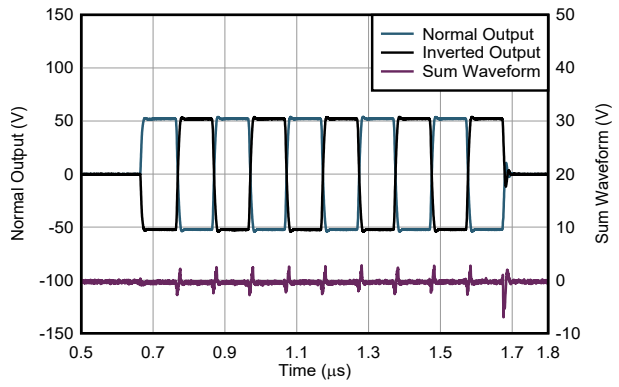

図 9-7. Pulser + TMUX9616, Mux Input Side, ±60 V Pulser Supplies, 5 MHz, 5 Cycles, 100 Ω || 100 pF Load

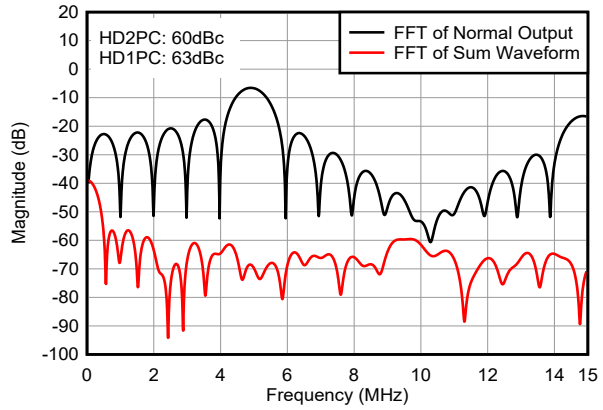

図 9-8. Pulser Only, Mux Input Side, ±60 V Pulser Supplies, 5 MHz, 5 Cycles, 100 Ω || 100 pF Load

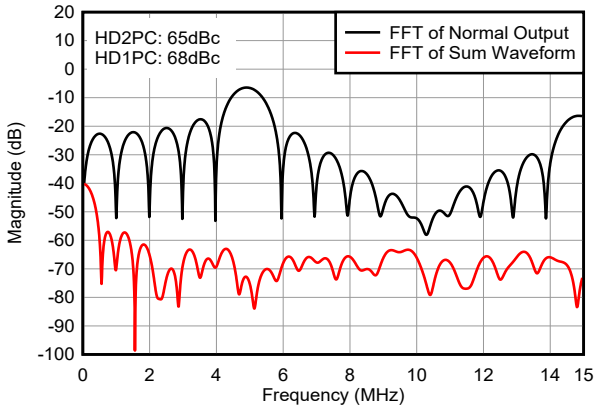

図 9-9. Pulser + TMUX9616, Mux Input Side, ±60 V Pulser Supplies, 5 MHz, 5 Cycles, 100 Ω || 100 pF Load

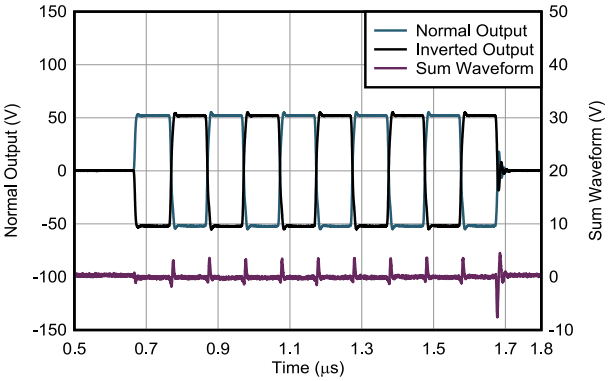

図 9-10. Pulser Only, Mux Output Side, ±60 V Pulser Supplies, 5 MHz, 5 Cycles, 100 Ω || 100 pF Load

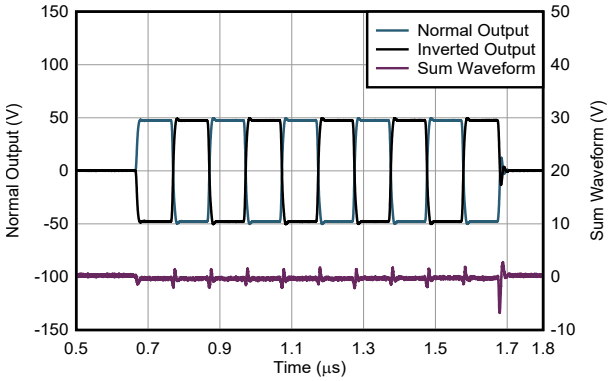

図 9-11. Pulser + TMUX9616, Mux Output Side, ±60 V Pulser Supplies, 5 MHz, 5 Cycles, 100 Ω || 100 pF Load

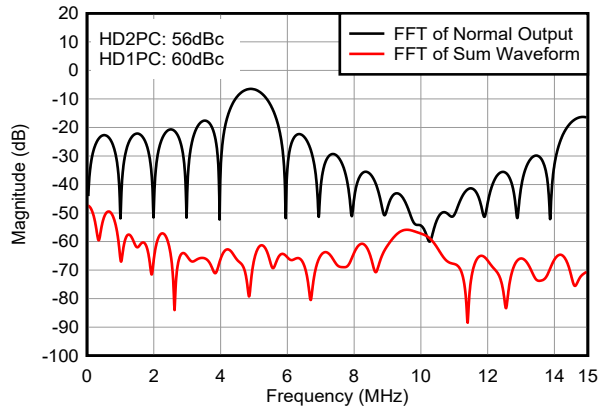

図 9-12. Pulser Only, Mux Output Side, ±60 V Pulser Supplies, 5 MHz, 5 Cycles, 100 Ω || 100 pF Load

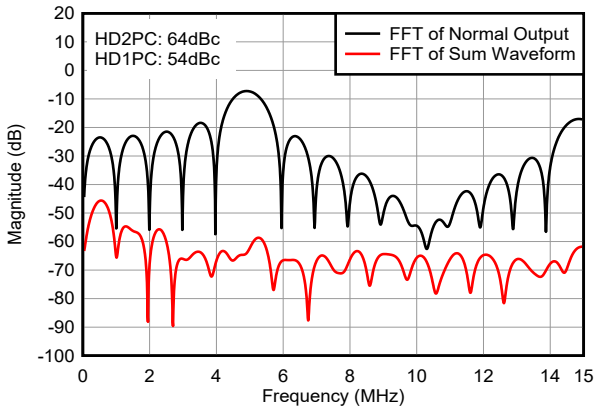

図 9-13. Pulser + TMUX9616, Mux Output Side, ±60 V Pulser Supplies, 5 MHz, 5 Cycles, 100 Ω || 100 pF Load

9.3 Power Supply Recommendations

The TMUX9616 supports a wide signal range of ±110 V (signals from V_{SS} to V_{DD}). It is recommended to use a supply decoupling capacitor of at least 0.1 µF at the V_{DD} pin to ground and at the V_{SS} pin to ground. It is also recommended to use a supply decoupling capacitor for the logic supply V_{LL} of at least 0.1 µF (V_{LL} pin to ground). The TMUX9616 EVM uses 1 µF capacitor in parallel with a 0.1 µF capacitor for both the V_{DD}, V_{SS}, and V_{LL} supply pins.

There are no specific power sequencing requirements between the V_{DD}, V_{SS}, and V_{LL} supplies.

9.4 Layout

9.4.1 Layout Guidelines

The following image shows an example of a PCB layout with the TMUX9616. Some key considerations are as follows:

- For reliable operation, connect at least one decoupling capacitor of at least 0.1 µF of capacitance between V_{DD} and V_{SS} to GND. The TMUX9616 EVM uses a 0.1 µF in parallel with a 1 µF capacitor. It is recommended to place the lowest value capacitor as close to the pin as possible. Ensure that the capacitor voltage rating is sufficient for the supply voltage.
- Keep the input lines as short as possible.
- Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

9.4.2 Layout Example

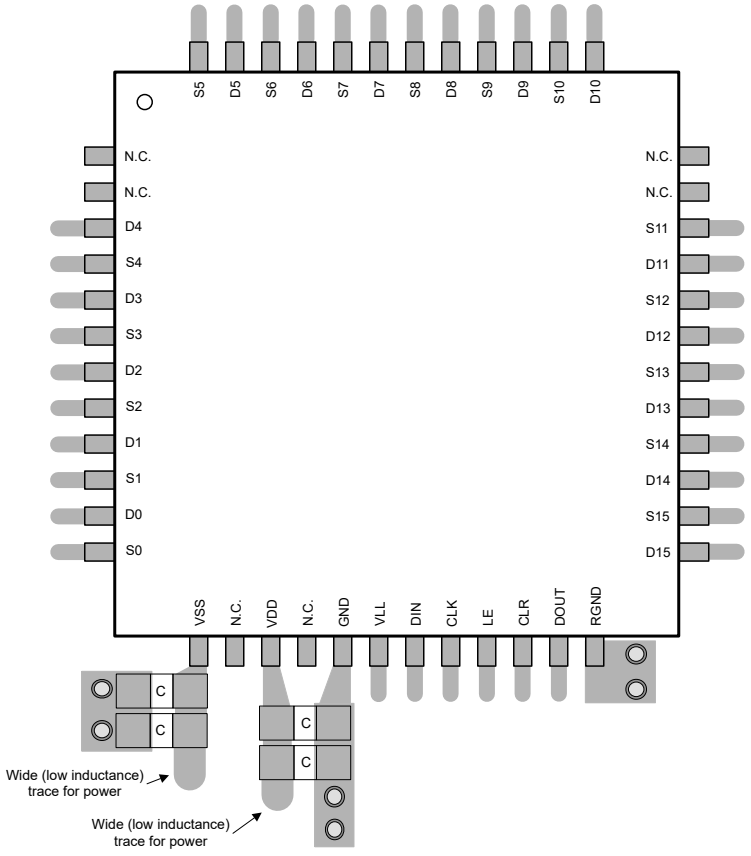

図 9-14. TMUX9616 Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, *Using Latch Up Immune Multiplexers to Help Improve System Reliability*

10.2 ドキュメントの更新通知を受け取る方法

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10.3 サポート・リソース

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10.5 静電気放電に関する注意事項

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10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUX9616PTR	ACTIVE	LQFP	PT	48	1000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 85	TM9616	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

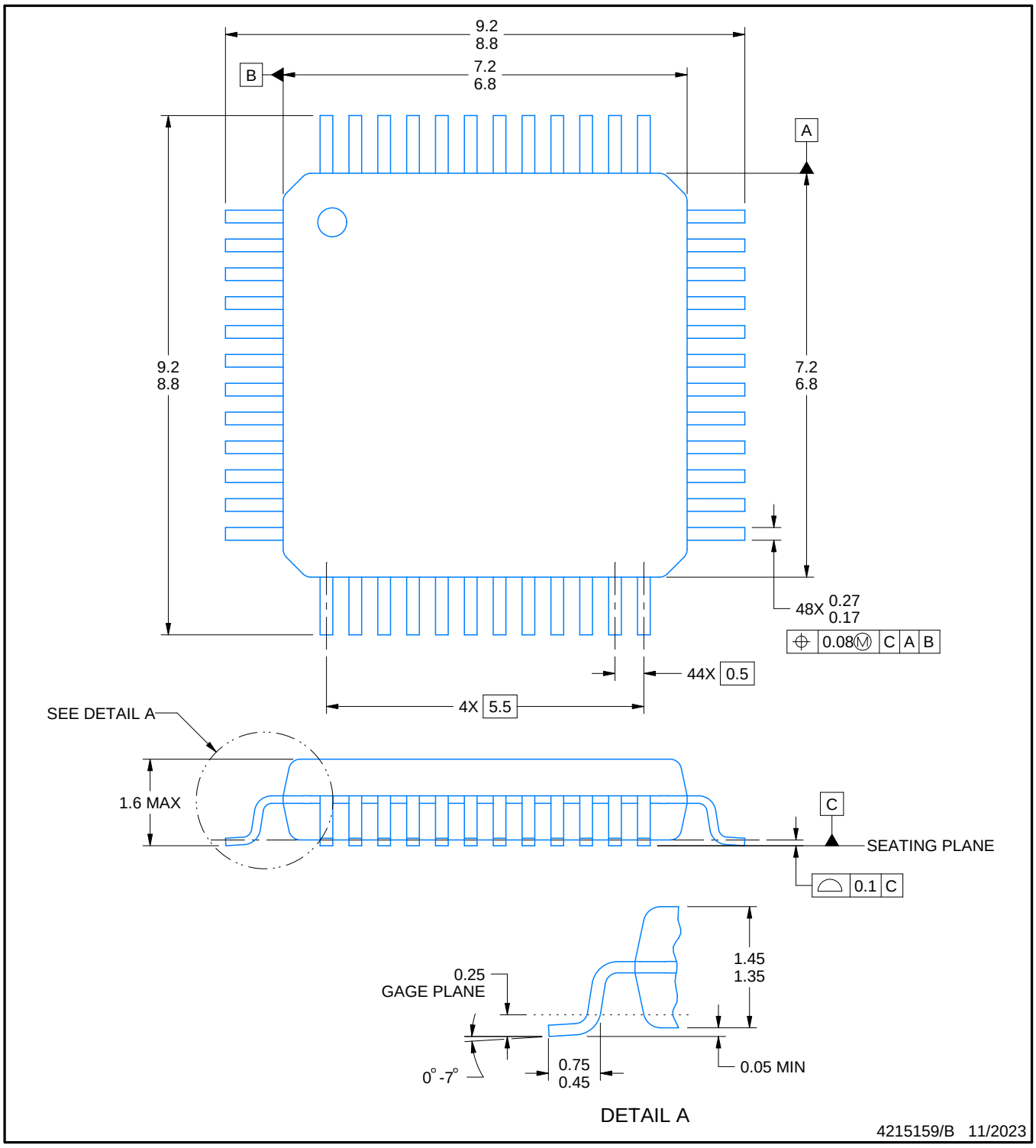
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

PT0048A

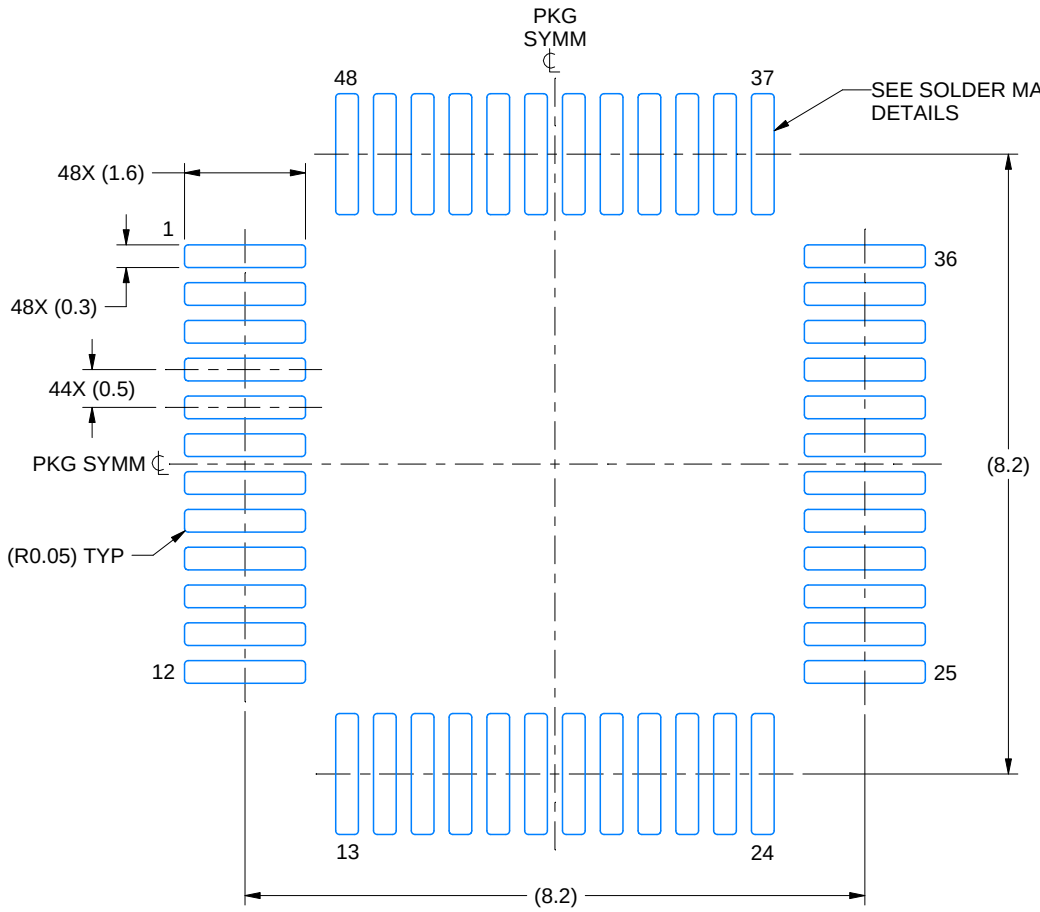
LQFP - 1.6 mm max height

LOW PROFILE QUAD FLATPACK

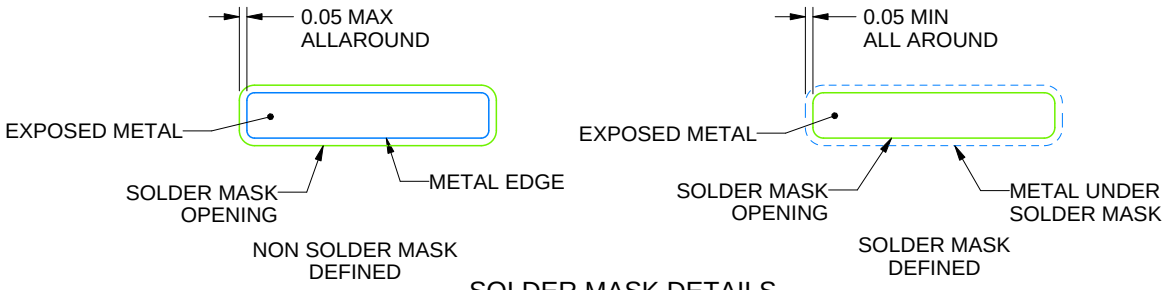


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC registration MS-026.
4. This may also be a thermally enhanced plastic package with leads conected to the die pads.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE 10.000



SOLDER MASK DETAILS

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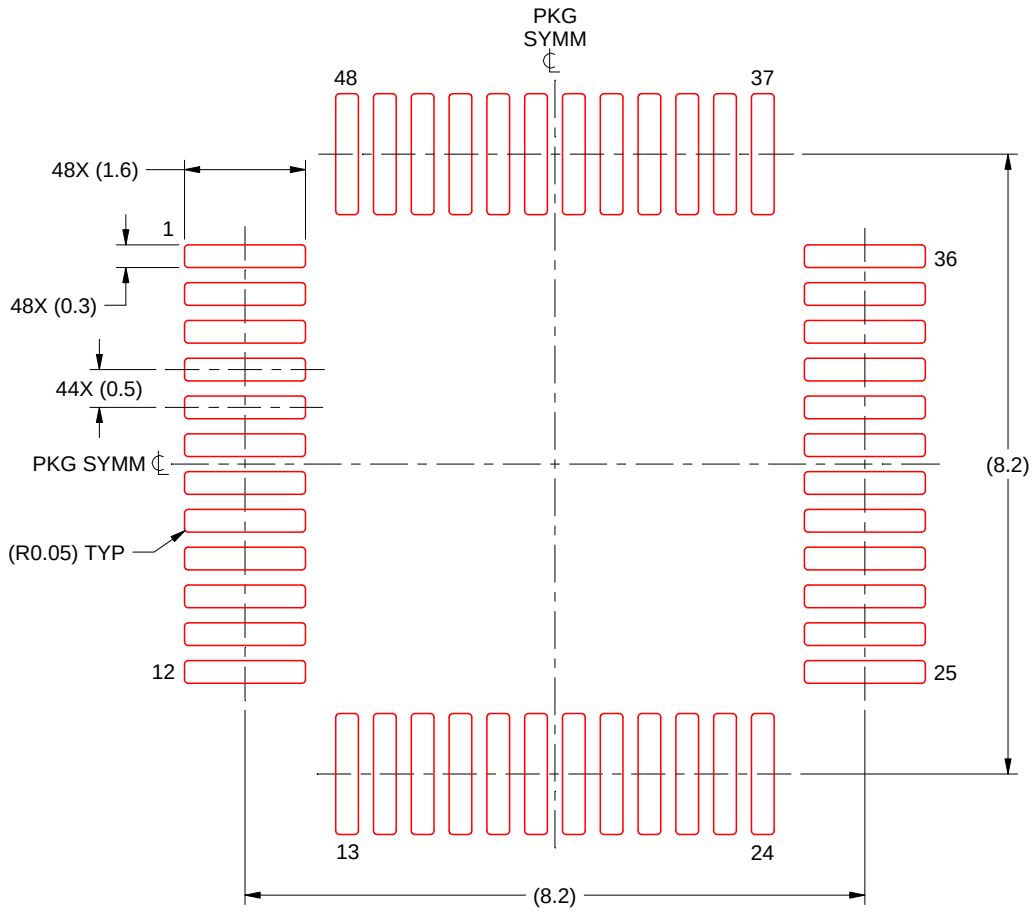
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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