TPD4E101 4-Channel Bidirectional Low Capacitance ESD Protection Device with 15-kV Contact and Ultra-Low Clamping Voltage

1 Features

- Provides System-Level ESD Protection for Low-Voltage I/O Interface
- IEC 61000-4-2 Level 4 ESD Protection
  - ±15-kV Contact Discharge
  - ±15-kV Air-Gap Discharge
- IEC 61000-4-5 (Surge): 3 A (8/20 µs)
- I/O Capacitance 4.8 pF (Typical)
- Dynamic Resistance 0.45 Ω (Typical)
- DC Breakdown Voltage ±6 V (Minimum)
- Ultra-Low Leakage Current 100 nA (Maximum) Overtemperature
- 10-V Clamping Voltage (Maximum at I_{PP} = 1 A)
- Industrial Temperature Range: –40°C to +125°C
- Space Saving DPW package (0.8-mm × 0.8-mm)

2 Applications

- End Equipment:
  - Cell Phones
  - Portable Media Players
  - Wearables
  - Set-Top Boxes
  - eBooks
- Interfaces:
  - SIM Card Interfaces
  - Audio Lines
  - SD Interfaces
  - Push-Buttons

3 Description

The TPD4E101 device is a four-channel electrostatic discharge (ESD) transient voltage suppression (TVS) diode array in an ultra small 0.8-mm × 0.8-mm package. This TVS protection device offers ±15-kV contact ESD, ±15-kV IEC air-gap protection, and has four back-to-back TVS diodes for bipolar or bidirectional signal support. The 4.8-pF typical line capacitance of this ESD protection diode array is suitable for a wide range of applications supporting data rates up to 700 Mbps. The DPW package is convenient for component placement in space-constrained applications and the 0.48-mm pitch helps save on PCB manufacturing costs.

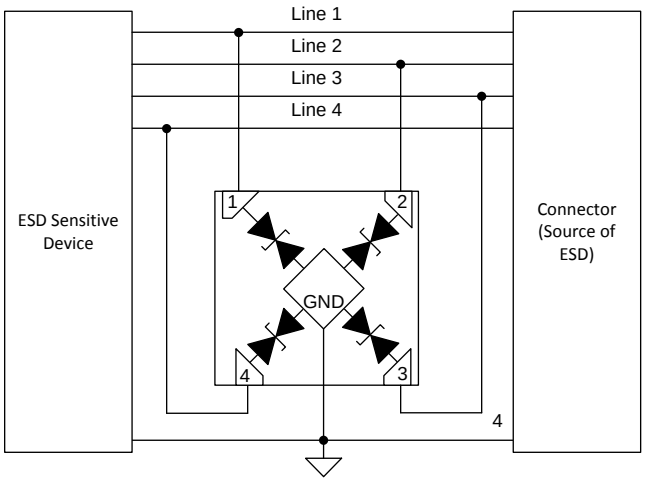
Typical applications of this ESD protection device are circuit protection for SIM cards, audio lines (microphones, earphones, and speakerphones), SD interfaces and pushbuttons. This ESD clamp is good for providing protection in end-equipment like cell phones, portable media players, wearables, set-top boxes, and eBooks.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPD4E101	X2SON (4)	0.80 mm × 0.80 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Schematic



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4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (July 2015) to Revision E — **Page**

- Updated pin configurations ... 1

Changes from Revision C (September 2013) to Revision D — **Page**

- Added *Pin Configuration and Functions* section, *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

Changes from Revision B (May 2013) to Revision C — **Page**

- Updated first page formatting. ... 1
- Changed VClamp1,2 Test Condition From: I_{PP} = 5 A, 8/20 μs To: I_{PP} = 3 A, 8/20 μs ... 4
- Changed VClamp2,1 Test Condition From: I_{PP} = 5 A, 8/20 μs To: I_{PP} = 3 A, 8/20 μs ... 4

Changes from Revision A (January 2013) to Revision B — **Page**

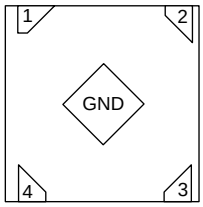
- Updated PARAMETER wording for VClamp1,2 and VClamp2,1 ... 4

Changes from Original (August 2012) to Revision A — **Page**

- Revised document to release full version of Datasheet. ... 1
- Added APPLICATION INFORMATION section. ... 9

5 Pin Configuration and Functions

DPW Package
4-Pin X2SON
Bottom View



Pin Functions

PIN	I/O	DESCRIPTION
1	I/O	ESD protected channels
2		
3		
4		
GND	Ground	Connected to PCB ground plane

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)

	MIN	MAX	UNIT
Peak Pulse Current (tp = 8/20 µs)		3	A
Peak Pulse Power (tp = 8/20 µs)		40	W
Operating temperature	–40	125	ºC
Storage temperature, T_{stg}	–65	155	ºC

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2500	V
	Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±1000	
	IEC 61000-4-2 Contact Discharge	±15000	
	IEC 61000-4-2 Air-gap Discharge	±15000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
Operating Free-Air Temperature, T_A		–40	125	°C
Operating Voltage	Pin 1,2,3,4 to GND	–5.5	5.5	V

6.4 Thermal Information

THERMAL METRIC (1)		TPD4E101 DPW (X2SON) 4 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	291.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	224.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	245.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	31.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	245.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	195.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

T_A = –40°C to +125°C (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{RWM}	Reverse stand-off voltage				±5.5	V
I_{LEAK}	Leakage current	Pins = 5 V, GND = 0 V			100	nA
VClamp1,2	Clamp voltage from data pin to ground pin	I_{PP} = 1 A, 8/20 µs (1)		10		V
		I_{PP} = 3 A, 8/20 µs (1)		13		V
VClamp2,1	Clamp voltage from ground pin to data pin	I_{PP} = 1 A, 8/20 µs (1)		9		V
		I_{PP} = 3 A, 8/20 µs (1)		13		V

(1) Non-repetitive current pulse 8/20 µs exponentially decaying waveform according to IEC61000-4-5.

Electrical Characteristics (continued)

T_A = –40°C to +125°C (unless otherwise specified)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{DYN}	Dynamic resistance	Pins to GND(2)		0.45		Ω
		GND to Pins(2)		0.42		Ω
C_{IO}	I/O Capacitance	V_{IO} = 2.5 V		4.8	7	pF
V_{BRF}	Break-down voltage, pin 1, 2, 3, or 4 to GND	I_{IO} = 1 mA	6			V
V_{BRR}	Break-down voltage, GND to pin 1, 2, 3, or 4	I_{IO} = 1 mA	6			V

(2) Extraction of R_{DYN} using least squares fit of TLP characteristics between I = 10 A and I = 20 A.

6.6 Typical Characteristics

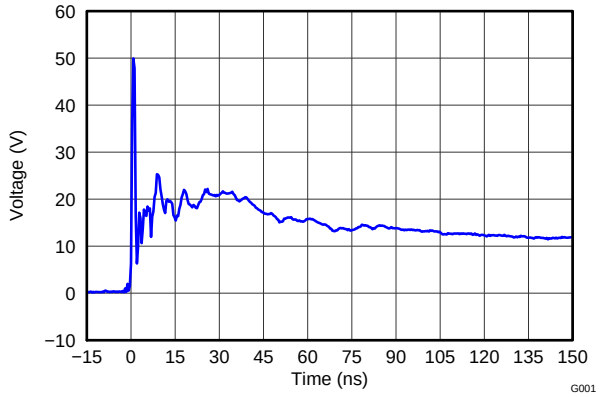


Figure 1. IEC 61000-4-2 Clamping Voltage, 8-kV Contact

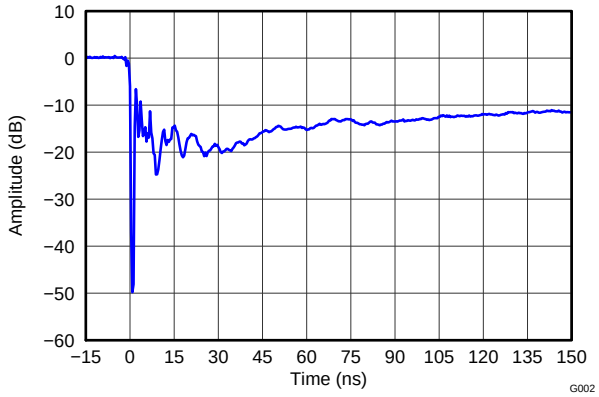


Figure 2. IEC 61000-4-2 Clamping Voltage, –8-kV Contact

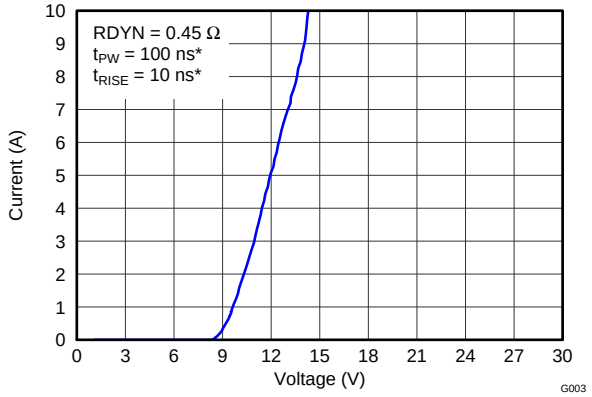


Figure 3. TLP, t_{PW} = 100 nS, t_{RISE} = 10 nS, Data to GND

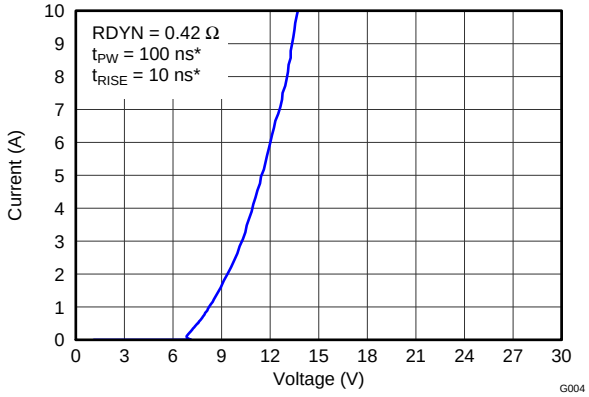


Figure 4. TLP, t_{PW} = 100 nS, t_{RISE} = 10 nS, GND to Data

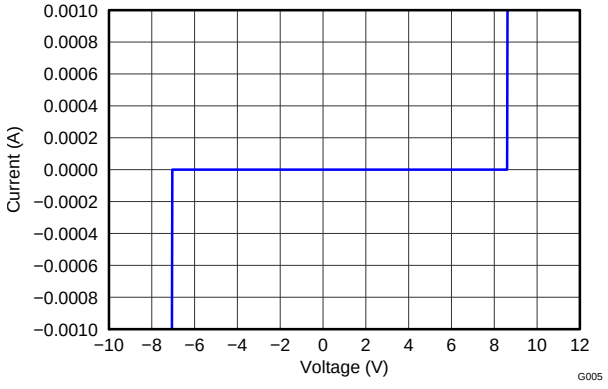


Figure 5. IV Curve

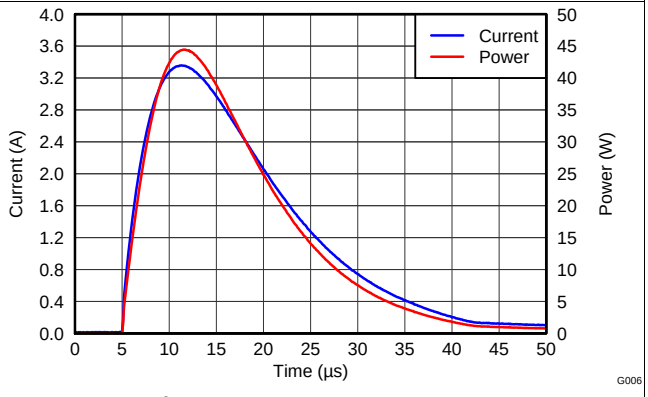


Figure 6. Surge Curves, Data to GND

Typical Characteristics (continued)

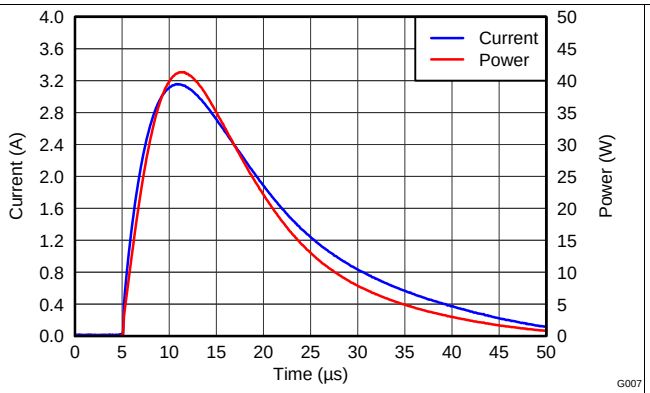


Figure 7. Surge Curves, GND to Data

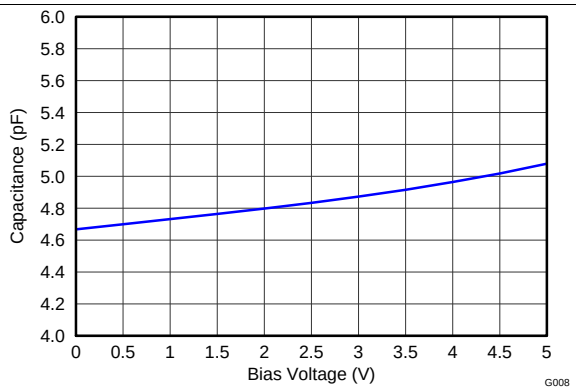


Figure 8. Capacitance

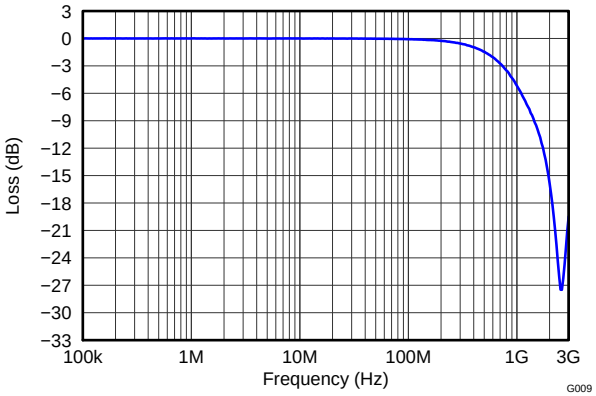


Figure 9. Insertion Loss

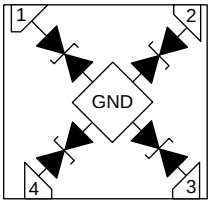
7 Detailed Description

7.1 Overview

The TPD4E101 is a four-channel ESD TVS diode protection device. The device offers ±15-kV IEC air-gap, ±15-kV contact ESD protection. Each channel has a back-to-back TVS diode to support bipolar or bidirectional signal. This device allows a wide range of applications supporting data rates up to 700 Mbps with the 4.8-pF typical line capacitance. The package is compact and convenient for component placement in space-constrained applications. The 0.48-mm pitch helps save on PCB manufacturing costs.

Typical interfaces that can be protected by TPD4E101 are SIM cards, audio lines (microphones, earphones, and speakerphones), SD interfaces, and push-buttons. The TPD4E101 is good for providing protection in end-equipment like cell phones, portable media players, wearables, set-top boxes, and eBooks.

7.2 Functional Block Diagram



7.3 Feature Description

The TPD4E101 is a four-channel bidirectional TVS device with high ESD protection level. This device provides a very robust protection from ESD strikes up to ±15-kV contact and ±15-kV air-gap specified in the IEC 61000-4-2 level 4 international standard. The device can also handle up to 3-A surge current (IEC61000-4-5 8/20 µs). The typical I/O capacitance of 4.8 pF supports a data rate up to 700 Mbps. This clamping device has a small dynamic resistance of 0.45 Ω typically. This makes the clamping voltage low when the device is actively protecting other circuits. For example, the clamping voltage is only 10 V when the device takes 1-A surge current. The small package makes it a great protection option for personal electronics applications like SIM cards and SD interfaces. The breakdown is bidirectional so that it is also a good fit for bidirectional signal applications like audio lines. Ultra-low leakage allows the diode to conserve power in the normal voltages. The industrial temperature range of –40°C to +125°C makes this ESD device work at extensive temperatures in most environments.

7.4 Device Functional Modes

The TPD4E101 is a four-channel passive clamps device that has low leakage during normal operation when the voltage between the ESD-protected channels and GND is within the range of –5.5 V to 5.5 V and activates when it goes out of the range. During IEC ESD events, transient voltages as high as ±15 kV can be clamped between the ESD protected channels and GND pin. When the voltages on the protected lines fall within the trigger range, the device reverts back to the low-leakage passive state.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

When a system contains a human interface, it becomes vulnerable to large system-level ESD strikes that standard ICs cannot survive. TVS ESD protection diodes are typically used to suppress ESD at these interfaces. The TPD4E101 is a four-channel bidirectional TVS device , which is typically used to provide paths to ground for dissipating ESD events on signal or power lines between a human interface connector and a system. As the current from ESD passes through the device, only a small voltage drop is present across the diode structure. This is the voltage presented to the protected IC. The low R_{DYN} of the triggered TVS holds this voltage, V_{CLAMP}, to a tolerable level to the protected IC.

8.2 Typical Application

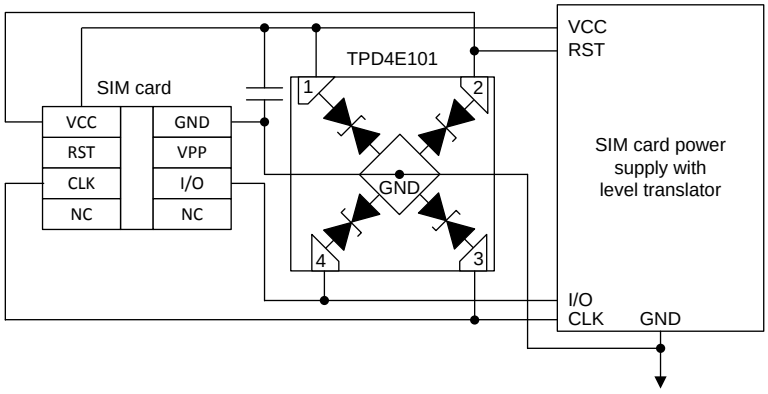


Figure 10. Typical Application Schematic

8.2.1 Design Requirements

For this design example, the TPD4E101 will be used to protect the SIM card. For this application, the system parameters listed in Table 1 are known.

Table 1. Design Parameters

DESIGN PARAMETER	VALUE
SIM card power supply voltage (Vcc)	3.3 V or 5 V
Signal pins voltage range	0 V to Vcc
Signal pins data rate	1 Mbps to 20 Mbps
Required IEC 61000-4-2 ESD Protection	±8-kV Contact / ±15-kV Air-Gap

8.2.2 Detailed Design Procedure

To begin the design process, some parameters must be decided upon; the designer must make sure:

- Voltage range on the protected line must not exceed the reverse standoff voltage of the TVS diode(s) (V_{RWM}).
- Operating frequency is supported by the I/O capacitance C_{IO} of the TVS diode.
- IEC 61000-4-2 protection requirement is covered by the IEC performance of the TVS diode.

For this application, the power supply and signal voltage range is 0 to 3.3 V or to 5 V. The V_{RWM} for the TVS is ±5.5 V; therefore, the bidirectional TVS will not break down during normal operation, and therefore normal operation of the power supply and signal pins will not be effected. Either a unidirectional or bidirectional ESD clamping device is good for this application.

Next, consider the data rate of the signal. The SIM card clock frequency that the signals run off is from 1 MHz to 20 MHz; ensure that the TVS I/O capacitance will not distort this signal by filtering it with the inherent capacitance. With TPD4E101's typical capacitance of 4.8 pF, which leads to a typical 3-dB bandwidth of 700 MHz, each channel has sufficient bandwidth to pass the signal without distorting it.

Finally, the human interface in this application requires the Level 4 IEC 61000-4-2 system-level ESD protection (±8-kV Contact and ±15-kV Air-Gap). The TPD4E101 can survive at least ±15-kV Contact/ ±15-kV Air-Gap. Therefore, the device can provide sufficient ESD protection for the interface. For any TVS diode to provide its full range of ESD protection capabilities, as well as to minimize the noise and EMI disturbances the board will see during ESD events, it is crucial that a system designer uses proper board layout of their TVS ESD protection diodes. See the *Layout Example* for instructions on properly laying out TPD4E101.

8.2.3 Application Curves

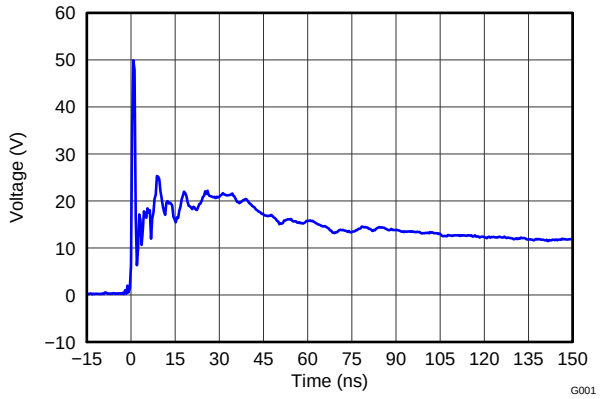


Figure 11. IEC 61000-4-2 Clamping Voltage, 8-kV Contact

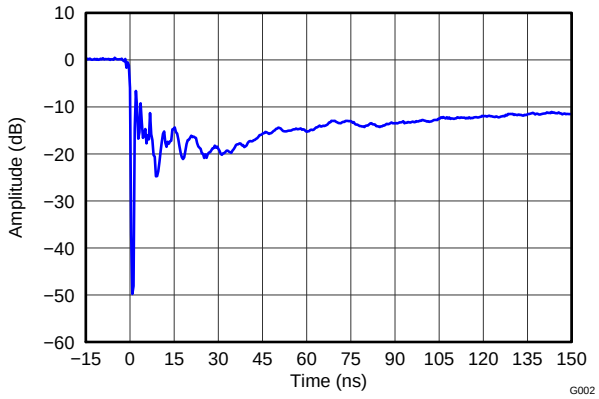


Figure 12. IEC 61000-4-2 Clamping Voltage, –8-kV Contact

9 Power Supply Recommendations

The TPD4E101 is a passive TVS diode-based ESD protection device, so there is no need to power it. Ensure that the maximum voltage specifications for each pin are not violated.

10 Layout

10.1 Layout Guidelines

- The optimum placement is as close to the interface as possible.
  - EMI during an ESD event can couple from the trace being struck to other nearby unprotected traces, resulting in early system failures.
  - The PCB designer must minimize the possibility of EMI coupling by keeping any unprotected traces away from the protected traces which are between the TVS and the interface.
- Route the protected traces as straight as possible.
- Eliminate any sharp corners on the protected traces between the TVS and the connector by using rounded corners with the largest radii possible.
  - Electric fields tend to build up on corners, increasing EMI coupling.
- Use a thick and short trace for the power supply and ground paths.

10.2 Layout Example

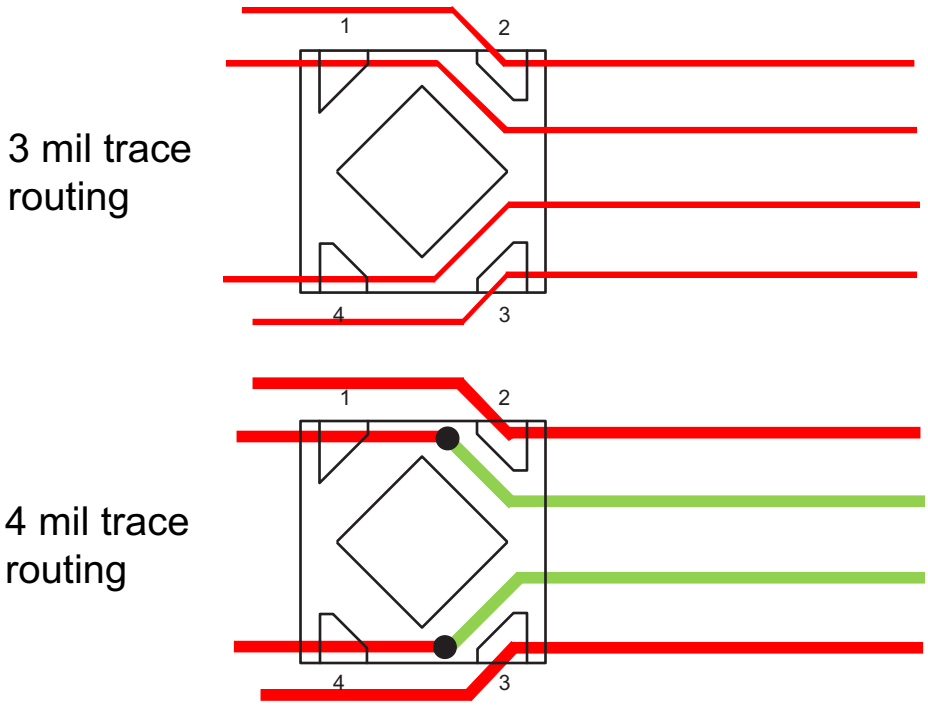


Figure 13. Board Layout Recommendation

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- *Reading and Understanding an ESD Protection Datasheet*, SLLA305
- *ESD Layout Guide*, SLVA680
- *ESD PROTECTION DIODES EVM*, SLVU702

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPD4E101DPWR	Active	Production	X2SON (DPW) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A1
TPD4E101DPWR.B	Active	Production	X2SON (DPW) | 4	3000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	A1

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

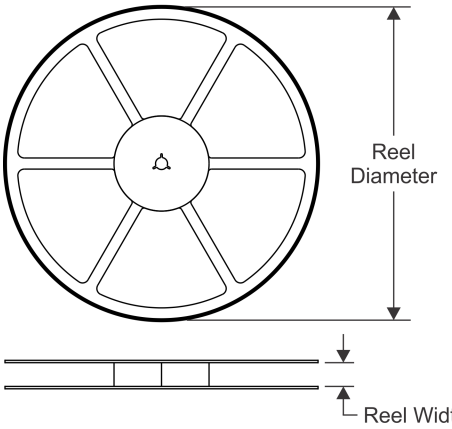
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

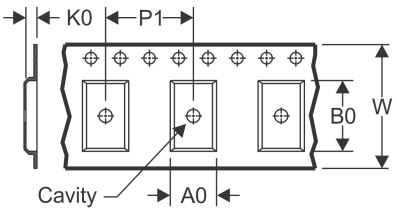
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

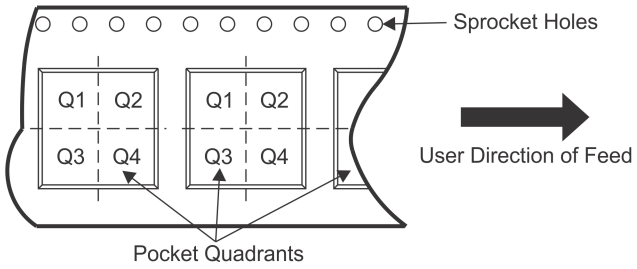


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

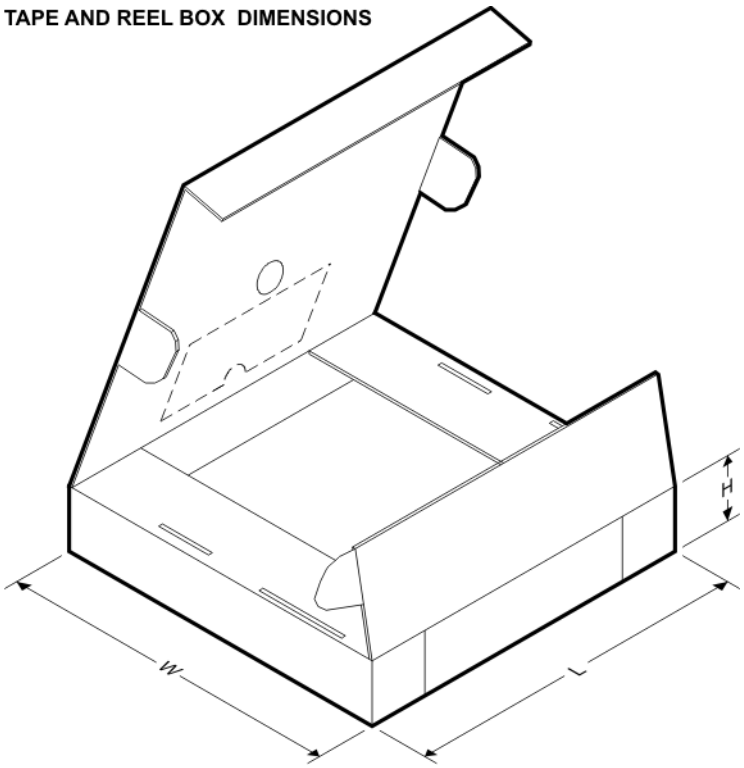
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPD4E101DPWR	X2SON	DPW	4	3000	180.0	9.5	0.91	0.91	0.5	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPD4E101DPWR	X2SON	DPW	4	3000	184.0	184.0	19.0

GENERIC PACKAGE VIEW

DPW 4 X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

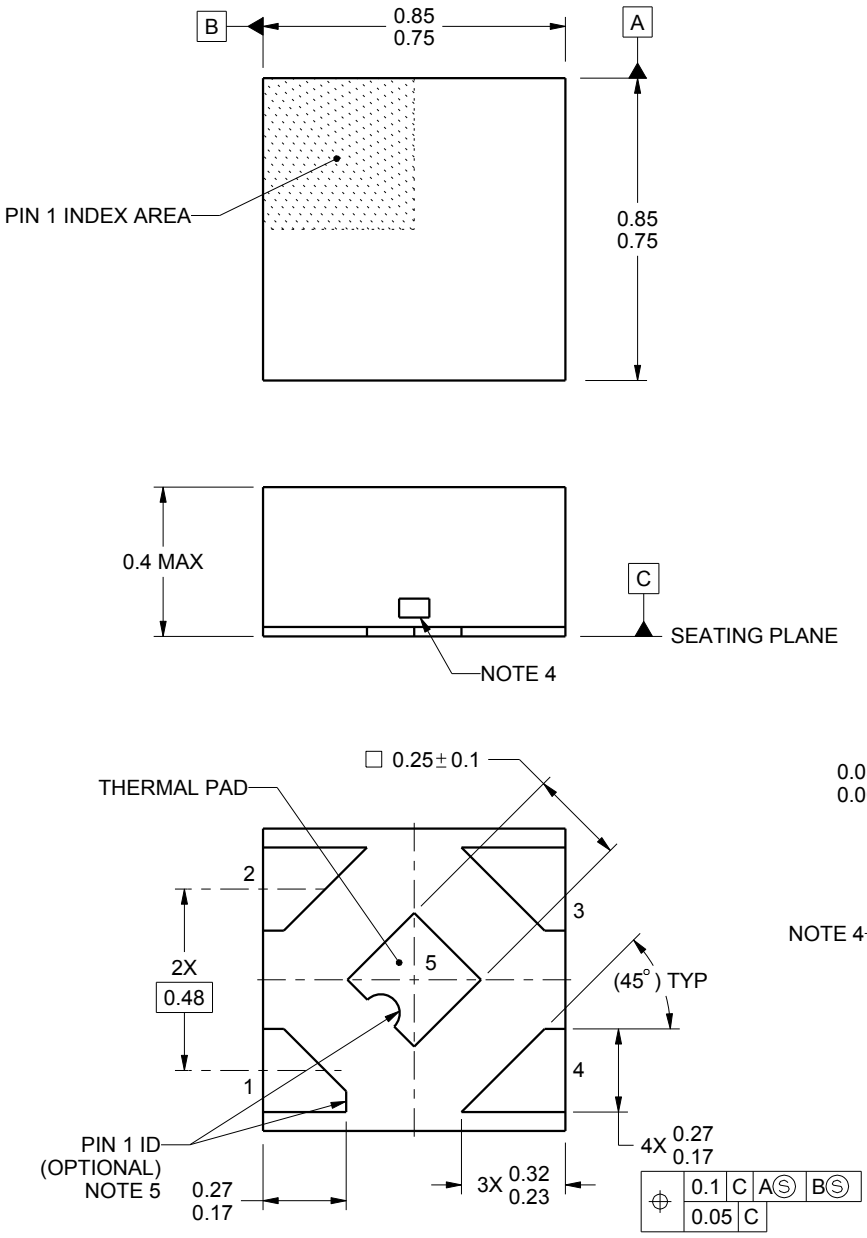
4211218-2/D

PACKAGE OUTLINE

DPW0004A

X2SON - 0.4 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



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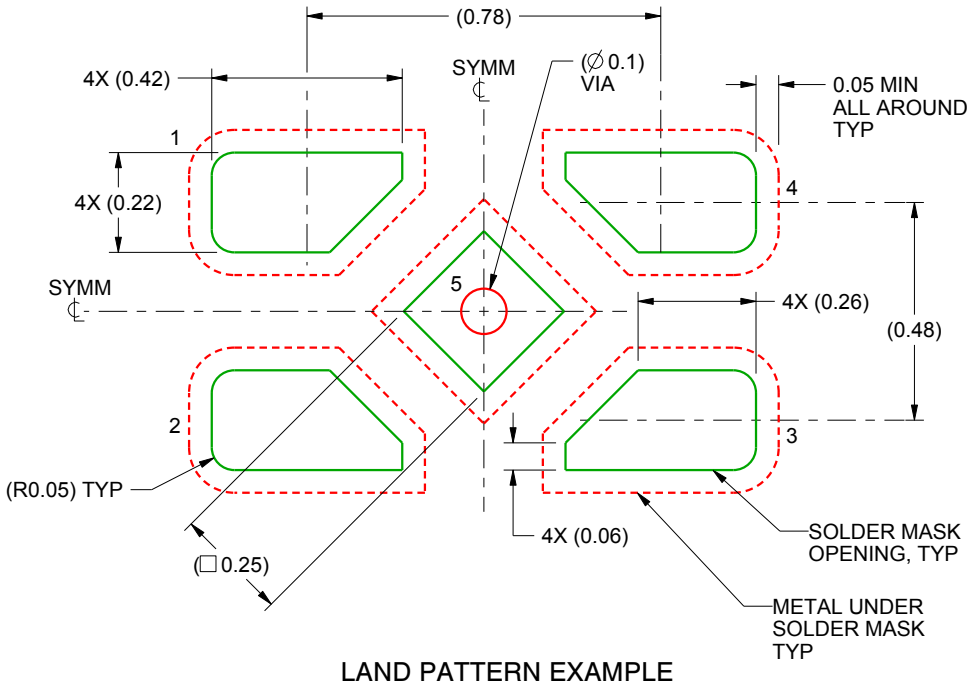
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.
4. The size and shape of this feature may vary.
5. Features may not exist. Recommend use of pin 1 marking on top of package for orientation purposes.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
SCALE:60X

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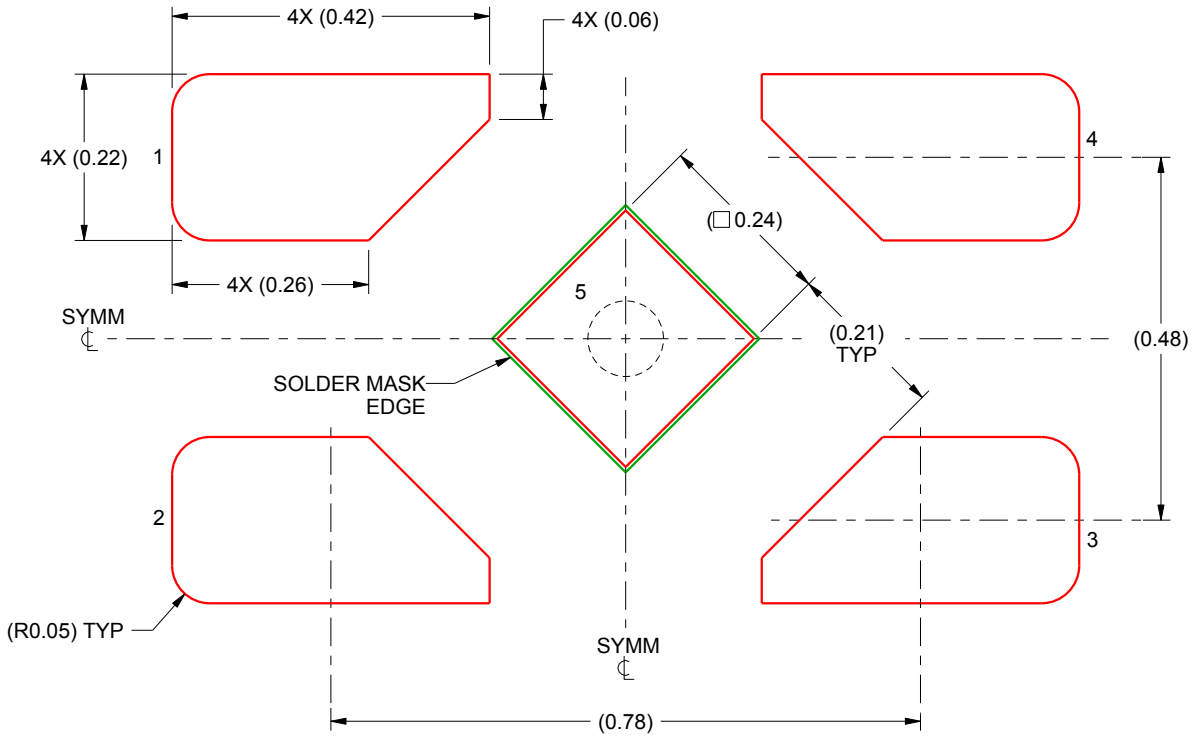
NOTES: (continued)

6. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
7. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL

EXPOSED PAD 5:
92% PRINTED SOLDER COVERAGE BY AREA
SCALE:100X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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