



TPL5010-Q1 AEC-Q100 ウォッチドッグ機能搭載Nano-Powerシステム・タイマ

1 特長

- 車載アプリケーションに対応
- 下記内容でAEC-Q100認定済み
 - デバイス温度グレード1: 動作時周囲温度範囲
–40°C~125°C
 - デバイスHBM ESD分類レベル2
 - デバイスCDM ESD分類レベルC5
- 消費電流: 2.5Vで35nA (標準値)
- 電源電圧: 1.8V~5.5V
- 時間インターバルを100ms~7200sの範囲で選択可能
- タイマ精度: 1% (標準値)
- 時間インターバルを抵抗で選択可能
- ウォッチドッグ機能
- 手動リセット
- TPL5x10QファミリのAEC-Q100 Nano-Powerシステム・タイマ:
 - **TPL5010-Q1:** ウォッチドッグ機能、プログラム可能な遅延範囲
 - **TPL5110-Q1:** MOSドライバ、プログラム可能な遅延範囲、ワンショット機能

2 アプリケーション

- 電気自動車
- 常時オンのシステム
- バッテリ駆動システム
- クラッチ・アクチュエータ回路
- 車のドアハンドル回路
- スマートキー
- リモート電流センサ
- 侵入者検出

3 概要

TPL5010-Q1 Nano Timerは低消費電力でAEC-Q100認定済みのタイマで、ウォッチドッグ機能を持ち、デューティ・サイクル制御またはバッテリー駆動のアプリケーションにおいて、システムのウェークアップを行うために理想的です。このようなシステムでは、マイクロコントローラのタイマを使用してシステムをウェークアップできますが、タイマのスリープ時電流が大きい場合には、スリープ・モード中にシステムの合計電流の最大60~80%がこのマイクロコントローラのタイマにより消費されることがあります。

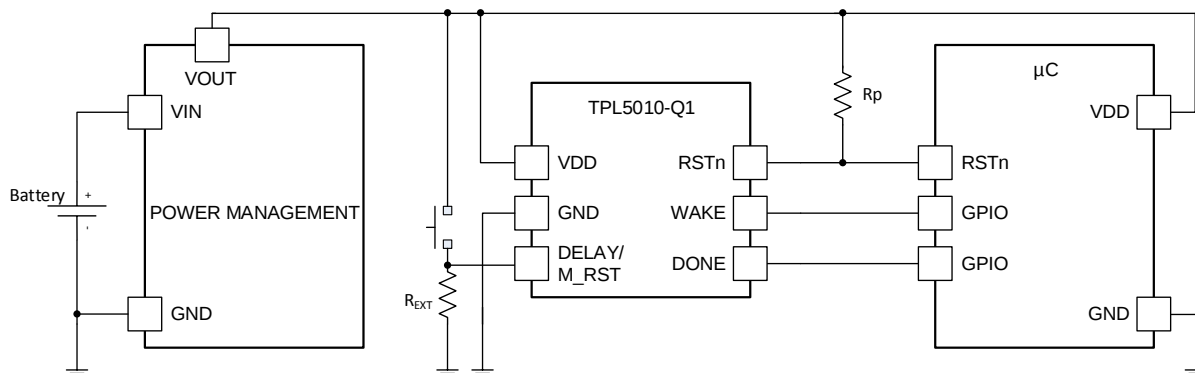
TPL5010-Q1は内蔵のマイクロコントローラのタイマに代わる機能を持ち、消費電流がわずか35nAで、マイクロコントローラを、消費電力がはるかに低いモードに移行できます。このような電力削減によりバッテリー駆動時間が延長され、より小さなバッテリーを使用できるようになるため、TPL5010-Q1は電力の制限が厳しいアプリケーションに理想的です。TPL5010-Q1はタイミング・インターバルを100ms~7200sの範囲で選択でき、割り込み駆動のアプリケーション用に設計されています。一部の標準(EN50271など)では、安全性のためにウォッチドッグの実装が要求されています。TPL5010-Q1を使用すると、ほぼ消費電力の増加なしに、このウォッチドッグ機能を実現できます。TPL5010-Q1は6ピンのSOT23パッケージで供給されます。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
TPL5010-Q1	SOT23 (6)	3.00mm×3.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

アプリケーション概略図



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4 改訂履歴

日付	改訂内容	注
2016年9月	*	初版

5 デバイス比較表

TPL5x10QファミリのAEC-Q100 Nano-Powerシステム・タイマ

型番	消費電流(標準値)	特別な機能
TPL5010-Q1	35nA	低消費電力タイマ
		ウォッチドッグ機能
		遅延範囲をプログラム可能
		手動リセット
TPL5110-Q1	35nA	低消費電力タイマ
		MOSドライバ
		遅延範囲をプログラム可能
		手動リセット
		ワンショット機能

6 Pin Configuration and Functions

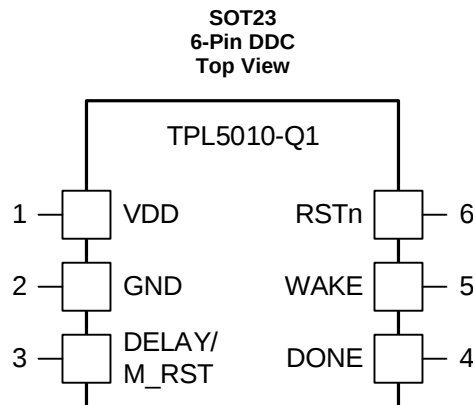


Table 1. Pin Functions

PIN		TYPE ⁽¹⁾	DESCRIPTION	APPLICATION INFORMATION
NO.	NAME			
1	VDD	P	Supply voltage	
2	GND	G	Ground	
3	DELAY/ M_RST	I	Time Interval set and Manual Reset	Resistance between this pin and GND is used to select the time interval. The reset switch is also connected to this pin.
4	DONE	I	Logic Input for watchdog functionality	Digital signal driven by the μ C to indicate successful processing of the WAKE signal.
5	WAKE	O	Timer output signal generated every t_{IP} period.	Digital pulsed signal to wake up the μ C at the end of the programmed time interval.
6	RSTn	O	Reset Output (open drain output)	Digital signal to RESET the μ C, pull-up resistance is required

(1) G= Ground, P= Power, O= Output, I= Input.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

	MIN	MAX	UNIT
Supply voltage (VDD-GND)	−0.3	6.0	V
Input voltage at any pin ⁽²⁾	−0.3	VDD + 0.3	V
Input current on any pin	−5	5	mA
T _{stg} Storage temperature	−65	150	°C
T _J Junction temperature ⁽³⁾		150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The voltage between any two pins should not exceed 6V.
- (3) The maximum power dissipation is a function of T_J(MAX), θ_{JA}, and the ambient temperature, T_A. The maximum allowable power dissipation at any ambient temperature is P_{DMAX} = (T_J(MAX) - T_A) / θ_{JA}. All numbers apply for packages soldered directly onto a PC board.

7.2 ESD Ratings

	VALUE	UNIT
V _(ESD) Electrostatic discharge	Human-body model, per AEC Q100-002 ⁽¹⁾	±2000
	Charged-device model (CDM), per AEC Q10-011	±750

- (1) AEC Q100-002 indicates that HBM stressing shall be in accordance with ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

	MIN	NOM	MAX	UNIT
Supply voltage (VDD-GND)	1.8		5.5	V
Temperature	−40		125	°C

7.4 Thermal Information

THERMAL METRIC ⁽¹⁾		TPL5010-Q1	UNIT
		SOT23	
		6 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	163	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	26	°C/W
R _{θJB}	Junction-to-board thermal resistance	57	°C/W
ψ _{JT}	Junction-to-top characterization parameter	7.5	°C/W
ψ _{JB}	Junction-to-board characterization parameter	57	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

 $T_A = 25^\circ\text{C}$, $V_{DD-GND} = 2.5\text{ V}$ (unless otherwise stated)⁽¹⁾

	PARAMETER	TEST CONDITIONS		MIN ⁽²⁾	TYP ⁽³⁾	MAX ⁽²⁾	UNIT
POWER SUPPLY							
IDD	Supply current ⁽⁴⁾	Operation mode		35	50		nA
		Digital conversion of external resistance (Rext)		200	400		μA
TIMER							
t _{IP}	Time interval period ⁽⁵⁾	1650 selectable time Intervals	Min time interval	100			ms
			Max time interval	7200			s
	Time interval setting accuracy ⁽⁶⁾	Excluding the precision of Rext		±0.6%			
	Timer interval setting accuracy over supply voltage	1.8 V ≤ VDD ≤ 5.5 V		±25			ppm/V
t _{OSC}	Oscillator accuracy			−0.5%	0.5%		
	Oscillator accuracy over temperature ⁽⁵⁾	−40°C ≤ T _A ≤ 125°C		150			ppm/°C
	Oscillator accuracy over supply voltage ⁽⁵⁾	1.8 V ≤ VDD ≤ 5.5 V		±0.4			%/V
	Oscillator accuracy over life time ⁽⁷⁾			0.24%			
t _{DONE}	Minimum DONE pulse width ⁽⁵⁾			100			ns
t _{RSTn}	RSTn pulse width			320			ms
t _{WAKE}	WAKE pulse width			20			ms
t _{_Rext}	Time to convert Rext ⁽⁵⁾			100			ms
DIGITAL LOGIC LEVELS							
VIH	Minimum logic high threshold DONE pin			0.7 × VDD			V
VIL	Maximum logic low threshold DONE pin			0.3 × VDD			V
VOH	Logic output high-level WAKE pin	Iout = 100 μA		VDD − 0.3			V
		Iout = 1 mA		VDD − 0.7			V
VOL	Logic output low-level WAKE pin	Iout = −100 μA		0.3			V
		Iout = −1 mA		0.7			V
VOL _{RSTn}	RSTn logic output low-level	IOL= −1 mA		0.3			V
IOH _{RSTn}	RSTn high-level output current	VOH _{RSTn} = VDD		1			nA
VIH _{M_RST}	Minimum logic high threshold DELAY/M_RST pin ⁽⁵⁾			1.5			V

- Values apply only for factory testing conditions at the temperature indicated. Factory testing conditions result in very limited self-heating of the device such that $T_J = T_A$. No specification of parametric performance is indicated in the electrical tables under conditions of internal self-heating where $T_J > T_A$. Absolute Maximum Ratings indicate junction temperature limits beyond which the device may be permanently degraded, either mechanically or electrically.
- Limits are specified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
- Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
- The supply current excludes load and pull-up resistor current. Input pins are at GND or VDD.
- This parameter is specified by design and/or characterization and is not tested in production.
- The accuracy for time interval settings below 1 second is ±100 ms.
- Operational life time test procedure equivalent to 10 years.

7.6 Timing Requirements

			MIN ⁽¹⁾	NOM ⁽²⁾	MAX ⁽¹⁾	UNIT
t_{RSTn}	Rise Time RSTn ⁽³⁾	Capacitive load 50 pF, Rpull-up 100 kΩ		11		μs
t_{FSTn}	Fall time RSTn ⁽³⁾	Capacitive load 50 pF, Rpull-up 100 kΩ		50		ns
t_{WAKE}	Rise time WAKE ⁽³⁾	Capacitive load 50 pF		50		ns
t_{FWAKE}	Fall time WAKE ⁽³⁾	Capacitive load 50 pF		50		ns
t_{DONE}	DONE to RSTn or WAKE to DONE delay	Min delay ⁽⁴⁾		100		ns
		Max delay ⁽⁴⁾		$t_{IP}-20$		ms
t_{M_RST}	Minimum valid manual reset ⁽³⁾	Observation time 30 ms		20		ms
t_{DB}	De-bounce manual reset			20		ms

- (1) Limits are specified by testing, design, or statistical analysis at 25°C. Limits over the operating temperature range are specified through correlations using statistical quality control (SQC) method.
- (2) Typical values represent the most likely parametric norm as determined at the time of characterization. Actual typical values may vary over time and will also depend on the application and configuration. The typical values are not tested and are not specified on shipped production material.
- (3) This parameter is specified by design and/or characterization and is not tested in production.
- (4) In case of RSTn from its falling edge, in case of WAKE, from its rising edge.

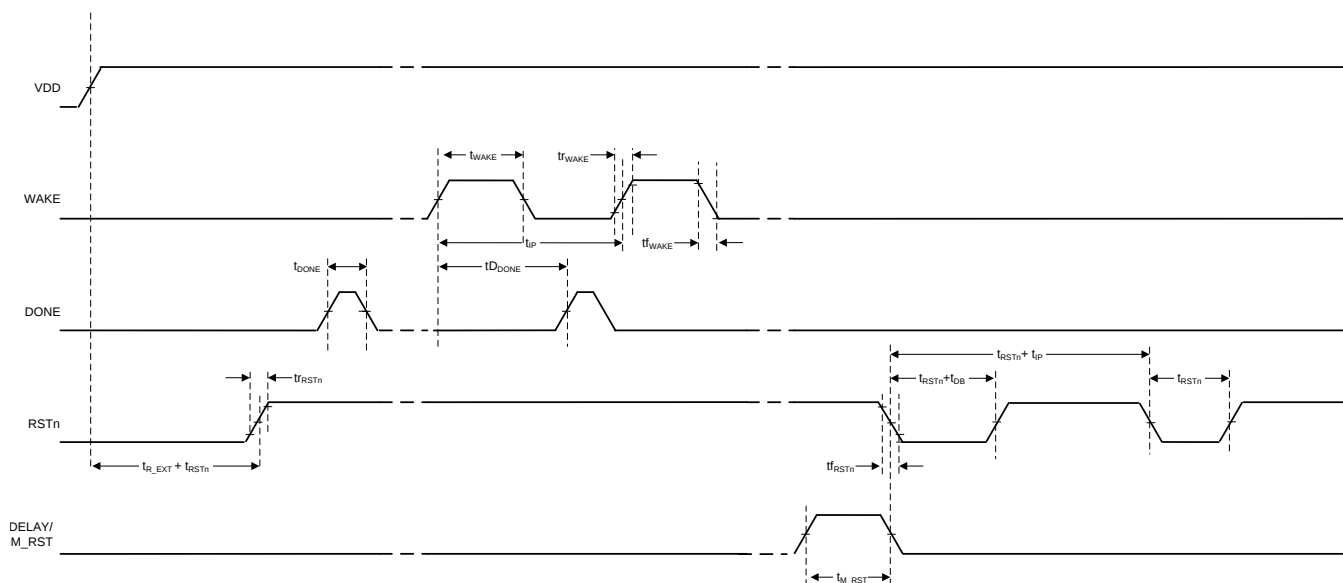


Figure 1. TPL5010-Q1 Timing

7.7 Typical Characteristics

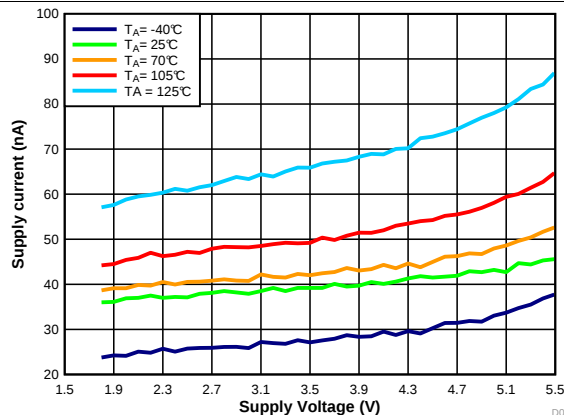


Figure 2. I_{DD} vs V_{DD}

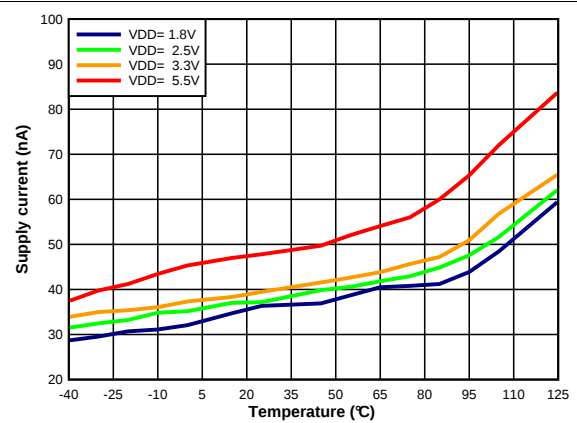


Figure 3. I_{DD} vs Temperature

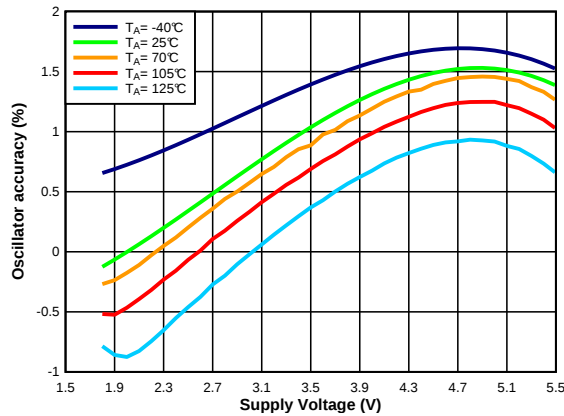


Figure 4. Oscillator Accuracy vs V_{DD}

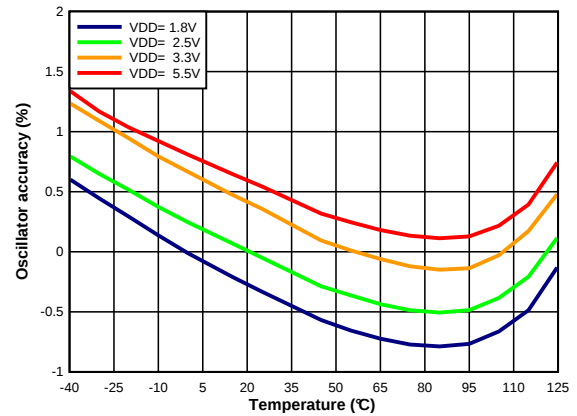


Figure 5. Oscillator Accuracy vs Temperature

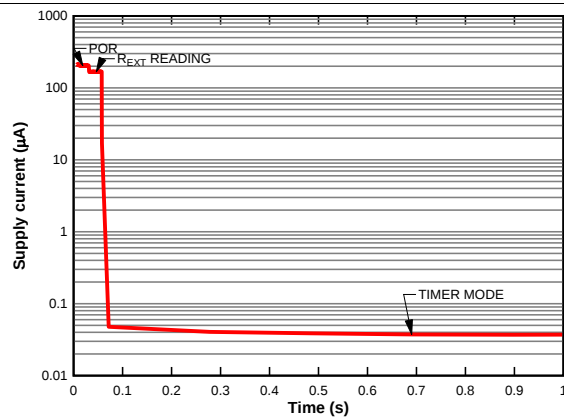


Figure 6. I_{DD} vs Time

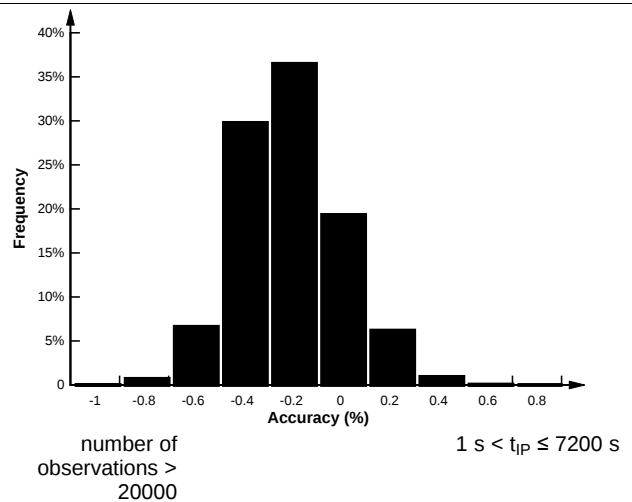


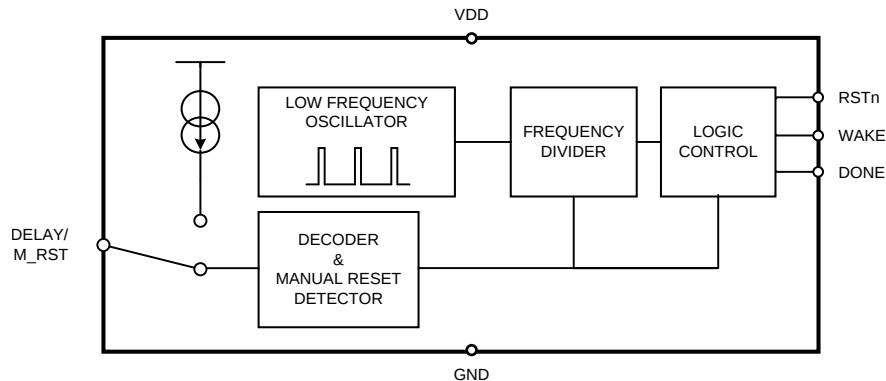
Figure 7. Time Interval Setting Accuracy

8 Detailed Description

8.1 Overview

The TPL5010-Q1 is a system wakeup timer with a watchdog feature, ideal for low power applications. TPL5010-Q1 is ideal for use in interrupt-driven applications and provides selectable timing from 100 ms to 7200 s.

8.2 Functional Block Diagram



8.3 Feature Description

The DONE, WAKE and RSTn signals are used to implement the watchdog function. The TPL5010-Q1 is programmed to issue a periodic WAKE pulse to a μ C which is in sleep or standby mode. After receiving the WAKE pulse, the μ C must issue a DONE signal to the TPL5010-Q1 at least 20 ms before the rising edge of the next WAKE pulse. If the DONE signal is not asserted, the TPL5010-Q1 asserts the RSTn signal to reset the μ C. A manual reset function is realized by momentarily pulling the DELAY/M_RST pin to VDD.

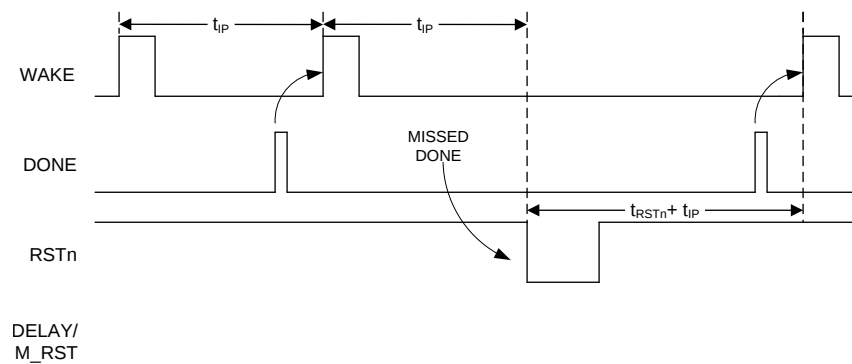


Figure 8. Watchdog

8.3.1 WAKE

The WAKE pulse is sent out from the TPL5010-Q1 when the programmed time interval starts (except at the beginning of the first cycle or if in the previous interval the DONE has not been received).

This signal is normally low.

8.3.2 DONE

The DONE pin is driven by a μ C to signal successful processing of the WAKE signal. The TPL5010-Q1 recognizes a valid DONE signal as a low to high transition; if two or more DONE signals are received within the time interval, only the first DONE signal is processed.

The DONE signal resets the counter of the watchdog only. If the DONE signal is received when the WAKE is still high, the WAKE will go low as soon as the DONE is recognized.

Feature Description (continued)

8.3.3 RSTn

To implement the reset interface between the TPL5010-Q1 and the μC a pull-up resistance is required. 100 k Ω is recommended, to minimize current.

During the POR and the reading of the REXT the RSTn signal is LOW.

RSTn is asserted (LOW) for either one of the following conditions:

- 1. If the DELAY/M_RST pin is high for at least two consecutive cycles of the internal oscillator (approximately 20 ms).
- 2. At the beginning of a new time interval if DONE is not received at least 20 ms before the next WAKE rising edge (see Figure 8).

8.4 Device Functional Modes

8.4.1 Startup

During startup, after POR, the TPL5010-Q1 executes a one-time measurement of the resistance attached to the DELAY/M_RST pin in order to determine the desired time interval for WAKE. This measurement interval is t_{R_EXT} . During this measurement a constant current is temporarily flowing into R_{EXT} .

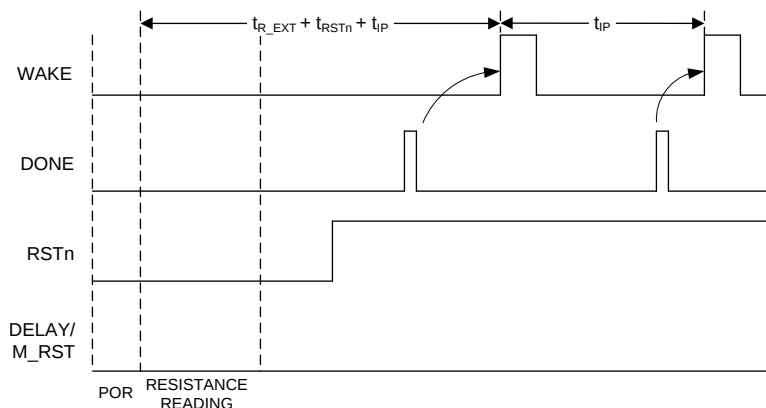


Figure 9. Startup

8.4.2 Normal Operating Mode

During normal operating mode, the TPL5010-Q1 asserts periodic WAKE pulses in response to valid DONE pulses from the μC . If either a manual reset is applied (logic HIGH on DELAY/M_RST pin) or the μC does not issue a DONE pulse within the required time, the TPL5010-Q1 asserts the RSTn signal to the μC and restarts its internal counters. See Figure 8 and Figure 10.

8.5 Programming

8.5.1 Configuring the WAKE Interval with the DELAY/M_RST Pin

The time interval between 2 adjacent WAKE pulses (rising edges) is selectable through an external resistance (R_{EXT}) between the DELAY/M_RST pin and ground. The value of the resistance R_{EXT} is converted one time after POR. The allowable range of R_{EXT} is 500 Ω to 170 k Ω . At least a 1% precision resistance is recommended. See [Timer Interval Selection Using External Resistance](#) for how to set the WAKE pulse interval using R_{EXT} .

The time between 2 adjacent RESET signals (falling edges) or between a RESET (falling edge) and a WAKE (rising edge) is given by the sum of the programmed time interval and the t_{RSTn} (reset pulse width).

Programming (continued)

8.5.2 Manual Reset

If VDD is connected to the DELAY/M_RST pin, the TPL5010-Q1 recognizes this as a manual reset condition. In this case the time interval is not set. If the manual reset is asserted during the POR or during the reading procedure, the reading procedure is aborted and is re-started as soon as the manual reset switch is released. A pulse on the DELAY/M_RST pin is recognized as a valid manual reset only if it lasts at least 20 ms (observation time is 30 ms).

A valid manual reset resets all the counters inside the TPL5010-Q1. The counters restart only when the high digital voltage at DELAY/M_RST is removed and the next t_{RSTn} is elapsed.

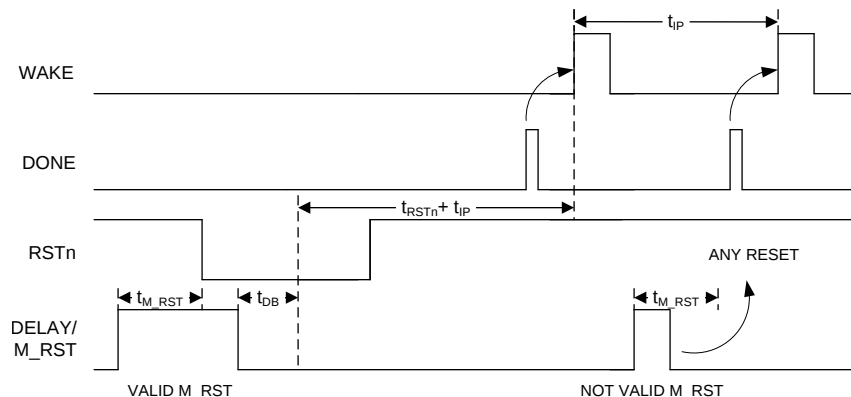


Figure 10. Manual Reset

8.5.2.1 DELAY/M_RST

A resistance in the range between 500 Ω and 170 k Ω needs to be connected in order to select a valid time interval. At the POR and during the reading of the resistance the DELAY/M_RST is connected to an analog signal chain though a mux. After the reading of the resistance the analog circuit is switched off and the DELAY/RST is connected to a digital circuit.

The manual reset detection is supported with a de-bounce feature which makes the TPL5010-Q1 insensitive to the glitches on the DELAY/M_RST pin. When a valid manual reset signal is asserted on the DELAY/M_RST pin, the RSTn signal is asserted LOW after a delay of t_{M_RST} . It remains LOW after a valid manual reset is asserted + $t_{DB} + t_{RSTn}$. Due to the asynchronous nature of the manual reset signal and its arbitrary duration, the LOW status of the RSTn signal maybe affected by an uncertainty of about ± 5 ms.

A valid manual reset puts all the digital output signals at their default values:

- WAKE = LOW
- RSTn = asserted LOW

8.5.2.2 Circuitry

The manual reset may be implemented using a switch (momentary mechanical action). The TPL5010-Q1 offers 2 possible approaches according to the power consumption constraints of the application.

Programming (continued)

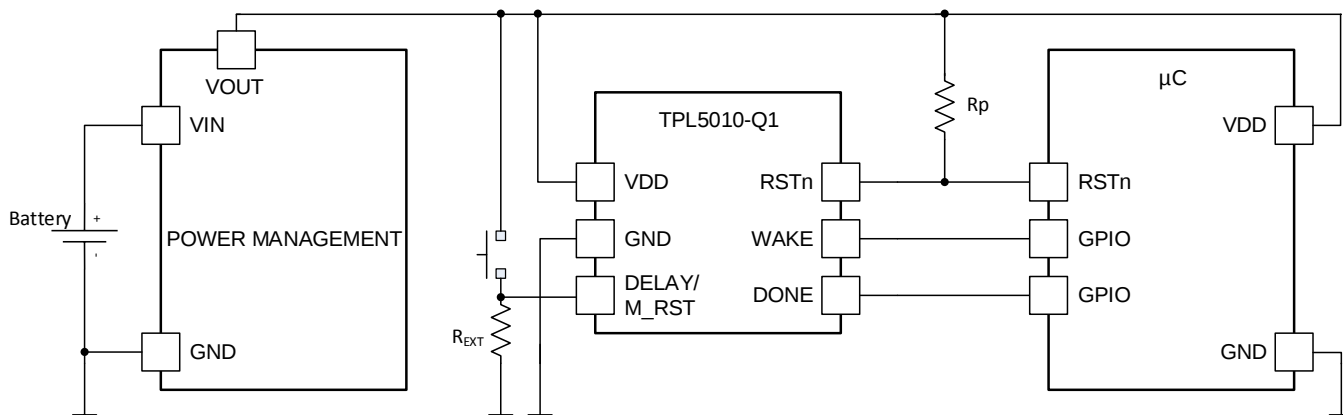


Figure 11. Manual Reset with SPST Switch

For use cases that do not require the lowest power consumption, using a single pole single throw switch may offer a lower cost solution. The DELAY/M_RST pin may be directly connected to VDD with R_{EXT} in the circuit. The current drawn from the supply voltage during the reset is given by VDD/R_{EXT} .

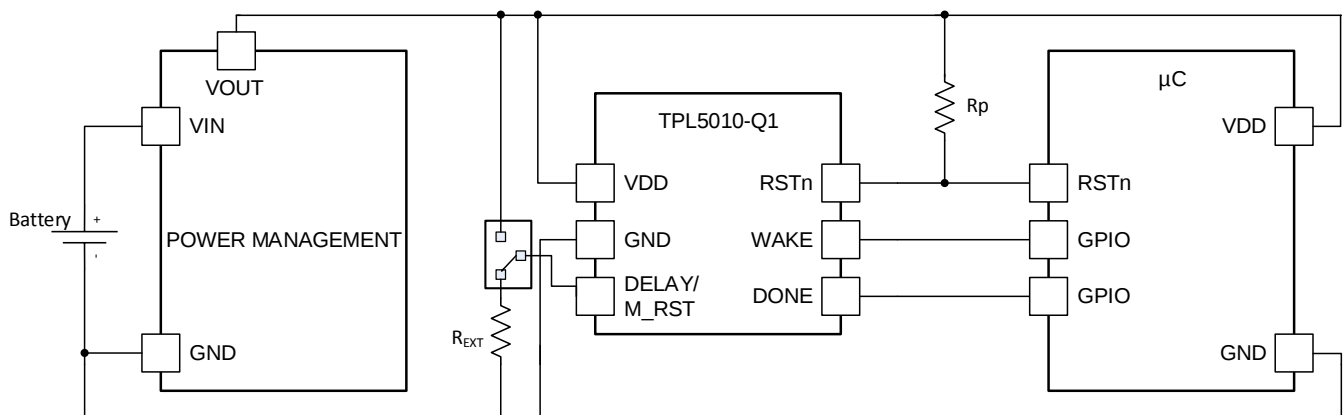


Figure 12. Manual Reset with SPDT Switch

The reset function may also be asserted by switching DELAY/M_RST from R_{EXT} to VDD using a single pole double throw switch, which will provide a lower power solution for the manual reset, because no current flows.

8.5.3 Timer Interval Selection Using External Resistance

In order to set the time interval, the external resistance R_{EXT} is selected according the following formula:

$$R_{EXT} = 100 \left(\frac{-b + \sqrt{b^2 - 4a(c - 100T)}}{2a} \right)$$

where

- T is the desired time interval in seconds
- R_{EXT} is the resistance value to use in Ω
- a, b, c are coefficients depending on the range of the time interval

(1)

Programming (continued)

Table 2. Coefficients for Equation 1

SET	TIME INTERVAL RANGE (s)	a	b	c
1	1 < T ≤ 5	0.2253	–20.7654	570.5679
2	5 < T ≤ 10	–0.1284	46.9861	–2651.8889
3	10 < T ≤ 100	0.1972	–19.3450	692.1201
4	100 < T ≤ 1000	0.2617	–56.2407	5957.7934
5	T > 1000	0.3177	–136.2571	34522.4680

EXAMPLE

Required time interval: 8 s

The coefficient set to be selected is the number 2. The formula becomes:

$$R_{EXT} = 100 \left(\frac{46.9861 - \sqrt{46.9861^2 + 4 * 0.1284 (-2651.8889 - 100 * 8)}}{2 * 0.1284} \right) \quad (2)$$

The resistance value is 10.18 kΩ.

Table 3 and Table 4 contain example values of t_{IP} and their corresponding value of R_{EXT}.

Table 3. First 9 Time Intervals

t _{IP} (ms)	RESISTANCE (Ω)	CLOSEST REAL VALUE (Ω)	PARALLEL OF TWO 1% TOLERANCE RESISTORS (kΩ)
100	500	500	1.0 // 1.0
200	1000	1000	-
300	1500	1500	2.43 // 3.92
400	2000	2000	-
500	2500	2500	4.42 // 5.76
600	3000	3000	5.36 // 6.81
700	3500	3500	4.75 // 13.5
800	4000	4000	6.19 // 11.3
900	4500	4501	6.19 // 16.5

Table 4. Most Common Time Intervals Between 1 s to 2 h

t _{IP}	CALCULATED RESISTANCE (kΩ)	CLOSEST REAL VALUE (kΩ)	PARALLEL OF TWO 1% TOLERANCE RESISTORS (kΩ)
1 s	5.20	5.202	7.15 // 19.1
2 s	6.79	6.788	12.4 // 15.0
3 s	7.64	7.628	12.7 // 19.1
4 s	8.30	8.306	14.7 // 19.1
5 s	8.85	8.852	16.5 // 19.1
6 s	9.27	9.223	18.2 // 18.7
7 s	9.71	9.673	19.1 // 19.6
8 s	10.18	10.180	11.5 // 8.87
9 s	10.68	10.68	17.8 // 26.7
10 s	11.20	11.199	15.0 // 44.2
20 s	14.41	14.405	16.9 // 97.6
30 s	16.78	16.778	32.4 // 34.8
40 s	18.75	18.748	22.6 // 110.0

Table 4. Most Common Time Intervals Between 1 s to 2 h (continued)

t_P	CALCULATED RESISTANCE (k Ω)	CLOSEST REAL VALUE (k Ω)	PARALLEL OF TWO 1% TOLERANCE RESISTORS (k Ω)
50 s	20.047	20.047	28.7 // 66.5
1 min	22.02	22.021	40.2 // 48.7
2 min	29.35	29.349	35.7 // 165.0
3 min	34.73	34.729	63.4 // 76.8
4 min	39.11	39.097	63.4 // 102.0
5 min	42.90	42.887	54.9 // 196.0
6 min	46.29	46.301	75.0 // 121.0
7 min	49.38	49.392	97.6 // 100.0
8 min	52.24	52.224	88.7 // 127.0
9 min	54.92	54.902	86.6 // 150.0
10 min	57.44	57.437	107.0 // 124.0
20 min	77.57	77.579	140.0 // 174.0
30 min	92.43	92.233	182.0 // 187.0
40 min	104.67	104.625	130.0 // 536.00
50 min	115.33	115.331	150.0 // 499.00
1 h	124.91	124.856	221.0 // 287.00
1 h 30 min	149.39	149.398	165.0 // 1580.0
2 h	170.00	170.00	340.0 // 340.0

8.5.4 Quantization Error

The TPL5010-Q1 can generate 1650 discrete timer intervals in the range of 100 ms to 7200 s. The first 9 intervals are multiples of 100 ms. The remaining 1641 intervals cover the range between 1 s to 7200 s. Because they are discrete intervals, there is a quantization error associated with each value.

The quantization error can be evaluated according to the following formula:

$$Err = 100 \frac{(T_{DESIRED} - T_{ADC})}{T_{DESIRED}} \quad (3)$$

Where:

$$T_{ADC} = INT \left[\frac{1}{100} \left(a \frac{R_D^2}{100^2} + b \frac{R_D}{100} + c \right) \right] \quad (4)$$

$$R_D = INT \left[\frac{R_{EXT}}{100} \right]$$

where

- R_{EXT} is the resistance calculated with [Equation 1](#)
 - a, b, c are the coefficients of the equation listed in [Table 2](#)
- (5)

8.5.5 Error Due to Real External Resistance

R_{EXT} is a theoretical value and may not be available in standard commercial resistor values. It is possible to closely approach the theoretical R_{EXT} using two or more standard values in parallel. However, standard values are characterized by a certain tolerance. This tolerance will affect the accuracy of the time interval.

The accuracy can be evaluated using the following procedure:

1. Evaluate the min and max values of R_{EXT} (R_{EXT_MIN} , R_{EXT_MAX} with [Equation 1](#) using the selected commercial resistance values and their tolerances.
2. Evaluate the time intervals ($T_{ADC_MIN}[R_{EXT_MIN}]$, $T_{ADC_MAX}[R_{EXT_MAX}]$) with [Equation 4](#).
3. Find the errors using [Equation 3](#) with T_{ADC_MIN} , T_{ADC_MAX} .

The results of the formula indicate the accuracy of the time interval.

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The example below illustrates the procedure.

- Desired time interval , $T_{\text{desired}} = 600 \text{ s}$
- Required R_{EXT} , from [Equation 1](#), $R_{\text{EXT}} = 57.44 \text{ k}\Omega$

From [Table 4](#), R_{EXT} can be built with a parallel combination of two commercial values with 1% tolerance: $R_1 = 107 \text{ k}\Omega$, $R_2 = 124 \text{ k}\Omega$. The uncertainty of the equivalent parallel resistance can be found using [Equation 6](#).

$$uR_{//} = R_{//} \sqrt{\left(\frac{u_{R1}}{R1}\right)^2 + \left(\frac{u_{R2}}{R2}\right)^2} \quad (6)$$

Where uR_n ($n=1,2$) represent the uncertainty of a resistance,

$$u_{Rn} = Rn \frac{\text{Tolerance}}{\sqrt{3}} \quad (7)$$

The uncertainty of the parallel resistance is 0.82%, meaning the value of R_{EXT} may range between $R_{\text{EXT_MIN}} = 56.96 \text{ k}\Omega$ and $R_{\text{EXT_MAX}} = 57.90 \text{ k}\Omega$.

Using these value of R_{EXT} , the digitized timer intervals calculated with [Equation 4](#) are respectively $T_{\text{ADC_MIN}} = 586.85 \text{ s}$ and $T_{\text{ADC_MAX}} = 611.3 \text{ s}$, giving an error range of $-1.88\% / +2.19\%$. The asymmetry of the error range is due to the quadratic transfer function of the resistance digitizer.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

In battery-powered applications, one design constraint is the need for low current consumption. The TPL5010-Q1 is ideal for applications where there is a need to monitor environmental conditions at a fixed time interval. Often in these applications, a watchdog or other internal timer in a μC is used to implement a wakeup function. Using the TPL5010-Q1 to implement the watchdog function will consume only tens of nA, significantly improving the power consumption of the system.

9.2 Typical Application

The TPL5010-Q1 can be used in conjunction with environment sensors to build a low-power environment data-logger, such as an air quality data-logger. In this application, due to the monitored phenomena, the μC and the front end of the sensor spend most of the time in the idle state, waiting for the next logging interval, usually a few hundred of milliseconds. Figure 13 illustrates a data logging application based on a μC , and a front end for a gas sensor based on the LMP91000.

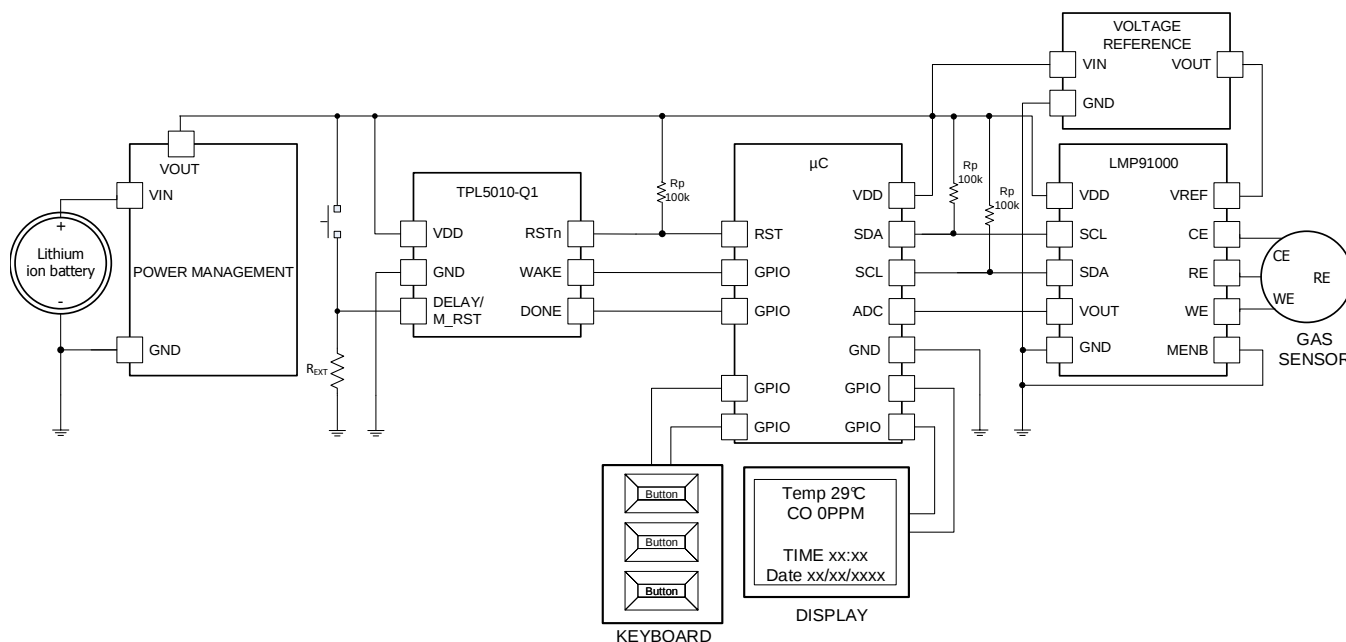


Figure 13. Data-Logger

9.2.1 Design Requirements

The design is driven by the low current consumption constraint. The data are usually acquired on a rate that ranges between 1 s and 10 s. The highest necessity is the maximization of the battery life. The TPL5010-Q1 helps achieve that goal because it allows putting the μC in its lowest power mode. The TPL5010-Q1 will take care of the watchdog and the timing.

Typical Application (continued)

9.2.2 Detailed Design Procedure

When the main constraint is the battery life, the selection of a low-power voltage reference, μC , and display is mandatory. The first step in the design is the calculation of the power consumption of the devices in their different mode of operations. For instance, the LMP91000 burns most of the power when in gas measurement mode, then according to the connected gas sensor it has 2 idle states: stand-by and deep sleep. The same is true for the μC , such as one of the MSP430 family, which can be placed in one of its lower power modes, such as LMP3.5 or LMP4.5. In this case, the TPL5010-Q1 can be used to implement the watchdog and wakeup timing functions.

After the power budget calculation it is possible to select the appropriate time interval which satisfies the application constraints and maximize the life of the battery.

9.2.3 Application Curves

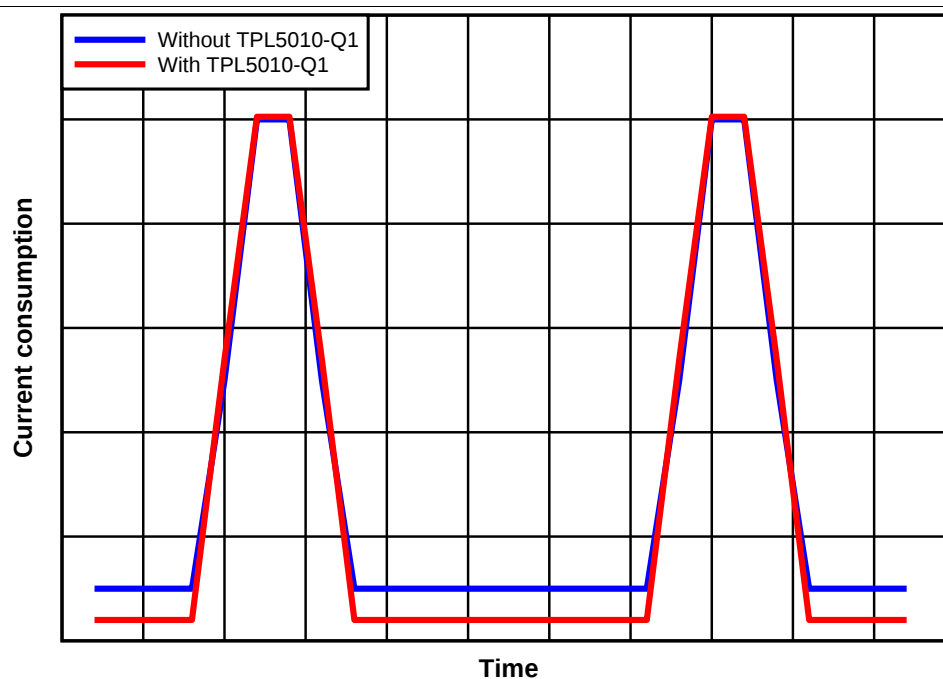


Figure 14. Effect of TPL5010-Q1 on Current Consumption

10 Power Supply Recommendations

The TPL5010-Q1 requires a voltage supply within 1.8 V and 5.5 V. A multilayer ceramic bypass X7R capacitor of 0.1 μ F between VDD and GND pin is recommended.

11 Layout

11.1 Layout Guidelines

The DELAY/M_RST pin is sensitive to parasitic capacitance. It is suggested that the traces connecting the resistance on this pin to GROUND be kept as short as possible to minimize parasitic capacitance. This capacitance can affect the initial set up of the time interval. Signal integrity on the WAKE and RSTn pins is also improved by keeping the trace length between the TPL5010-Q1 and the μ C short to reduce the parasitic capacitance.

11.2 Layout Example

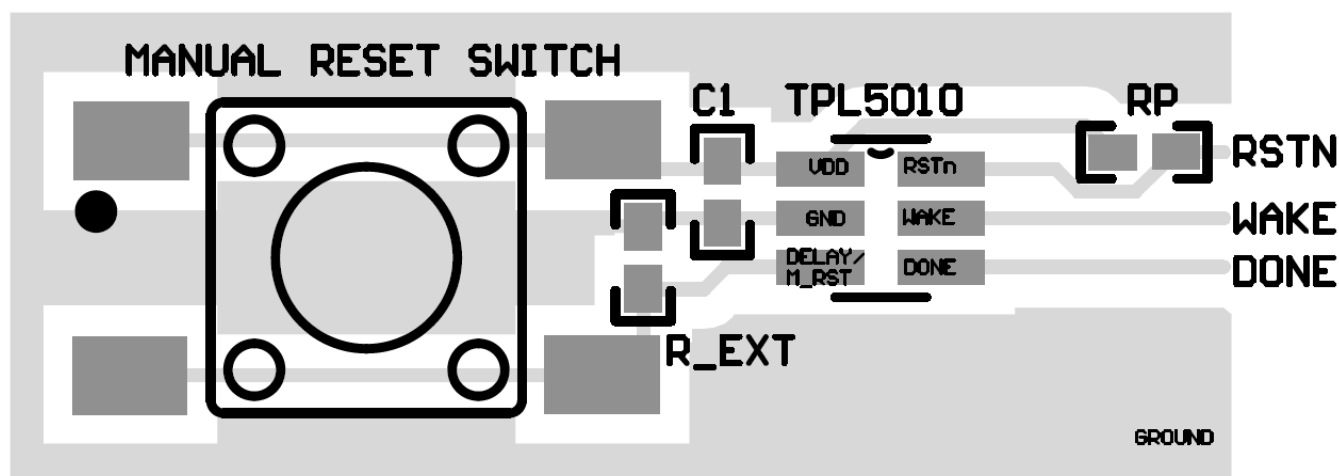


Figure 15. Layout

12 デバイスおよびドキュメントのサポート

12.1 ドキュメントの更新通知を受け取る方法

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12.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

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Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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12.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPL5010QDDCRQ1	ACTIVE	SOT-23-THIN	DDC	6	3000	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	13VX	Samples
TPL5010QDDCTQ1	ACTIVE	SOT-23-THIN	DDC	6	250	RoHS & Green	NIPDAU SN	Level-1-260C-UNLIM	-40 to 125	13VX	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPL5010-Q1 :

- Catalog : [TPL5010](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product



SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



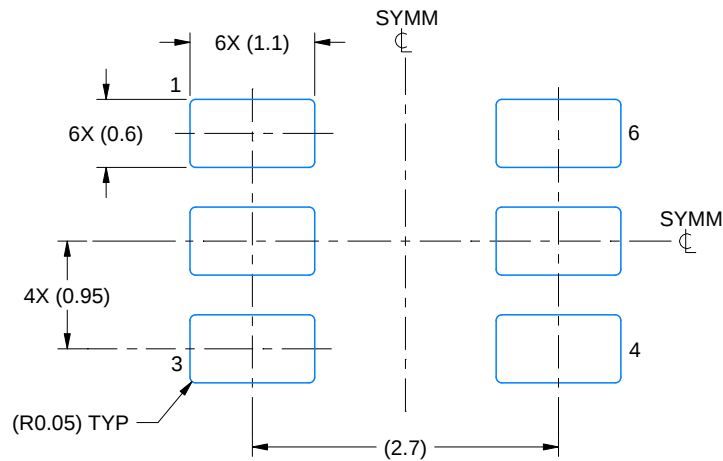
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-193.

EXAMPLE BOARD LAYOUT

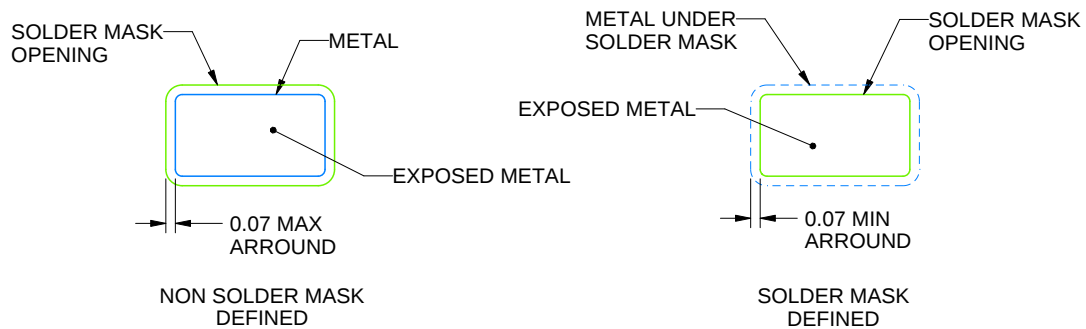
DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE
EXPLODED METAL SHOWN
SCALE:15X



SOLDERMASK DETAILS

4214841/C 04/2022

NOTES: (continued)

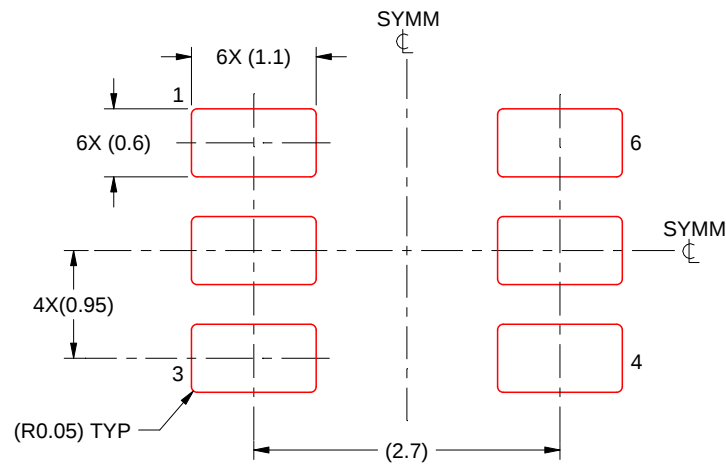
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DDC0006A

SOT-23 - 1.1 max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:15X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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