TEXAS INSTRUMENTS
TPS22811
JAJSOD0A – APRIL 2022 – REVISED JULY 2022

TPS22811x 2.7V～16V、10A、6mΩ ロード・スイッチ、可変過電圧保護および電流監視機能付き

1 特長

- 広い動作時入力電圧範囲:2.7V～16V
  - 絶対最大定格:20V
- 低オン抵抗の FET を内蔵:R_{ON} = 6mΩ (標準値)
- 可変の出力スルーレート (dVdt) 制御
- アクティブ HIGH のイネーブル入力、低電圧誤動作防止 (UVLO) スレッショルドを設定可能
- アクティブ LOW のイネーブル入力、低電圧誤動作防止 (UVLO) スレッショルドを設定可能
- 高速過電圧保護
  - 調整可能な過電圧誤動作防止 (OVLO) (1.2µs (標準値) の応答時間)
- アナログ負荷電流のモニタ出力 (IMON)
  - • 精度:±9% (I_{OUT} > 3A)
- 定常状態時の短絡保護用の高速トリップ応答
  - 応答時間 640ns (標準値)
  - 固定スレッショルド
- 過熱保護
- 可変スレッショルド (PGTH) 付きのパワー・グッド表示 (PG)
- クイック出力放電
- 小型サイズ:QFN 2mm × 2mm (0.45mm ピッチ)

2 アプリケーション

- 光モジュール
- サーバー、PC マザーボード、アドオン・カード
- エンタープライズ・ルータ、データ・センター・スイッチ
- 産業用 PC
- UHDTV

3 概要

TPS22811x は、小さいパッケージに搭載された、高集積のパワー・ディストリビューション・ソリューションです。このデバイスは、最小限の外付け部品で電源レールを制御および監視できます。

出力のスルーレートと突入電流は、1 個の外付けコンデンサを使用して調整できます。入力が過電圧スレッショルド (調整可能) を上回った場合は、出力を遮断することにより負荷を入力過電圧状態から保護します。このデバイスは、高速トリップ応答を内蔵しており、定常状態時に出力に重大なフォルトが発生しても保護できます。

出力負荷電流の正確なアナログ検出を備えており、システムの監視および診断に役立つデジタル・パワー・グッド表示も提供します。

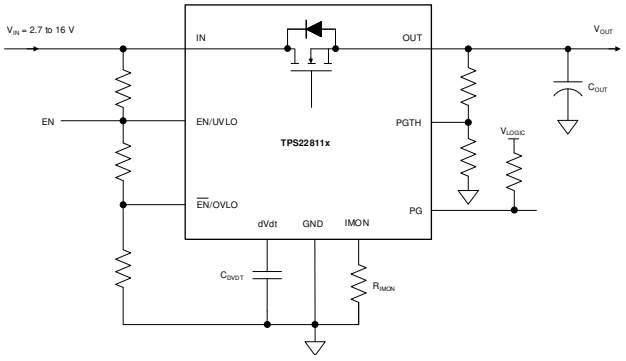
これらのデバイスは、2mm × 2mm、10 ピンの HotRod™ QFN パッケージで供給され、放熱性能の向上とシステムのフットプリントの削減に役立ちます。

これらのデバイスは、–40℃～+125℃の接合部温度範囲で動作が規定されています。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
TPS22811	RPW (VQFN-HR、10)	2.00mm × 2.00mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



概略回路図

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (April 2022) to Revision A (July 2022)	Page
• ステータスを「事前情報」から「量産データ」に変更	1

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5 Pin Configuration and Functions

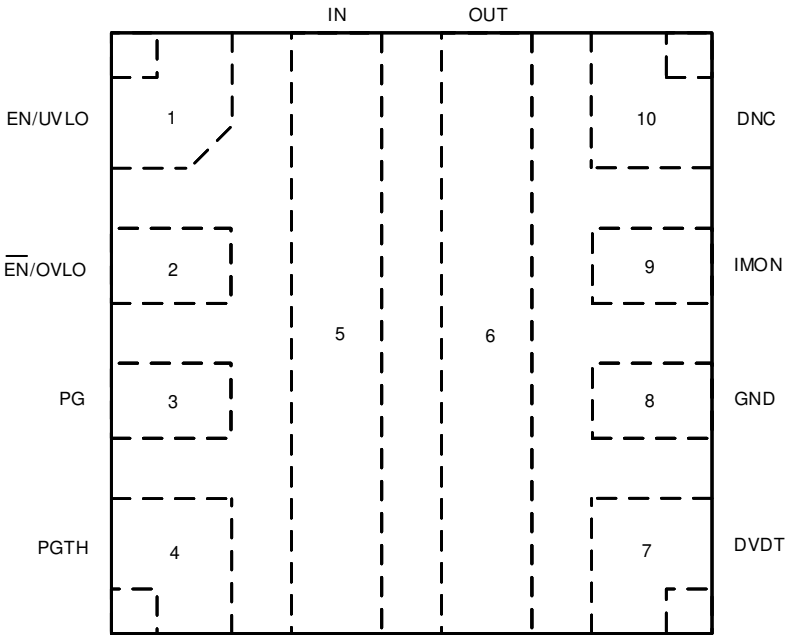

図 5-1. TPS22811x RPW Package 10-Pin QFN Top View

表 5-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
EN/UVLO	1	Analog Input	Active high enable for the device. A resistor divider on this pin from input supply to GND can be used to adjust the Undervoltage Lockout threshold. *Do not leave floating.* Refer to *Undervoltage Lockout (UVLO and UVP)* for details.
$\overline{EN}$/OVLO	2	Analog Input	A resistor divider on this pin from supply to GND can be used to adjust the overvoltage lockout threshold. This pin can also be used as an active low enable for the device. *Do not leave floating.* Refer to *Overvoltage Lockout (OVLO)* for more details.
PG	3	Digital Output	Power-good indication. This pin is an open-drain signal which is asserted high when the internal power path is fully turned ON and PGTH input exceeds a certain threshold. Refer to *Power-Good Indication (PG)* for more details.
PGTH	4	Analog Input	Power-good threshold. Refer to *Power-Good Indication (PG)* for more details.
IN	5	Power	Power input
OUT	6	Power	Power output
DVDT	7	Analog Output	A capacitor from this pin to GND sets the output turn on slew rate. Leave this pin floating for the fastest turn on slew rate. Refer to *Slew Rate (dVdt) and Inrush Current Control* for more details.
GND	8	Ground	This pin is the ground reference for all internal circuits and must be connected to system GND.
IMON	9	Analog Output	Analog load current monitor output. An external resistor from this pin to GND sets the gain for the current monitor. This pin also provides a secondary function of setting the current limit during start-up. Connect to GND if neither of these features are used. *Do not leave floating.* Refer to *Analog Load Current Monitor* and *Active Current Limiting During Start-Up* for more details.
DNC	10	X	Do not connect anything to this pin.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Maximum input voltage range, –40℃ ≤ T_J ≤ 125℃	IN	–0.3	20	V
V_{OUT}	Maximum output voltage range, –40℃ ≤ T_J ≤ 125℃	OUT	–0.3	V_{IN} + 0.3	
$V_{OUT,PLS}$	Minimum output voltage pulse (< 1 µs)	OUT	–0.8		
$V_{EN/UVLO}$	Maximum Enable pin voltage range	EN/UVLO	–0.3	6.5	V
V_{OV}	Maximum $\overline{EN}$/OVLO pin voltage range	$\overline{EN}$/OVLO	–0.3	6.5	V
V_{dVdT}	Maximum dVdT pin voltage range	dVdt	Internally limited		V
V_{PG}	Maximum PG pin voltage range	PG	–0.3	6.5	V
VPGTH	Maximum PGTH pin voltage range	PGTH	–0.3	6.5	V
V_{IMON}	Maximum IMON pin voltage range	IMON	Internally limited		V
I_{MAX}	Maximum continuous switch current	IN to OUT	10		A
T_J	Junction temperature		Internally limited		°C
T_{LEAD}	Maximum lead temperature			300	°C
T_{stg}	Storage temperature		–65	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

Parameter		Pin	MIN	MAX	UNIT
V_{IN}	Input voltage range	IN	2.7	16	V
V_{OUT}	Output voltage range	OUT		V_{IN}	V
$V_{EN/UVLO}$	EN/UVLO pin voltage range	EN/UVLO		5(1)	V
V_{OV}	$\overline{EN}$/OVLO pin voltage range	$\overline{EN}$/OVLO	0.5	1.5	V
V_{dVdT}	dVdT pin capacitor voltage rating	dVdt	V_{IN} + 5 V		V
V_{PGTH}	PGTH pin voltage range	PGTH		5	V
V_{PG}	PG pin voltage range	PG		5	V
I_{MAX}	Continuous switch current, T_J ≤ 125℃	IN to OUT		10	A
T_J	Junction temperature		–40	125	°C

(1) For supply voltages below 5 V, it is okay to pull up the EN pin to IN directly. For supply voltages greater than 5 V , TI recommends to use a resistor divider with minimum pullup resistor value of 350 kΩ.

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6.4 Thermal Information

THERMAL METRIC (1)		TPS25981xx RPW (QFN) 10 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	49.7(2)	°C/W
		71.8(3)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	15.7	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	2.1(2)	°C/W
	Junction-to-top characterization parameter	1.3(3)	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	23 (2)	°C/W
		14.5 (3)	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.
(2) Based on simulations conducted with the device mounted on a custom 4-layer PCB (2s2p) with 8 thermal vias under device.
(3) Based on simulations conducted with the device mounted on a JEDEC 4-layer PCB (2s2p) with no thermal vias under device.

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6.5 Electrical Characteristics

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, V_{OVLO} = 0 V, R_{IMON} = 600 Ω , dVdT = Open, PGTH = Open, PG = Open. All voltages referenced to GND.

Test Parameter	Description	MIN	TYP	MAX	UNITS
INPUT SUPPLY (IN)					
$I_{Q(ON)}$	IN supply quiescent current		381	470	µA
$I_{Q(OFF)}$	IN supply OFF state current ($V_{SD(F)}$ < V_{EN} < $V_{UVLO(F)}$)		68	90	µA
I_{SD}	IN supply shutdown current (V_{EN} < $V_{SD(F)}$)		3	25	µA
$V_{UVP(R)}$	IN supply UVP rising threshold	2.44	2.53	2.64	V
$V_{UVP(F)}$	IN supply UVP falling threshold	2.35	2.42	2.55	V
OUTPUT LOAD CURRENT MONITOR (IMON)					
G_{IMON}	Analog load current monitor gain (I_{MON} : I_{OUT}), I_{OUT} = 1.5 A, I_{OUT} < I_{LIM}	82.9	95.3	107.6	µA/A
	Analog load current monitor gain (I_{MON} : I_{OUT}), I_{OUT} = 3 A, I_{OUT} < I_{LIM}	87	95.3	104.5	µA/A
	Analog load current monitor gain (I_{MON} : I_{OUT}), I_{OUT} = 4.5 A, I_{OUT} < I_{LIM}	87.6	95.3	103.1	µA/A
	Analog load current monitor gain (I_{MON} : I_{OUT}), I_{OUT} = 8 A, I_{OUT} < I_{LIM}	87.7	95.3	102.6	µA/A
	Analog load current monitor gain (I_{MON} : I_{OUT}), I_{OUT} = 10 A, I_{OUT} < I_{LIM}	87.8	95.3	102.4	µA/A
SHORT-CIRCUIT PROTECTION (OUT)					
I_{FT}	Fixed fast-trip current threshold		39.5		A
ON RESISTANCE (IN - OUT)					
R_{ON}	2.7 ≤ V_{IN} ≤ 4 V, I_{OUT} = 3 A, T_J = 25°C		6.07		mΩ
	4 < V_{IN} ≤ 16 V, I_{OUT} = 3 A, T_J = 25°C		5.81		mΩ
	2.7 ≤ V_{IN} ≤ 16 V, I_{OUT} = 3 A, -40°C ≤ T_J ≤ 125°C			8.4	mΩ
ENABLE/UNDERVOLTAGE LOCKOUT (EN/UVLO)					
$V_{UVLO(R)}$	EN/UVLO rising threshold	1.176	1.20	1.224	V
$V_{UVLO(F)}$	EN/UVLO falling threshold	1.073	1.09	1.116	V
$V_{SD(F)}$	EN/UVLO falling threshold for lowest shutdown current	0.45	0.75		V
I_{ENLKG}	EN/UVLO pin leakage current	–0.1		0.1	µA
OVERVOLTAGE LOCKOUT ($\overline{EN}$/OVLO)					
$V_{OV(R)}$	OVLO rising threshold	1.176	1.20	1.224	V
$V_{OV(F)}$	OVLO falling threshold	1.074	1.09	1.116	V
I_{OVLKG}	OVLO pin leakage current (0.5 V < V_{OVLO} < 1.5 V)	–0.1		0.1	µA
POWER GOOD INDICATION (PG)					
V_{PGD}	PG pin voltage while de-asserted. V_{IN} < $V_{UVP(F)}$, V_{EN} < $V_{SD(F)}$, Weak pullup (I_{PG} = 26 µA)		0.66	0.80	V
	PG pin voltage while de-asserted. V_{IN} < $V_{UVP(F)}$, V_{EN} < $V_{SD(F)}$, Strong pullup (I_{PG} = 242 µA)		0.78	0.90	V
	PG pin voltage while de-asserted, V_{IN} > $V_{UVP(R)}$		0	0.60	V
I_{PGLKG}	PG pin leakage current, PG asserted			3	µA
POWER GOOD THRESHOLD (PGTH)					
$V_{PGTH(R)}$	PGTH rising threshold	1.178	1.20	1.224	V
$V_{PGTH(F)}$	PGTH falling threshold	1.071	1.09	1.116	V
$I_{PGTHLKG}$	PGTH leakage current	–1		1	µA
OVERTEMPERATURE PROTECTION (OTP)					
TSD	Thermal Shutdown rising threshold, T_J ↑		154		°C

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6.5 Electrical Characteristics (continued)

(Test conditions unless otherwise noted) –40°C ≤ T_J ≤ 125°C, V_{IN} = 12 V, OUT = Open, $V_{EN/UVLO}$ = 2 V, V_{OVLO} = 0 V, R_{IMON} = 600 Ω , dVdT = Open, PGTH = Open, PG = Open. All voltages referenced to GND.

Test Parameter	Description	MIN	TYP	MAX	UNITS
TSD_{HYS}	Thermal Shutdown hysteresis, T_J ↓		10		°C
DVDT					
I_{dVdt}	dVdt pin internal charging current	1.4	3.45	5.7	µA
QUICK OUTPUT DISCHARGE (OUT)					
R_{QOD}	Quick Output Discharge Resistance, V_{EN} < $V_{UVLO(F)}$	455	488	530	Ω

6.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{OVLO}	Overvoltage lock-out response time	V_{OVLO} > $V_{OV(R)}$ to V_{OUT} ↓		1.2		µs
t_{FT}	Fixed fast-trip response time	I_{OUT} > I_{FT} to I_{OUT} ↓		640		ns
t_{PGA}	PG assertion de-glitch time			14		µs
t_{PGD}	PG de-assertion de-glitch time			14		µs

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6.7 Switching Characteristics

The output rising slew rate is internally controlled and constant across the entire operating voltage range to ensure the turn on timing is not affected by the load conditions. The rising slew rate can be adjusted by adding capacitance from the dVdt pin to ground. As C_{dVdt} is increased it slows the rising slew rate (SR). See Slew Rate and Inrush Current Control (dVdt) section for more details. The Turn-Off Delay and Fall Time, however, are dependent on the RC time constant of the load capacitance (C_{OUT}) and Load Resistance (R_L). The Switching Characteristics are only valid for the power-up sequence where the supply is available in steady-state condition and the load voltage is completely discharged before the device is enabled. Typical values are taken at T_J = 25°C unless specifically noted otherwise. R_L = 100 Ω, C_{OUT} = 1 µF.

PARAMETER		V_{IN}	C_{dVdt} = Open	C_{dVdt} = 1800 pF	C_{dVdt} = 3300 pF	UNITS
SR_{ON}	Output rising slew rate	2.7 V	8.19	1.30	0.78	V/ms
		5 V	11.28	1.42	0.84	
		12 V	19.71	1.68	0.98	
$t_{D,ON}$	Turn-on delay	2.7 V	0.14	0.46	0.70	ms
		5 V	0.14	0.60	0.96	
		12 V	0.14	0.93	1.57	
t_R	Rise time	2.7 V	0.26	1.66	2.77	ms
		5 V	0.36	2.82	4.78	
		12 V	0.49	5.74	9.84	
t_{ON}	Turn-on time	2.7 V	0.40	2.11	3.47	ms
		5 V	0.50	3.42	5.74	
		12 V	0.63	6.67	11.41	
$t_{D,OFF}$	Turn-off delay	2.7 V	24.90	24.90	24.90	µs
		5 V	21.10	21.10	21.10	
		12 V	18.80	18.80	18.80	

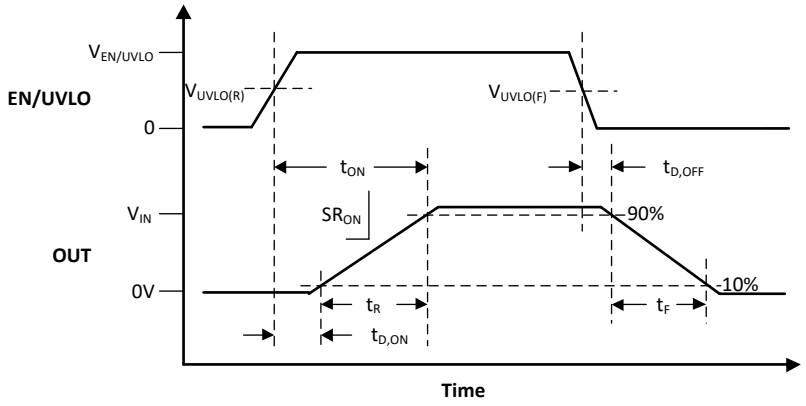

図 6-1. TPS22811x Switching Times

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6.8 Typical Characteristics

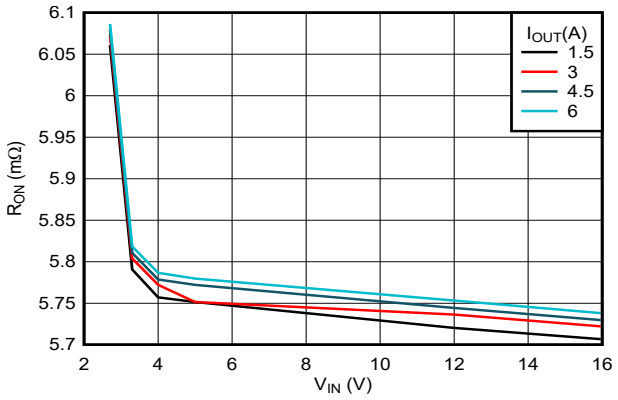

図 6-2. ON-Resistance vs Supply Voltage (T_A = 25°C)

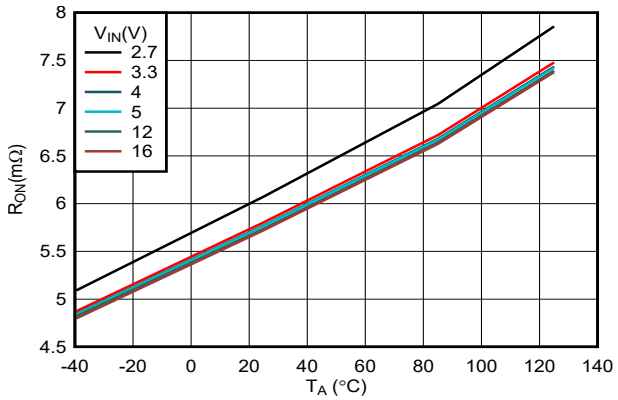

図 6-3. ON-Resistance vs Temperature (I_{OUT} = 3 A)

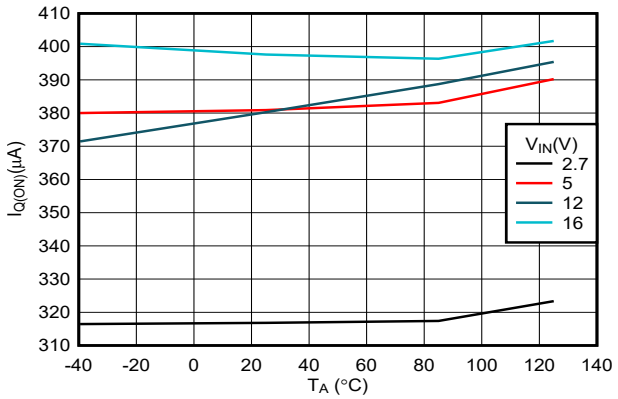

図 6-4. IN Quiescent Current vs Temperature

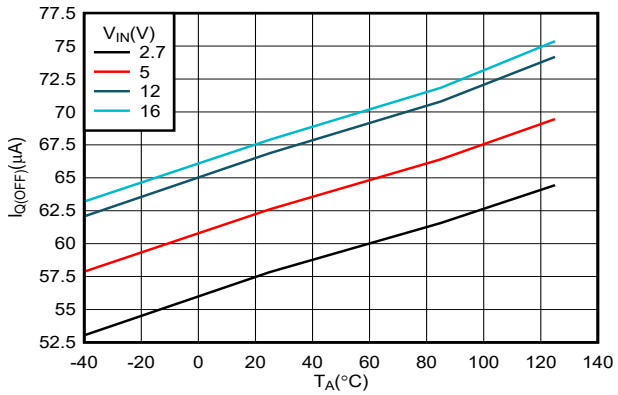

図 6-5. IN OFF State (UVLO) Current vs Temperature

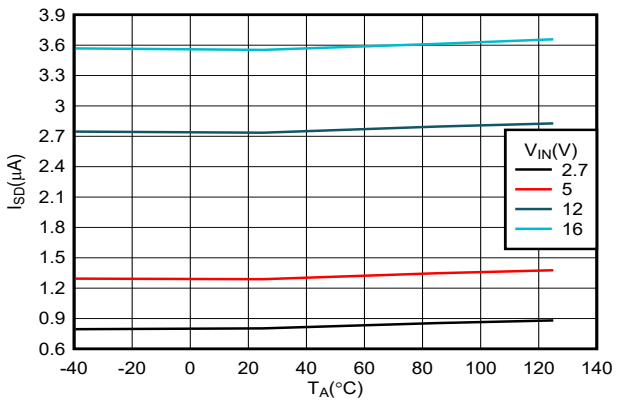

図 6-6. IN Shutdown Current vs Temperature

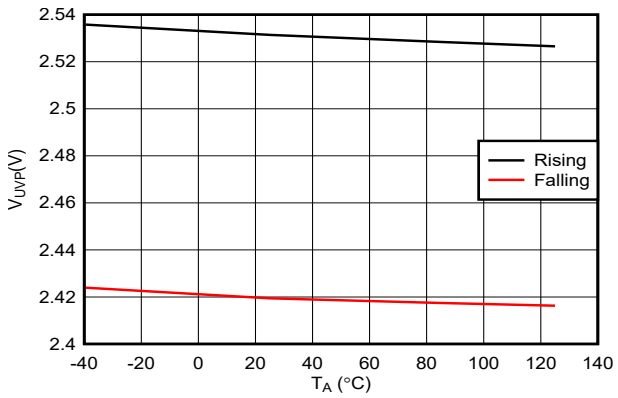

図 6-7. IN Undervoltage Threshold vs Temperature

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6.8 Typical Characteristics (continued)

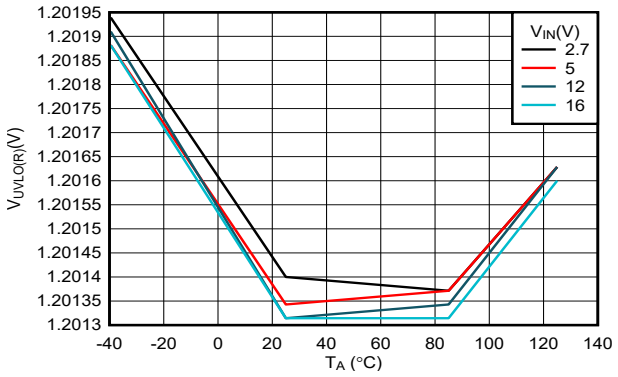

図 6-8. EN/UVLO Rising Threshold vs Temperature

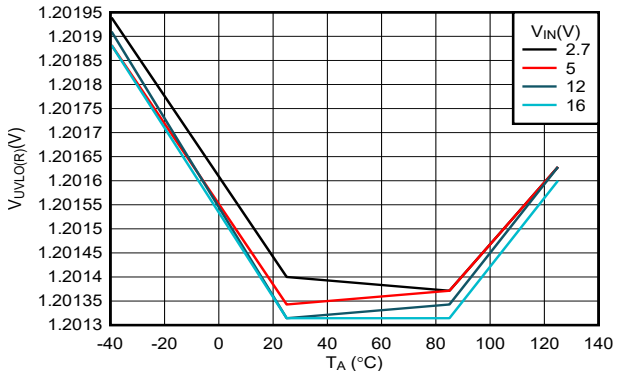

図 6-9. EN/UVLO Falling Threshold vs Temperature

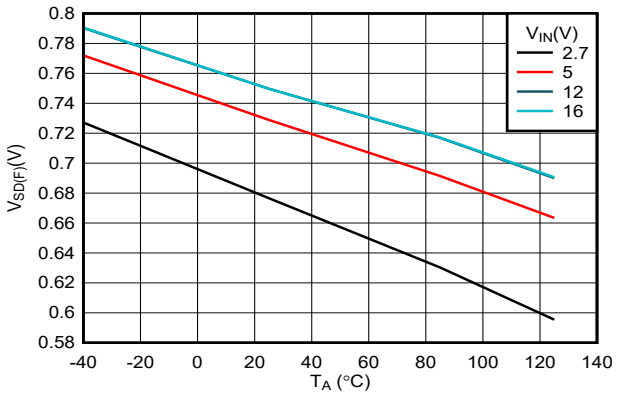

図 6-10. EN/UVLO Shutdown Falling Threshold vs Temperature

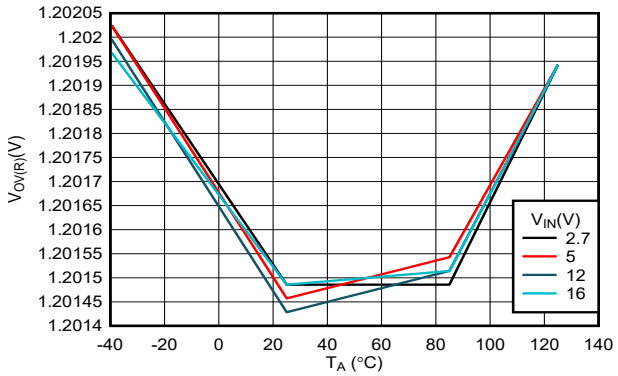

図 6-11. $\overline{EN}$/OVLO Rising Threshold vs Temperature

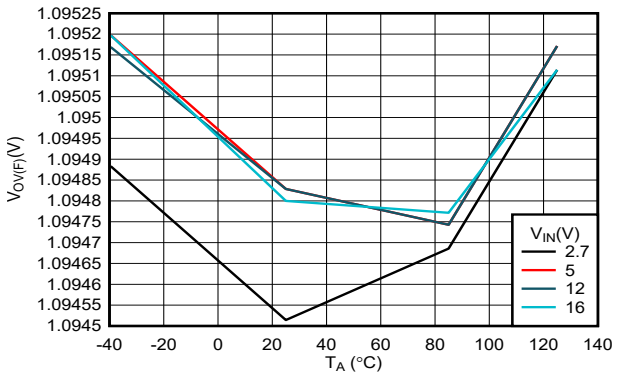

図 6-12. $\overline{EN}$/OVLO Falling Threshold vs Temperature

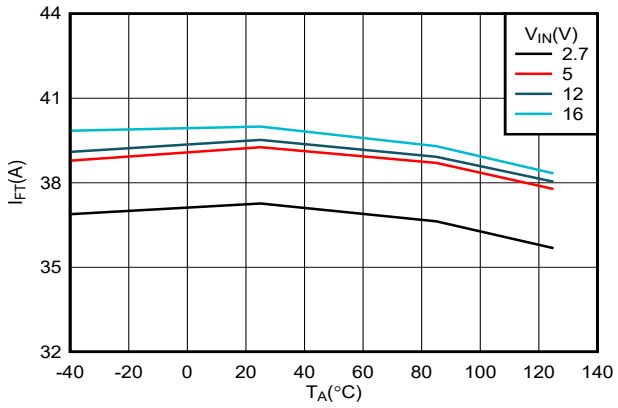

図 6-13. Fixed Fast-Trip Threshold vs Temperature

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6.8 Typical Characteristics (continued)

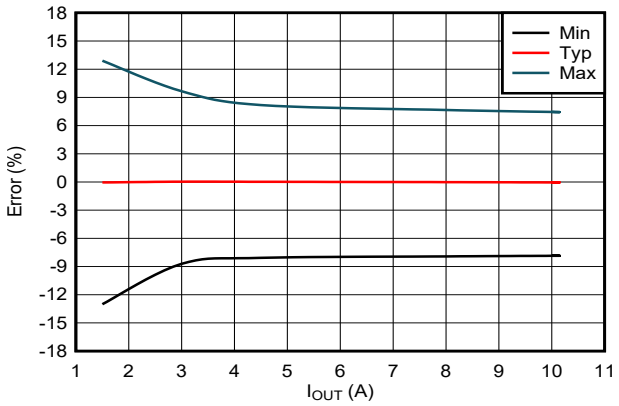


図 6-14. Analog Current Monitor Gain Accuracy

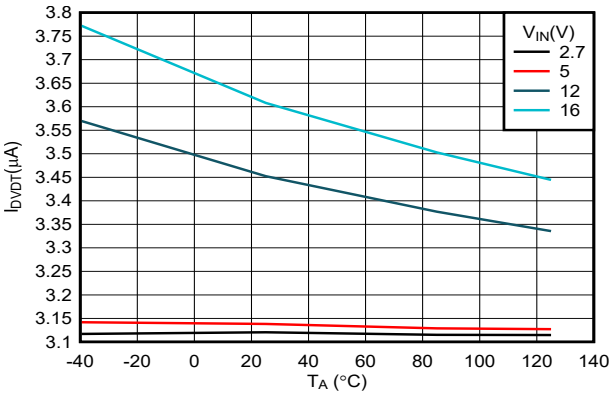


図 6-15. DVDT Charging Current vs Temperature

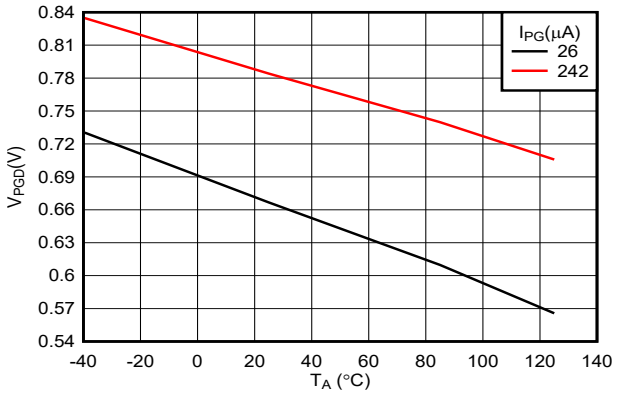


図 6-16. PG Pin Voltage vs Temperature (VIN = 0 V)

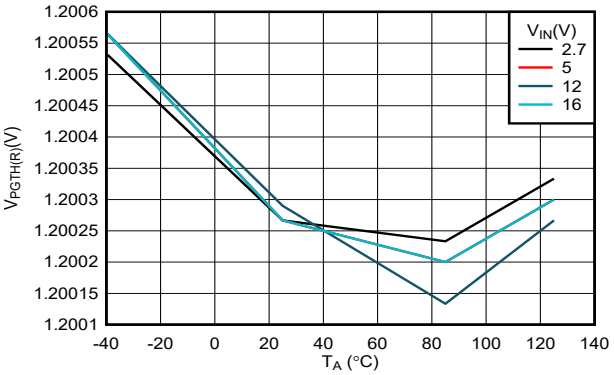


図 6-17. PGTH Rising Threshold vs Temperature

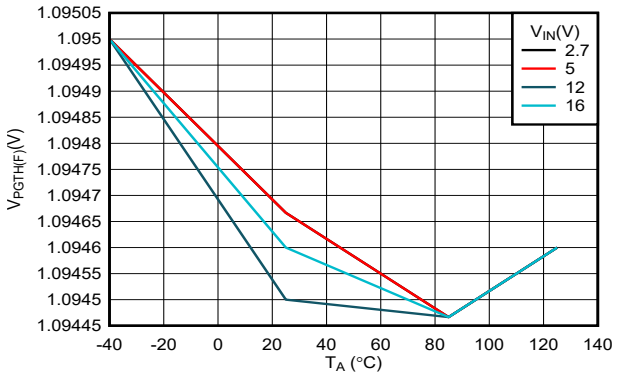


図 6-18. PGTH Falling Threshold vs Temperature

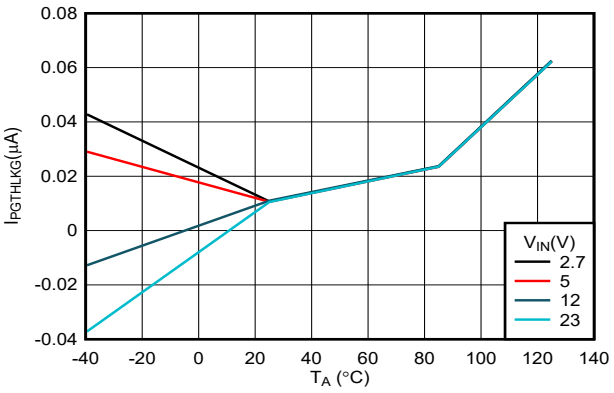


図 6-19. PGTH Pin Leakage Current vs Temperature

6.8 Typical Characteristics (continued)

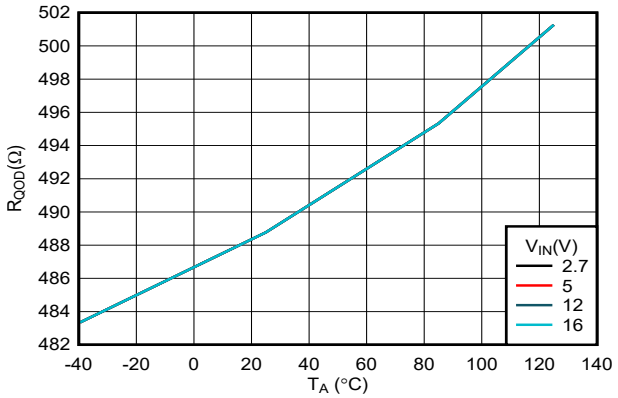


図 6-20. Quick Output Discharge Resistance vs Temperature

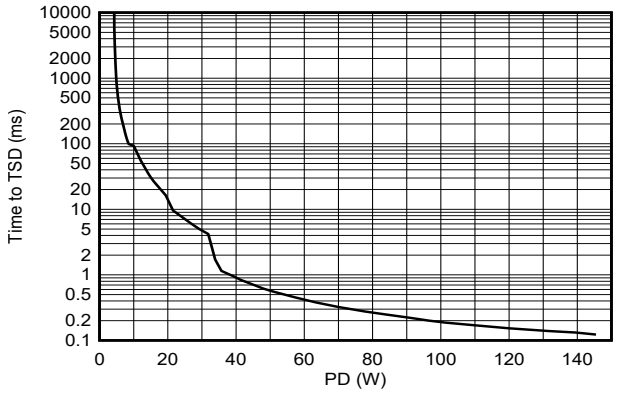


図 6-21. Time to Thermal Shutdown During Inrush State

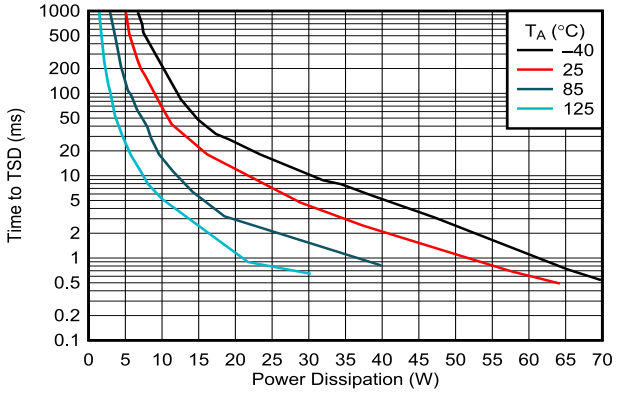
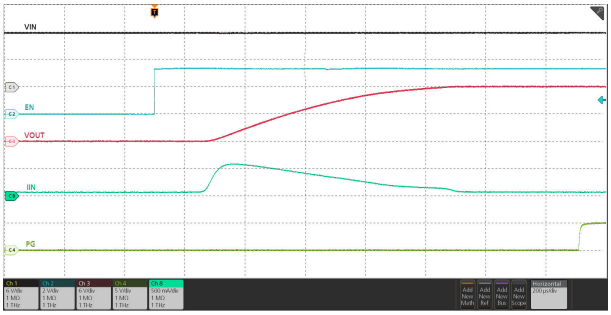
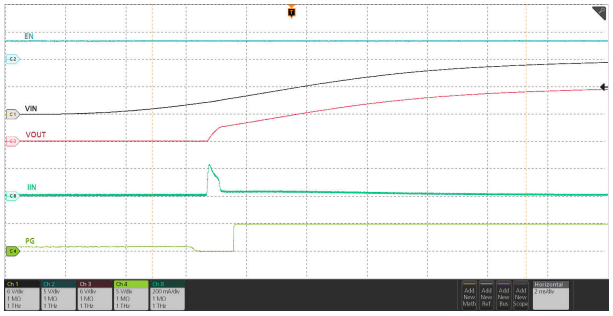


図 6-22. Time to Thermal Shutdown During Steady-State



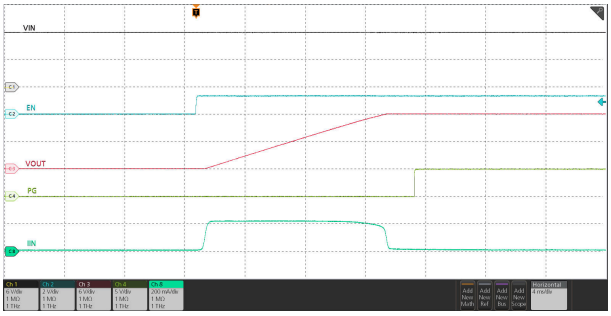
V_{IN} = 12 V, C_{OUT} = 10 µF, C_{dVdt} = Open, $V_{EN/UVLO}$ stepped up to 3.3 V

図 6-23. Start-Up with Enable



$V_{EN/UVLO}$ = 3.3 V, C_{OUT} = 10 µF, C_{dVdt} = Open, V_{IN} ramped up to 12 V

図 6-24. Start- Up with Supply



V_{IN} = 12 V, C_{OUT} = 220 µF, C_{dVdt} = 3300 pF, $V_{EN/UVLO}$ stepped up to 1.4 V

図 6-25. Inrush Current with Capacitive Load

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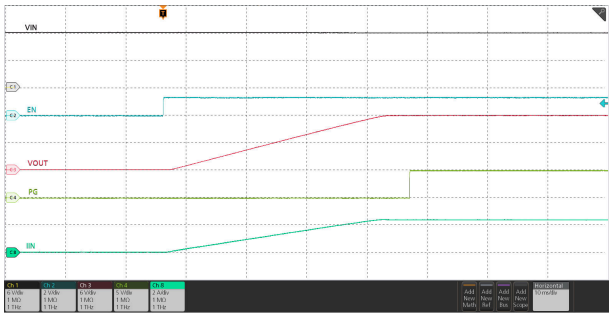
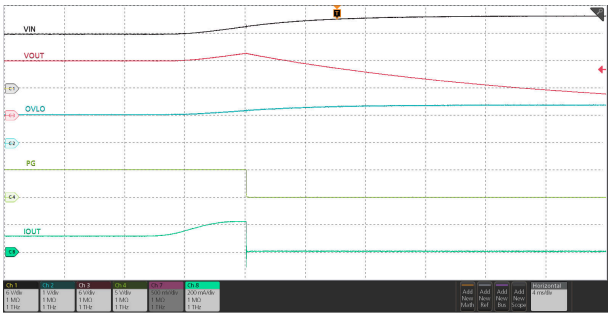
6.8 Typical Characteristics (continued)



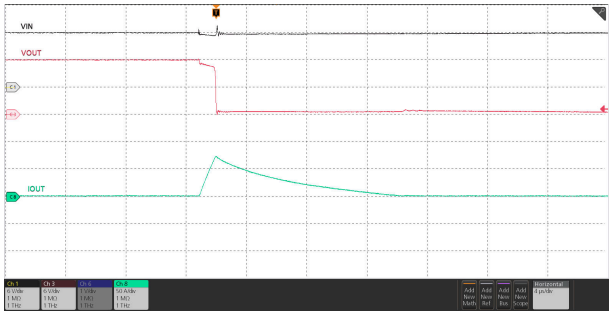
V_{IN} = 12 V, C_{OUT} = 220 µF, R_{OUT} = 5 Ω, C_{dVdt} = 3300 pF, $V_{EN/UVLO}$ stepped up to 1.4 V

図 6-26. Inrush Current with Resistive and Capacitive Load



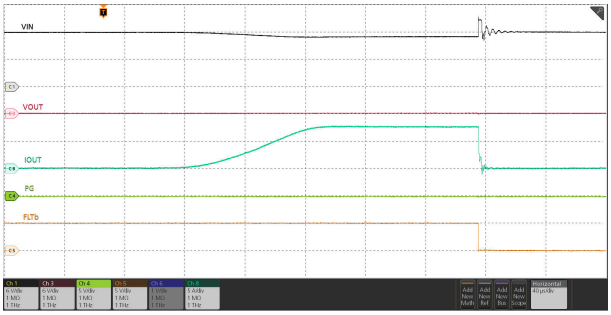
V_{IN} Overvoltage threshold set to 13.6 V using resistor ladder connected on OVLO pin, V_{IN} ramped up from 12 V to 16 V

図 6-27. Overvoltage Lockout Response



V_{IN} = 12 V, OUT stepped from open → short circuit to GND

図 6-28. Output Short Circuit During Steady-State (Zoomed In)



V_{IN} = 12 V, C_{OUT} = Open, OUT short circuit to GND, R_{IMON} = 649 Ω, $V_{EN/UVLO}$ stepped from 0 V to 3.3 V

図 6-29. Power Up into Short-Circuit

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7 Detailed Description

7.1 Overview

TPS22811x is an integrated load switch with protection and monitoring. The device starts its operation by monitoring the IN bus. When the input supply voltage (V_{IN}) exceeds the undervoltage protection threshold (V_{UVP}), the device samples the EN/UVLO pin. A high level (> V_{UVLO}) on this pin enables the internal power path to start conducting and allow current to flow from IN to OUT. When EN/UVLO is held low (< V_{UVLO}), the internal power path is turned off.

After a successful start-up sequence, the device now actively monitors its load current and input voltage, and controls the internal FET to ensure that the fast-trip current threshold is not exceeded and overvoltage spikes are cut-off after they cross the user adjustable overvoltage lockout threshold (V_{OVLO}). This feature keeps the system safe from harmful levels of voltage and current.

The device also has a built-in thermal sensor based shutdown mechanism to protect itself in case the device temperature (T_J) exceeds the recommended operating conditions.

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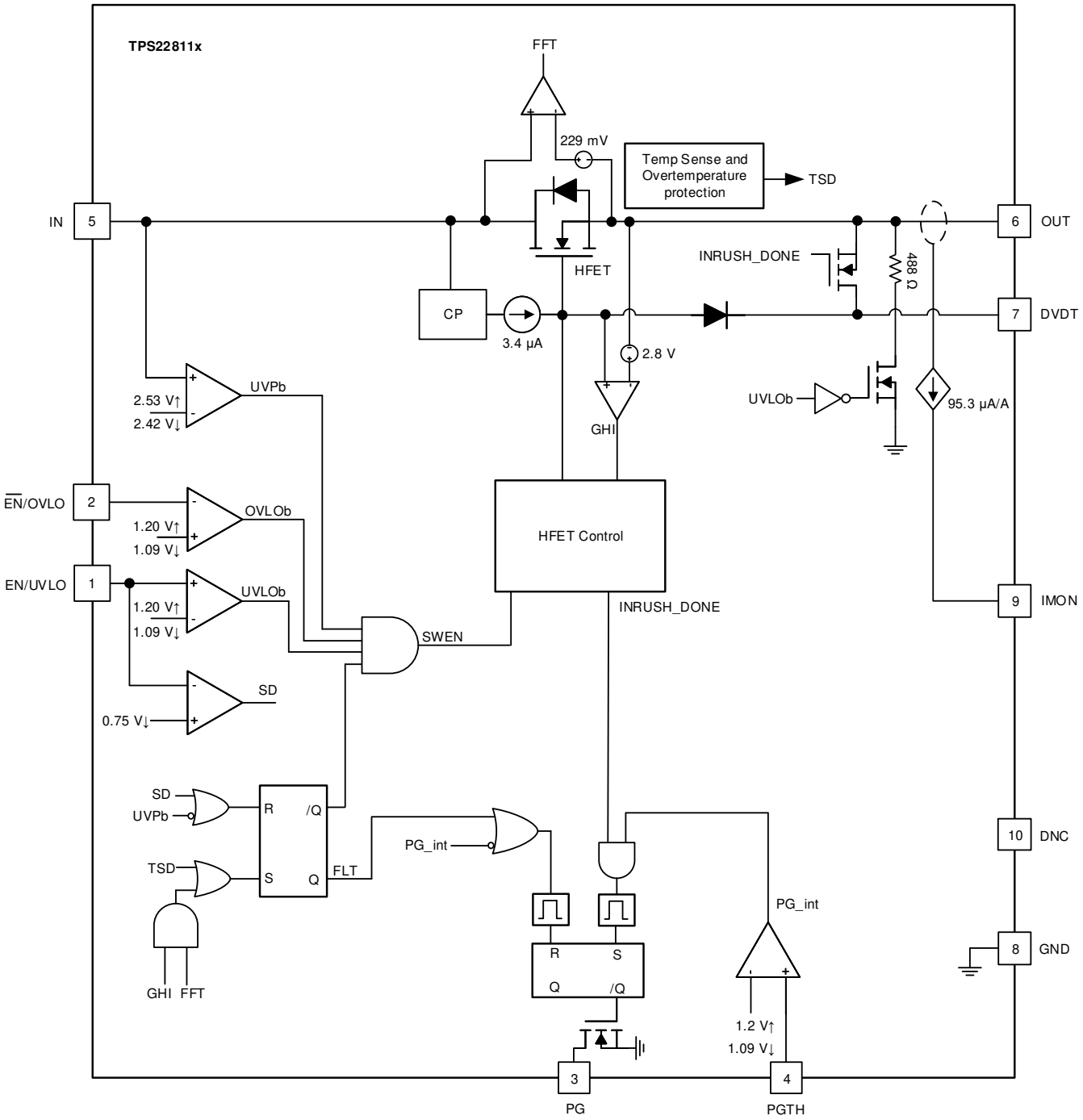
7.2 Functional Block Diagram



7.3 Feature Description

The TPS22811x eFuse is a compact, feature rich power management device that provides detection, protection and indication in the event of system faults.

7.3.1 Undervoltage Lockout (UVLO and UVP)

The TPS22811x implements undervoltage protection on IN in case the applied voltage becomes too low for the system or device to properly operate. The undervoltage protection has a default lockout threshold of V_{UVP} which is fixed internally. Also, the UVLO comparator on the EN/UVLO pin allows the undervoltage protection threshold to be externally adjusted to a user defined value. 図 7-1 and 式 1 show how a resistor divider can be used to set the UVLO set point for a given voltage supply.

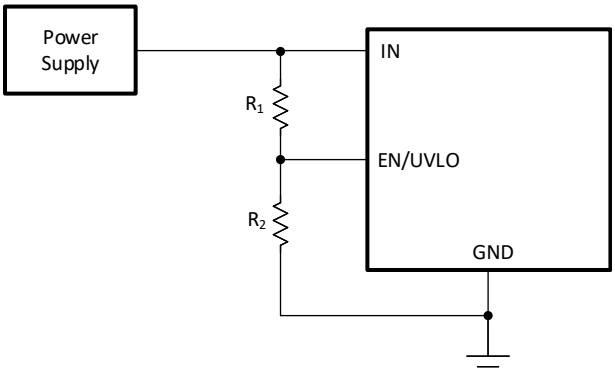


図 7-1. Adjustable Undervoltage Protection

$$V_{IN(UV)} = \frac{V_{UVLO} \times (R_1 + R_2)}{R_2} \quad (1)$$

7.3.2 Overvoltage Lockout (OVLO)

The TPS22811x allows the user to implement overvoltage lockout to protect the load from input overvoltage conditions. The OVLO comparator on the $\overline{EN}$/OVLO pin allows the overvoltage protection threshold to be adjusted to a user defined value. After the voltage at the $\overline{EN}$/OVLO pin crosses the OVLO rising threshold $V_{OV(R)}$, the device turns off the power to the output. Thereafter, the devices wait for the voltage at the $\overline{EN}$/OVLO pin to fall below the OVLO falling threshold $V_{OV(F)}$ before the output power is turned ON again. The rising and falling thresholds are slightly different to provide hysterisis. 図 7-2 and 式 2 show how a resistor divider can be used to set the OVLO set point for a given voltage supply.

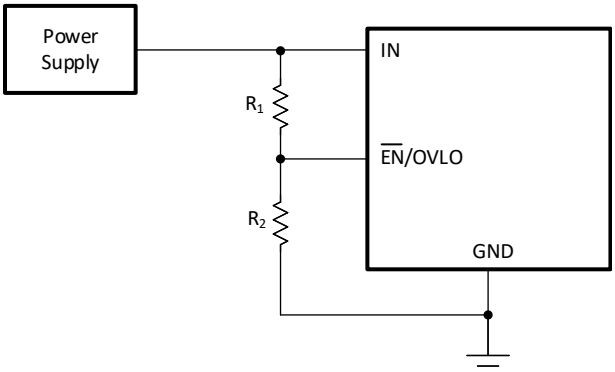


図 7-2. Adjustable Overvoltage Protection

$$V_{IN(OV)} = \frac{V_{OV} \times (R_1 + R_2)}{R_2} \quad (2)$$

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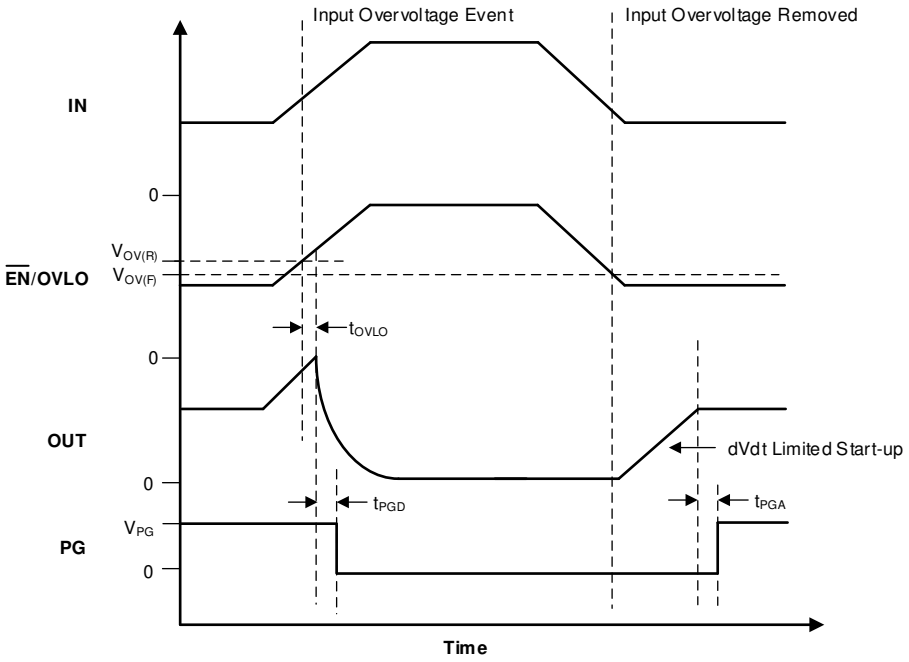

図 7-3. TPS22811x Overvoltage Lockout and Recovery

While recovering from a OVLO event, the TPS22811x starts up with inrush control (dVdt).

7.3.3 Inrush Current, Overcurrent, and Short-Circuit Protection

TPS22811x incorporates three levels of protection against overcurrent:

1. Adjustable slew rate (dVdt) for inrush current control
2. Fixed threshold (I_{FT}) for fast-trip response to quickly protect against hard output short circuits during steady-state
3. Adjustable current limit (I_{LIM}) for protection against overcurrent or short circuit during start-up

7.3.3.1 Slew Rate (dVdt) and Inrush Current Control

During hot-plug events or while trying to charge a large output capacitance at start-up, there can be a large inrush current. If the inrush current is not managed properly, it can damage the input connectors and cause the system power supply to droop leading to unexpected restarts elsewhere in the system. The inrush current during turn on is directly proportional to the load capacitance and rising slew rate. 式 3 can be used to find the slew rate (SR) required to limit the inrush current (I_{INRUSH}) for a given load capacitance (C_{OUT}):

$$SR\left(\frac{V}{ms}\right) = \frac{I_{INRUSH}\,(mA)}{C_{OUT}\,(\mu F)} \tag{3}$$

A capacitor can be connected to the dVdt pin to control the rising slew rate and lower the inrush current during turn on. Use 式 4 to calculate the required C_{dVdt} capacitance to produce a given slew rate.

$$C_{dVdt}\,(pF) = \frac{3300}{SR\left(\frac{V}{ms}\right)} \tag{4}$$

The fastest output slew rate is achieved by leaving the dVdt pin open.

注

For C_{dVdt} > 10 nF, TI recommends to add a 100-Ω resistor in series with the capacitor on the dVdt pin.

7.3.3.2 Short-Circuit Protection

During an output short-circuit event, the current through the device increases very rapidly. When a severe overcurrent condition is detected, the TPS22811x triggers a fast-trip response to cut off the power path. The device employs a fixed fast-trip threshold (I_{FT}) to protect fast protection against hard short circuits during steady-state. After the current exceeds I_{FT}, the FET is turned off completely within t_{FT}. Thereafter, the device remains off till the device is power cycled or re-enabled using EN/UVLO pin.

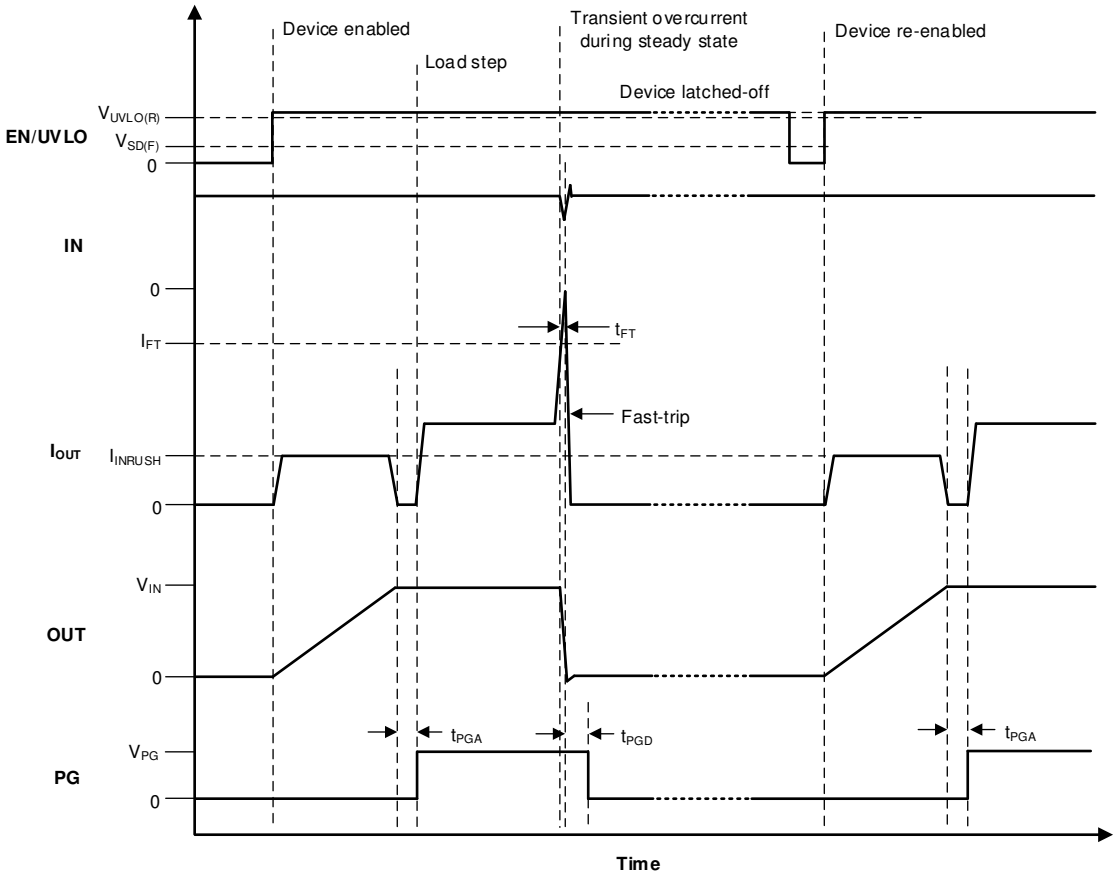

図 7-4. TPS22811x Short-Circuit Response

7.3.3.3 Active Current Limiting During Start-Up

The TPS22811x devices respond to output overcurrent conditions during start-up by actively limiting the current. If the load current exceeds the set overcurrent threshold (I_{LIM}) set by the IMON pin resistor (R_{IMON}), but stays lower than the fast-trip threshold (I_{FT}), the current limit loop starts regulating the FET to actively limit the current to the set overcurrent threshold (I_{LIM}). 式 5 can be used to calculate the R_{IMON} value for a desired overcurrent threshold.

$$R_{IMON}\,(\Omega) = \frac{6595}{I_{LIM}\,(A)} \tag{5}$$

注

1. Leaving the IMON pin open sets the current limit to nearly zero and results in the part entering current limit with the slightest amount of loading at the output.
2. The current limit circuit employs a foldback mechanism. The current limit threshold in the foldback region (0 V < V_{OUT} < V_{FB}) is lower than the target current limit threshold (I_{LIM}).
3. Connecting the IMON pin to GND disables the active current limit protection during start-up.

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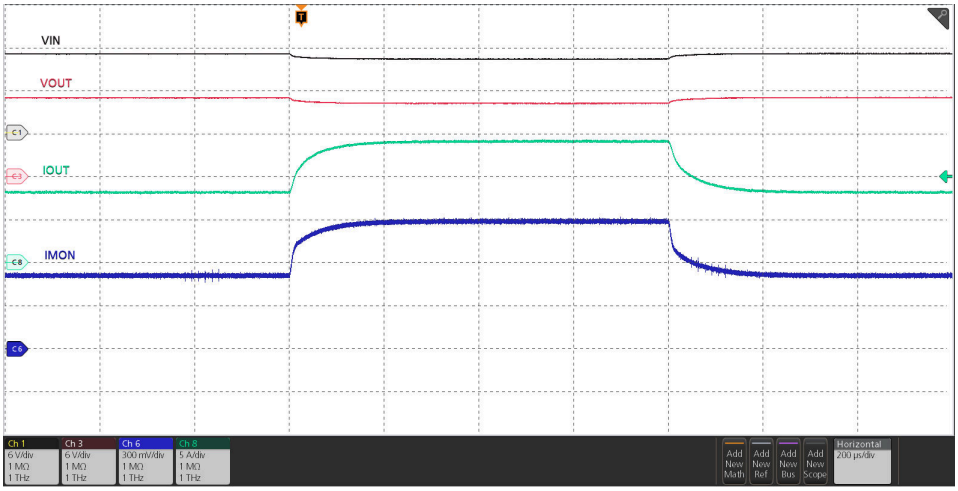
During active current limit, the output voltage drops, resulting in increased device power dissipation across the FET. If the device internal temperature (T_J) exceeds the thermal shutdown threshold (TSD), the FET is turned off. After the part shuts down due to TSD fault, it stays latched off. For more details on device response to overtemperature, see *Overtemperature Protection (OTP)*.

7.3.4 Analog Load Current Monitor

The TPS22811x allows the system to accurately monitor the output load current by providing an analog current sense output on the IMON pin which is proportional to the current through the FET. The user can sense the voltage (V_{IMON}) across the R_{IMON} to get a measure of the output load current.

$$I_{LOAD}\,(A) = \frac{V_{IMON}\,(\mu V)}{G_{IMON}\,(\mu A/A) \times R_{IMON}\,(\Omega)} \tag{6}$$

The waveform below shows the IMON signal response to a load step at the output.



V_{IN} = 12 V, R_{IMON} = 649 Ω, I_{OUT} varied dynamically between 8 A and 14 A

図 7-5. Analog Load Current Monitor Response

7.3.5 Overtemperature Protection (OTP)

The device monitors the internal die temperature (T_J) at all times and shuts down the part as soon as the temperature exceeds a safe operating level (TSD) thereby protecting the device from damage. The device does turn back on until the junction cools down sufficiently, that is the die temperature falls below (TSD – TSD_{HYS}).

When the TPS22811x detects thermal overload, it shuts down and remains latched-off until the device is power cycled or re-enabled.

表 7-1. Thermal Shutdown

Enter TSD	Exit TSD
$T_J \geq$ TSD	$T_J <$ TSD – TSD_{HYS} V_{IN} cycled to 0 V and then above $V_{UVP(R)}$ or EN/UVLO toggled below $V_{SD(F)}$

7.3.6 Fault Response

The following table summarizes the device response to various fault conditions.

表 7-2. Fault Summary

Event	Protection Response	Fault Latched Internally
Overtemperature	Shutdown	Y
Undervoltage (UVP or UVLO)	Shutdown	N
Input overvoltage	Shutdown	N
Output short circuit to GND	Fast-trip	Y

Faults which are latched internally can be cleared either by power cycling the part (pulling V_{IN} to 0 V) or by pulling the EN/UVLO pin voltage below V_{SD}.

During a latched fault, pulling the EN/UVLO just below the UVLO threshold has no impact on the device.

7.3.7 Power-Good Indication (PG)

The TPS22811x provides an active high digital output (PG) which serves as a power-good indication signal and is asserted high depending on the voltage at the PGTH pin along with the device state information. The PG is an open-drain pin and must be pulled up to an external supply.

After power up, PG is pulled low initially. The device initiates a inrush sequence in which the HFET is turned on in a controlled manner. When the HFET gate voltage reaches the full overdrive indicating that the inrush sequence is complete and the voltage at PGTH is above $V_{PGTH(R)}$, the PG is asserted after a de-glitch time (t_{PGA}).

PG is de-asserted if at any time during normal operation, the voltage at PGTH falls below $V_{PGTH(F)}$, or the device detects a fault (except overcurrent). The PG de-assertion de-glitch time is t_{PGD}.

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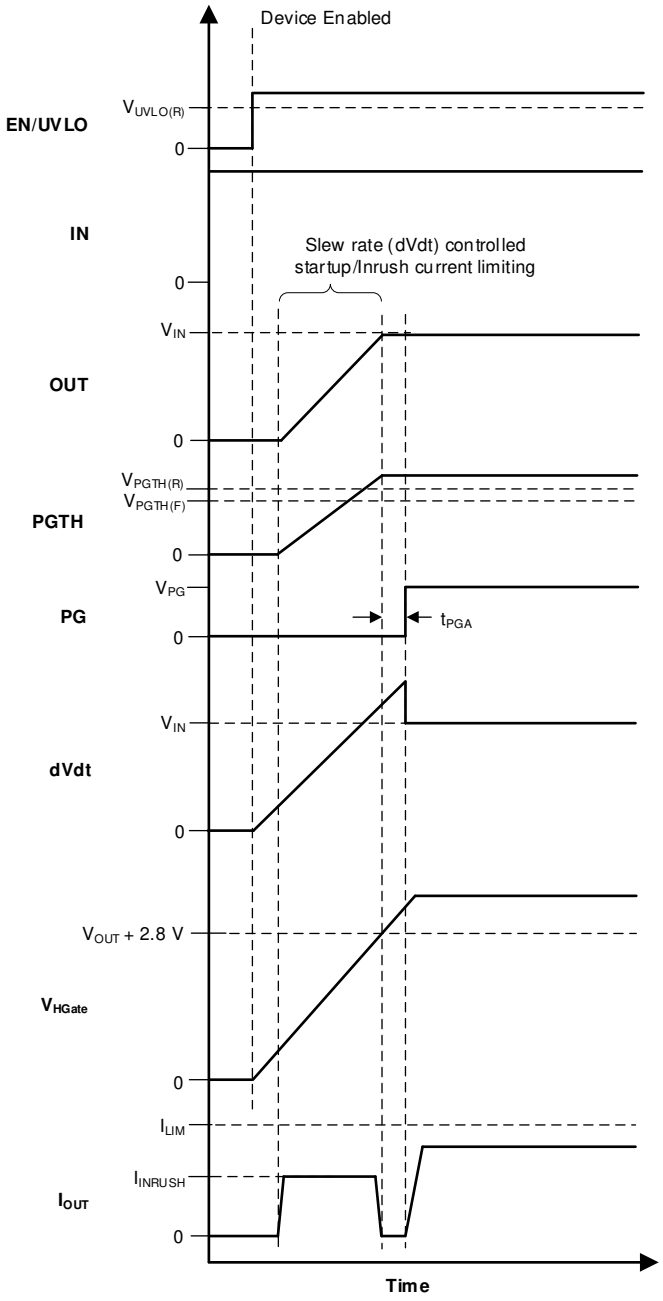

図 7-6. TPS22811xx PG Timing Diagram

表 7-3. TPS22811x PG Indication Summary

Event	Protection Response	PG Pin	PG Delay
Undervoltage (UVP or UVLO)	Shutdown	L	
Overvoltage (OVLO)	Shutdown	L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGD}
Steady-state	NA	H (If PGTH pin voltage > $V_{PGTH(R)}$) L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGA} t_{PGD}
Output short circuit to GND	Fast-trip followed by current limit	H (If PGTH pin voltage > $V_{PGTH(R)}$) L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGA} t_{PGD}
Overtemperature	Shutdown	L (If PGTH pin voltage < $V_{PGTH(F)}$)	t_{PGD}

When there is no supply to the device, the PG pin is expected to stay low. However, there is no active pulldown in this condition to drive this pin all the way down to 0 V. If the PG pin is pulled up to an independent supply which is present even if the device is unpowered, there can be a small voltage seen on this pin depending on the pin sink current, which is a function of the pullup supply voltage and resistor. Minimize the sink current to keep this pin voltage low enough not to be detected as a logic HIGH by associated external circuits in this condition.

7.3.8 Quick Output Discharge (QOD)

The TPS22811x has an integrated output discharge function which can be helpful in quickly removing residual charge left on the large output capacitors and avoids bus floating at some undefined voltage. The internal QOD pulldown FET on the OUT pin is activated when the EN/UVLO is held low ($V_{EN} < V_{UVLO(F)}$). The output discharge function can result in excess power dissipation inside the device leading to increase in junction temperature. The output discharge is disabled if the junction temperature (T_J) crosses the thermal shutdown threshold (TSD) to avoid long term degradation of the part.

7.4 Device Functional Modes

The device has one mode of operation that applies when operated within the Recommended Operating Conditions.

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8 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The TPS22811x is a 2.7-V to 16-V, 10-A load switch that is typically used for power rail protection applications. The device operates from 2.7 V to 16 V with adjustable overvoltage and undervoltage protection. The device provides ability to control inrush current. The device can be used in a variety of systems such as server motherboard/add-on cards/NIC, optical modules, enterprise switches/routers, Industrial PC, UHDTV. The design procedure explained in the subsequent sections can be used to select the supporting component values based on the application requirement. Additionally, a spreadsheet design tool, *TPS22811xx Design Calculator*, is available in the web product folder.

8.1.1 Single Device, Self-Controlled

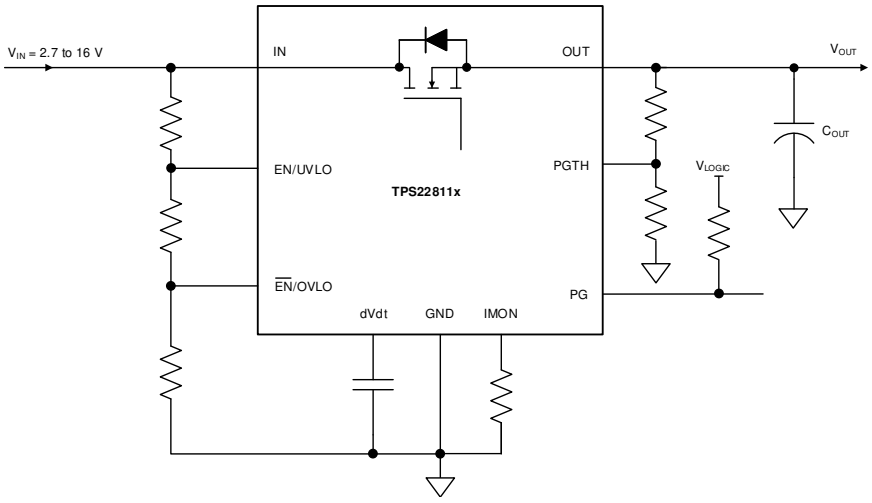

図 8-1. Single Device, Self-Controlled

Other variations:

In a Host MCU controlled system, EN/UVLO or OVLO can also be driven from the host GPIO to control the device.

IMON pin can be connected to the MCU ADC input for current monitoring purpose.

8.1.2 Parallel Operation

Applications which need higher steady current can use two TPS22811x devices connected in parallel as shown in 図 8-2 below. In this configuration, the first device turns on initially to provide the inrush current limiting. The second device is held in an OFF state by driving its EN/UVLO pin low using the PG signal of the first device. After the inrush sequence is complete, the first device asserts its PG pin high and turns on the second device. The second device asserts its PG signal to indicate when it has turned on fully, thereby indicating to the system that the parallel combination is ready to deliver the full steady-state current.

After in steady-state, both devices share current nearly equally. There can be a slight skew in the currents depending on the part-to-part variation in the R_{ON} as well as the PCB trace resistance mismatch.

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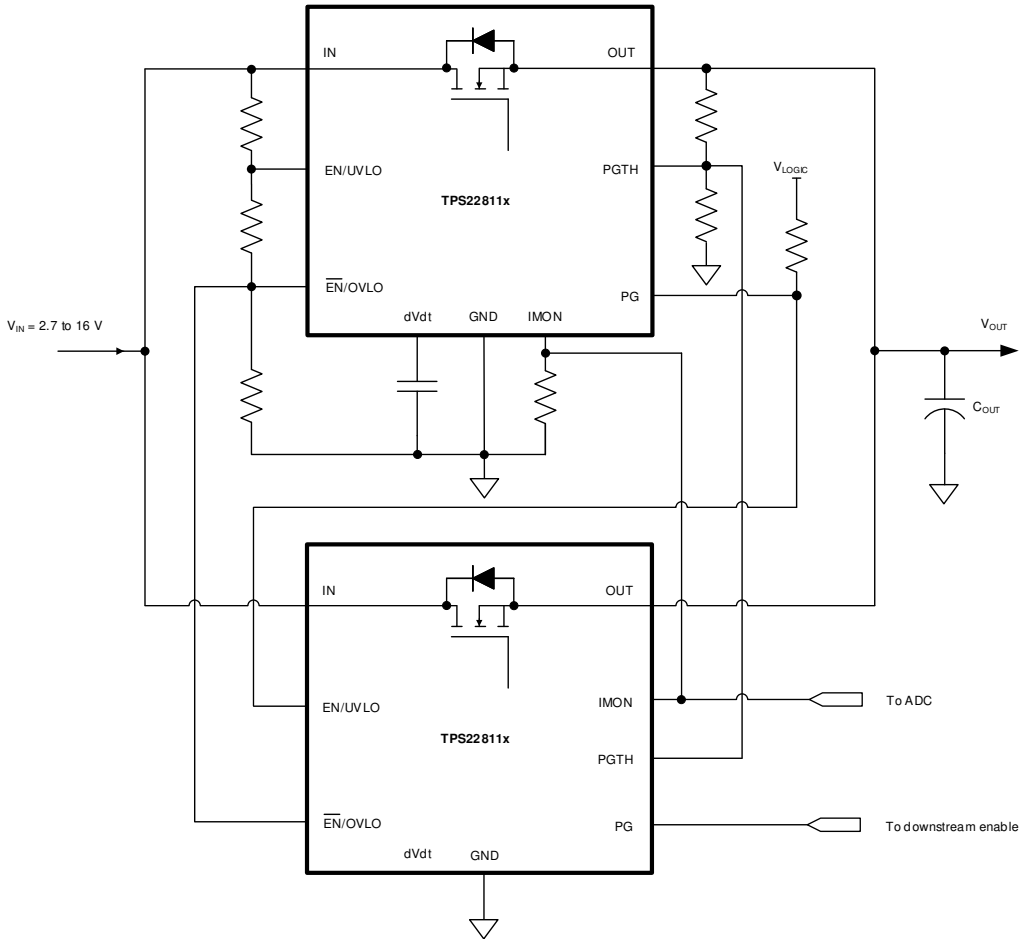

図 8-2. Two Devices Connected in Parallel for Higher Steady-State Current Capability

The waveforms below illustrate the behavior of the parallel configuration during start-up as well as during steady-state.

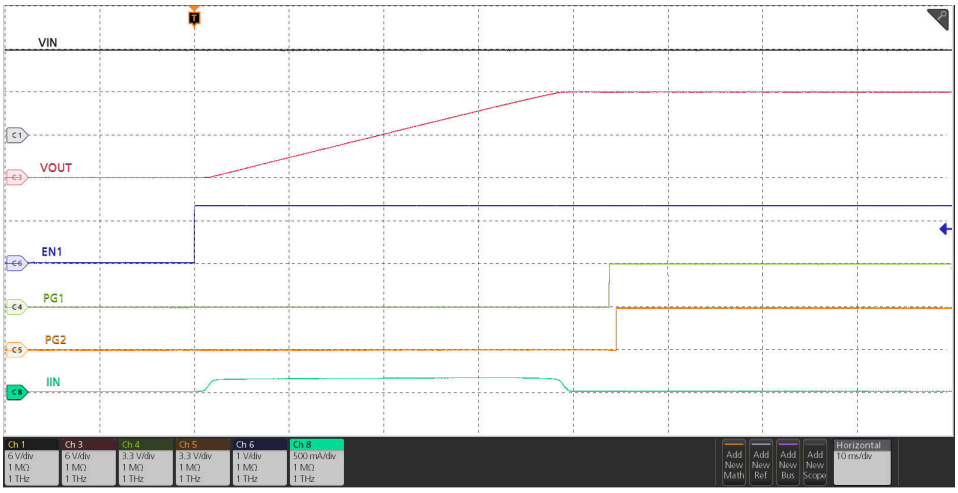

図 8-3. Parallel Devices Sequencing During Start-Up

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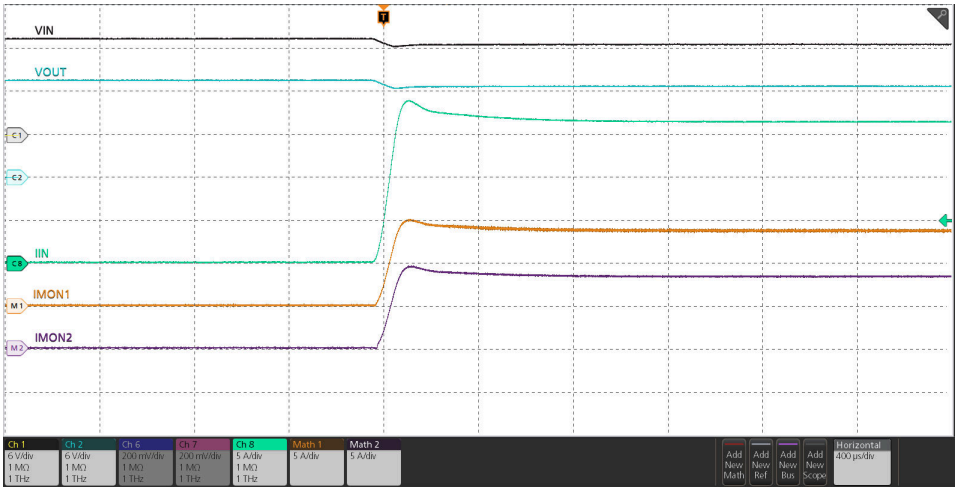


図 8-4. Parallel Devices Load Current During Steady-State

8.2 Typical Application

The TPS22811 device can be used in an industrial PC for input power protection of PCIe card. Industrial PCs provide flexible PCIe expansion slots with different combination of PCIe x16, PCIe x4 and PCI. PCIe x16 slot draws maximum current of up to 5.5 A from on board a 12-V rail. Load switch devices like TPS22811 can support the power requirements of these PCIe expansion slots and can be used for switching 12-V supply to PCIe card. During plugging or unplugging the PCIe card power pin of PCIe slot can short to ground that can cause the 12-V rail to droop or even damage the power tree due to very high current draw. The TPS22811 device can quickly respond to fault events like short circuit and isolate supply from load side thus preventing supply from drooping. The controlled rise time for the device greatly reduces inrush current caused by large bulk load capacitances, thereby reducing or eliminating power-supply droop.

The TPS22811 device can also be used for switching the 12-V bulk power rail of DDR5 DIMM. The PG pin of TPS22811 device can be used to enable downstream DC-DC converters after the 12-V rail is fully up.

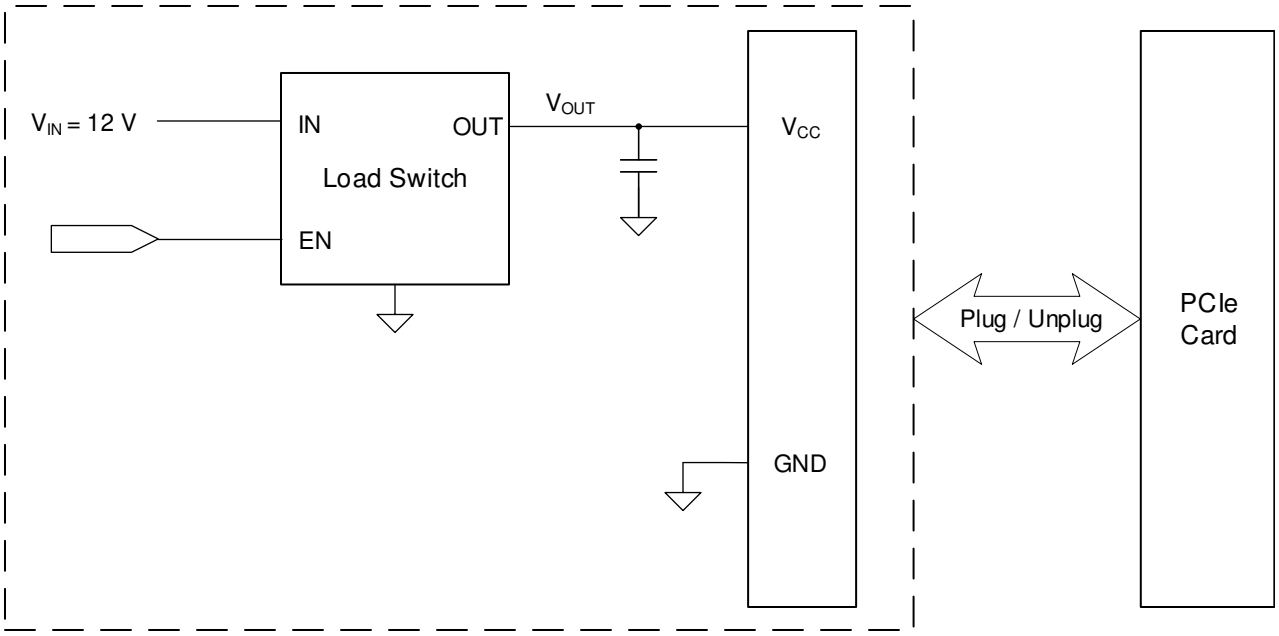
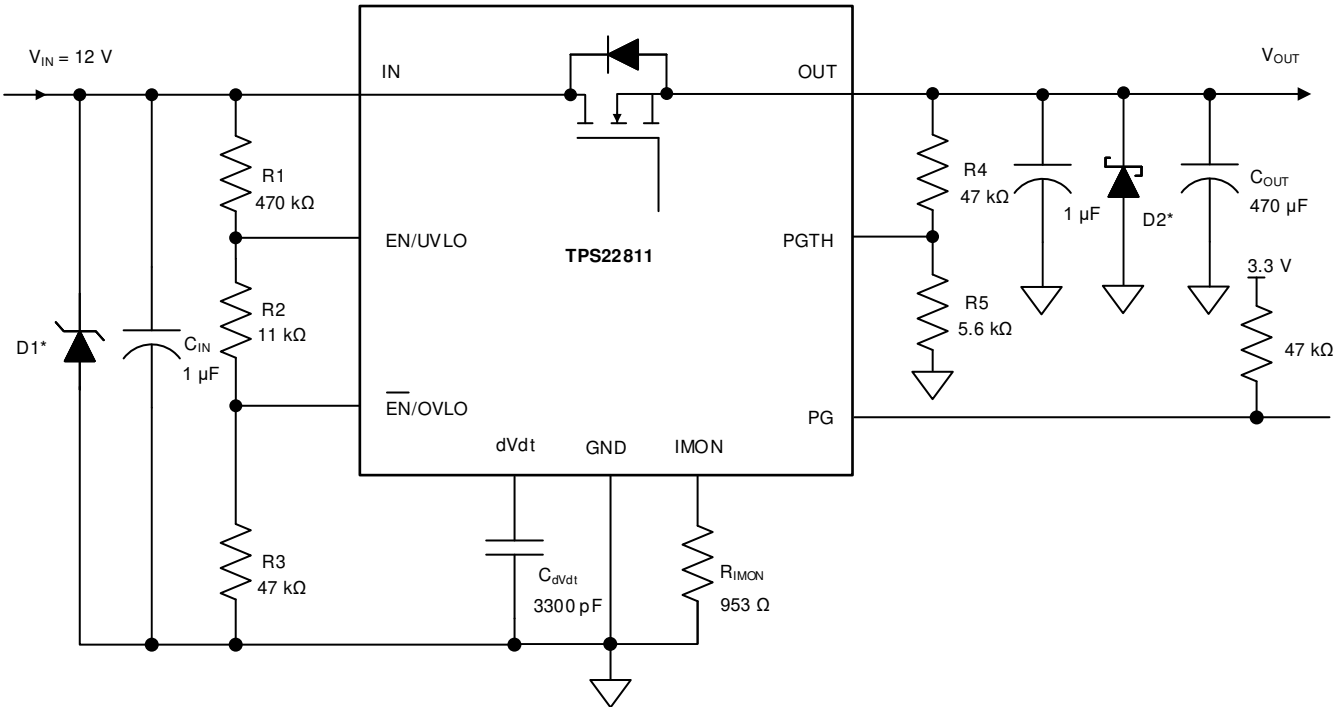


図 8-5. Power Path Protection Block Diagram of a Typical PCIe Slot



* Optional circuit components needed for transient protection depending on input and output inductance. Please refer to *Transient Protection* section for details.

図 8-6. PCIe Expansion Slot Protection

8.2.1 Design Requirements

表 8-1. Design Parameters

PARAMETER	VALUE
Input supply voltage (V_{IN})	12 V
Undervoltage threshold ($V_{IN(UV)}$)	10.8 V
Overvoltage threshold ($V_{IN(OV)}$)	13.2 V
Output power-good threshold (V_{PG})	11.4 V
Maximum continuous current	5.5 A
Analog load current monitor voltage range ($V_{IMONmax}$)	0.5 V
Output capacitance (C_{OUT})	470 µF
Output rise time (t_R)	12 ms

8.2.2 Detailed Design Procedure

8.2.2.1 Setting Undervoltage and Overvoltage Thresholds

The supply undervoltage and overvoltage thresholds are set using the resistors R1, R2 and R3. Use 式 7 and 式 8 to calculate these values:

$$V_{IN(UV)} = \frac{V_{UVLO(R)} \times \left(R_1 + R_2 + R_3\right)}{R_2 + R_3} \quad (7)$$

$$V_{IN(OV)} = \frac{V_{OV(R)} \times \left(R_1 + R_2 + R_3\right)}{R_3} \quad (8)$$

Where $V_{UVLO(R)}$ is the UVLO rising threshold and $V_{OV(R)}$ is the OVLO rising threshold. Because R1, R2 and R3 leak the current from input supply V_{IN}, these resistors must be selected based on the acceptable leakage current

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from input power supply V_{IN}. The current drawn by R1, R2 and R3 from the power supply is IR123 = V_{IN} / (R1 + R2 + R3). However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, IR123 must be chosen to be 20 times greater than the leakage current expected on the EN/UVLO and OVLO pins.

From the device electrical specifications, both the EN/UVLO and OVLO leakage currents are 0.1 µA (maximum), $V_{OV(R)}$ = 1.2 V and $V_{UVLO(R)}$ = 1.2 V. From design requirements, $V_{IN(OV)}$ = 13.2 V and $V_{IN(UV)}$ = 10.8 V. To solve the equation, first choose the value of R1 = 470 kΩ and use the above equations to solve for R2 = 10.7 kΩ and R3 = 48 kΩ.

Using the closest standard 1% resistor values, we get R1 = 470 kΩ, R2 = 11 kΩ, and R3 = 47 kΩ.

8.2.2.2 Setting Output Voltage Rise Time (t_R)

For a successful design, the junction temperature of device must be kept below the absolute maximum rating during both dynamic (start-up) and steady-state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and inrush current limit required with system capacitance to avoid thermal shutdown during start-up.

The slew rate (SR) needed to achieve the desired output rise time can be calculated as:

$$SR\left(\frac{V}{ms}\right) = \frac{V_{IN}\,(V)}{t_R\,(ms)} = \frac{12\,V}{12\,ms} = 1\,\frac{V}{ms} \tag{9}$$

The C_{dVdt} needed to achieve this slew rate can be calculated as:

$$C_{dVdt}\,(pF) = \frac{3300}{SR\left(\frac{V}{ms}\right)} = \frac{3300}{1\,\frac{V}{ms}} = 3300\,pF \tag{10}$$

Choose the nearest standard capacitor value as 3300 pF.

For this slew rate, the inrush current can be calculated as:

$$I_{INRUSH}\,(mA) = C_{OUT}\,(\mu F) \times SR\left(\frac{V}{ms}\right) = 470\,\mu F \times 1\,\frac{V}{ms} = 470\,mA \tag{11}$$

The average power dissipation inside the part during inrush can be calculated as:

$$PD_{INRUSH} = 0.5 \times V_{IN}\,(V) \times I_{INRUSH}\,(mA) = 0.5 \times 12\,V \times 470\,mA = 2.82\,W \tag{12}$$

For the given power dissipation, the thermal shutdown time of the device must be greater than the ramp-up time t_R to avoid start-up failure. 図 8-7 shows the thermal shutdown limit, for 2.82 W of power, the shutdown time is more than 10 s which is very large as compared to t_R = 12 ms. Therefore, it is safe to use 12 ms as the start-up time for this application.

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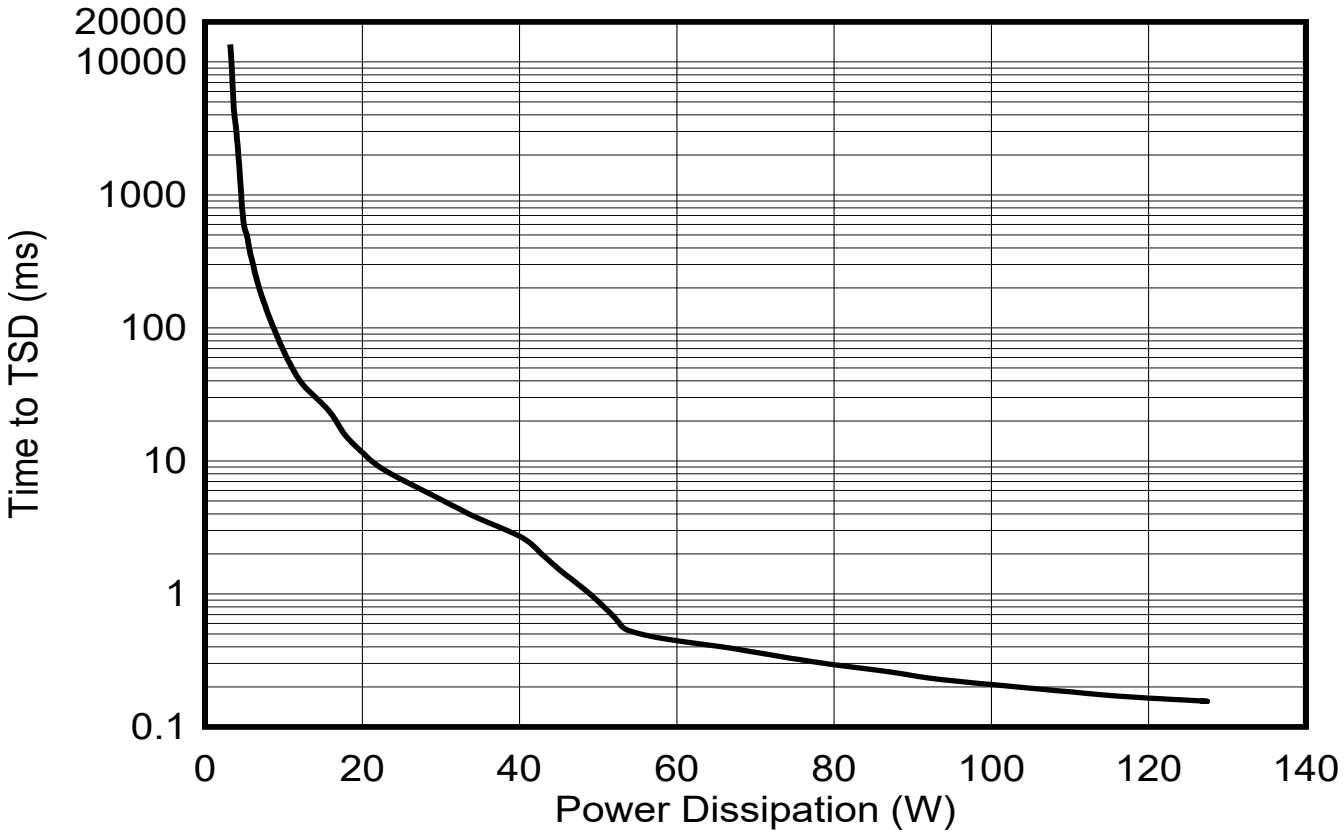

図 8-7. Thermal Shutdown Plot During Inrush

8.2.2.3 Setting Power-Good Assertion Threshold

The power-good assertion threshold can be set using the resistors R4 and R5 connected to the PGTH pin whose values can be calculated as:

$$V_{PG} = \frac{V_{PGTH(R)} \times \left(R_4 + R_5\right)}{R_5} \tag{13}$$

Because R4 and R5 leak the current from the output rail VOUT, these resistors must be selected to minimize the leakage current. The current drawn by R4 and R5 from the power supply is IR45 = VOUT / (R4 + R5). However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, IR123 must be chosen to be 20 times greater than the PGTH leakage current expected. From the device electrical specifications, PGTH leakage current is 1 µA (maximum), $VPGTH_{(R)}$ = 1.2 V and from design requirements, VPG = 11.4 V. To solve the equation, first choose the value of R4 = 47 kΩ and calculate R5 = 5.52 kΩ. Choose nearest 1% standard resistor value as R5 = 5.6 kΩ.

8.2.2.4 Setting Analog Current Monitor Voltage (IMON) Range

The analog current monitor voltage range can be set using the RIMON resistor whose value can be calculated as:

$$R_{IMON}\,(\Omega) = \frac{V_{IMON}\,(\mu V)}{G_{IMON}\,(\mu A/A) \times I_{OUTmax}\,(A)} = \frac{0.5 \times 10^6}{95 \times 5.5} = 957\ \Omega \tag{14}$$

Choose nearest 1% standard resistor value as 953 Ω.

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8.2.3 Application Curves

図 8-8. Power Up

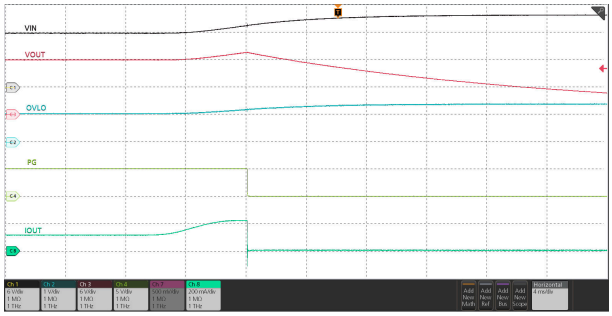

図 8-9. Overvoltage Response

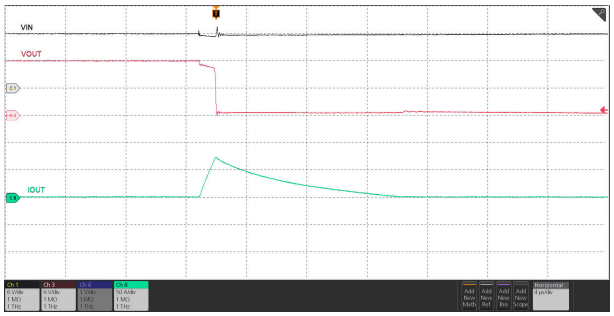

図 8-10. Output Short-Circuit During Steady-State

9 Power Supply Recommendations

The TPS22811x devices are designed for a supply voltage range of 2.7 V ≤ V_{IN} ≤ 16 V. TI recommends an input ceramic bypass capacitor higher than 0.1 µF if the input supply is located more than a few inches from the device. The power supply must be rated higher than the set current limit to avoid voltage droops during overcurrent and short-circuit conditions.

9.1 Transient Protection

In the case of a short-circuit or device turn off during steady-state when the device interrupts current flow, the input inductance generates a positive voltage spike on the input, and the output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on the value of inductance in series to the input or output of the device. Such transients can exceed the absolute maximum ratings of the device if steps are not taken to address the issue. Typical methods for addressing transients include:

- Minimize lead length and inductance into and out of the device.
- Use a large PCB GND plane.
- Connect a Schottky diode from the OUT pin ground to absorb negative spikes.
- Connect a low ESR capacitor larger than 1 µF at the OUT pin very close to the device.
- Use a low-value ceramic capacitor C_{IN} = 1 µF to absorb the energy and dampen the transients. The capacitor voltage rating must be at least twice the input supply voltage to be able to withstand the positive voltage excursion during inductive ringing.

  Use 式 15 to estimate the approximate value of input capacitance:

$$V_{SPIKE(Absolute)} = V_{IN} + I_{LOAD} \times \sqrt{\frac{L_{IN}}{C_{IN}}} \quad (15)$$

  where

  – V_{IN} is the nominal supply voltage.
  – I_{LOAD} is the load current.
  – L_{IN} equals the effective inductance seen looking into the source.
  – C_{IN} is the capacitance present at the input.
- Some applications can require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the absolute maximum ratings of the device. In some cases, even if the maximum amplitude of the transients is below the absolute maximum rating of the device, a TVS can help to absorb the excessive energy dump and prevent it from creating very fast transient voltages on the input supply pin of the IC, which can couple to the internal control circuits and cause unexpected behavior.

図 9-1 shows the circuit implementation with optional protection components.

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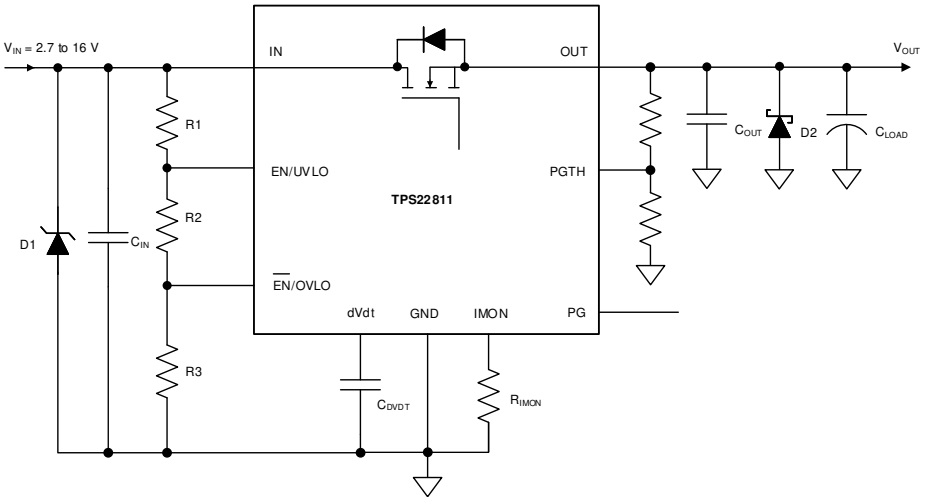

図 9-1. Circuit Implementation with Optional Protection Components

9.2 Output Short-Circuit Measurements

Obtaining repeatable and similar short-circuit testing results is difficult. The following contribute to variation in results:

- Source bypassing
- Input leads
- Circuit layout
- Component selection
- Output shorting method
- Relative location of the short
- Instrumentation

The actual short exhibits a certain degree of randomness because it microscopically bounces and arcs. Ensure that configuration and methods are used to obtain realistic results. Do not expect to see waveforms exactly like those in this data sheet because every setup is different.

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10 Layout

10.1 Layout Guidelines

- For all applications, TI recommends a ceramic decoupling capacitor of 0.1 µF or greater between the IN terminal and GND terminal.
- The optimal placement of the decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC.
- High current-carrying power-path connections must be as short as possible and must be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC with the shortest possible trace. The PCB ground must be a copper plane or island on the board. TI recommends to have a separate ground plane island for the eFuse. This plane does not carry any high currents and serves as a quiet ground reference for all the critical analog signals of the eFuse. The device ground plane must be connected to the system power ground plane using a star connection.
- The IN and OUT pins are used for heat dissipation. Connect to as much copper area on top and bottom PCB layers using as possible with thermal vias. The vias under the device also help to minimize the voltage gradient across the IN and OUT pads and distribute current uniformly through the device, which is essential to achieve the best on-resistance and current sense accuracy.
- Locate the following support components close to their connection pins:
  - R_{IMON}
  - C_{dVdT}
  - Resistors for the EN/UVLO, $\overline{EN}$/OVLO pins
- Connect the other end of the component to the GND pin of the device with shortest trace length. The trace routing for the R_{IMON} and C_{dVdt} components to the device must be as short as possible to reduce parasitic effects on the current monitor and soft start timing. These traces must not have any coupling to switching signals on the board.
- Protection devices such as TVS, snubbers, capacitors, or diodes must be placed physically close to the device they are intended to protect. These protection devices must be routed with short traces to reduce inductance. For example, TI recommends a protection Schottky diode to address negative transients due to switching of inductive loads. TI also recommends to add a ceramic decoupling capacitor of 1 µF or greater between OUT and GND. These components must be physically close to the OUT pins. Care must be taken to minimize the loop area formed by the Schottky diode/bypass-capacitor connection, the OUT pin and the GND terminal of the IC.

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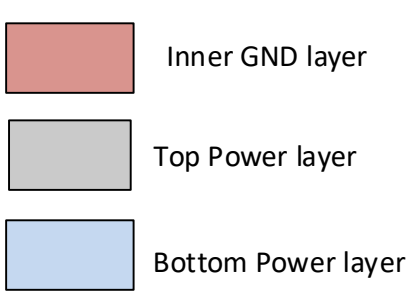
10.2 Layout Example



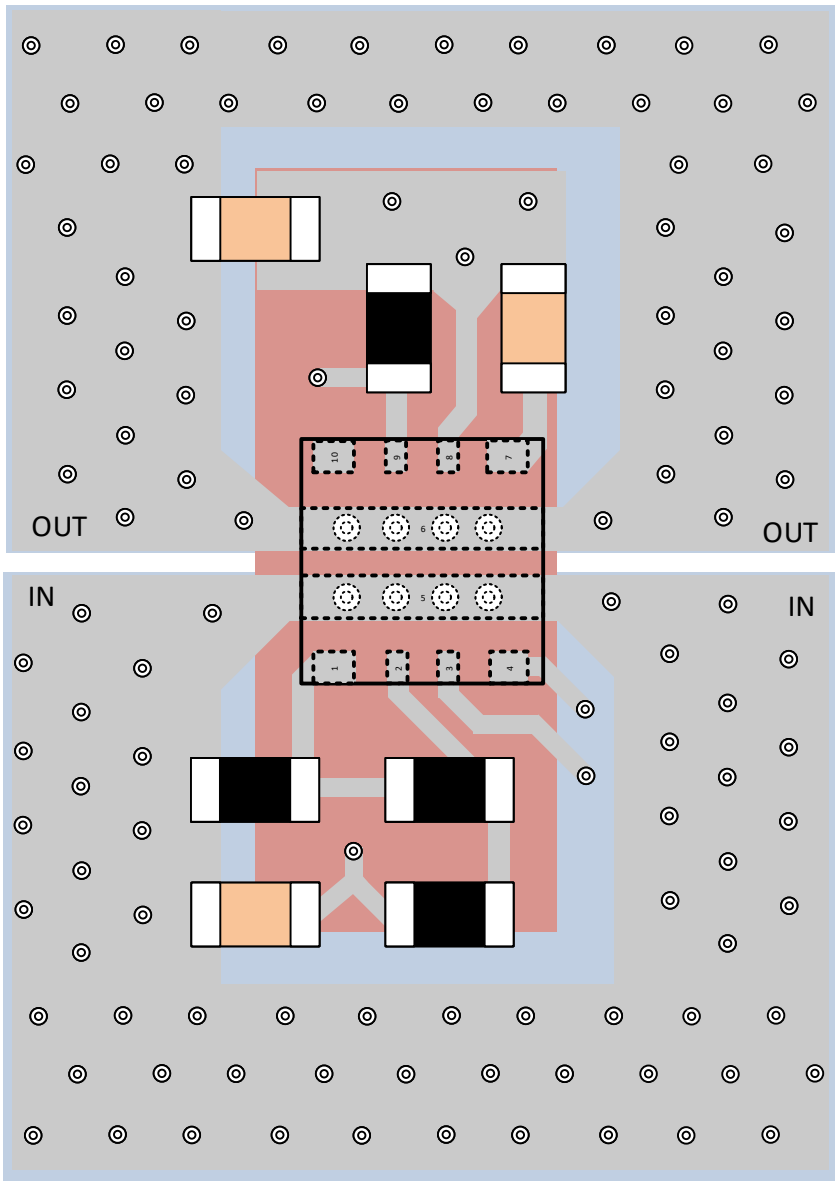


図 10-1. Layout Example

11 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

- Texas Instruments, *TPS22811EVM eFuse Evaluation Board*
- Texas Instruments, *TPS22811x Design Calculator*

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22811LRPWR	ACTIVE	VQFN-HR	RPW	10	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	2KZH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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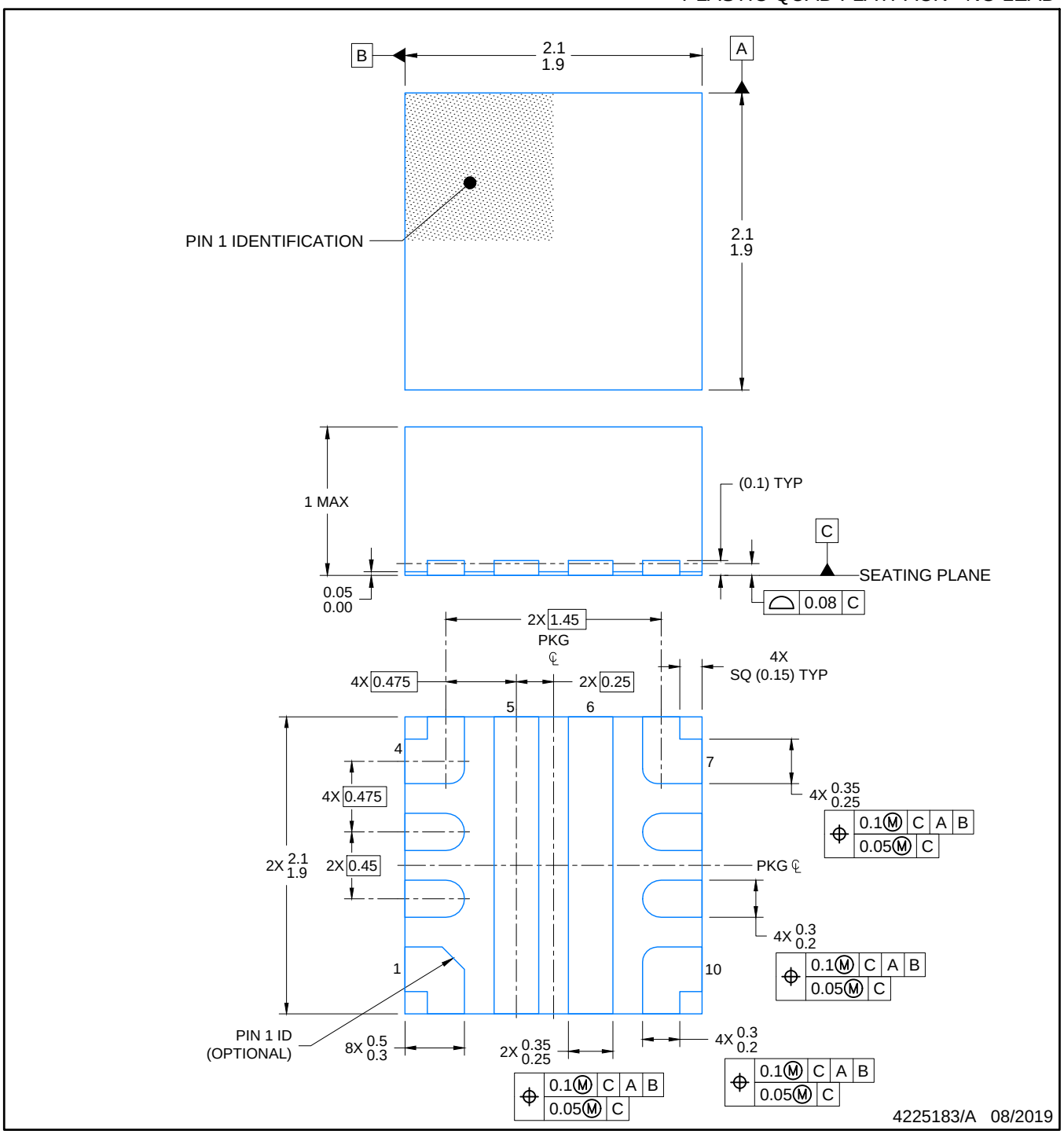
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGE OUTLINE

RPW0010A

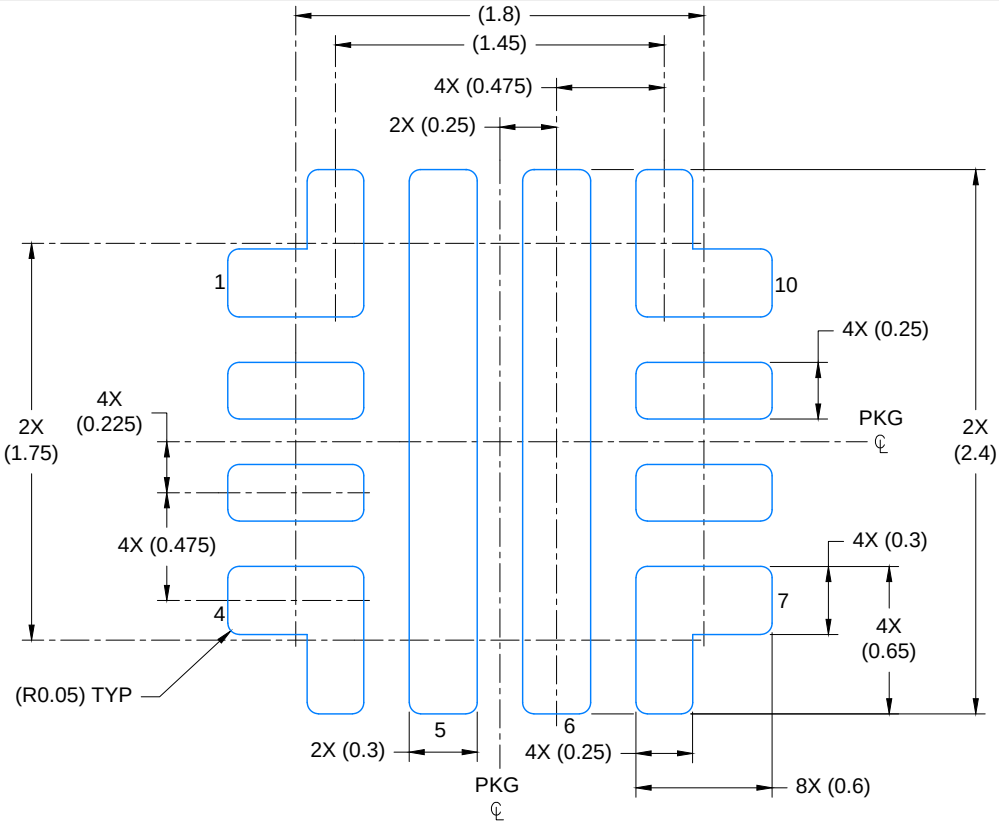
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



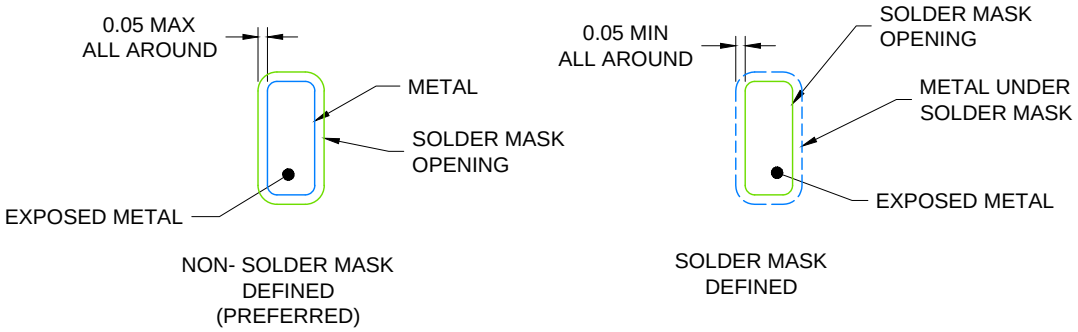
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE

SCALE: 30X



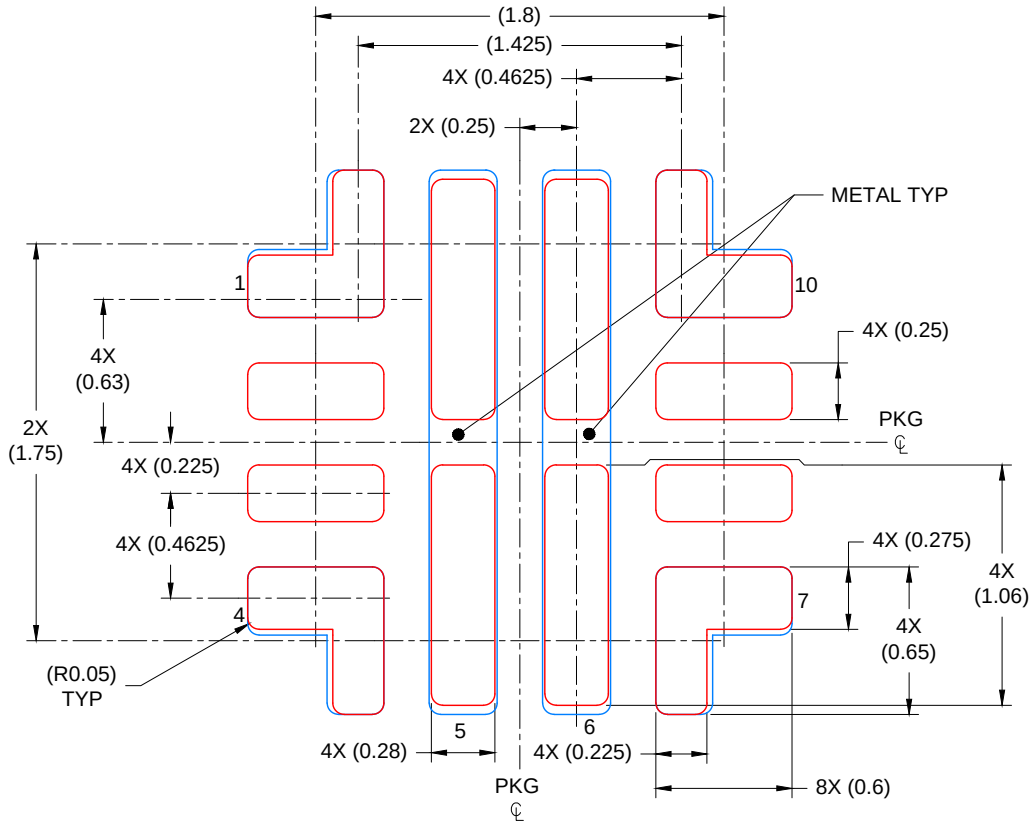
SOLDER MASK DETAILS

NOT TO SCALE

4225183/A 08/2019

NOTES: (continued)

3. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.100 mm THICK STENCIL

PADS 1, 4,7 & 10: 93%; PADS 5 & 6: 82%
SCALE: 30X

4225183/A 08/2019

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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