TPS23523: -48Vのホットスワップand Single OR-ingコントローラ

1 特長

- -10V～-80VのDC動作、絶対最大定格-200V
- ソフトスタート・コンデンサの切断機能
- デュアル・ホットスワップ・ゲート・ドライブ
- 400µAのゲート・ソーシング電流
- デュアル電流制限(V_{DS}に基づく)
  - 低V_{DS}時に25mV ±4%
  - 高V_{DS}時に3mV ±25%
- UV (±1.5%)およびOV (±2%)をプログラム可能
  - ヒステリシスをプログラム可能(±11%)
- 内蔵のORingコントローラ
  - レギュレーション: 25mV ±15mV
  - 高速なターンオフ: -6mV ±4mV
- タイムアウト後の再試行
- 16ピンTSSOP

2 アプリケーション

- リモート無線ユニット
- ベースバンド・ユニット
- ルータおよびスイッチ
- スモールセル
- -48Vのテレコミュニケーション・インフラストラクチャ

3 概要

TPS23523は、統合型ホットスワップおよびORingコントローラで、大電力のテレコム・システムが厳格な過渡要件に準拠するために使用できます。絶対最大定格が200Vで、雷サージ・テストに簡単に耐えられます(IEC61000-4-5)。ソフトスタート・コンデンサの切断機能により、過渡応答を損なうことなく突入電流が制限されるため、小さなホットスワップFETを使用できます。デュアル・ホットスワップ・ゲート・ドライバにより、複数のホットスワップFETを必要とする大電力のアプリケーションで、スペースとBOMコストを削減できます。400µAのソーシング電流により、高速な回復が可能になり、雷サージ・テスト中にシステム・リセットを避けるため役立ちます。デュアル電流制限により、ATIS 0600315.2013で要求されるようなブラウン・アウトおよび入力ステップへの準拠が容易になります。最後に、正確な低電圧および過電圧保護機能があり、スレッショルドとヒステリシスをプログラム可能です。

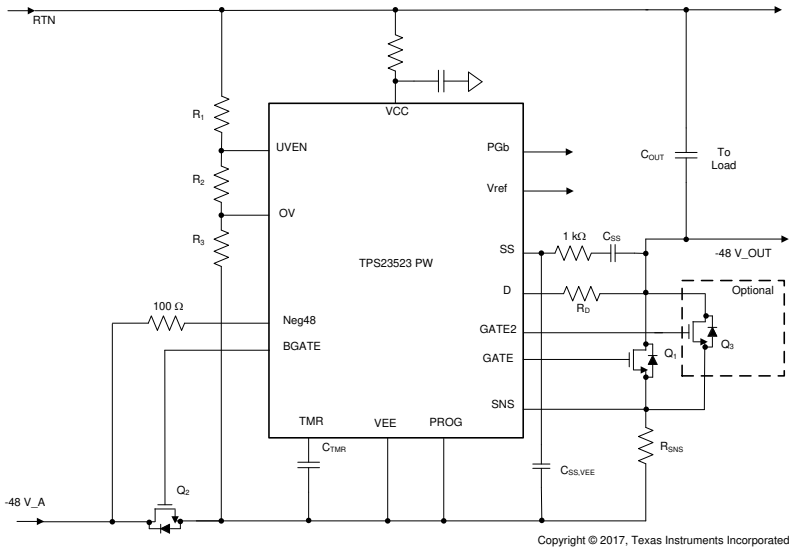
TPS23523にはORingコントローラが内蔵されており、逆フックアップ保護および逆電流保護を必要とする-48Vシステムに理想的です。ORingコントローラは、入力の低下時に出力を保護し、システム・リセットを回避します。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS23523	TSSOP (16)	5.00mm×4.40mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図



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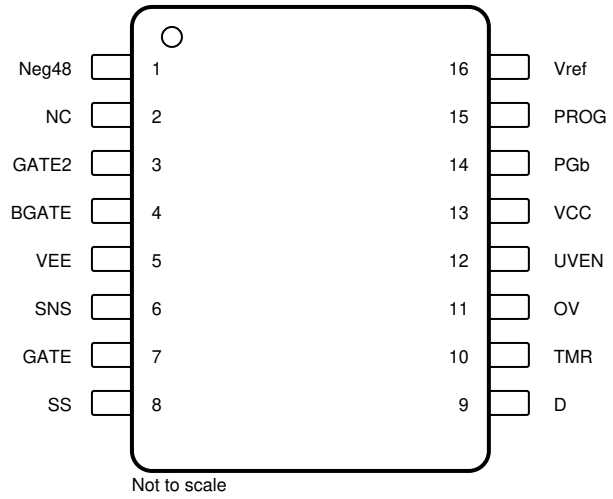
4 改訂履歴

2017年12月発行のものから更新 **Page**

- Added a row for V_D in the *Absolute Maximum Ratings* table ... 4
- Added tablenote 2 to the *Absolute Maximum Ratings* table ... 4
- Updated Equation 12 ... 20
- Updated Equation 22 ... 22

5 Pin Configuration and Functions

PW Package
16-Pin (TSSOP)
Top View



Not to scale

Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
Neg48	1	I	Input to the OR-ing controller for the –48 feed. The TPS23523 will regulate the drop from VEE to Neg48 to 25 mV to mimic an ideal diode.
NC	2		No connect to space high voltage pins.
GATE2	3	O	Gate driver for the 2nd hot swap FET. NC if feature isn't used.
BGATE	4	O	Gate driver for the OR-ing FET.
VEE	5	GND	This pin corresponds to the IC GND. Kelvin sense to the bottom of R_{SNS} to ensure accurate current limit.
SNS	6	I	Sense pin, used to measure current and regulate it. Kelvin Sense to R_{SNS} to ensure accurate current limits.
GATE	7	O	Gate drive for the main hot swap FET.
SS	8	O	Pin used for soft starting the output. Connect a capacitor (C_{SS}) between the SS pin and -48V_OUT. The dv/dt rate on the -48V_OUT pin is proportional to the gate sourcing current divided by C_{SS}.
D	9	I	Pin used to sense the drain of the hot swap FET and to program the threshold where the hot swap switches from the CL1 and CL2. Connect a resistor from this pin to the drain of the hot swap FET (also called -48V_OUT) to program the threshold.
TMR	10	O	Timer pin used to program the duration when the hot swap FET can be in current limit. Program this time by adding a capacitor between the TMR pin and VEE.
OV	11	I	Input overvoltage comparator. Tie a resistor divider to program the threshold where the device turns off due to overvoltage event.
UVEN	12	I	Input undervoltage comparator. Tie a resistor divider to program the threshold where the device turns on.
VCC	13	S	Clamped supply. Tie to RTN through resistor.
PGb	14	O	Power Good Bar, which is an open drain output that indicated when the power is good and the load can start drawing full power. PGb goes low when the hot swap is fully on and the DC/DC can draw full power.
PROG	15	I	Adjust current limit and fast trip threshold by tying to VEE, floating, or tying to VEE through resistor.
Vref	16	O	5V reference output. Connect to the base of a BJT to generate a rail that can be used to power current monitors and digital Isolators.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply voltage	V_{VCC} (current into V_{CC} <10 mA)	–0.3	20	V
Input voltage	V_{SNS}, V_{OV}	–0.3	6.5	V
	V_{UVEN}, , V_{SS}	–0.3	30	V
	V_D(2)	–0.3	40	V
Input voltage	V_{Neg48}	–0.3	200	V
	V_{Neg48} through 100-Ω resistor	–1	200	V
	V_{Neg48} through 1-kΩ resistor	–2	200	V
Output voltage	V_{GATE}, V_{GATE2}, V_{BGATE}	–0.3	VCC	V
	V_{TMR} , V_{PROG}, V_{VREF}	–0.3	6.5	V
Output voltage	V_{PGb}	–0.3	200	V
Operating junction temperature, T_J		–40	125	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Current into the Pin D should be limited to < 1 mA through RD resistor

6.2 ESD Ratings

		VALUE	UNIT
$V_{(ESD)}$ Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	1000	V
	Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VCC}	Supply voltage (current into V_{CC} <10 mA)	0		20	V
V_{SNS}, V_{OV}	Input voltage	0		5.5	V
V_{UVEN}, V_D, V_{SS}	Input voltage	0		18	V
V_{Neg48}	Input voltage, through 100-Ω resistor	–0.2		150	V
V_{GATE}, V_{GATE2}, V_{BGATE}	Output voltage	0		VCC	V
V_{TMR} , V_{PROG}, V_{VREF}	Output voltage	0		5.5	V
V_{PGb}	Output voltage	0		80	V
C_{SS}	Capacitance	1		200	nF
R_{SS}	Resistance	1		10	kΩ
R_D	Resistance	120		2,000	kΩ
R_{NEG48V}	Resistance	100		1	kΩ

6.4 Thermal Information

THERMAL METRIC[1]		TPS23523 PW (TSSOP) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	98.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.3	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	43.6	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

–40°C ≤ T_J ≤125°C, 1.1 mA < I_{VCC} < 10 mA, $V_{(UVEN)}$ = 2 V, $V_{(OV)}$ = $V_{(SNS)}$ = $V_{(D)}$ = 0 V, $V_{(SS)}$ = GATEx = Hi-Z , $V_{(TMR)}$ = 0 V, –1 V < $V_{NEG48Vx}$ < 150 V, V_{Vref} = V_{PROG} = Hi-Z; All pin voltages are relative to VEE (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCC – Clamped Supply						
$V_{(UVLO\_VCC)}$	UVLO on VCC	rising	9	9.5	10	V
$V_{(UVLO\_VCC,hyst)}$	UVLO hysteresis on VCC	hysteresis		1		V
$V_{(VCC)}$	VCC regulation	1.1< $I_{(VCC)}$ < 10 mA (current into VCC)	12	14.5	18	V
I_Q	Quiescent Current	V_{VCC} = 10 V. Off			1	mA
		V_{VCC} = 10 V. On			1	mA
		V_{VCC} = 10 V, Gateand BGATE in regulation			1.1	mA
UVEN – Undervoltage and Enable						
$V_{(UVEN\_T)}$	Threshold voltage for $V_{(UVEN)}$		0.985	1	1.015	V
$I_{(UV\_hyst)}$	Hysteresis current, sourcing from UV pin	V_{UV} = 1.5 V	9	10	11.2	µA
OV – Overvoltage						
$V_{(OV\_T)}$	Threshold voltage for V_{OV}		0.98	1	1.02	V
$I_{(OV\_hyst)}$	Hysteresis current, sourcing from OV pin	V_{OV} = 1.5 V	9	10	11.2	µA
TMR – Timer						
V_{TMR}	Voltage on timer when part times out.	V_D = 0 V, TMR ↑, measure V_{TMR} when V_{GATE} = 0	1.47	1.5	1.53	V
V_{TMR2}	Voltage on timer when part times out.	V_D = 1 V, TMR ↑, measure V_{TMR} when V_{GATE} = 0	0.735	0.75	0.765	V
$I_{TMR,SRs}$	Timer Sourcing current when in fault condition or when retrying.	V_{SNS} = 0.1 V, V_D = 0 V, V_{TMR} = 0 V, measure I out from TMR	9	10	11	µA
		V_{SNS} = 0.1 V, VD = 2 V, V_{TMR} = 0 V, measure I out from TMR	45	50	55	µA
$I_{TMR,SNC}$	Timer sinking current when not in fault condition.	V_{SNS} = 0 V, V_D = 0 V, V_{TMR} = 2 V,	1.5	2	2.5	µA
$V_{TMR,RETRY}$	Voltage on timer when the timer starts going back up in retry. Retry version only.	V_{SNS} = 0 V, V_D = 0 V, TMR ↑ = 2 V, TMR ↓, measure V_{TMR} when I into TMR change polarity	0.475	0.5	0.525	V
N_{RETRY}	Number of retry duty cycles. Retry version only.			64		
D_{RETRY}	Retry duty cycle. Retry version only.			0.4%		
$I_{GATE,TIMER}$	Gate Sourcing Current Threshold When timer starts to run.	V_G = 5 V, V_D = 2 V, V_{SNS} ↑, measure I_{GATE} when TMR sources current	5	10	15	µA

Electrical Characteristics (continued)

–40°C ≤ T_J ≤125°C, 1.1 mA < I_{VCC} < 10 mA, $V_{(UVEN)}$ = 2 V, $V_{(OV)}$ = $V_{(SNS)}$ = $V_{(D)}$ = 0 V, $V_{(SS)}$ = GATEx = Hi-Z , $V_{(TMR)}$ = 0 V, –1 V < $V_{NEG48Vx}$ < 150 V, V_{Vref} = V_{PROG} = Hi-Z; All pin voltages are relative to VEE (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{SNS,TMR1}$	Sense Voltage when Timer starts to run.	V_D = 2 V, V_{TMR} = 0 V, V_G = 5 V; V_{SNS} ↑, measure V_{SNS} when TMR sources current	1.5	2.5		mV
$V_{SNS,TMR2}$	Sense Voltage when Timer starts to run.	V_D = 0 V, V_{TMR} = 0 V , V_G = 5 V; V_{SNS} ↑, measure V_{SNS} when TMR sources current	23.25	24.5		mV
SNS – Sense Pin For Current Limit						
$I_{SNS,LEAK}$	Leakage current on sense pin		-2		2	µA
$V_{SNS,CL1}$	PROG = Float	V_{TMR} = 0 V. V_{GATE} = 5 V. V_D = 0 V, V_{SNS} ↑, measure when I_{GATE} = 0;	24	25	26	mV
	PROG = VEE		38	40	42	mV
$V_{SNS,FST}$	PROG = FLOAT	V_{TMR} = 0 V. V_{GATE} = 5 V. V_D = 0 V, V_{SNS} ↑,measure when I_{GATE}> 100 mA	45	50	55	mV
	PROG = VEE		72	80	88	mV
	R_{PROG} = 78.7kΩ		110	120	130	mV
	R_{PROG} = 162 kΩ		68	75	82	mV
$V_{SNS,CL2}$	Fold Back Current Limit	V_{TMR} = 0 V, V_{GATE} = 5 V, V_D = 5 V, V_{SNS} ↑, measure when I_{GATE} = 0;	2.25	3	3.75	mV
$V_{SNS,FST2}$	Fast Trip during start-up	V_{TMR} = 0 V, V_{GATE} = 5 V, V_D = 5 V, V_{SNS} ↑, Measure when I_{GATE}> 100 mA	6	9	12	mV
PROG – Programing Pin to Set Current Limit (CL) and Fast Trip						
i_{PROG}	PROG pin current		7.9	10.1	12	µA
$V_{PROG,LOW}$	Prog pin voltage	Threshold on V_{PROG}, where the fast trip setting changes from 80mV to 120mV.			0.48	V
$V_{PROG,MID}$	Prog pin voltage	Threshold on V_{PROG}, where the current limit setting changes from 25mV to 40mV.	0.94	1.23	1.51	V
$V_{PROG,High}$	Prog pin voltage	Threshold on V_{PROG}, where the fast trip setting changes from 80mV to 120mV.	2.4			V
GATE – Gate Drive for Main Hot Swap FET						
$V_{(VCC-GATE)}$	Output gate voltage	$V_{(SNS)}$ = 0 V			1	V
$I_{(GATE,SRS,NORM)}$	Sourcing Current during normal operation.	$V_{(TMR)}$ = 0 V. $V_{(GATE)}$ = 8 V. V_D = 0 V, $V_{(SNS)}$ = 0 V	250	400		µA
$I_{(GATE,SRS,START)}$	Sourcing Current during star-up	$V_{(TMR)}$ = 0 V. $V_{(GATE)}$ = 5 V. V_D = 0 V, $V_{(SNS)}$ = 0 V	15	20	25	µA
$I_{(GATE,wkpd)}$	Weak pull down current	$V_{(SNS)}$ = 0 V. V_{UVEN} = 0 V	3	5	7	mA
$I_{(GATE,FST)}$	Fast Pull down current with 10mV overdrive		0.4	1	1.5	A
GATE2 – Gate Drive for Auxiliary Hot Swap FET						
$V_{(VCC-GATE2)}$	Output gate voltage	$V_{(SNS)}$ = 0 V			1	V
$I_{(GATE2,wkpd)}$	weak pull down	V_{GATE} = 0 V		5		mA
$I_{(GATE2,SRC)}$	Sourcing Current			50		µA
$I_{GATE2,FST}$	Fast Pull down current with 10 mV overdrive		0.4	1	1.5	A
$V_{GATE,TH}$	Threshold on V_{GATE} when GATE2 turns on	Raise V_{GATE}, measure when V_{GATE2} comes up.	6.25	7.25	8	V
$V_{GATE,TH,hyst}$	Hysteresis of threshold on V_{GATE} when GATE2 turns on	hysteresis		0.5		V
D – Drain Sense						

Electrical Characteristics (continued)

–40°C ≤ T_J ≤125°C, 1.1 mA < I_{VCC} < 10 mA, $V_{(UVEN)}$ = 2 V, $V_{(OV)}$ = $V_{(SNS)}$ = $V_{(D)}$ = 0 V, $V_{(SS)}$ = GATEx = Hi-Z , $V_{(TMR)}$ = 0 V, –1 V < $V_{NEG48Vx}$ < 150 V, V_{Vref} = V_{PROG} = Hi-Z; All pin voltages are relative to VEE (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{(D,INT)}$	Resistance from the drain pin to GND.		28.5	30	31.5	kΩ
$V_{(D,CL\_SW)}$	Voltage on drain that switches between two current limits	$V_{(TMR)}$ = 0 V, $V_{(GATE)}$ = 5 V, $V_{(SNS)}$ = 20 mV, D↑, measure V when $I_{(GATE)}$ = 0	1.46	1.5	1.54	V
$V_{(D,TMR\_SW)}$	Voltage on drain that switches the V_{TMR} threshold.	$V_{(TMR)}$ = 1 V, $V_{(GATE)}$ = 5 V, $V_{(SNS)}$ = 20 mV, D↑, measure V when $I_{(GATE)}$ = 0	0.73	0.75	0.77	V
$V_{(D,TMR\_SW,hyst)}$	hysteresis for $V_{(D,TMR,SW)}$	hysteresis		75		mV
SS (Soft Start)						
$I_{(SS,PD)}$	Pull down current when not in inrush	V_{SS} = 5 V	100			mA
$R_{(SS,GATE)}$	Resistance between GATE and SS in the start-up phase			80		Ω
Vref						
V_{Vref}	Reference output	0 < I_{Vref} < 800 µA	4	4.9	5.5	V
I_{Vref}	V_{Vref} SC current	Vref ON, V_{Vref} (shorted)		2		mA
Neg48						
$I_{(lkg,Neg48)}$	Leakage current	V_{Neg48} = –50 mV, BGATE ON	-2		2	µA
		V_{Neg48} = –100 mV, BGATE ON	-7		7	µA
		V_{Neg48} = 150 V, BGATE off			30	µA
$V_{(FWD)}$	Forward regulation voltage of the OR-ing controller. V_{FWD} = V_{EE} – $V_{(NEG48Vx)}$		10	25	40	mV
$V_{(FWD,FST)}$	Forward voltage where a fast pull up is activated.	V_{GATEx} = 5 V. V_{VEE} – $V_{Neg48Vx}$ ↑ measure when I_{GATEx} = 100 µA	50	80	105	mV
$V_{(RV)}$	Fast reverse trip voltage.		2	6	10	mV
BGATE						
$V_{VCC-BGATE}$	Gate Output Voltage.			0.65	1.1	V
$I_{(BGATE,SRS)}$	Gate sourcing current in regulation	V_{VEE} – $V_{Neg48Vx}$ = 50 mV		5		µA
$I_{(BGATE,SINK)}$	Gate sinking current in regulation	V_{VEE} – $V_{Neg48Vx}$ = 0		5		µA
$R_{GATE,SRC,FST}$	Pull up resistance in fast sourcing mode.	V_{VEE} – $V_{Neg48Vx}$ = 100 mV; Measure current at V_{GATEx} = 0 V. R = $V_{VCC/I}$		10		kΩ
$I_{(BGATE,FST)}$	Fast Gate pull down current	$V_{(VEE)}$ – V_{Neg48} = –15 mV	0.4	1	1.5	A
PGb (Power Good Bar)						
$V_{(GATE2,PGb)}$	Threshold on GATE2 that triggers PGb to assert.	Raise V_{GATE2} until PGb asserts	6.5	7.25	8	V
$V_{(PGb,PD)}$	Pull down strength on PGb	PGb sinking 1 mA			1.5	V
$I_{(PGb,LEAK)}$	leakage current on PGb pin				1	µA
OTSD (Over Temperature Shut Down)						
T_{SD}	Shutdown temperature	Temp Rising	135	155	175	°C
$T_{SD,hyst}$	Shutdown temperature Hysteresis			8		°C

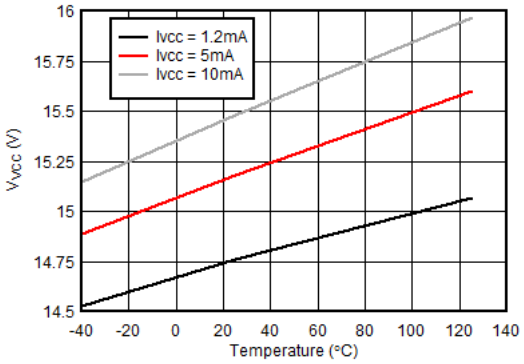
6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VCC – Clamped Supply						
t_{ID}	Insertion Delay	V_{VCC}: 0 V → 10 V, measure delay before V_{GATE} ↑		32		ms
UVEN						
$T_{UV,degl}$	Deglitch on UVEN			4		µs
OV						
$T_{OV,degl}$	Deglitch on OV			4		µs
SNS						
$T_{SNS,FST,RESP}$	Response time to large over current	V_{SNS} steps from 0 mV to 60 mV. Measure time for GATE and GATE2 to come down.		300		ns
Neg48V						
$T_{Neg48V,FST,RESP}$	Response time to large reverse current	V_{NEG48V} steps from -40 mV to 15 mV. Measure time for BGATE to come down.		300		ns
PGb						
$t_{PGb,DEGL}$	Deglitch of PGb. (GATE2 = unloaded, raise GATE, measure delay between GATE and PGb)	Power Good ↑ ($V_{(GATE)}$ 0 V → 10 V) Look for PGb ↓		1		ms
		Power Good ↓ ($V_{(GATE)}$ 10 V → 0 V) Look for PGb ↑		32		ms

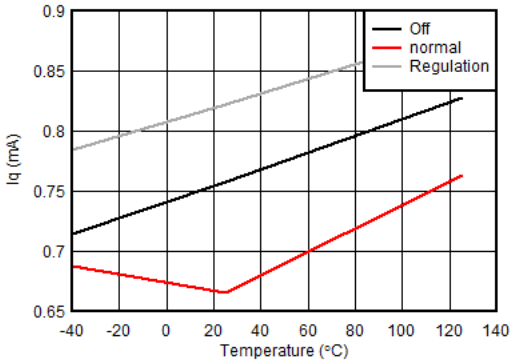
6.7 Typical Characteristics

Unless otherwise noted: –40°C ≤ T_J ≤125°C, 1.1 mA < I_{VCC} < 10 mA, $V_{(UVEN)}$ = 2 V, $V_{(OV)}$ = $V_{(SNS)}$ = $V_{(D)}$ = 0 V, $V_{(SS)}$ = GATEx = Hi-Z , $V_{(TMR)}$ = 0 V, –1 V < $V_{NEG48Vx}$ < 150 V , V_{Vref} = V_{PROG} = Hi-Z;



Ivcc injected into VCC pin

Figure 1. VCC Regulation Voltage vs Current and Temperature



V_{VCC} = 10 V, Regulation is current limit

Figure 2. Iq vs Temperature and Operating Condition

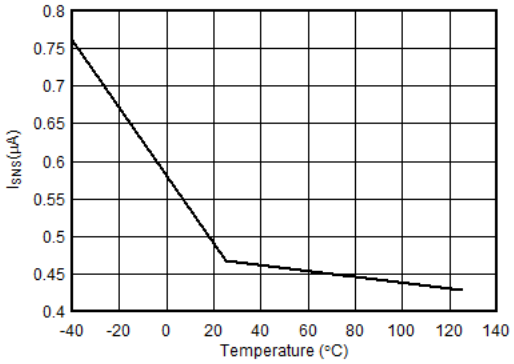


Figure 3. I_{sns} Current Vs Temperature

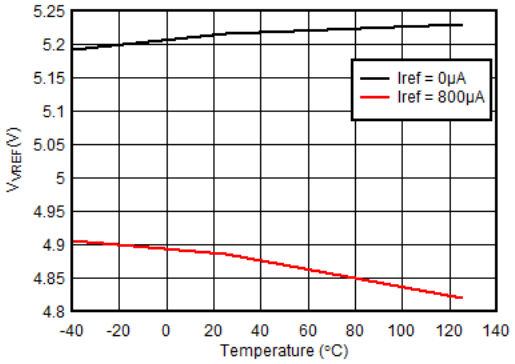
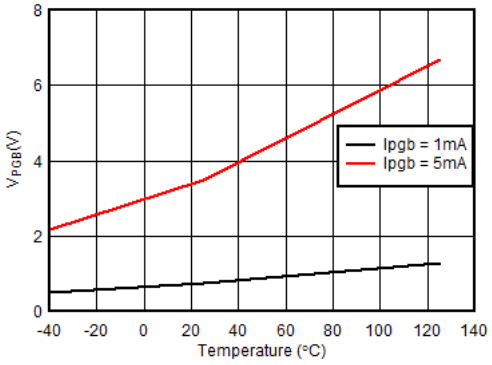


Figure 4. V_{Vref} vs Temperature and I_{VREF}



In Power Good

Figure 5. Vpgb vs Temperature

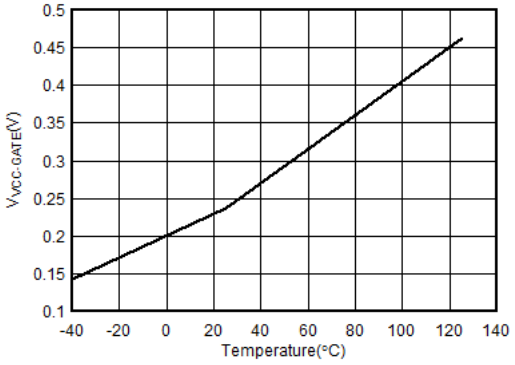


Figure 6. $V_{VCC-GATE}$ vs Temperature

7 Parameter Measurement Information

7.1 Relationship between Sense Voltage, Gate Current, and Timer

The diagram below illustrates the relationship between the V_{SNS} (voltage across R_{SNS}), Gate current, and the timer operation. The diagram is intended to help explain the various parameters in the electrical characteristic table and is not drawn to scale.

Note that I_{GATE} reduces as the sense voltage approaches the current limit threshold and it equals zero at the current limit regulation point. To ensure that the timer always runs when the IC is in regulation the timer starts at a slightly positive I_{GATE}.

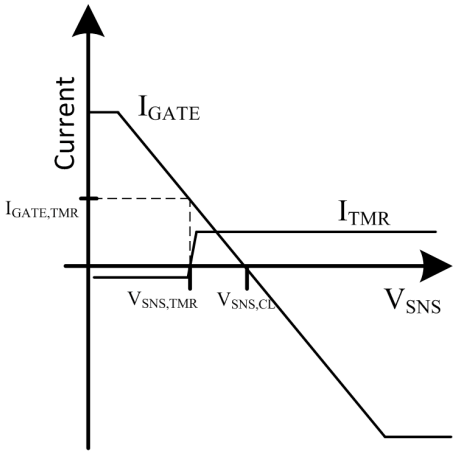


Figure 7. Relationship Between Timer, Gate Current, and Sense Voltage (V_{GATE} = 5 V)

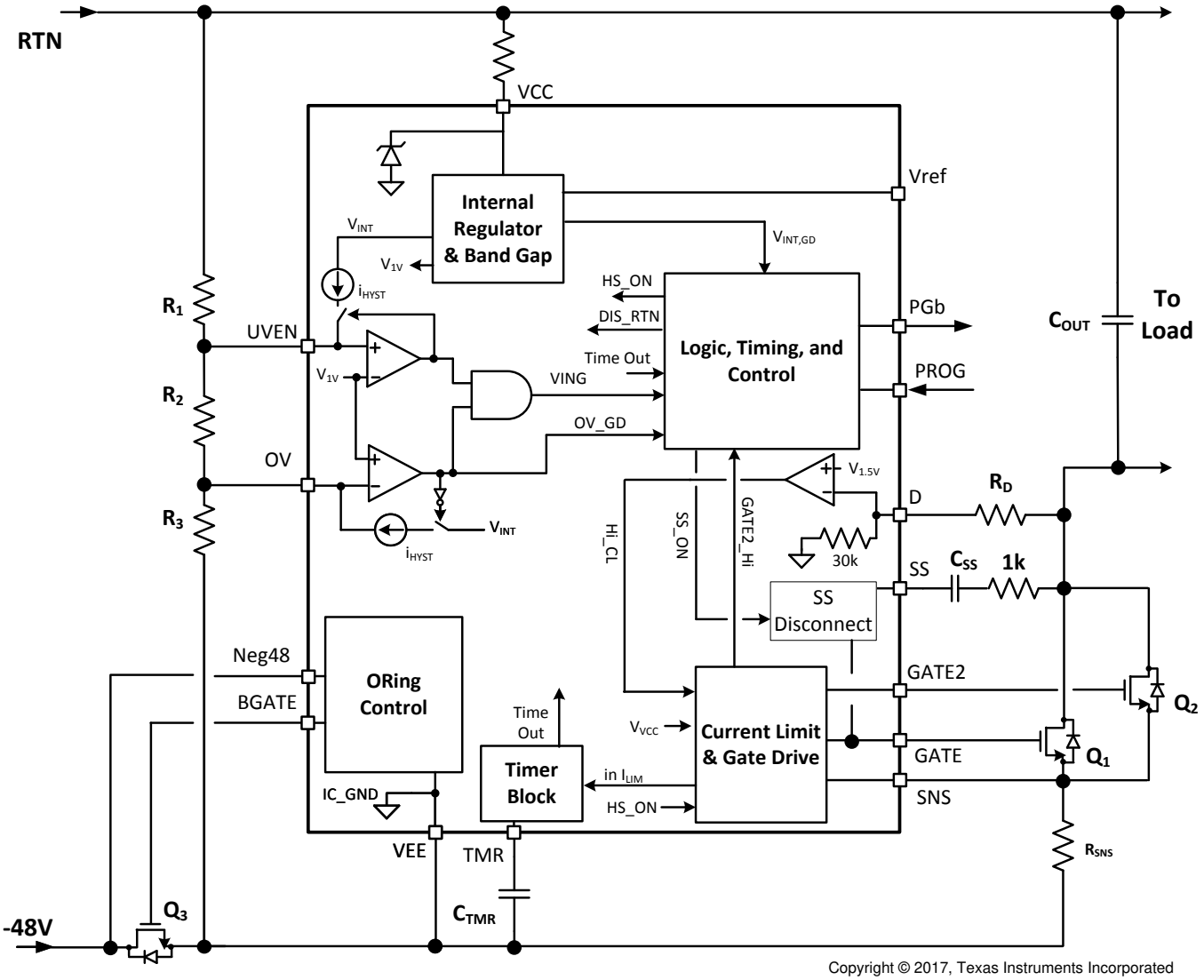
8 Detailed Description

8.1 Overview

The TPS23523 is an integrated hot swap and Single OR-ing controller that enables high power telecom systems to comply with stringent transient requirements. The soft start cap disconnect allows soft start at start-up and disconnects the soft start cap during normal operation. This allows for the use of smaller hot swap FETs without hurting the transient response. GATE2 is a second hot swap FET driver, which only turns ON when the main hot swap FET is fully on. Thus the FETs driven by GATE2 don't need to have strong SOA. This saves space and BOM cost in high power applications that require multiple hot swap FETs.The 400 µA sourcing current allows fast recovery, which helps to avoid system resets during lightning surge tests. The dual current limit makes it easier to pass brown outs and input steps such as required by the ATIS 0600315.2013. Finally, the TPS23523 offers accurate undervoltage and overvoltage protection with programmable thresholds and hysteresis.

The TPS23523 integrates an OR-ing controller, making it ideal for –48 V systems that require reverse hook-up protection and reverse-current protection. The OR-ing controller protects the output when the input drops avoiding system resets. The OR-ing controller will turn off if any reverse current is detected.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Current Limit

The TPS23523 utilizes two current limit thresholds:

- I_{CL1} – also referred to as high current limit threshold, which is used when the V_{DS} of the hot swap FET is low.
- I_{CL2} – lower current limit threshold, which is used when the V_{DS} of the hot swap FET is high.

This dual level protection scheme ensures that the part has a higher chance of riding out voltage steps and other transients due to the higher current limit at low V_{DS}, while protecting the MOSFET during start into short and hot-short events, by setting a lower current limit threshold for conditions with high $V_{DS.}$ The transition threshold is programmed with a resistor that is connected from the drain of the hot swap FET to the D pin of the TPS23523. The figure below illustrates an example with a I_{CL1} set to 25 A and I_{CL2} set to 3 A. Note that compared to a traditional SOA protection scheme this approach allows better utilization of the SOA in the 10 V < $V_{DS.}$ < 40-V range, which is critical in riding through transients and voltage steps.

Note that in both cases the TPS23523 regulated the gate voltage to enforce the current limit. However, this regulation is not very fast and doesn't offer the best protection against hot-shorts on the output. To protect in this scenario a fast comparator is used, which quickly pulls down the gate in case of severe over current events (2x bigger than V_{CL1}).

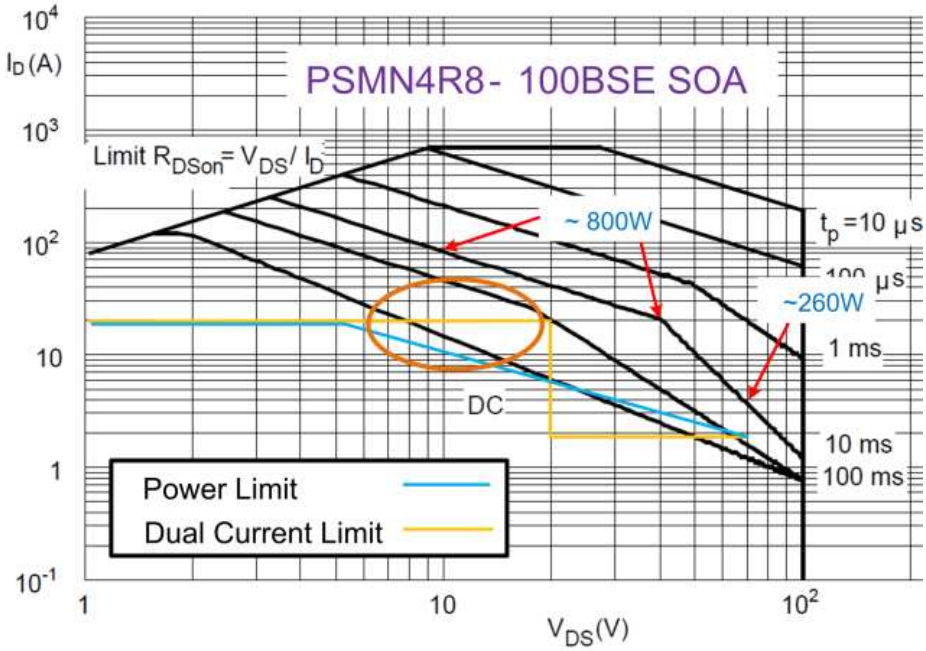


Figure 8. Dual Current Limit vs FET Power Limit

8.3.1.1 Programming the CL Switch-Over Threshold

The V_{DS} threshold when the TPS23523 switches over from I_{CL1} to I_{CL2} ($V_{D,SW}$) can be computed using Equation 1. For example, if a 15-V switch over is desired, R_D should be set to 270 kΩ.

$$V_{DS,SW} = \frac{1.5\ V \times \left(30\ k\Omega + R_D\right)}{30\ k\Omega} \quad (1)$$

8.3.1.2 Setting Up the PROG Pin

The PROG pin can be tied to VEE, left floating, or tied to VEE through a resistor to adjust $V_{SNS,CL1}$ and the ratio of fast trip to current limit. The options are set as follows:

- PROG = NC or Float: $V_{SNS,CL1}$ = 25 mV, $V_{SNS,FST}$ is 2x $V_{SNS,CL1}$
- R_{PROG} = 196 kΩ (1%): $V_{SNS,CL1}$ = 25 mV, $V_{SNS,FST}$ is 3x $V_{SNS,CL1}$

Feature Description (continued)

- R_{PROG} = 66.5 kΩ (1%): $V_{SNS,CL1}$ = 40 mV, $V_{SNS,FST}$ is 3x $V_{SNS,CL1}$
- PROG = VEE: $V_{SNS,CL1}$ = 40 mV, $V_{SNS,FST}$ is 2x $V_{SNS,CL1}$

8.3.1.3 Programming CL1

The current limit at low V_{DS} (I_{CL1}) of the TPS23523 can be computed using Equation 2.

$$I_{CL1} = \frac{V_{SNS,CL1}}{R_{SNS}} \tag{2}$$

To compute I_{CL1} for a 1-mΩ sense resistor use Equation 3 below.

$$I_{CL1} = \frac{V_{SNS,CL1}}{R_{SNS}} = \frac{25\ mV}{1\ m\Omega} = 25\ A \tag{3}$$

8.3.1.4 Programming CL2

The current limit at high V_{DS} (I_{CL2}) of the TPS23523 can be computed using Equation 4.

$$I_{CL2} = \frac{V_{SNS,CL2}}{R_{SNS}} \tag{4}$$

To compute I_{CL2} for a 1-mΩ sense resistor use Equation 5.

$$I_{CL2} = \frac{V_{SNS,CL2}}{R_{SNS}} = \frac{3\ mV}{1\ m\Omega} = 3\ A \tag{5}$$

8.3.2 Soft Start Disconnect

The inrush current into the output capacitor (C_{OUT}) can be limited by placing a capacitor between the SS (Soft Start) pin and the drain of the hot swap MOSFET. In that case the inrush current can be computed using Equation 6.

$$I_{INR} = \frac{C_{OUT} \times I_{GATE,SRS,START}}{C_{SS}} = \frac{660\ \mu F \times 20\ \mu A}{33\ nF} = 0.4\ A \tag{6}$$

Note that with most hot swap the C_{SS} pin is tied simply to the gate pin, but this can interfere with performance during normal operation if transients or short circuits are encountered. In addition the C_{SS} capacitor tends to pull up the gate during hot plug and cause shoot through current if it is always tied to the gate. For that reason the TPS23523 has a disconnect switch between the gate pin and the SS pin as well as a discharge resistor. During the initial hot plug and during the insertion delay the switch between SS and GATE is open and SS is being discharged to GND through a resistor. Then during start-up SS and GATE are connected to limit the slew rate. Once in normal operation the SS pin is not tied to GATE and it is not shorted to GND, which prevents it from interfering with the operation during transients.

Feature Description (continued)

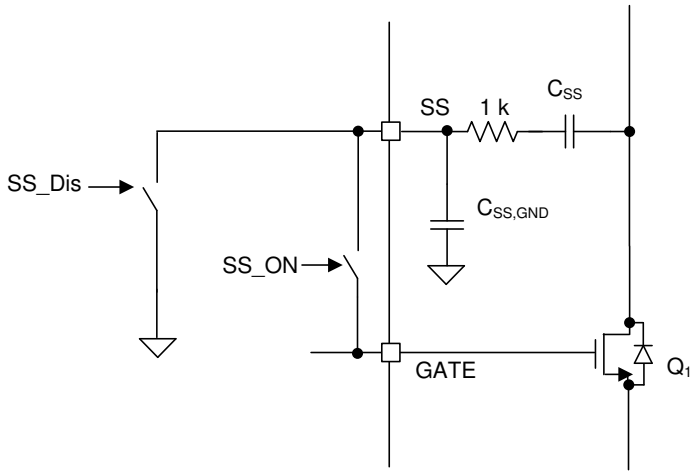


Figure 9. Implementation of SS Disconnect

8.3.3 Timer

Timer is a critical feature in the hot swap, which manages the stress level in the MOSFET. The timer will source and sink current into the timer capacitor as follows:

- Not in current limit: sink 2 µA
- If the part is in current limit and $V_{GATE} < V_{GATE,TH}$, the timer sources current as follows:
  - $V_D < V_{D,CL\_SW}$: source 10 µA
  - $V_D > V_{D,CL\_SW}$: source 50 µA

The TPS23523 times out and shuts down the hot swap as follows.

- If $V_D < V_{D,TMR\_SW}$ then the hot swap times out when V_{TMR} reaches 1.5 V.
- If $V_D > V_{D,TMR\_SW}$ then the hot swap times out when V_{TMR} reaches 0.75 V.

The above behavior maximizes the ability of the hot swap to ride out voltage steps, while ensuring that the FET remains safe even if the part can not ride out a voltage step.

A cool down period follows after the part times out. During this time the timer performs the following:

- Discharge C_{TMR} with a 2-µA current source until 0.5 V
- Charge C_{TMR} with a 10-µA current source until it is back to 1.5 V.
- Repeat the above 64 times
- Discharge timer to 0 V.

The part attempts to restart after finishing the above. If the UVEN signal is toggled while the 64 cycles are in progress the part restarts immediately after the 64 cycles are completed.

The timer operates as follows when recovering from POR:

- If $V_{TMR} < 0.5$ V:
  - Proceed to regular startup
  - Do not discharge V_{TMR}
- If $V_{TMR} > 0.5$ V:
  - Go through 64 charge/discharge cycles
  - Discharge V_{TMR}
  - Proceed to startup

The Time Out (T_{TO}) can be computed using the equations below. Note that the time out depends on the V_{DS} of the MOSFET.

Feature Description (continued)

$$T_{TO} = \frac{C_{TMR} \times V_{TMR}}{I_{TMR,SRS}} \quad (7)$$

$$T_{TO}(V_D < 0.75\ V) = \frac{C_{TMR} \times 1.5\ V}{10\ \mu A} \quad (8)$$

$$T_{TO}(0.75\ V < V_D < 1.5\ V) = \frac{C_{TMR} \times 0.75\ V}{10\ \mu A} \quad (9)$$

$$T_{TO}(V_D > 1.5\ V) = \frac{C_{TMR} \times 0.75\ V}{50\ \mu A} \quad (10)$$

8.3.4 Gate 2

The TPS23523 features a second hot swap Gate drive, which can be used to save BOM cost and size in applications that require multiple hot swap MOSFETs. The 2nd MOSFET is only turned ON when the main FET is enhanced. As a result the 2nd MOSFET doesn't operate with large current and large voltage across it, thus reducing the SOA requirements. In many cases a 5x6 QFN FET can replace a D^2PACK FET. The following figures show the operation during start-up and Hot Short event. It can be seen that the second FET is OFF during stressful operation and turns on during normal operation to improve steady state efficiency and reduce power losses.

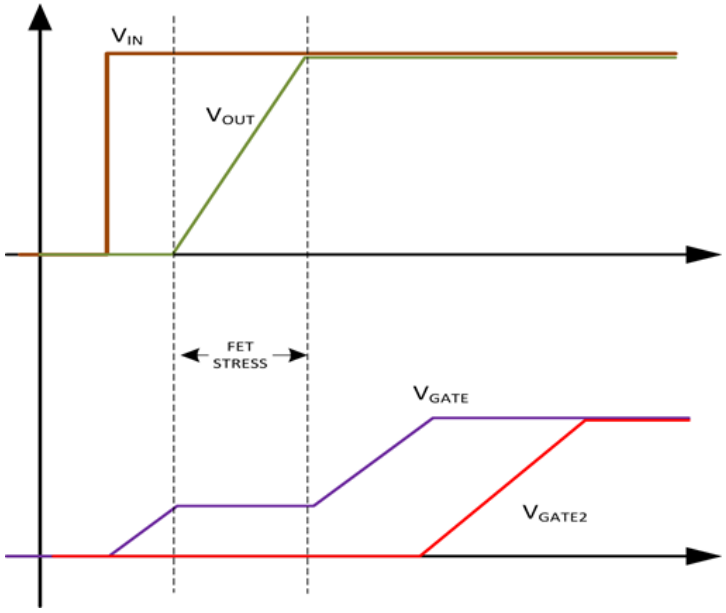


Figure 10. Gate 2 Operation During Start-Up

Feature Description (continued)

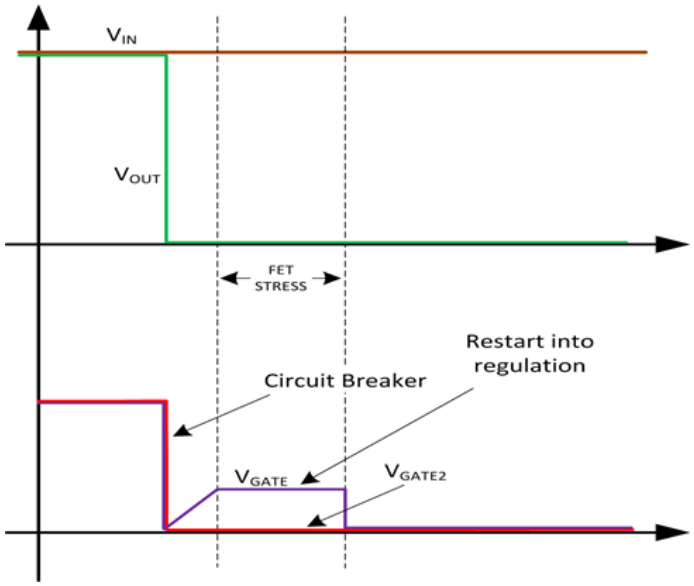


Figure 11. Gate2 Operation During Hot Short

8.3.5 OR-ing

The TPS23523 features integrated OR-ing that controls the external MOSFET in a way to emulate an ideal diode. The TPS23523 will regulate the forward drop across the OR-ing FET to 25 mV. This is accomplished by controlling the V_{GS} of the MOSFET. As the current decreases the V_{GS} is also decreased, which effectively increases the R_{DSON} of the MOSFET. This process is regulated with a low gain amplifier that is gate (OR-ing FET) pole compensated. The lower gain helps ensure stability over various operating conditions. The regulating amplifier ensures that there is no DC reverse current.

However, the amplifier is not very fast and thus it is paired with a fast comparator. This comparator quickly turns off the FET if there is significant reverse current detected.

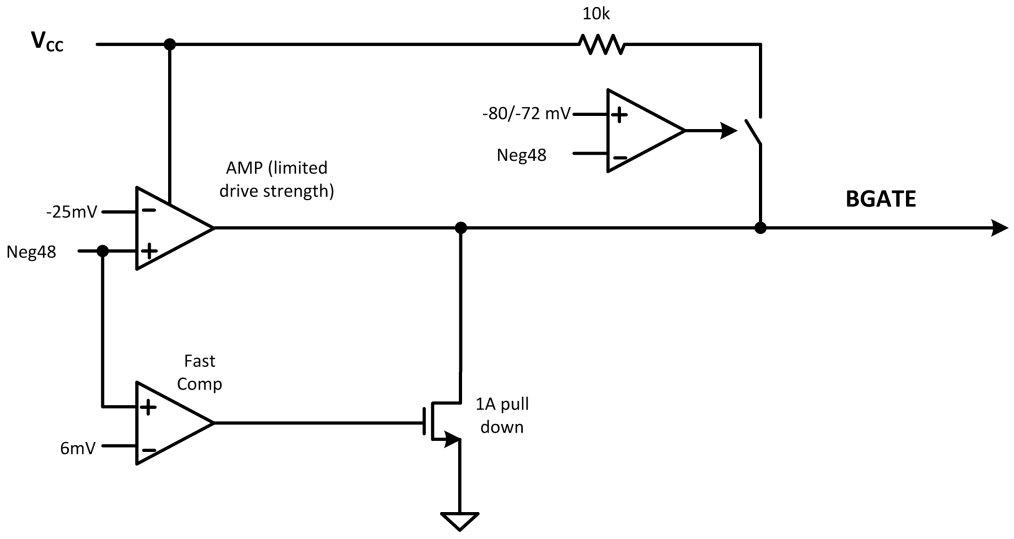


Figure 12. Simplified Diagram of OR-ing Block

8.4 Device Functional Modes

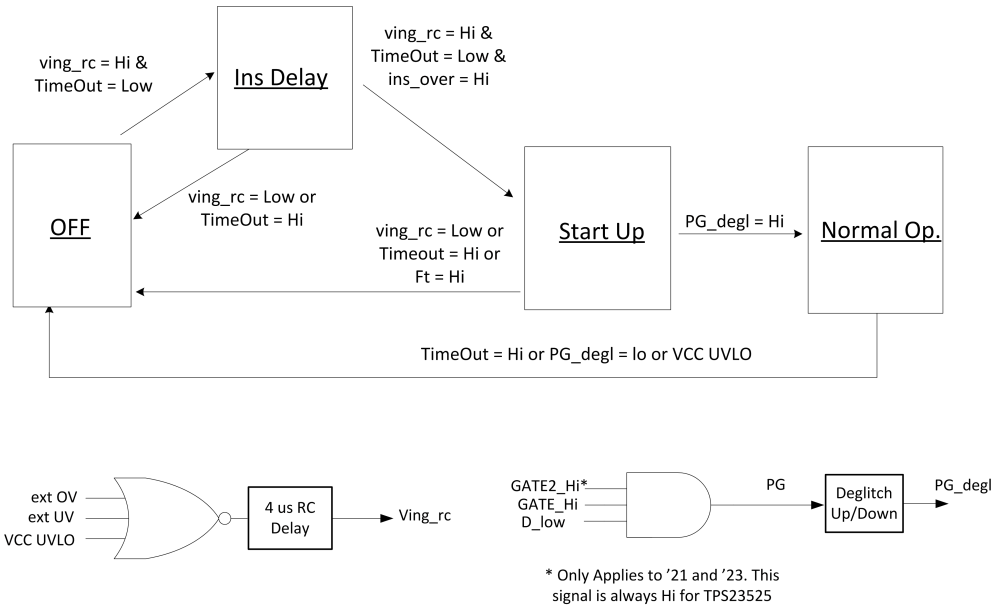


Figure 13. Simplified Hot Swap State Machine

The Figure above shows a simplified state machine of the hot swap controller. It has 4 distinct operating states and the controller switches between these states based on the following signals:

- Ving_rc: This means that both the input voltage is in the right range and the IC has power with Vcc. A 4-µs delay is added for deglitching. If the input voltage is above the OV threshold, input voltage is below the UV threshold, or VCC is below its internal UVLO, Ving_rc will be low.
- TimeOut: This signal comes from the timer block and will be asserted Hi if the IC has timed out due to an over-current condition. This signal is also Hi while the timer is going through the restart cycles. Once the cycles are completed this signal will go Low.
- ins_over: This signal states that the insertion delay has been completed and the hot swap is ready to start-up.
- FT: this is the fast trip signal coming from the fast trip comparator. It goes Hi if an extreme over current event is detected.
- PG: Internal Power good signal. This is high when the hot swap is fully on and the load can draw full power. For PG to be Hi, the GATE has to be Hi, GATE2 needs to be Hi, and the drain pin needs to be below 0.75 V.
- PG_degl: This is a deglitched version of the PG and is the signal used to move between states and controls the external PGb pin.

8.4.1 OFF State

In this state the hot swap FET is turned off and the controller is waiting to start-up. The controller can be in this state due to any of these scenarios:

- Input voltage is not in the valid range.
- The hot swap is in the cool down state and the timer is going through the retry cycle after a fault condition such as output hot short or over current.
- VCC is below its UVLO threshold and the IC doesn't have enough power to operate properly.

8.4.2 Insertion Delay State

In this state the hot swap FET is turned off and the controller is waiting for the insertion delay to finish. This allows the input supply to settle after a Hot Plug. If any of the following occur, the controller will be kicked back to the OFF state:

- Input voltage is not in the valid range.
- VCC is below its UVLO threshold and the IC doesn't have enough power to operate properly.

Device Functional Modes (continued)

Once the insertion delay is finished, the controller will move to the Start-up state.

8.4.3 Start-up State

In this state the controller is turning on and charging the output cap. The operation is set as follows:

- The SS pin is internally connected to the GATE pin to allow for output dv/dt control.
- Lower gate sourcing current is applied to the GATE pin to allow for smaller SS caps.
- The lower current limit setting of $V_{SNS,CL2}$ and a lower fast trip setting of $V_{SNS,FST2}$ is used to minimize the MOSFET stress in case of a fault condition.

If any of the following occur, the controller will be kicked back to the OFF state:

- Input voltage is not in the valid range.
- The timer times out due to over-current.
- VCC is below its UVLO threshold and the IC doesn't have enough power to operate properly.
- Fast trip is triggered.

Once the PG_degl signal goes Hi, the controller will move to the Normal Operation state.

8.4.4 Normal Operation State

In this state the hot swap is fully on and the operation is set as follows:

- The SS pin is disconnected from the GATE pin to improve transient response.
- The full gate sourcing current is used to improve transient response.
- The current limit and fast trip threshold are a function of the D pin to optimize the transient response while protecting the MOSFET.

If any of the following occur, the controller will be kicked back to the OFF state:

- PG_degl goes low.
- The timer times out due to over-current.
- VCC is below its UVLO threshold and the IC doesn't have enough power to operate properly.

Note that if the input voltage is outside the valid range or the fast trip is triggered, the hot swap FET will turn off, but the controller will not exit the Normal Operation state. In this case the PG signal would go low immediately. If this condition persists, the PG_degl will go low as well and the controller would move to the OFF state. This operation prevents the controller from re-starting the system during quick transients.

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS23523 is a hot swap controller for –48-V applications and is used to manage inrush current and protect downstream circuitry and the upstream bus in case of fault conditions. The following key scenarios should be considered when designing a –48-V hot swap circuit:

- Start Up.
- Output of a hot swap is shorted to ground while the hot swap is on. This is often referred to as a Hot Short.
- Powering up a board when the output and ground are shorted. This is usually called a start-into-short.
- Input lightning surge. Here it is usually desired to avoid damage to downstream circuitry and to avoid system restarts.

These scenarios place a lot of stress on the hot swap MOSFET and the board designer should take special care to ensure that the MOSFET stays within it's Safe Operating Area (SOA) under all of these conditions. A detailed design example is provided below and the key equations are written out. Note that solving all of these equations by hand is cumbersome and can result in errors. Instead, TI recommends using the TPS2352X Design Calculator provided on the product page.

9.2 Typical Application

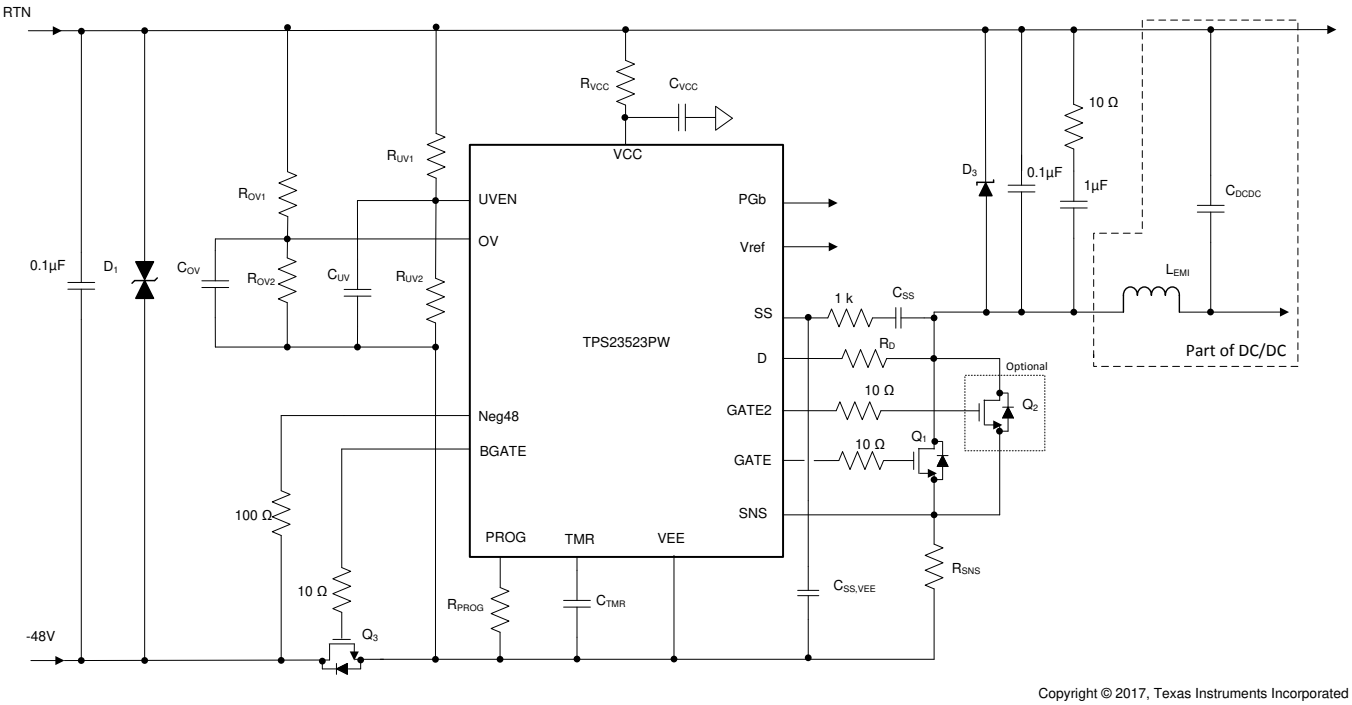


Figure 14. Application Diagram for Design Example

Typical Application (continued)

9.2.1 Design Requirements

The table below summarizes the design parameters that must be known before designing a hot swap circuit. When charging the output capacitor through the hot swap MOSFET, the FET's total energy dissipation equals the total energy stored in the output capacitor ($1/2CV^2$). Thus both the input voltage and output capacitance will determine the stress experienced by the MOSFET. The maximum load power will drive the current limit and sense resistor selection. In addition, the maximum load current, maximum ambient temperature, and the thermal properties of the PCB ($R_{\theta CA}$) will drive the selection of the MOSFET's R_{DSON} and the number of MOSFETs used. $R_{\theta CA}$ is a strong function of the layout and the amount of copper that is connected to the drain of the MOSFET. Air cooling will also reduce $R_{\theta CA}$ substantially. Finally, it's important to know what transients the circuit has to pass in order to size up the input protection accordingly.

Table 1. Design Requirements for a –38 V to –60 V, 400-W Protection Circuit

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range	–38 V to –60 V
Maximum Load Power	400 W
Output Capacitance	660 µF
Location of Output Cap	After EMI filter with ~5 µH of inductance.
Maximum Ambient Temperature	85°C
MOSFET $R_{\theta CA}$ (function of layout)	20°C/W
Pass "Hot-Short" on Output?	Yes
Pass a "Start into short"?	Yes
Is the load off until PG asserted?	Yes
Max Input Inductance	10 µH
Level of IEC61000-4-5 to pass	2-kV Line to Line with 2-Ω series impedance
Pass Reverse Hook Up	Yes

9.2.2 Detailed Design Procedure

9.2.2.1 Selecting R_{SNS}

Before selecting R_{SNS}, first compute the maximum load current. For this example the worst case load current happens at the minimum input voltage of 38 V. Thus the maximum current is 400 W/38 V = 10.5 A. To provide some margin, set the target current limit to 12 A and compute R_{SNS} using equation below:

$$R_{SNS,CLC} = \frac{V_{SNS,CL1}}{I_{CL1}} = \frac{25\ mV}{12\ A} = 2.08\ m\Omega \tag{11}$$

Use next available R_{SNS} of 2 mΩ.

9.2.2.2 Selecting Soft Start Setting: C_{SS} and $C_{SS,VEE}$

First, compute the minimum inrush current where the timer will trip using equation below.

$$I_{INR,TMR} = \frac{V_{SNS,TMR1}}{R_{SNS}} = \frac{1.5\ mV}{2\ m\Omega} = 0.75\ A \tag{12}$$

To avoid running the timer the inrush current needs to be sufficiently low. Target 0.4 A of inrush current to allow margin, and compute the target C_{SS} using equation below.

$$c_{SS} = \frac{c_{OUT,MAX} \times I_{GATE,SRS,START}}{I_{INR,TGT}} = \frac{792\ \mu F \times 20\ \mu A}{0.4\ A} = 39.6\ nF \tag{13}$$

Next choose, the next available C_{SS} greater than 39.6 nF. For this example 43 nF was used, which assumes a 33 nF and 10 nF cap in parallel. This results in an inrush current of 0.37 A at max C_{OUT} (792 µF) and inrush current of 0.31 A at typical C_{OUT} (660 µF). Also it is recommended to add a capacitor between the soft start pin and VEE ($C_{SS,VEE}$) to improve immunity to input voltage noise during soft start. It's recommended to chose a capacitor that's 3x larger than C_{SS}. In this case a 150 nF capacitor was chosen.

Finally the start-up time at maximum input voltage can be computed using the equation below:

$$T_{START}\left(V_{IN,MAX}\right) = \frac{c_{SS} \times V_{IN,MAX}}{I_{GATE,SRS,START}} = \frac{43\,nF \times 60\,V}{20\,\mu A} = 129\ ms \tag{14}$$

9.2.2.3 Selecting V_{DS} Switch Over Threshold

The V_{DS} threshold where the current limit switches from CL1 to CL2 can be programmed using R_D. In general a higher threshold improves ability to ride through voltage steps, brown outs, and other transients. However, a larger setting can also expose the MOSFET to more stress, because the larger current limit is now allowed at higher V_{DS} voltages. If there are no specific voltage step requirements, 20 V is a good starting point. Use the equation below to compute the target R_D.

$$R_D = 30\ k\Omega \times \left(\frac{V_{DS,SW}}{1.5\ V} - 1\right) = 370\ k\Omega \tag{15}$$

9.2.2.4 Timer Selection

The timer determines how long the hot swap can be in current limit before timing out and can be programmed using C_{TMR}. In general a longer time out (T_{TO}) improves ability to ride through voltage steps, brown outs, and other transients. However, a larger setting can also expose the MOSFET to more stress, because it takes longer for the FET to shut down during fault conditions. If there are no specific voltage step or transient requirements, 2 ms is a good starting point. Use the equation below to compute the target C_{TMR}. Choose the next available capacitor value of 15 nF, which results in a 2.25 ms time out.

$$C_{TMR} = \frac{T_{TO} \times I_{TMR,SRS}}{V_{TMR}} = \frac{2\ ms \times 10\ \mu A}{1.5\ V} = 13.3\,nF \tag{16}$$

9.2.2.5 MOSFET Selection and SOA Checks

When selecting MOSFETs for the –48 V application the three key parameters are: V_{DS} rating, R_{DSON}, and safe operating area (SOA). For this application the CSD19535KTT was selected to provide a 100 V V_{DS} rating, low R_{DSON}, and sufficient SOA. After selecting the MOSFET, it is important to double check that it has sufficient SOA to handle the key stress scenarios: start-up, output Hot Short, and Start into Short. MOSFET's SOA is usually specified at a case temperature of 25°C and should be derated based on the maximum case temperature expected in the application. Compute the maximum case temperature using the equation below. Note that the R_{DSON} will vary with temperature and solving the equation below could be a repetitive process. The CSD19535KTT, has a maximum 3.4 mΩ R_{DSON} at room temperature and is ~1.5x higher at 100°C. N stands for the number of MOSFETs used in parallel.

$$T_{C,MAX} = T_{A,MAX} + R_{\theta CA} \times \left(\frac{I_{LOAD,MAX}}{N}\right)^2 \times R_{DSON}\left(T_J\right) \tag{17}$$

$$T_{C,MAX} = 85\ °C + 20°\frac{C}{W} \times \left(10.5\ A\right)^2 \times \left(3.4 \times 1.5\ m\Omega\right) = 96.3\ °C \tag{18}$$

Next the stress the MOSFET will experience during operation should be compared to the FETs capability. First, consider the power up. The inrush current with max C_{OUT} will be 0.37 A and the inrush will last for 129 ms. Note that the power dissipation of the FET will start at $V_{IN,MAX} \times I_{INR}$ and reduce to zero as the V_{DS} of the MOSFET is reduced. The SOA curve of a typical MOSFET assume the same power dissipation for a given time. A conservative approach is to assume an equivalent power profile where $P_{FET} = V_{IN,MAX} \times I_{INR}$ for t = Tstart-up /2. In this instance, the SOA can be checked by looking at a 60 V, 0.4 A, 64.5 ms pulse. Based on the SOA of the CSD19535KTT, it can handle 60 V, 1.8 A for 10 ms and it can handle 60 V, 1 A for 100 ms. The SOA at T_C = 25°C for 64.5 ms can be extrapolated by approximating SOA vs time as a power function as shown in equations below:

$$I_{SOA}(t) = a \times t^{m} \tag{19}$$

$$m = \frac{\ln\left(I_{SOA}(t_1) / I_{SOA}(t_2)\right)}{\ln\left(t_1 / t_2\right)} = \frac{\ln\left(\frac{1.8\ A}{1\ A}\right)}{\ln\left(\frac{10\ ms}{100\ ms}\right)} = -0.25 \tag{20}$$

$$a = \frac{I_{SOA}(t_2)}{t_2^{m}} = \frac{1\ A}{(100\ ms)^{-0.25}} = 3.16\ A \times (ms)^{0.25} \tag{21}$$

$$I_{SOA}(64.5\ ms, 25\ °C) = 3.16\ A \times (ms)^{0.25} \times (64.5\ ms)^{-0.25} = 1.12\ A \tag{22}$$

Finally, the FET SOA needs to be derated based on the maximum case temperature as shown below. Note that the FET can handle 0.59 A, while it will have 0.37 A during start-up. Thus there is a lot of margin during this test condition.

$$I_{SOA}(64.5\ ms, T_{C,MAX}) = 1.12\ A \times \frac{175\ °C - 96.3\ °C}{175\ °C - 25\ °C} = 0.59\ A \tag{23}$$

A similar approach should be taken to compute the FETs SOA capability during a Hot Short and start into short. As shown in the following figure, during a start into short the gate is coming up very slowly due to a large capacitance tied to the gate through the SS pin. Thus it is more stressful than a Hot Short and should be used for worst case SOA calculations. To compare the FET stress during start-up into short to the SOA curves the stress needs to be approximated as a square pulse as showing in the figure below. In this example, the stress is approximated with a 1.1 ms (Teq), 1.5 A, 60 V pulse. The FET can handle 6 A, 60 V for 1 ms and 1.8 A, 60 V for 10 ms. Using approximation and temp derating as shown earlier, the FET's capability can be computed as 3 A, 60 V, for 1.1 ms at 96°C. 3 A is significantly larger than 1.5 A implying good margin.

Figure 15. Teq During a Start Into a Short

The final operating point to check is the operation with high current and V_{DS} just below the $V_{DS,SW}$ threshold. In this example, the time out would be 1.1ms (one half of the time out at Vd = 0 V), the current will be 12.5 A, and the voltage would be 20 V. Looking up the SOA curve, the FET can handle 30 A, 20 V for 1 ms and 10 A, 20 V for 10 ms. Repeating previously shown approximations and temp derating, the FET's capability is computed to be 16 A, 20 V, for 1.1 ms at 96°C. Again this is below the worst case operating point of 12.5 A and 20 V suggesting good margin.

9.2.2.6 Input Cap, Input TVS, and OR-ing FET selection

This design example is sized for an application that needs to pass a 2 kV, 2Ω lightning strike per IEC61000-4-5. This equates to almost 1000 A of input current that needs to be clamped. In addition, the design needs to pass reverse hook up and thus the TVS needs to be bi directional. A ceramic transient voltage suppressor (2x B72540T6500S162) CT2220K50E2G was used to clamp this huge surge of current. According to it's datasheet it can clamp 500 A of current to 150 V. Note that the lightning strike can be positive or negative. The worst case voltage is dropped across the OR-ing FETs when the strike is positive (–48 V line goes above RTN). If the output of the OR-ing is –48 V and the input goes to +150 V that is a 200 V drop. Thus BSC320N20NS3 was chosen for the OR-ing FETs. This is a 200 V FET with a 32 mΩ R_{DSON} at room temperature. 2 of these were used in parallel to minimize power loss and manage thermal. Finally a 0.1 µF input bypass cap is recommended.

9.2.2.7 EMI Filter Consideration

In this example it is assumed that the EMI filter is right after the hot swap and the bulk cap is after the EMI filter. The EMI filter adds significant inductance and needs to be accounted for. During a Hot Short, the inductor builds up significant current that needs to go somewhere after the FET opens. For that a free wheeling diode should be used along with a snubber. For this example a 150 V, SMA diode was used: STPS1150A. The snubber consisted of a 10-Ω resistor in series with a 1-µF ceramic capacitor. In addition a 0.1-µF ceramic cap was tied directly on the output.

9.2.2.8 Undervoltage and Overvoltage Settings

Both the threshold and hysteresis can be programmed for undervoltage and overvoltage protection. In general the rising UV threshold should be set sufficiently below the minimum input voltage and the falling OV threshold should be set sufficiently above the maximum input voltage to account for tolerances. For this example a rising UV threshold of 37 V and a falling UV threshold of 35 V was chosen as the target. First, choose R_{UV1} based on the 2 V UV hysteresis as shown below.

$$R_{UV1} = \frac{V_{UV,hyst,tgt}}{i_{UV,hyst}} = \frac{2\ V}{10\ \mu A} = 200\ k\Omega \quad (24)$$

Once R_{UV1} is known R_{UV2} can be computed based on the target rising UV threshold as shown below.

$$R_{UV2} = \frac{R_{UV1}}{V_{UV,TGT,Rising} - 1\ V} = \frac{200\ k\Omega}{37\ V - 1\ V} = 5.56\ k\Omega \quad (25)$$

The OV setting can be programmed in a similar fashion as shown in equations below.

$$R_{OV1} = \frac{V_{OV,hyst,tgt}}{i_{OV,hyst}} = \frac{3\ V}{10\ \mu A} = 300\ k\Omega \quad (26)$$

(27)

$$R_{OV2} = \frac{R_{OV1}}{V_{OV,TGT,Rising} - 1\ V} = \frac{300\ k\Omega}{65\ V - 1\ V} = 4.68\ k\Omega \quad (28)$$

Optional filtering capacitors can be added to the UV and OV to improve immunity to noise and transients on the input bus. These should be tuned based on system requirements and input inductance. In this example place holders were added to the PCB, but the components were not populated.

9.2.2.9 Choosing R_{VCC} and C_{VCC}

The VCC is used as internal supply rail and is a shunt regulator. To ensure stability of internal loop a minimum of 0.1 µF is required for C_{VCC}. To ensure reasonable power on time it is recommended to keep C_{VCC} below 1 µF. R_{VCC} should be sized in such a way to ensure that sufficient current is supplied to the IC at minimum operating voltage corresponding to the falling UV threshold. To allow for some margin it is recommended that the current through R_{VCC} is at least 1.2x of $I_{Q,MAX}$ when RTN = Falling UV threshold and VCC = 10 V (minimum recommended operating voltage on VCC). For this example R_{VCC} of 16.2 kΩ was used.

9.2.2.10 Power Good Interface to Downstream DC/DC

It's critical to keep the downstream DC/DC off while the hot swap is charging the bulk capacitor. This can be accomplished through the PGb pin. Note that the VEE of the hot swap and the DC/DC are different and the Power Good can not be directly tied to the EN or UV of the DC/DC. The application circuit below provides a simple way to control the downstream converter with the PGb pin of the hot swap.

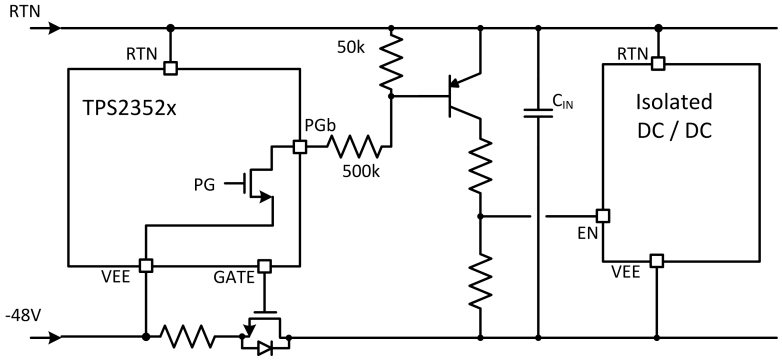


Figure 16. Interface to DC/DC

9.2.3 Application Curves

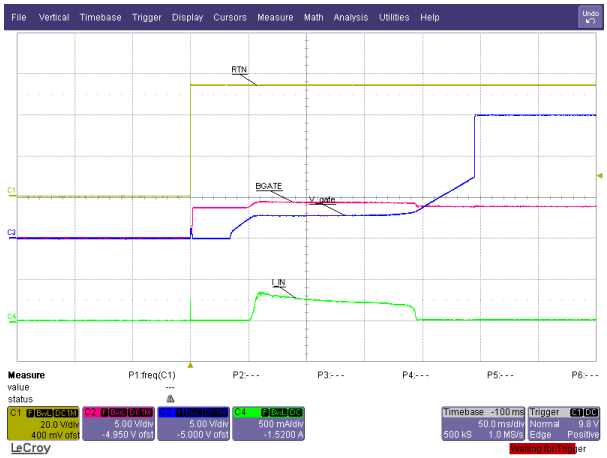


Figure 17. Start Up (Vin = 54 V)

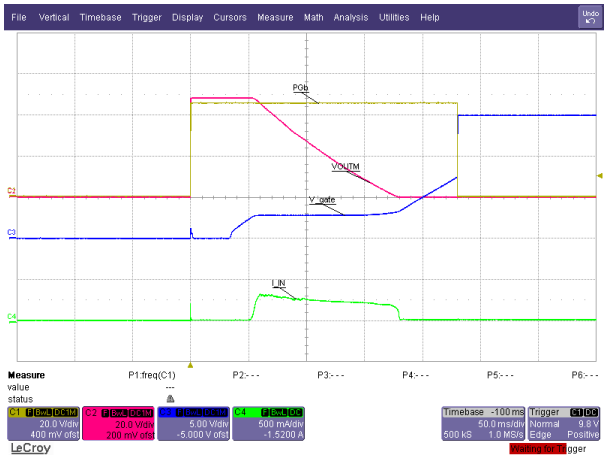


Figure 18. Start Up (Vin = 54 V)

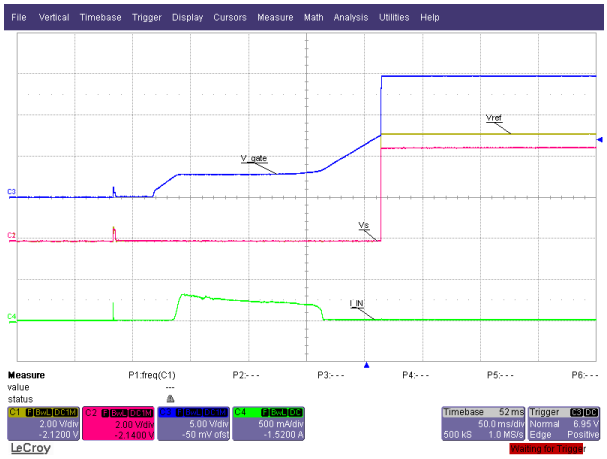


Figure 19. Start Up (Vin = 54 V)

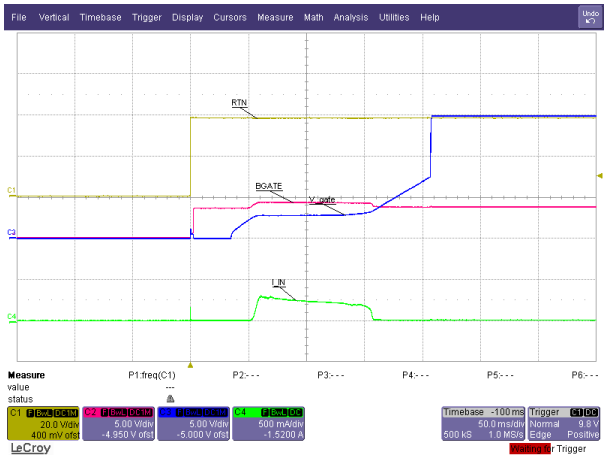


Figure 20. Start Up (Vin = 38 V)

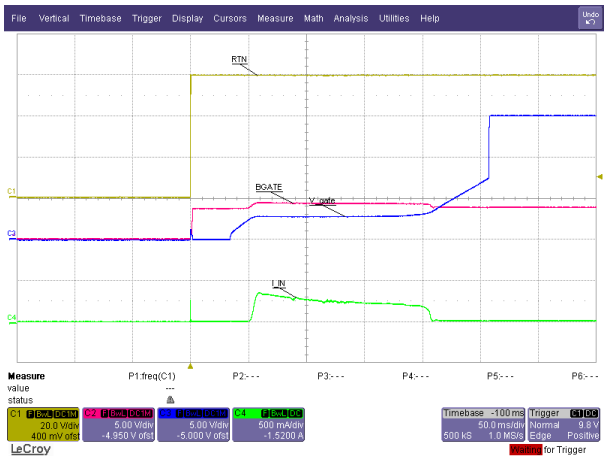


Figure 21. Start Up (Vin = 60 V)

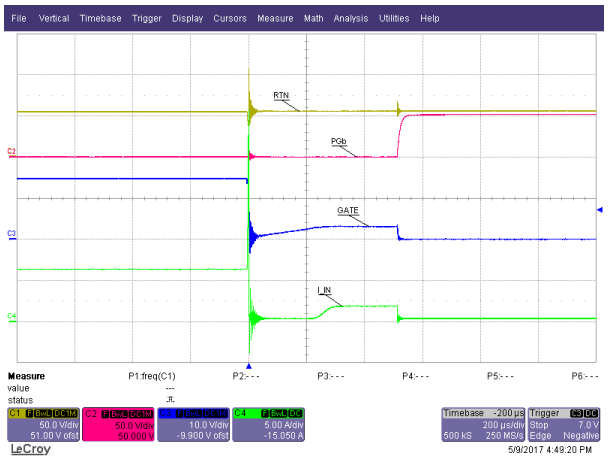


Figure 22. Hot Short (Vin = 54 V)

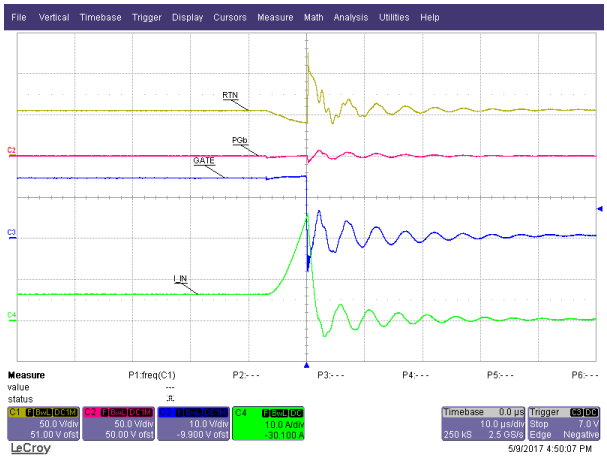


Figure 23. Hot Short (Vin = 54 V)

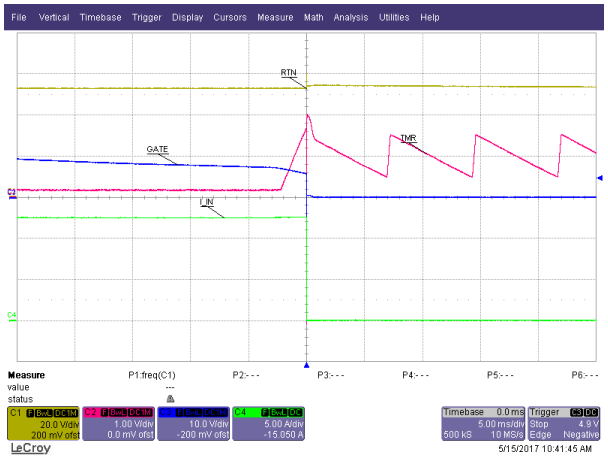


Figure 24. Gradual Over Current

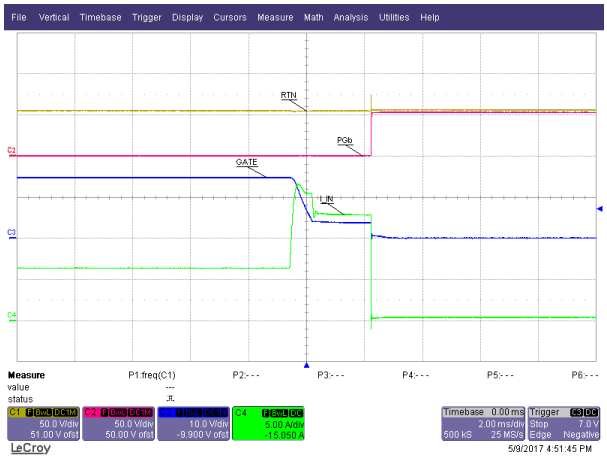


Figure 25. Load Step Into Current Limit

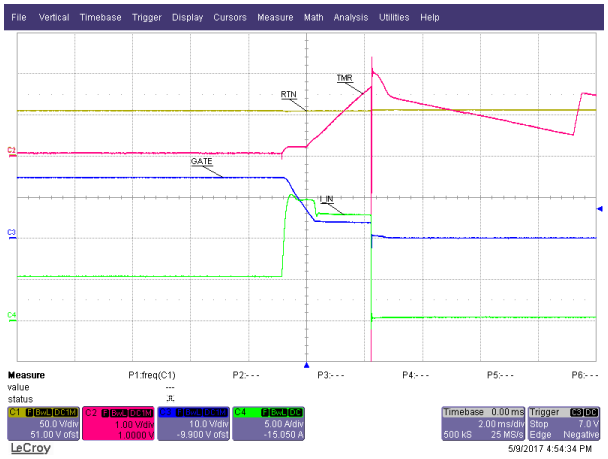


Figure 26. Load Step Into Current Limit

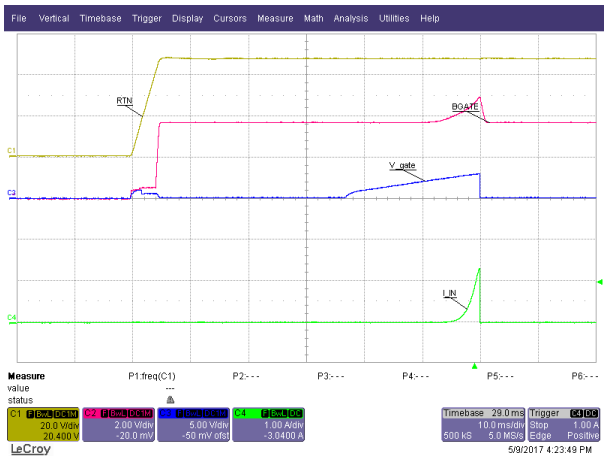


Figure 27. Start Into Short

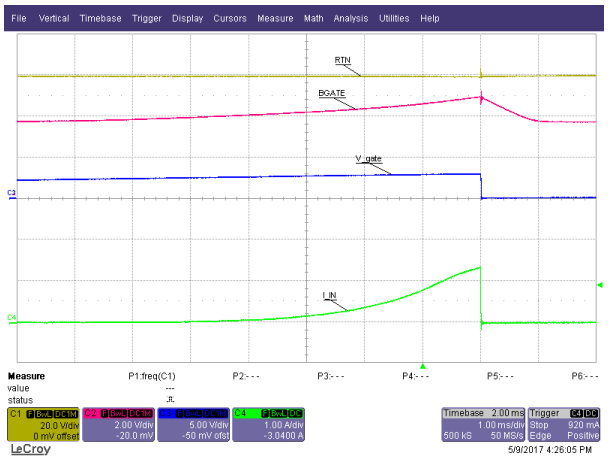
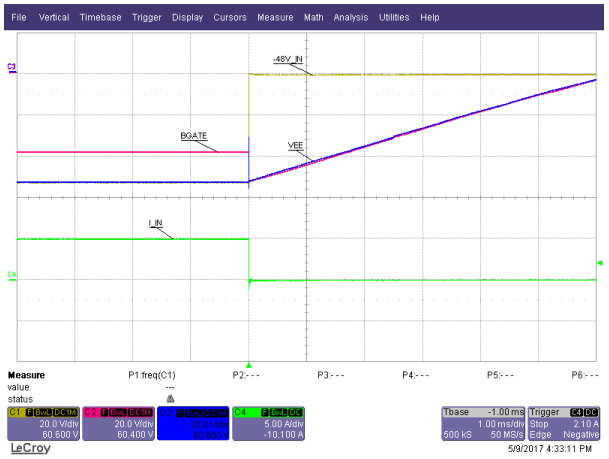
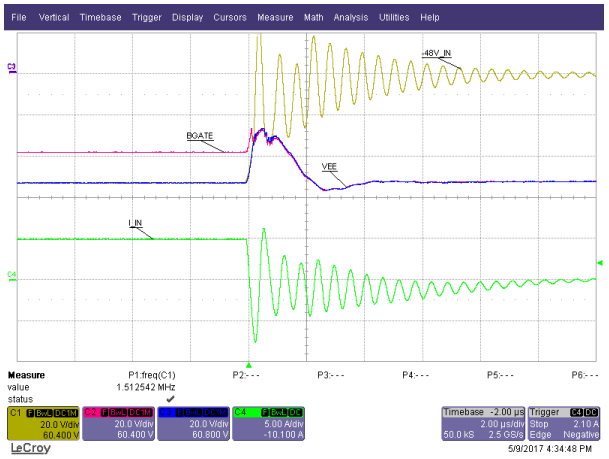


Figure 28. Start Into Short



5-A load

Figure 29. Short on Vin



5-A load

Figure 30. Short on Vin

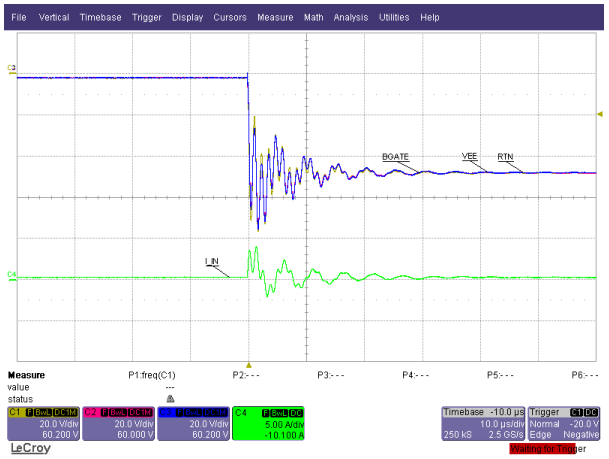
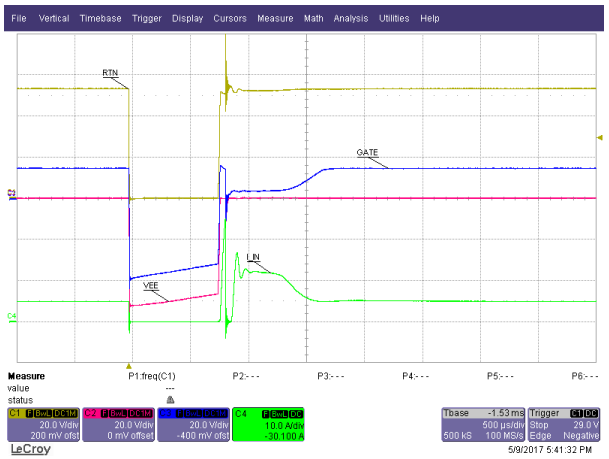


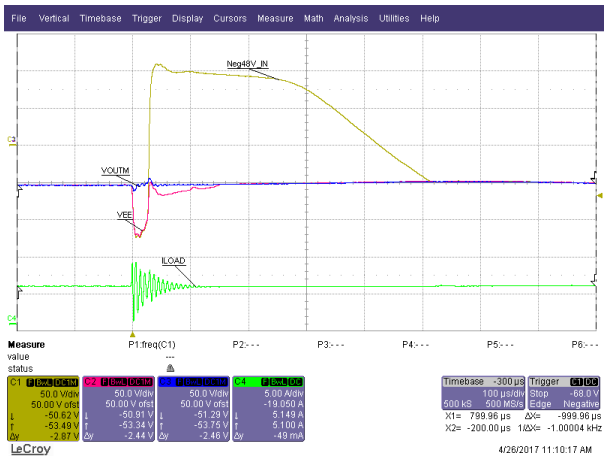
Figure 31. Reverse Hook Up

Figure 32. Reverse Hook Up



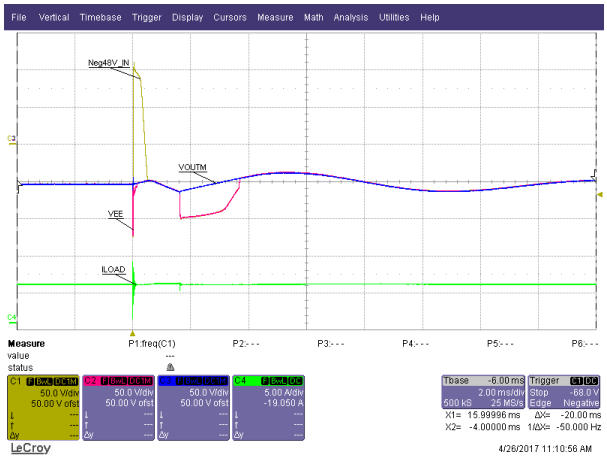
5-A load

Figure 33. 1-ms Brown Out



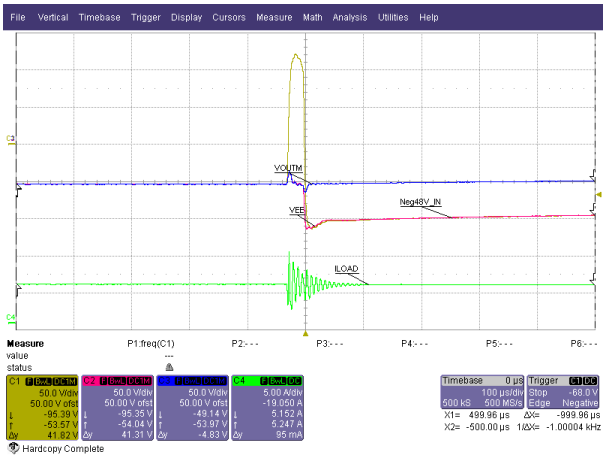
6-A load, per IEC61000-4-5

Figure 34. 2 kV (2 Ω) Lightning Surge



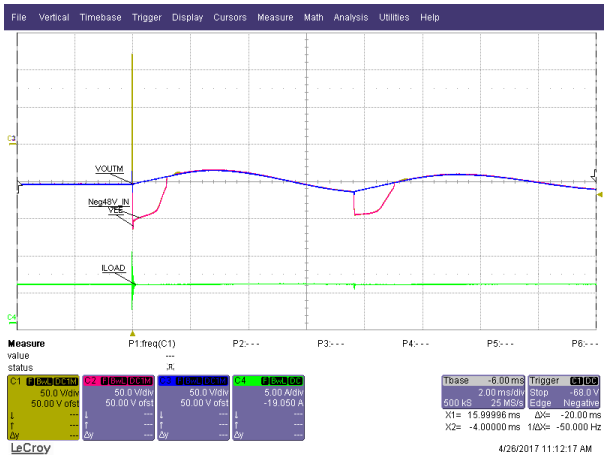
6-A load, per IEC61000-4-5

Figure 35. 2 kV (2 Ω) Lightning Surge



6-A load, per IEC61000-4-5

Figure 36. -2 kV (2 Ω) Lightning Surge



6-A load, per IEC61000-4-5

Figure 37. -2 kV (2 Ω) Lightning Surge

10 Power Supply Recommendations

In general, the TPS23523 is designed to have robust operation from a non-ideal –48 V bus with various transients such as the lightning surge. The IC is powered through RVCC making it more immune to supply drop outs and high voltage spikes. Regardless, TI recommends following several key precautions:

- Always test the solution with the various transients that can be encountered in the systems. This especially applies to transients that were not tested with TI's EVM.
- If large input ripple is expected during start-up, increase the ratio of $C_{SS,\ VEE}$ to C_{SS} to reduce input current ripple at start-up.
- Operating from large input inductance (>40 µH) can cause instability to the current limit loop or oscillations during start-up. Add a capacitor from Gate to VEE to help stabilize the current limit loop. Add an input snubber if oscillations are observed at start-up.

11 Layout

11.1 Layout Guidelines

There are several things to keep in mind during layout of the TPS23523 circuit:

- The VEE and SNS pin need to have a Kelvin Sense connection to the sense resistor.
- The VEE trace carries current and needs to be thick and short in order to minimize IR drop and to avoid introducing current sensing error.
- It is recommended to use a net-tie to separate the power plane coming into the R_{SNS} and the Kelvin connection to VEE.
- Connect the Neg48Vx filtering caps, UVEN resistor divider, OV resistor divider, and TMR cap to the "VEE" to insure maximum accuracy.
- The filtering caps on Neg48V and SNS should be placed as close to the IC as possible.

11.2 Layout Example

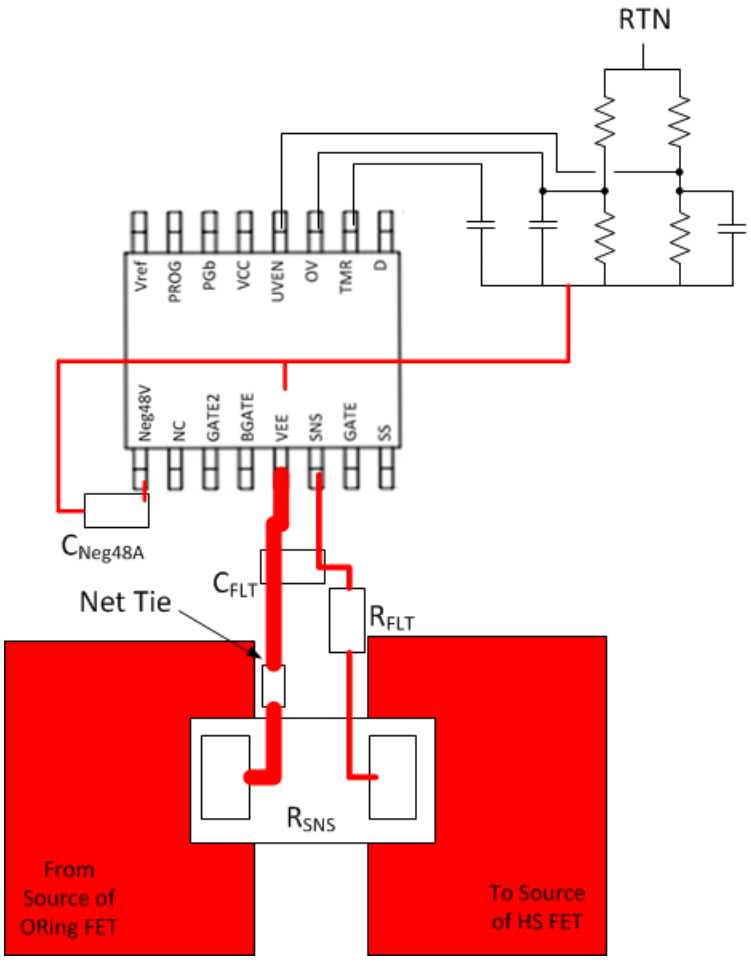


Figure 38. Layout Example

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デベロッパー・ネットワークの製品に関する免責事項

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12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください。

- 『TPS23525EVM-815評価基板ユーザー・ガイド』(SLVUB36)

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

12.5 商標

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12.6 静電気放電に関する注意事項

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS23523PWR	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	23523
TPS23523PWR.B	Active	Production	TSSOP (PW) | 16	2000 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	23523
TPS23523PWT	Active	Production	TSSOP (PW) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	23523
TPS23523PWT.B	Active	Production	TSSOP (PW) | 16	250 | SMALL T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	23523

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

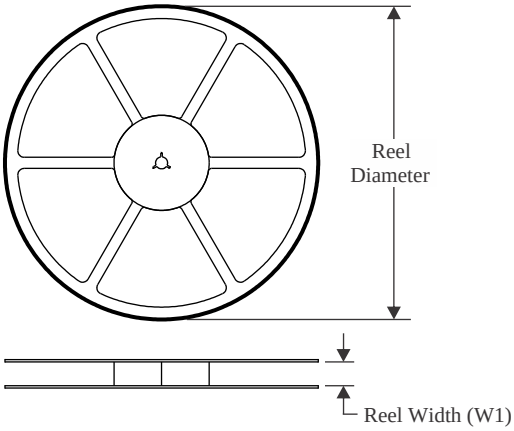
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

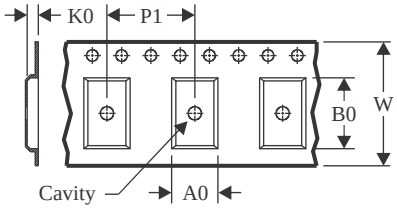
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

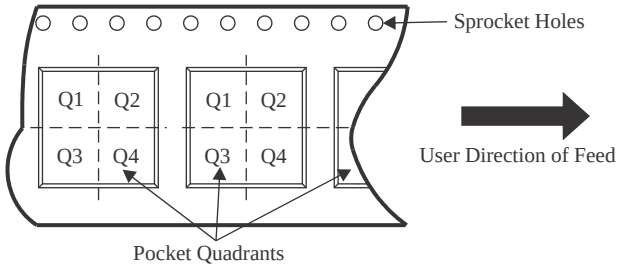


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

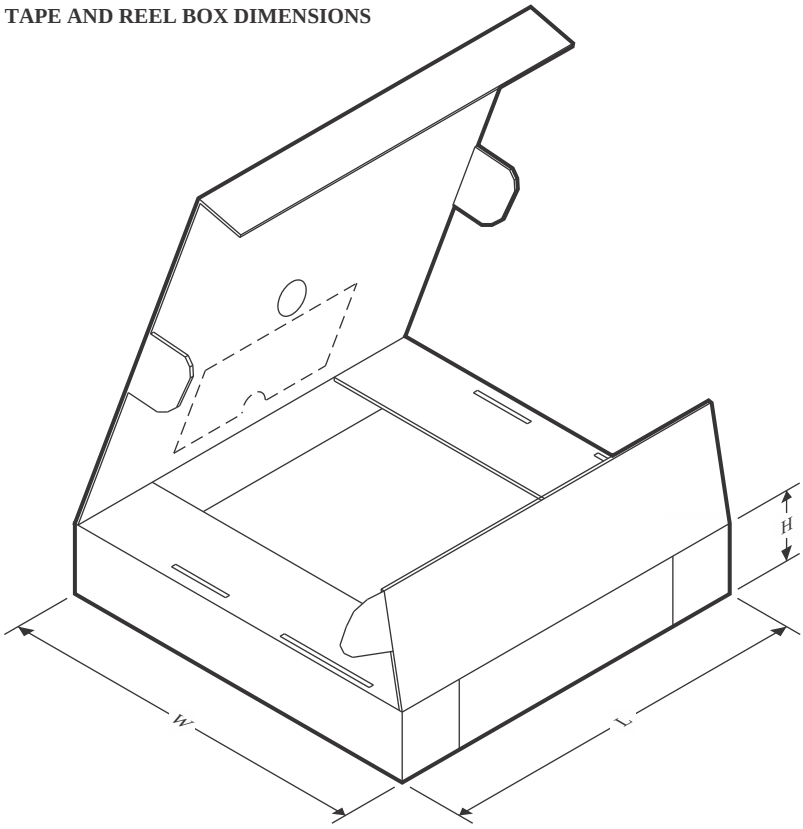
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS23523PWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TPS23523PWT	TSSOP	PW	16	250	180.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

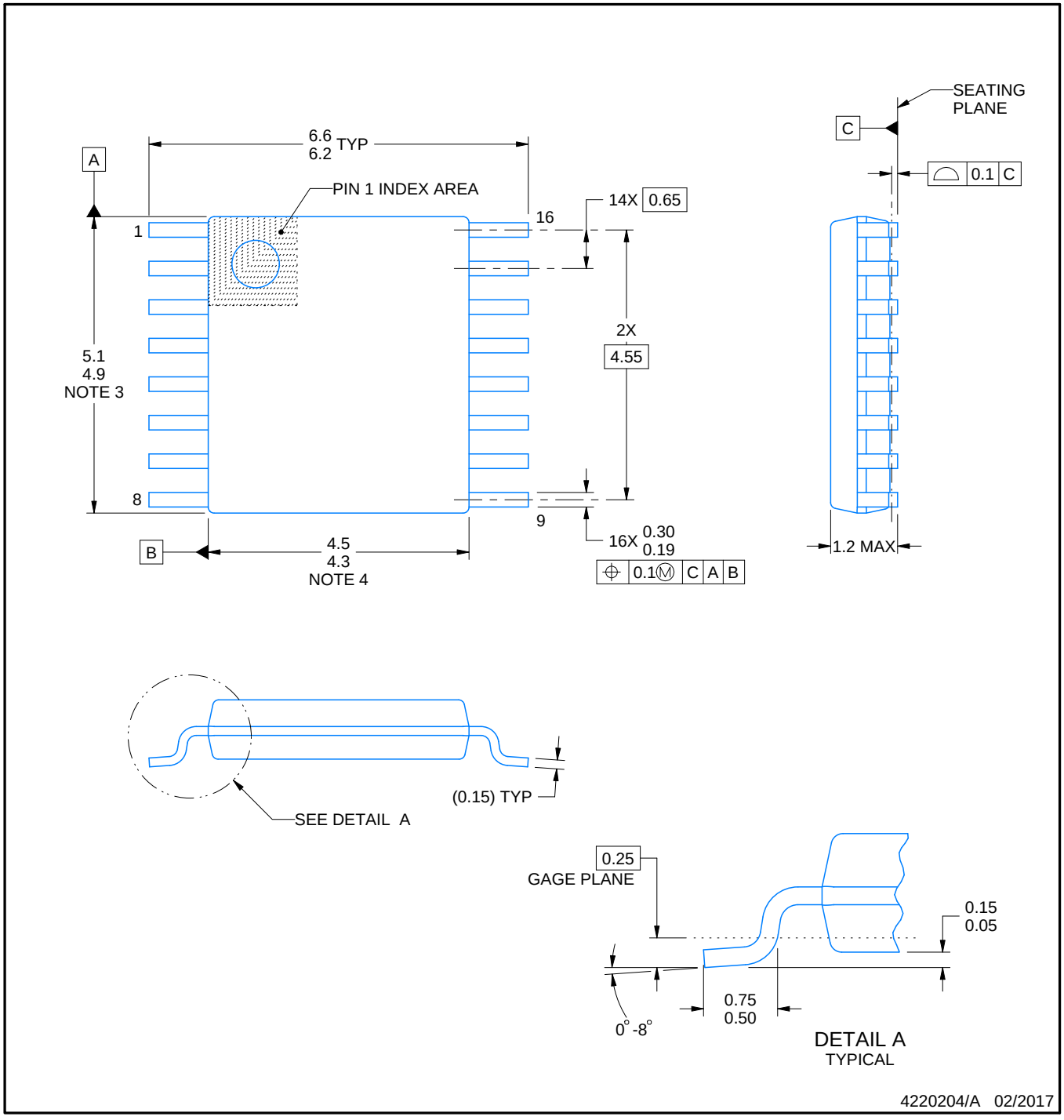
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS23523PWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TPS23523PWT	TSSOP	PW	16	250	210.0	185.0	35.0

PACKAGE OUTLINE

PW0016A

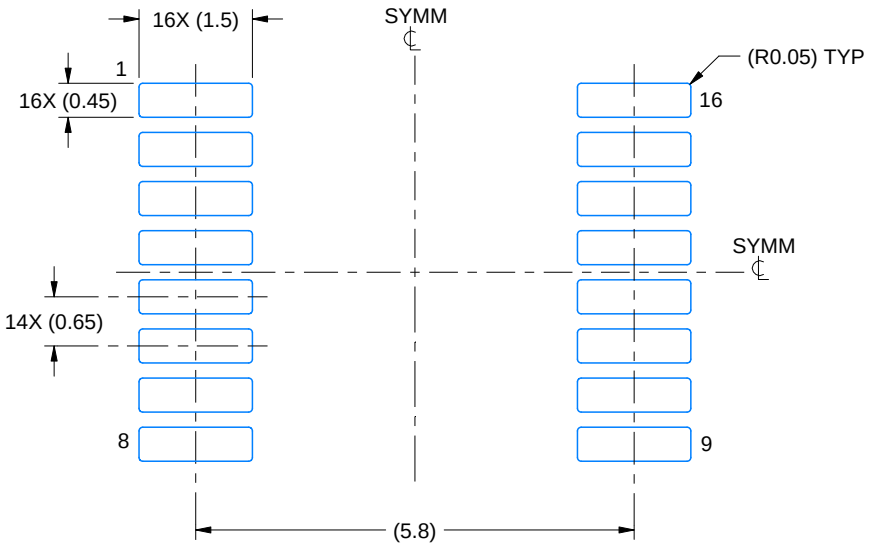
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

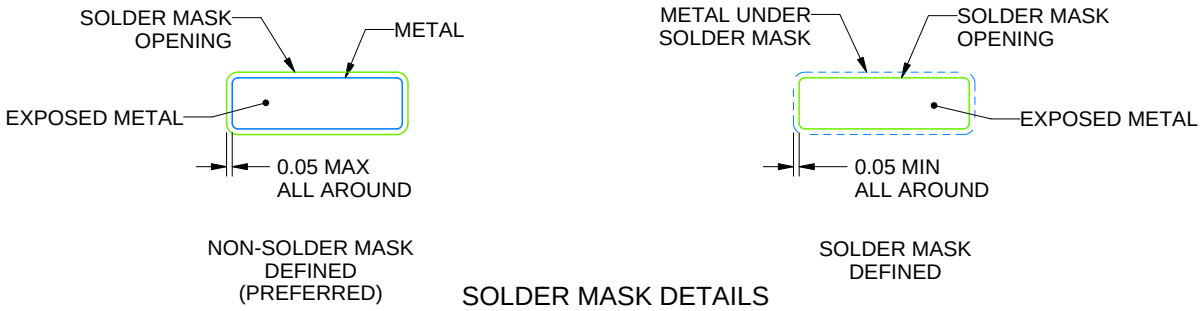


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

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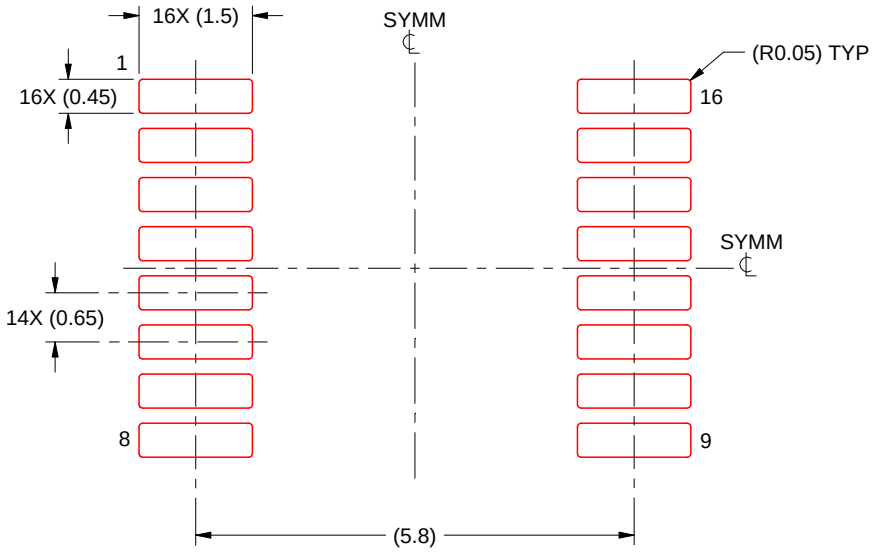
NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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