TPS25921x 4.5V - 18V eFuse with Precise Current Limit and Over Voltage Protection

1 Features

- 4.5 V – 18 V Operating Voltage, 20 V (Max)
- 90 mΩ $R_{DS(ON)}$ (Typical)
- 0.4 A to 1.6 A Adjustable Current Limit
- ±2% Accurate I_{LIMIT} at 1A at 25°C
- ±3% Overvoltage, Undervoltage Threshold
- Programmable dV_O/dt Control
- Fault Output for Thermal Shutdown, UVLO and OVP
- -40°C to 125°C Junction Temperature Range
- Auto-Retry and Latch-Off Versions
- UL2367 Recognized - File No. E169910
- UL60950 - Safe during Single Point Failure Test

2 Applications

- White Goods, Appliances
- Set Top Boxes, DVD and Gaming Consoles
- HDD and SSD drives
- Smart Meters, Gas Analyzers
- Smart Load Switch
- USB Switch
- Adapter Power Devices

3 Description

The TPS25921 is a compact, feature rich eFuse with a full suite of protection functions. The wide operating voltage allows control of many popular DC buses. The precise ±2% current limit, at room temperature, provides excellent accuracy making the TPS25921 well suited for many system protection applications.

Load, source and device protection are provided with multiple programmable features including overcurrent, overvoltage and undervoltage. 3% threshold accuracy for UV and OV, ensures tight supervision of bus voltages, eliminating the need for supervisor circuitry. Fault flag output ($\overline{FLT}$) is provided for system status monitoring and down stream load control.

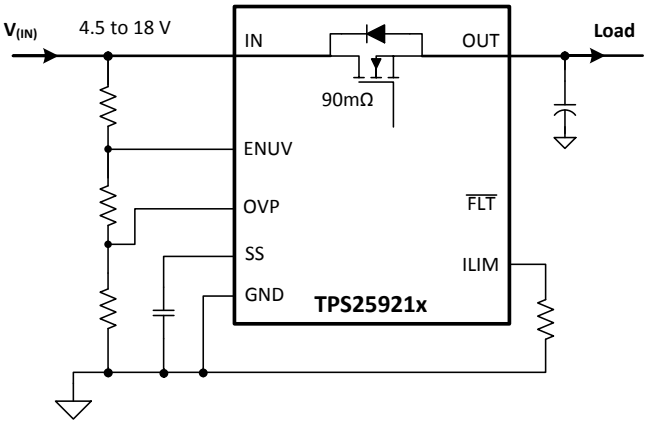
For hot-plug-in boards, TPS25921 provides in-rush current control and programmable output ramp-rate. Output ramp rate is programmable using a capacitor at soft-start (SS) pin, for maximum design flexibility.

Device Information(1)

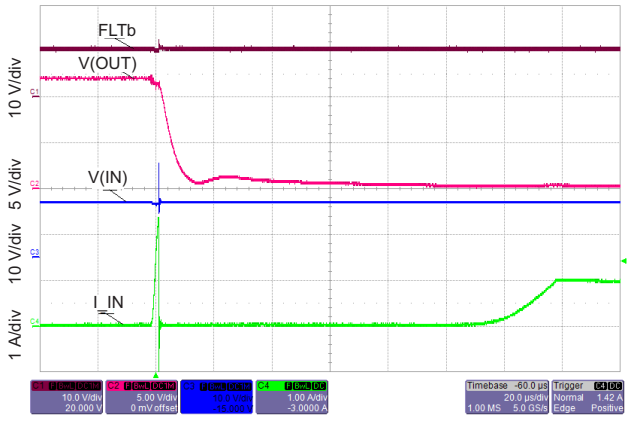
PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS25921A	SOIC	4.90mm x 3.91mm
TPS25921L		

(1) For all available packages, see the orderable addendum at the end of the datasheet.

4 Application Schematic



12V Short Circuit Response



TIME = 20 µs/div

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5 Revision History

Changes from Revision B (August 2015) to Revision C **Page**

- Changed Equation 2 From: 0.07 To: 70 pF, and added text "where $C_{(ss)}$ is in Farad" ... 14
- Changed Equation 21 From: (1 + 0.07) To: (1 x10^{-9} + 70 x 10^{-12}) ... 22
- Changed Equation 26 From: (4.7 + 0.07) To: (4.7 x10^{-9} + 70 x 10^{-12}) ... 22

Changes from Revision A (March 2015) to Revision B **Page**

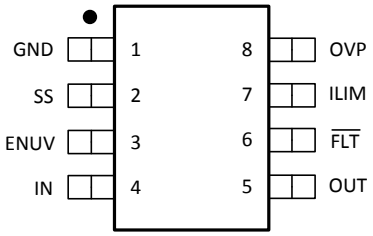
- Changed t_{ss} in *Timing Requirements* From: $V_{(OUT)}$ = 11.7 V To $V_{(OUT)}$ = 11 V and $C_{(SS)}$ = 1 nF To: $C_{(SS)}$ = 1.2 nF ... 6

Changes from Original (August 2014) to Revision A **Page**

- Changed *Features* From: UL2367 Recognition Pending To: UL2367 Recognized - File No. E169910 ... 1
- Moved the Storage temperature range From: *Handling Ratings*table To : *Absolute Maximum Ratings* ... 3
- Changed the *Handling Ratings* table To: *ESD Ratings* ... 3
- Changed Equation 31 From: $V_{(IN)}$ x $I_{(LOAD)}$ To: $V_{(IN)}$ + $I_{(LOAD)}$. ... 28

6 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



Pin Functions

NAME	NUMBER	DESCRIPTION
GND	1	Ground.
SS	2	A capacitor from this pin to GND sets the ramp rate of output voltage at device turn-on.
ENUV	3	Input for setting programmable undervoltage lockout threshold. An undervoltage event will open internal FET and assert $\overline{FLT}$ to indicate power-failure. When pulled to GND, resets the thermal fault latch in TPS25921L.
IN	4	Power Input and supply voltage of the device.
OUT	5	Power Output of the device.
$\overline{FLT}$	6	Fault event indicator, goes low to indicate fault condition due to Undervoltage, Overvoltage, and Thermal shutdown event. A nuisance fast trip does not trigger fault. It is an open drain output.
ILIM	7	A resistor from this pin to GND will set the overload and short circuit limit.
OVP	8	Input for setting programmable overvoltage protection threshold. An overvoltage event will open the internal FET and assert $\overline{FLT}$ to indicate overvoltage.

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		VALUE (2)		UNIT
		MIN	MAX	
Input voltage range	IN, OUT, ENUV, OVP, $\overline{FLT}$	–0.3	20	V
	IN (10 ms Transient)		22	
	ILIM, SS	–0.3	7	
Sink current	SS		5	mA
	$\overline{FLT}$		100	mA
Source current	ILIM, SS, $\overline{FLT}$	Internally Limited		
Maximum junction temperature, T_J		Internally Limited		°C
Storage temperature range, T_{stg}		-65	150	°C

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential voltages, are with respect to network ground terminal.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 (2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
Input voltage range	IN	4.5		18	V
	OUT, OVP, ENUV, $\overline{FLT}$	0		18	
	SS	0		6	
	ILIM	0		3.3	
Resistance	ILIM	35.7	95.3	158	kΩ
External capacitance	OUT	0.1	1		µF
	SS		1	1000	nF
Operating junction temperature range, T_J		–40	25	125	°C

7.4 Thermal Characteristics(1)

THERMAL METRIC		TPS2592xx	UNIT
		SOIC (8) PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	120.8	°C/W
$R_{\theta JCtop}$	Junction-to-case (top) thermal resistance	65.5	
$R_{\theta JB}$	Junction-to-board thermal resistance	51.8	
ψ_{JT}	Junction-to-top characterization parameter	17.4	
ψ_{JB}	Junction-to-board characterization parameter	61.2	

(1) For more information about traditional and new thermal metrics, see the IC Package Thermal Metrics application report, SPRA953.

7.5 Electrical Characteristics

Conditions (unless otherwise noted) are –40°C ≤ T_J ≤ 125°C, 4.5 V ≤ $V_{(IN)}$ ≤ 18 V, $V_{(EN\ UV)}$ = 2 V, $V_{(OVP)}$ = 0 V, $R_{(ILIM)}$ = 95.3 kΩ, C_{SS} = OPEN, FLT = OPEN. Positive current into terminals. All voltages are referenced to GND (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE AND INTERNAL UNDERVOLTAGE LOCKOUT						
$V_{(IN)}$	Operating Input Voltage		4.5		18	V
$V_{(UVR)}$	UVLO Threshold, Rising		4.10	4.26	4.40	V
$V_{(UVHys)}$	UVLO Hysteresis		168	224	279	mV
$I_{Q(\ ON)}$	Supply Current, Enabled	$V_{(ENUV)}$ = 2 V, $V_{(IN)}$ = 12 V	0.22	0.41	0.58	mA
$I_{Q(\ OFF)}$	Supply Current, Disabled	$V_{(ENUV)}$ = 0 V, $V_{(IN)}$ = 12 V	0.08	0.132	0.20	mA
OVERVOLTAGE PROTECTION (OVP) INPUT						
$V_{(OVPR)}$	Overvoltage Threshold Voltage, Rising		1.35	1.39	1.43	V
$V_{(OVPF)}$	Overvoltage Threshold Voltage, Falling		1.30	1.34	1.37	V
$I_{(OVP)}$	OVP Input Leakage Current	0V ≤ $V_{(OVP)}$ ≤ 18 V	–100	0	100	nA
ENABLE AND UNDERVOLTAGE LOCKOUT (ENUV) INPUT						
$V_{(ENR)}$	ENUV Threshold voltage, rising		1.36	1.39	1.42	V
$V_{(ENF)}$	ENUV Threshold voltage, falling		1.30	1.34	1.37	V
$V_{(ENF\_RST)}$	ENUV Threshold voltage to reset thermal fault, falling		0.5	0.61	0.8	V
I_{EN}	EN Input leakage current	0 ≤ $V_{(ENUV)}$ ≤ 18 V	–100	0	100	nA
SOFT START: OUTPUT RAMP CONTROL (SS)						
$I_{(SS)}$	SS charging current	$V_{(SS)}$ = 0 V	0.9	1.04	1.2	µA
$R_{(SS)}$	SS discharging resistance	$V_{(ENUV)}$ = 0 V, $I_{(SS)}$ = 10 mA sinking	60	70	85	Ω
$V_{(SSmax)}$	SS maximum capacitor voltage			5.5		V
$GAIN_{(SS)}$	SS to OUT gain	$\Delta V_{(OUT)}/\Delta V_{(SS)}$	4.81	4.86	4.92	V/V
CURRENT LIMIT PROGRAMMING (ILIM)						
$I_{(ILIM)}$	ILIM Bias current		6	10	16	µA
I_{LIMIT}	Current Limit(1)	$R_{(ILIM)}$ = 35.7 kΩ, ($V_{(IN)}$ - $V_{(OUT)}$) = 1 V	0.284	0.368	0.452	A
		$R_{(ILIM)}$ = 45.3 kΩ, ($V_{(IN)}$ - $V_{(OUT)}$) = 1 V	0.394	0.471	0.547	
		$R_{(ILIM)}$ = 95.3 kΩ, ($V_{(IN)}$ - $V_{(OUT)}$) = 1 V, T_A = T_J= 25°C	0.98	1.0	1.02	
		$R_{(ILIM)}$ = 95.3 kΩ, ($V_{(IN)}$ - $V_{(OUT)}$) = 1 V	0.93	1.0	1.062	
		$R_{(ILIM)}$ = 150 kΩ, ($V_{(IN)}$ - $V_{(OUT)}$) = 1 V	1.43	1.57	1.7	
		$R_{(ILIM)}$ = SHORT, Shorted resistor current limit $R_{(ILIM)}$ = OPEN, Open resistor current limit (Single Point Failure Test: UL60950)	0.12	0.257	0.406	
I_{OS}	Short-circuit current limit(1)	$R_{(ILIM)}$ = 35.7 kΩ, ($V_{(IN)}$ - $V_{(OUT)}$) = 12 V	0.275	0.356	0.438	A
		$R_{(ILIM)}$ = 45.3 kΩ, ($V_{(IN)}$ - $V_{(OUT)}$) = 12 V	0.376	0.45	0.522	
		$R_{(ILIM)}$ = 95.3 kΩ, ($V_{(IN)}$ - $V_{(OUT)}$) = 12 V	0.837	0.9	0.964	
		$R_{(ILIM)}$ = 150 kΩ, ($V_{(IN)}$ - $V_{(OUT)}$) = 12 V	1.219	1.34	1.46	
$I_{(FASTRIP)}$	Fast-Trip comparator threshold	$R_{(ILIM)}$ in kΩ		0.0142 x $R_{(ILIM)}$ + 0.36		A
$V_{(ILIMopen)}$	ILIM Open resistor detect threshold	$V_{(ILIM)}$ Rising, $R_{(ILIM)}$ = OPEN	2.81	3.0	3.25	V
MOSFET – POWER SWITCH						
$R_{DS(on)}$	FET ON resistance(2)	–40°C ≤ T_J ≤ 85°C	55	87	120	mΩ
		–40°C ≤ T_J ≤ 125°C	55	87	135	
PASS FET OUTPUT (OUT)						
$I_{lkg(OUT)}$	OUT Bias current in off state	$V_{(ENUV)}$ = 0 V, $V_{(OUT)}$ = 0 V (Sourcing)	–2	0	1	µA
$I_{sink(OUT)}$		$V_{(ENUV)}$ = 0V, $V_{(OUT)}$ = 300 mV (Sinking)	5	7	10	

(1) Pulse-testing techniques maintain junction temperature close to ambient temperature. Thermal effects must be taken into account separately.
(2) The limits for these parameters are specified based on design and characterization data, and are not tested during production.

Electrical Characteristics (continued)

Conditions (unless otherwise noted) are –40°C ≤ T_J ≤ 125°C, 4.5 V ≤ $V_{(IN)}$ ≤ 18 V, $V_{(EN\ UV)}$ = 2 V, $V_{(OVP)}$ = 0 V, $R_{(ILIM)}$ = 95.3 kΩ, C_{SS} = OPEN, FLT = OPEN. Positive current into terminals. All voltages are referenced to GND (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FAULT FLAG ($\overline{FLT}$): ACTIVE LOW						
$R_{(\overline{FLT})}$	$\overline{FLT}$ Pull down Resistance	Device in fault condition, $V_{(ENUV)}$ = 0V, $I_{(\overline{FLT})}$ = 100mA	22	26	32	Ω
$I_{(\overline{FLT})}$	$\overline{FLT}$ Input Leakage Current	Device not in fault condition, $V_{(\overline{FLT})}$ = 0V, 18V	–0.5	0	0.5	µA
THERMAL SHUT DOWN (TSD)						
$T_{(TSD)}$	TSD Threshold, rising[2]			155		°C
$T_{(TSDhys)}$	TSD Hysteresis[2]			20		°C
	Thermal fault: Latched or Auto Retry	TPS25921L		LATCHED		
		TPS25921A		AUTO-RETRY		

7.6 Timing Requirements

Conditions (unless otherwise noted) are –40°C ≤ T_J ≤ 125°C, $V_{(IN)}$= 12 V, $V_{(EN\ UV)}$ = 2 V, $V_{(OVP)}$ = 0 V, $R_{(ILIM)}$ = 95.3 kΩ, C_{SS} = OPEN, FLT = OPEN. Positive current into terminals. All voltages are referenced to GND (unless otherwise noted). Refer to Figure 26 for the timing diagrams

			MIN	TYP	MAX	UNIT
ENABLE AND UNDERVOLTAGE LOCKOUT (ENUV) INPUT						
$t_{OFF(dly)}$	Turn Off delay	ENUV ↓ to $V_{(OUT)}$↓		8		µs
$t_{ON(dly)}$	Turn-On delay	ENUV ↑ to $V_{(OUT)}$ = 1V, $C_{(SS)}$ = OPEN		96		µs
		ENUV ↑ to $V_{(OUT)}$ = 1V, $C_{(SS)}$ > 0.39nF, [C(dVdT) in nF]		14.5 + 0.5 x (70p + $C_{(SS)}$)		
OVERVOLTAGE PROTECTION (OVP) INPUT						
$t_{OVP(dly)}$	OVP Disable delay	OVP↑ to $V_{(OUT)}$↓		8		µs
SOFT START: OUTPUT RAMP CONTROL (SS)						
t_{SS}	Output ramp time	ENUV ↑ to $V_{(OUT)}$ = 11 V, with $C_{(SS)}$ = open, $C_{(OUT)}$ = 2.2 µF	0.2	0.26	0.33	ms
		ENUV ↑ to $V_{(OUT)}$ = 11 V, with $C_{(SS)}$ = 1.2 nF, $C_{(OUT)}$ = 2.2 µF	2.1	3	3.6	
CURRENT LIMIT PROGRAMMING (ILIM)						
$t_{FASTRIP(dly)}$	Fast-Trip comparator delay	$I_{(OUT)}$ > $I_{(FASTRIP)}$		3		µs
THERMAL SHUT DOWN (TSD)						
$t_{TSD(dly)}$	Retry Delay after TSD recovery, T_J < [$T_{(TSD)}$ - 20°C]	TPS25921A Only, $V_{(IN)}$ = 12 V		150		ms
		TPS25921A Only, $V_{(IN)}$ = 4.5 V		100		ms

7.7 Typical Characteristics

Conditions (unless otherwise noted) are –40°C ≤ T_J ≤ 125°C, $V_{(IN)}$= 12 V, $V_{(EN\ UV)}$ = 2 V, $V_{(OVP)}$ = 0 V, $R_{(ILIM)}$ = 95.3 kΩ, $C_{(OUT)}$ = 2.2 µF, C_{SS} = OPEN, FLT = OPEN. Positive current into terminals. All voltages referenced to GND (unless otherwise noted). For all oscilloscope waveforms T_A = 25°C.

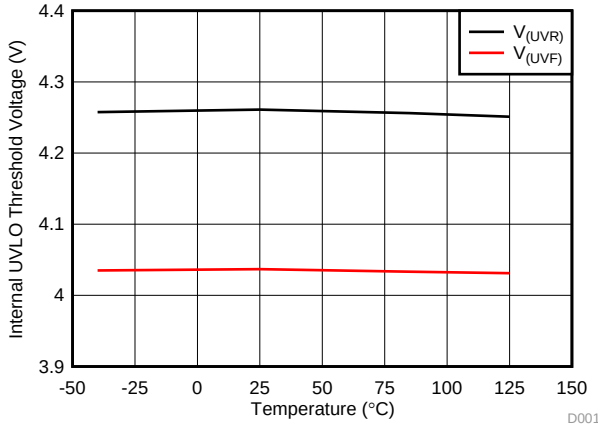


Figure 1. UVLO Threshold Voltage vs Temperature

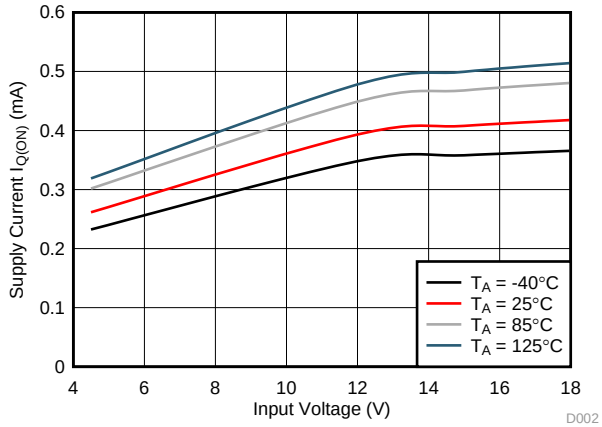


Figure 2. Input Supply Current vs Supply Voltage During Normal Operation

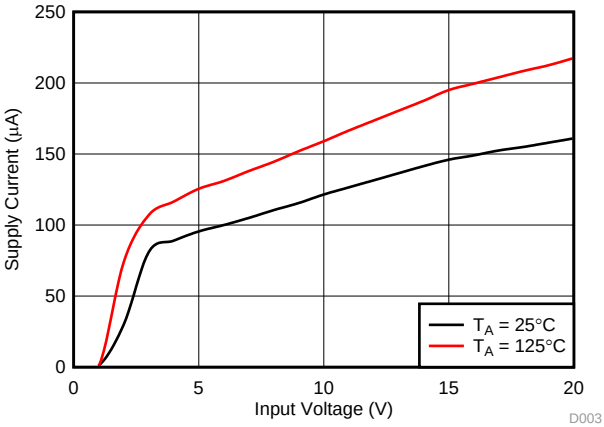


Figure 3. Input Supply Current vs Supply Voltage at Shutdown

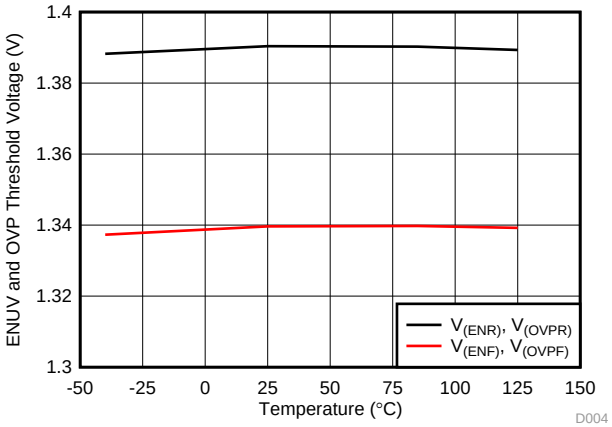


Figure 4. ENUV and OVP Threshold Voltage vs Temperature

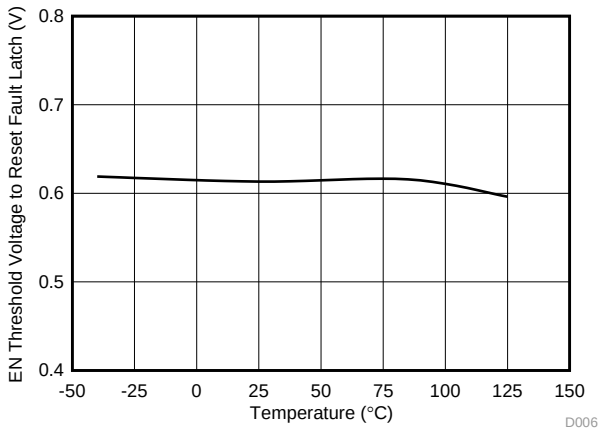


Figure 5. EN Threshold Voltage to Reset Fault Latch vs Temperature

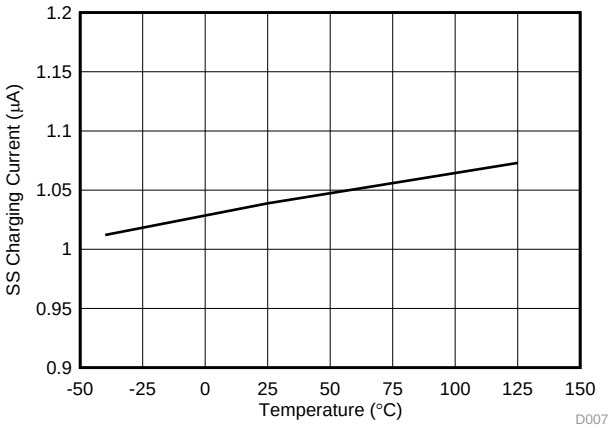


Figure 6. SS Pin Charging Current vs Temperature

Typical Characteristics (continued)

Conditions (unless otherwise noted) are –40°C ≤ T_J ≤ 125°C, $V_{(IN)}$= 12 V, $V_{(EN\ UV)}$ = 2 V, $V_{(OVP)}$ = 0 V, $R_{(ILIM)}$ = 95.3 kΩ, $C_{(OUT)}$ = 2.2 µF, C_{SS} = OPEN, FLT = OPEN. Positive current into terminals. All voltages referenced to GND (unless otherwise noted). For all oscilloscope waveforms T_A = 25°C.

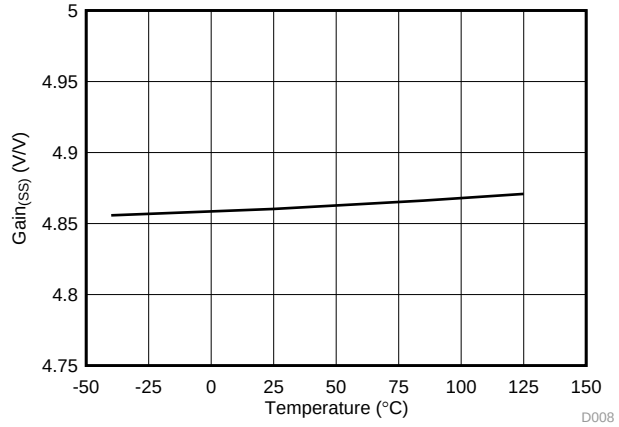


Figure 7. $GAIN_{(SS)}$ vs Temperature

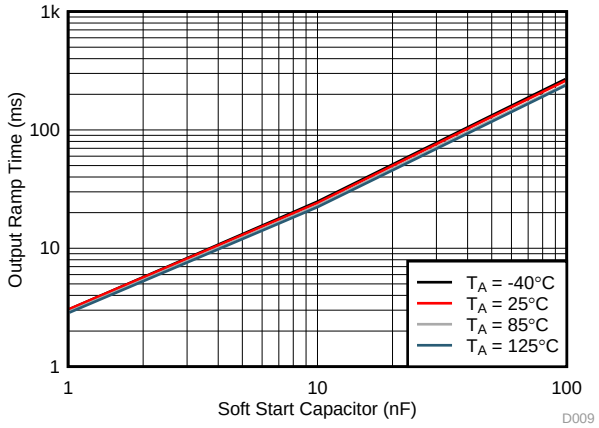
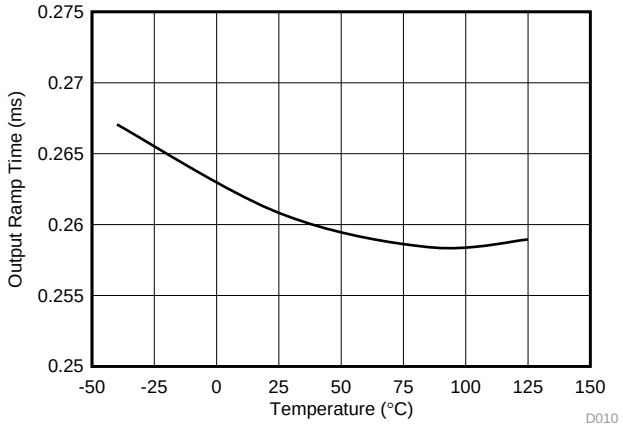


Figure 8. Output Ramp Time vs $C_{(SS)}$



$C_{(SS)}$ = Open

Figure 9. Output Ramp Time vs Temperature

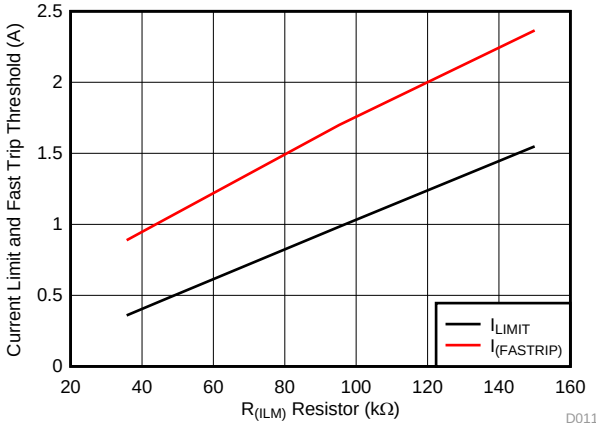


Figure 10. Current Limit vs Current Limit Resistor

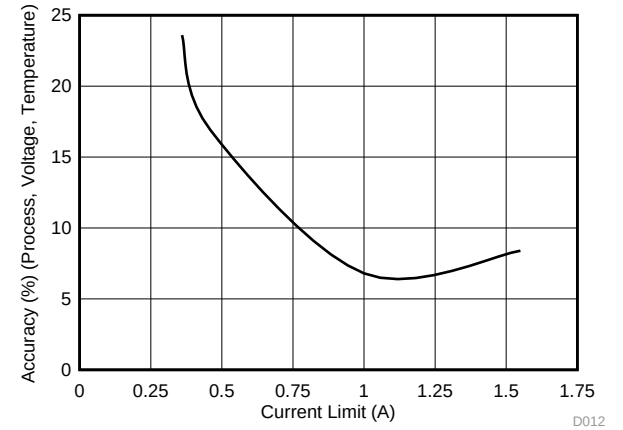


Figure 11. Current Limit Accuracy vs Current Limit

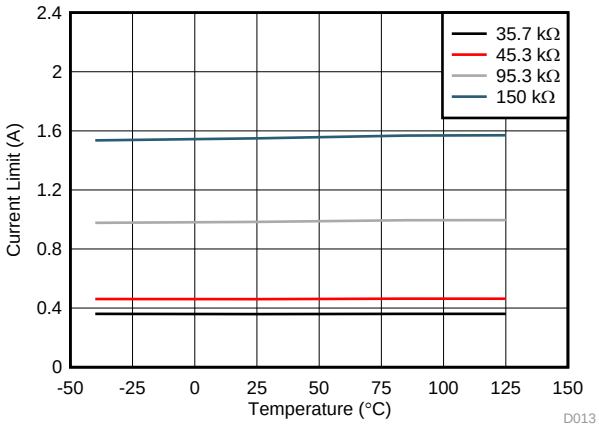
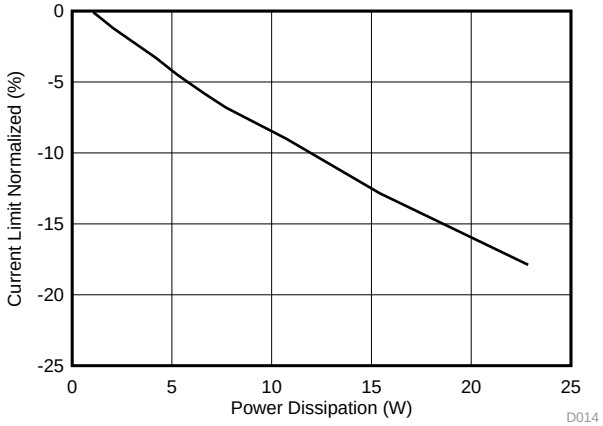


Figure 12. Current Limit vs Temperature Across $R_{(ILIM)}$

Typical Characteristics (continued)

Conditions (unless otherwise noted) are –40°C ≤ T_J ≤ 125°C, $V_{(IN)}$= 12 V, $V_{(EN\ UV)}$ = 2 V, $V_{(OVP)}$ = 0 V, $R_{(ILIM)}$ = 95.3 kΩ, $C_{(OUT)}$ = 2.2 µF, C_{SS} = OPEN, FLT = OPEN. Positive current into terminals. All voltages referenced to GND (unless otherwise noted). For all oscilloscope waveforms T_A = 25°C.



$P_D = [V_{(IN)} - V_{(OUT)}]*I_{LIMIT}$

Figure 13. Current Limit Normalized (%) vs Power Dissipation in the Device P_D

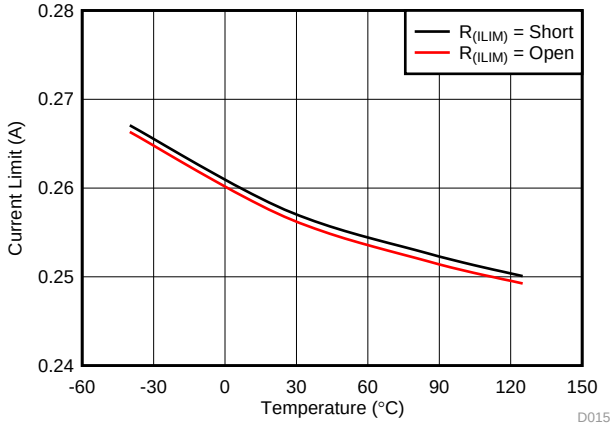


Figure 14. Current Limit for $R_{(ILIM)}$ = Open and Short vs Temperature

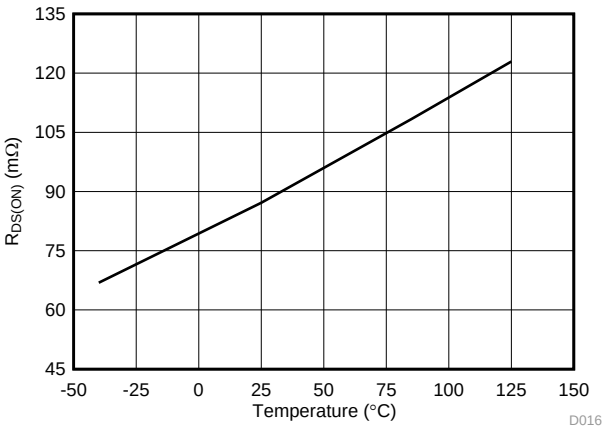
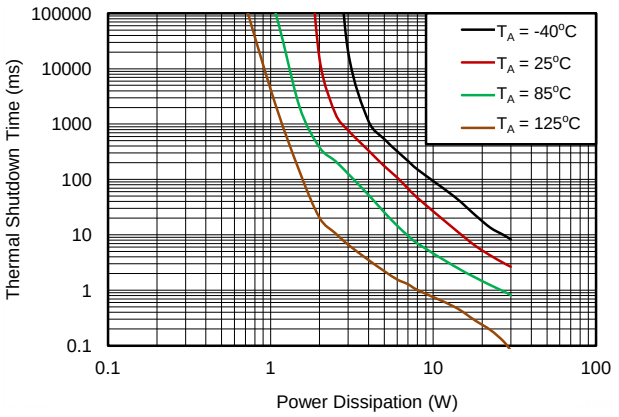
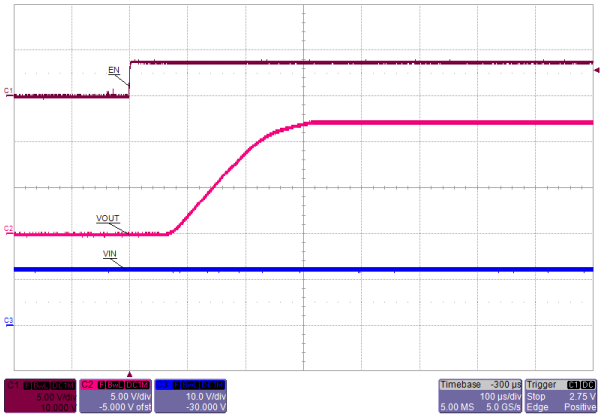


Figure 15. $R_{DS(ON)}$ vs Temperature



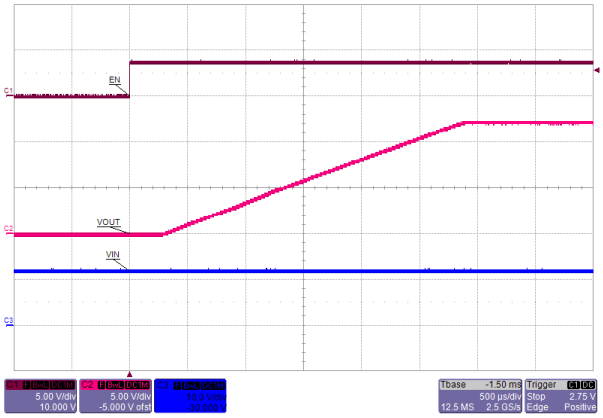
Taken on 1-Layer board, 2oz.(0.08-mm thick) with GND plane area: 14 cm2 (bottom)

Figure 16. Thermal Shutdown Time vs Power Dissipation



$C_{(SS)}$ = Open $C_{(OUT)}$ = 4.7 nF

Figure 17. Turn ON with Enable



$C_{(SS)}$ = 1nF $C_{(OUT)}$ = 4.7 nF

Figure 18. Turn ON with Enable

Typical Characteristics (continued)

Conditions (unless otherwise noted) are –40°C ≤ T_J ≤ 125°C, $V_{(IN)}$= 12 V, $V_{(EN\ UV)}$ = 2 V, $V_{(OVP)}$ = 0 V, $R_{(ILIM)}$ = 95.3 kΩ, $C_{(OUT)}$ = 2.2 µF, C_{SS} = OPEN, FLT = OPEN. Positive current into terminals. All voltages referenced to GND (unless otherwise noted). For all oscilloscope waveforms T_A = 25°C.

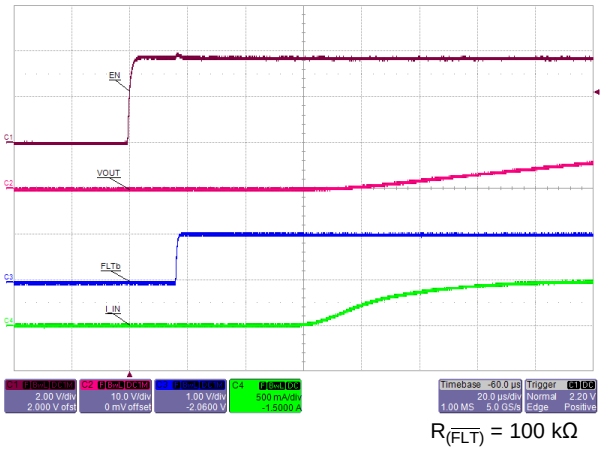


Figure 19. EN Turn ON Delay : EN ↑ to Output Ramp ↑

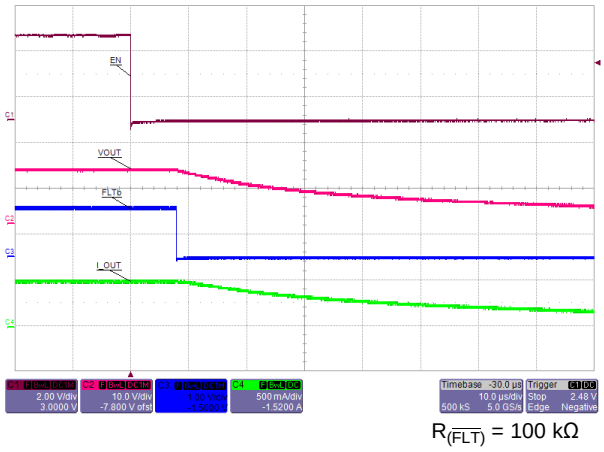


Figure 20. EN Turn OFF Delay : EN ↓ to Fault ↓

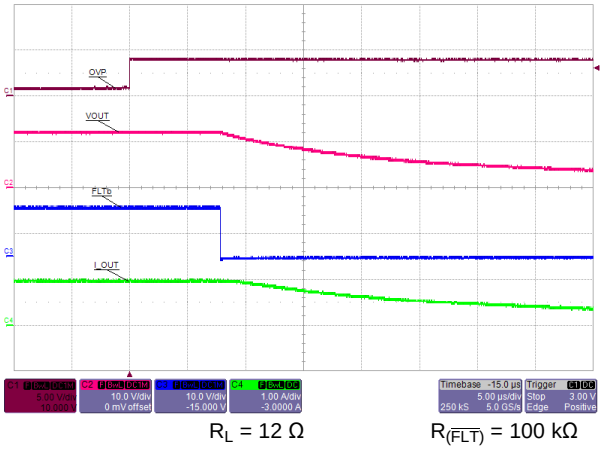


Figure 21. OVP Turn OFF delay: OVP ↑ to Fault ↓

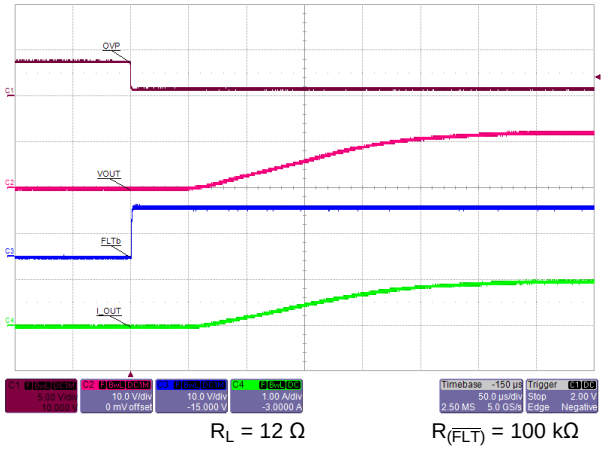


Figure 22. OVP Turn ON delay: OVP ↓ to Output Ramp ↑

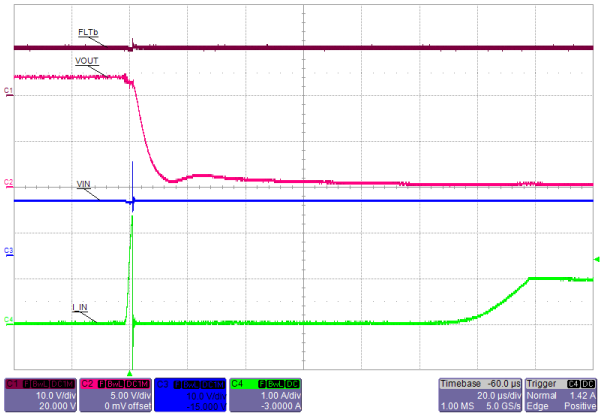


Figure 23. Hot-Short: Fast Trip Response and Current Regulation

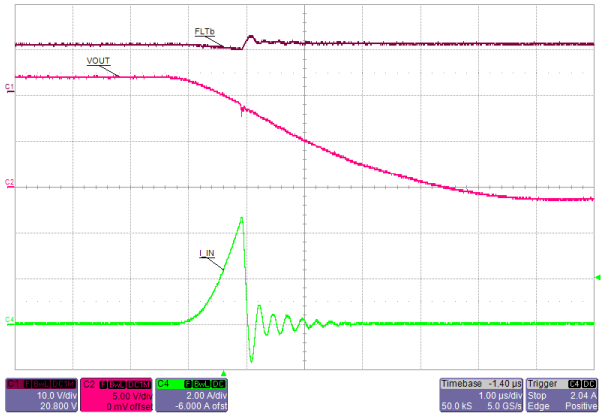


Figure 24. Hot-Short: Fast Trip Response (Zoomed)

8 Parametric Measurement Information

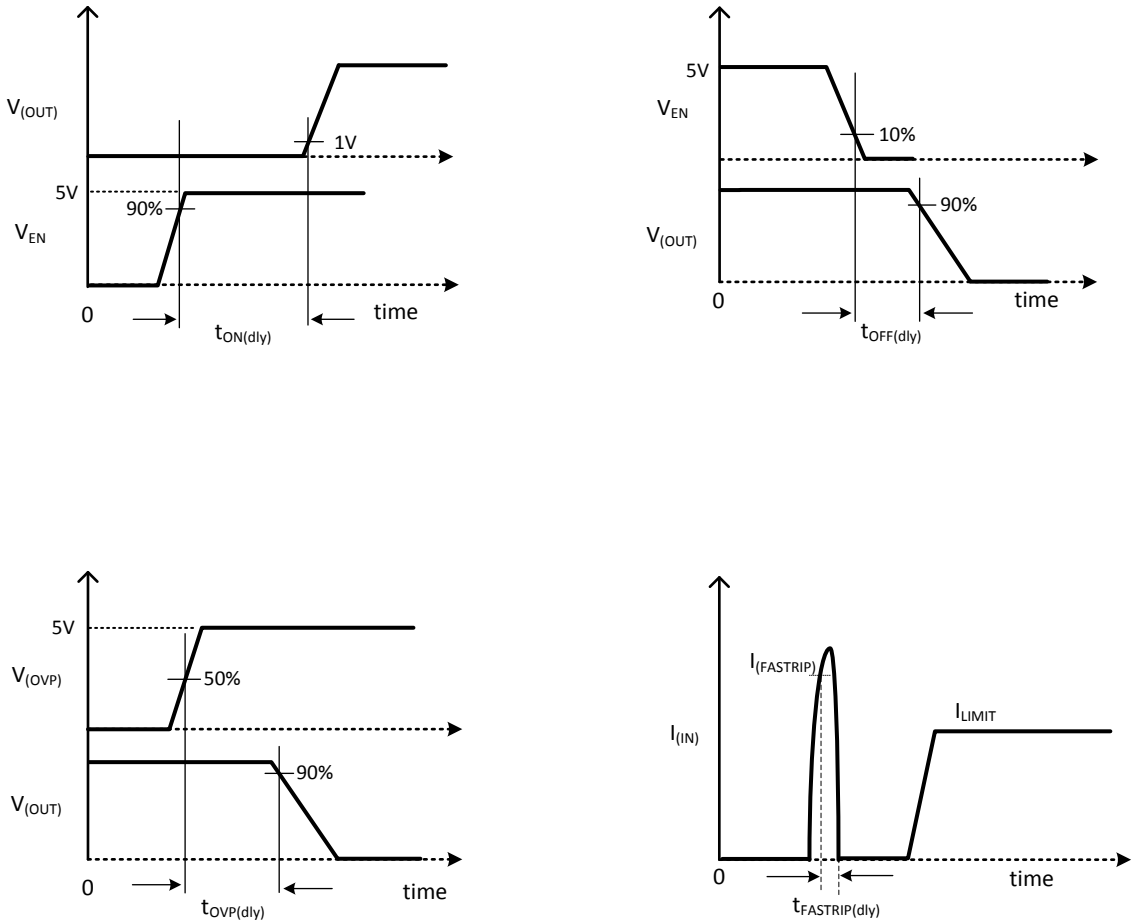


Figure 25. Timing Diagrams

9 Detailed Description

9.1 Overview

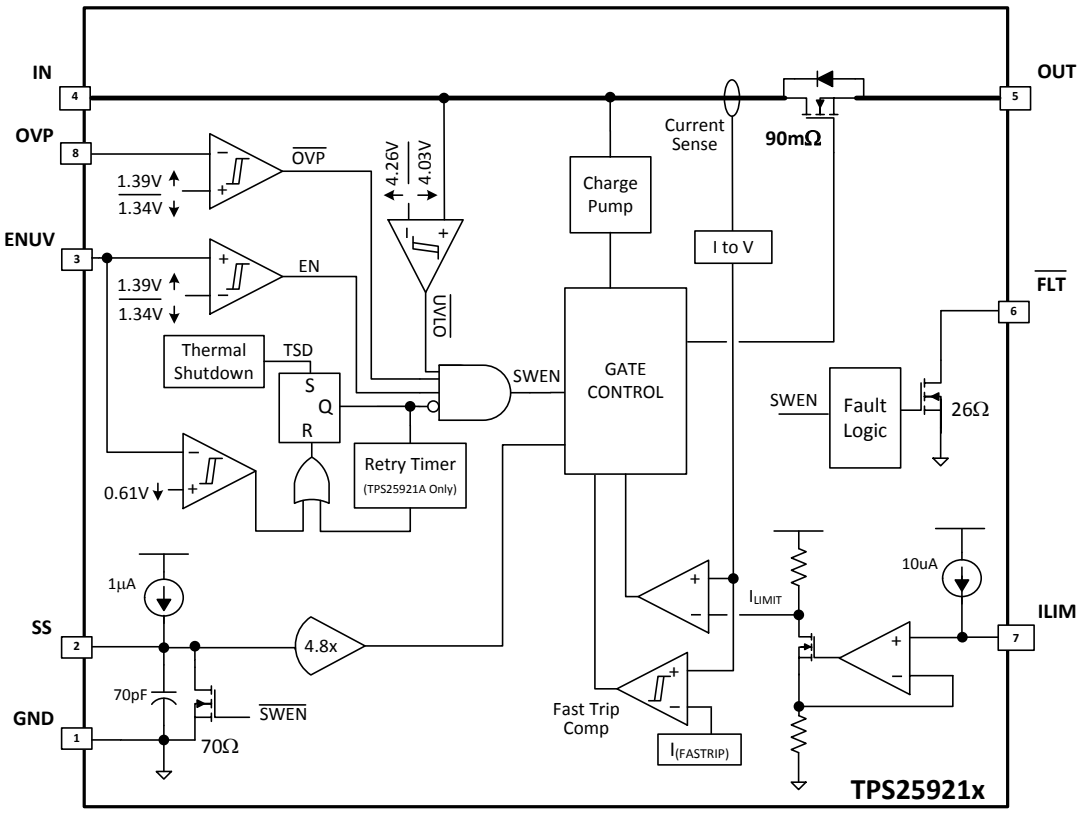
TPS25921 is a smart eFuse with enhanced built-in protection circuitry. It provides robust protection for all systems and applications powered from 4.5 V to 18 V.

For hot-plug-in boards, the device provides in-rush current control and programmable output ramp-rate. TPS25921 integrates overcurrent and short circuit protection. The precision overcurrent limit helps to minimize over design of the input power supply, while the fast response short circuit protection immediately isolates the load from input when a short circuit is detected. The device allows the user to program the overcurrent limit threshold between 0.4 A and 1.6 A via an external resistor. The device provides precise monitoring of voltage bus for brown-out and overvoltage conditions and asserts fault for downstream system. Its threshold accuracy of 3% ensures tight supervision of bus, eliminating the need for a separate supply voltage supervisor chip. TPS25921 is designed to protect systems such as White Goods, STBs, DTVs, Smart Meters and Gas Analyzers.

The additional features include:

- Over temperature protection to safely shutdown in the event of an overcurrent event
- Fault reporting for brown-out and overvoltage faults
- A choice of latched or automatic restart mode

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Enable and Adjusting Undervoltage Lockout (UVLO)

The ENUV pin controls the ON/OFF state of the internal FET. A voltage $V_{(ENUV)} < V_{(ENF)}$ on this pin turns off the internal FET, thus disconnecting IN from OUT.

Toggling the ENUV pin below $V_{(ENF\_RST)}$ resets the TPS25921L that has latched off due to a fault condition. The internal de-glitch delay on ENUV falling edge is kept low for quick detection of power failure. For applications where a higher de-glitch delay on ENUV is desired, or when the supply is particularly noisy, it is recommended to use an external filter capacitor from the ENUV terminal to GND.

The undervoltage lockout threshold can be programmed by using an external resistor divider from the supply IN terminal to the ENUV terminal to GND as shown in Figure 26. When an undervoltage or input power fail event is detected, the internal FET is quickly turned off, and $\overline{FLT}$ is asserted. If the undervoltage lockout function is not needed, the ENUV pin should be connected to the IN terminal. The ENUV terminal should not be left floating.

TPS25921 also implements internal undervoltage lockout (UVLO) circuitry on the IN pin. The device gets disabled when the IN terminal voltage falls below internal UVLO Threshold $V_{(UVF)}$.

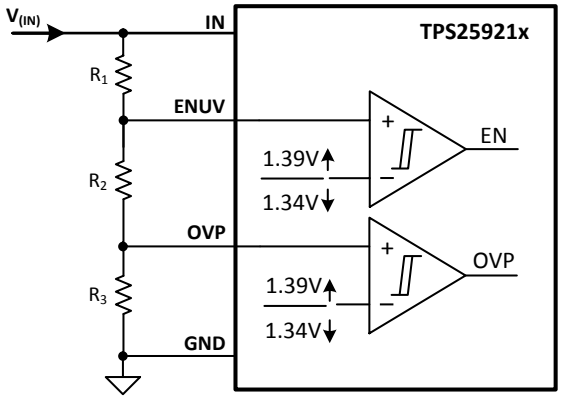


Figure 26. UVLO and OVP Thresholds Set By R_1, R_2 and R_3

9.3.2 Overvoltage Protection (OVP)

TPS25921 incorporates circuits to protect the system during overvoltage conditions. A resistor divider, connected from the supply to OVP terminal to GND (as shown in Figure 26), programs the overvoltage threshold. A voltage more than $V_{(OVPR)}$ on the OVP pin turns off the internal FET and protects the downstream load. This pin should be tied to GND when not used.

9.3.3 Hot Plug-in and In-Rush Current Control

TPS25921 is designed to control the in-rush current upon insertion of a card into a live backplane or other "hot" power source. This limits the voltage sag on the backplane's supply voltage and prevents unintended resets of the system power. A slew rate controlled startup (SS) also helps to eliminate conductive and radiated interference. An external capacitor from the SS pin to GND defines the slew rate of the output voltage at power-on (as shown in Figure 27). The equation governing slew rate at start-up is shown in Equation 1 :

Feature Description (continued)

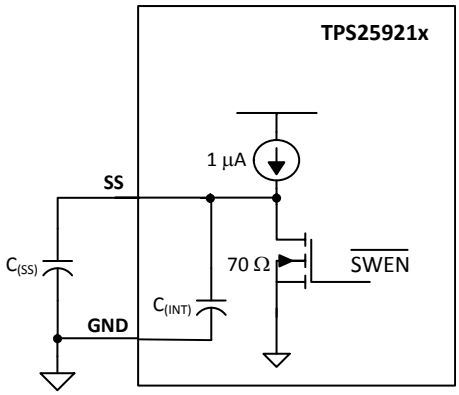


Figure 27. Output Ramp Up Time t_{dVdT} is Set by $C_{(dVdT)}$

$$I_{(SS)} = \frac{(C_{(SS)} + C_{(INT)})}{Gain_{(SS)}} \times \frac{dV_{(OUT)}}{dt} \quad (1)$$

Where:

- $I_{(SS)}$ = 1 µA (typical)
- $\frac{dV_{(OUT)}}{dt}$ = Desired output slew rate
- $GAIN_{(SS)} = \Delta V_{(OUT)}/\Delta V_{(SS)}$ gain = 4.85

The total ramp time (t_{SS}) of $V_{(OUT)}$ for 0 to $V_{(IN)}$ can be calculated using Equation 2:

$$t_{SS} = 20.6 \times 10^{4} \times V_{(IN)} \times \left(C_{(SS)} + 70\ pF\right) \quad (2)$$

Where $C_{(ss)}$ is in Farad.

The inrush current, $I_{(INRUSH)}$ can be calculated as

$$I_{(INRUSH)} = C_{(OUT)} \times \frac{V_{(IN)}}{t_{SS}} \quad (3)$$

The SS pin can be left floating to obtain a predetermined slew rate (t_{SS}) on the output. When terminal is left floating, the device sets an internal ramp rate of ~50V/ms for output ($V_{(OUT)}$) ramp.

Figure 36 and Figure 37 illustrate the inrush current control behavior of the device. For systems where load is present during start-up, the current never exceeds the overcurrent limit set by $R_{(ILIM)}$ resistor for the application. For defining appropriate charging time/rate under different load conditions, refer to the *Setting Output Voltage Ramp time (t_{SS})* section.

9.3.4 Overload and Short Circuit Protection :

At all times load current is monitored by sensing voltage across an internal sense resistor. During overload events, current is limited to the current limit (I_{LIMIT}) programmed by $R_{(ILIM)}$ resistor

$$I_{LIMIT} = 10.73 \times 10^{-3} \times R_{(ILIM)} - 0.018 \quad (4)$$

$$R_{(ILIM)} = \frac{I_{LIMIT} + 0.018}{10.73 \times 10^{-3}} \quad (5)$$

- I_{LIMIT} is overload current limit in Ampere
- $R_{(ILIM)}$ is the current limit programming resistor in kΩ

TPS25921 incorporates two distinct overcurrent protection levels: the current limit (I_{LIMIT}) and the fast-trip threshold ($I_{(FASTRIP)}$). The fast trip and current limit operations are shown in Figure 28.

Feature Description (continued)

Bias current on ILIM pin directly controls current-limiting behavior of the device, and PCB routing of this node must be kept away from any noisy (switching) signals.

9.3.4.1 Overload Protection

For overload conditions, the internal current-limit amplifier regulates the output current to I_{LIMIT}. The output voltage droops during current limit regulation, resulting in increased power dissipation in the device. If the device junction temperature reaches the thermal shutdown threshold ($T_{(TSD)}$), the internal FET is turned off. Once in thermal shutdown, The TPS25921L version stays latched off, whereas TPS25921A commences an auto-retry cycle $t_{TSD(dly)}$ ms after $T_J < [T_{(TSD)} - 20°C]$. During thermal shutdown, the fault pin $\overline{FLT}$ pulls low to signal a fault condition. Figure 40 and Figure 41 illustrate overload behavior.

9.3.4.2 Short Circuit Protection

During a transient short circuit event, the current through the device increases very rapidly. As current-limit amplifier cannot respond quickly to this event due to its limited bandwidth, the device incorporates a fast-trip comparator, with a threshold $I_{(FASTRIP)}$. When the current through the internal FET exceeds $I_{(FASTRIP)}$ ($I_{(OUT)} > I_{(FASTRIP)}$), this comparator shuts down the pass device within 3 µs and terminates the rapid short-circuit peak current. The $I_{(FASTRIP)}$ threshold is dependent on programmed overload current limit and function of $R_{(ILIM)}$. See Equation 6 for the calculation.

$$I_{(FASTRIP)} = 1.42 \times 10^{-2} \times R_{(ILIM)} + 0.36 \quad (6)$$

where

- $I_{(FASTRIP)}$ is fast trip current limit in Ampere
- $R_{(ILIM)}$ is the current limit resistor in kΩ

The fast-trip circuit holds the internal FET off for only a few microseconds, after which the device attempts to turn back on normally, allowing the current-limit loop to regulate the output current to I_{LIMIT}. Then, device behaves similar to overload condition. Figure 42 through Figure 44 illustrate the behavior of the system when the current exceeds the fast-trip threshold.

9.3.4.3 Start-Up with Short on Output

During start-up into a short circuit current is limited to I_{LIMIT}. Figure 45 and Figure 46 illustrate start-up with a short on the output. This feature helps in quick fault isolation and hence ensures stability of the DC bus.

9.3.4.4 Constant Current Limit Behavior during Overcurrent Faults

When power dissipation in the internal FET [$P_D = (V_{(IN)} - V_{(OUT)}) \times I_{(OUT)}$] > 2 W, there is a ~1 to 20 % thermal fold back in the current limit value so that the regulated current drops from I_{LIMIT} to I_{OS}. Eventually, the device shuts down due to over temperature.

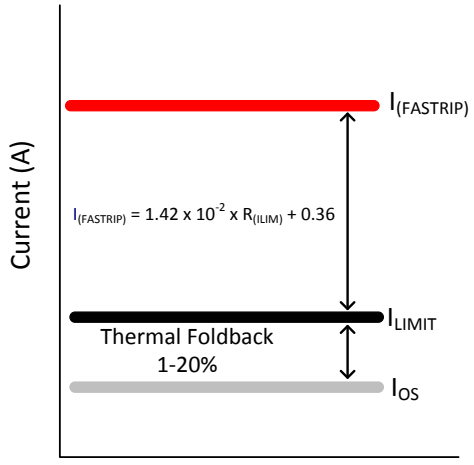


Figure 28. Overcurrent Protection Levels

Feature Description (continued)

9.3.5 FAULT Response

The $\overline{FLT}$ open-drain output is asserted (active low) during undervoltage, overvoltage and thermal shutdown conditions. The $\overline{FLT}$ signal remains asserted until the fault condition is removed and the device resumes normal operation. During thermal shutdown, TPS25921L version stays latched off, whereas TPS25921A commences an auto-retry cycle $t_{TSD(dly)}$ millisecond after $T_J < [T_{(TSD)} - 20°C]$. For TPS25921L, thermal fault latch can be reset by cycling the ENUV pin below $V_{(ENF\_RST)}$ threshold. A nuisance fast trip does not trigger fault.

Connect $\overline{FLT}$ with a pull up resistor to Input or Output voltage rail. $\overline{FLT}$ may be left open or tied to ground when not used.

9.3.6 IN, OUT and GND Pins

The IN pin should be connected to the power source. A ceramic bypass capacitor close to the device from IN to GND is recommended to alleviate bus transients. The recommended operating voltage range is 4.5 V – 18 V.

The OUT pin should be connected to the load. $V_{(OUT)}$ in the ON condition, is calculated using the Equation 7

$$V_{(OUT)} = V_{(IN)} - \left(R_{DS(ON)} \times I_{(OUT)}\right) \quad (7)$$

where, $R_{DS(ON)}$ is the ON resistance of the internal FET.

GND terminal is the most negative voltage in the circuit and is used as a reference for all voltage reference unless otherwise specified.

9.3.7 Thermal Shutdown:

Internal over temperature shutdown disables/turns off the FET when $T_J > 155°C$ (typical). The TPS25921L version latches off the internal FET, whereas TPS25921A commences an auto-retry cycle $t_{TSD(dly)}$ milliseconds after T_J drops below $[T_{(TSD)} - 20°C]$. During the thermal shutdown, the fault pin $\overline{FLT}$ is pulled low to signal a fault condition.

9.4 Device Functional Modes

9.4.1 Shutdown Control

The internal FET and hence the load current can be remotely switched off by taking the ENUV pin below its 1.34 V threshold with an open collector or open drain device as shown in Figure 29. Upon releasing the ENUV pin the device turns on with soft-start cycle.

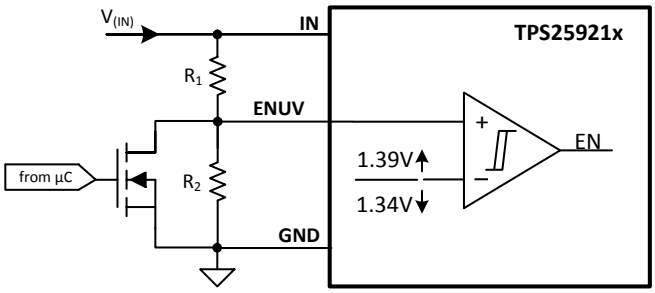


Figure 29. Shutdown Control

9.4.2 Operational Overview of Device Functions

The device functionality for various conditions are shown in Table 1.

Table 1. Operational Overview of Device Functions

Device	TPS25921
Start Up	Inrush ramp controlled by capacitor at SS pin
	Inrush limited to I_{LIMIT} level as set by $R_{(ILIM)}$
	If $T_J > T_{(TSD)}$ device shuts off
Overcurrent Response	Current is limited to $I_{(LIM)}$ level as set by $R_{(ILIM)}$
	Power dissipation increases as $V_{(IN)} - V_{(OUT)}$ grows
	Device turns off when $T_J > T_{(TSD)}$
	'L' Version remains off
	'A' Version will attempt restart $t_{TSD(dly)}$ ms after $T_J < [T_{(TSD)} -20°C]$
Short-Circuit Response	Fast shut off when $I_{(LOAD)} > I_{(FASTRIP)}$
	Quick restart and current limited to I_{LIMIT}, follows standard startup cycle

10 Applications and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

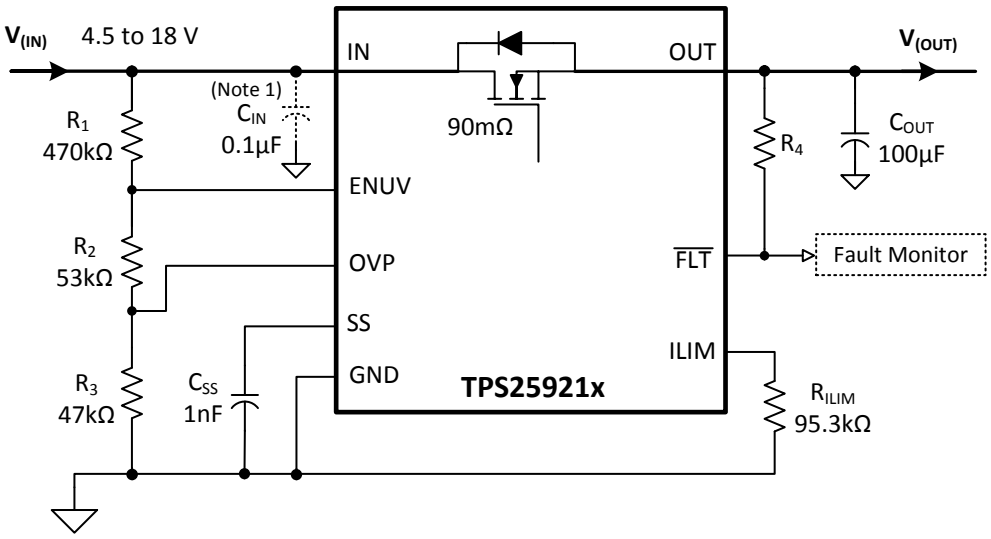
10.1 Application Information

The TPS25921x is a smart eFuse. It is typically used for Hot-Swap and Power rail protection applications. It operates from 4.5 V to 18 V with programmable current limit, overvoltage and undervoltage protection. The device aids in controlling the in-rush current and provides precise current limiting during overload conditions for systems such as White Goods, Set-Top-Box, DTVs, Gaming Consoles, SSDs/HDDs and Smart Meters. The device also provides robust protection for multiple faults on the sub-system rail.

Alternatively, the WEBENCH® software may be used to generate a complete design. The WEBENCH® software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. Additionally, a spreadsheet design tool *TPS25921 Design Calculator* is available on web folder.

10.2 Typical Application

10.2.1 Precision Current Limiting and Protection for White Goods



(1) C_{IN}: Optional and only for noise suppression.

Figure 30. Typical Application Schematics: eFuse for White Goods

Typical Application (continued)

10.2.1.1 Design Requirements

For this design example, use the parameters shown in Table 2.

Table 2. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage range, $V_{(IN)}$	12 V
Undervoltage lockout set point, $V_{(UV)}$	8 V
Overvoltage protection set point , $V_{(OV)}$	17 V
Load at Start-Up , $R_{L(SU)}$	24 Ω
Current limit, I_{LIMIT}	1 A
Load capacitance , $C_{(OUT)}$	100 µF
Maximum ambient temperatures , T_A	85°C

10.2.1.2 Detailed Design Procedure

The following design procedure can be used to select component values for the TPS25921A and TPS25921L.

10.2.1.2.1 Step by Step Design Procedure

To begin the design process a few parameters must be decided upon. The designer needs to know the following:

- Normal input operation voltage
- Maximum output capacitance
- Maximum current Limit
- Load during start-up
- Maximum ambient temperature of operation

This design procedure below seeks to control the junction temperature of device under both static and transient conditions by proper selection of output ramp-up time and associated support components. The designer can adjust this procedure to fit the application and design criteria.

10.2.1.2.2 Programming the Current-Limit Threshold: $R_{(ILIM)}$ Selection

The $R_{(ILIM)}$ resistor at the ILIM pin sets the over load current limit, this can be set using Equation 5.

$$R_{(ILIM)} = \frac{1 + 0.018}{10.73 \times 10^{-3}} = 94.8\ k\Omega \quad (8)$$

Choose closest standard value: 95.3 kΩ, 1% standard value resistor.

10.2.1.2.3 Undervoltage Lockout and Overvoltage Set Point

The undervoltage lockout (UVLO) and overvoltage trip point are adjusted using the external voltage divider network of R_1, R_2 and R_3 as connected between IN, ENUV, OVP and GND pins of the device. The values required for setting the undervoltage and overvoltage are calculated solving Equation 9 and Equation 10.

$$V_{(OVPR)} = \frac{R_3}{R_1 + R_2 + R_3} \times V_{(OV)} \quad (9)$$

$$V_{(ENR)} = \frac{R_2 + R_3}{R_1 + R_2 + R_3} \times V_{(UV)} \quad (10)$$

For minimizing the input current drawn from the power supply {$I_{(R123)} = V_{(IN)}/(R_1 + R_2 + R_3)$}, it is recommended to use higher values of resistance for R_1, R_2 and R_3.

However, leakage currents due to external active components connected to the resistor string can add error to these calculations. So, the resistor string current, $I_{(R123)}$ must be chosen to be 20x greater than the leakage current expected.

From the device electrical specifications, $V_{(OVPR)}$ = 1.40 V and $V_{(ENR)}$ = 1.40 V. For design requirements, $V_{(OV)}$ is 17 V and $V_{(UV)}$ is 8 V. To solve the equation, first choose the value of R_3 = 47 kΩ and use Equation 9 to solve for (R_1 + R_2) = 523.71 kΩ. Use Equation 10 and value of (R_1 + R_2) to solve for R_2 = 52.88 kΩ and finally R_1= 470.83 kΩ.

Using the closest standard 1% resistor values gives R_1 = 470 kΩ, R_2 = 53 kΩ, and R_3 = 47 kΩ.

The power failure threshold is detected on the falling edge of supply. This threshold voltage is 4% lower than the rising threshold, $V_{(UV)}$. This is calculated using Equation 11.

$$V_{(PFAIL)} = 0.96 \times V_{(UV)} \quad (11)$$

Power fail threshold set is : 7.68 V

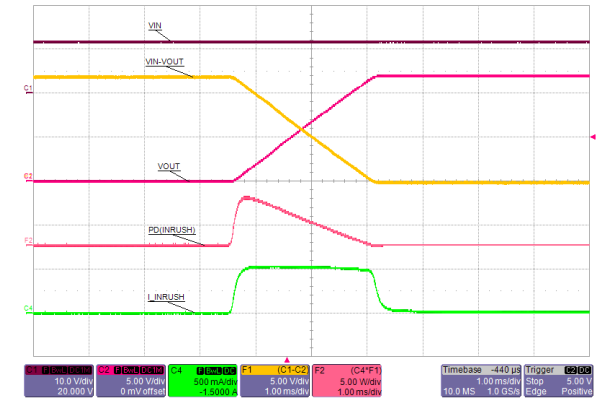
10.2.1.2.4 Setting Output Voltage Ramp time (t_{SS})

For a successful design, the junction temperature of device should be kept below the absolute-maximum rating during both dynamic (start-up) and steady state conditions. Dynamic power stresses often are an order of magnitude greater than the static stresses, so it is important to determine the right start-up time and in-rush current limit required with system capacitance to avoid thermal shutdown during start-up with and without load.

The ramp-up capacitor $C_{(SS)}$ needed is calculated considering the two possible cases:

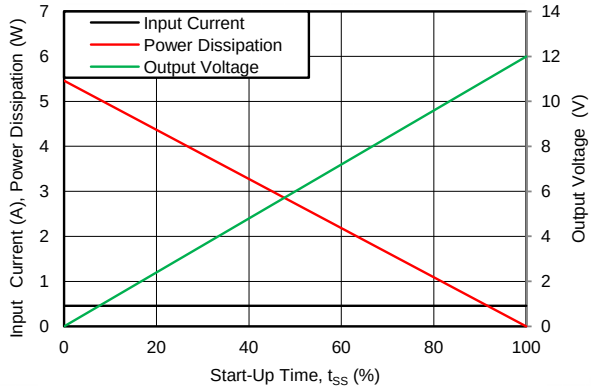
10.2.1.2.4.1 Case1: Start-up Without Load: Only Output Capacitance $C_{(OUT)}$ Draws Current During Start-up

During start-up, as the output capacitor charges, the voltage difference across the internal FET decreases, and the power dissipated decreases as well. Typical ramp-up of output voltage $V_{(OUT)}$ with inrush current limit of 0.5A and power dissipated in the device during start-up is shown in Figure 31. The average power dissipated in the device during start-up is equal to area of triangular plot (red curve in Figure 32) averaged over t_{SS}.



$V_{(IN)}$ = 12 V $C_{(SS)}$ = 1 nF $C_{(OUT)}$=100 µF

Figure 31. Start-up Without Load



$V_{(IN)}$ = 12 V $C_{(SS)}$ = 1 nF $C_{(OUT)}$=100 µF

Figure 32. $P_{D(INRUSH)}$ Due to Inrush Current

For TPS25921 device, the inrush current is determined as,

$$I = C \times \frac{dV}{dT} \Rightarrow I_{(INRUSH)} = C_{(OUT)} \times \frac{V_{(IN)}}{t_{SS}} \quad (12)$$

Power dissipation during start-up is:

$$P_{D(INRUSH)} = 0.5 \times V_{(IN)} \times I_{(INRUSH)} \quad (13)$$

Equation 13 assumes that load does not draw any current until the output voltage has reached its final value.

10.2.1.2.4.2 Case 2: Start-up With Load: Output Capacitance $C_{(OUT)}$ and Load Draws Current During Start-up

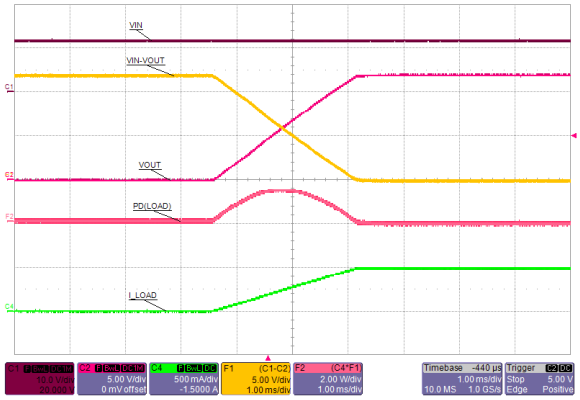
When load draws current during the turn-on sequence, there will be additional power dissipated. Considering a resistive load $R_{L(SU)}$ during start-up, load current ramps up proportionally with increase in output voltage during t_{SS} time. Typical ramp-up of output voltage, load current and power dissipation in the device is shown in Figure 33 and power dissipation with respect to time is plotted in Figure 34. The additional power dissipation during start-up phase is calculated as follows.

$$(V_I - V_O)(t) = V_{(IN)} \times \left(1 - \frac{t}{t_{SS}}\right) \quad (14)$$

$$I_L(t) = \left(\frac{V_{(IN)}}{R_{L(SU)}}\right) \times \frac{t}{t_{SS}} \quad (15)$$

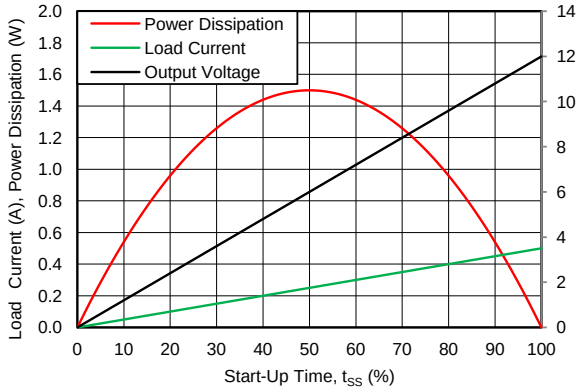
Where $R_{L(SU)}$ is the load resistance present during start-up. Average energy loss in the internal FET during charging time due to resistive load is given by:

$$W_t = \int_0^{tss} V_{(IN)} \times \left(1 - \frac{t}{t_{SS}}\right) \times \left(\frac{V_{(IN)}}{R_{L(SU)}} \times \frac{t}{t_{SS}}\right) dt \quad (16)$$



$V_{(IN)}$ = 12 V $C_{(SS)}$ = 1 nF , $C_{(OUT)}$=100 µF $R_{L(SU)}$ = 24 Ω

Figure 33. Start-up With Load



$V_{(IN)}$ = 12 V $C_{(SS)}$ = 1 nF $R_{L(SU)}$ = 24 Ω

Figure 34. $P_{D(LOAD)}$ in Device during Start-up with Load

On solving Equation 16 the average power loss in the internal FET due to load is:

$$P_{D(LOAD)} = \left(\frac{1}{6}\right) \times \frac{V^2_{(IN)}}{R_{L(SU)}} \quad (17)$$

Total power dissipated in the device during startup is:

$$P_{D(STARTUP)} = P_{D(INRUSH)} + P_{D(LOAD)} \quad (18)$$

Total current during startup is given by:

$$I_{(STARTUP)} = I_{(INRUSH)} + I_L(t) \quad (19)$$

If $I_{(STARTUP)} > I_{LIMIT}$, the device limits the current to I_{LIMIT} and the current limited charging time is determined by:

$$t_{SS(current\text{-}limited)} = C_{(OUT)} \times R_{L(SU)} \times \left[\frac{I_{(LIMIT)}}{I_{(INRUSH)}} - 1 + LN\left(\frac{I_{(INRUSH)}}{I_{(LIMIT)} - \frac{V_{(IN)}}{R_{L(SU)}}}\right)\right] \quad (20)$$

The power dissipation, with and without load, for selected start-up time should not exceed the shutdown limits as shown in Figure 35.

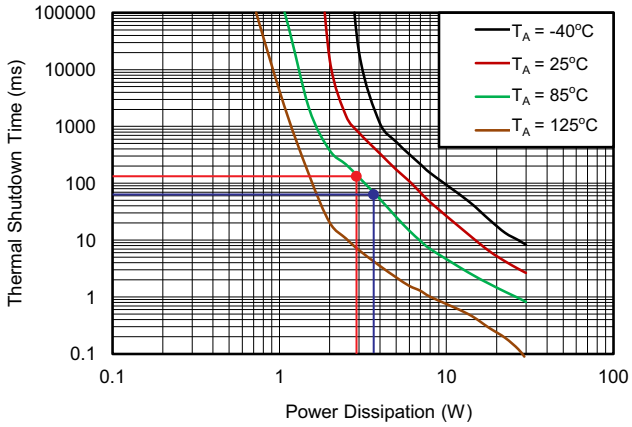


Figure 35. Thermal Shutdown Limit Plot

For the design example under discussion,

Select ramp-up capacitor $C_{(SS)}$ = 1nF, using Equation 2.

$$t_{SS} = 20.6 \times 10^{4} \times 12 \times \left(1 \times 10^{-9} + 70 \times 10^{-12}\right) = 2.64 \text{ ms} \quad (21)$$

The inrush current drawn by the load capacitance ($C_{(OUT)}$) during ramp-up using Equation 3.

$$I_{(INRUSH)} = \left(100 \times 10^{-6}\right) \times \left(\frac{12}{2.64 \times 10^{-3}}\right) = 0.454 \text{ A} \quad (22)$$

The inrush Power dissipation is calculated, using Equation 13.

$$P_{D(INRUSH)} = 0.5 \times 12 \times 0.454 = 2.72 \text{ W} \quad (23)$$

For 2.72 W of power loss, the thermal shut down time of the device should not be less than the ramp-up time t_{SS} to avoid the false trip at maximum operating temperature. From thermal shutdown limit graph Figure 35 at T_A = 85°C, for 2.72 W of power the shutdown time is ~170 ms. So it is safe to use 2.64 ms as start-up time without any load on output.

Considering the start-up with load 24 Ω, the additional power dissipation, when load is present during start up is calculated, using Equation 17.

$$P_{D(LOAD)} = \left(\frac{1}{6}\right) \times \left(\frac{12 \times 12}{24}\right) = 1 \text{ W} \quad (24)$$

The total device power dissipation during start up is:

$$P_{D(STARTUP)} = 2.72 + 1 = 3.72 \text{ W} \quad (25)$$

From thermal shutdown limit graph at T_A = 85°C, the thermal shutdown time for 3.72 W is close to 60 ms. It is safe to have 30% margin to allow for variation of system parameters such as load, component tolerance, and input voltage. So it is well within acceptable limits to use the 1 nF capacitor with start-up load of 24 Ω.

If there is a need to decrease the power loss during start-up, it can be done with increase of $C_{(SS)}$ capacitor.

To illustrate, choose $C_{(SS)}$ = 4.7 nF as an option and recalculate:

$$t_{SS} = 20.6 \times 10^{4} \times 12 \times \left(4.7 \times 10^{-9} + 70 \times 10^{-12}\right) = 11.8 \text{ ms} \quad (26)$$

$$I_{(INRUSH)} = \left(100 \times 10^{-6}\right) \times \left(\frac{12}{11.8 \times 10^{-3}}\right) = 0.102 \text{ A} \quad (27)$$

$$P_{D(INRUSH)} = 0.5 \times 12 \times 0.102 = 0.61 \text{ W} \quad (28)$$

$$P_{D(LOAD)} = \left(\frac{1}{6}\right) \times \left(\frac{12 \times 12}{24}\right) = 1 \text{ W} \quad (29)$$

$$P_{D(STARTUP)} = 0.61 + 1 = 1.61 \text{ W} \quad (30)$$

From thermal shutdown limit graph at T_A = 85°C, the shutdown time for 1.61 W power dissipation is ~1000 ms, which increases the margins further for shutdown time and ensures successful operation during start up and steady state conditions.

The spreadsheet tool available on the web can be used for iterative calculations.

10.2.1.2.5 Support Component Selections - R_4 and C_{IN}

Reference to application schematics, R_4 is required only if $\overline{FLT}$ is used; The resistor serves as pull-up for the open-drain output driver. The current sunk by this pin should not exceed 100 mA (refer to the *Absolute Maximum Ratings* table). C_{IN} is a bypass capacitor to help control transient voltages, unit emissions, and local supply noise. Where acceptable, a value in the range of 0.001 µF to 0.1 µF is recommended for $C_{(IN)}$.

10.2.1.3 Application Curves

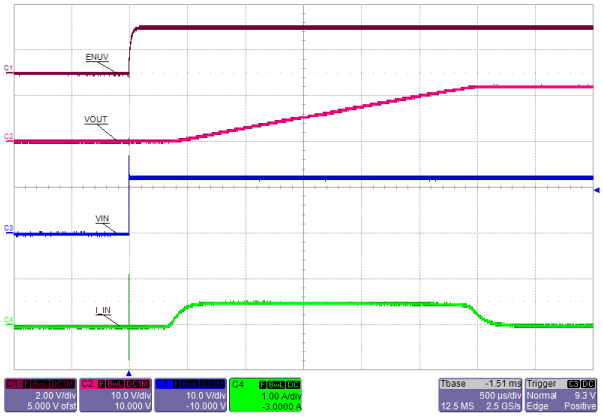


Figure 36. Hot-Plug Start-Up: Output Ramp Without Load on Output

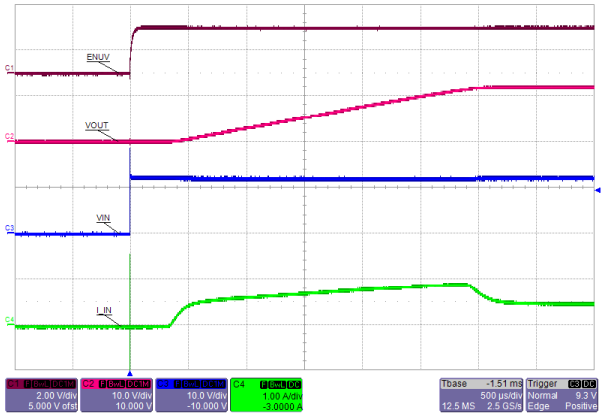


Figure 37. Hot-Plug Start-Up: Output Ramp With 24 Ω Load at Start Up

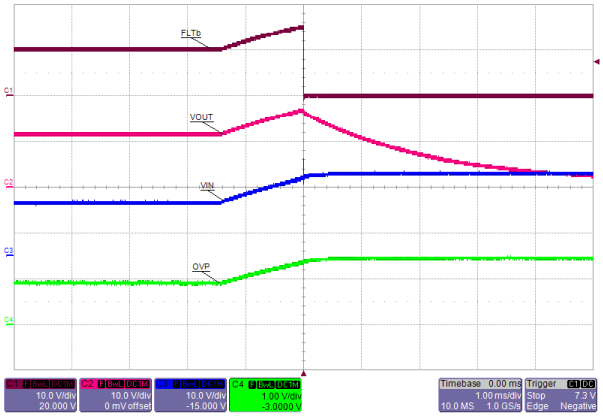


Figure 38. Overvoltage Shutdown

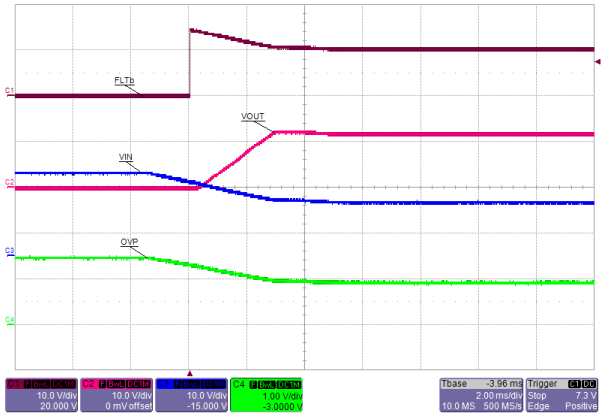


Figure 39. Overvoltage Recovery

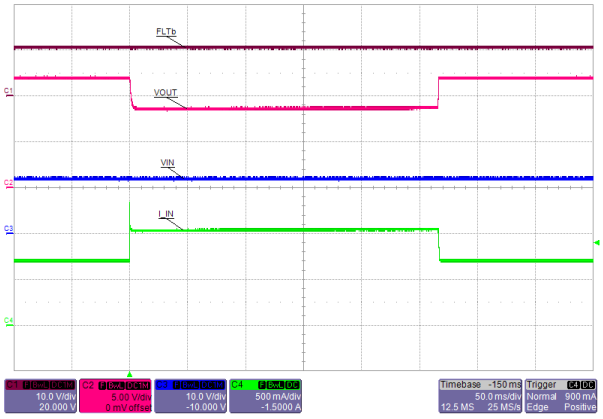


Figure 40. Over Load: Step Change in Load from 19 Ω to 9 Ω Back

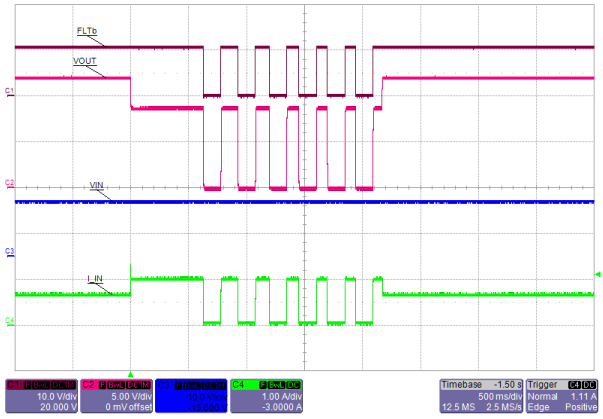


Figure 41. Overload Condition: Auto Retry and Recovery - TPS25921A

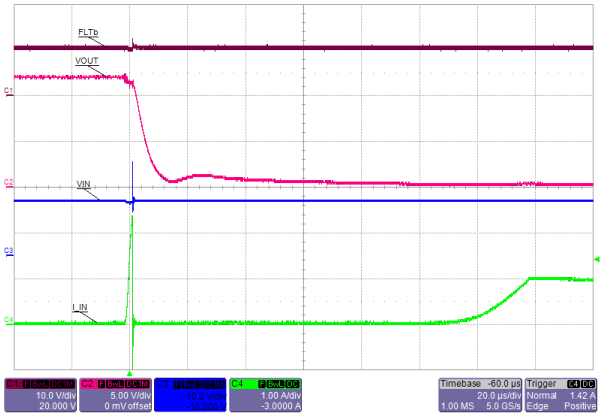


Figure 42. Hot Short: Fast Trip and Current Regulation

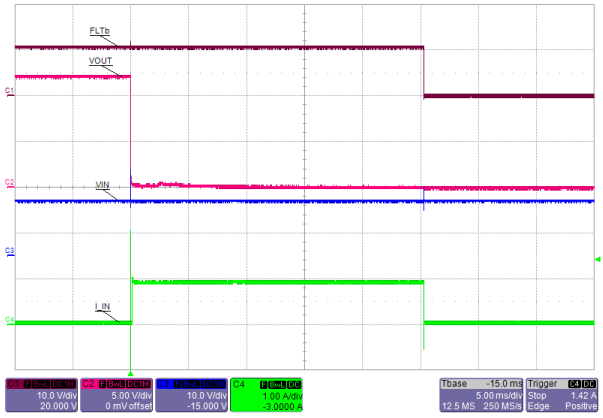


Figure 43. Hot Short: Latched - TPS25921L

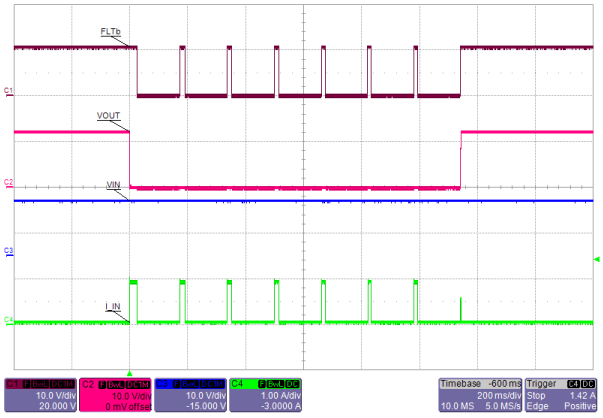


Figure 44. Hot Short: Auto-Retry and Recovery from Short Circuit - TPS25921A

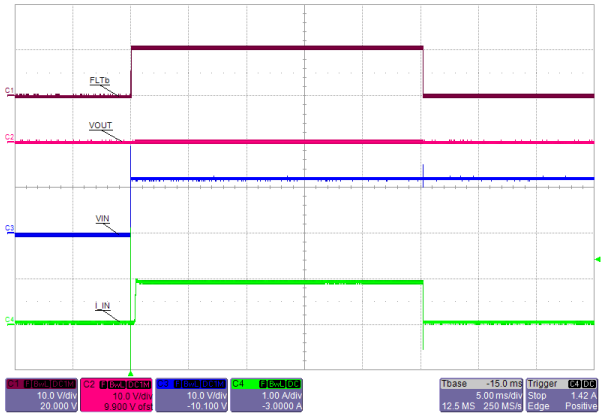


Figure 45. Hot Plug-in with Short on Output: Latched - TPS25921L

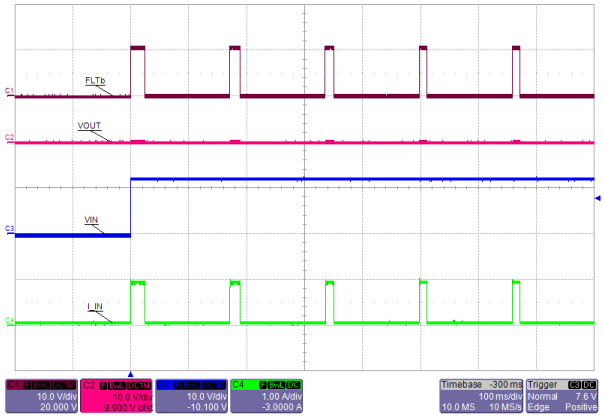


Figure 46. Hot Plug-in with Short on Output: Auto-Retry - TPS25921A

10.3 System Examples

The TPS25921 provides a simple solution for current limiting, inrush current control and supervision of power rails for wide range of applications operating at 4.5 V to 18 V and delivering up to 1.5 A.

10.3.1 Protection and Current Limiting for Primary-Side Regulated Power Supplies

Primary side regulated power supplies and adapters are dominant today in many of the applications such as Smart-phones, Portable hand-held devices, White Goods, Set-Top-Box and Gaming consoles. These supplies provide efficient, low cost and low component count solutions for power needs ranging from 5W to 30W. But, these come with drawbacks of

- No secondary side protection for immediate termination of critical faults such as short circuit and over voltage
- Do not provide precise current limiting for overload transients
- Have poor output voltage regulation for sudden change in AC input voltages - triggering output overvoltage condition

Many of the above applications require precise output current limiting and secondary side protection, driving the need for current sensing in the secondary side. This needs additional circuit implementation using precision operational amplifiers. This increases the complexity of the solution and also results in sensing losses The TPS25921 with its integrated low-ohmic N-channel FET provides a simple and efficient solution. Figure 47 shows the typical implementation using TPS25921.

System Examples (continued)

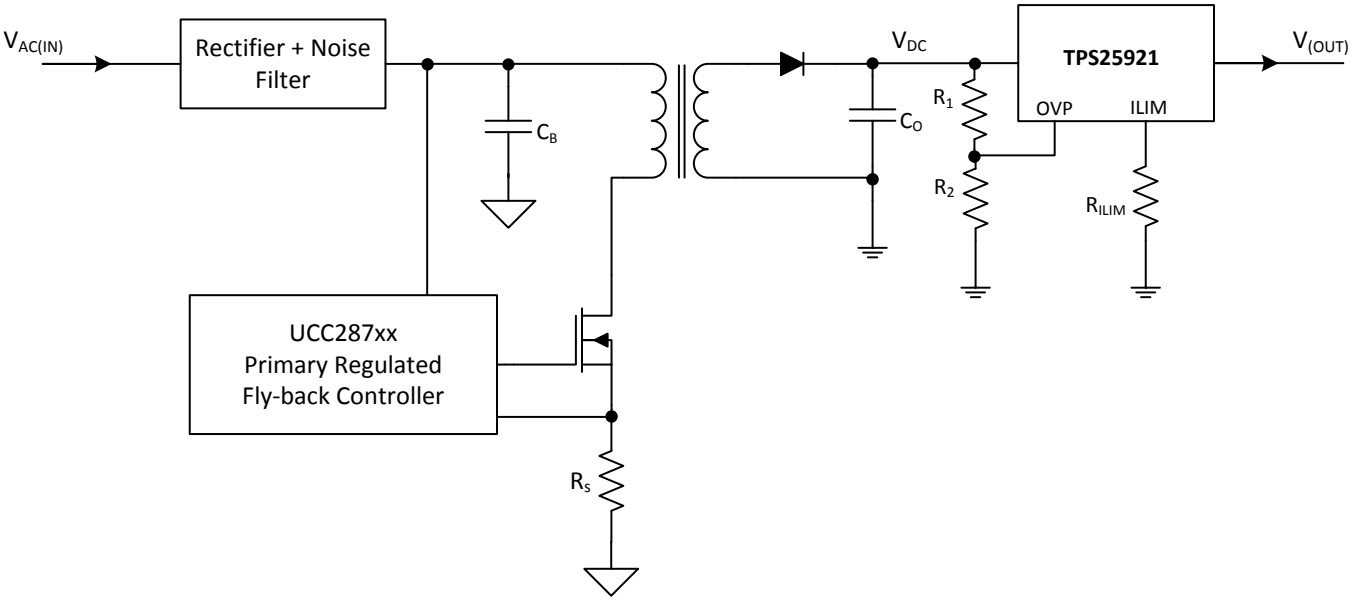


Figure 47. Current Limiting and Protection for AC-DC Power Supplies

During short circuit conditions, the internal fast comparator of TPS25921 turns OFF the internal FET in less than 3 µs (typical) as soon as current exceeds $I_{(FASTRIP)}$, set by the current limit $R_{(ILIM)}$ resistor. The OVP comparator with 3% precision helps in quick isolation of the load from the input when inputs exceeds the set $V_{(OVPR)}$

Figure 42 and Figure 38 shows short circuit and overvoltage response waveforms of implementation using TPS25921. In addition to above, the TPS25921 provides inrush current limit when output is hot-plugged into any of the system loads.

10.3.2 Precision Current Limiting in Intrinsic Safety Applications

Intrinsic safety (IS) is becoming prominent need for safe operation of electrical and electronic equipment in hazardous areas. Intrinsic safety requires that equipment is designed such that the total amount of energy available in the apparatus is simply not enough to ignite an explosive atmosphere. The energy can be electrical, in the form of a spark, or thermal, in the form of a hot surface.

This calls for precise current limiting and precision shutdown of the circuit for over voltage conditions ensuring that set voltage and current limits are not exceeded for wide operating temperature range and variable environmental conditions. Applications such as Gas Analyzers, Medical equipment (such as electrocardiographs), Portal Industrial Equipment, Cabled Power distribution systems and hand-held motor operated tools need to meet these critical safety standards.

The TPS25921 device can be used as simple protection solution for each of the internal rails. Figure 48 shows the typical implementation using TPS25921.

System Examples (continued)

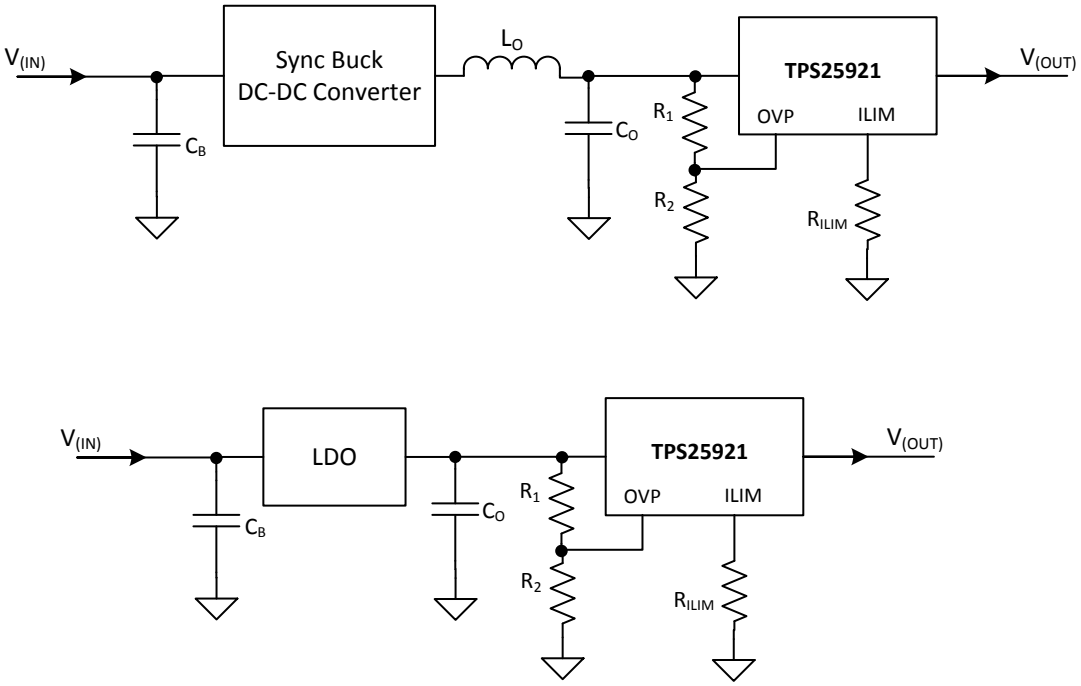


Figure 48. Precision current Limit and Protection of Internal Rails

10.3.3 Smart Load Switch

A smart load switch is a series FET used for switching of the load (resistive or inductive). It also provides protection during fault conditions. Typical discrete implementation is shown in Figure 49. Discrete solutions have higher component count and require complex circuitry to implement each of the protection fault needs.

TPS25921 can be used as a smart power switch for applications ranging from 4.5 V to 18 V. TPS25921 provides programmable soft start, programmable current limits, over-temperature protection, a fault flag, and under-voltage lockout.

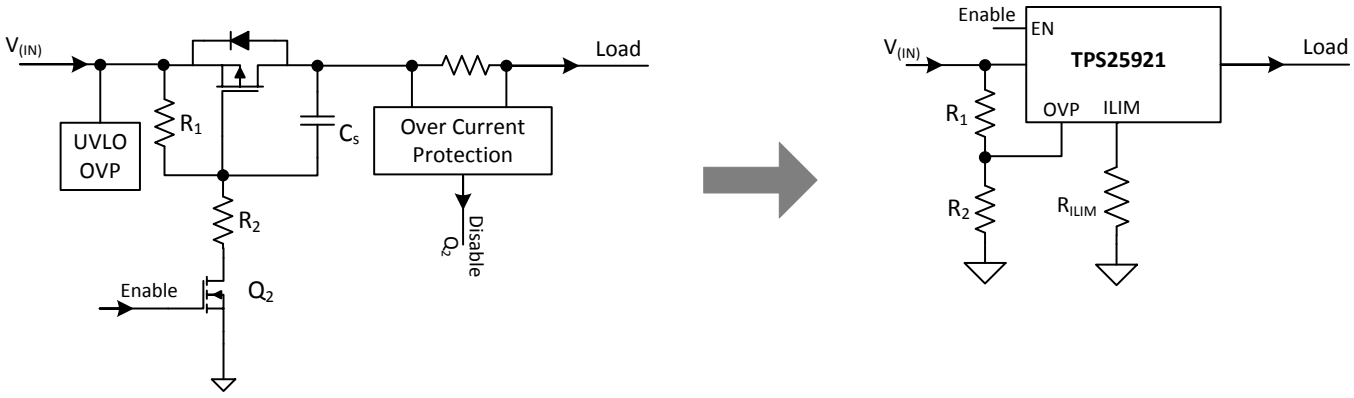


Figure 49. Smart Load Switch Implementation

Figure 49 shows typical implementation and usage as load switch. This configuration can be used for driving a solenoid and FAN control. It is recommended to use a freewheeling diode across the load when load is highly inductive.

System Examples (continued)

Figure 50 shows load switching waveforms using TPS25921 for 12 V Bus

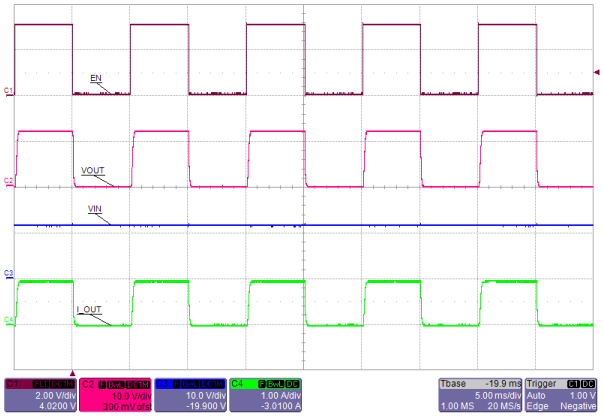


Figure 50. Smart Load Switch (100 Hz Operation)

11 Power Supply Recommendations

The device is designed for supply voltage range of 4.5 V ≤ V_{IN} ≤ 18 V. If the input supply is located more than a few inches from the device an input ceramic bypass capacitor higher than 0.1 µF is recommended. Power supply should be rated higher than the current limit set to avoid voltage droops during over current and short-circuit conditions.

11.1 Transient Protection

In case of short circuit and over load current limit, when the device interrupts current flow, input inductance generates a positive voltage spike on the input and output inductance generates a negative voltage spike on the output. The peak amplitude of voltage spikes (transients) is dependent on value of inductance in series to the input or output of the device. Such transients can exceed the *Absolute Maximum Ratings* of the device if steps are not taken to address the issue.

Typical methods for addressing transients include

- Minimizing lead length and inductance into and out of the device
- Using large PCB GND plane
- Schottky diode across the output to absorb negative spikes
- A low value ceramic capacitor ($C_{(IN)}$ = 0.001 µF to 0.1 µF) to absorb the energy and dampen the transients. The approximate value of input capacitance can be estimated with Equation 31.

$$V_{SPIKE(Absolute)} = V_{(IN)} + I_{(LOAD)} \times \sqrt{\frac{L_{(IN)}}{C_{(IN)}}} \quad (31)$$

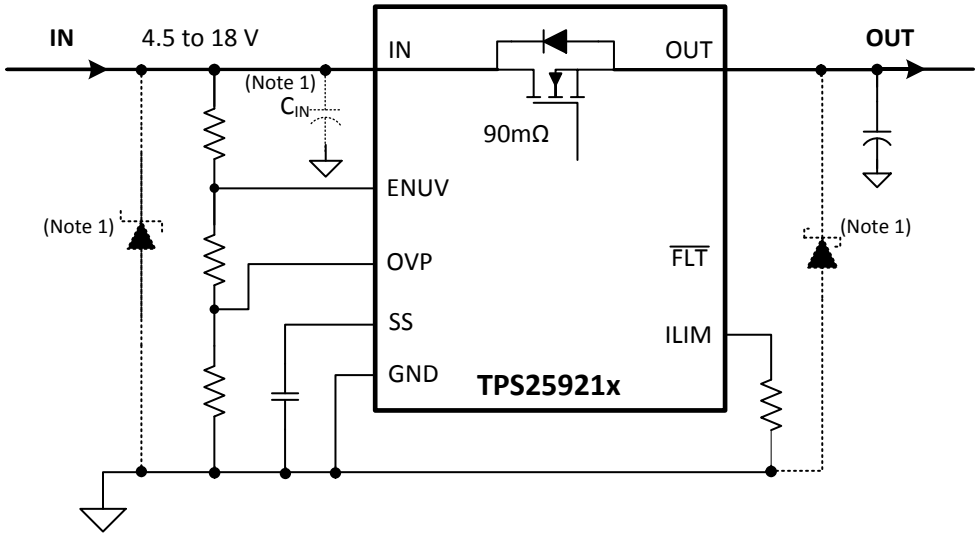
Where:

- $V_{(IN)}$ is the nominal supply voltage
- $I_{(LOAD)}$ is the load current,
- $L_{(IN)}$ equals the effective inductance seen looking into the source
- $C_{(IN)}$ is the capacitance present at the input

Some applications may require the addition of a Transient Voltage Suppressor (TVS) to prevent transients from exceeding the *Absolute Maximum Ratings* of the device.

The circuit implementation with optional protection components (a ceramic capacitor, TVS and schottky diode) is shown in Figure 51.

Transient Protection (continued)



(1) Optional components needed for suppression of transients

Figure 51. Circuit Implementation With Optional Protection Components

11.2 Output Short-Circuit Measurements

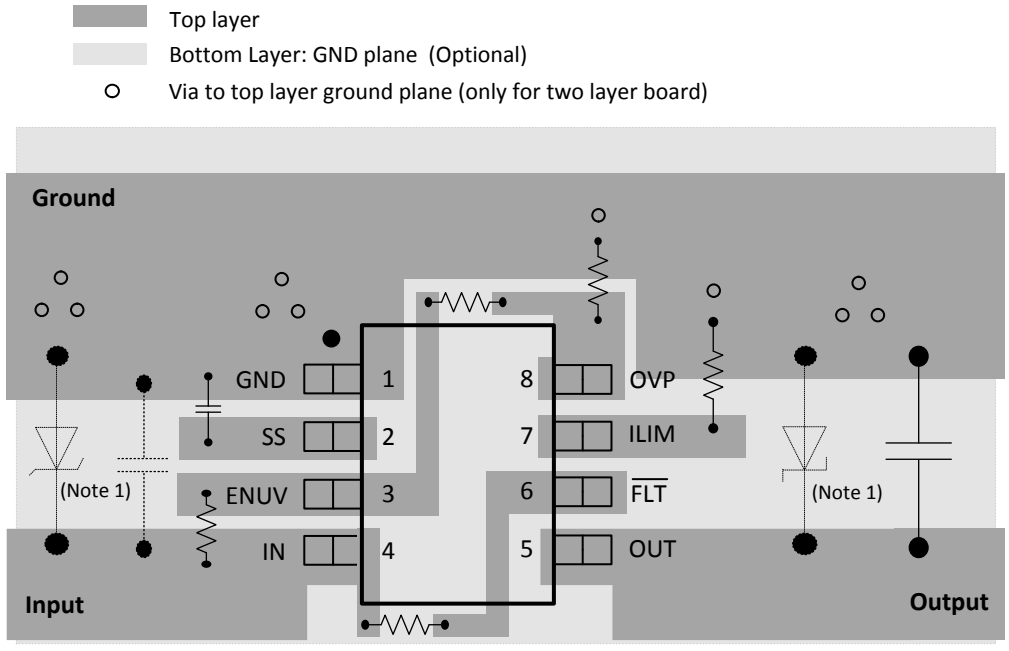
It is difficult to obtain repeatable and similar short-circuit testing results. Source bypassing, input leads, circuit layout and component selection, output shorting method, relative location of the short, and instrumentation all contribute to variation in results. The actual short itself exhibits a certain degree of randomness as it microscopically bounces and arcs. Care in configuration and methods must be used to obtain realistic results. Do not expect to see waveforms exactly like those in the data sheet; every setup differs.

12 Layout

12.1 Layout Guidelines

- For all applications, a 0.01-uF or greater ceramic decoupling capacitor is recommended between IN terminal and GND. For hot-plug applications, where input power path inductance is negligible, this capacitor can be eliminated/minimized.
- The optimum placement of decoupling capacitor is closest to the IN and GND terminals of the device. Care must be taken to minimize the loop area formed by the bypass-capacitor connection, the IN terminal, and the GND terminal of the IC. See Figure 52 for a PCB layout example.
- High current carrying power path connections should be as short as possible and should be sized to carry at least twice the full-load current.
- The GND terminal must be tied to the PCB ground plane at the terminal of the IC. The PCB ground should be a copper plane or island on the board.
- Locate all TPS25921x support components: $R_{(ILIM)}$, C_{SS}, and resistors for $\overline{FLT}$, ENUV and OVP, close to their connection pin. Connect the other end of the component to the GND pin of the device with shortest trace length.
- The trace routing for the R_{ILIM} and C_{SS} components to the device should be as short as possible to reduce parasitic effects on the current limit and soft start timing. These traces should not have any coupling to switching signals on the board.
- OVP and ENUV signal traces should be routed with sufficient spacing from $\overline{FLT}$ signal trace, to avoid spurious coupling of $\overline{FLT}$ switching, during fault conditions.
- Protection devices such as TVS, snubbers, capacitors, or diodes should be placed physically close to the device they are intended to protect, and routed with short traces to reduce inductance. For example, a protection Schottky diode is recommended to address negative transients due to switching of inductive loads, and it should be physically close to the OUT pins.
- Obtaining acceptable performance with alternate layout schemes is possible; however this layout has been shown to produce good results and is intended as a guideline.

12.2 Layout Example



(1) Optional: Needed only to suppress the transients caused by inductive load switching.

Figure 52. Board Layout

13 Device and Documentation Support

13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
TPS25921A	Click here	Click here	Click here	Click here	Click here
TPS25921L	Click here	Click here	Click here	Click here	Click here

13.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

13.4 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
TPS25921AD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	25921A
TPS25921AD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	25921A
TPS25921ADR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	25921A
TPS25921ADR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	25921A
TPS25921ADRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	25921A
TPS25921ADRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	25921A
TPS25921LD	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	25921L
TPS25921LD.A	Active	Production	SOIC (D) | 8	75 | TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	25921L
TPS25921LDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	25921L
TPS25921LDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	25921L
TPS25921LDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	25921L
TPS25921LDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	25921L

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

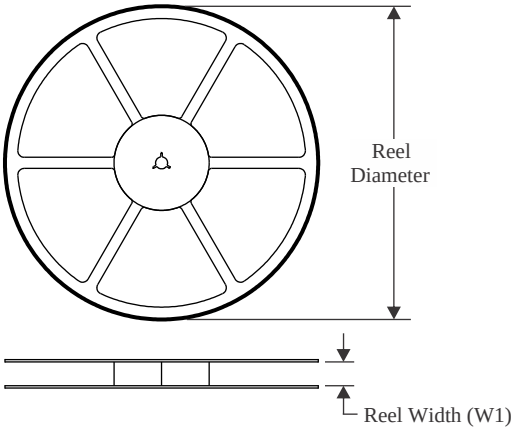
(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

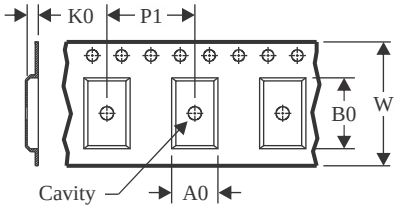
Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

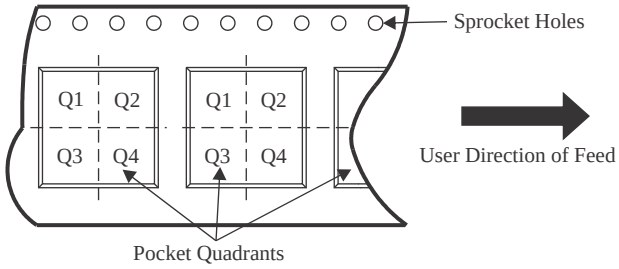


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

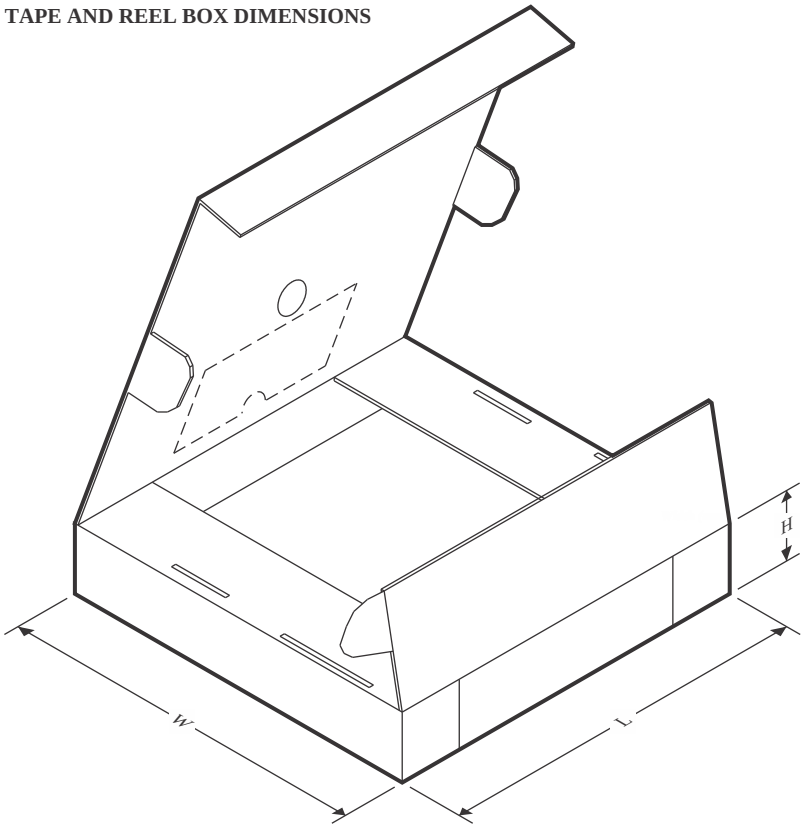
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS25921ADR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS25921ADRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS25921LDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
TPS25921LDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

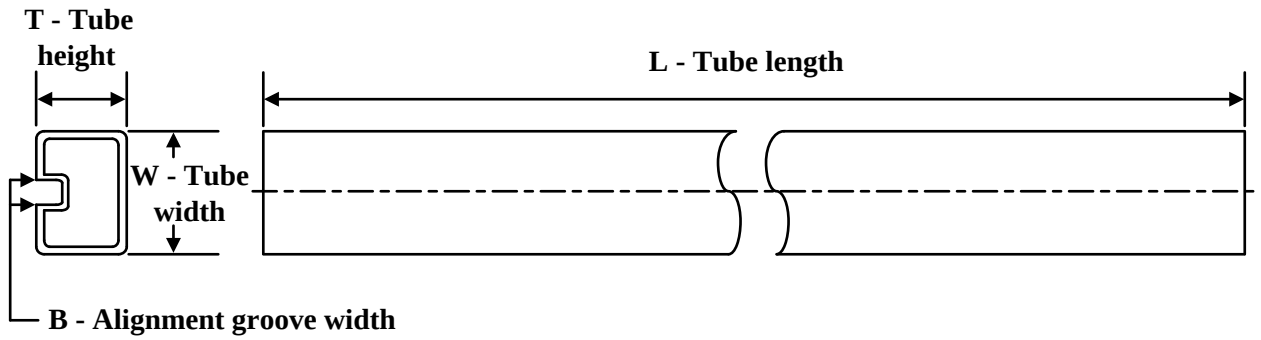
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

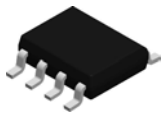
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS25921ADR	SOIC	D	8	2500	353.0	353.0	32.0
TPS25921ADRG4	SOIC	D	8	2500	353.0	353.0	32.0
TPS25921LDR	SOIC	D	8	2500	353.0	353.0	32.0
TPS25921LDRG4	SOIC	D	8	2500	353.0	353.0	32.0

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
TPS25921AD	D	SOIC	8	75	507	8	3940	4.32
TPS25921AD.A	D	SOIC	8	75	507	8	3940	4.32
TPS25921LD	D	SOIC	8	75	507	8	3940	4.32
TPS25921LD.A	D	SOIC	8	75	507	8	3940	4.32

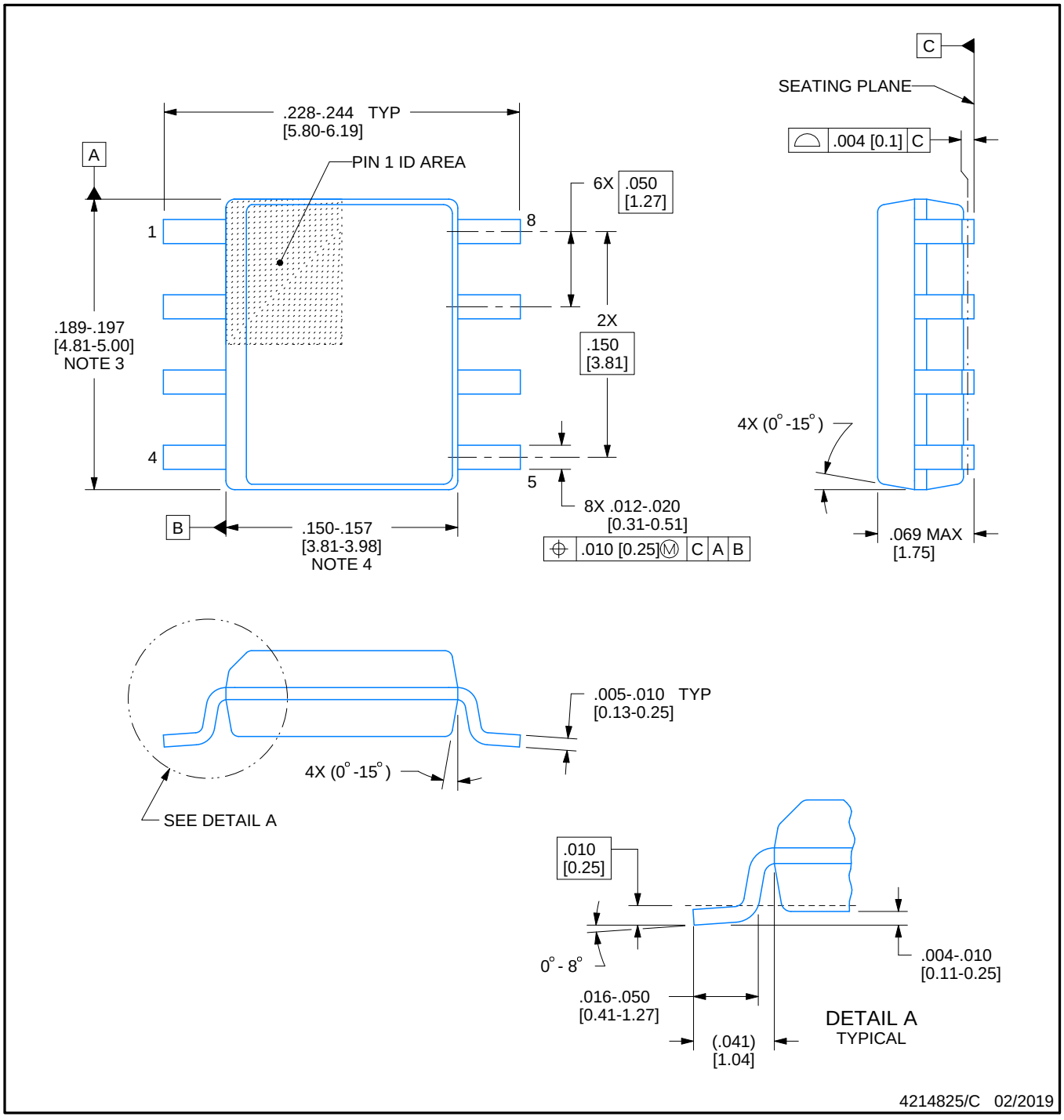


PACKAGE OUTLINE

D0008A

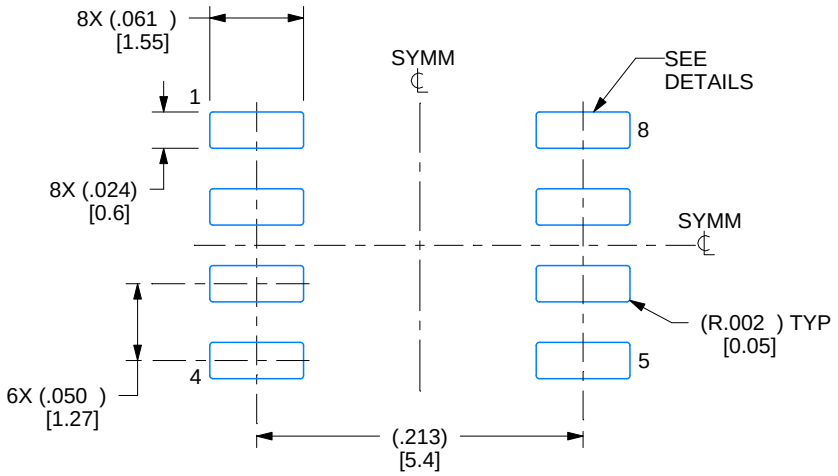
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

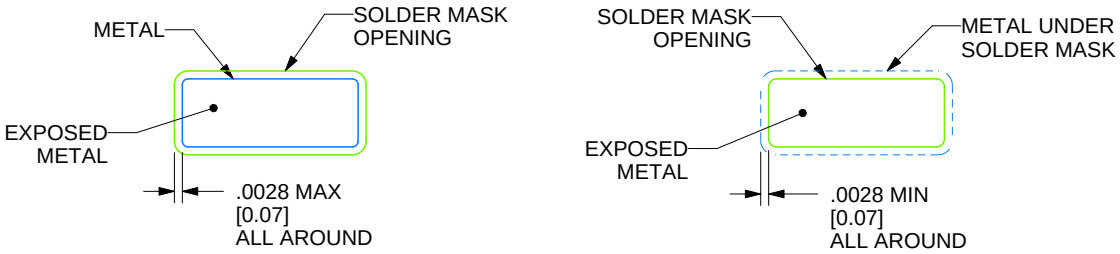


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

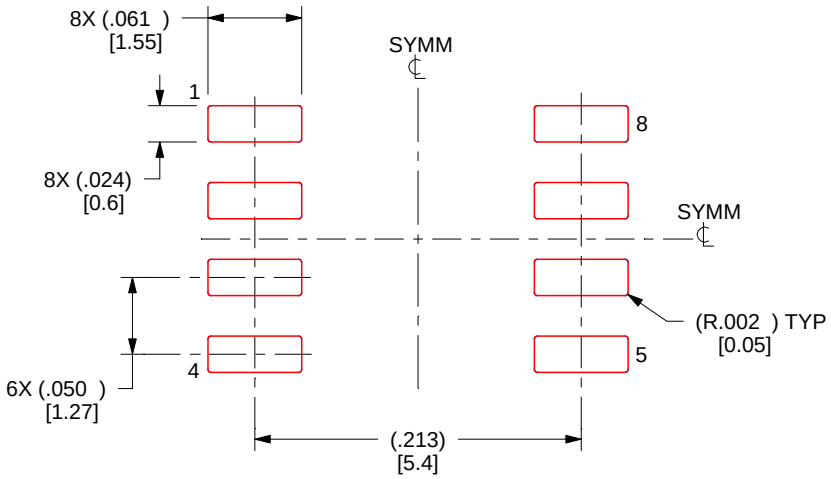
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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