TEXAS INSTRUMENTS
TPS3762-Q1
JAJSRP6 – OCTOBER 2023

TPS3762-Q1 車載用ワイド VIN 65V ウィンドウ (OV および UV) スーパーバイザ、内蔵セルフ・テスト付き

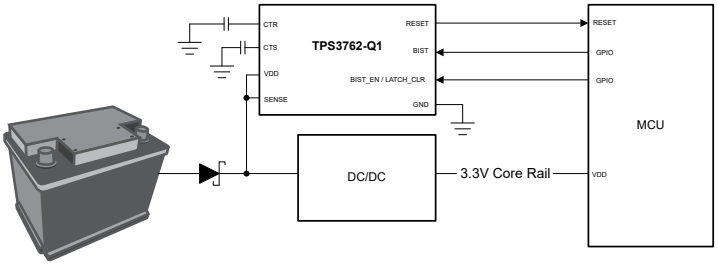
ADVANCE INFORMATION

1 特長

- ASIL-D 機能安全準拠製品向け
  - 機能安全アプリケーション向け開発
  - ISO 26262 システムの設計に役立つ資料
  - ASIL-D までの決定論的対応能力に対応予定
  - ASIL-D までのハードウェア対応能力に対応予定
- 車載アプリケーション向けに AEC-Q100 認定済み
  - デバイス温度グレード 1:-40℃～+125℃
- 高電圧電源レールを監視
  - 幅広い入力電圧範囲:2.7V～65V
  - センス・ピン -65V の逆極性保護
  - 高電圧レールの電源オフに外付け部品が不要
- 設計要件を満たすデバイスの柔軟性
  - 幅広い電圧スレッショルド範囲:2.7V～60V
  - 800mV オプション - スレッショルドを設定するには、外付け分割抵抗と併用
  - ヒステリシス内蔵 (2%、5%、10% のオプション)
  - 固定またはプログラム可能なリセット時間遅延
  - 固定およびプログラム可能な検出遅延
- 安全アプリケーション向けに設計
  - 出力リセット・ラッチ機能により、システムを安全な状態に移行
  - 超高速の検出時間遅延 (5µs 未満) により、システムのフォルト・トレラント時間間隔 (FTTI) を最小化
  - デバイスの機能を監視し、システム保護を強化するための内蔵セルフ・テスト

2 アプリケーション

- センサ・フュージョンおよびカメラ
- デジタル・コックピット処理装置
- オンボード充電器
- ADAS ドメイン・コントローラ



代表的なアプリケーション回路

3 概要

TPS3762-Q1 は、4µA I_{DD}、0.8% 精度、高速検出時間、内蔵セルフテスト機能を備えた 65V 入力電圧スーパーバイザです。このデバイスは 12V/24V 車載用バッテリ・システムに直接接続し、過電圧 (OV) または低電圧 (UV) 状態を継続的に監視できます。また、分割抵抗を内蔵しているため、TPS3762-Q1 はソリューション全体のサイズを最小化できます。コールド・クランク、スタート / ストップ、車の各種バッテリ電圧過渡の影響を受けないように、幅広いヒステリシス電圧オプションを選択できます。SENSE ピンに組み込まれたヒステリシスは、電源電圧レール監視中のリセット信号の誤検出を防止します。

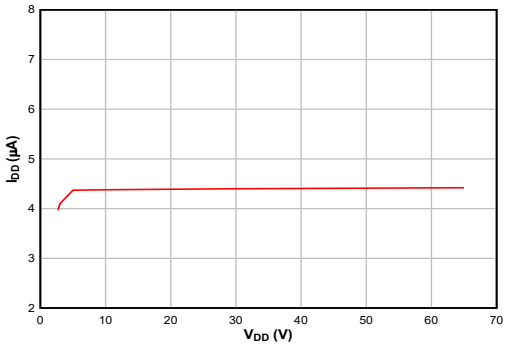
VDD ピンと SENSE ピンが独立しているため、信頼性が高い車載用システムが求める冗長性を実現できます。また、SENSE は VDD よりも高い電圧と低い電圧を監視できます。SENSE ピンは高インピーダンス入力なので外付け抵抗を使うこともできます。CTS ピンおよび CTR ピンを使うことで、RESET 信号の立ち上がり / 立ち下がりエッジの遅延を調整できます。CTS は、監視対象の電圧レールの電圧グリッチを無視することで、デバウンシング機能として機能します。

TPS3762-Q1 は、2.9mm × 1.6mm の SOT23 8 ピン・パッケージで供給されます。TPS3762-Q1 は -40℃～+125℃の T_A で動作します。

製品情報

部品番号	パッケージ (1)	本体サイズ (公称)
TPS3762-Q1	SOT-23 (8) (DDF)	2.9mm × 1.6mm

(1) パッケージの詳細については、このデータシートの末尾の外形図を参照してください。



I_{DD} と V_{DD} との代表的な関係 ($\overline{RESET}$ = Low、V_{IT} = 0.8V)

ADVANCE INFORMATION

Table of Contents

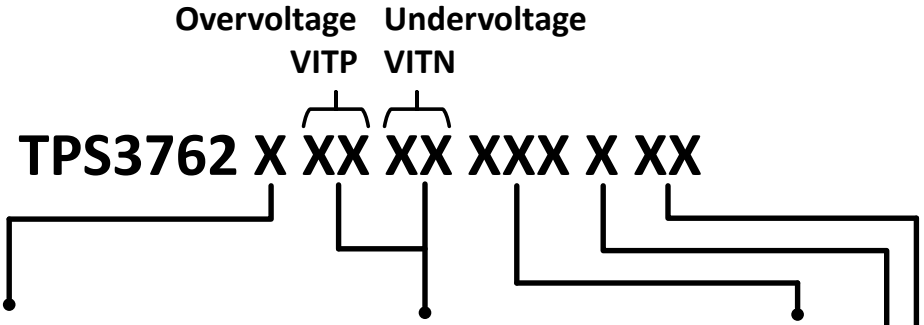
4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

DATE	REVISION	NOTES
October 2023	*	Initial Release

5 Device Comparison

Device Decoder shows some of the device naming nomenclature of the TPS3762-Q1. Not all device namings follow this nomenclature table. For a detailed breakdown of every device part number by threshold voltage options, BIST configurations, Latch configurations, CTR options, CTS options, and UV bypass, see セクション 10.1 for more details. Contact TI sales representatives or on TI's E2E forum for detail and availability of other options.



Topology

Suffix	CTR	CTS	Latch / UV Bypass	BIST RESET Trigger
A	ADJ	ADJ	Disabled	Yes
B	ADJ	ADJ	Latch	Yes
C	ADJ	ADJ	UVBypass	Yes
D	ADJ	ADJ	Both	Yes
E	ADJ	5 µs	Disabled	Yes
F	ADJ	5 µs	Latch	Yes
G	ADJ	5 µs	UVBypass	Yes
H	ADJ	5 µs	Both	Yes
I	ADJ	ADJ	Disabled	No
J	ADJ	ADJ	Latch	No
K	ADJ	ADJ	UVBypass	No
L	ADJ	ADJ	Both	No
M	ADJ	5 µs	Disabled	No
N	ADJ	5 µs	Latch	No
O	ADJ	5 µs	UVBypass	No
P	ADJ	5 µs	Both	No
Q	200ms	5 µs	Disabled	Yes
R	200ms	5 µs	Latch	Yes

Threshold Voltage

2% Hysteresis Option

Suffix	VIT	Suffix	VIT
02	800mV	D7	8.5V
A7	2.7V	D8	9V
A8	2.8V	D9	9.5V
A9	2.9V	E0	10V
B0	3V	E1	11V
B1	3.1V	E2	12V
B2	3.2V	E3	13V
B3	3.3V	E4	14V
B4	3.4V	E5	15V
B5	3.5V	E6	16V
B6	3.6V	E7	17V
B7	3.7V	E8	18V
B8	3.8V	E9	20V
B9	3.9V	F0	22V
C0	4V	F1	24V
C1	4.1V	F2	26V
C2	4.2V	F3	28V
C3	4.3V	F4	30V
C4	4.4V	F5	32V
C5	4.5V	F6	34V
C6	4.6V	F7	36V
C7	4.7V	F8	38V
C8	4.8V	F9	40V
C9	4.9V	G0	42V
D0	5V	G1	46V
D1	5.5V	G2	48V
D2	6V	G3	50V
D3	6.5V	G4	54V
D4	7V	G5	57V
D5	7.5V	G6	58V
D6	8V	G7	60V
W7	+/-7%		
UV	UV Only	OV	OV Only

5% Hysteresis Option

Suffix	VIT	Suffix	VIT
05	800mV	K7	8.5V
H7	2.7V	K8	9V
H8	2.8V	K9	9.5V
H9	2.9V	L0	10V
I0	3V	L1	11V
I1	3.1V	L2	12V
I2	3.2V	L3	13V
I3	3.3V	L4	14V
I4	3.4V	L5	15V
I5	3.5V	L6	16V
I6	3.6V	L7	17V
I7	3.7V	L8	18V
I8	3.8V	L9	20V
I9	3.9V	M0	22V
J0	4V	M1	24V
J1	4.1V	M2	26V
J2	4.2V	M3	28V
J3	4.3V	M4	30V
J4	4.4V	M5	32V
J5	4.5V	M6	34V
J6	4.6V	M7	36V
J7	4.7V	M8	38V
J8	4.8V	M9	40V
J9	4.9V	N0	42V
K0	5V	N1	46V
K1	5.5V	N2	48V
K2	6V	N3	50V
K3	6.5V	N4	54V
K4	7V	N5	57V
K5	7.5V	N6	58V
K6	8V	N7	60V

10% Hysteresis Option

Suffix	VIT	Suffix	VIT
10	800mV	Q1	4.1V
O7	2.7V	Q2	4.2V
O8	2.8V	Q3	4.3V
O9	2.9V	Q4	4.4V
P0	3V	Q5	4.5V
P1	3.1V	Q6	4.6V
P2	3.2V	Q7	4.7V
P3	3.3V	Q8	4.8V
P4	3.4V	Q9	4.9V
P5	3.5V	R0	5V
P6	3.6V	R1	5.5V
P7	3.7V	R2	6V
P8	3.8V	R3	6.5V
P9	3.9V	R4	7V
Q0	4V	R5	7.5V

10% Hysteresis Option

Suffix	VIT	Suffix	VIT
R6	8V	T2	26V
R7	8.5V	T3	28V
R8	9V	T4	30V
R9	9.5V	T5	32V
S0	10V	T6	34V
S1	11V	T7	36V
S2	12V	T8	38V
S3	13V	T9	40V
S4	14V	U0	42V
S5	15V	U1	46V
S6	16V	U2	48V
S7	17V	U3	50V
S8	18V	U4	54V
S9	20V	U5	57V
T0	22V	U6	58V
T1	24V	U7	60V

Package

Suffix	Name
DDF	SOT-23

Reel

Suffix	Name
R	Large

Rating

Suffix	Name
Q1	AUTO

1. Suffix 02, 05, and 10 with VIT of 800 mV corresponds to the adjustable variant, do not have internal voltage divider
2. Not all TPS3762-Q1 devices can be decoded by this table. Refer to セクション 10.1 for a decoding table by part number.

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6 Pin Configuration and Functions

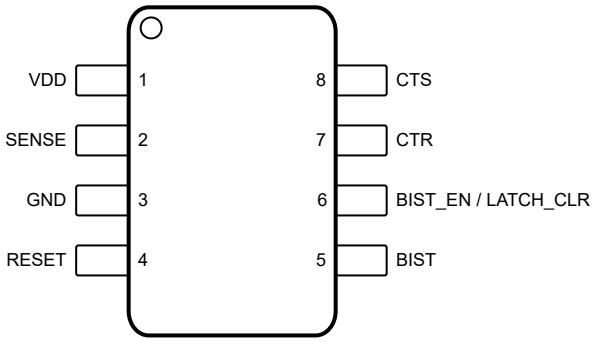


図 6-1. DDF Package, 8-Pin SOT-23, TPS3762-Q1 (Top View)

表 6-1. Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
VDD	1	I	**Input Supply Voltage:** Bypass with a 0.1 µF capacitor to GND.
SENSE	2	I	**Sense Voltage:** Connect this pin to the supply rail that must be monitored. See Section 8.3.2 for more details. Sensing Topology: **Overvoltage (OV) or Undervoltage (UV) or Window (OV + UV)**
GND	3	-	**Ground.** All GND pins must be electrically connected to the board ground.
$\overline{\text{RESET}}$	4	O	**Output Reset Signal:** $\overline{\text{RESET}}$ asserts when SENSE crosses the voltage threshold after the sense time delay, set by CTS. $\overline{\text{RESET}}$ remains asserted for the reset time delay period after SENSE transitions out of a fault condition. The active low open-drain reset output requires an external pullup resistor. See Section 8.3.3.2 for more details. Output topology: **Open-Drain Active-Low**
BIST	5	O	**Built-In Self-Test:** BIST asserts when BIST_EN or BIST_EN/LATCH_CLR activated the internal BIST testing. BIST recovers once after TD_BIST to signify BIST completed successfully. BIST remains asserted for a time period longer than TD_BIST if there is a failure during BIST. BIST active-low open-drain output requires an external pullup resistor. Refer to BIST section for more details. See Section 8.3.6 for more details.
BIST_EN / LATCH_CLR	6	I	**Built-in Self-test Enable and Latch Clear:** A rising transition (edge) must occur at BIST_EN/LATCH_CLR to initiate BIST and clear $\overline{\text{OV}}$/$\overline{\text{UV}}$ fault. See Section 8.3.6 for more details.
CTR	7	O	**RESET Time Delay:** User-programmable reset time delay for $\overline{\text{RESET}}$/RESET. Connect an external capacitor for adjustable time delay or leave the pin floating for the shortest delay. See Section8.3.4 for more details.
CTS	8	O	**SENSE Time Delay:** User-programmable sense time delay for SENSE. Connect an external capacitor for adjustable time delay or leave the pin floating for the shortest delay. See Section 8.3.5 for more details.

7 Specifications

7.1 仕様

7.1.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted (1)

		MIN	MAX	UNIT
Voltage	V_{DD}, $V_{SENSE(Adjustable)}$, $V_{\overline{RESET}}$	–0.3	70	V
Voltage	$V_{SENSE(Fixed)}$	–65	70	V
Voltage	V_{CTS}, V_{CTR}	–0.3	6	V
Voltage	V_{BIST}, V_{BIST_EN}, $V_{BIST\_EN/LATCH\_CLR}$	–0.3	6	V
Current	I_{RESET}, I_{BIST}		10	mA
Temperature (2)	Operating junction temperature, T_J	–40	150	°C
Temperature (2)	Operating Ambient temperature, T_A	–40	150	°C
Temperature (2)	Storage, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

7.1.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002 (1)	±2000	V
		Charged device model (CDM), per AEC Q100-011	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.1.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Voltage	V_{DD}	2.7		65	V
Voltage	V_{SENSE}, $V_{\overline{RESET}}$	0		65	V
Voltage	V_{CTS}, V_{CTR}	0		5.5	V
Voltage	V_{BIST}, V_{BIST_EN}, $V_{BIST\_EN/LATCH\_CLR}$	0		5.5	V
Current	I_{RESET}, I_{BIST}	0		±5	mA
T_J	Junction temperature (free air temperature)	–40		125	°C

ADVANCE INFORMATION

7.1.4 Thermal Information

THERMAL METRIC (1)		TPS3762-Q1 DDF 8-PIN	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	154.6	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	77.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	73.2	°C/W
ψ_{JT}	Junction-to-top characterization parameter	4.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	72.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

ADVANCE INFORMATION

7.1.5 Electrical Characteristics

At $V_{DD(MIN)} \le V_{DD} \le V_{DD\ (MAX)}$, CTR = CTS = open, output reset pull-up resistor R_{PU} = 10 kΩ, voltage V_{PU} = 5.5 V, output BIST pull-up resistor R_{PU_BIST} = 10 kΩ, voltage V_{PU_BIST} = 5.5 V, and load C_{LOAD} = 10 pF. The operating free-air temperature range T_A = – 40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C and VDD = 16 V and V_{IT} = 6.5 V (V_{IT} refers to V_{ITN} or V_{ITP}).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VDD						
V_{DD}	Supply Voltage		2.7		65	V
UVLO (1)	Undervoltage Lockout	V_{DD} rising above $V_{DD\ (MIN)}$			2.6	V
UVLO(HYS) (1)	Undervoltage Lockout Hysteresis	V_{DD} falling below $V_{DD\ (MIN)}$		500		mV
V_{POR}	Power on Reset Voltage (2) $\overline{RESET}$, Active Low (Open-Drain)	$V_{OL(MAX)}$ = 300 mV $I_{OUT\ (Sink)}$ = 15 µA			1.4	V
I_{DD}	Supply current into VDD pin	V_{IT} = 800 mV $V_{DD\ (MIN)} \le V_{DD} \le V_{DD\ (MAX)}$			8.1	µA
SENSE (Input)						
I_{SENSE}	Input current	V_{IT} = 800 mV			200	nA
V_{ITN}	Input Threshold Negative (Undervoltage)	V_{IT} = 800 mV (3)	-0.8		0.8	%
V_{ITP}	Input Threshold Positive (Overvoltage)	V_{IT} = 800 mV (3)	-0.8		0.8	%
V_{HYS}	Hysteresis Accuracy (4)	V_{IT} = 0.8 V V_{HYS} Range = 2%	1.5	2	2.5	%
V_{HYS}	Hysteresis Accuracy (4)	V_{IT} = 0.8 V V_{HYS} Range = 5%	4.5	5	6	%
V_{HYS}	Hysteresis Accuracy (4)	V_{IT} = 0.8 V V_{HYS} Range = 10%	9	10	11	%
RESET (Output)						
$I_{lkg(OD)}$	Open-Drain leakage	V_{RESET} = 5.5 V $V_{ITN} < V_{SENSE} < V_{ITP}$			300	nA
$I_{lkg(OD)}$	Open-Drain leakage	V_{RESET} = 65 V $V_{ITN} < V_{SENSE} < V_{ITP}$			300	nA
V_{OL} (5)	Low level output voltage	2.7 V ≤ VDD ≤ 65 V I_{RESET} = 2.7 mA			350	mV

ADVANCE INFORMATION

7.1.5 Electrical Characteristics (続き)

At $V_{DD(MIN)} \le V_{DD} \le V_{DD\ (MAX)}$, CTR = CTS = open, output reset pull-up resistor R_{PU} = 10 kΩ, voltage V_{PU} = 5.5 V, output BIST pull-up resistor R_{PU_BIST} = 10 kΩ, voltage V_{PU_BIST} = 5.5 V, and load C_{LOAD} = 10 pF. The operating free-air temperature range T_A = – 40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C and VDD = 16 V and V_{IT} = 6.5 V (V_{IT} refers to V_{ITN} or V_{ITP}).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Capacitor Timing (CTS, CTR)						
R_{CTR}	Internal resistance (CTR)			3600		Kohm
R_{CTS}	Internal resistance (CTS)			3600		Kohm
Built-In Self-Test						
$I_{lkg(BIST)}$	Open-Drain leakage	V_{BIST} = 5.5 V $V_{ITN} < V_{SENSE} < V_{ITP}$			300	nA
$I_{lkg(BIST)}$	Open-Drain leakage	V_{BIST} = 3.3 V $V_{ITN} < V_{SENSE} < V_{ITP}$			300	nA
V_{BIST_OL}	Low level output voltage	2.7 V ≤ VDD ≤ 65 V I_{BIST} = 5 mA			300	mV
V_{BIST_EN}	BIST_EN pin logic low input				500	mV
V_{BIST_EN}	BIST_EN pin logic high input		1300			mV
$V_{BIST\_EN/LATCH\_CLR}$	BIST_EN pin logic low input				500	mV
$V_{BIST\_EN/LATCH\_CLR}$	BIST_EN pin logic high input		1300			mV

(1) When V_{DD} voltage falls below UVLO, reset is asserted for Sense. V_{DD} slew rate ≤ 100 mV / µs
(2) V_{POR} is the minimum V_{DD} voltage for a controlled output state. Below V_{POR}, the output cannot be determined. V_{DD} slew rate ≤ 100mV/µs
(3) For adjustable voltage guidelines and resistor selection refer to **Adjustable Voltage Thresholds** in **Application and Implementation section**
(4) Hysteresis is with respect to V_{ITP} and V_{ITN} voltage threshold. V_{ITP} has negative hysteresis and V_{ITN} has positive hysteresis.
(5) For V_{OH} and V_{OL} relation to output variants refer to **Timing Figures after the Timing Requirement Table**

ADVANCE INFORMATION

7.1.6 Timing Requirements

At $V_{DD(MIN)} \le V_{DD} \le V_{DD\ (MAX)}$, CTR = CTS = open and enabled, output reset pull-up resistor R_{PU} = 10 kΩ, voltage V_{PU} = 5.5 V, output BIST pull-up resistor R_{PU_BIST} = 10 kΩ, voltage V_{PU_BIST} = 5.5 V, and load C_{LOAD} = 10 pF. The operating free-air temperature range T_A = – 40°C to 125°C, unless otherwise noted. Typical values are at T_A = 25°C and VDD = 16 V and V_{IT} = 6.5 V (V_{IT} refers to V_{ITN} or V_{ITP}).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Common timing parameters						
t_{CTR}	Reset release time delay (CTR)(2)	CT delay accuracy not counting external cap tolerance	-20		20	%
$t_{CTR(No\ Cap)}$	Reset release time delay (CTR)(2)	VIT = 800 mV C_{CTR} = Open 20% Overdrive from Hysteresis			455	µs
t_{CTS}	Sense detect time delay (CTS)(3)	CT delay accuracy not counting external cap tolerance	-20		20	%
$t_{CTS(No\ Cap)}$	Sense detect time delay (CTS)(3)	VIT = 800 mV C_{CTS} = Open 20% Overdrive from V_{IT}		75	100	µs
t_{SD}	Startup Delay (3)	C_{CTR} = Open		1		ms
t_{GI_SNS}	Sense Glitch	10% overdrive, Fixed threshold		55		µs
BIST timing parameters						
$t_{BIST\_en\ Glitch}$	BIST EN Glitch immunity			1.6		µs
t_{BIST_en}	BIST EN input width to initiate BIST			3.5	8	µs
$t_{BIST\_en\_pd}$	Rising edge of BIST_EN to BIST asserting			4		µs
$t_{BIST\_en\_pd}$	Rising edge of BIST_EN to RESET asserting			4		µs
$t_{BIST\_recover}$	Rising edge of BIST to SENSE input valid	CTR = 0		350	600	µs
t_{BIST_test}	Test time for BIST				2.5	ms
LATCH timing parameters						
$t_{BIST\_EN/LATCH\_CLR\ Glitch}$	Latch Glitch immunity			2000		ns
$t_{BIST\_EN/LATCH\_CLR}$	Latch input width to clear latch			3		µs
$t_{BIST\_EN/LATCH\_CLR\_recover}$	rising edge of $t_{BIST\_EN/LATCH\_clr}$ to SENSE input valid			10		µs

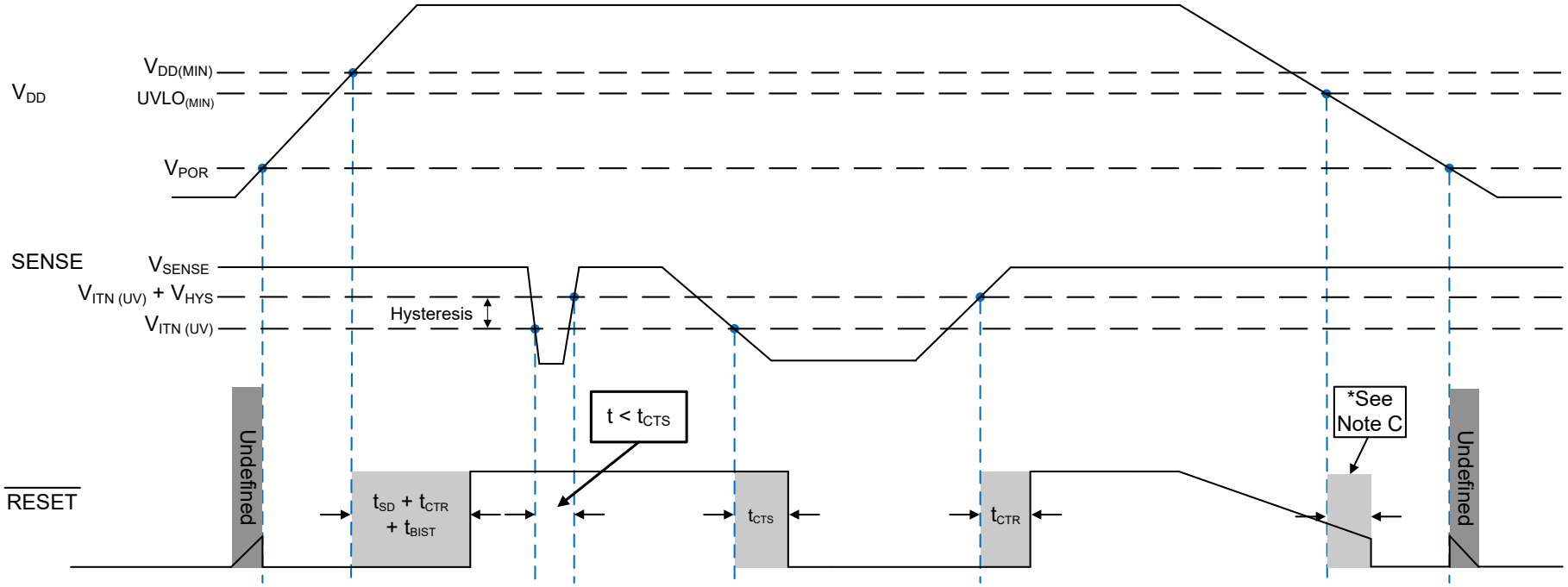
(1) **CTR Reset detect time delay:**
Overvoltage active-LOW output is measure from $V_{ITP\ -\ HYS}$ to V_{OH}
Undervoltage active-LOW output is measure from $V_{ITN\ +\ HYS}$ to V_{OH}
Overvoltage active-HIGH output is measure from $V_{ITP\ -\ HYS}$ to V_{OL}
Undervoltage active-HIGH output is measure from $V_{ITN\ +\ HYS}$ to V_{OL}

(2) **CTS Sense detect time delay:**
Active-low output is measure from V_{IT} to V_{OL} (or V_{Pullup})
Active-high output is measured from V_{IT} to V_{OH}
V_{IT} refers to either V_{ITN} or V_{ITP}

(3) During the power-on sequence, V_{DD} must be at or above $V_{DD\ (MIN)}$ for at least t_{SD} before the output is in the correct state based on V_{SENSE}.
t_{SD} time includes the propagation delay (C_{CTR} = Open). Capaicitor in C_{CTR} will add time to t_{SD}.

ADVANCE INFORMATION

7.2 Timing Diagrams



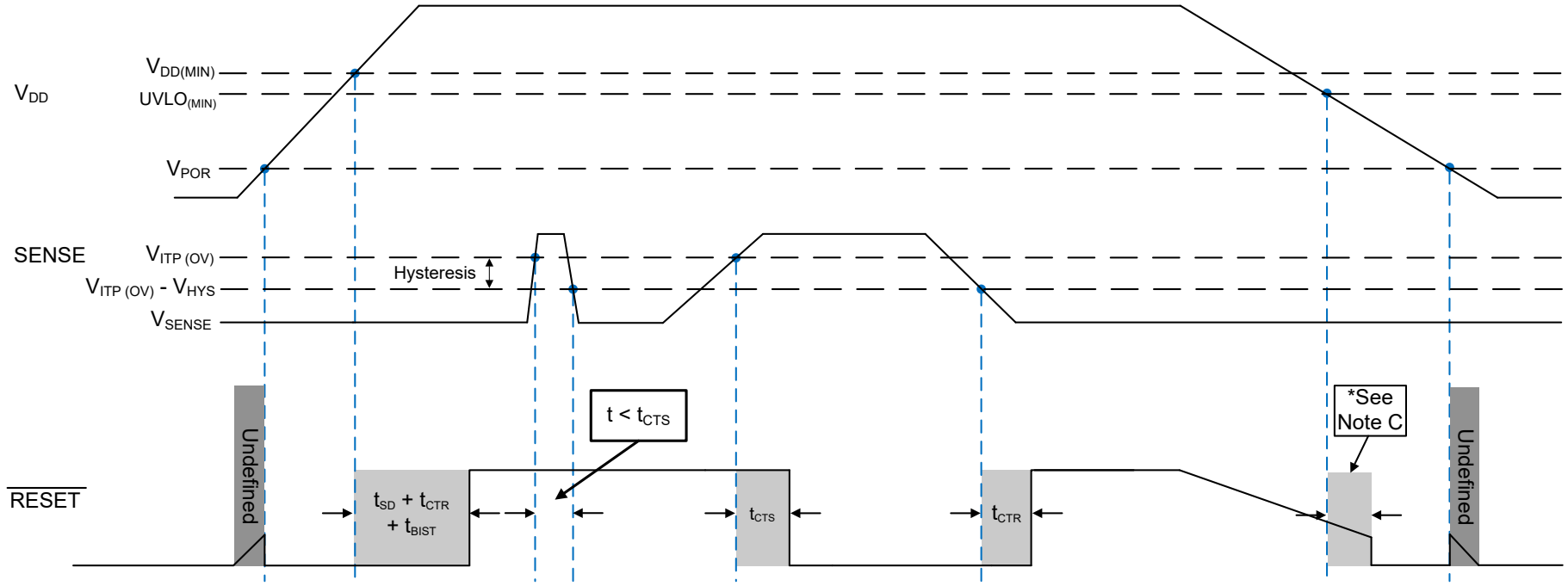
A. The timing diagram assumes the open-drain output $\overline{\text{RESET}}$ pin is connected via an external pull-up resistor to V_{DD}.

B. Be advised that 図 7-1 shows the V_{DD} falling slew rate is slow or the V_{DD} decay time is much larger than the propagation detect delay (t_{CTR}) time.

C. $\overline{\text{RESET}}$ is asserted when V_{DD} goes below the $UVLO_{(MIN)}$ threshold after the time delay, t_{CTR}, is reached.

図 7-1. SENSE Undervoltage (UV) Timing Diagram

ADVANCE INFORMATION



A. The timing diagram assumes the open-drain output $\overline{\text{RESET}}$ pin is connected via an external pull-up resistor to V_{DD}.

B. Be advised that 図 7-2 shows the V_{DD} falling slew rate is slow or the V_{DD} decay time is much larger than the propagation detect delay (t_{CTR}) time.

C. $\overline{\text{RESET}}$ is asserted when V_{DD} goes below the $UVLO_{(MIN)}$ threshold after the time delay, t_{CTR}, is reached.

図 7-2. SENSE Overvoltage (OV) Timing Diagram

ADVANCE INFORMATION

7.3 Typical Characteristics

Typical characteristics show the typical performance of the TPS3762-Q1 device. Test conditions are taken at T_A = 25°C, unless otherwise noted.

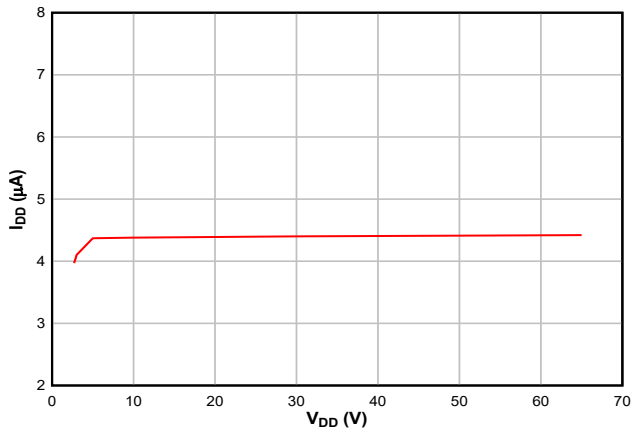


図 7-3. I_{DD} vs V_{DD} ($\overline{RESET}$ = Low, V_{IT} = 0.8 V)

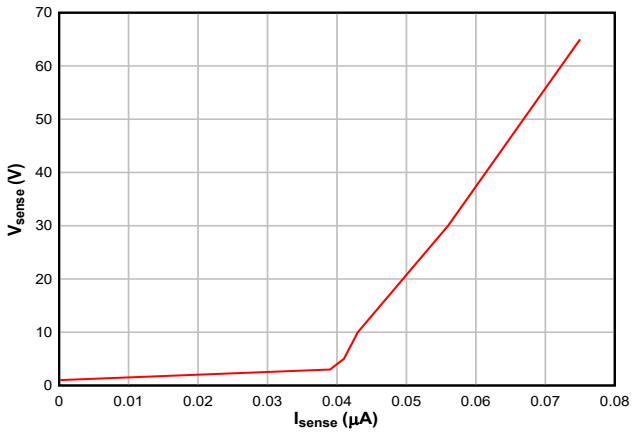


図 7-4. V_{SENSE} vs I_{SENSE} (V_{DD} = 2.7 V)

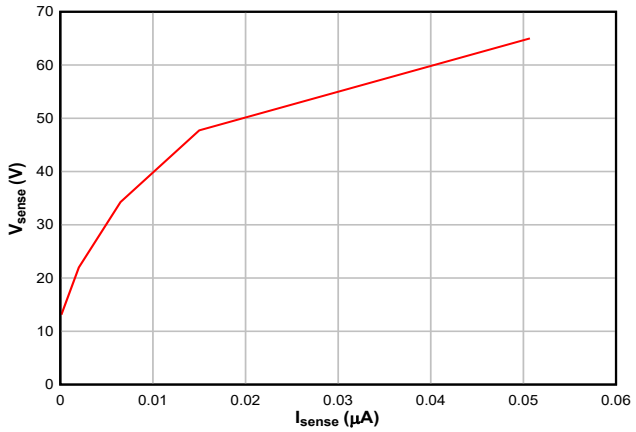


図 7-5. V_{SENSE} vs I_{SENSE} (V_{DD} = 65 V)

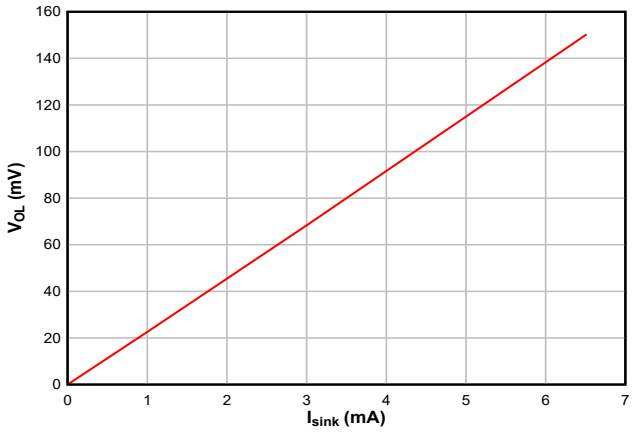


図 7-6. Open-Drain Active Low V_{OL} vs I_{RESET} (V_{DD} = 2.7 V)

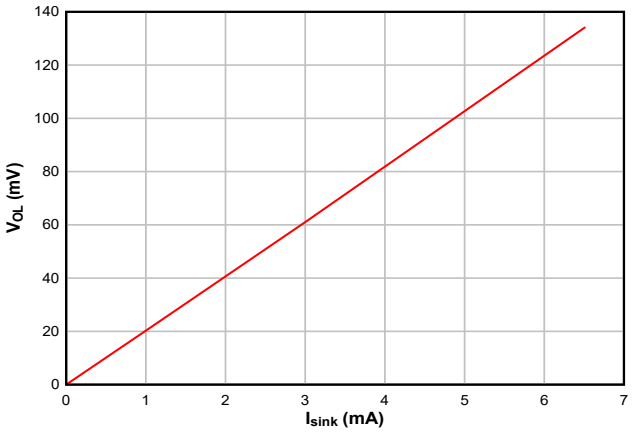


図 7-7. Open-Drain Active Low V_{OL} vs I_{RESET} (V_{DD} = 65 V)

ADVANCE INFORMATION

8 Detailed Description

8.1 Overview

The TPS3762-Q1 is a family of high voltage and low quiescent current voltage supervisors with fixed and adjustable threshold voltage options, Built-in Self-Test, and ASIL-D certification targeted. A voltage divider is integrated to eliminate the need for either inaccurate or expensive external resistor dividers and provide lower system leakage current. However, TPS3762-Q1 can also support an external resistor if required by the application. The lowest threshold 800 mV (bypass internal resistor ladder) is recommenced for external resistors use case to take advantage of faster detection time and lower I_{SENSE} current.

VDD, SENSE and $\overline{\text{RESET}}$ pins can support 65 V continuous operation. SENSE has -65 V reverse polarity protection. Both VDD and SENSE voltage levels can be independent of each other, meaning VDD pin can be connected at 2.7 V while the SENSE pin is connected to a higher voltage. TPS3762-Q1 includes a reset output latching feature that holds to output active to help system achieve safe state. Fixed and programmable sense and reset delay are available to avoid false resets and false reset releases. Note, the TPS3762-Q1 does not have clamps within the device so external circuits or devices must be added to limit the voltages outside the absolute maximum limit.

8.2 Functional Block Diagram

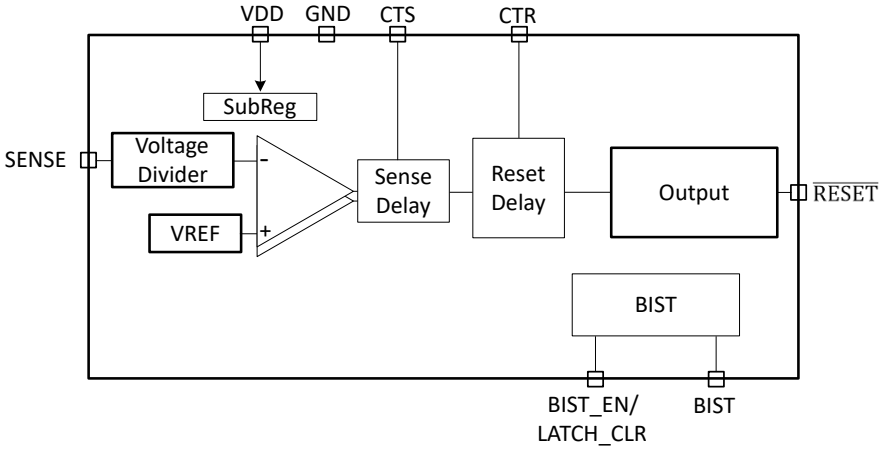


図 8-1. Functional Block Diagram [1]

ADVANCE INFORMATION

[1] Refer to セクション 5 for complete list of topologies and output logic combination

8.3 Feature Description

8.3.1 Input Voltage (VDD)

VDD operating voltage ranges from 2.7 V to 65 V. An input supply capacitor is not required for this device; however, if the input supply is noisy good analog practice is to place a 0.1 µF capacitor between the VDD and GND.

VDD needs to be at or above $V_{DD(MIN)}$ for at least the start-up time delay (t_{SD}) for the device to be fully functional.

VDD voltage is independent of V_{SENSE} and V_{RESET}, meaning that VDD can be higher or lower than the other pins.

8.3.1.1 Undervoltage Lockout (V_{POR} < V_{DD} < UVLO)

When the voltage on V_{DD} is less than the UVLO voltage, but greater than the power-on reset voltage (V_{POR}), the $\overline{\text{RESET}}$ and BIST pins will be asserted, regardless of the voltage at SENSE pins.

8.3.1.2 Power-On Reset (V_{DD} < V_{POR})

When the voltage on VDD is lower than the power on reset voltage (V_{POR}), the output signal is undefined and is not to be relied upon for proper device function.

Note: 図 8-2 and 図 8-3 assume an external pull-up resistor is connected to the $\overline{\text{RESET}}$ pin to VDD.

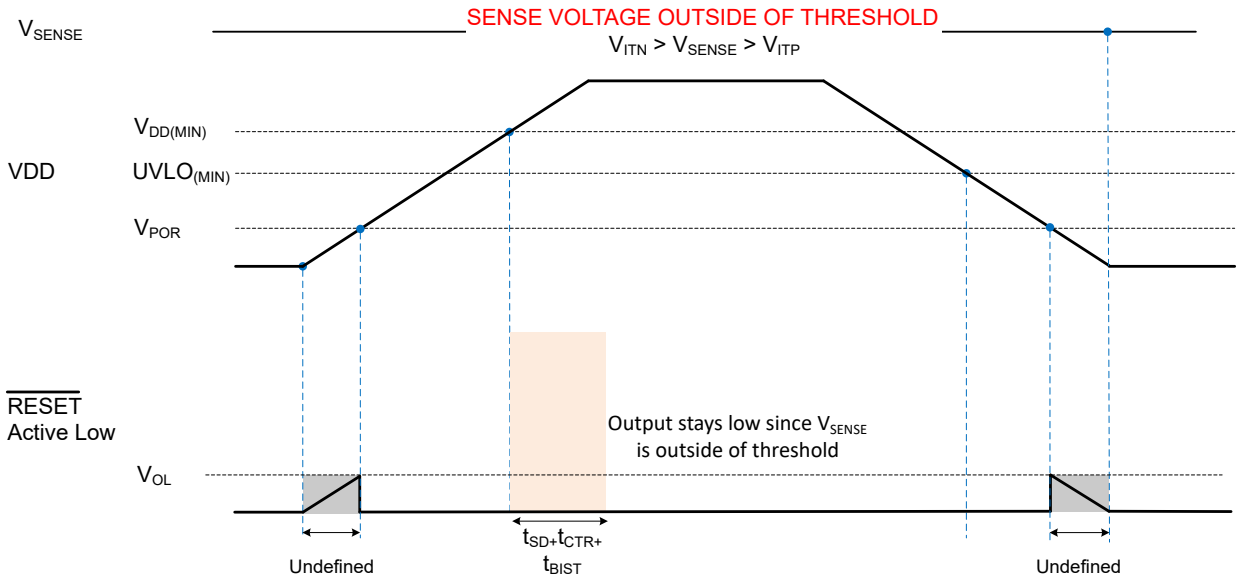


図 8-2. Power Cycle (SENSE Outside of Nominal Window Threshold)

ADVANCE INFORMATION

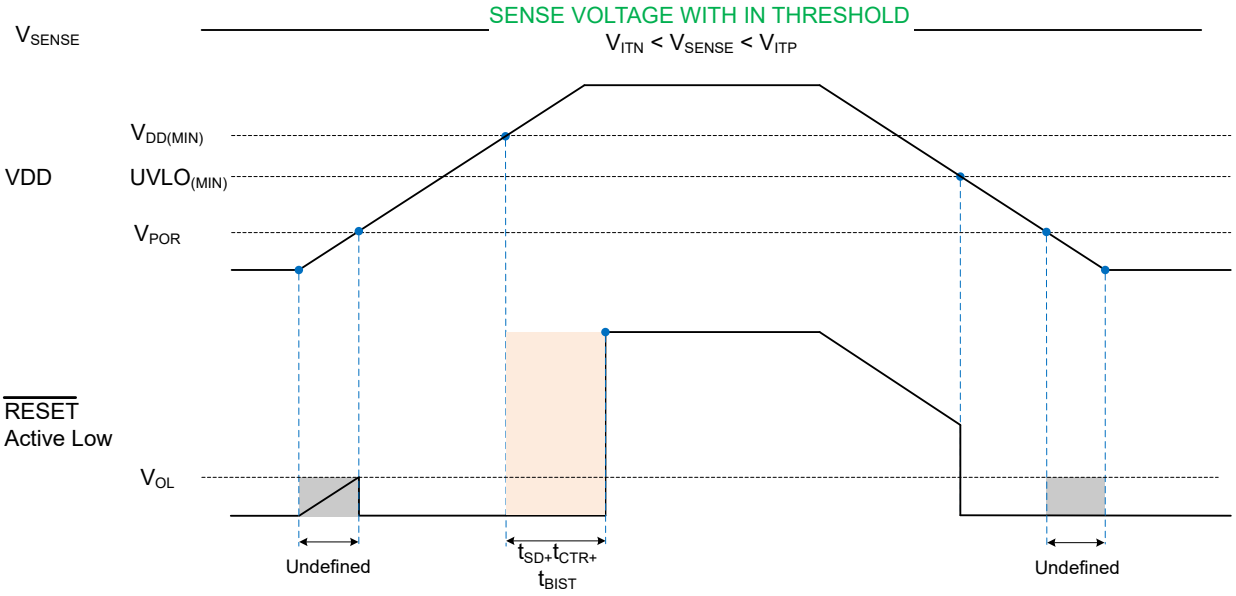


図 8-3. Power Cycle (SENSE Within Nominal Window Threshold)

ADVANCE INFORMATION

8.3.2 SENSE

The SENSE pin connects to the supply rail that is to be monitored. The sense pin on each device is configured to monitor either overvoltage (OV), undervoltage (UV), or window (OV&UV) conditions. TPS3762-Q1 device offers built-in hysteresis that provides noise immunity and maintains stable operation.

Although not required in most cases, for noisy applications good analog design practice is to place a 10 nF to 100 nF bypass capacitor at the SENSE inputs to reduce sensitivity to transient voltages on the monitored signal. SENSE can be connected directly to VDD pin.

8.3.2.1 SENSE Hysteresis

TPS3762-Q1 device offers built-in hysteresis around the UV and OV thresholds to avoid erroneous $\overline{\text{RESET}}$ de-assert. The hysteresis is opposite to the threshold voltage; for overvoltage options the hysteresis is subtracted from the positive threshold (V_{ITP}), for undervoltage options hysteresis is added to the negative threshold (V_{ITN}).

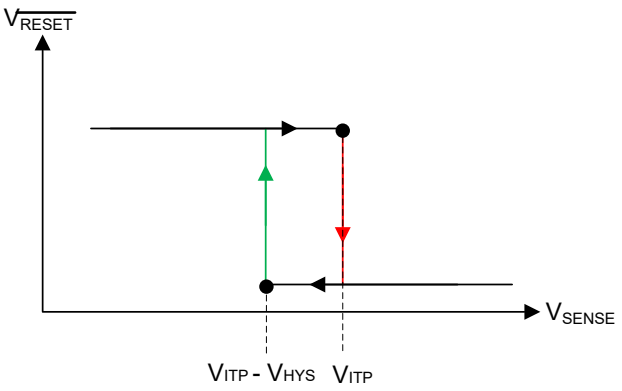


図 8-4. Hysteresis (Overvoltage Active-Low)

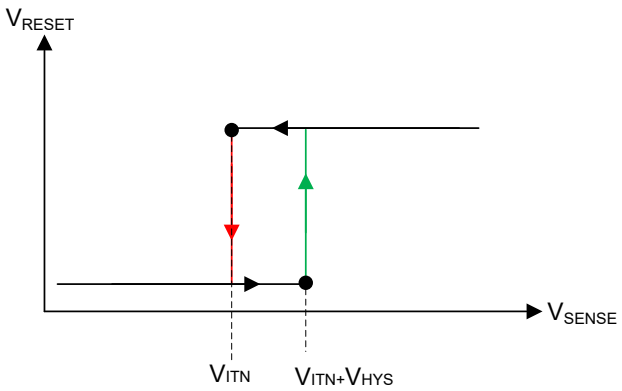


図 8-5. Hysteresis (Undervoltage Active-Low)

ADVANCE INFORMATION

表 8-1. Common Adjustable Hysteresis Lookup Table

TARGET			DEVICE ACTUAL HYSTERESIS OPTION
ADJUSTABLE THRESHOLD	TOPOLOGY	RELEASE VOLTAGE (V)	
800 mV	Overvoltage	784 mV	-2%
800 mV	Overvoltage	760 mV	-5%
800 mV	Overvoltage	720 mV	-10%
800 mV	Undervoltage	816 mV	2%
800 mV	Undervoltage	840 mV	5%
800 mV	Undervoltage	880 mV	10%

表 8-1 shows a sample of hysteresis for the 800 mV adjustable variant for the TPS3762-Q1.

Knowing the amount of hysteresis voltage, the release voltage for the undervoltage (UV) channel is ($V_{ITN\ (UV)}$ + V_{HYS}) and for the overvoltage (OV) channel is ($V_{ITP\ (OV)}$ - V_{HYS}).

Undervoltage (UV) Channel

V_{ITN} = 800 mV

Voltage Hysteresis (V_{HYS}) = 2% = 16 mV

Hysteresis Accuracy = +1.5% to +2.5% = 16.24 mV to 16.4 mV

Release Voltage = V_{ITN} + V_{HYS} = 816.24 mV to 816.4 mV

Overvoltage (OV) Channel

V_{ITP} = 800 mV

Voltage Hysteresis (V_{HYS}) = 2% = 16 mV

Hysteresis Accuracy = +1.5% to +2.5% = 16.24 mV to 16.4 mV

Release Voltage = V_{ITP} - V_{HYS} = 783.6 mV to 783.76 mV

ADVANCE INFORMATION

8.3.3 Output Logic Configurations

TPS3762-Q1 is a single channel device that has a single input sense pin and a single reset pin. The single reset is available with open drain topology.

8.3.3.1 Open-Drain

Open-drain output requires an external pull-up resistor to hold the voltage high to the required voltage logic. Connect the pull-up resistor to the proper voltage rail to enable the output to be connected to other devices at the correct interface voltage levels.

To select the right pull-up resistor consider system V_{OH} and the Open-Drain Leakage Current (I_{lkg}) provided in the electrical characteristics, high resistors values have a higher voltage drop affecting the output voltage high. The open-drain output can be connected as a wired-AND logic with other open-drain signals such as another TPS3762-Q1 open-drain output pin.

8.3.3.2 Active-Low ($\overline{RESET}$)

$\overline{RESET}$ (active low) denoted with a bar above the pin label. $\overline{RESET}$ remains high voltage (V_{OH}, deasserted) (open-drain variant V_{OH} is measured against the pullup voltage) as long as sense voltage is in normal operation within the threshold boundaries and VDD voltage is above UVLO. To assert a reset sense pins needs to meet the condition below:

- For undervoltage variant the SENSE voltage need to cross the lower boundary (V_{ITN}).
- For overvoltage variant the SENSE voltage needs to cross the upper boundary (V_{ITP}).

8.3.3.3 Latching

The TPS3762-Q1 comes with the optional output reset latching feature for the window (OV & UV) and OV variants, check the セクション 5 to verify variant specific latch functionality. When using the window variant, whenever a fault, OV or UV, occurs $\overline{RESET}$ goes low and remains low until cleared by a rising edge transition on the BIST_EN / LATCH_CLR pin. When using the OV variant, whenever a OV fault occurs $\overline{RESET}$ goes low and remains low until cleared by a logic input high greater than $V_{BIST\_EN/LATCH\_CLR}$ on the BIST_EN / LATCH_CLR pin. See セクション 8.3.6 for more details.

ADVANCE INFORMATION

8.3.4 User-Programmable Reset Time Delay

TPS3762-Q1 has adjustable reset release time delay with external capacitors.

- A capacitor on CTR programs the reset time delay of the output.
- No capacitor on this pin gives the fastest reset delay time indicated by t_{CTR} in セクション 7.1.6.
- Variants such as TPS3762Q use a fixed internal time delay. check the セクション 5 to verify variant specific timing.

8.3.4.1 Reset Time Delay Configuration

The time delay (t_{CTR}) can be programmed by connecting a capacitor between CTR pin and GND.

The relationship between external capacitor $C_{CTR\_EXT\ (typ)}$ and the time delay $t_{CTR\ (typ)}$ is given by 式 1.

$$t_{CTR\ (typ)} = R_{CTR\ (typ)} \times C_{CTR\_EXT\ (typ)} + t_{CTR\ (no\ cap)} \quad (1)$$

$R_{CTR\ (typ)}$ = is in kilo ohms (kΩ)

$C_{CTR\_EXT\ (typ)}$ = is given in microfarads (µF)

$t_{CTR\ (typ)}$ = is the reset time delay (ms)

The reset delay varies according to three variables: the external capacitor (C_{CTR_EXT}), CTR pin internal resistance (R_{CTR}) provided in セクション 7, and a constant. The minimum and maximum variance due to the constant is show in 式 2 and 式 3:

$$t_{CTR\ (min)} = R_{CTR\ (min)} \times C_{CTR\_EXT\ (min)} + t_{CTR\ (no\ cap\ (min))} \quad (2)$$

$$t_{CTR\ (max)} = R_{CTR\ (max)} \times C_{CTR\_EXT\ (max)} + t_{CTR\ (no\ cap\ (max))} \quad (3)$$

There is no limit to the capacitor on CTR pin. Having a too large of a capacitor value can cause very slow charge up (rise times) due to capacitor leakage and system noise can cause the internal circuit to hold $\overline{\text{RESET}}$ active.

ADVANCE INFORMATION

8.3.5 User-Programmable Sense Delay

TPS3762-Q1 has adjustable sense release time delay with external capacitors.

- A capacitor in CTS programs the excursion detection on SENSE.
- No capacitor on this pin gives the fastest sense delay time indicated by t_{CTS} in セクション 7.1.6.
- The TPS3762-Q1 comes with an optional fixed internal time delay that ignoes the capacitor value at the CTS pin, check the セクション 5 to verify variant specific functionality.

8.3.5.1 Sense Time Delay Configuration

The time delay (t_{CTS}) can be programmed by connecting a capacitor between CTS pin and GND.

The relationship between external capacitor $C_{CTS\_EXT\ (typ)}$ and the time delay $t_{CTS\ (typ)}$ is given by 式 4.

$$t_{CTS\ (typ)} = R_{CTS\ (typ)} \times C_{CTS\_EXT\ (typ)} + t_{CTS\ (no\ cap)} \quad (4)$$

R_{CTS} = is in kilo ohms (kΩ)

C_{CTS_EXT} = is given in microfarads (µF)

t_{CTS} = is the sense time delay (ms)

The sense delay varies according to three variables: the external capacitor (C_{CTS_EXT}), CTS pin internal resistance (R_{CTS}) provided in Electrical Characteristics, and a constant. The minimum and maximum variance due to the constant is show in 式 5 and 式 6:

$$t_{CTS\ (min)} = R_{CTS\ (min)} \times C_{CTS\_EXT\ (min)} + t_{CTS\ (no\ cap\ (min))} \quad (5)$$

$$t_{CTR\ (max)} = R_{CTS\ (max)} \times C_{CTS\_EXT\ (max)} + t_{CTSx\ (no\ cap\ (max))} \quad (6)$$

The recommended maximum sense delay capacitor for the TPS3762-Q1 is limited to 10 µF as this makes sure enough time for the capacitor to fully discharge when a voltage fault occurs. Also, having a too large of a capacitor value can cause very slow charge up (rise times) and system noise can cause the internal circuit to trip earlier or later near the threshold. This leads to variation in time delay where it can make the delay accuracy worse in the presence of system noise.

8.3.6 Built-In Self-Test

The TPS3762-Q1 has a Built-In Self-Test (BIST) feature that runs diagnostics internally in the device. BIST is initiated automatically after crossing $V_{DD(min)}$. During power-up, the BIST test asserts and holds $\overline{RESET}$ and BIST low until the BIST test completes successfully. The length of the BIST is specified by t_{BIST}. If BIST is not successful due to the internal blocks not working properly, the $\overline{RESET}$ and BIST are held low signifying a fault internal to the device. See 図 8-6 for more details.

ADVANCE INFORMATION

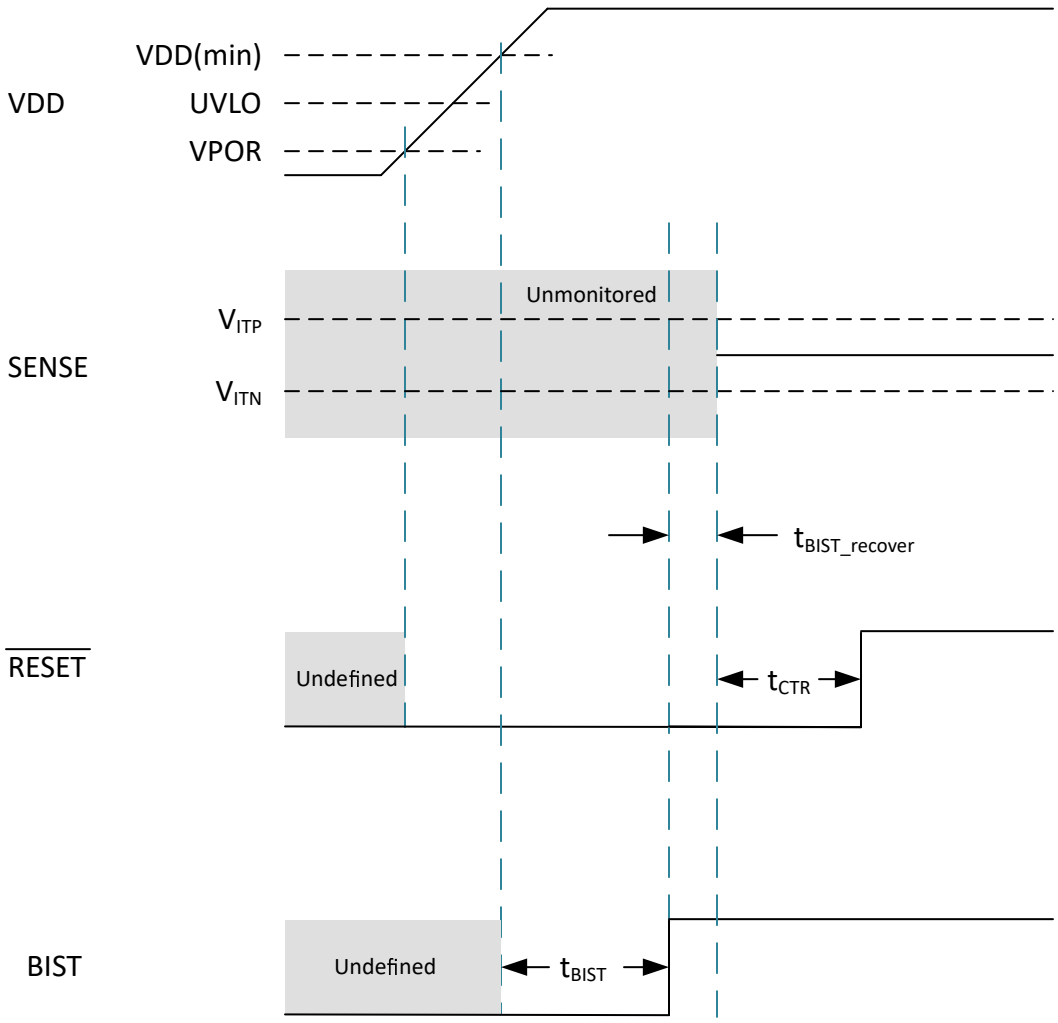


図 8-6. TPS3762-Q1 Start-Up Sequence

After a successful power-up sequence, BIST can be initiated any time with a positive edge transition on the BIST_EN pin or BIST_EN/LATCH_CLR pin. BIST only initiates if the SENSE pin is not in a overvoltage or undervoltage fault mode. During this BIST test time period, t_{BIST}, BIST pin asserts low to signify that BIST has started and $\overline{\text{RESET}}$ assertion is dependent on the device variant. Upon successful BIST the BIST pin and $\overline{\text{RESET}}$ pin is deasserted. If BIST is not successful due to the internal device not working properly, the $\overline{\text{RESET}}$ pin and BIST pin is asserted low signifying a fault internal to the device. See 図 8-7 and 図 8-8 for more details.

ADVANCE INFORMATION

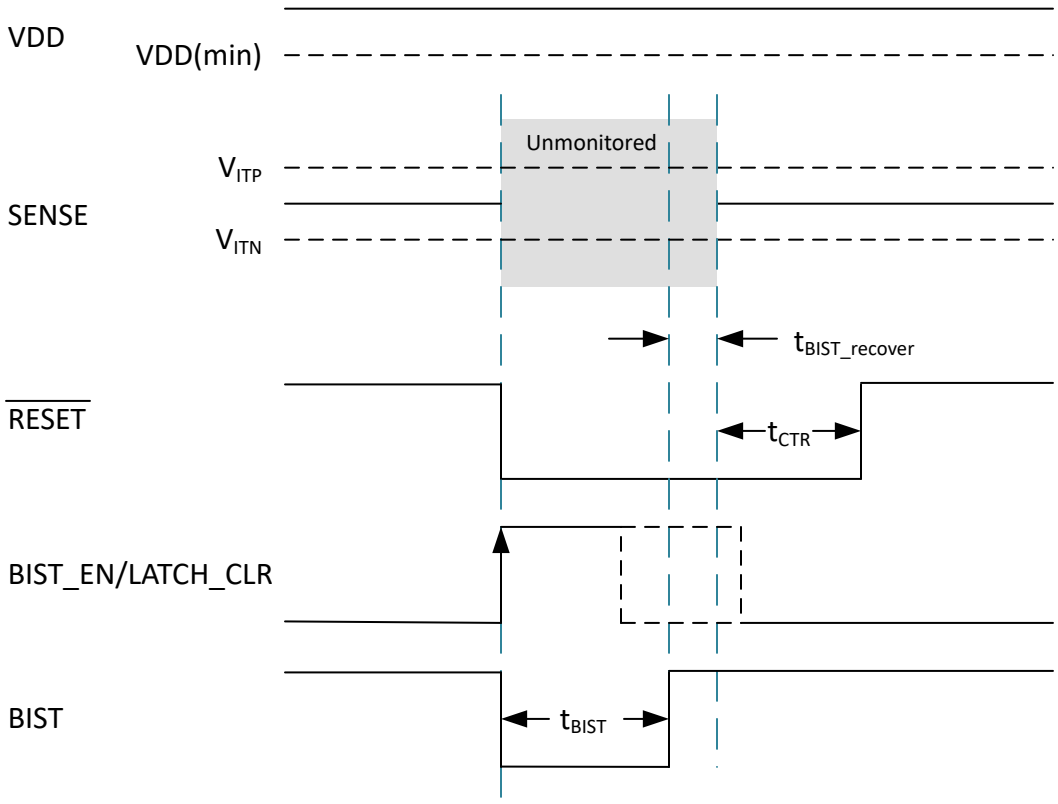


図 8-7. BIST With $\overline{RESET}$ Assertion

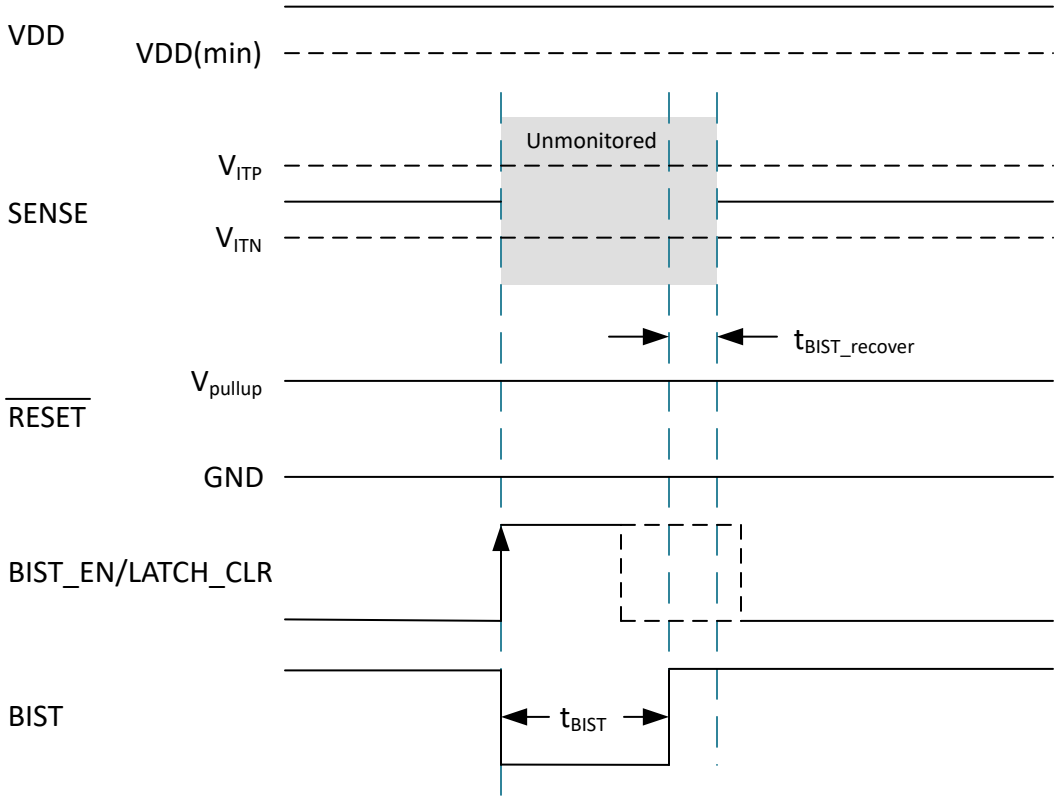


図 8-8. BIST With No $\overline{RESET}$ Assertion

BIST checks for internal faults in the device. During BIST the device is not monitoring the SENSE pin for faults and the $\overline{\text{RESET}}$ pin is not dependent on the SENSE pin voltage. The BIST sequence tests the internal signal chain of the device by checking for faults on the internal comparators on the SENSE pin, the internal digital logic, and the $\overline{\text{RESET}}$ output. See 図 8-9 and 図 8-10 for more details.

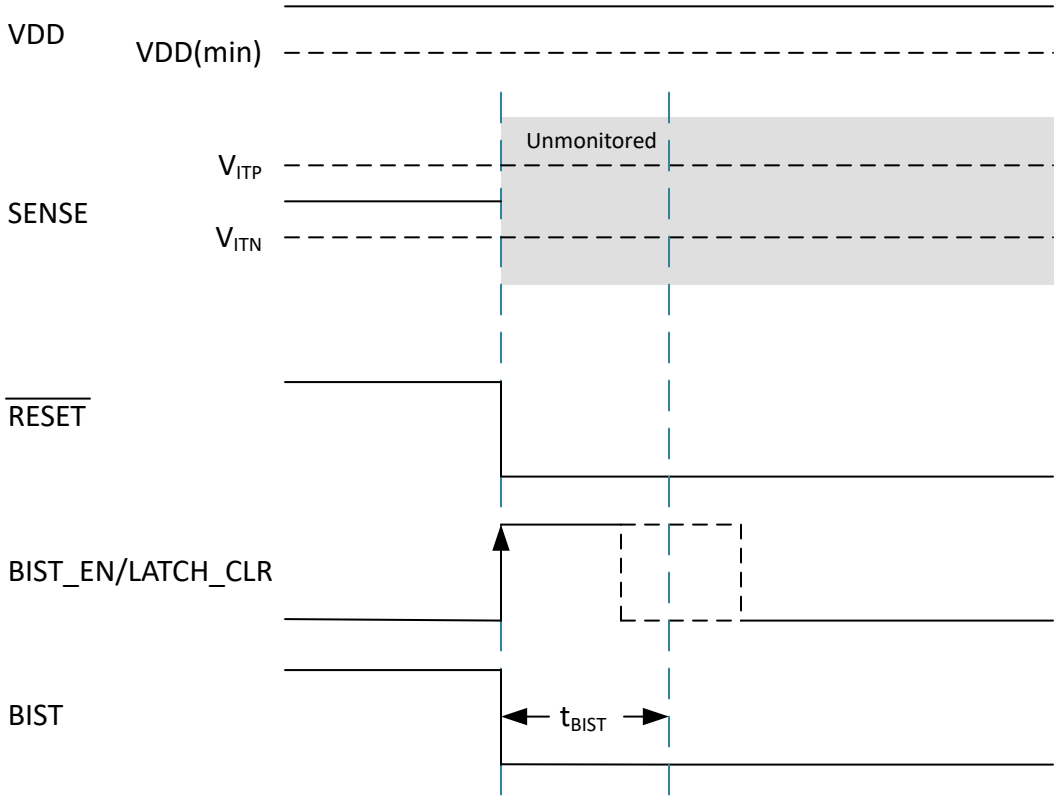


図 8-9. BIST Fail With $\overline{\text{RESET}}$ Assertion

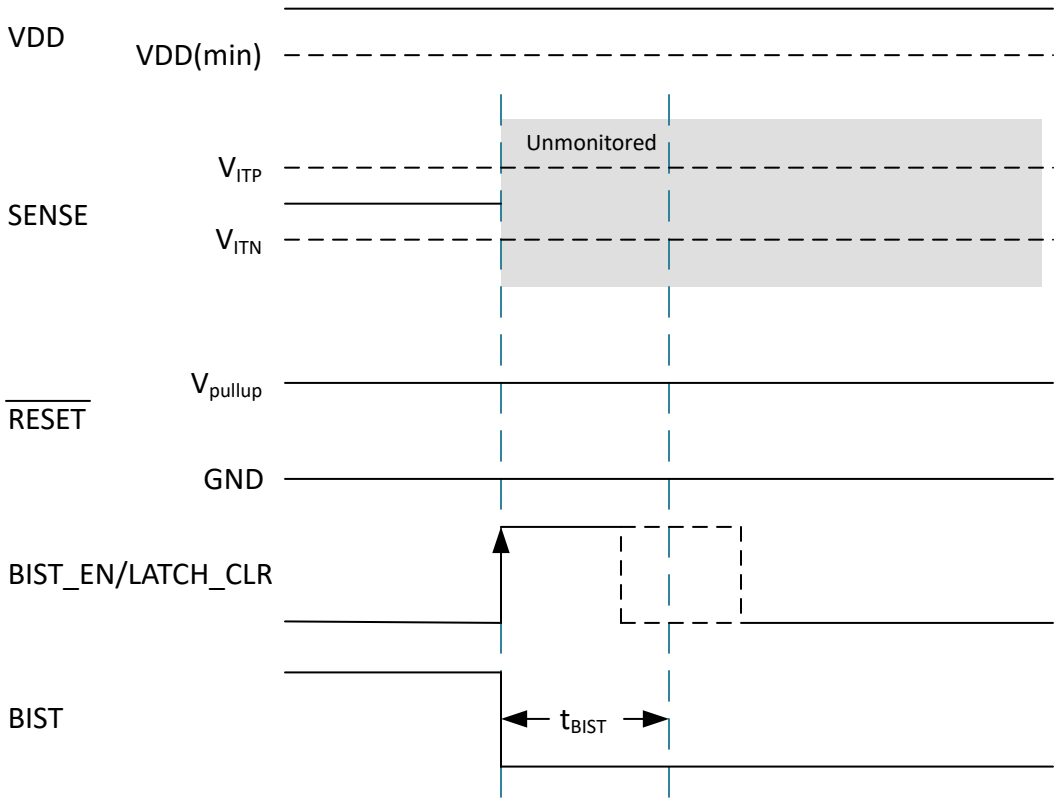


図 8-10. BIST Fail With No $\overline{RESET}$ Assertion

ADVANCE INFORMATION

9 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The following sections describe in detail proper device implementation, depending on the final application requirements.

9.2 Adjustable Voltage Thresholds

式 7 illustrates an example of how to adjust the voltage threshold with external resistor dividers. The resistors can be calculated depending on the desired voltage threshold and device part number. TI recommends using the 0.8 V voltage threshold device when using an adjustable voltage variant. This variant bypasses the internal resistor ladder.

For example, consider a 12 V rail being monitored V_{MON} for overvoltage (OV) using of the TPS3762D02OVDDFRQ1 variant. As shown in 図 9-1, R_1 is the top resistor of the resistor divider that is between V_{MON} and V_{SENSE}, R_2 is the bottom resistor that is between V_{SENSE} and GND, V_{MON} is the voltage rail that is being monitored and V_{SENSE} is the input to the sense pin. The monitored O V threshold, denoted as V_{MON+}, where the device asserts a reset signal occurs when $V_{SENSE} = V_{ITP}$, for this example, V_{MON+} = 35 V. Using 式 7 and assuming R_2 = 10 kΩ , R_1 can be calculated shown in 式 8 where I_{R1} is represented in 式 9:

$$V_{ITP} = V_{MON+} \times (R_2 \div (R_1 + R_2)) \quad (7)$$

$$R_1 = (V_{MON+} - V_{ITP}) \div I_{R1} \quad (8)$$

$$I_{R1} = I_{R2} = V_{ITP} \div R_2 \quad (9)$$

Substituting 式 9 into 式 8 and solving for R_1 we get, R_1 = 427.5kΩ. The TPS3762D02OVDDFRQ1 is typically meant to monitor a 0.8 V rail with variant specific 2 %, 5 %, or 10 % voltage threshold hysteresis. For the reset signal to become deasserted, V_{MON} needs to go below $V_{ITP} - V_{HYS}$. For this example, we assume a 10 % voltage threshold hysteresis was selected. Therefore, V_{MON} = 31.5 V when the reset signal becomes deasserted.

There are inaccuracies that must be taken into consideration while adjusting voltage thresholds. Aside from the tolerance of the resistor divider, there is an internal resistance of the SENSE pin that can affect the accuracy of the resistor divider. Although expected to be very high impedance, users are recommended to calculate the values for the design specifications. The internal SENSE resistance R_{SENSE} can be calculated by the SENSE voltage V_{SENSE} divided by the SENSE current I_{SENSE} as shown in 式 11. V_{SENSE} can be calculated using 式 7 depending on the resistor divider and monitored voltage. I_{SENSE} can be calculated using 式 10.

$$I_{SENSE} = [(V_{MON} - V_{SENSE}) \div R_1] - (V_{SENSE} \div R_2) \quad (10)$$

$$R_{SENSE} = V_{SENSE} \div I_{SENSE} \quad (11)$$

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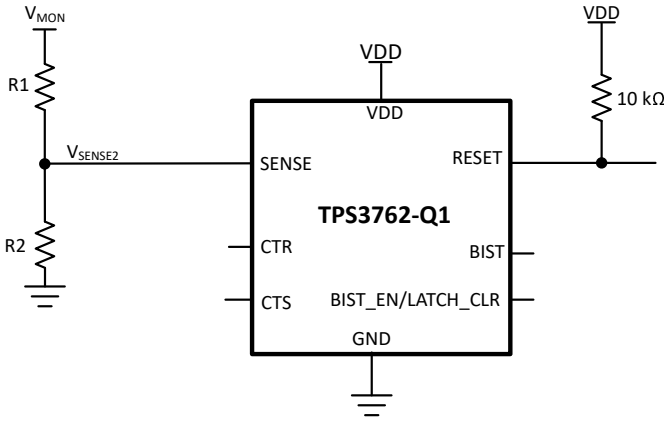

図 9-1. Adjustable Voltage Threshold with External Resistor Dividers

9.3 Typical Application

9.3.1 Design 1: Off-Battery Monitoring

This application is intended for the initial power stage in applications with the 12 V batteries. The TPS3762-Q1 utilizes high-voltage SENSE and V_{DD} inputs to monitor an automotive battery without needing external resistors. This keeps the overall system I_Q of the design low while still achieving the desired rail monitoring.

図 9-6 illustrates an example of how the TPS3762 Q1 is monitoring the battery voltage while being powered by it, as well.

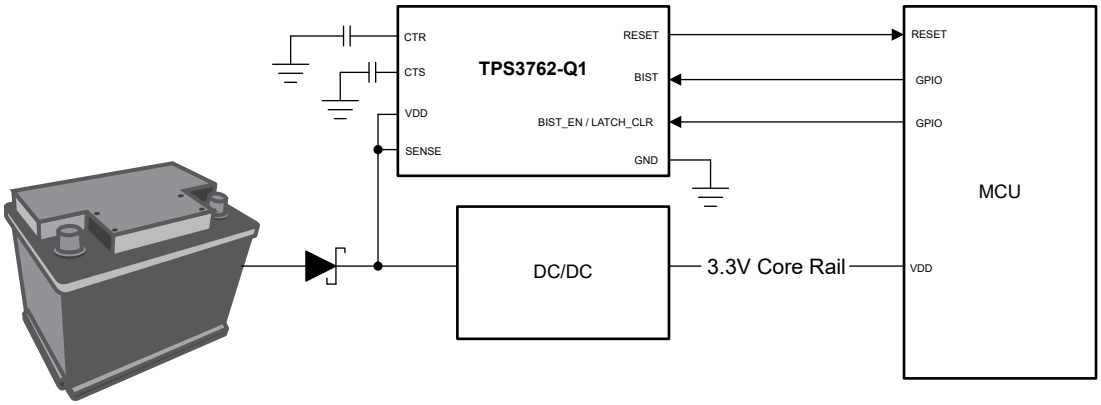

図 9-2. Off-Battery Monitoring

9.3.1.1 Design Requirements

表 9-1. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Voltage Threshold	Typical O V voltage threshold 30 V. Typical UV voltage threshold 7 V.	Typical O V voltage threshold 30 V. Typical UV voltage threshold 7 V.
Maximum Input Power	Operate with power supply input up to 42 V	The TPS3762-Q1 can support a V_{DD} of up to 65 V.
Output Logic	Open-Drain	Open-Drain
SENSE Delay	119 ms	119 ms
$\overline{\text{RESET}}$ Delay	360 ms	360 ms
Maximum Device Current Consumption	10 µA	4 µA typical, 8.1 µA maximum

9.3.1.2 Detailed Design Procedure

The TPS3762-Q1 utilizes high-voltage SENSE and V_{DD} inputs to monitor an automotive battery without needing external resistors. This keeps the overall system I_Q of the design low while still achieving the desired rail monitoring.

9.3.1.2.1 Setting Voltage Threshold

The voltage rail monitoring is done by connecting the SENSE input directly to the battery rail without the need for external resistor dividers. The threshold voltage is set by the device variant. Threshold voltage decoding can be found in 表 10-1. In this example, the nominal supply voltage from the battery is 12 V and the variation of the battery voltage is common between 9 V and 16 V. Setting a overvoltage threshold of 30 V and a undervoltage threshold of 7 V makes sure that the device resets before supply voltage violates the allowed boundary. For adjustable voltage variant devices see セクション 9.2.

9.3.1.2.2 Meeting the Sense and Reset Delay

The TPS3762-Q1 features two options for selecting sense and reset delays: fixed delays and capacitor-programmable delays. セクション 8.3.5 and セクション 8.3.4 show how to set the timings for the capacitor-programmable delays. The application requires a 119ms sense delay, thus a 0.033 µF capacitor is used. The application requires a 360 ms reset delay, thus a 0.1 µF capacitor is used.

9.3.1.2.3 Setting Supply Voltage

Setting the supply voltage is done by connecting the V_{DD} input directly to the battery rail without the need for external circuitry. This The device being able to handle 65 V on V_{DD} means the monitored voltage rail can handle any typical 42 V battery load dump. Good analog design practice recommends using a 0.1 µF capacitor on the V_{DD} pin.

ADVANCE INFORMATION

9.3.1.3 Application Curves

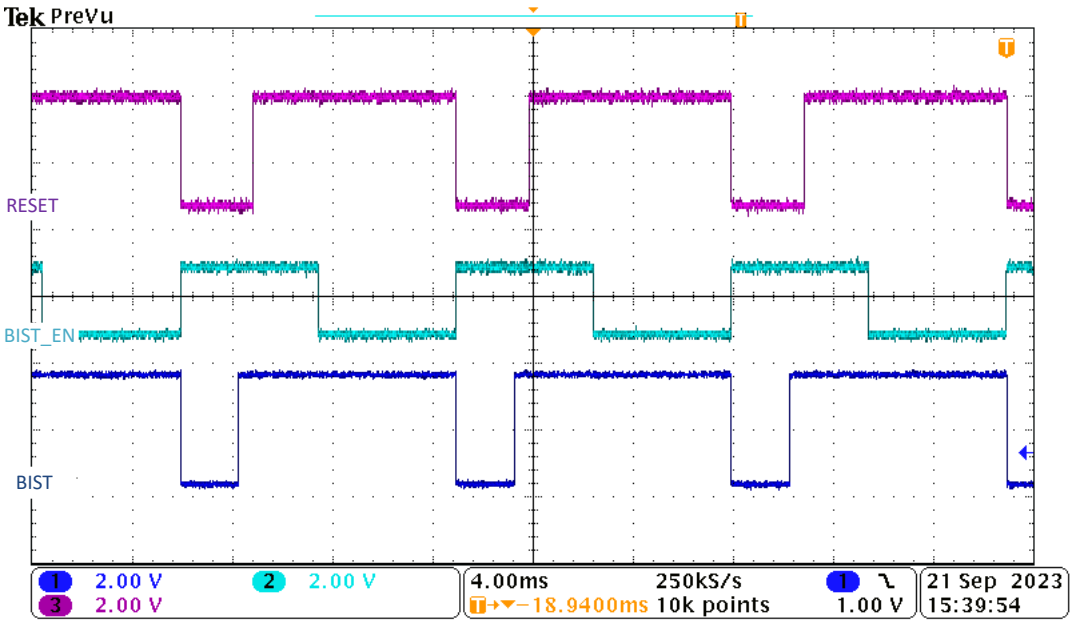

図 9-3. BIST with $\overline{\text{RESET}}$ Assertion Waveform

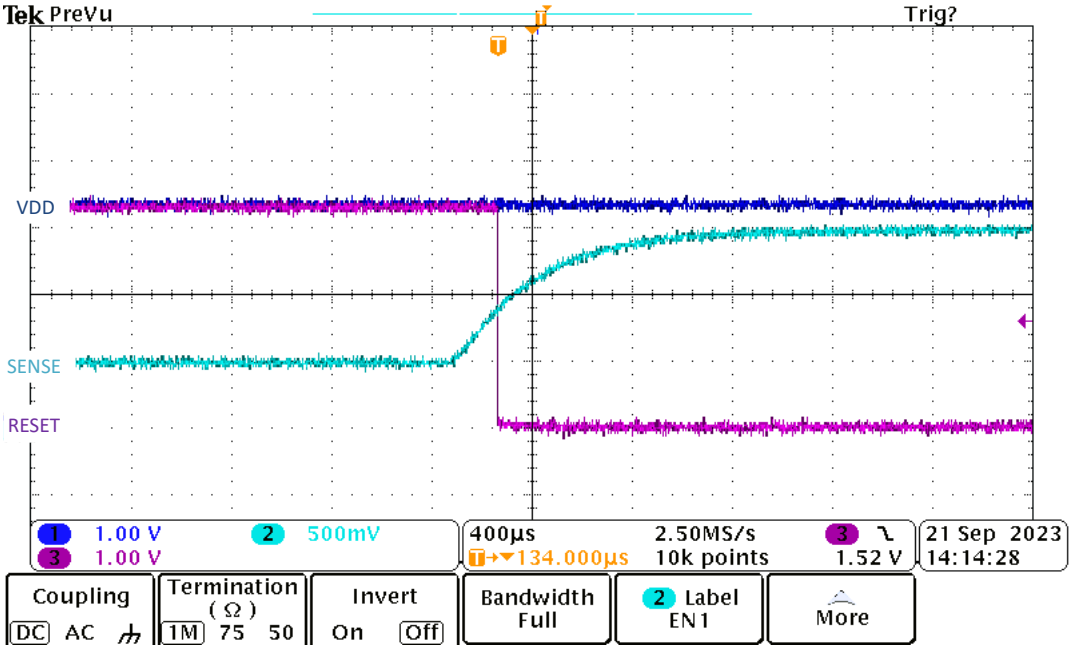

図 9-4. Overvoltage $\overline{\text{RESET}}$ Latching Waveform

ADVANCE INFORMATION

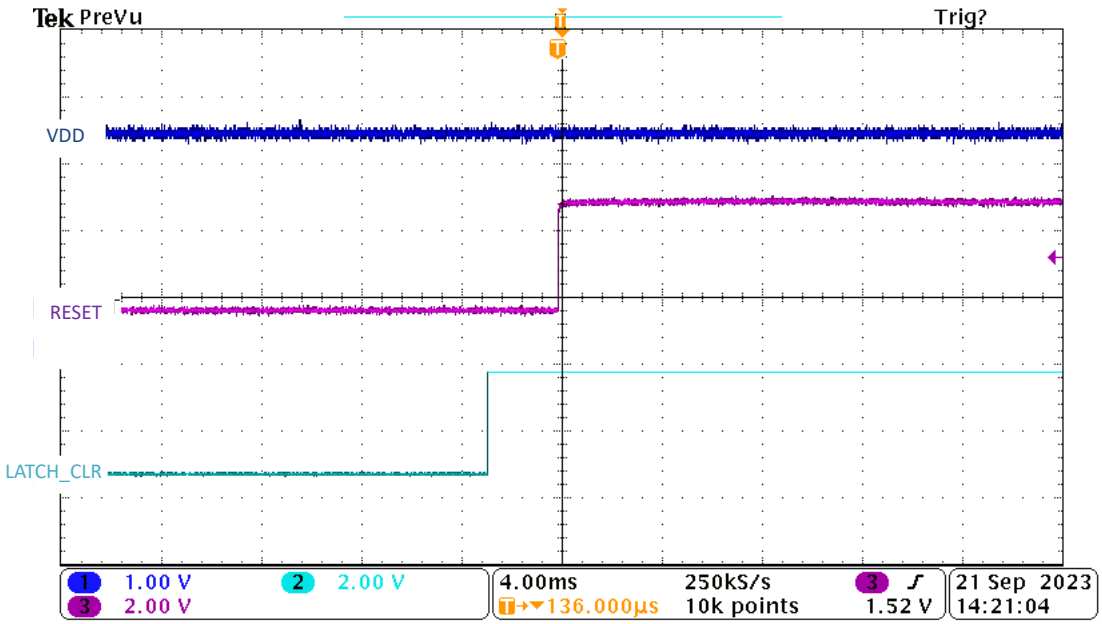

図 9-5. Overvoltage $\overline{\text{RESET}}$ Unlatching Waveform

9.4 Power Supply Recommendations

TPS3762-Q1 is designed to operate from an input supply with a V_{DD} voltage between 2.7 V (minimum operation) to 65 V (maximum operation). Good analog design practice recommends placing a minimum 0.1 µF ceramic capacitor as near as possible to the V_{DD} pin.

9.4.1 Power Dissipation and Device Operation

The permissible power dissipation for any package is a measure of the capability of the device to pass heat from the power source, the junctions of the IC, to the ultimate heat sink, the ambient environment. Thus, the power dissipation is dependent on the ambient temperature and the thermal resistance across the various interfaces between the die junction and ambient air.

The maximum continuous allowable power dissipation for the device in a given package can be calculated using 式 12:

$$P_{D\text{-}MAX} = ((T_{J\text{-}MAX} – T_A) / R_{\theta JA}) \quad (12)$$

The actual power being dissipated in the device can be represented by 式 13:

$$P_D = V_{DD} \times I_{DD} + p_{RESET} \quad (13)$$

p_{RESET} is calculated by 式 14 or 式 15

$$p_{RESET\ (PUSHPULL)} = V_{DD} - V_{RESET} \times I_{RESET} \quad (14)$$

$$p_{RESET\ (OPEN\text{-}DRAIN)} = V_{RESET} \times I_{RESET} \quad (15)$$

式 12 and 式 13 establish the relationship between the maximum power dissipation allowed due to thermal consideration, the voltage drop across the device, and the continuous current capability of the device. These two equations must be used to determine the optimum operating conditions for the device in the application.

In applications where lower power dissipation (P_D) and/or excellent package thermal resistance ($R_{\theta JA}$) is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) can be increased.

In applications where high power dissipation and/or poor package thermal resistance is present, the maximum ambient temperature ($T_{A\text{-}MAX}$) may have to be de-rated. $T_{A\text{-}MAX}$ is dependent on the maximum operating junction temperature ($T_{J\text{-}MAX\text{-}OP}$ = 125°C), the maximum allowable power dissipation in the device package in the application ($P_{D\text{-}MAX}$), and the junction-to ambient thermal resistance of the part/package in the application ($R_{\theta JA}$), as given by 式 16:

$$T_{A\text{-}MAX} = (T_{J\text{-}MAX\text{-}OP} – (R_{\theta JA} \times P_{D\text{-}MAX})) \quad (16)$$

9.5 Layout

9.5.1 Layout Guidelines

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a greater than 0.1 µF ceramic capacitor as near as possible to the VDD pin.
- To further improve the noise immunity on the SENSE pins, placing a 10 nF to 100 nF capacitor between the SENSE pin and GND can reduce the sensitivity to transient voltages on the monitored signal.
- If a capacitor is used on CTS or CTR, place these components as close as possible to the respective pins. If the capacitor adjustable pins are left unconnected, make sure to minimize the amount of parasitic capacitance on the pins to less than 5 pF.
- Place the pull-up resistors on $\overline{\text{RESET}}$ as close to the pin as possible.
- When laying out metal traces, separate high voltage traces from low voltage traces as much as possible. If high and low voltage traces need to run close by, spacing between traces should be greater than 20 mils (0.5 mm).

- Do not have high voltage metal pads or traces closer than 20 mils (0.5 mm) to the low voltage metal pads or traces.

9.5.2 Layout Example

The layout example in 図 9-6 shows how the TPS3762-Q1 is laid out on a printed circuit board (PCB) with user-defined delays.

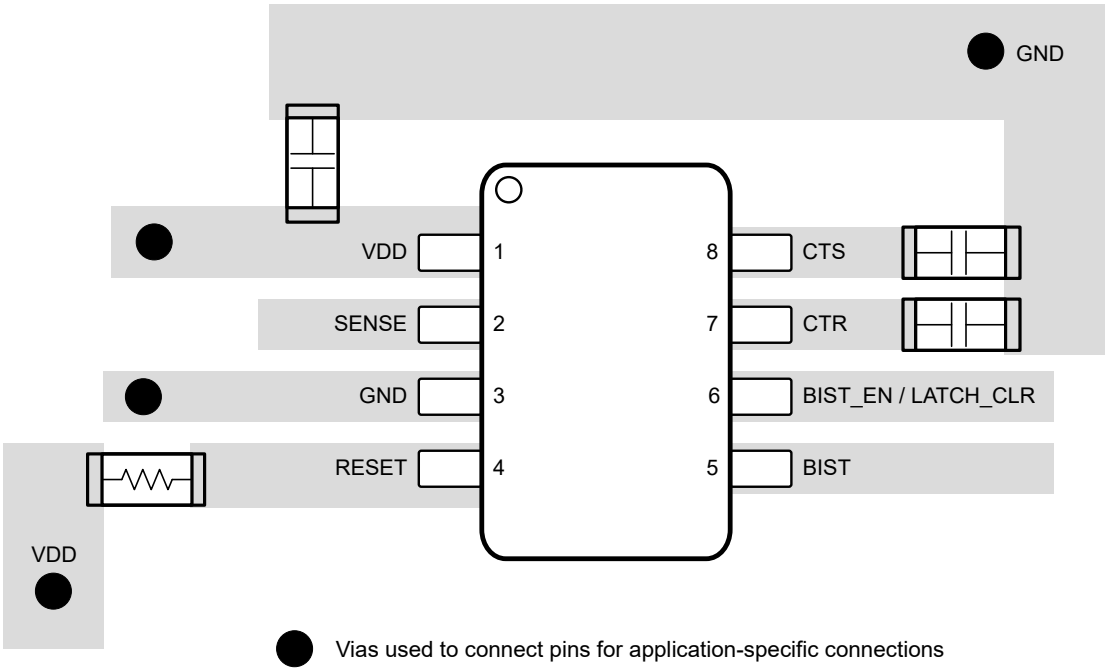

図 9-6. TPS3762-Q1 Recommended Layout

ADVANCE INFORMATION

9.5.3 Creepage Distance

Per IEC 60664 Creepage is the shortest distance between two conductive parts or as shown in 図 9-7 the distance between high voltage conductive parts and grounded parts, the floating conductive part is ignored and subtracted from the total distance.

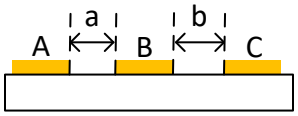

図 9-7. Creepage Distance

図 9-7 details

- A = Left pins (high voltage)
- B = Central pad (conductive not internally connected, can be left floating or connected to GND)
- C = Right pins (low voltages)
- Creepage distance = a + b

10 Device and Documentation Support

10.1 Device Nomenclature

Device Decoder in セクション 5 describe how to decode certain device function of the device based on its part number. Not all part numbers follow this nomenclature. Use 表 10-1 as the part number decoding table for all devices.

表 10-1. Device Configuration Table

ORDERABLE PART NAME	Overvoltage (V_{ITP})	Overvoltage Hysteresis	Undervoltage (V_{ITN})	Undervoltage Hysteresis	CTR / CTS	Latch / UVbypass	BIST RESET Trigger
PS3762D02OVDDFRQ1	800mV	2%	N/A	N/A	ADJ / ADJ	Both	Yes

10.2 ドキュメントの更新通知を受け取る方法

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10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

ADVANCE INFORMATION

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PS3762D02OVDDFRQ1	ACTIVE	SOT-23-THIN	DDF	8	3000	TBD	Call TI	Call TI	-40 to 125		Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

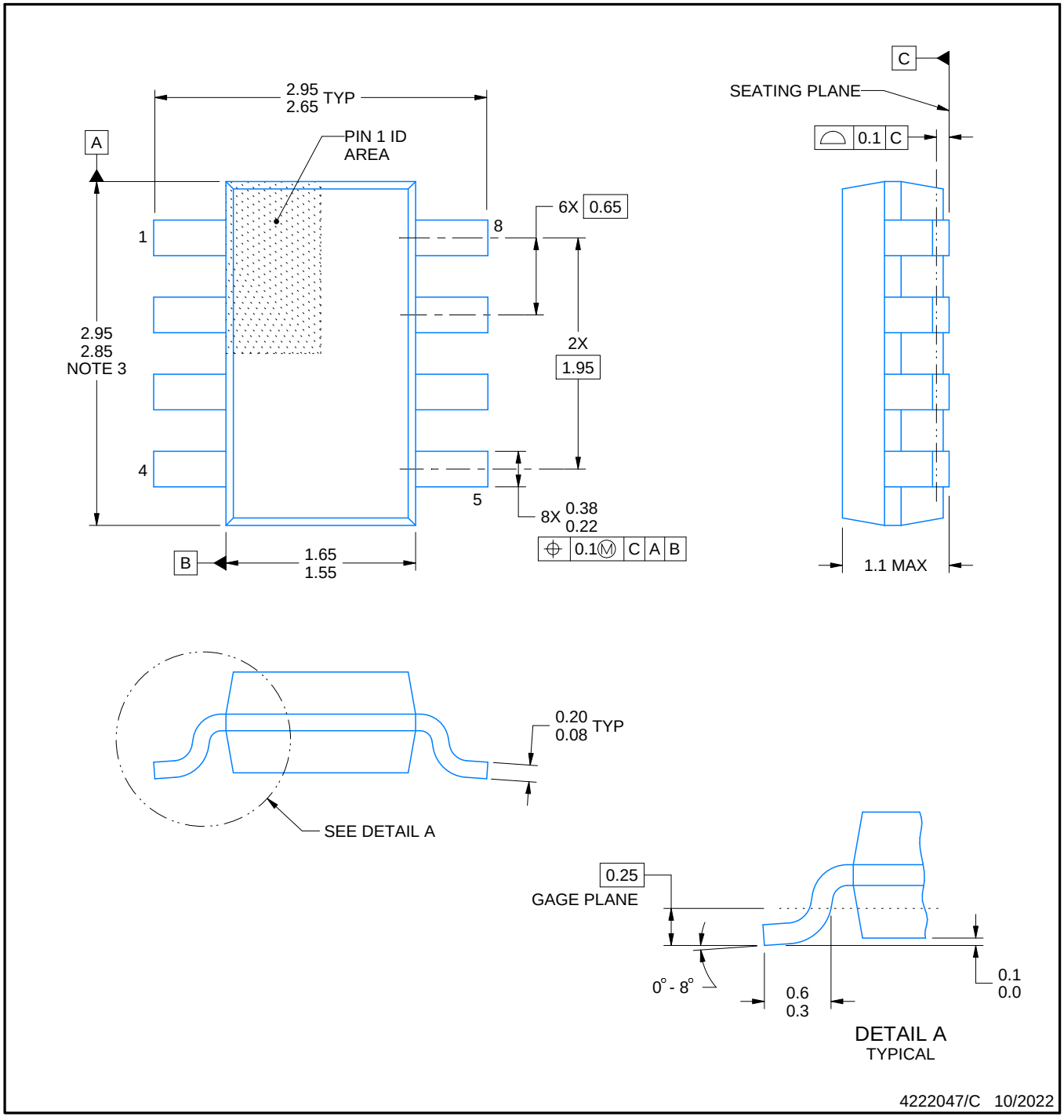
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

PACKAGE OUTLINE

DDF0008A

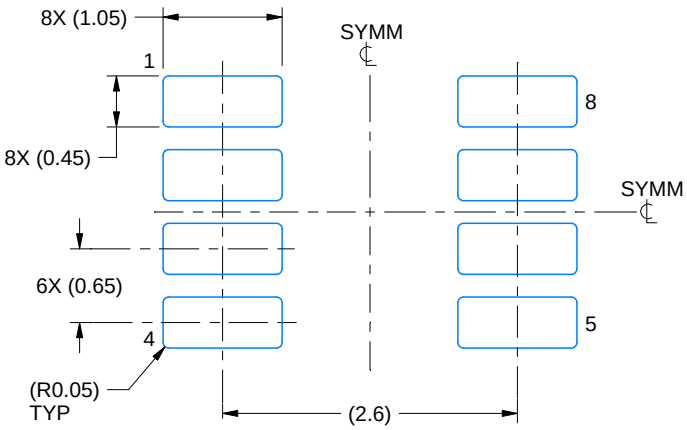
SOT-23 - 1.1 mm max height

PLASTIC SMALL OUTLINE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
SCALE:15X

NON SOLDER MASK
DEFINED

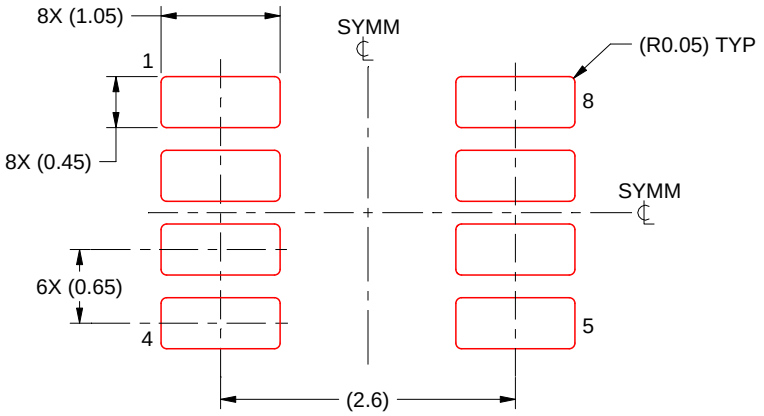
SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4222047/C 10/2022

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4222047/C 10/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

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