TEXAS INSTRUMENTS
TPS3779-Q1, TPS3780-Q1
JAJSCA1A – JUNE 2016 – REVISED SEPTEMBER 2016

TPS37xx-Q1
デュアル・チャネル、低電力、高精度電圧検出器

1 特長

- 車載アプリケーションに対応
- 下記内容でAEC-Q100認定済み：
  - デバイス温度グレード 1: 動作時周囲温度 –40℃～125℃ 範囲
  - デバイスHBM ESD分類レベルH2
  - デバイスCDM ESD分類レベルC4B
- 小型パッケージの2チャネル検出器
- 高精度のスレッショルドとヒステリシス: 1.0%
- 低い静止電流: 2µA (標準値)
- 検出電圧を最小1.2Vまで調整可能
- 5%および10%のヒステリシス・オプション
- 温度範囲: -40℃～+125℃
- プッシュプル(TPS3779-Q1)およびオープン・ドレイン(TPS3780-Q1)出力オプション
- SOT-23パッケージで利用可能

2 アプリケーション

- DSP、マイクロコントローラ、マイクロプロセッサ
- 先進運転支援システム(ADAS)
- インフォテイメントおよびクラスタ
- 電源シーケンス・アプリケーション

3 概要

TPS3779-Q1およびTPS3780-Q1は高精度の2チャネル電圧検出器ファミリで、低電力と小さなソリューション・サイズが特長です。SENSE1およびSENSE2入力には、短時間のグリッチを除去するためのヒステリシスが含まれているため、誤ったトリガが発生せず出力動作が安定します。このデバイス・ファミリは、工場出荷時のヒステリシスが5%または10%のオプションを選択できます。

TPS3779-Q1およびTPS3780-Q1には可変のSENSEx入力があり、外部の分圧抵抗によって構成可能です。SENSE1またはSENSE2入力の電圧が下降時のスレッショルドを下回ると、それぞれOUT1またはOUT2がLOWになります。SENSE1またはSENSE2が上昇時のスレッショルドよりも高くなると、それぞれOUT1またはOUT2がHIGHになります。

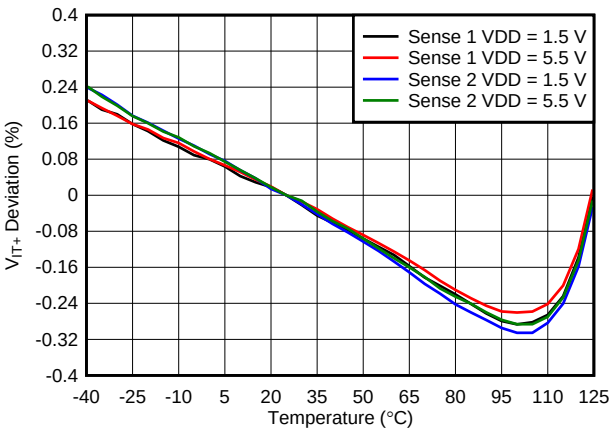
このデバイスは静止電流が2µA (標準値)と非常に低く、正確な電圧を検出できる、省スペースのソリューションで、低電力、システム監視、および携帯用のアプリケーションに適しています。TPS3779-Q1およびTPS3780-Q1は1.5V～5.5V、-40℃～+125℃の温度範囲で動作します。

製品情報(1)

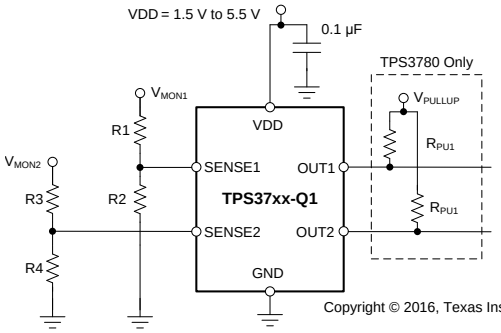
型番	パッケージ	本体サイズ(公称)
TPS37xx-Q1	SOT-23 (6)	2.90mm×1.60mm

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

感知スレッショルド(V_{IT+})の偏差と温度との関係



代表的な回路図



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

2016年6月発行のものから更新 **Page**

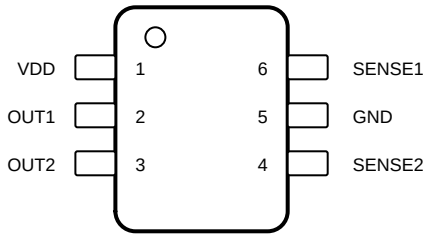
- Added TPS3780A-Q1 row to *Device Comparison Table* ... 3
- Added TPS37xxA-Q1 row to V_{IT-} parameter in *Electrical Characteristics* table ... 5

5 Device Comparison Table

PRODUCT	HYSTERESIS (%)	OUTPUT
TPS3779B-Q1	5	Push-pull
TPS3779C-Q1	10	Push-pull
TPS3780A-Q1	0.5	Open-drain
TPS3780B-Q1	5	Open-drain
TPS3780C-Q1	10	Open-drain

6 Pin Configuration and Functions

DBV Package
6-Pin SOT-23
Top View



Not to scale

Pin Functions

NAME	NO.	I/O	DESCRIPTION
GND	5	—	Ground
OUT1	2	O	OUT1 is the output for SENSE1. OUT1 is asserted (driven low) when the voltage at SENSE1 falls below V_{IT-}. OUT1 is deasserted (goes high) after SENSE1 rises higher than V_{IT+}. OUT1 is a push-pull output for the TPS3779-Q1 and an open-drain output for the TPS3780-Q1. The open-drain device (TPS3780-Q1) can be pulled up to 5.5 V independent of VDD; a pullup resistor is required for this device.
OUT2	3	O	OUT2 is the output for SENSE2. OUT2 is asserted (driven low) when the voltage at SENSE2 falls below V_{IT-}. OUT2 is deasserted (goes high) after SENSE2 rises higher than V_{IT+}. OUT2 is a push-pull output for the TPS3779-Q1 and an open-drain output for the TPS3780-Q1. The open-drain device (TPS3780-Q1) can be pulled up to 5.5 V independent of VDD; a pullup resistor is required for this device.
SENSE1	6	I	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this pin drops below the threshold voltage (V_{IT-}), OUT1 is asserted.
SENSE2	4	I	This pin is connected to the voltage to be monitored with the use of an external resistor divider. When the voltage at this pin drops below the threshold voltage (V_{IT-}), OUT2 is asserted.
VDD	1	I	Supply voltage input. Connect a 1.5-V to 5.5-V supply to VDD in order to power the device. Good analog design practice is to place a 0.1-µF ceramic capacitor close to this pin (required for VDD < 1.5 V).

7 Specifications

7.1 Absolute Maximum Ratings

over operating junction temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Voltage	VDD	–0.3	7	V
	OUT1, OUT2 (TPS3779-Q1 only)	–0.3	VDD + 0.3	
	OUT1, OUT2 (TPS3780-Q1 only)	–0.3	7	
	SENSE1, SENSE2	–0.3	7	
Current	OUT1, OUT2		±20	mA
Temperature	Operating junction, T_J(2)	–40	125	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) For low-power devices, the junction temperature rise above the ambient temperature is negligible; therefore, the junction temperature is considered equal to the ambient temperature ($T_J = T_A$).

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±2000	V
		Charged-device model (CDM), per AEC Q100-011	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating junction temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
	Power-supply voltage		1.5		5.5	V
	Sense voltage	SENSE1, SENSE2	0		5.5	V
	Output voltage (TPS3779-Q1 only)	OUT1, OUT2	0		VDD + 0.3	V
	Output voltage (TPS3780-Q1 only)	OUT1, OUT2	0		5.5	V
R_{PU}	Pullup resistor (TPS3780-Q1 only)		1.5		10,000	kΩ
	Current	OUT1, OUT2	–5		5	mA
C_{IN}	Input capacitor			0.1		µF
T_J	Junction temperature		–40	25	125	°C

7.4 Thermal Information

THERMAL METRIC(1)		TPS3779-Q1, TPS3780-Q1 DBV (SOT-23) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	193.9	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	134.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	30.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	38.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

all specifications are over the operating temperature range of –40°C < T_J < +125°C and 1.5 V ≤ VDD ≤ 5.5 V (unless otherwise noted); typical values are at T_J = 25°C and VDD = 3.3 V

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
VDD	Input supply range			1.5		5.5	V
$V_{(POR)}$	Power-on-reset voltage(1)	V_{OL} (max) = 0.2 V, I_{OL} = 15 µA				0.8	V
I_{DD}	Supply current (into VDD pin)	VDD = 3.3 V, no load			2.09	5.80	µA
		VDD = 5.5 V, no load			2.29	6.50	
V_{IT+}	Positive-going input threshold voltage	$V_{(SENSEx)}$ rising			1.194		V
				–1%		1%	
$V_{IT–}$	Negative-going input threshold voltage	$V_{(SENSEx)}$ falling	TPS37xxA-Q1 (0.5% hysteresis)		1.188		V
			TPS37xxB-Q1 (5% hysteresis)		1.134		
			TPS37xxC-Q1 (10% hysteresis)		1.074		
		$V_{(SENSEx)}$ falling		–1%		1%	
$I_{(SENSEx)}$	Input current	$V_{(SENSEx)}$ = 0 V or VDD		–15		15	nA
V_{OL}	Low-level output voltage	VDD ≥ 1.5 V, I_{SINK} = 0.4 mA				0.25	V
		VDD ≥ 2.7 V, I_{SINK} = 2 mA				0.25	
		VDD ≥ 4.5 V, I_{SINK} = 3.2 mA				0.30	
V_{OH}	High-level output voltage (TPS3779-Q1 only)	VDD ≥ 1.5 V, I_{SOURCE} = 0.4 mA		0.8 VDD			V
		VDD ≥ 2.7 V, I_{SOURCE} = 1 mA		0.8 VDD			
		VDD ≥ 4.5 V, I_{SOURCE} = 2.5 mA		0.8 VDD			
$I_{lkg(OD)}$	Open-drain output leakage current (TPS3780-Q1 only)	High impedance, $V_{(SENSEx)}$ = $V_{(OUTx)}$ = 5.5 V		–250		250	nA

(1) Outputs are undetermined below $V_{(POR)}$.

7.6 Timing Requirements

typical values are at T_J = 25°C and VDD = 3.3 V; SENSEx transitions between 0 V and 1.3 V

		MIN	NOM	MAX	UNIT
$t_{PD(r)}$	SENSEx (rising) to OUTx propagation delay		5.5		µs
$t_{PD(f)}$	SENSEx (falling) to OUTx propagation delay		10		µs
t_{SD}	Startup delay(1)		570		µs

(1) During power-on or when a VDD transient is below VDD(min), the outputs reflect the input conditions 570 µs after VDD transitions through VDD(min).

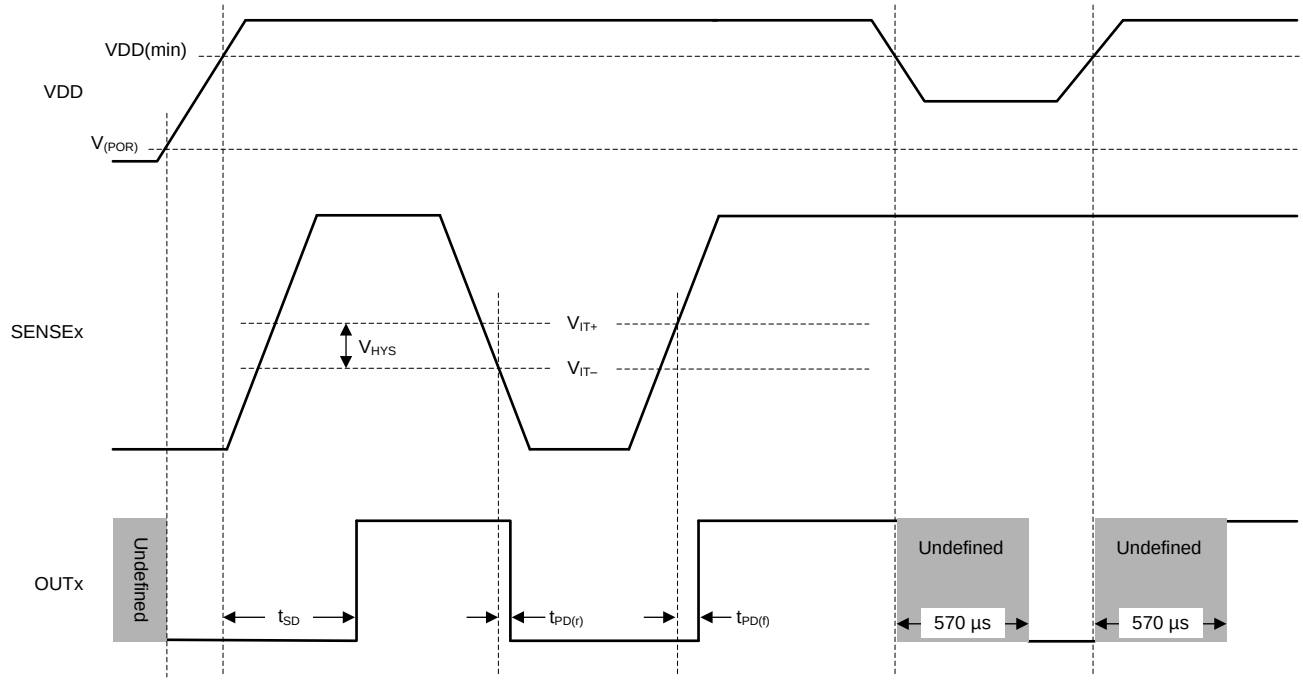


図 1. Timing Diagram

7.7 Typical Characteristics

at T_J = 25°C with a 0.1-µF capacitor close to VDD (unless otherwise noted)

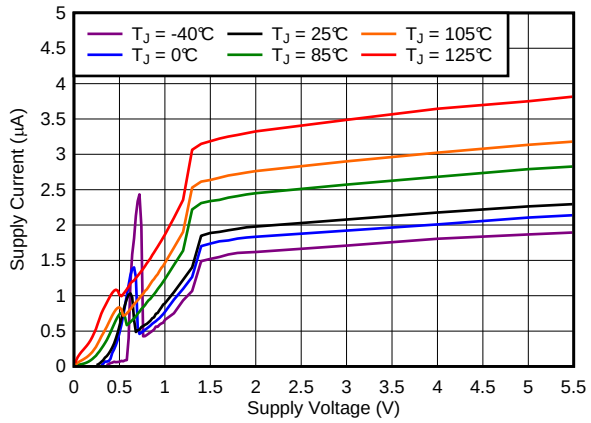


図 2. Supply Current vs Supply Voltage

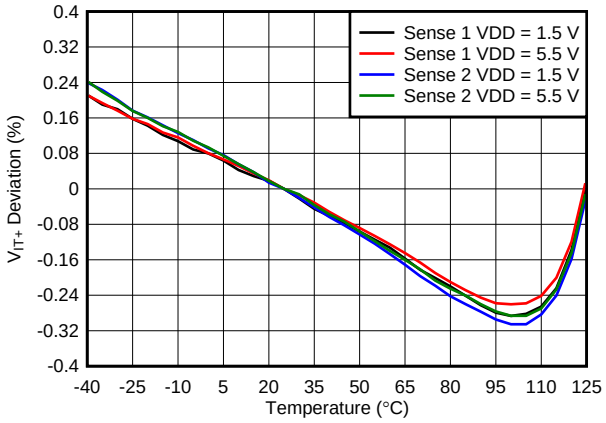


図 3. Sense Threshold (V_{IT+}) Deviation vs Temperature

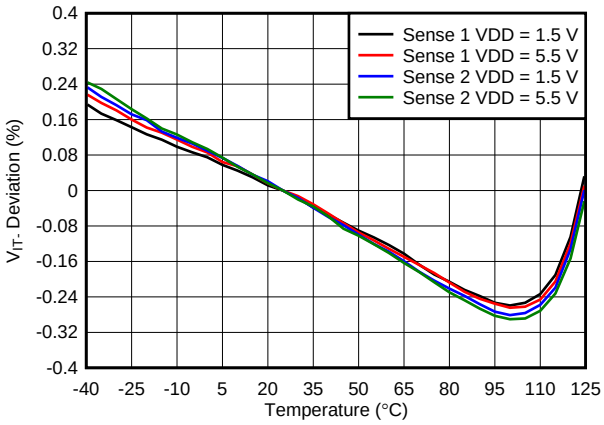


図 4. Sense Threshold (V_{IT-}) Deviation vs Temperature

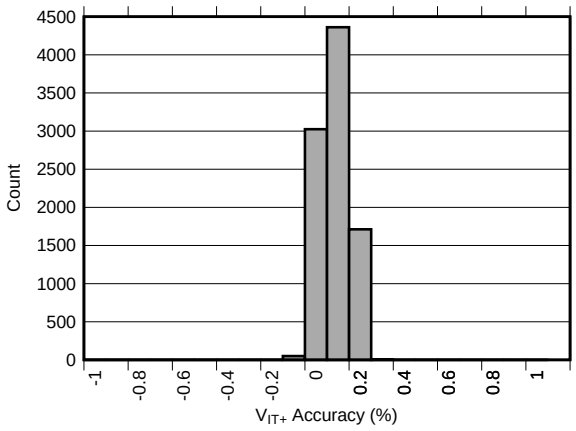


図 5. Sense Threshold (V_{IT+})

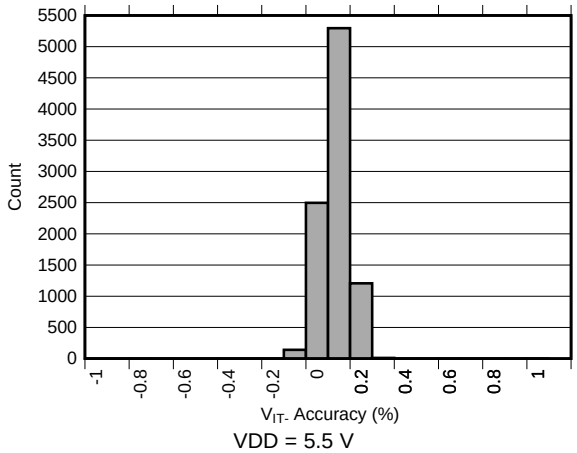


図 6. Sense Threshold (V_{IT-})

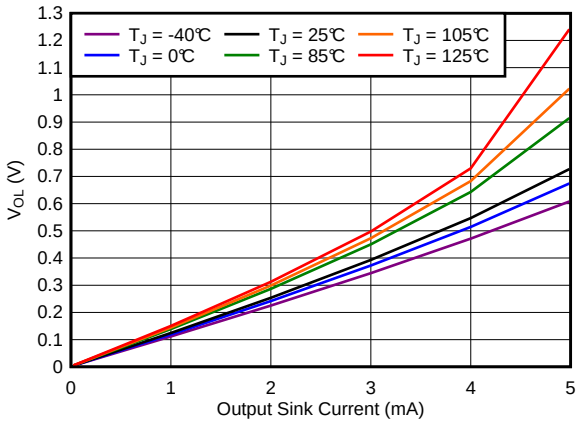


図 7. Output Voltage Low vs Output Current (VDD = 1.5 V)

Typical Characteristics (continued)

at T_J = 25°C with a 0.1-µF capacitor close to VDD (unless otherwise noted)

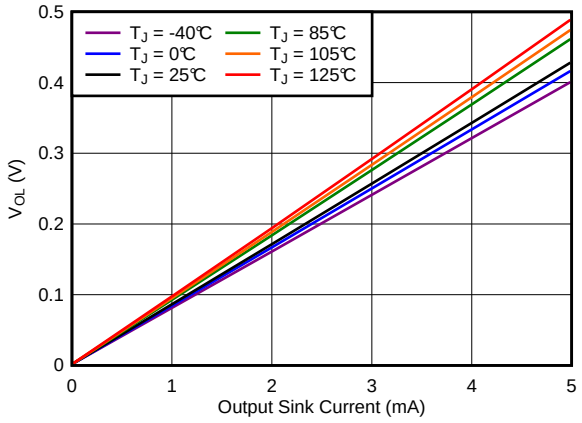


図 8. Output Voltage Low vs Output Current (VDD = 3.3 V)

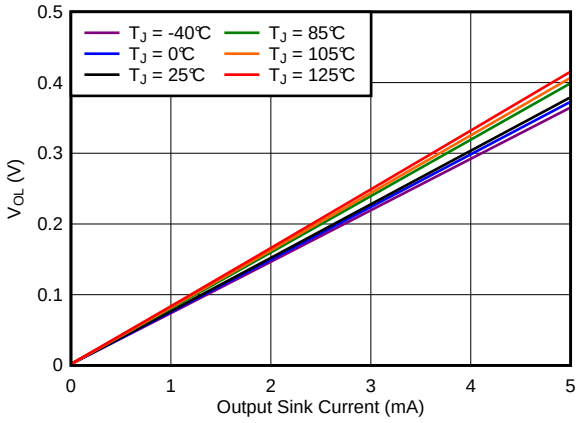


図 9. Output Voltage Low vs Output Current (VDD = 5.5 V)

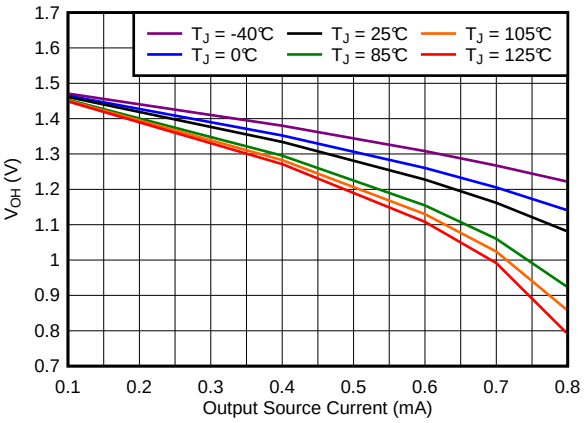


図 10. Output Voltage High vs Output Current (VDD = 1.5 V)

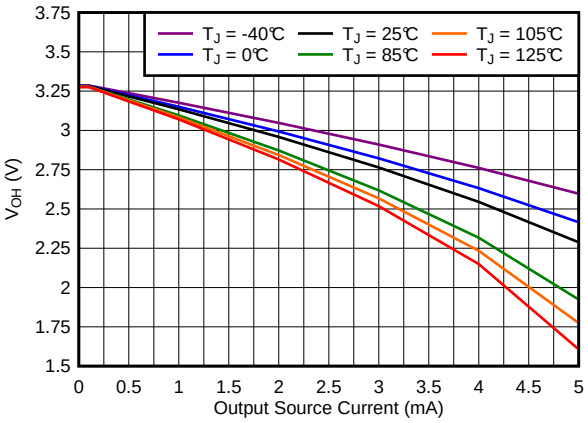


図 11. Output Voltage High vs Output Current (VDD = 3.3 V)

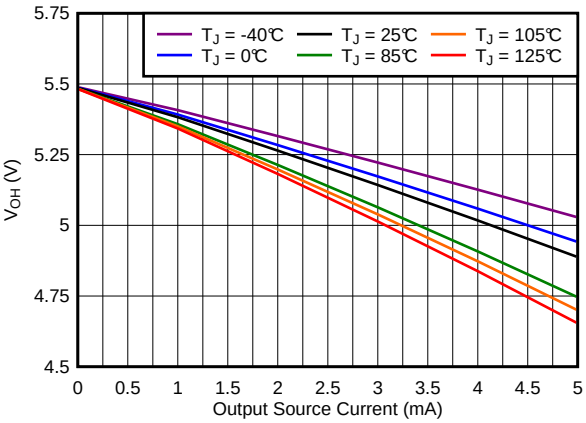
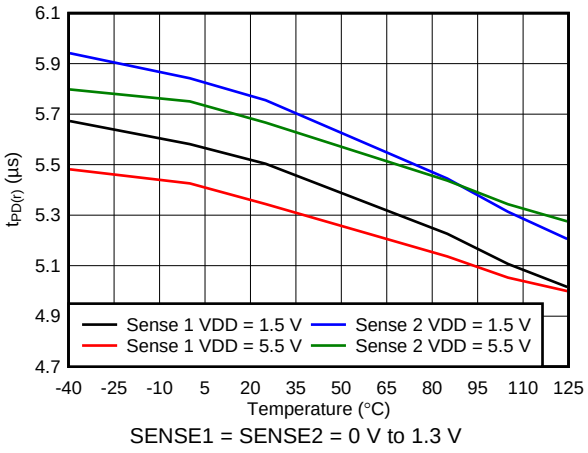


図 12. Output Voltage High vs Output Current (VDD = 5.5 V)

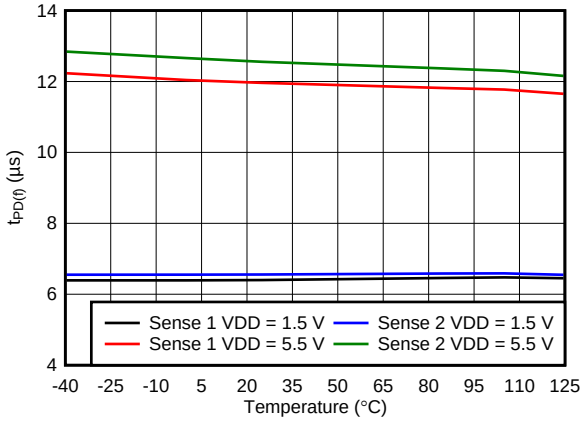


SENSE1 = SENSE2 = 0 V to 1.3 V

図 13. Propagation Delay from SENSEx High to Output High

Typical Characteristics (continued)

at T_J = 25°C with a 0.1-µF capacitor close to VDD (unless otherwise noted)



SENSE1 = SENSE2 = 1.3 V to 0 V

図 14. Propagation Delay from SENSEx Low to Output Low

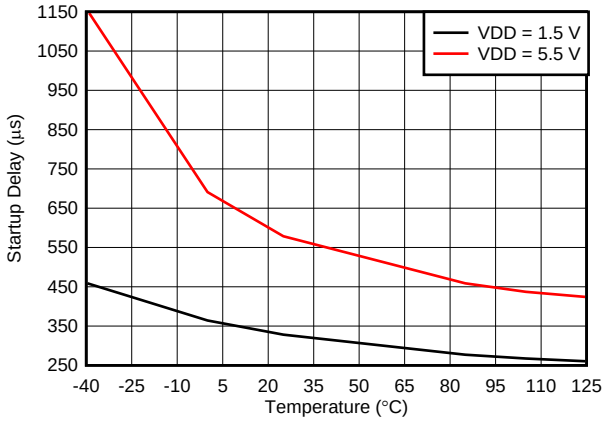
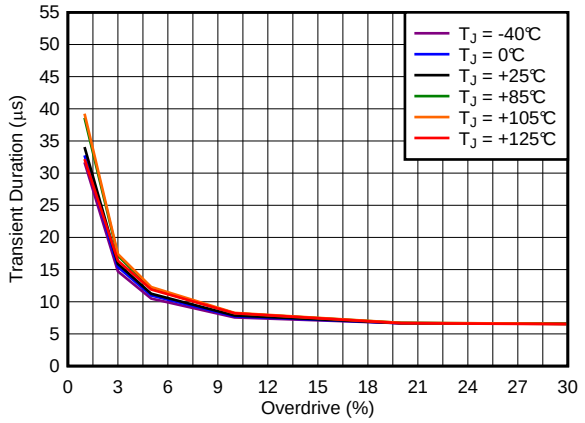
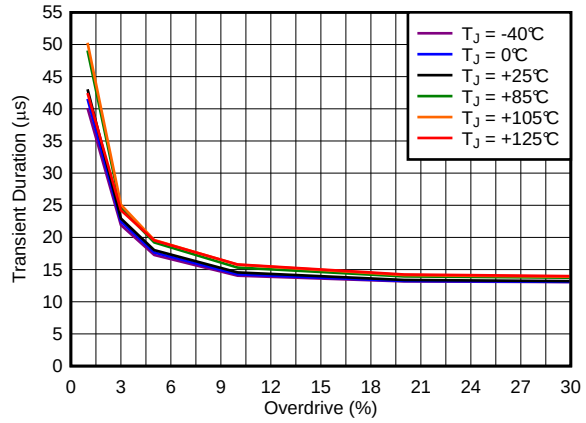


図 15. Startup Delay



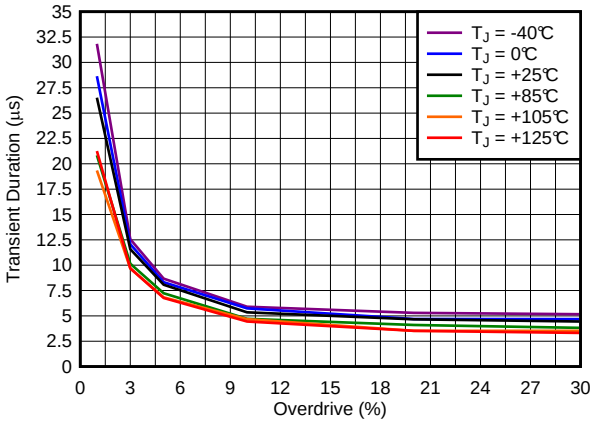
High-to-low transition occurs above the curve

図 16. Minimum Transient Duration vs Overdrive (VDD = 1.5 V)



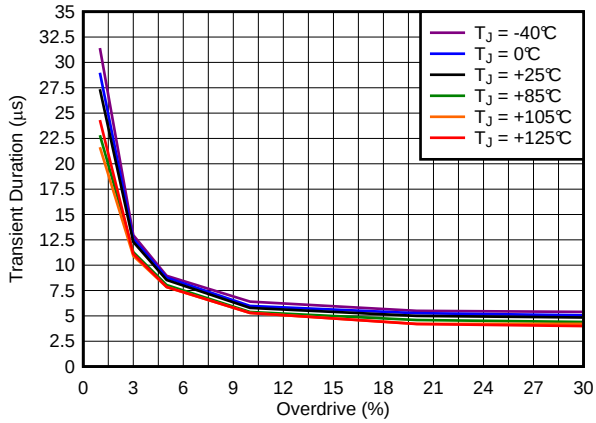
High-to-low transition occurs above the curve

図 17. Minimum Transient Duration vs Overdrive (VDD = 5.5 V)



Low-to-high transition occurs above the curve

図 18. Minimum Transient Duration vs Overdrive (VDD = 1.5 V)



Low-to-high transition occurs above the curve

図 19. Minimum Transient Duration vs Overdrive (VDD = 5.5 V)

8 Detailed Description

8.1 Overview

The TPS3779-Q1 and TPS3780-Q1 are small, low quiescent current (I_{DD}), dual-channel voltage detectors. These devices have high-accuracy rising and falling input thresholds, and assert the output as shown in 表 1. The output (OUTx pin) goes low when the SENSEx pin is less than V_{IT-} and goes high when the pin is greater than V_{IT+}. The TPS3779-Q1 and TPS3780-Q1 offer two hysteresis options (5% and 10%) for use in a wide variety of applications. These devices have two independent voltage-detection channels that can be used in systems where multiple voltage rails are required to be monitored, or where one channel can be used as an early warning signal and the other channel can be used as the system reset signal.

表 1. TPS3779-Q1, TPS3780-Q1 Truth Table

CONDITIONS	OUTPUT
SENSE1 < V_{IT-}	OUT1 = low
SENSE2 < V_{IT-}	OUT2 = low
SENSE1 > V_{IT+}	OUT1 = high
SENSE2 > V_{IT+}	OUT2 = high

8.2 Functional Block Diagrams

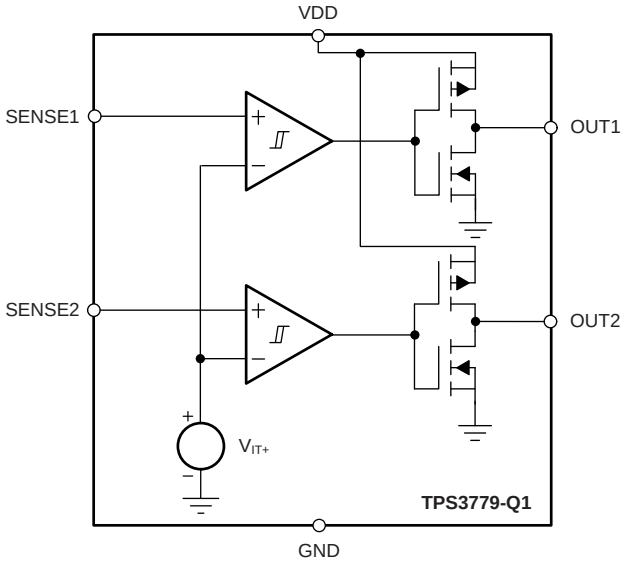


図 20. TPS3779-Q1 Block Diagram

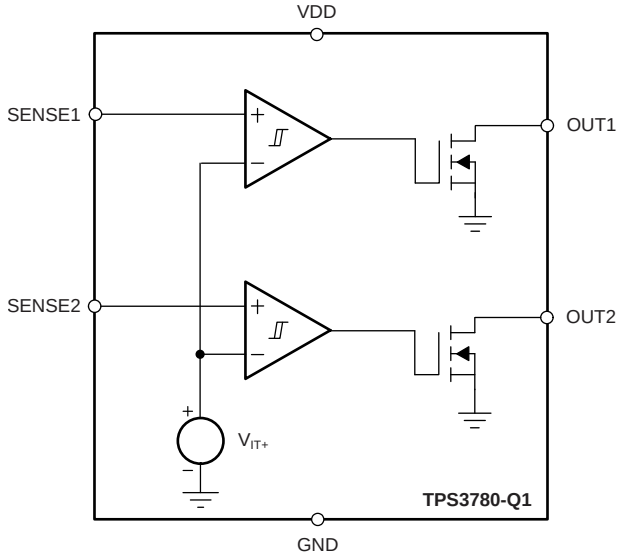


図 21. TPS3780-Q1 Block Diagram

8.3 Feature Description

8.3.1 Inputs (SENSE1, SENSE2)

The TPS3779-Q1 and TPS3780-Q1 each have two comparators for voltage detection. Each comparator has one external input; the other input is connected to the internal reference. The comparator rising threshold is designed and trimmed to be equal to V_{IT+}, and the falling threshold is trimmed to be equal to V_{IT-}. The built-in falling hysteresis options make the devices immune to supply rail noise and ensure stable operation.

The comparator inputs can swing from ground to 5.5 V, regardless of the device supply voltage used. Although not required in most cases, for extremely noisy applications, good analog design practice is to place a 1-nF to 10-nF bypass capacitor at the comparator input in order to reduce sensitivity to transients and layout parasitic.

For each SENSEx input, the corresponding output (OUTx) is driven to logic low when the input voltage drops below V_{IT-}. When the voltage exceeds V_{IT+}, the output (OUTx) is driven high; see 図 1.

8.3.2 Outputs (OUT1, OUT2)

In a typical device application, the outputs are connected to a reset or enable input of another device, such as a digital signal processor (DSP), central processing unit (CPU), field-programmable gate array (FPGA), or application-specific integrated circuit (ASIC); or the outputs are connected to the enable input of a voltage regulator, such as a dc-dc or low-dropout (LDO) regulator.

The TPS3779-Q1 provides two push-pull outputs. The logic high level of the outputs is determined by the VDD pin voltage. Pullup resistors are not required with this configuration, thus saving board space. However, all interface logic levels must be examined. All OUTx connections must be compatible with the VDD pin logic level.

The TPS3780-Q1 provides two open-drain outputs (OUT1 and OUT2); pullup resistors must be used to hold these lines high when the output goes to a high-impedance condition (not asserted). By connecting pullup resistors to the proper voltage rails, the outputs can be connected to other devices at correct interface voltage levels. The outputs can be pulled up to 5.5 V, independent of the device supply voltage. To ensure proper voltage levels, make sure to choose the correct pullup resistor values. The pullup resistor value is determined by V_{OL}, the sink current capability, and the output leakage current ($I_{lkg(OD)}$). These values are specified in the *Electrical Characteristics* table. By using wired-AND logic, OUT1 and OUT2 can be combined into one logic signal. The *Inputs (SENSE1, SENSE2)* section describes how the outputs are asserted or deasserted. See 図 1 for a description of the relationship between threshold voltages and the respective output.

8.4 Device Functional Modes

8.4.1 Normal Operation (VDD ≥ VDD(min))

When the voltage on VDD is greater than VDD(min) for t_{SD}, the output signals react to the present state of the corresponding SENSEx pins.

8.4.2 Power-On-Reset (VDD < $V_{(POR)}$)

When the voltage on VDD is lower than the required voltage to internally pull the logic low output to GND ($V_{(POR)}$), both outputs are undefined and are not to be relied upon for proper system function.

9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TPS3779-Q1 and TPS3780-Q1 are used as precision, dual-voltage detectors. The monitored voltage, VDD voltage, and output pullup voltage (TPS3780-Q1 only) can be independent voltages or connected in any configuration.

9.1.1 Threshold Overdrive

Threshold overdrive is how much V_{SENSE1} or V_{SENSE2} exceeds the specified threshold, and is important to know because a smaller overdrive results in a slower OUTx response. Threshold overdrive is calculated as a percent of the threshold in question, as shown in 式 1:

$$\text{Overdrive} = | (V_{SENSE1,2} / V_{IT} - 1) \times 100\% | \quad (1)$$

where

- V_{IT} is either V_{IT-} or V_{IT+}, depending on whether calculating the overdrive for the negative-going threshold or the positive-going threshold, respectively
- $V_{SENSE1,2}$ is the voltage at the SENSE1 or SENSE2 input

図 16 illustrates the minimum detectable pulse on the SENSEx inputs versus overdrive, and is used to visualize the relationship that overdrive has on $t_{PD(f)}$ for negative-going events.

9.1.2 Sense Resistor Divider

The resistor divider values and target threshold voltage can be calculated by using 式 2 and 式 3 to determine $V_{MON(UV)}$ and $V_{MON(PG)}$, respectively.

$$V_{MON(UV)} = \left(1 + \frac{R1}{R2}\right) \times V_{IT-} \quad (2)$$

$$V_{MON(PG)} = \left(1 + \frac{R1}{R2}\right) \times V_{IT+} \quad (3)$$

where

- R1 and R2 are the resistor values for the resistor divider on the SENSEx pins
- $V_{MON(UV)}$ is the target voltage at which an undervoltage condition is detected
- $V_{MON(PG)}$ is the target voltage at which the output goes high when V_{MONx} rises

Choose R_{TOTAL} (equal to R1 + R2) so that the current through the divider is approximately 100 times higher than the input current at the SENSEx pins. The resistors can have high values to minimize current consumption as a result of low input bias current without adding significant error to the resistive divider. For details on sizing input resistors, see the *Optimizing Resistor Dividers at a Comparator Input* application report (SLVA450), available for download from www.ti.com.

9.2 Typical Applications

9.2.1 Monitoring Two Separate Rails

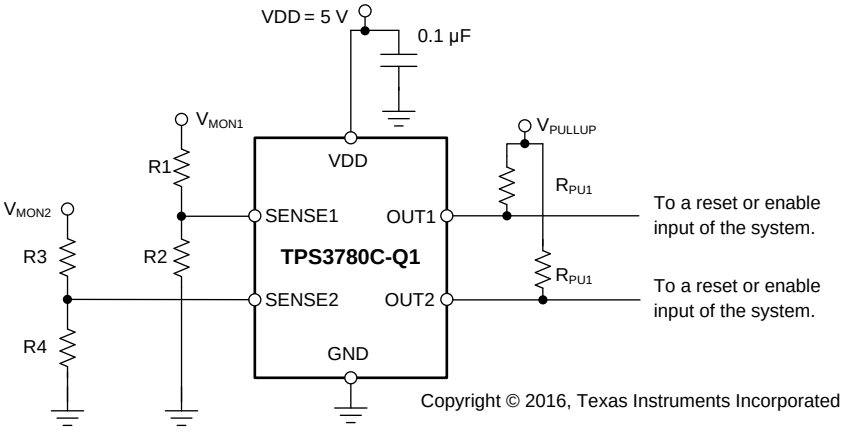


図 22. Monitoring Two Separate Rails Schematic

9.2.1.1 Design Requirements

表 2. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
VDD	5 V	5 V
Hysteresis	10%	10%
Monitored voltage 1	3.3 V nominal, $V_{MON(PG)}$ = 2.9 V, $V_{MON(UV)}$ = 2.6 V	$V_{MON(PG)}$ = 2.908 V, $V_{MON(UV)}$ = 2.618 V
Monitored voltage 2	3 V nominal, $V_{MON(PG)}$ = 2.6 V, $V_{MON(UV)}$ = 2.4 V	$V_{MON(PG)}$ = 2.606 V, $V_{MON(UV)}$ = 2.371 V
Output logic voltage	3.3-V CMOS	3.3-V CMOS

9.2.1.2 Detailed Design Procedure

1. Select the TPS3780C-Q1. The C version is selected to satisfy the hysteresis requirement. The TPS3780-Q1 is selected for the output logic requirement. An open-drain output allows for the output to be pulled up to a voltage other than VDD.
2. The resistor divider values are calculated by using 式 2 and 式 3. For SENSE1, R1 = 1.13 MΩ and R2 = 787 kΩ. For SENSE2, R3 (R1) = 681 kΩ and R4 (R2) = 576 kΩ.

9.2.1.3 Application Curve

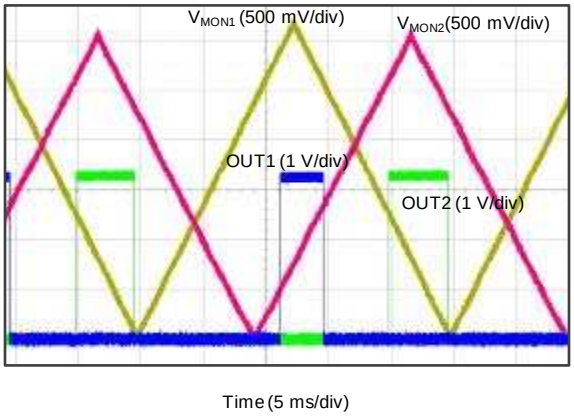


図 23. Monitoring Two Separate Rails Curve

9.2.2 Early Warning Detection

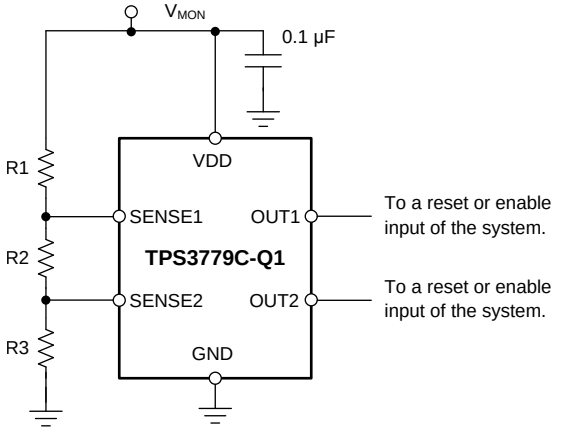


図 24. Early Warning Detection Schematic

9.2.2.1 Design Requirements

表 3. Design Parameters

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
VDD	V_{MON}	V_{MON}
Hysteresis	10%	10%
Monitored voltage 1	$V_{MON(PG)}$ = 3.3 V, $V_{MON(UV)}$ = 3 V	$V_{MON(PG)}$ = 3.330 V, $V_{MON(UV)}$ = 2.997 V
Monitored voltage 2	$V_{MON(PG)}$ = 3.9 V, $V_{MON(UV)}$ = 3.5 V	$V_{MON(PG)}$ = 3.921 V, $V_{MON(UV)}$ = 3.529 V

9.2.2.2 Detailed Design Procedure

1. Select the TPS3779C-Q1. The C version is selected to satisfy the hysteresis requirement. The TPS3779-Q1 is selected to save on component count and board space.
2. Use 式 4 to calculate the total resistance for the resistor divider. Determine the minimum total resistance of the resistor network necessary to achieve the current consumption specification. For this example, the current flow through the resistor network is chosen to be 1.41 µA. Use the key transition point for V_{MON2}. For this example, the low-to-high transition, $V_{MON(PG)}$, is considered more important.

$$R_{TOTAL} = \frac{V_{MON(PG\_2)}}{I} = \frac{3.9\ V}{1.41\ \mu A} = 2.78\ M\Omega \quad (4)$$

where

- $V_{MON(PG\_2)}$ is the target voltage at which OUT2 goes high when V_{MON} rises
- I is the current flowing through the resistor network

3. After R_{TOTAL} is determined, R3 can be calculated using 式 5. Select the nearest 1% resistor value for R3. In this case, 845 kΩ is the closest value.

$$R3 = \frac{V_{IT+}}{I} = \frac{1.194\ V}{1.41\ \mu A} = 846\ k\Omega \quad (5)$$

4. Use 式 6 to calculate R2. Select the nearest 1% resistor value for R2. In this case, 150 kΩ is the closest value. Use the key transition point for V_{MON1}. For this example, the high-to-low transition, $V_{MON(UV)}$, is considered more important.

$$R2 = \frac{R_{TOTAL}}{V_{MON(UV\_1)}} \bullet V_{IT-} - R3 = \frac{2.78\ M\Omega}{3\ V} \bullet 1.074\ V - 845\ k\Omega = 149\ k\Omega \quad (6)$$

where

- $V_{MON(UV\_1)}$ is the target voltage at which OUT1 goes low when V_{MON} falls

5. Use 式 7 to calculate R1. Select the nearest 1% resistor value for R1. In this case, 1.78 MΩ is a 1% resistor.

$$R1 = R_{TOTAL} - R2 - R3 = 2.78\ M\Omega - 150\ k\Omega - 845\ k\Omega = 1.78\ M\Omega \quad (7)$$

9.2.2.3 Application Curve

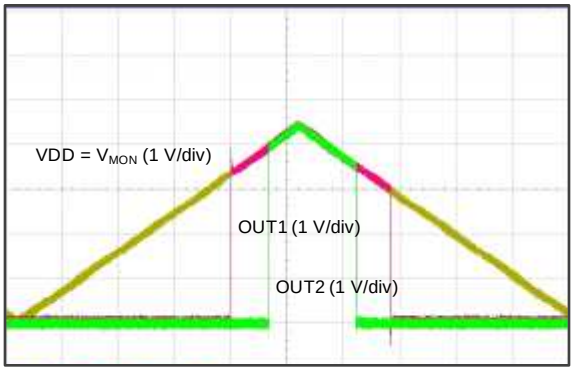


図 25. Early Warning Detection Curve

10 Power-Supply Recommendations

The TPS3779-Q1 and TPS3780-Q1 are designed to operate from an input voltage supply range between 1.5 V and 5.5 V. An input supply capacitor is not required for this device; however, good analog practice is to place a 0.1-µF or greater capacitor between the VDD pin and the GND pin. This device has a 7-V absolute maximum rating on the VDD pin. If the voltage supply providing power to VDD is susceptible to any large voltage transient that can exceed 7 V, additional precautions must be taken.

For applications where SENSEx is greater than 0 V before VDD, and is subject to a startup slew rate of less than 200 mV per 1 ms, the output can be driven to logic high in error. To correct the output, cycle the SENSEx lines below V_{IT-} or sequence SENSEx after VDD.

11 Layout

11.1 Layout Guidelines

Place the VDD decoupling capacitor close to the device.

Avoid using long traces for the VDD supply node. The VDD capacitor, along with parasitic inductance from the supply to the capacitor, can form an LC tank circuit that creates ringing with peak voltages above the maximum VDD voltage.

11.2 Layout Example

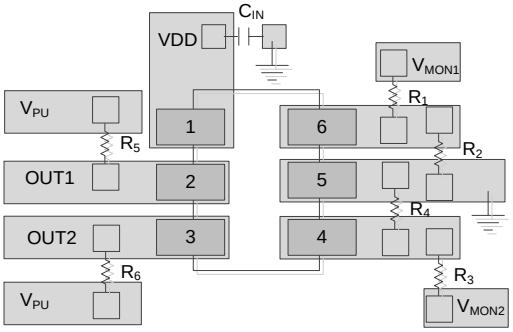


図 26. Example SOT-23 Layout

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 開発サポート

12.1.1.1 評価モジュール

TPS3779-Q1およびTPS3780-Q1を使用する回路性能の初期評価に役立てるため、評価モジュール(EVM)を利用可能です。*『TPS3780EVM-154評価モジュール』*には、TPS3780EVM-154用の設計キットと評価モジュールの詳細が記載されています。

このEVMは、テキサス・インスツルメンツのTPS3779-Q1およびTPS3780-Q1の製品フォルダから請求するか、TIのeStoreから直接購入できます。

12.1.1.2 SPICEモデル

SPICEを使用した回路性能のコンピュータによるシミュレーションは、アナログ回路やシステムの性能を分析するため多くの場合に有用です。TPS3779-Q1およびTPS3780-Q1のSPICEモデルは、「シミュレーション・モデル」の下にある該当デバイスの製品フォルダで利用できます。

12.1.2 デバイスの項目表記

TPS3779xQyyyzQ1およびTPS3780xQyyyzQ1は、これらのデバイスの汎用的な名前付け規則です。TPS3779-Q1およびTPS3780-Q1はこれらのデバイスのファミリを表します。xはヒステリシスのバージョンを示し、yyyはパッケージの指定用に予約され、zはパッケージ数量を示します。

- 例: TPS3780CDBVRQ1
- ファミリ: TPS3780-Q1 (オープン・ドレイン)
- ヒステリシス: 10%
- DBVパッケージ: 6ピンのSOT-23
- パッケージ数量: Rは3000個を示します。

12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください。

- *『TPS3780EVM-154評価モジュール』*(SLVU796)
- *『コンパレータ入力における分圧抵抗の最適化』*アプリケーション・レポート(SLVA450)

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「*通知を受け取る*」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 4. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
TPS3779-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS3780-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.5 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.6 商標

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

12.7 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3779BQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12OE	Samples
TPS3779CQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12PE	Samples
TPS3780AQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12FE	Samples
TPS3780BQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12GE	Samples
TPS3780CQDBVRQ1	ACTIVE	SOT-23	DBV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	12HE	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

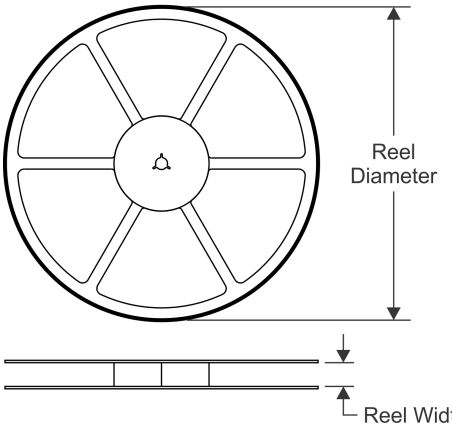
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

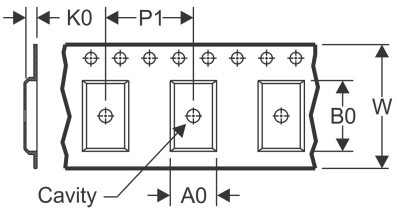
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

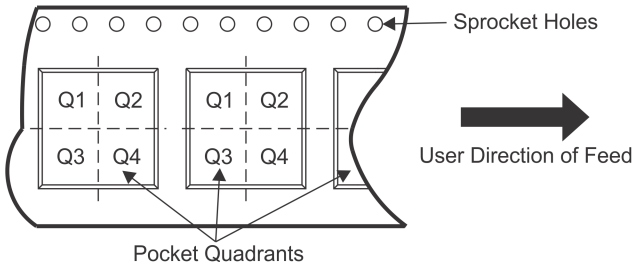


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

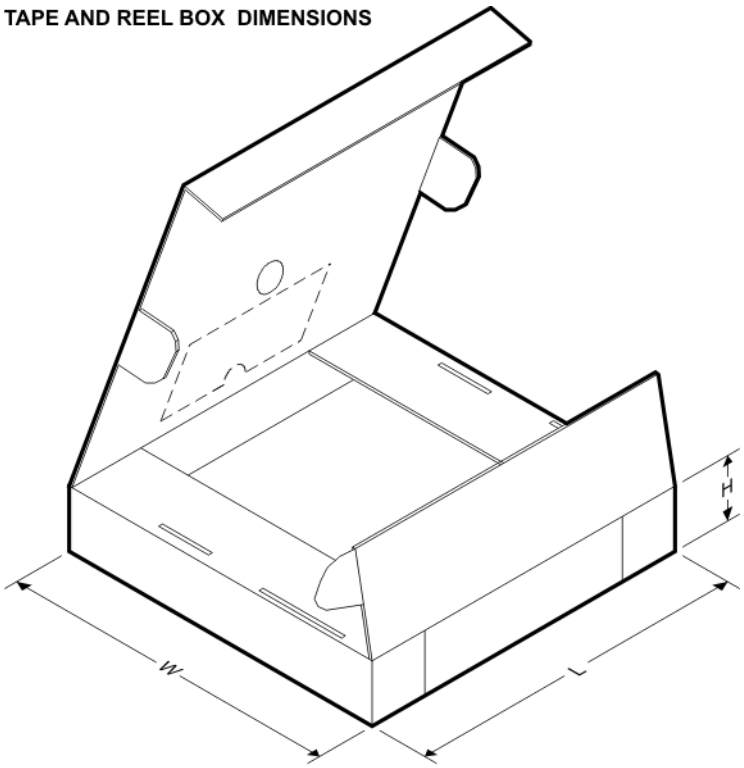
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3779BQDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3779CQDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3780AQDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3780BQDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS3780CQDBVRQ1	SOT-23	DBV	6	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

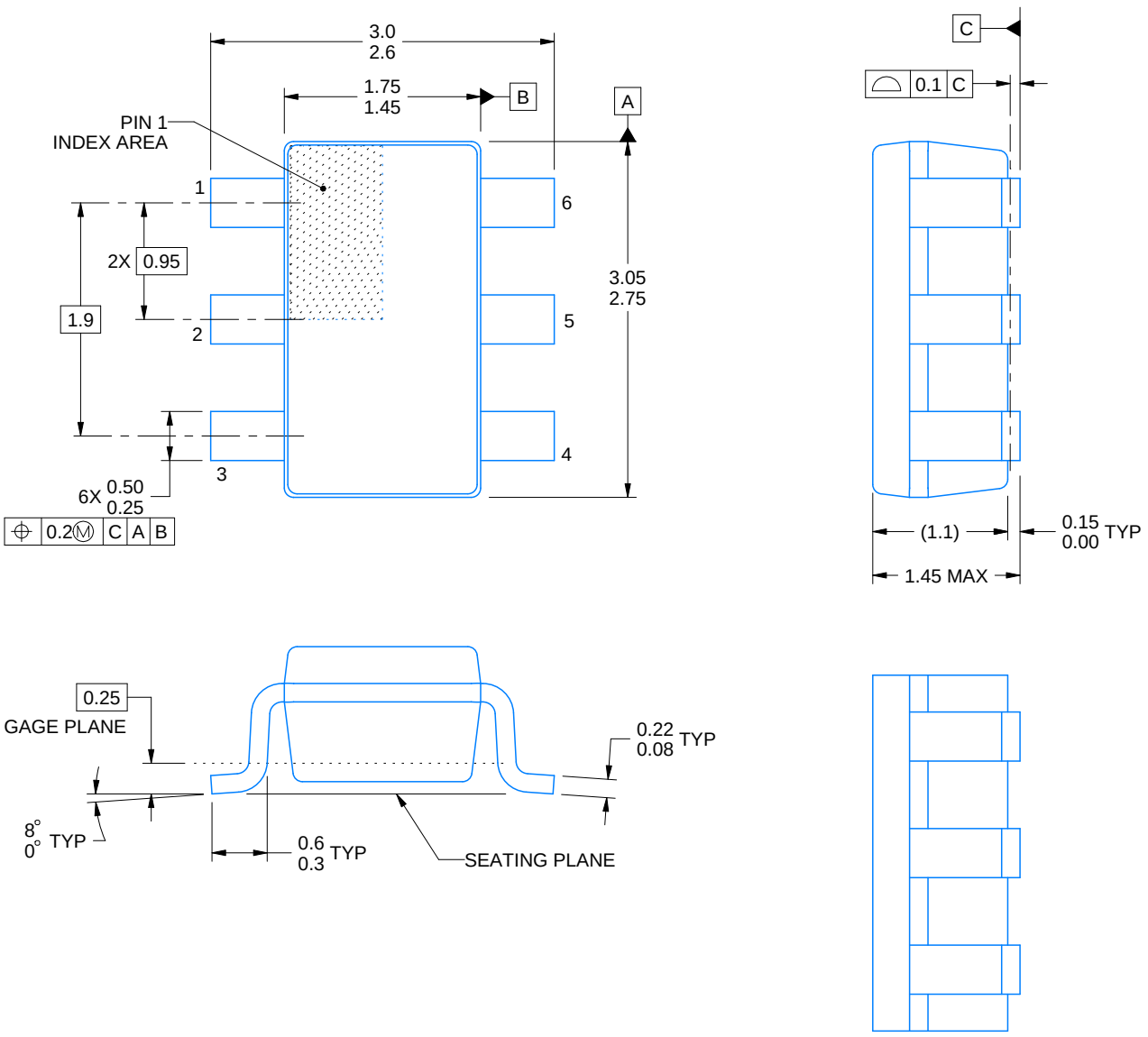
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3779BQDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3779CQDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3780AQDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3780BQDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0
TPS3780CQDBVRQ1	SOT-23	DBV	6	3000	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0006A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

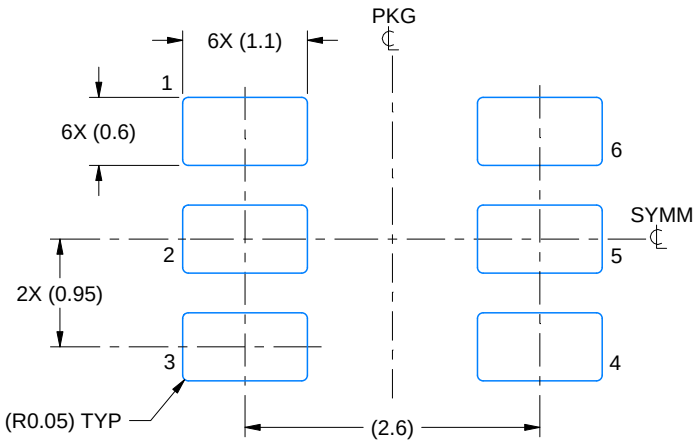


ALTERNATIVE PACKAGE SINGULATION VIEW

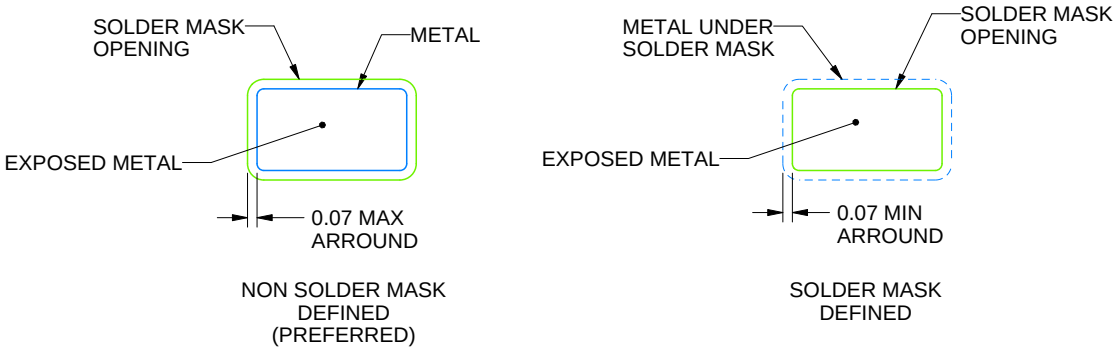
4214840/E 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

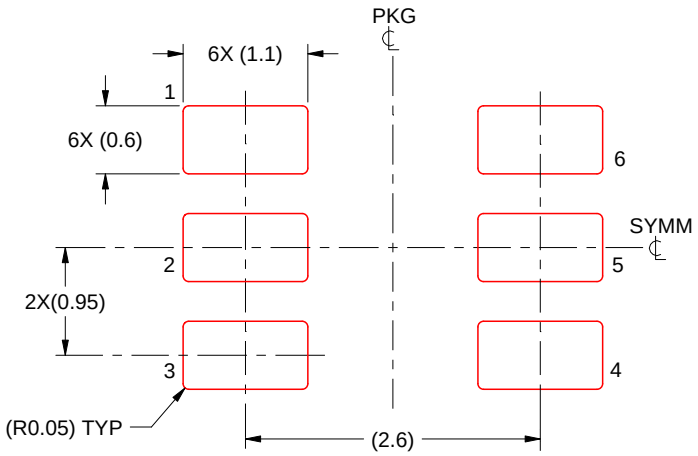


SOLDER MASK DETAILS

4214840/E 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/E 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265