TEXAS INSTRUMENTS
TPS3840
JAJSGL5C – DECEMBER 2018 – REVISED AUGUST 2019

TPS3840 $\overline{MR}$ およびプログラマブル遅延機能搭載のナノパワー、高入力電圧スーパーバイザ

1 特長

- 広い動作電圧：1.5V～10V
- ナノアンペア単位の消費電流：標準値 300nA、最大値 700nA
- 固定スレッショルド電圧 (V_{IT-})
  - 1.6V から 4.9V まで 0.1V 刻みのスレッショルド
  - 高精度：標準値 1%、最大値 1.5%
  - ヒステリシス内蔵 (V_{IT+})
    - $1.6V < V_{IT-} \leq 3.0V$：100mV (標準値)
    - $3.1V \leq V_{IT-} < 4.9V$：200mV (標準値)
- スタートアップ遅延 (t_{STRT})：標準値 220µs、最大値 350µs
- リセット遅延時間をプログラム可能 (t_D)
  - 50µs (コンデンサなし) から 6.2s (10µF) まで
- アクティブ LOW のマニュアル・リセット ($\overline{MR}$)
- 3 つの出力トポロジ
  - TPS3840DL：オープン・ドレイン、アクティブ LOW ($\overline{RESET}$)、プルアップ抵抗が必要
  - TPS3840PL：プッシュプル、アクティブ LOW ($\overline{RESET}$)
  - TPS3840PH：プッシュプル、アクティブ HIGH (RESET)
- 広い温度範囲：-40℃～+125℃
- パッケージ：SOT23-5 (DBV)

2 アプリケーション

- グリッド・インフラストラクチャ：サーキット・ブレーカ、スマート・メータ、その他の監視および保護機器
- ファクトリ・オートメーション：フィールド・トランスミッタ、PLC
- ビルディング・オートメーション：防火、煙感知器、HVAC
- POS システム
- ポータブル / バッテリ駆動システム

3 概要

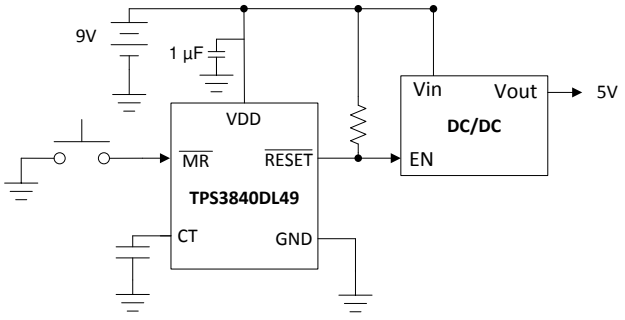
Vin が広いため、外付け部品を使用しないで 9V のレールまたはバッテリを監視できます。また、外付け抵抗を使用すると 24V のレールを監視できます。Nano-Iq により低消費電力アプリケーションでのバッテリ動作時間を延長し、また外付け抵抗を使用する際の消費電流を最小化できます。スタートアップ遅延により、システムの他の部分が電源オンになる前に電圧フォルトを検出できるため、危険なスタートアップ・フォルト条件でも最大限の安全性を確保できます。パワーオン・リセット電圧 (V_{POR}) が低いため、誤ったリセットや次のデバイスの早すぎるイネーブルまたは電源オンを防止し、電源オンおよびオフ時に適切なトランジスタ制御を実現できます。

製品情報(1)

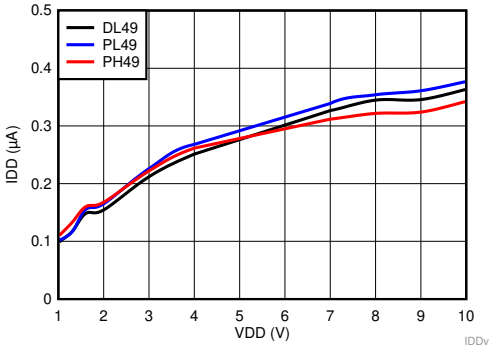
型番	パッケージ	本体サイズ(公称)
TPS3840	SOT-23 (5) (DBV)	2.90mm×1.60mm

(1) パッケージの詳細については、このデータシートの末尾の外形図を参照してください。

代表的なアプリケーション回路



TPS3840 の標準的な消費電流



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision B (July 2019) から **Revision C** に変更 **Page**

- Changed Device Comparison Table ... 4

Revision A (May 2019) から **Revision B** に変更 **Page**

- Updated Device Comparison Table ... 4
- Updated Functional Block Diagram ... 17
- 変更 equation 5 and 6 ... 18
- Updated Application Design #2 ... 23

2018年12月発行のものから更新 **Page**

- データシートを「事前情報」から「量産データ」に 変更 ... 1

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5 概要 (続き)

リセット出力信号は、V_{DD} の電圧が負の電圧スレッショルド (V_{IT-}) を下回った場合、またはマニュアル・リセット ($\overline{MR}$) が論理 LOW ($V_{\overline{MR}_L}$) に駆動された場合、アサートされます。リセット信号は、V_{DD} が V_{IT-} にヒステリシスを加えた値 (V_{IT+}) を上回った場合、またはマニュアル・リセットがフローティングまたは $V_{\overline{MR}_H}$ を上回った状態でリセット遅延時間 (t_D) が経過した場合、クリアされます。CT ピンとグランドの間にコンデンサを接続することで、リセット遅延時間をプログラムできます。高速にリセットする場合は、CT ピンをフローティングのままにします。

その他の特長として、$\overline{MR}$ と V_{DD} の内蔵グリッチ耐性保護、内蔵ヒステリシス、低いオープン・ドレイン出力リーク電流 ($I_{LKG(OD)}$) があります。

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6 Device Comparison Table

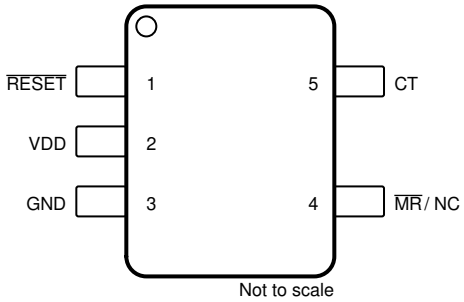
Device Comparison Table shows the available (Active) device variants and variants releasing soon (Preview). Other voltages from 表 3 at the end of datasheet can be sample upon request, please contact TI sales representative for details.

PART NUMBER	OUTPUT TOPOLOGY	THRESHOLD (V_{it-}) (V)	HYSTERESIS (mV)	Status
TPS3840DL18	Open-Drain, Active-Low	1.8	100	Active
TPS3840DL20	Open-Drain, Active-Low	2.0	100	Active
TPS3840PL20	Push-Pull, Active-Low	2.0	100	Active
TPS3840DL22	Open-Drain, Active-Low	2.2	100	Active
TPS3840PL25	Push-Pull, Active-Low	2.5	100	Active
TPS3840DL27	Open-Drain, Active-Low	2.7	100	Active
TPS3840PL27	Push-Pull, Active-Low	2.7	100	Active
TPS3840DL28	Open-Drain, Active-Low	2.8	100	Active
TPS3840PL28	Push-Pull, Active-Low	2.8	100	Active
TPS3840DL29	Open-Drain, Active-Low	2.9	100	Active
TPS3840DL30	Open-Drain, Active-Low	3.0	100	Active
TPS3840PL30	Push-Pull, Active-Low	3.0	100	Active
TPS3840PH30	Push-Pull, Active-High	3.0	100	Active
TPS3840PL43	Push-Pull, Active-Low	4.3	200	Active
TPS3840DL45	Open-Drain, Active-Low	4.5	200	Active
TPS3840PL45	Push-Pull, Active-Low	4.5	200	Active

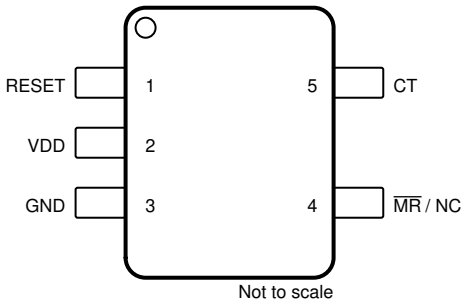
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7 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
TPS3840PL, TPS3840DL Top View



DBV Package
5-Pin SOT-23
TPS3840PH Top View



Pin Functions

PIN			I/O	DESCRIPTION
NAME	TPS3840PL, TPS3840DL	TPS3840PH		
RESET	N/A	1	O	**Active-High Output Reset Signal:** This pin is driven high when either the $\overline{MR}$ pin is driven to a logic low or VDD voltage falls below the negative voltage threshold (V_{IT-}). RESET remains high (asserted) for the delay time period (t_D) after both $\overline{MR}$ is floating or above $V_{\overline{MR}_L}$ and VDD voltage rise above V_{IT+}.
$\overline{RESET}$	1	N/A	O	**Active-Low Output Reset Signal:** This pin is driven logic when either the $\overline{MR}$ pin is driven to a logic low or VDD voltage falls below the negative voltage threshold (V_{IT-}). $\overline{RESET}$ remains low (asserted) for the delay time period (t_D) after both $\overline{MR}$ is floating or above $V_{\overline{MR}_L}$ and VDD voltage rise above V_{IT+}.
VDD	2	2	I	**Input Supply Voltage.** TPS3840 monitors VDD voltage
GND	3	3	_	**Ground**
$\overline{MR}$ / NC	4	4	I	**Manual Reset**. Pull this pin to a logic low ($V_{\overline{MR}_L}$) to assert a reset signal in the output pin. After the $\overline{MR}$ pin is left floating or pull to V_{MR_H} the output goes to the nominal state after the reset delay time(t_D) expires. **$\overline{MR}$ can be left floating when not in use. NC stands for "No Connection" or floating.**
CT	5	5	-	**Capacitor Time Delay Pin**. The CT pin offers a user-programmable delay time. Connect an external capacitor on this pin to adjust time delay. When not in use leave pin floating for the smallest fixed time delay.

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8 Specifications

8.1 Absolute Maximum Ratings

over operating free-air temperature range, unless otherwise noted(1)

		MIN	MAX	UNIT
Voltage	VDD	–0.3	12	V
	$\overline{\text{RESET}}$ (TPS3840PL)	–0.3	V_{DD} + 0.3	
	RESET (TPS3840PH)	–0.3	V_{DD} + 0.3	
	$\overline{\text{RESET}}$ (TPS3840DL)	–0.3	12	
	$\overline{\text{MR}}$(2)	–0.3	12	
	CT	–0.3	5.5	
Current	$\overline{\text{RESET}}$ pin and RESET pin		±70	mA
Temperature(3)	Operating junction temperature, T_J	–40	150	°C
	Storage, T_{stg}	–65	150	

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) If the logic signal driving MR is less than V_{DD}, then additional current flows into V_{DD} and out of MR. V_{MR} should not be higher than V_{DD}.
(3) As a result of the low dissipated power in this device, it is assumed that $T_J = T_A$.

8.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	± 2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	± 750	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

8.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{DD}	Input supply voltage	1.5		10	V
$V_{\overline{\text{RESET}}}$, V_{RESET}	$\overline{\text{RESET}}$ pin and RESET pin voltage	0		10	V
$I_{\overline{\text{RESET}}}$, I_{RESET}	$\overline{\text{RESET}}$ pin and RESET pin current	0		±5	mA
T_J	Junction temperature (free air temperature)	–40		125	°C
$V_{\overline{\text{MR}}}$(1)	Manual reset pin voltage	0		V_{DD}	V

(1) If the logic signal driving MR is less than V_{DD}, then additional current flows into V_{DD} and out of MR. V_{MR} should not be higher than V_{DD}.

8.4 Thermal Information

THERMAL METRIC(1)		TPS3840 DBV (SOT23-5) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	187.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	109.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	92.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	35.4	°C/W
ψ_{JB}	Junction-to-board characterization parameter	92.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

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8.5 Electrical Characteristics

At 1.5 V ≤ V_{DD} ≤ 10 V, CT = $\overline{MR}$ = Open, $\overline{RESET}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to VDD, output reset load (C_{LOAD}) = 10 pF and over the operating free-air temperature range – 40°C to 125°C, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMMON PARAMETERS						
V_{DD}	Input supply voltage		1.5		10	V
V_{IT-}	Negative-going input threshold accuracy(1)	-40°C to 125°C	–1.5	1	1.5	%
V_{HYS}	Hysteresis on V_{IT-} pin	V_{IT-} = 3.1 V to 4.9 V	175	200	225	mV
V_{HYS}	Hysteresis on V_{IT-} pin	V_{IT-} = 1.6 V to 3.0 V	75	100	125	mV
I_{DD}	Supply current into VDD pin	VDD = 1.5 V < V_{DD} < 10 V VDD > V_{IT+}(2) T_A = -40°C to 125°C		300	700	nA
$V_{\overline{MR}_L}$	Manual reset logic low input(3)				600	mV
$V_{\overline{MR}_H}$	Manual reset logic high input(3)		0.7V_{DD}			V
$R_{\overline{MR}}$	Manual reset internal pull-up resistance			100		kΩ
R_{CT}	CT pin internal resistance		350	500	650	kΩ
TPS3840PL (Push-Pull Active-Low)						
V_{POR}	Power on Reset Voltage(4)	$V_{OL(max)}$ = 200 mV $I_{OUT(Sink)}$ = 200 nA			300	mV
V_{OL}	Low level output voltage	1.5 V < V_{DD} < 5 V V_{DD} < V_{IT-} $I_{OUT(Sink)}$ = 2 mA			200	mV
V_{OH}	High level output voltage	1.5 V < V_{DD} < 5 V V_{DD} > V_{IT+}(2) $I_{OUT(Source)}$) = 2 mA	0.8V_{DD}			V
		5 V < V_{DD} < 10 V V_{DD} > V_{IT+}(2) $I_{OUT(Source)}$ = 5 mA	0.8V_{DD}			V
TPS3840PH (Push-Pull Active-High)						
V_{POR}	Power on Reset Voltage(4)	V_{OH}, $I_{OUT(Source)}$ = 500 nA			950	mV
V_{OL}	Low level output voltage	1.5 V < V_{DD} < 5 V V_{DD} > V_{IT+}(2) $I_{OUT(Sink)}$ = 2 mA			200	mV
		1.5 V < V_{DD} < 5 V V_{DD} > V_{IT+}(2) $I_{OUT(Sink)}$ = 5 mA			200	mV
V_{OH}	High level output voltage	1.5 V < V_{DD} < 5 V, V_{DD} < V_{IT-}, $I_{OUT(Source)}$ = 2 mA	0.8V_{DD}			V
TPS3840DL(Open-Drain)						
V_{POR}	Power on Reset Voltage(4)	$V_{OL(max)}$ = 0.2 V $I_{OUT\ (Sink)}$ = 5.6 uA			950	mV
V_{OL}	Low level output voltage	1.5 V < V_{DD} < 5 V V_{DD} < V_{IT-} $I_{OUT(Sink)}$ = 2 mA			200	mV
$I_{lkg(OD)}$	Open-Drain output leakage current	$\overline{RESET}$ pin in High Impedance, V_{DD} = V_{RESET} = 5.5 V V_{IT+} < V_{DD}			90	nA

(1) V_{IT-} threshold voltage range from 1.6 V to 4.9 V in 100 mV steps, for released versions see Device Voltage Thresholds table.
(2) V_{IT+} = V_{HYS} + V_{IT-}
(3) If the logic signal driving $\overline{MR}$ is less than VDD, then additional current flows into VDD and out of $\overline{MR}$
(4) V_{POR} is the minimum V_{DD} voltage level for a controlled output state. V_{DD} slew rate ≤ 100mV/µs

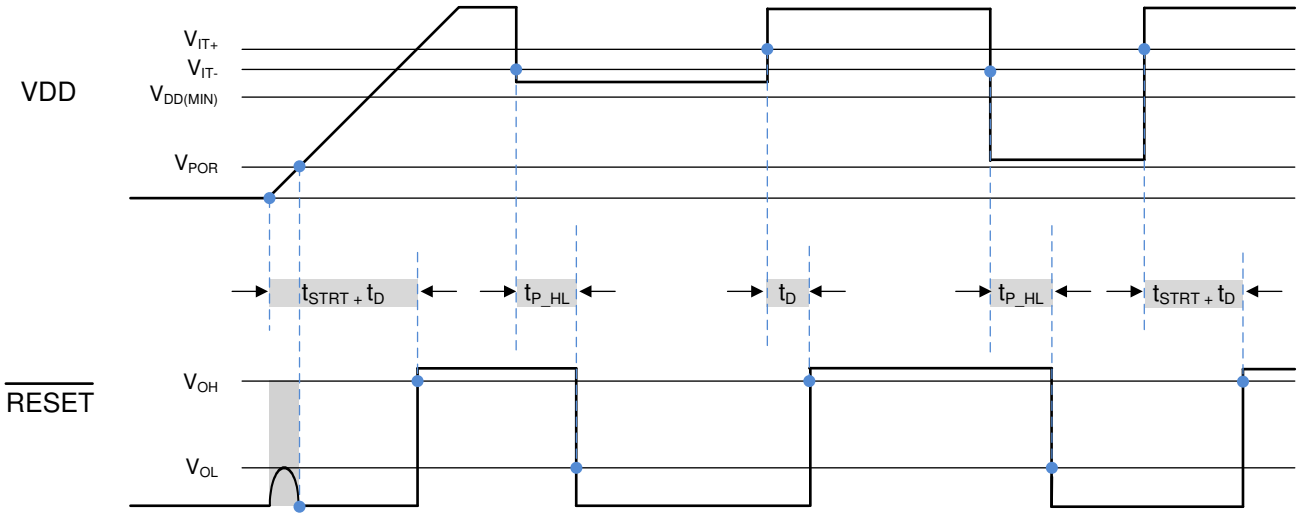
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8.6 Timing Requirements

At 1.5 V ≤ V_{DD} ≤ 10 V, CT = $\overline{MR}$ = Open, $\overline{RESET}$ pull-up resistor ($R_{pull-up}$) = 100 kΩ to VDD, output reset load (C_{LOAD}) = 10 pF and over the operating free-air temperature range – 40°C to 125°C, VDD slew rate < 100mV / us, unless otherwise noted. Typical values are at T_J = 25°C.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STRT}	Startup Delay(1)	CT pin open	100	220	350	µs
t_{P_HL}	Propagation detect delay for VDD falling below V_{IT-}	V_{DD} = V_{IT+} to (V_{IT-}) - 10%(2)		15	30	µs
t_D	Reset time delay	CT pin = open			50	µs
		CT pin = 10 nF		6.2		ms
		CT pin = 1 µF		619		ms
t_{GI_VIT-}	Glitch immunity V_{IT-}	5% V_{IT-} overdrive(3)		10		µs
t_{MR_PW}	$\overline{MR}$ pin pulse duration to initiate reset			300		ns
t_{MR_RES}	Propagation delay from $\overline{MR}$ low to reset	V_{DD} = 4.5 V, $\overline{MR}$ < $V_{\overline{MR}_L}$		700		ns
t_{MR_tD}	Delay from release $\overline{MR}$ to deasert reset	V_{DD} = 4.5 V, $\overline{MR}$ = $V_{\overline{MR}_L}$ to $V_{\overline{MR}_H}$		t_D		ms

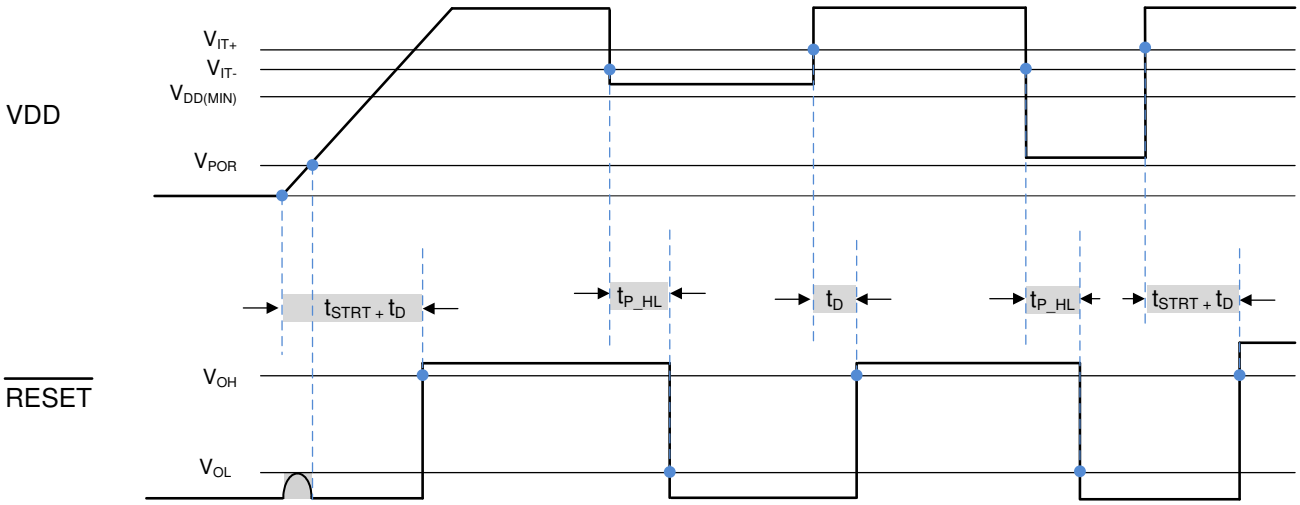
(1) When VDD starts from less than the specified minimum V_{DD} and then exceeds V_{IT+}, reset is release after the startup delay (t_{STRT}), a capacitor at CT pin will add t_D delay to t_{STRT} time
(2) t_{P_HL} measured from threhold trip point (V_{IT-}) to V_{OL} for active low variants and V_{OH} for active high variants.
(3) Overdrive % = [(V_{DD}/ V_{IT-}) - 1] × 100%



(1) $t_{D\ (no\ cap)}$ is included in t_{STRT} time delay. If t_D delay is programmed by an external capacitor connected to CT pin then t_D programmed time will be added to the startup time, VDD slew rate = 100 mV / µs.
(2) Open-Drain timing diagram assumes pull-up resistor is connected to $\overline{RESET}$
(3) $\overline{RESET}$ output is undefined when VDD is < V_{POR}

図 3. Timing Diagram TPS3840DL (Open-Drain Active-Low)

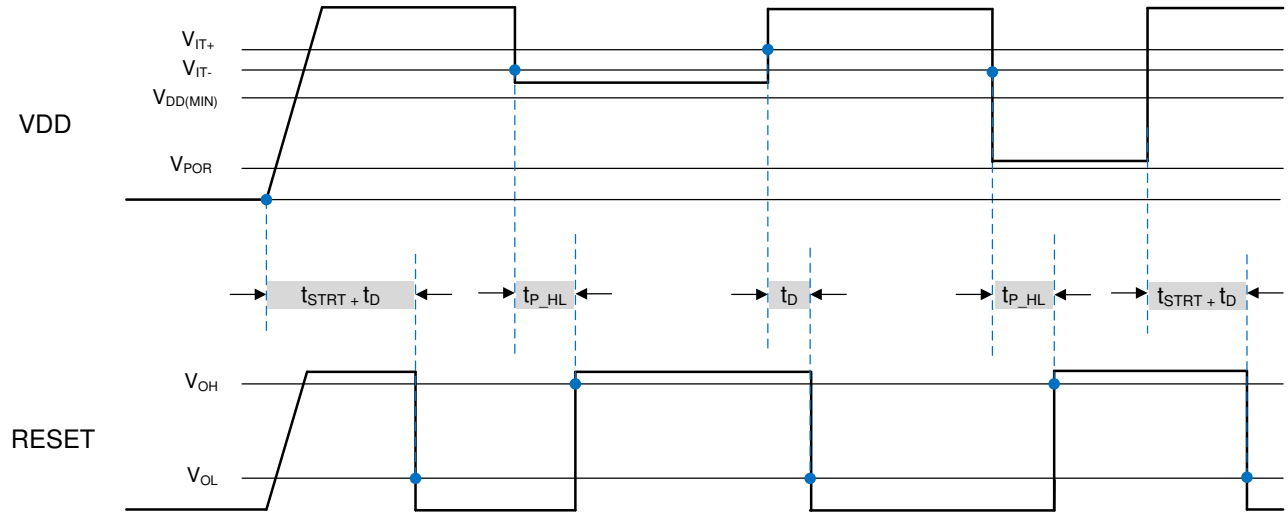
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(4) $t_{D\ (no\ cap)}$ is included in t_{STRT} time delay. If t_D delay is programmed by an external capacitor connected to CT pin, then t_D programmed time will be added to the startup time. VDD slew rate = 100 mV / µs.

(5) $\overline{\text{RESET}}$ output is undefined when VDD < V_{POR} and limited to V_{OL} for VDD slew rate = 100 mV / µs

図 4. Timing Diagram TPS3840PL (Push-Pull Active-Low)



(6) $t_{D\ (no\ cap)}$ is included in t_{STRT} time delay. If t_D delay is programmed by an external capacitor connected to CT pin, then t_D programmed time will be added to the total startup time. VDD slew rate = 100 mV / µs.

図 5. Timing Diagram TPS3840PH (Push-Pull Active-High)

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8.7 Typical Characteristics

Typical characteristics show the typical performance of the TPS3840 device. Test conditions are T_J = 25°C, V_{DD} = 3.3 V, $R_{pull-up}$ = 100 kΩ, C_{Load} = 50 pF, unless otherwise noted.

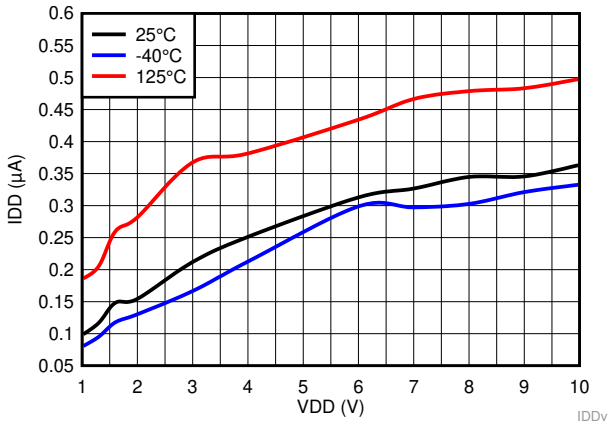


図 6. Supply Current vs Supply Voltage for TPS3840DL49

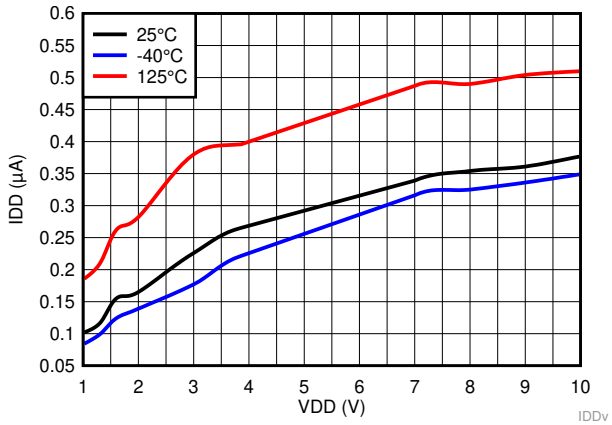


図 7. Supply Current vs Supply Voltage for TPS3840PL49

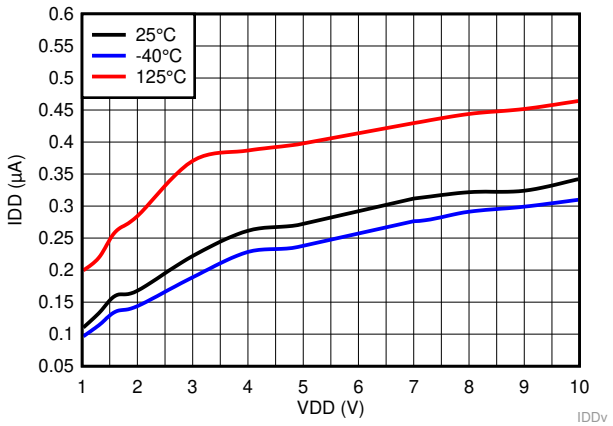


図 8. Supply Current vs Supply Voltage for TPS3840PH49

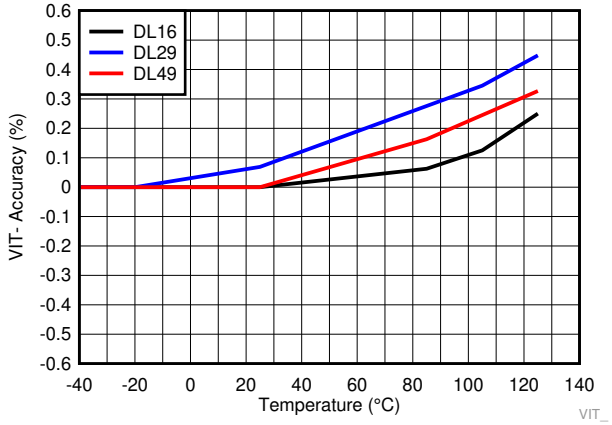


図 9. Negative-going Input Threshold Accuracy over Temperature for TPS3840DLXX

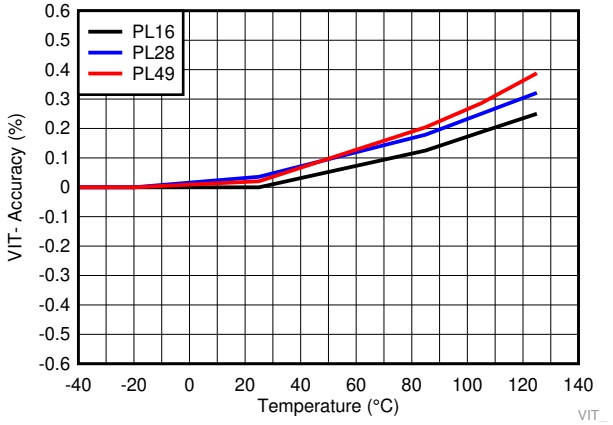


図 10. Negative-going Input Threshold Accuracy over Temperature for TPS3840PLXX

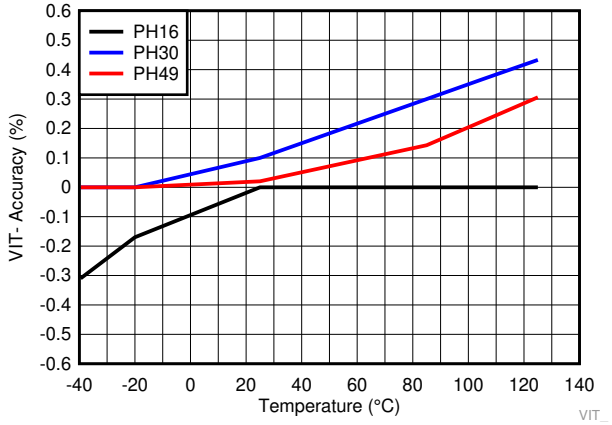


図 11. Negative-going Input Threshold Accuracy over Temperature for TPS3840PHXX

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Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3840 device. Test conditions are T_J = 25°C, V_{DD} = 3.3 V, $R_{pull-up}$ = 100 kΩ, C_{Load} = 50 pF, unless otherwise noted.

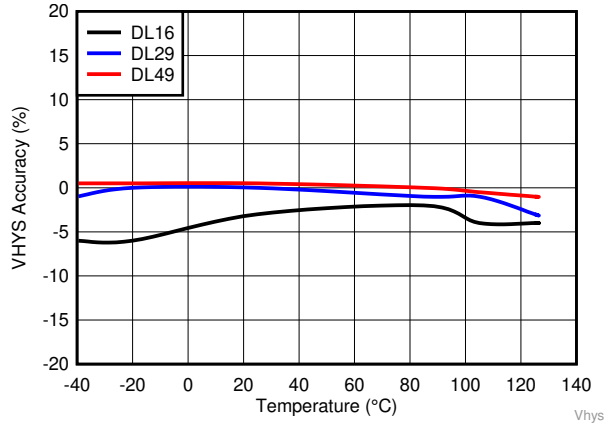


図 12. Input Threshold V_{IT-} Hysteresis Accuracy for TPS3840DLXX

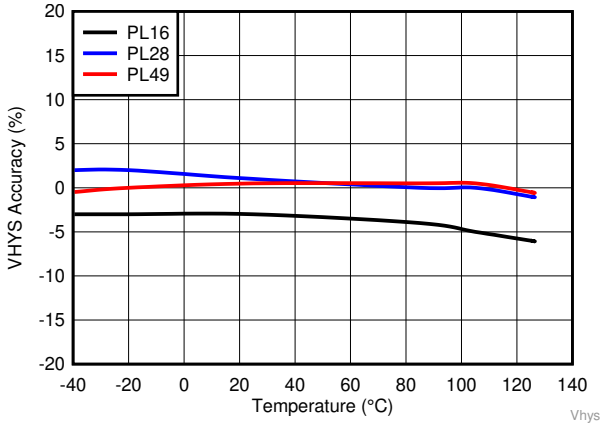


図 13. Input Threshold V_{IT-} Hysteresis Accuracy for TPS3840PLXX

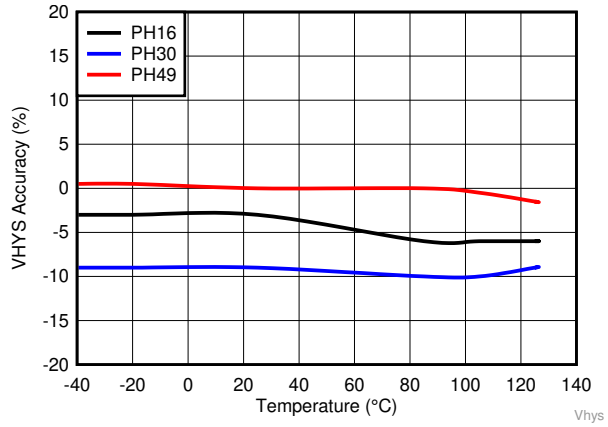


図 14. Input Threshold V_{IT-} Hysteresis Accuracy for TPS3840PHXX

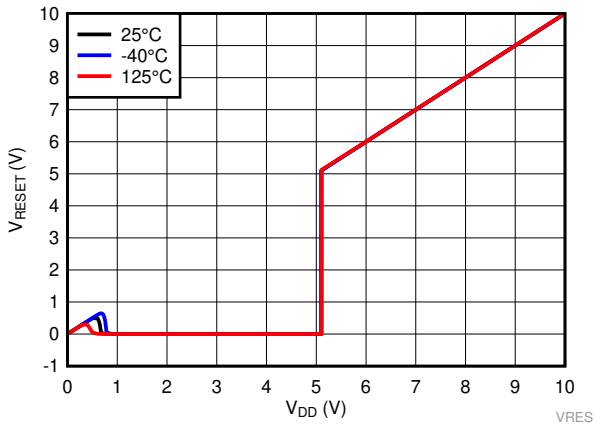


図 15. Output Voltage vs Input Voltage for TPS3840DL49

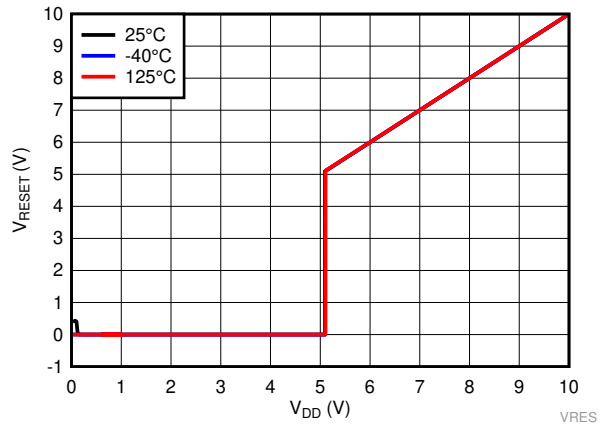


図 16. Output Voltage vs Input Voltage for TPS3840PL49

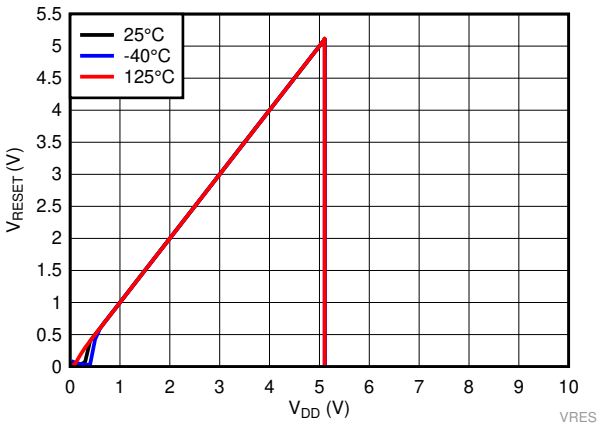


図 17. Output Voltage vs Input Voltage for TPS3840PH49

Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3840 device. Test conditions are T_J = 25°C, V_{DD} = 3.3 V, $R_{pull-up}$ = 100 kΩ, C_{Load} = 50 pF, unless otherwise noted.

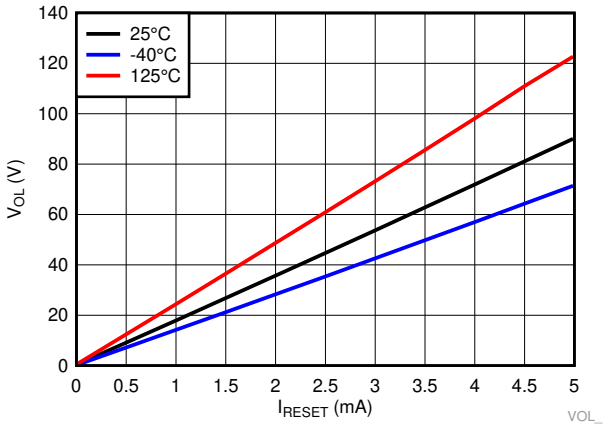


図 18. Low Level Output Voltage vs I_{RESET} for TPS3840DL49

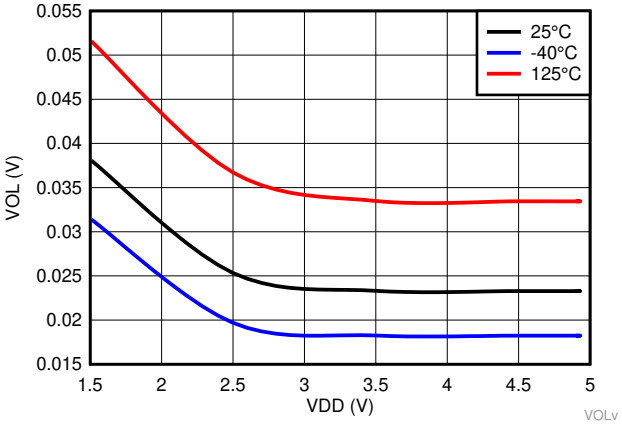


図 19. Low Level Output Voltage vs V_{DD} for TPS3840DL49

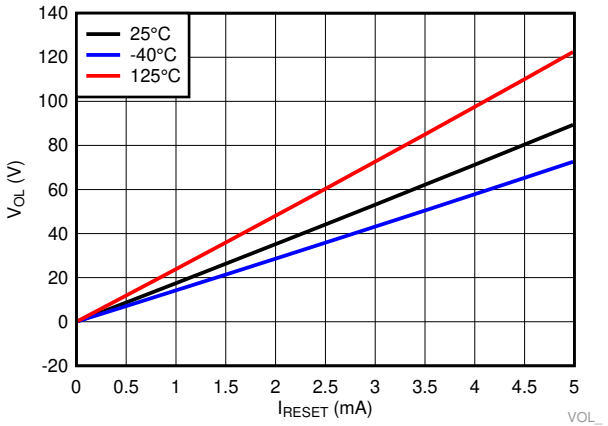


図 20. Low Level Output Voltage vs I_{RESET} for TPS3840PL49

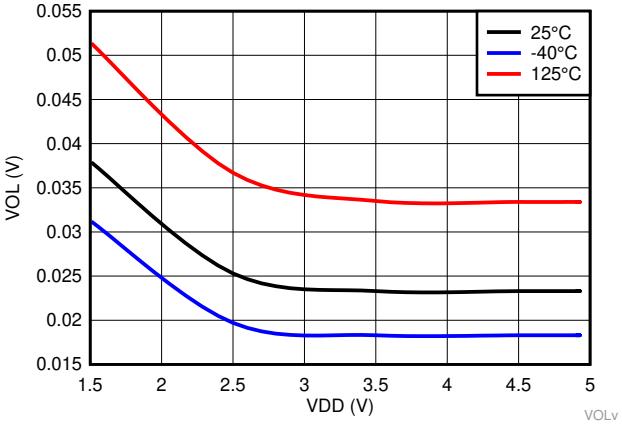


図 21. Low Level Output Voltage vs VDD for TPS3840PL49

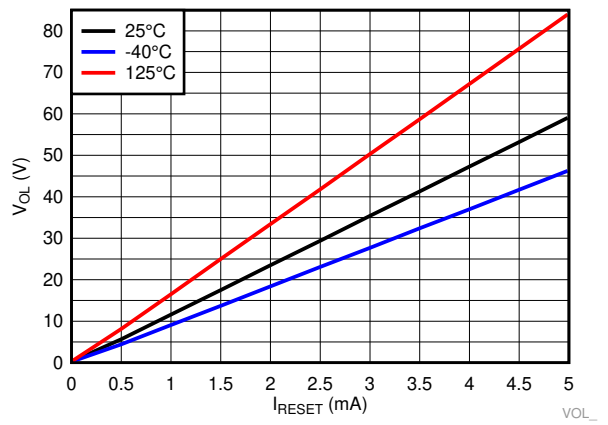


図 22. Low Level Output Voltage vs I_{RESET} for TPS3840PH49

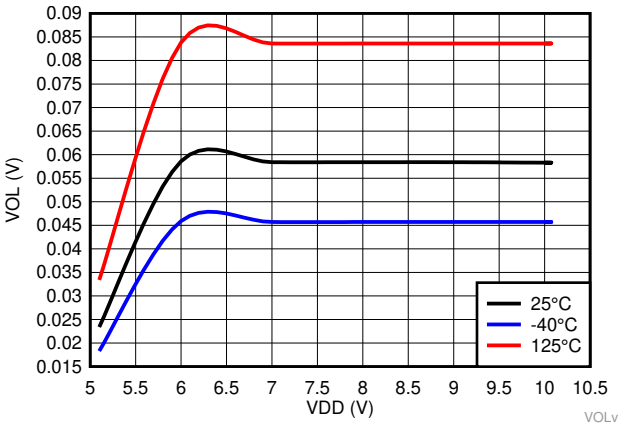


図 23. Low Level Output Voltage vs VDD for TPS3840PH49

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Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3840 device. Test conditions are T_J = 25°C, V_{DD} = 3.3 V, $R_{pull-up}$ = 100 kΩ, C_{Load} = 50 pF, unless otherwise noted.

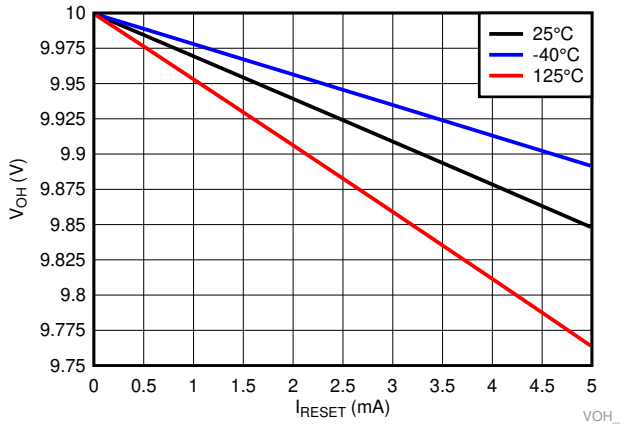


図 24. High Level Output Voltage vs I_{RESET} for TPS3840PL49

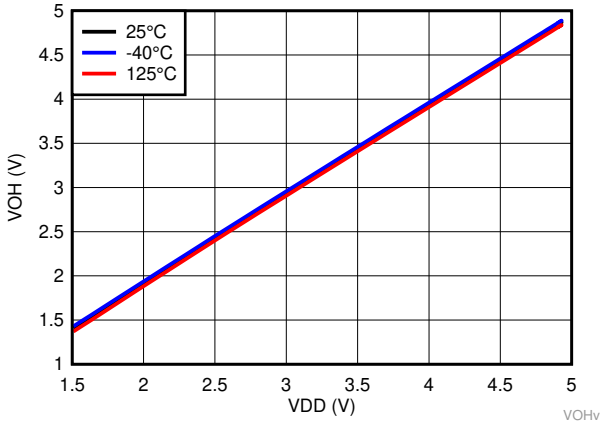


図 25. High Level Output Voltage over Temperature for TPS3840PL49

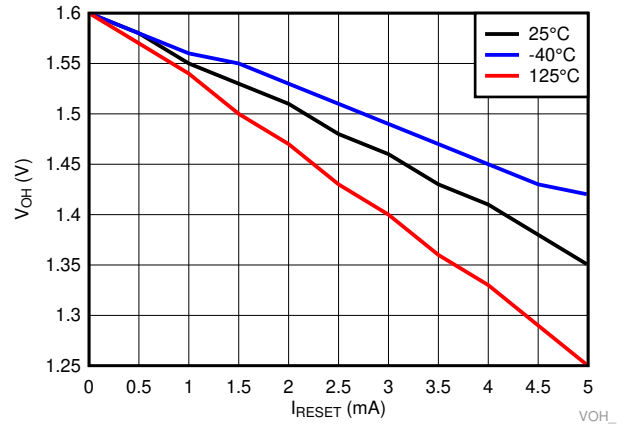


図 26. High Level Output Voltage vs I_{RESET} for TPS3840PH49

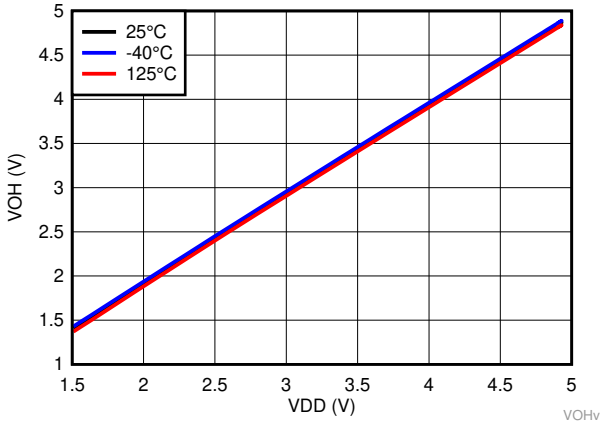


図 27. High Level Output Voltage over Temperature for TPS3840PH49

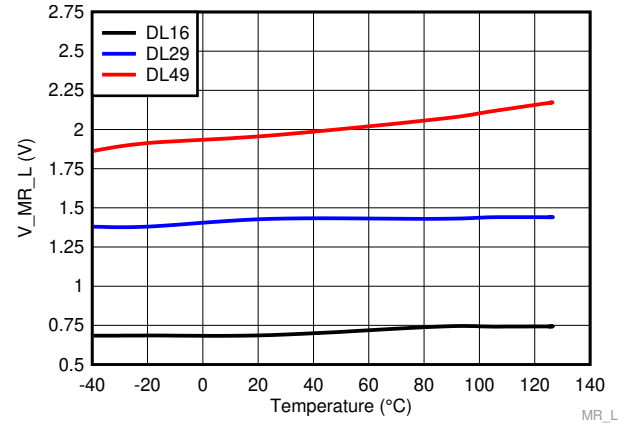


図 28. Manual Reset Logic Low Voltage Threshold over Temperature for TPS3840DLXX

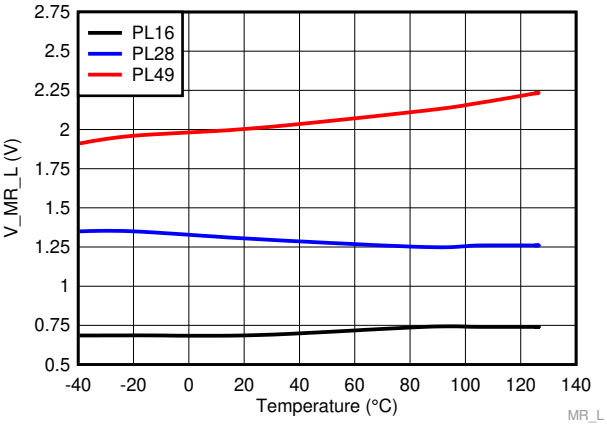


図 29. Manual Reset Logic Low Voltage Threshold over Temperature for TPS3840PLXX

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Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3840 device. Test conditions are T_J = 25°C, V_{DD} = 3.3 V, $R_{pull-up}$ = 100 kΩ, C_{Load} = 50 pF, unless otherwise noted.

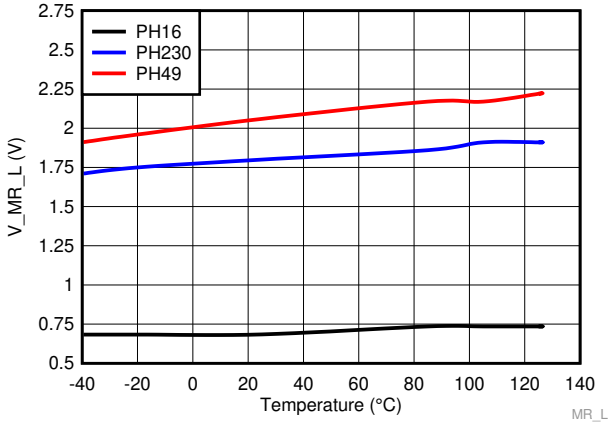


図 30. Manual Reset Logic Low Voltage Threshold over Temperature for TPS3840PHXX

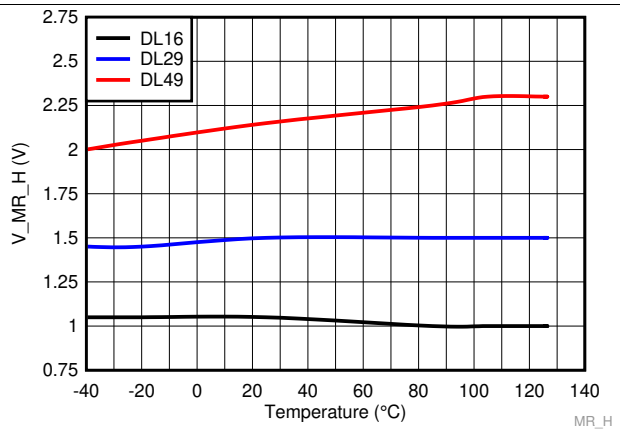


図 31. Manual Reset Logic High Voltage Threshold over Temperature for TPS3840DLXX

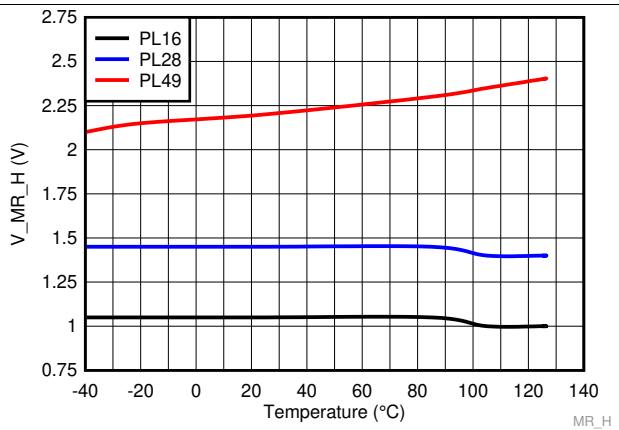


図 32. Manual Reset Logic High Voltage Threshold over Temperature for TPS3840PLXX

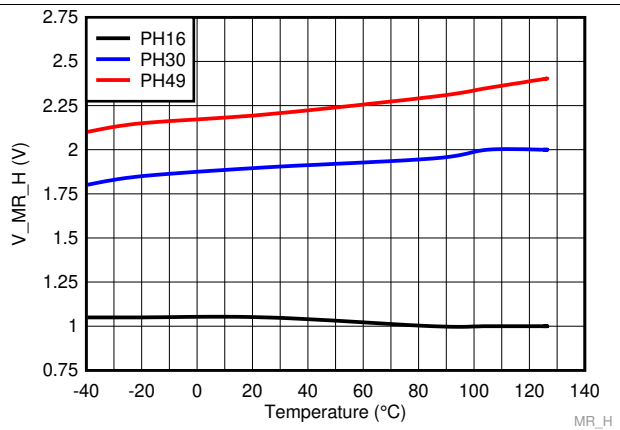


図 33. Manual Reset Logic High Voltage Threshold over Temperature for TPS3840PHXX

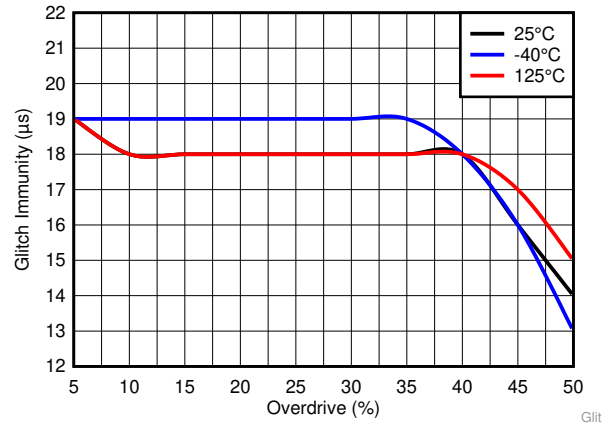


図 34. Glitch Immunity on V_{IT-} vs Overdrive (Data Taken with TPS3840PL28)

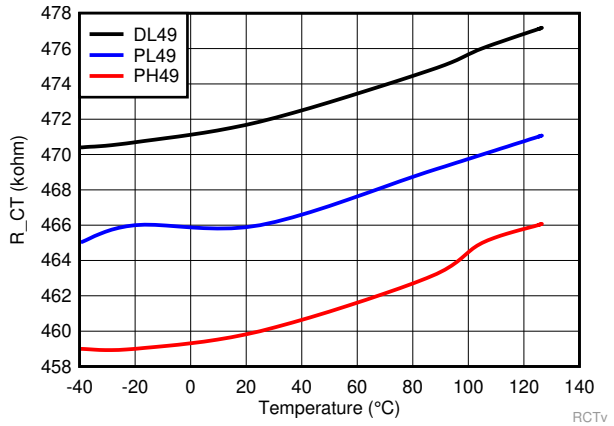


図 35. CT Pin Internal Resistance over Temperature

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Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3840 device. Test conditions are T_J = 25°C, V_{DD} = 3.3 V, $R_{pull-up}$ = 100 kΩ, C_{Load} = 50 pF, unless otherwise noted.

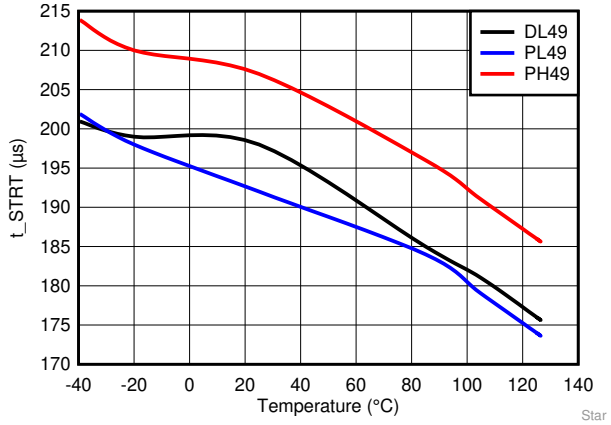


図 36. Startup Delay over Temperature

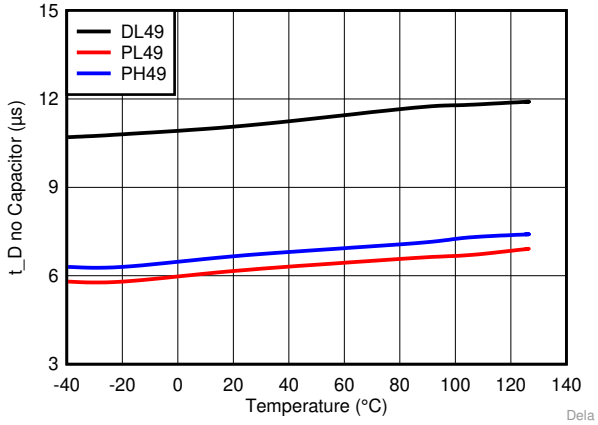


図 37. Reset Time Delay with No Capacitor over Temperature

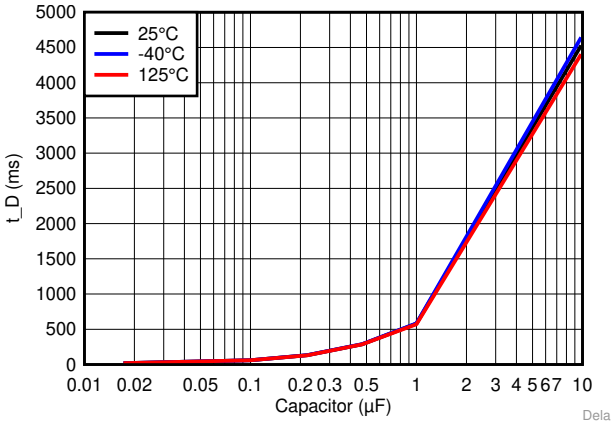


図 38. Reset Time Delay vs Capacitor Value (Data Taken with TPS3840PL16)

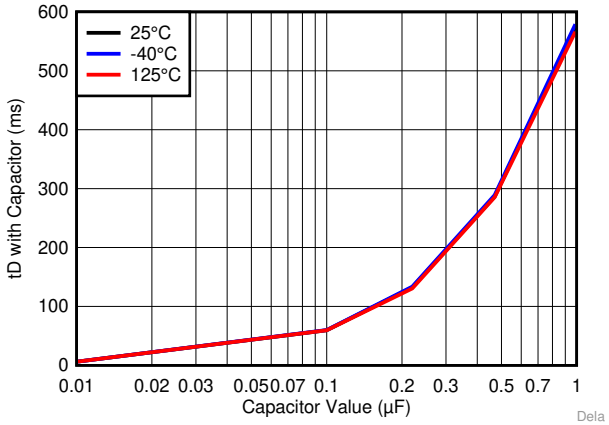


図 39. Reset Time Delay vs Small Capacitor Values (Data Taken with TPS3840PL16)

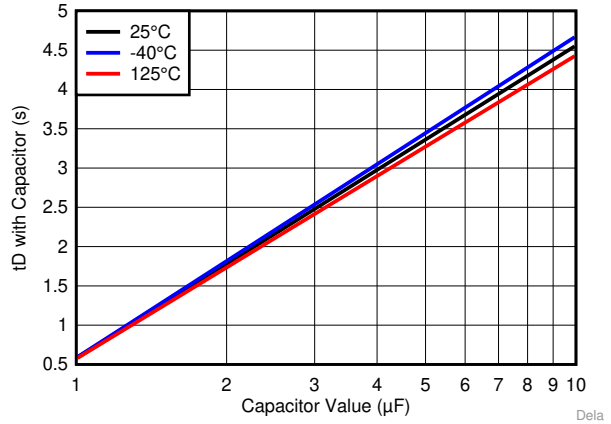


図 40. Reset Time Delay vs Large Capacitor Values (Data Taken with TPS3840PL16)

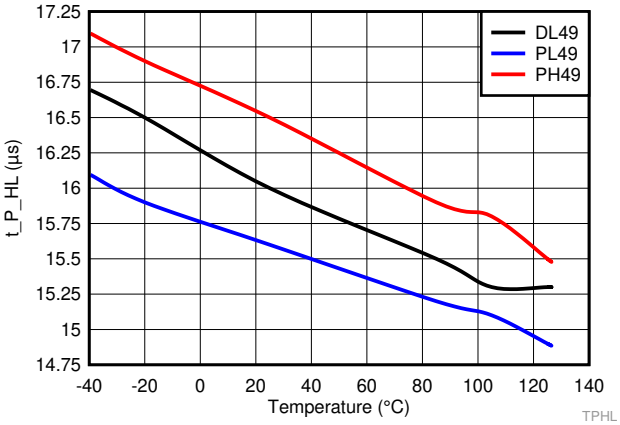


図 41. Propagation Detect Time Delay for VDD Falling Below V_{IT-} (High-to-Low) over Temperature

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Typical Characteristics (continued)

Typical characteristics show the typical performance of the TPS3840 device. Test conditions are T_J = 25°C, V_{DD} = 3.3 V, $R_{pull-up}$ = 100 kΩ, C_{Load} = 50 pF, unless otherwise noted.

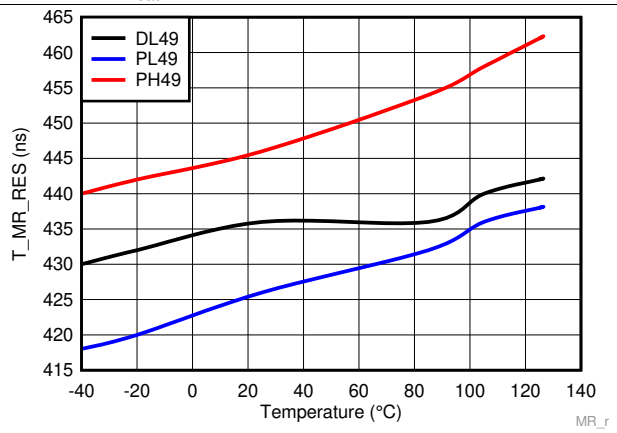


図 42. Propagation Time Delay from $\overline{MR}$ Asserted to Reset over Temperature

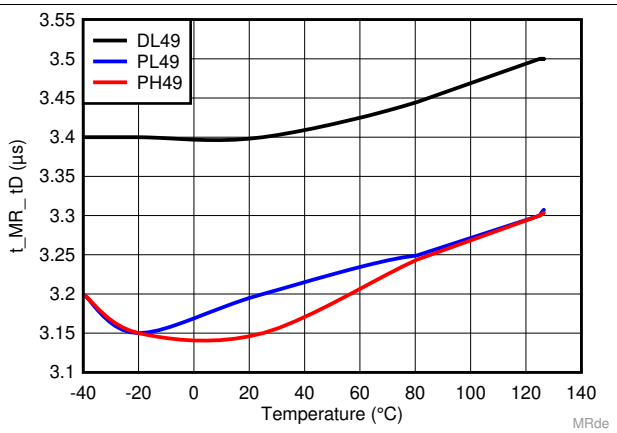


図 43. Propagation Time Delay from $\overline{MR}$ Release to Deasserted Reset over Temperature

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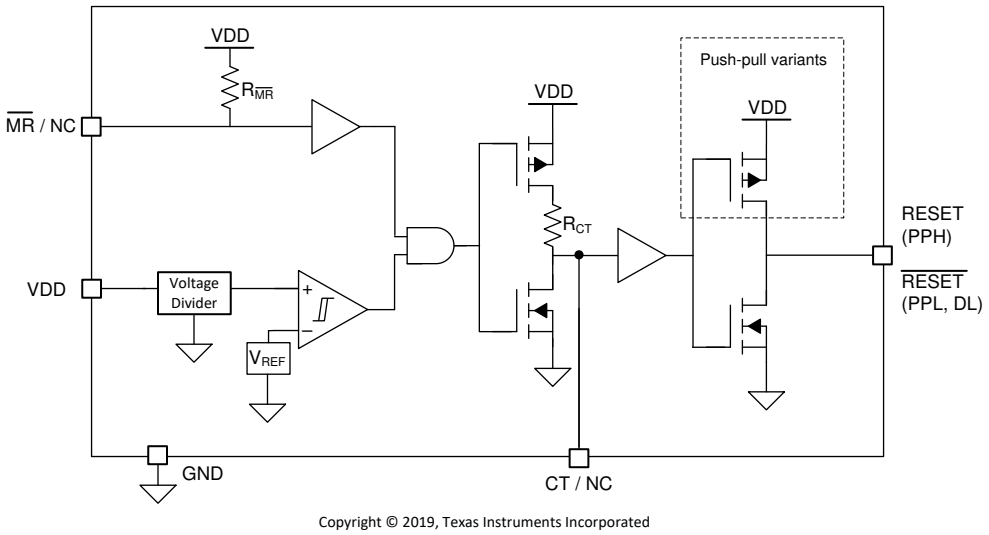
9 Detailed Description

9.1 Overview

The TPS3840 is a family of wide VDD and nano-quiescent current voltage detectors with fixed threshold voltage. TPS3840 features include programable reset time delay using external capacitor, active-low manual reset, 1% typical monitor threshold accuracy with hysteresis and glitch immunity.

Fixed negative threshold voltages (V_{IT-}) can be factory set from 1.6 V to 4.9 V (see the *Device Comparison Table* for available options). TPS3840 is available in SOT-23 5 pin industry standard package.

9.2 Functional Block Diagram



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9.3 Feature Description

9.3.1 Input Voltage (VDD)

VDD pin is monitored by the internal comparator to indicate when VDD falls below the fixed threshold voltage. VDD also functions as the supply for the internal bandgap, internal regulator, state machine, buffers and other control logic blocks. Good design practice involve placing a 0.1 uF to 1 uF bypass capacitor at VDD input for noisy applications to ensure enough charge is available for the device to power up correctly.

Feature Description (continued)

9.3.1.1 VDD Hysteresis

The internal comparator has built-in hysteresis to avoid erroneous output reset release. If the voltage at the VDD pin falls below V_{IT-} the output reset is asserted. When the voltage at the VDD pin goes above V_{IT-} plus hysteresis (V_{HYS}) the output reset is deasserted after t_D delay.

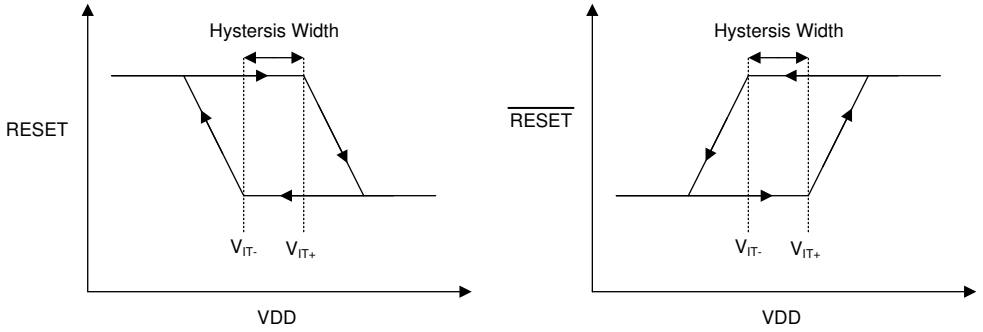


図 44. Hysteresis Diagram

9.3.1.2 VDD Transient Immunity

The TPS3840 is immune to quick voltage transients or excursion on VDD. Sensitivity to transients depends on both pulse duration and overdrive. Overdrive is defined by how much VDD deviates from the specified threshold. Threshold overdrive is calculated as a percent of the threshold in question, as shown in 式 1.

$$\text{Overdrive} = | (V_{DD} / V_{IT-} - 1) \times 100\% | \quad (1)$$

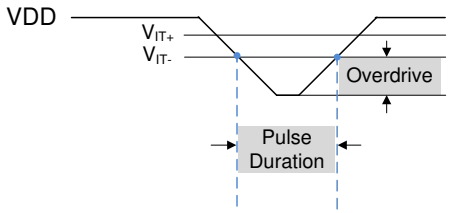


図 45. Overdrive vs Pulse Duration

9.3.2 User-Programmable Reset Time Delay

The reset time delay can be set to a minimum value of 50 µs by leaving the CT pin floating, or a maximum value of approximately 6.2 seconds by connecting 10 µF delay capacitor. The reset time delay (t_D) can be programmed by connecting a capacitor no larger than 10 µF between CT pin and GND.

The relationship between external capacitor (C_{CT_EXT}) in µF at CT pin and the time delay (t_D) in seconds is given by 式 2.

$$t_D = -\ln (0.29) \times R_{CT} \times C_{CT_EXT} + t_D \text{ (no cap)} \quad (2)$$

式 2 is simplified to 式 3 by plugging R_{CT} and $t_{D(no\ cap)}$ given in *Electrical Characteristics* section:

$$t_D = 618937 \times C_{CT_EXT} + 50\ \mu s \quad (3)$$

式 4 solves for external capacitor value (C_{CT_EXT}) in units of µF where t_D is in units of seconds

$$C_{CT_EXT} = (t_D - 50\ \mu s) \div 618937 \quad (4)$$

The reset delay varies according to three variables: the external capacitor variance (C_{CT}), CT pin internal resistance (R_{CT}) provided in the Electrical Characteristics table, and a constant. The minimum and maximum variance due to the constant is shown in Equation 5 and Equation 6.

$$t_{D\ (minimum)} = -\ln (0.36) \times R_{CT\ (min)} \times C_{CT\ (min)} + t_{D\ (no\ cap,\ min)} \quad (5)$$

$$t_{D\ (maximum)} = -\ln (0.26) \times R_{CT\ (max)} \times C_{CT\ (max)} + t_{D\ (no\ cap,\ max)} \quad (6)$$

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Feature Description (continued)

The recommended maximum delay capacitor for the TPS3840 is limited to 10 µF as this ensures there is enough time for the capacitor to fully discharge when the reset condition occurs. When a voltage fault occurs, the previously charged up capacitor discharges, and if the monitored voltage returns from the fault condition before the delay capacitor discharges completely, the delay capacitor will begin charging from a voltage above zero and the reset delay will be shorter than expected. Larger delay capacitors can be used so long as the capacitor has enough time to fully discharge during the duration of the voltage fault.

9.3.3 Manual Reset ($\overline{MR}$) Input

The manual reset ($\overline{MR}$) input allows a processor GPIO or other logic circuits to initiate a reset. A logic low on $\overline{MR}$ with pulse duration longer than $t_{\overline{MR}_RES}$ will causes reset output to assert. After $\overline{MR}$ returns to a logic high ($V_{\overline{MR}_H}$) and VDD is above V_{IT+}, reset is deasserted after the user programmed reset time delay (t_D) expires.

If $\overline{MR}$ is not controlled externally, then $\overline{MR}$ can be left disconnected. If the logic signal controlling $\overline{MR}$ is less than VDD, then additional current flows from VDD into $\overline{MR}$ internally. For minimum current consumption, drive $\overline{MR}$ to either VDD or GND. $V_{\overline{MR}}$ should not be higher than VDD voltage.

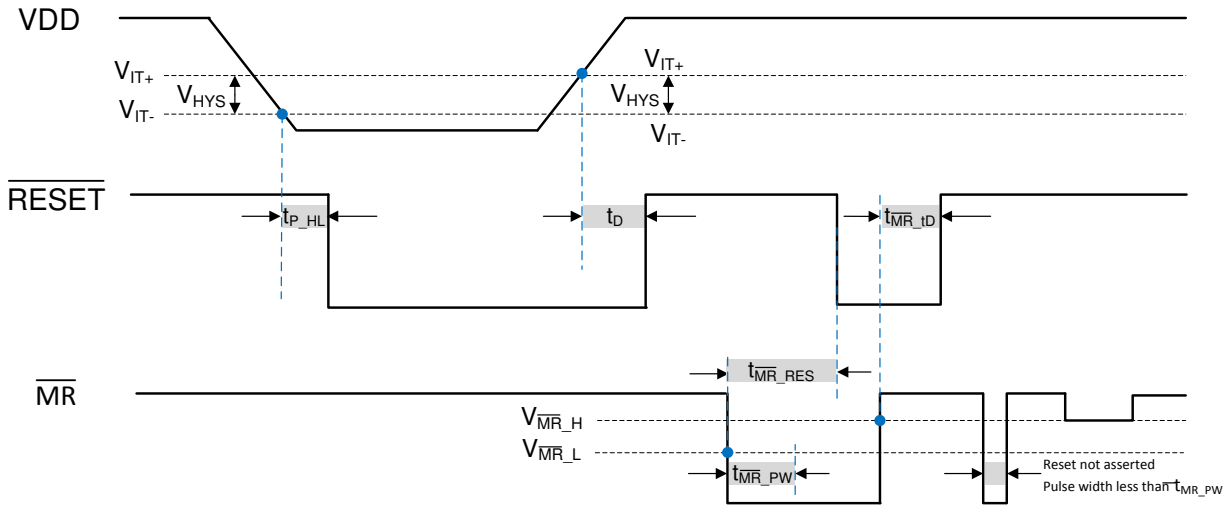


図 46. Timing Diagram $\overline{MR}$ and $\overline{RESET}$ (TPS3840DL)

9.3.4 Output Logic

9.3.4.1 $\overline{RESET}$ Output, Active-Low

$\overline{RESET}$ (Active-Low) applies to TPS3840D**L** (Open-Drain) and TPS3840P**L** (Push-Pull) hence the "**L**" in the device name. $\overline{RESET}$ remains high (deasserted) as long as VDD is above the negative threshold (V_{IT-}) and the $\overline{MR}$ pin is floating or above $V_{\overline{MR}_H}$. If VDD falls below the negative threshold (V_{IT-}) or if $\overline{MR}$ is driven low, then $\overline{RESET}$ is asserted.

When $\overline{MR}$ is again logic high or floating and VDD rise above V_{IT+}, the delay circuit will hold $\overline{RESET}$ low for the specified reset time delay (t_D). When the reset time delay has elapsed, the $\overline{RESET}$ pin goes back to logic high voltage (V_{OH}).

The TPS3840DL (Open-Drain) version, denoted with "**D**" in the device name, requires a pull-up resistor to hold $\overline{RESET}$ pin high. Connect the pull-up resistor to the desired pull-up voltage source and $\overline{RESET}$ can be pulled up to any voltage up to 10 V independent of the VDD voltage. To ensure proper voltage levels, give some consideration when choosing the pull-up resistor values. The pull-up resistor value determines the actual V_{OL}, the output capacitive loading, and the output leakage current ($I_{LKG(OD)}$).

The Push-Pull variants (TPS3840**P**L and TPS3840**P**H), denoted with "**P**" in the device name, does not require a pull-up resistor

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Feature Description (continued)

9.3.4.2 RESET Output, Active-High

RESET (active-high), denoted with no bar above the pin label, applies only to TPS3840PH push-pull active-high version. RESET remains low (deasserted) as long as VDD is above the threshold (V_{IT-}) and the manual reset signal ($\overline{MR}$) is logic high or floating. If VDD falls below the negative threshold (V_{IT-}) or if $\overline{MR}$ is driven low, then RESET is asserted driving the RESET pin to high voltage (V_{OH}).

When $\overline{MR}$ is again logic high and VDD is above V_{IT+} the delay circuit will hold RESET high for the specified reset time delay (t_D). When the reset time delay has elapsed, the RESET pin goes back to low voltage (V_{OL})

9.4 Device Functional Modes

表 1 summarizes the various functional modes of the device. Logic high is represented by "H" and logic low is represented by "L".

表 1. Truth Table

VDD	$\overline{MR}$	RESET	$\overline{RESET}$
VDD < V_{POR}	Ignored	Undefined	Undefined
V_{POR} < V_{DD} < V_{IT-} (1)	Ignored	H	L
VDD ≥ V_{IT-}	L	H	L
VDD ≥ V_{IT-}	H	L	H
VDD ≥ V_{IT-}	Floating	L	H

(1) When V_{DD} falls below $V_{DD(MIN)}$, undervoltage-lockout (UVLO) takes effect and output reset is held asserted until V_{DD} falls below V_{POR}.

9.4.1 Normal Operation (V_{DD} > $V_{DD(min)}$)

When VDD is greater than $V_{DD(min)}$, the reset signal is determined by the voltage on the VDD pin with respect to the trip point (V_{IT-}) and the logic state of $\overline{MR}$.

- $\overline{MR}$ high: the reset signal corresponds to VDD with respect to the threshold voltage.
- $\overline{MR}$ low: in this mode, the reset is asserted regardless of the threshold voltage.

9.4.2 VDD Between VPOR and $V_{DD(min)}$

When the voltage on VDD is less than the $V_{DD(min)}$ voltage, and greater than the power-on-reset voltage (V_{POR}), the reset signal is asserted.

9.4.3 Below Power-On-Reset (V_{DD} < V_{POR})

When the voltage on VDD is lower than V_{POR}, the device does not have enough bias voltage to internally pull the asserted output low or high and reset voltage level is undefined.

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10 Application and Implementation

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Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

The following sections describe in detail how to properly use this device, depending on the requirements of the final application.

10.2 Typical Application

10.2.1 Design 1: Dual Rail Monitoring with Power-Up Sequencing

A typical application for the TPS3840 is voltage rail monitoring and power-up sequencing as shown in 図 47. The TPS3840 can be used to monitor any rail above 1.6 V. In this design application, two TPS3840 devices monitor two separate voltage rails and sequences the rails upon power-up. The TPS3840PL30 is used to monitor the 3.3-V main power rail and the TPS3840DL16 is used to monitor the 1.8-V rail provided by the LDO for other system peripherals. The $\overline{\text{RESET}}$ output of the TPS3840PL30 is connected to the ENABLE input of the LDO. A reset event is initiated on either voltage supervisor when the VDD voltage is less than V_{IT-} or when $\overline{\text{MR}}$ is driven low by an external source.

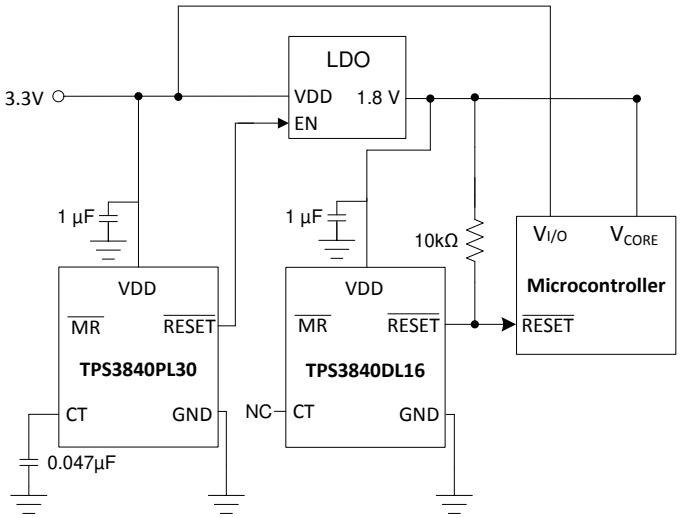


図 47. TPS3840 Voltage Rail Monitor and Power-Up Sequencer Design Block Diagram

Typical Application (continued)

10.2.1.1 Design Requirements

This design requires voltage supervision on two separate rails: 3.3-V and 1.8-V rails. The voltage rail needs to sequence upon power up with the 3.3-V rail coming up first followed by the 1.8-V rail at least 25 ms after.

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Two Rail Voltage Supervision	Monitor 3.3-V and 1.8-V rails	Two TPS3840 devices provide voltage monitoring with 1% accuracy with device options available in 0.1 V variations
Voltage Rail Sequencing	Power up the 3.3-V rail first followed by 1.8-V rail 25 ms after	The CT capacitor on TPS38240PL28 is set to 0.047 µF for a reset time delay of 29 ms typical
Output logic voltage	3.3-V Open-Drain	3.3-V Open-Drain
Maximum device current consumption	1 µA	Each TPS3840 requires 350 nA typical

10.2.1.2 Detailed Design Procedure

The primary constraint for this application is choosing the correct device to monitor the supply voltage of the microprocessor. The TPS3840 can monitor any voltage between 1.6 V and 10 V and is available in 0.1 V increments. Depending on how far away from the nominal voltage rail the user wants the voltage supervisor to trigger determines the correct voltage supervisor variant to choose. In this example, the first TPS3840 triggers when the 3.3-V rail falls to 3.0 V. The second TPS3840 triggers a reset when the 1.8-V rail falls to 1.6 V. The secondary constraint for this application is the reset time delay that must be at least 25 ms to allow the microprocessor, and all other devices using the 3.3-V rail, enough time to startup correctly before the 1.8-V rail is enabled via the LDO. Because a minimum time is required, the user must account for capacitor tolerance. For applications with ambient temperatures ranging from –40°C to +125°C, C_{CT} can be calculated using R_{CT} and solving for C_{CT} in 式 2. Solving 式 2 for 25 ms gives a minimum capacitor value of 0.04 µF which is rounded up to a standard value 0.047 µF to account for capacitor tolerance.

A 1-µF decoupling capacitor is connected to the VDD pin as a good analog design practice. The pull-up resistor is only required for the Open-Drain device variants and is calculated to maintain the $\overline{\text{RESET}}$ current within the ±5 mA limit found in the *Recommended Operating Conditions*: $R_{Pull\text{-}up} = V_{Pull\text{-}up} \div 5$ mA. For this design, a standard 10-kΩ pull-up resistor is selected to minimize current draw when $\overline{\text{RESET}}$ is asserted. Keep in mind the lower the pull-up resistor, the higher V_{OL}. The $\overline{\text{MR}}$ pin can be connected to an external signal if desired or left floating if not used due to the internal pull-up resistor to VDD.

10.2.1.3 Application Curves

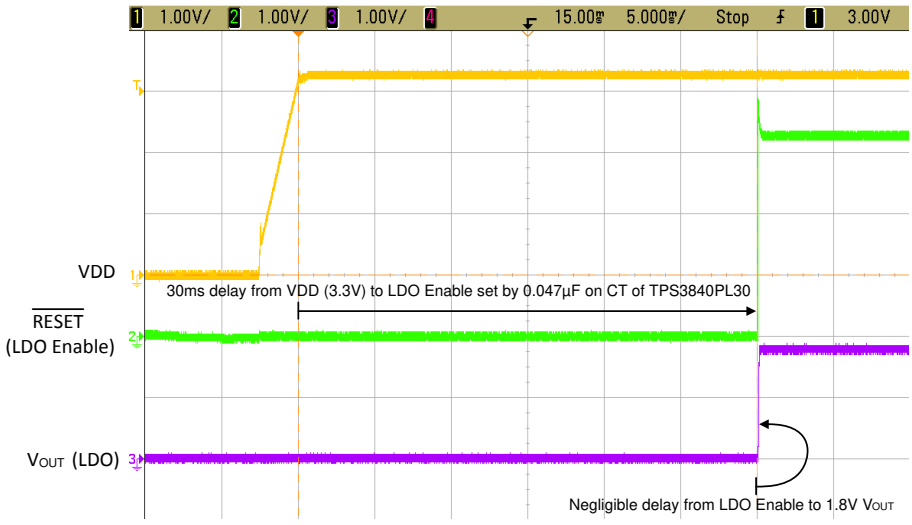


図 48. Startup Sequence Highlighting the Delay Between 3.3V and 1.8V Rails

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10.2.2 Design 2: Battery Voltage and Temperature Monitor

A typical application for the TPS3840 is battery voltage and temperature monitoring. The TPS3840 is offered in active-low or active-high output topologies and can operate above or below the voltage threshold meaning the device can be used as an undervoltage monitor as shown in 図 49 or overvoltage monitor as shown in 図 50. The TPS3840 can be used to monitor any rail above 1.6 V. In this design application, one TPS3840DL30 monitors the 3.3-V battery voltage rail and triggers an active-low reset fault condition if the battery voltage falls below the 3-V threshold. For overvoltage monitoring, another TPS3840DL30 monitors a 2.8-V battery and triggers a logic high at the 3-V threshold plus 100 mV hysteresis so at 3.1 V. Both applications monitor the battery temperature using TMP303, a push-pull, active-high temperature switch. A temperature fault is triggered if the battery temperature falls outside of a defined window temperature range set by the TMP303 variant chosen.

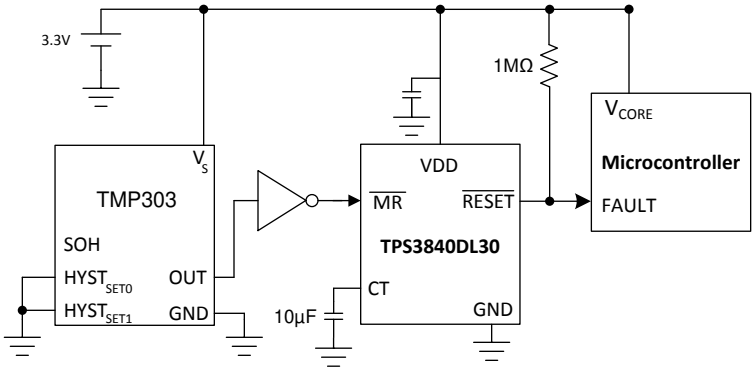


図 49. Low Battery Voltage and Window Temperature Monitoring Solution

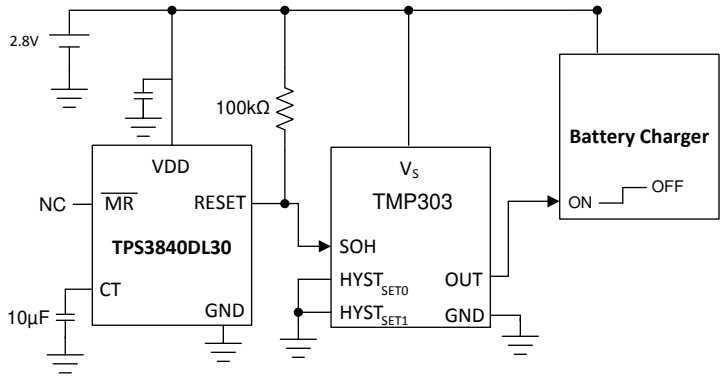


図 50. Overvoltage and Window Temperature Monitoring Solution

10.2.2.1 Design Requirements

This design requires voltage and temperature supervision on a battery voltage rail and the requirements may differ depending on if undervoltage or overvoltage monitoring is required. For this design, both requirements are considered to show the flexibility of the TPS3840 device. The first application example shown in 図 49 uses TPS3840DL30, an open-drain active-low voltage supervisor to monitoring undervoltage and TMP303, a push-pull active-high window temperature switch to monitor under and over temperature. For the undervoltage application, the TPS3840DL30 is operating in the inactive logic high region so an overvoltage fault occurs when the battery voltage falls below V_{IT-} = 3.0 V or when the battery temperature is outside the range from 0°C to 60°C. The second application example uses TPS3840DL30 operating in the active-low region to monitor overvoltage and TMP303 to monitor under and over temperature. For the overvoltage requirement, the fault occurs when the battery voltage rises above 3.1 V or when the battery temperature is outside the range from 0°C to 60°C.

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PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Battery Voltage Supervision	Monitor 3.3-V battery for undervoltage condition	TPS3840 provides voltage monitoring with 1% accuracy with device options available in 0.1 V variations. TPS3840DL30 triggers a reset when VDD falls below 3 V. TPS3840PH30 triggers a reset when VDD rises above 3 V plus hysteresis setting the overvoltage threshold to 3.1 V.
	Monitor 2.8-V battery for overvoltage condition	
Battery Temperature Supervision	Monitor battery temperature between 0°C and 60°C with 1°C resolution for undervoltage design	TMP303A monitors temperature within 0°C to 60°C with 1°C resolution. Note this is a push-pull, active-high output device.
Output Topology	Undervoltage: Active-Low, Open-Drain	TPS3840 is offered in Active-Low Open-drain, Active-Low Push-Pull, and Active-High Push-Pull topologies
	Overvoltage: Active-High, Push-Pull	
Maximum device current consumption	10 µA	TPS3840 requires 350 nA (typical) and TMP303 requires 3.5 µA (typical)
Delay when returning from fault condition	Delay of at least 6 seconds when returning from the fault to prevent operation in fault conditions	C_{CT} = 10 µF sets 6.18 second delay

10.2.2.2 Detailed Design Procedure

The primary constraint for this application is choosing the correct device to monitor the battery supply voltage. The TPS3840 can monitor any voltage between 1.6 V and 10 V and is available in 0.1 V increments. Depending on how far away from the nominal voltage rail the user wants the voltage supervisor to trigger determines the correct voltage supervisor variant to choose. In this design example, the TPS3840DL30 is chosen for both the undervoltage and overvoltage monitoring. For undervoltage monitoring, the undervoltage fault occurs when the 3.3-V rail falls to 3 V and for the overvoltage monitoring, the overvoltage fault occurs when the 2.8-V rail rises above the 3-V threshold (V_{IT-}) plus 100mV hysteresis (V_{HYS}). It's important to note that in the undervoltage application, the TPS3840 $\overline{\text{RESET}}$ output is logic high during normal conditions whereas in the overvoltage application, the TPS3840 $\overline{\text{RESET}}$ output is logic low during normal conditions which is the reason a single device can be used for either type of monitoring depending on the logic required at the output. The opposite $\overline{\text{RESET}}$ output logic is offered in the push-pull, active-high device TPS3840PH noted with the RESET output. The secondary constraint for this application is the battery temperature monitoring accomplished by the TMP303A. Typical Lithium Ion battery discharge temperature range is 0°C to 60°C which is accomplished by the 'A' variante of TMP303A. The TMP303A triggers a fault to the $\overline{\text{MR}}$ pin of the TPS3840 or directly to the battery charger whenever the temperature is outside of the temperature range. The TMP303A offers 1°C resolution to meet the high resolution requirement. Because the undervoltage monitor design uses TMP303A, a push-pull active-high output device, an additional inverter is required before the $\overline{\text{MR}}$ pin because during normal operation, the TMP303 output is low but the $\overline{\text{MR}}$ pin must be logic high during normal operation. If using two TPS3840 devices for both undervoltage and overvoltage monitoring on the same battery, only one single temperature monitoring device is required. The last constraint is the $\overline{\text{RESET}}$/RESET time delay set by C_{CT}. For applications with ambient temperatures ranging from –40°C to +125°C, C_{CT} can be calculated using R_{CT} and solving for C_{CT} in 式 2. By choosing a standard 10% capacitor value of 10 µF ensures the $\overline{\text{RESET}}$/RESET time delay will be at least 6 seconds. Note: active-low devices use the output label $\overline{\text{RESET}}$ and active-high devices use the output label RESET.

A 0.1-µF decoupling capacitor is connected to the VDD pin as a good analog design practice. The pull-up resistor is only required for the Open-Drain device variants and is calculated to maintain the $\overline{\text{RESET}}$ current within the ±5 mA limit found in the *Recommended Operating Conditions*: $R_{Pull\text{-}up} = V_{Pull\text{-}up} \div 5$ mA. For this design, a 1-MΩ pull-up resistor is selected to minimize current draw when $\overline{\text{RESET}}$ is asserted and to prevent the battery from unnecessary discharge. Keep in mind the lowering the pull-up resistor, increases V_{OL} and I_{OUT}. The $\overline{\text{MR}}$ pin is used for a second fault condition provided by the temperature switch.

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10.2.3 Design 3: Fast Start Undervoltage Supervisor with Level-shifted Input

A typical application for the TPS3840 is a fast startup undervoltage supervisor that operates with an input power supply higher than the recommended maximum of 10 V through the use of a resistor divider at the input as shown in 図 51. The TPS3840 can be used to monitor any rail above 1.6 V and only requires maximum 350 µs upon startup before the device can begin monitoring a voltage. In this design application, a TPS3840 monitors a 12-V rail and triggers a reset fault condition if the voltage rail voltage drops below 10 V using a TPS3840 device with V_{IT-} of 4.9 V. This design also accounts for a wide input range in the case the 12-V rail rises higher, the resistor divider is set so that the voltage at the VDD pin never exceeds 10 V. The resistor values must not be so large that the external resistor divider affects the accuracy or operation of the device. TPS3840 is available in both active-low and active-high topologies providing the flexibility to monitor undervoltage or overvoltage with either output logic. This design uses the active-low, open-drain TPS3840DL49 variant so that when the undervoltage condition occurs, that is when the voltage at VDD pin falls below the voltage threshold set by the external resistor divider, the output transitions to logic-low and can be used to flag an undervoltage condition or used to connect to the ENABLE of the next device to shut it off as a logic low on an ENABLE pin typically disables the device. In this design, the output of the TPS3840 simply connects to a MCU to flag an undervoltage condition.

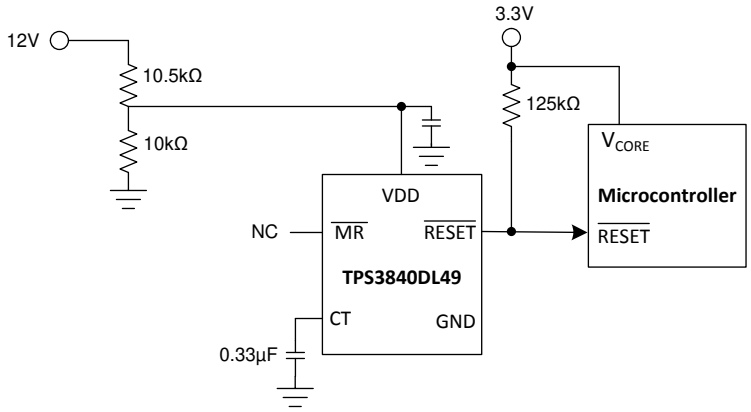


図 51. Fast Start Undervoltage Supervisor with Level-shifted Input

10.2.3.1 Design Requirements

This design requires voltage supervision on a 12-V power supply voltage rail with possibility of the 12-V rail rising up as high as 18 V. The undervoltage fault occurs when the power supply voltage drops below 10 V.

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Power Rail Voltage Supervision	Monitor 12-V power supply for undervoltage condition, trigger a undervoltage fault at 10 V.	TPS3840 provides voltage monitoring with 1% accuracy with device options available in 0.1 V variations. The TPS3840 monitors voltages above 1.6 V.
Maximum Input Power	Operate with power supply input up to 18 V.	The TPS3840 limits VDD to 10 V but can monitor voltages higher than the maximum VDD voltage with the use of an external resistor divider.
Output logic voltage	3.3-V Open-Drain	3.3-V Open-Drain
Maximum device current consumption	35 µA when power supply is at 18 V maximum	TPS3840 requires 350 nA (typical) and the external resistor divider will also consume current. There is a tradeoff between current consumption and voltage monitor accuracy but generally set the resistor divider to consume 100 times current into VDD.
Voltage Monitor Accuracy	Typical voltage monitor accuracy of 2.5%. This allows the voltage threshold to range between 11.75 V and 10.25 V.	The TPS3840 has 1% typical voltage monitor accuracy. By decreasing the ratio of resistor values, the resistor divider will consume more current but the accuracy will increase. The resistor tolerance also needs to be accounted for.
Delay when returning from fault condition	$\overline{\text{RESET}}$ delay of at least 200 ms when returning from a undervoltage fault.	C_{CT} = 0.33 µF sets 204 ms delay

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10.2.3.2 Detailed Design Procedure

The primary constraint for this application is monitoring a 12-V rail while preventing the VDD pin on TPS3840 from exceeding the recommended maximum of 10 V. This is accomplished by sizing the resistor divider so that when the 12-V rail drops to 10 V, the VDD pin for TPS3840 will be at 4.9 V which is the V_{IT-} threshold for triggering a undervoltage condition for TPS3840DL49 as shown in 式 7.

$$V_{rail_trigger} = V_{IT-} \times (R_{bottom} \div (R_{top} + R_{bottom})) \quad (7)$$

where $V_{rail_trigger}$ is the trigger voltage of the rail being monitored, V_{IT-} is the falling threshold on the VDD pin of TPS3840, and R_{top} and R_{bottom} are the top and bottom resistors of the external resistor divider. V_{IT-} is fixed per device variant and is 4.9 V for TPS3840DL49. Substituting in the values from 図 51, the undervoltage trigger threshold for the rail is set to 10.045 V.

Since the undervoltage trigger of 10 V on the rail corresponds to 4.9 V undervoltage threshold trigger of the TPS3840 device, there is plenty of room for the rail to rise up while maintaining less than 10 V on the VDD pin of the TPS3840. 式 8 shows the maximum rail voltage that still meets the 10 V maximum at the VDD pin for TPS3840.

$$V_{rail_max} = 10 \times (10{,}000 \div (10{,}500 + 10{,}000)) = 20.5\ V \quad (8)$$

This means the monitored voltage rail can go as high as 20.5 V and still not violate the recommended maximum for the VDD pin on TPS3840. This is useful when monitoring a voltage rail that has a wide range that may go much higher than the nominal rail voltage such as in this case with the specification that the 12-V rail can go as high as 18 V. Notice that the resistor values chosen are less than 100kΩ to preserve the accuracy set by the internal resistor divider. Good design practice recommends using a 0.1-µF capacitor on the VDD pin and this capacitance may need to increase when using an external resistor divider.

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10.2.4 Design 4: Voltage Monitor with Back-up Battery Switchover

A typical application for the TPS3840 is to monitor a voltage rail and switch the power to a back-up battery if the main supply is in undervoltage condition. Because systems that utilize a back-up battery tend to require low quiescent current, TPS3840 serves as the perfect solution as this device only requires 350 nA typically. The TPS3840 monitors the main power rail via the VDD pin and when the main power rail falls, the $\overline{\text{RESET}}$ output asserts causing a switch to close on the back-up battery rail. The diodes provide an ORing logic function to prevent reverse leakage and to allow either rail to connect to the output depending on the status of the main voltage rail.

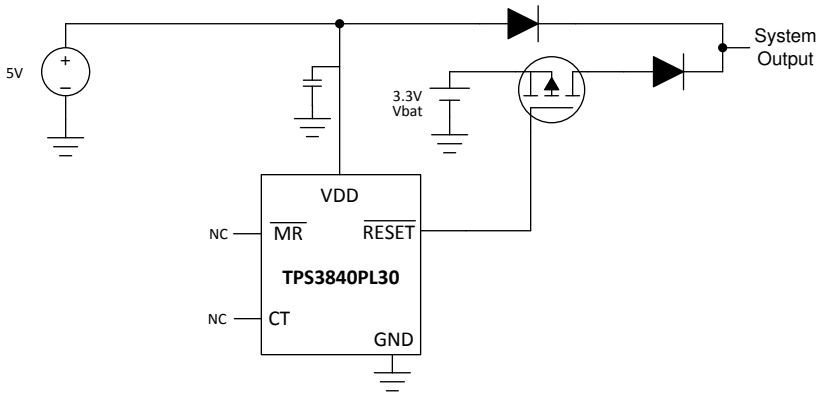


図 52. Voltage Monitor with Back-up Battery Switchover Solution

10.2.4.1 Design Requirements

This design requires voltage supervision on a 5-V main supply voltage rail and when the main rail fails, switch to a back-up battery supply to prevent complete power loss in the system. The System Output must remain above 1.8 V even when the main supply completely fails. The design requires less than 500 nA of total current consumption and must prevent battery leakage when the battery is not being used. When the system is using the back-up battery and the main supply voltage rail comes back up, the system must switch back to the main power supply in less than 100 µs to save battery power.

PARAMETER	DESIGN REQUIREMENT	DESIGN RESULT
Main Supply Voltage Supervision	Monitor 5-V main supply for undervoltage condition. When main supply drops below 3 V, switch to back-up battery.	TPS3840 provides voltage monitoring with 1% accuracy with device options available in 0.1 V variations. This design uses TPS3840PL30 to set the undervoltage trigger at 3 V.
Batck-up Battery Switchover	When undervoltage occurs on the main supply voltage rail, switch to the back-up batter.	When undervoltage occurs on the main supply rail, the PMOS switch closes allowing the back-up battery to connect to the system output. The diodes prevent reverse leakage and allow either power supply to connect to the system output.
Main Power Supply to Back-up Battery Switch Response Time	No more than 50 µs to switch to the back-up battery when the main power supply falls to undervoltage condition.	TPS3840 provides a propagation delay for VDD falling below the undervoltage threshold (t_{P_HL}) of 50 µs maximum to meet the requirement.
Back-up Battery to Main Power Supply Switch Back Response Time	Less than 100 µs when switching from back-up battery back to main power supply when undervoltage condition is removed.	By leaving $\overline{\text{MR}}$ disconnected, the $\overline{\text{RESET}}$ delay is set to a maximum of 50 µs to meet the requirement.
Device Current Consumption	500 nA	TPS3840 requires 350 nA (typical)
System Output Voltage	System Output must remain above 1.8 V in all cases	When the main 5-V rail is connected, the System Output will be the rail voltage minus a diode voltage drop so at least 3 V - 0.7 V ~ 2.3 V. When the voltage rail drops below 3 V, the back-up battery switches into the system and the System Output becomes the battery voltage minus a diode voltage drop so 3.3 V - 0.7 V ~ 2.6 V. The threshold at which the battery switches into the system directly depends on the TPS3840 variant chosen.

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10.2.4.2 Detailed Design Procedure

The primary constraints for this application are choosing the correct device variant for the monitored voltage and deciding the preferred solution to switch the back-up battery in and out of the system. For this design, the TPS3840PL30 provides an active-low, push-pull output topology that turns on the PFET when the 5-V rail monitored by VDD drops to 3.0 V. The diodes logically OR the power supply with the back-up battery and prevents reverse current leakage. Using this solution, the System Output remains above 1.8 V in all circumstances unless both the 5-V rail and back-up battery fail. The System Output voltage will follow the 5-V rail minus a diode drop until the 5-V rail drops to 3 V then the back-up battery switches into the system providing 3.3 V minus a diode drop to the System Output. When the 5-V rail comes back above 3.1 V accounting for hysteresis, the PFET turns off to disconnect the back-up battery from the system. Since this design disconnects the battery when not being used, this solution maximizes battery life.

10.2.5 Application Curve: TPS3840EVM

These application curves are taken with the *TPS3840EVM*. Please see the *TPS3840EVM User Guide* for more information.

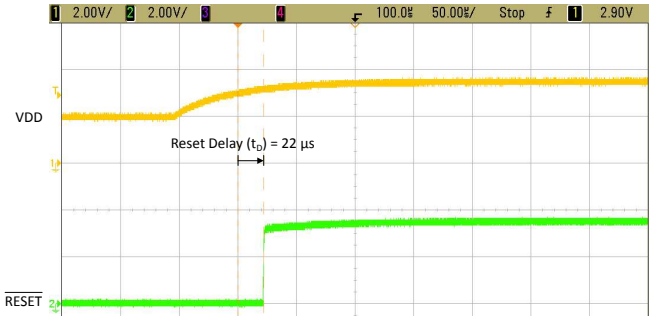


図 53. TPS3840EVM $\overline{\text{RESET}}$ Time Delay (t_D) with No Capacitor



図 54. TPS3840EVM $\overline{\text{RESET}}$ Time Delay (t_D) with 0.01-µF Capacitor

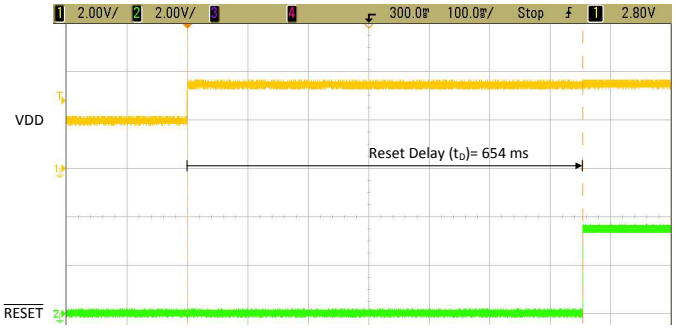


図 55. TPS3840EVM $\overline{\text{RESET}}$ Time Delay (t_D) with 1-µF Capacitor

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11 Power Supply Recommendations

These devices are designed to operate from an input supply with a voltage range between 1.5 V and 10 V. TI recommends an input supply capacitor between the VDD pin and GND pin. This device has a 12-V absolute maximum rating on the VDD pin. If the voltage supply providing power to VDD is susceptible to any large voltage transient that can exceed 12 V, additional precautions must be taken.

12 Layout

12.1 Layout Guidelines

Make sure that the connection to the VDD pin is low impedance. Good analog design practice recommends placing a minimum 0.1-µF ceramic capacitor as near as possible to the VDD pin. If a capacitor is not connected to the CT pin, then minimize parasitic capacitance on this pin so the rest time delay is not adversely affected.

- Make sure that the connection to the VDD pin is low impedance. Good analog design practice is to place a >0.1-µF ceramic capacitor as near as possible to the VDD pin.
- If a C_{CT} capacitor is used, place these components as close as possible to the CT pin. If the CT pin is left unconnected, make sure to minimize the amount of parasitic capacitance on the pin to <5 pF.
- Place the pull-up resistors on $\overline{\text{RESET}}$ pin as close to the pin as possible.

12.2 Layout Example

The layout example in shows how the TPS3840 is laid out on a printed circuit board (PCB) with a user-defined delay.

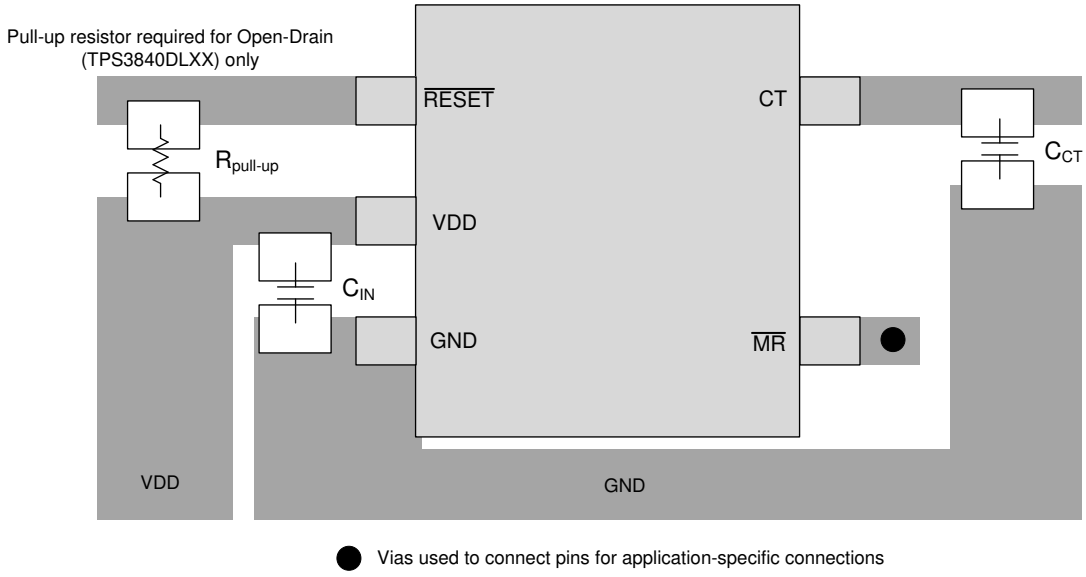


図 56. TPS3840 Recommended Layout

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13 デバイスおよびドキュメントのサポート

13.1 デバイスの項目表記

表 2 に、デバイスの部品番号の機能コードの意味を示します。

表 2. デバイスの命名規則

説明	項目表記	値
型番	TPS3840	TPS3840
バリアント・コード (出力トポロジ)	DL	オープン・ドレイン、アクティブ LOW
	PH	プッシュプル、アクティブ HIGH
	PL	プッシュプル、アクティブ LOW
検出電圧オプション	## (2 文字)	例:16 は 1.6V のスレッショルドを表します。
パッケージ	DBV	SOT23-5
リール	R	大型リール

表 3 に、TPS3840 の提供中のバリアントを示します。下記以外のオプションの詳細と入手可能性については、テキサス・インスツルメンツにお問い合わせください。最小注文数量があります。

表 3. デバイスのスレッショルド

製品名			電圧スレッショルド (V_{IT-})	ヒステリシス (V_{HYST})
オープン・ドレイン、アクティブ **LOW**	プッシュプル、アクティブ **LOW**	プッシュプル、アクティブ **HIGH**	標準値 (V)	標準値 (V)
TPS3840DL16	TPS3840PL16	TPS3840PH16	1.6	0.100
TPS3840DL17	TPS3840PL17	TPS3840PH17	1.7	0.100
TPS3840DL18	TPS3840PL18	TPS3840PH18	1.8	0.100
TPS3840DL19	TPS3840PL19	TPS3840PH19	1.9	0.100
TPS3840DL20	TPS3840PL20	TPS3840PH20	2.0	0.100
TPS3840DL21	TPS3840PL21	TPS3840PH21	2.1	0.100
TPS3840DL22	TPS3840PL22	TPS3840PH22	2.2	0.100
TPS3840DL23	TPS3840PL23	TPS3840PH23	2.3	0.100
TPS3840DL24	TPS3840PL24	TPS3840PH24	2.4	0.100
TPS3840DL25	TPS3840PL25	TPS3840PH25	2.5	0.100
TPS3840DL26	TPS3840PL26	TPS3840PH26	2.6	0.100
TPS3840DL27	TPS3840PL27	TPS3840PH27	2.7	0.100
TPS3840DL28	TPS3840PL28	TPS3840PH28	2.8	0.100
TPS3840DL29	TPS3840PL29	TPS3840PH29	2.9	0.100
TPS3840DL30	TPS3840PL30	TPS3840PH30	3.0	0.100
TPS3840DL31	TPS3840PL31	TPS3840PH31	3.1	0.100
TPS3840DL32	TPS3840PL32	TPS3840PH32	3.2	0.200
TPS3840DL33	TPS3840PL33	TPS3840PH33	3.3	0.200
TPS3840DL34	TPS3840PL34	TPS3840PH34	3.4	0.200
TPS3840DL35	TPS3840PL35	TPS3840PH35	3.5	0.200
TPS3840DL36	TPS3840PL36	TPS3840PH36	3.6	0.200
TPS3840DL37	TPS3840PL37	TPS3840PH37	3.7	0.200
TPS3840DL38	TPS3840PL38	TPS3840PH38	3.8	0.200
TPS3840DL39	TPS3840PL39	TPS3840PH39	3.9	0.200
TPS3840DL40	TPS3840PL40	TPS3840PH40	4.0	0.200
TPS3840DL41	TPS3840PL41	TPS3840PH41	4.1	0.200
TPS3840DL42	TPS3840PL42	TPS3840PH42	4.2	0.200
TPS3840DL43	TPS3840PL43	TPS3840PH43	4.3	0.200

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表 3. デバイスのスレッショルド (continued)

製品名			電圧スレッショルド (V_{IT-})	ヒステリシス (V_{HYST})
オープン・ドレイン、アクティブ LOW	プッシュプル、アクティブ LOW	プッシュプル、アクティブ HIGH	標準値 (V)	標準値 (V)
TPS3840DL44	TPS3840PL44	TPS3840PH44	4.4	0.200
TPS3840DL45	TPS3840PL45	TPS3840PH45	4.5	0.200
TPS3840DL46	TPS3840PL46	TPS3840PH46	4.6	0.200
TPS3840DL47	TPS3840PL47	TPS3840PH47	4.7	0.200
TPS3840DL48	TPS3840PL48	TPS3840PH48	4.8	0.200
TPS3840DL49	TPS3840PL49	TPS3840PH49	4.9	0.200

13.2 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

13.3 商標

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13.4 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

13.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3840DL16DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL16	Samples
TPS3840DL17DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL17	Samples
TPS3840DL18DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL18	Samples
TPS3840DL19DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL19	Samples
TPS3840DL20DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL20	Samples
TPS3840DL22DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL22	Samples
TPS3840DL24DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL24	Samples
TPS3840DL25DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL25	Samples
TPS3840DL27DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL27	Samples
TPS3840DL28DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL28	Samples
TPS3840DL29DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL29	Samples
TPS3840DL30DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL30	Samples
TPS3840DL31DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL31	Samples
TPS3840DL35DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL35	Samples
TPS3840DL40DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL40	Samples
TPS3840DL42DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL42	Samples
TPS3840DL44DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL44	Samples
TPS3840DL45DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL45	Samples
TPS3840DL46DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL46	Samples
TPS3840DL49DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	DL49	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3840PH18DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PH18	Samples
TPS3840PH19DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PH19	Samples
TPS3840PH27DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PH27	Samples
TPS3840PH30DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PH30	Samples
TPS3840PH40DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PH40	Samples
TPS3840PH45DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PH45	Samples
TPS3840PH49DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PH49	Samples
TPS3840PL16DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL16	Samples
TPS3840PL18DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL18	Samples
TPS3840PL20DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL20	Samples
TPS3840PL25DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL25	Samples
TPS3840PL26DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL26	Samples
TPS3840PL27DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL27	Samples
TPS3840PL28DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL28	Samples
TPS3840PL29DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL29	Samples
TPS3840PL30DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL30	Samples
TPS3840PL31DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PL31	Samples
TPS3840PL33DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PL33	Samples
TPS3840PL34DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL34	Samples
TPS3840PL40DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PL40	Samples
TPS3840PL41DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PL41	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS3840PL42DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL42	Samples
TPS3840PL43DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL43	Samples
TPS3840PL44DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	SN	Level-1-260C-UNLIM	-40 to 125	PL44	Samples
TPS3840PL45DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL45	Samples
TPS3840PL48DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU | SN	Level-1-260C-UNLIM	-40 to 125	PL48	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF TPS3840 :

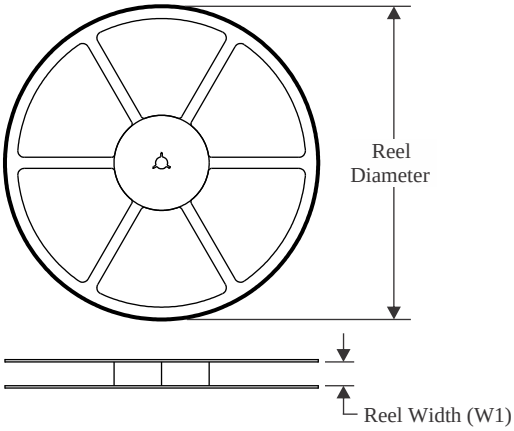
- Automotive : TPS3840-Q1

NOTE: Qualified Version Definitions:

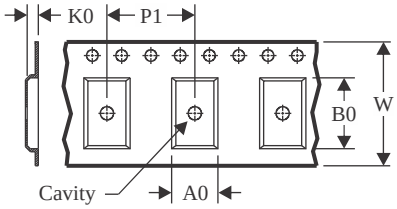
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

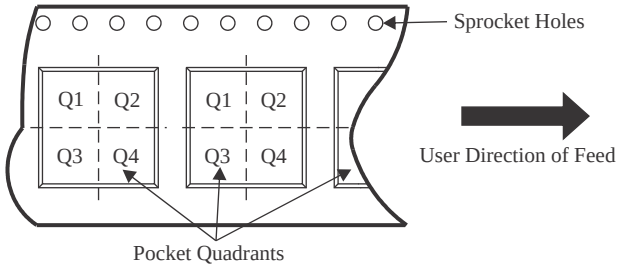


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



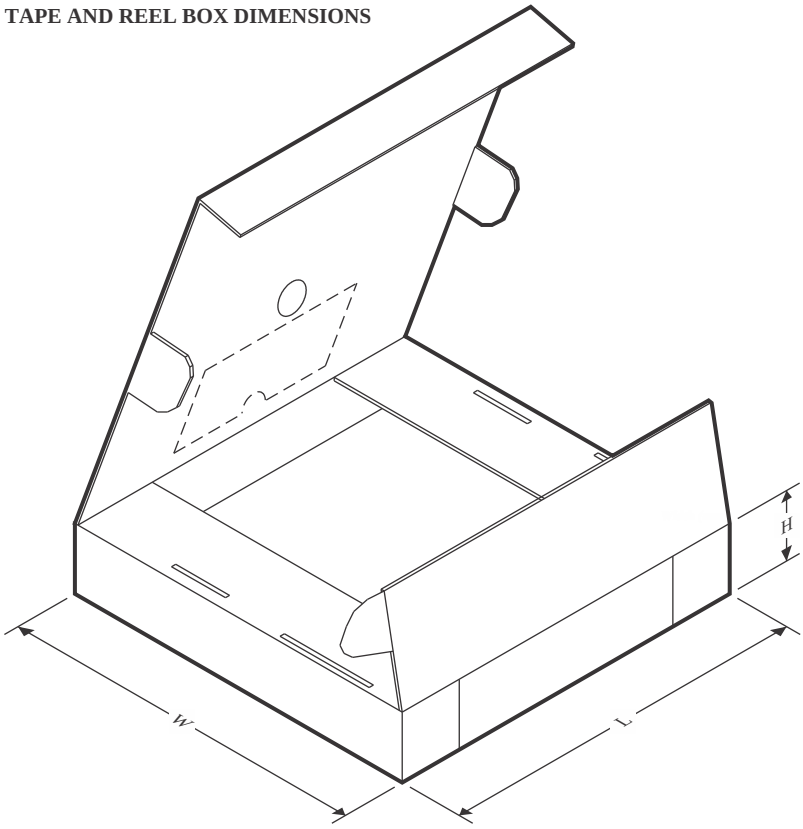
*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3840DL16DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL16DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL17DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL17DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL18DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL19DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL19DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL20DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL22DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL24DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL24DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL25DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL27DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL28DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL29DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL30DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3840DL30DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL31DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL35DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL35DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL40DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL40DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL42DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL44DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL45DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL45DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL46DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL46DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840DL49DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PH18DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PH19DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PH19DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PH27DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PH27DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PH30DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PH30DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PH40DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PH40DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PH45DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PH45DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PH49DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PH49DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL16DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL16DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL18DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL20DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL25DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL25DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL26DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL26DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL27DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL27DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL28DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL29DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL30DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL31DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL33DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS3840PL34DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL34DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL40DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL41DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL42DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL42DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL43DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL43DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL44DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL45DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL45DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS3840PL48DBVR	SOT-23	DBV	5	3000	180.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3840DL16DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL16DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL17DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL17DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL18DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL19DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL19DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL20DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL22DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL24DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL24DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL25DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL27DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL28DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL29DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL30DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL30DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL31DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3840DL35DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL35DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL40DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL40DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL42DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL44DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL45DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL45DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL46DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL46DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840DL49DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PH18DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PH19DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PH19DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PH27DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PH27DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PH30DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PH30DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PH40DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PH40DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PH45DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PH45DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PH49DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PH49DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL16DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL16DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL18DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL20DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL25DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL25DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL26DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL26DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL27DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL27DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL28DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL29DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL30DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL31DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL33DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL34DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL34DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL40DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL41DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0

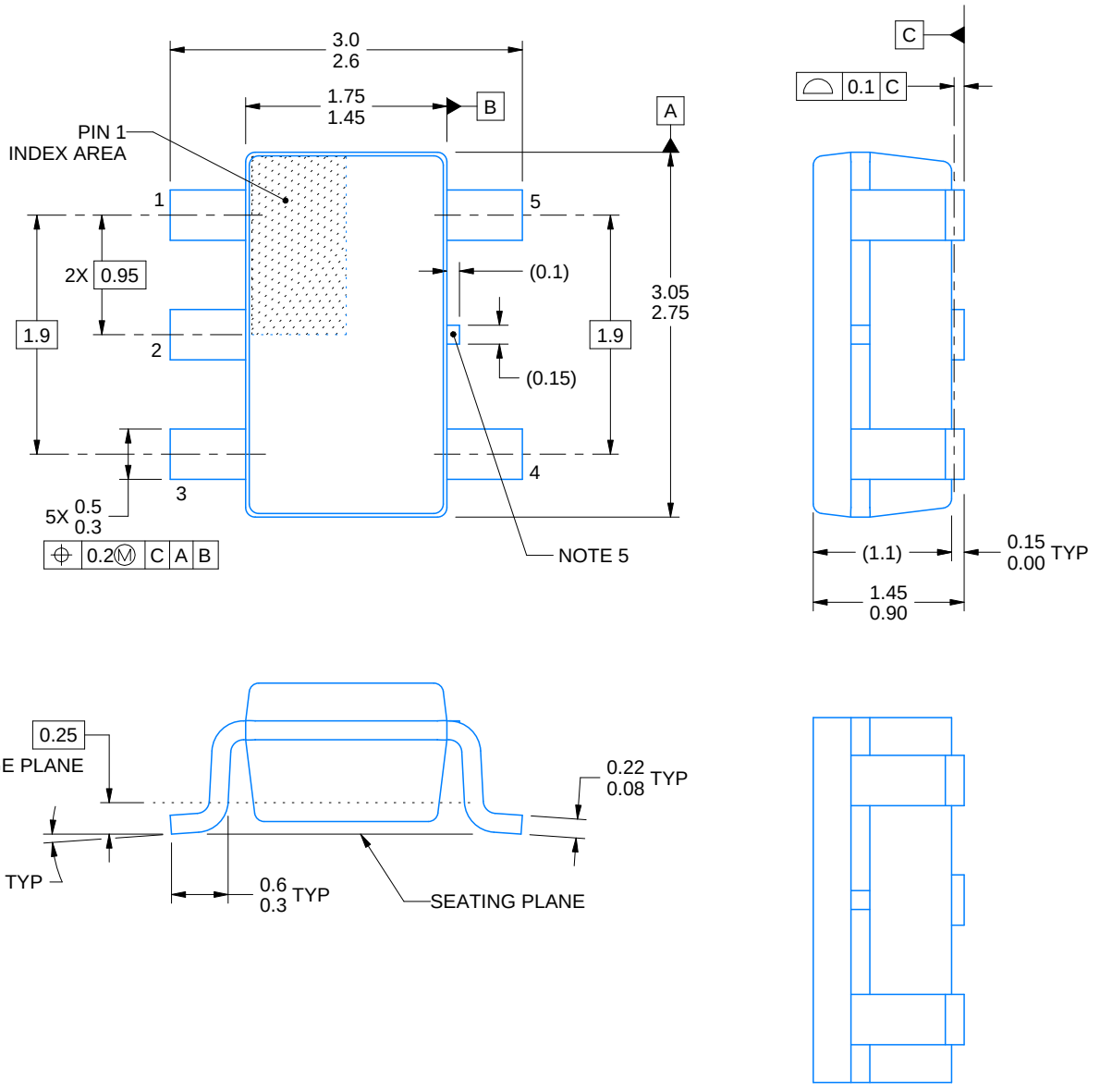
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS3840PL42DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL42DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL43DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL43DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL44DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL45DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL45DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0
TPS3840PL48DBVR	SOT-23	DBV	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

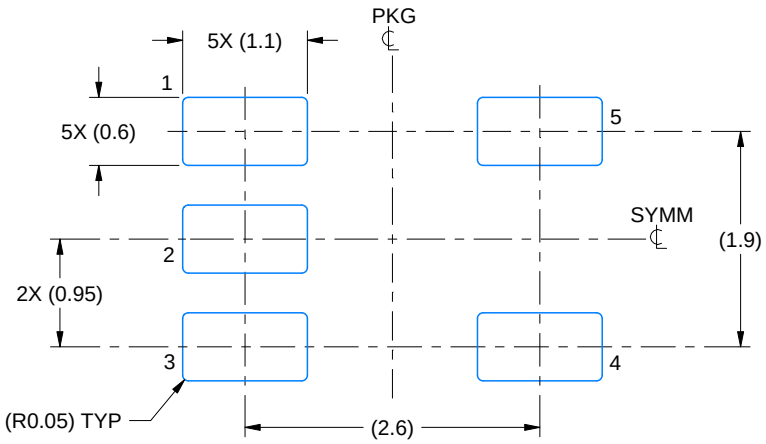


ALTERNATIVE PACKAGE SINGULATION VIEW

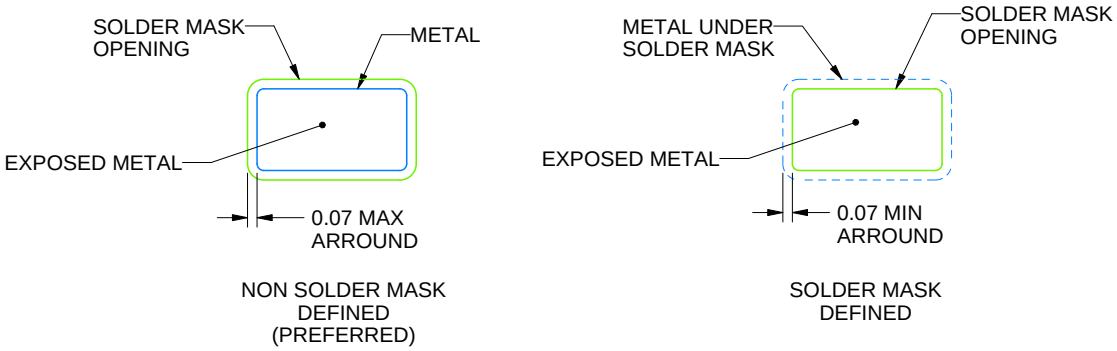
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NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

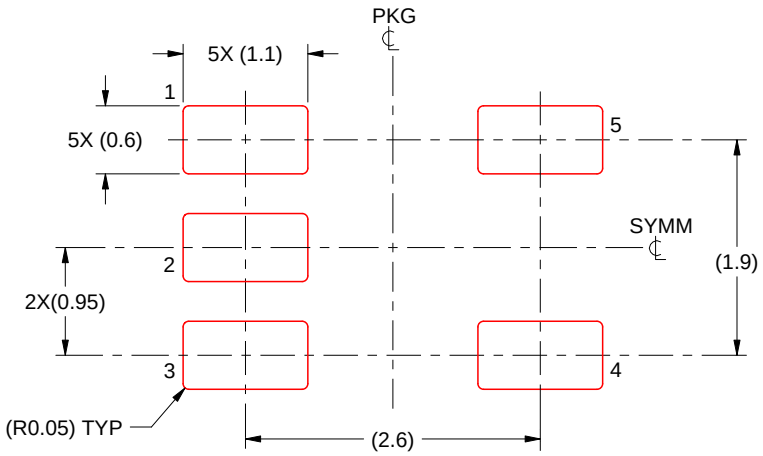


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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