TPS54678 2.95V～6V 入力、6A、ヒカップ電流制限搭載の同期整流降圧型 SWIFT™ コンバータ

1 特長

- 2 つの 12mΩ (標準値) MOSFET により 6A の連続出力電流に対応
- 200kHz～ 2MHz のスイッチング周波数
- -40℃～+150℃ の温度範囲全体で 0.6V ±1% の基準電圧
- 外部クロックに同期
- プリバイアス電圧でのスタートアップ
- パワー・グッド出力
- 調整可能なスロー・スタートとシーケンシング
- サイクル単位の電流制限とヒカップ電流保護
- 入力電圧 UVLO を調整可能
- 熱的に強化された 16 ピン、3mm × 3mm WQFN (RTE)
- WEBENCH® Power Designer により、TPS54678 を使用するカスタム設計を作成

2 アプリケーション

- 低電圧、高密度の電源システム
- 高性能 DSP、FPGA、ASIC、マイクロプロセッサのポイント・オブ・ロード・レギュレーション
- ブロードバンド、ネットワーク、光通信
- 通信インフラ
- ゲーム、DTV、セットトップ・ボックス

3 概要

TPS54678 デバイスは、2 つの MOSFET を内蔵したフル機能の 6V、6A 同期整流降圧型電流モード・コンバータです。

TPS54678 は、MOSFET を内蔵し、電流モード制御の実装により外付け部品数が少なく、スイッチング周波数が最大 2MHz と高いためインダクタのサイズを小さくでき、熱的に強化された小型 (3mm × 3mm) WQFN パッケージにより IC のフットプリントを最小化できるため、小型の設計を実現できます。

TPS54678 は、温度範囲全体で ±1% の正確な基準電圧 (V_{REF}) により、各種の負荷について正確なレギュレーションを行います。

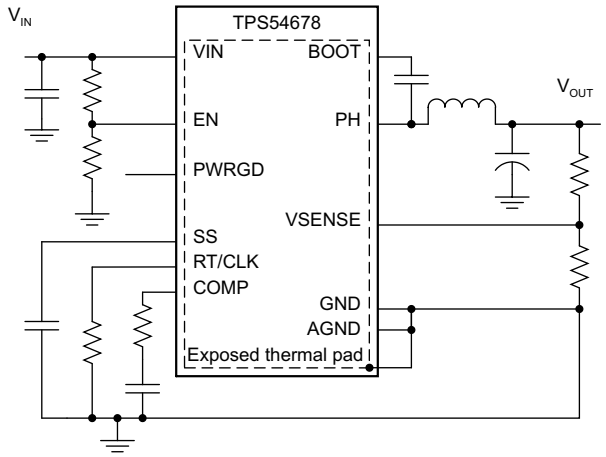
内蔵の 12mΩ MOSFET により効率を最大化できます。イネーブル (EN) ピンを使用してデバイスをディセーブルすると、シャットダウン時消費電流を低減できます。

製品情報(1)

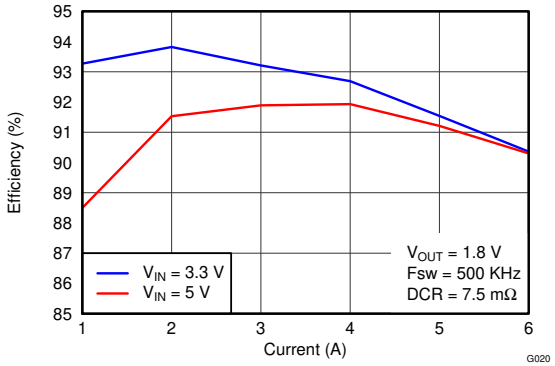
型番	パッケージ	本体サイズ (公称)
TPS54678	WQFN (16)	3.00mm×3.00mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

概略回路図



効率と出力電流との関係



目次

4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (November 2015) から Revision B に変更 **Page**

- 編集上の変更のみ、技術的内容の変更なし。WEBENCH へのリンクを追加 ... 3

2012年6月発行のものから更新 **Page**

- 「*ピン構成および機能*」セクション、「*ESD 定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを追加 ... 1
- Changed *Thermal Information* table values ... 5

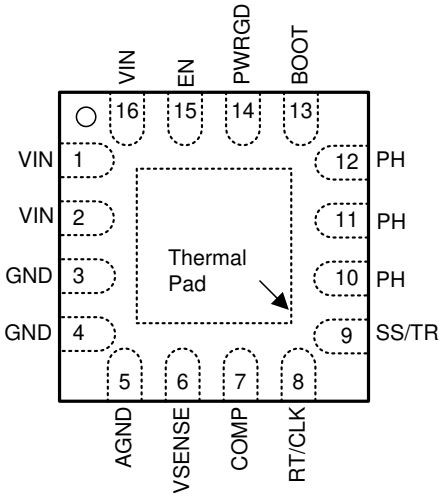
5 概要（続き）

出力電圧のスタートアップ・ランプは、ソフトスタート (SS) ピンにより制御されます。このピンはシーケンス処理やトラッキング用に構成することも可能です。プリバイアスされた電圧での単調なスタートアップを実現します。低電圧誤動作防止は、イネーブル・ピンの抵抗分圧器でスレッショルドをプログラムすることで、高い値に変更できます。オープン・ドレインのパワー・グッド信号は、出力が公称電圧の93%～105%の範囲内にあることを示します。

サイクル単位の電流制限、ヒカップ過電流保護、サーマル・シャットダウンは、過電流条件中、デバイスを保護します。

6 Pin Configuration and Functions

RTE Package
16-Pin WQFN
Top View



Pin Functions

PIN		I/O(1)	DESCRIPTION
NAME	NO.		
AGND	5	G	Analog ground should be electrically connected to GND close to the device.
BOOT	13	I	A bootstrap capacitor is required between BOOT and PH. If the voltage on this capacitor is below the minimum required by the BOOT UVLO, the output is forced to switch off until the capacitor is refreshed.
COMP	7	O	Error amplifier output, and input to the output switch current comparator. Connect frequency compensation components to this pin.
EN	15	I	Enable pin, internal pullup current source. Pull below 1.2 V to disable. Float to enable. Can be used to set the on and off threshold (adjust UVLO) with two additional resistors.
GND	3	G	Power ground. This pin should be electrically connected directly to the thermal pad under the device.
	4		
PH	10	O	The source of the internal high-side power MOSFET, and drain of the internal low-side (synchronous) rectifier MOSFET.
	11		
	12		
PWRGD	14	O	An open-drain output asserts low if output voltage is low due to thermal shutdown, overvoltage, undervoltage, or EN shut down.
RT/CLK	8	I/O	Resistor Timing or External Clock input pin
SS/TR	9	I/O	Slow-start and Tracking. An external capacitor connected to this pin sets the output voltage rise time. This pin can also be used for tracking.
VIN	1	I	Input supply voltage, 2.95 V to 6 V
	2		
	16		
VSENSE	6	I	Inverting node of the transconductance (gm) error amplifier
Thermal Pad		–	GND pin should be connected to the exposed thermal pad for proper operation. This thermal pad should be connected to any internal PCB ground plane using multiple vias for good thermal performance.

(1) I = Input, O = Output, G = Ground

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input voltage	VIN, EN	–0.3	7	V
	RT/CLK, PWRGD	–0.3	6	
	COMP, SS/TR, VSENSE	–0.3	3	
Output voltage	BOOT-PH		7	V
	PH	–0.7	7	
	PH (20 ns transent)	–2	10	
	PH (5 ns transient)	–4	12	
Source current	EN, RT/CLK		100	µA
Sink current	COMP, SS		100	µA
	PWRGD		10	mA
Operating junction temperature, T_J		–40	150	°C
Storage temperature, T_{stg}		–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage	3	6	V
T_J	Operating junction temperature	–40	150	°C

7.4 Thermal Information(1)

THERMAL METRIC(2)		TPS54678 RTE (WQFN) 16 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	43.4	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	44.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	14.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	14.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	4.1	°C/W

(1) Unless otherwise specified, metrics listed in this table refer to JEDEC high-K board measurements
(2) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Electrical Characteristics

T_J = –40°C to +150°C, V_{IN} = 2.95 to 6 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY VOLTAGE (VIN PIN)					
Operating input voltage		2.95		6	V
Shutdown supply current	EN = 0 V, 25°C, 2.95 V ≤ VIN ≤ 6 V		1	3	µA
Operating non-switching supply current	VSENSE = 0.6 V, VIN = 5 V, 25°C, f_{SW} = 500 kHz		570	800	µA
ENABLE AND UVLO (EN PIN)					
Enable threshold	Rising		1.3		V
Enable threshold	Falling		1.18		V
Input current	Enable threshold + 50 mV		–3.5		µA
Input current	Enable threshold – 50 mV		–0.70		µA
VOLTAGE REFERENCE					
Voltage reference	2.95 V ≤ V_{IN} ≤ 6 V, –40°C < T_J < 150°C	0.594	0.600	0.606	V
MOSFET					
High-side switch resistance	BOOT-PH = 5 V		12	25	mΩ
High-side switch resistance	BOOT-PH = 2.95 V		17	33	
Low-side switch resistance	BOOT-PH = 5 V		12	25	mΩ
Low-side switch resistance	BOOT-PH = 2.95 V		17	33	
ERROR AMPLIFIER					
Input current			7		nA
Error amplifier transconductance (gm)	–2 µA < $I_{(COMP)}$ < 2 µA $V_{(COMP)}$ = 1 V		245		umhos
Error amplifier transconductance (gm) during slow-start	–2 µA < $I_{(COMP)}$ < 2 µA $V_{(COMP)}$ = 1 V, $V_{(VSENSE)}$ = 0.4 V		80		umhos
Error amplifier source and sink	$V_{(COMP)}$ = 1 V 100-mV overdrive		±20		µA
COMP to I_{switch} gm			20		A/V
CURRENT LIMIT					
Current limit threshold	Fs = 500 KHz	9.5	10.5	11.5	A
Cycles before entering hiccup during overcurrent			512		cycles
Hiccup cycles			16384		cycles
Low-side sourcing current threshold		7	8.5	10.5	A
Low-side FET reverse current protection			4		A
THERMAL SHUTDOWN					
Thermal shutdown			170		°C
Hysteresis			15		°C
TIMING RESISTOR AND EXTERNAL CLOCK (RT/CLK PIN)					
Switching frequency range using RT mode		200		2000	kHz
Switching frequency	R_t = 82.5 kΩ	400	500	600	kHz
Switching frequency range using CLK mode		300		2000	kHz
Minimum CLK pulse width			75		ns
RT/CLK voltage	$R_{(RT/CLK)}$ = 82.5 kΩ		0.5		V
RT/CLK high threshold			1.6	2.2	V
RT/CLK low threshold		0.4	0.6		V
RT/CLK falling edge to PH rising edge delay	Measure at 500 kHz with RT resistor in series		55		ns
PLL lock in time	Measure at 500 kHz		40		µs

Electrical Characteristics (continued)

T_J = –40°C to +150°C, V_{IN} = 2.95 to 6 V (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
PH (PH PIN)					
Minimum ON-time	Measured at 50% points on PH. I_{OUT} = 3 A		85	110	ns
	Measured at 50% points on PH. I_{OUT} = 0 A		100		ns
Minimum OFF-time	Prior to skipping off pulses, BOOT-PH = 3 V, I_{OUT} = 3 A		70		ns
Rise and fall dV/dT	BOOT-PH = 3 V; I_O = 6 A		1.5		V/ns
BOOT (BOOT PIN)					
Charging resistor	V_{IN} = 6 V, BOOT-PH = 6 V		7		Ω
BOOT-PH UVLO	V_{IN} = 3.3 V		2.2		V
SLOW START AND TRACKING (SS/TR PIN)					
Charge current	$V_{(SS/TR)}$ < 0.15 V		47		µA
	$V_{(SS/TR)}$ > 0.15 V		2.2		
SS/TR to VSENSE matching	V_{IN} = 3.3 V		60		mV
SS/TR to reference crossover	98% nominal		0.8		V
SS/TR discharge voltage (overload)	VSENSE = 0 V		4.5		mV
SS/TR discharge to current (overload)	VSENSE = 0 V; $V_{(SS/TR)}$ = 4 V		95		µA
SS/TR discharge current (UVLO, EN, thermal fault)	V_{IN} = 3 V; $V_{(SS/TR)}$ = 4 V		925		µA
POWER GOOD (PWRGD PIN)					
VSENSE threshold	VSENSE falling (Fault)		91		% V_{REF}
	VSENSE rising (Good)		93		% V_{REF}
	VSENSE rising (Fault)		105		% V_{REF}
	VSENSE falling (Good)		103		% V_{REF}
Output high leakage	VSENSE = V_{REF}, $V_{(PWRGD)}$ = 5.5 V		2		nA
ON-Resistance	V_{IN} = 5 V		65	120	Ω
Output low	$I_{(PWRGD)}$ = 2.5 mA		0.2	0.3	V
Minimum VIN for valid output	$V_{(PWRGD)}$ < 0.5 V at 100 µA		1.2	1.5	V

7.6 Typical Characteristics

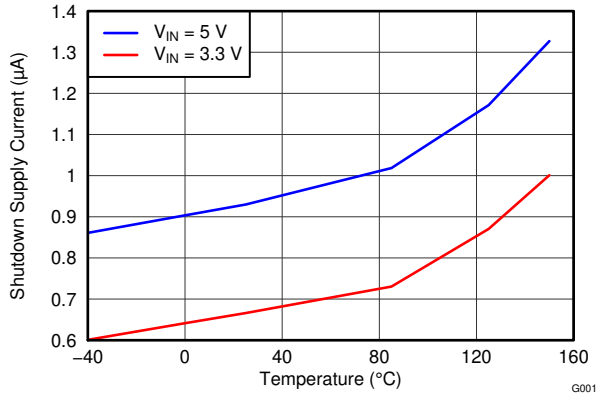


Figure 1. Shutdown Supply Current vs Junction Temperature

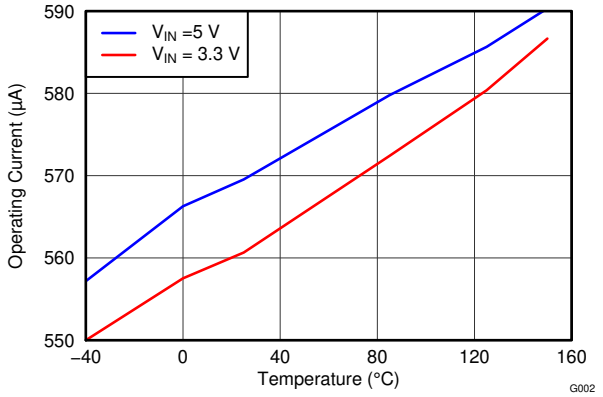


Figure 2. VIN Operating Current vs Junction Temperature

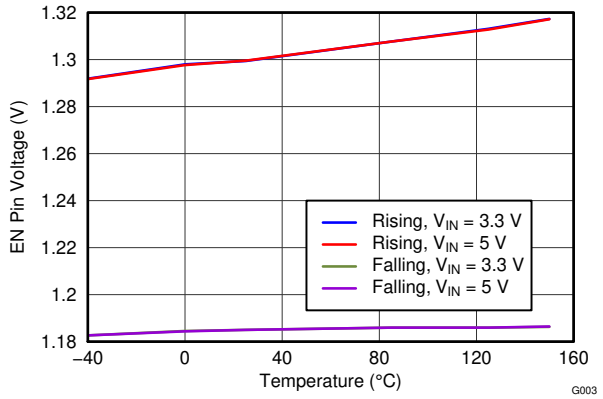


Figure 3. EN Pin Voltage vs Junction Temperature

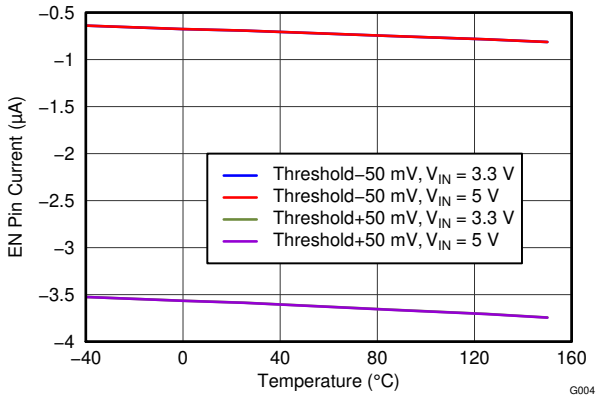


Figure 4. EN Pin Current vs Junction Temperature

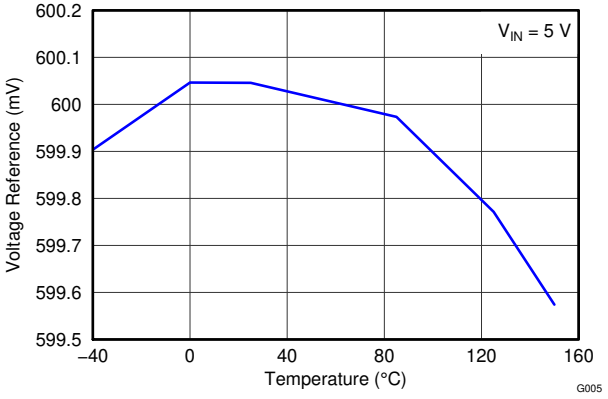


Figure 5. Voltage Reference vs Junction Temperature

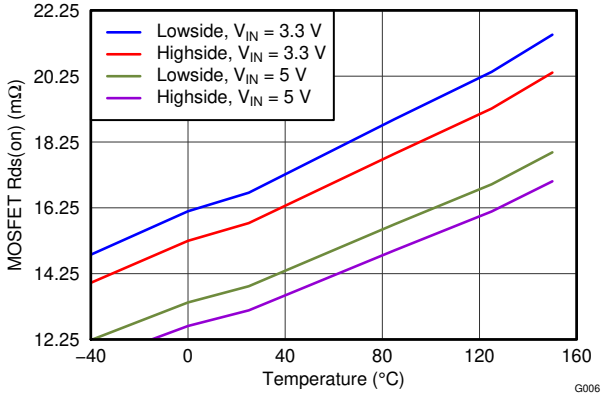


Figure 6. MOSFET $R_{ds(on)}$ vs Junction Temperature

Typical Characteristics (continued)

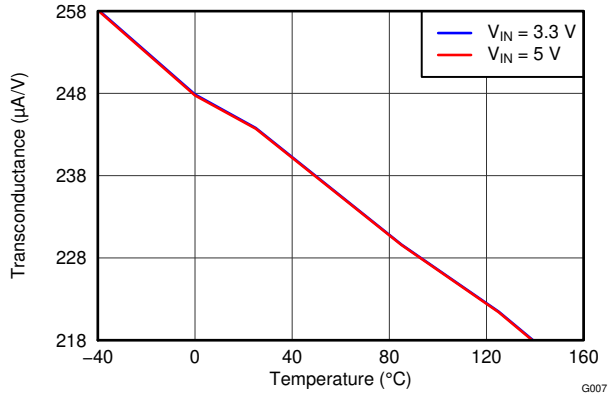


Figure 7. Transconductance vs Junction Temperature

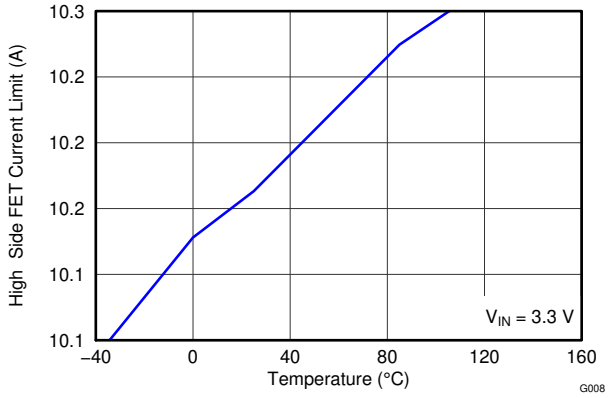


Figure 8. High-Side FET Current Limit vs Junction Temperature

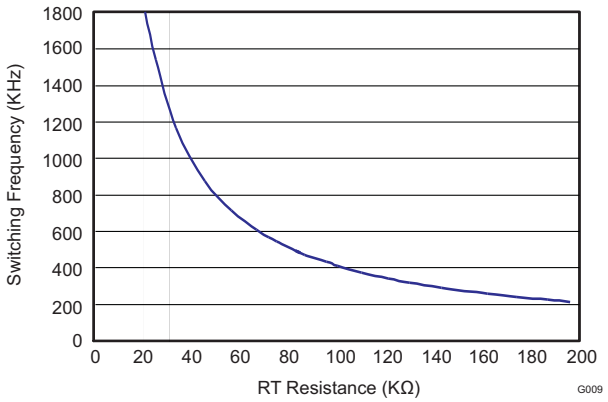


Figure 9. Switching Frequency vs RT Pin Resistance

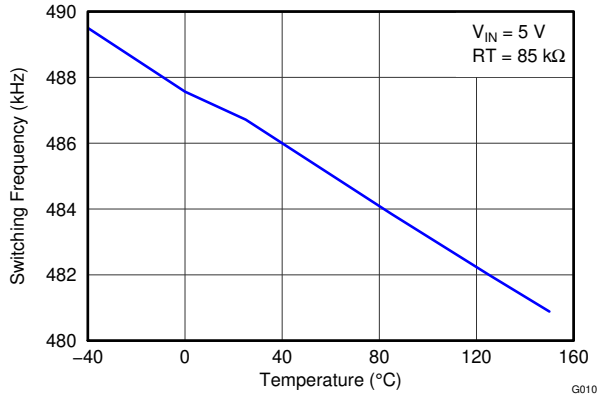


Figure 10. Switching Frequency vs Junction Temperature

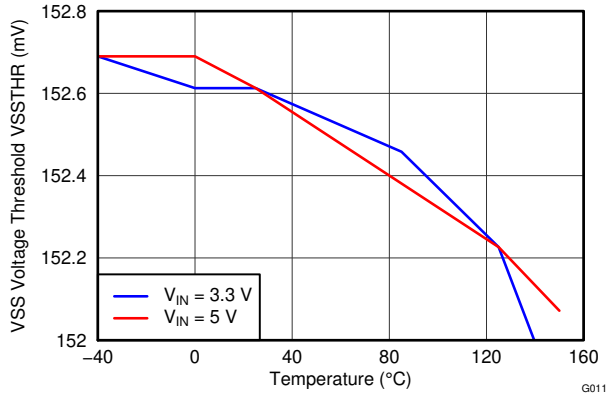


Figure 11. VSS Voltage Threshold vs Junction Temperature

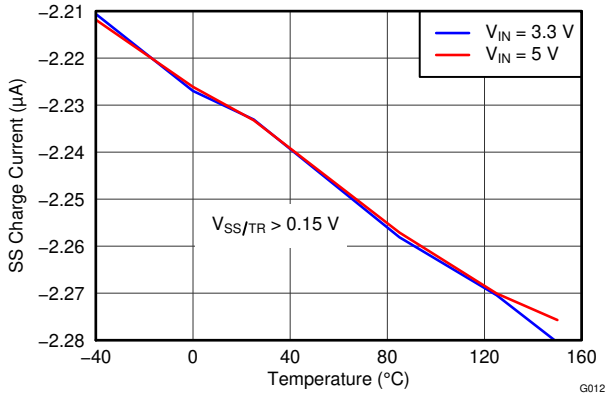


Figure 12. SS Charge Current vs Junction Temperature

Typical Characteristics (continued)

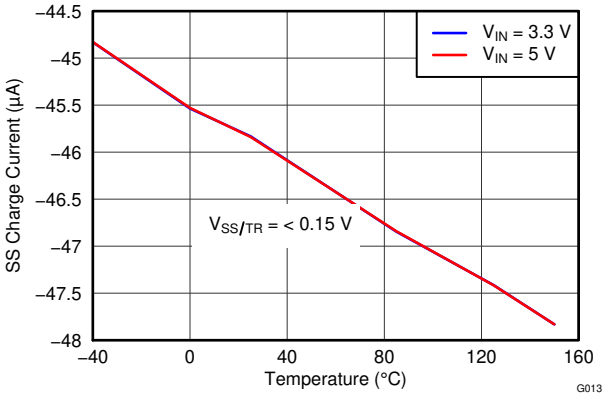


Figure 13. SS Charge Current vs Junction Temperature

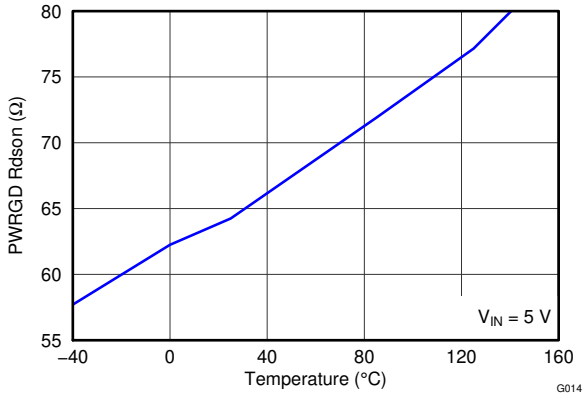


Figure 14. PWRGD $R_{ds(on)}$ vs Junction Temperature

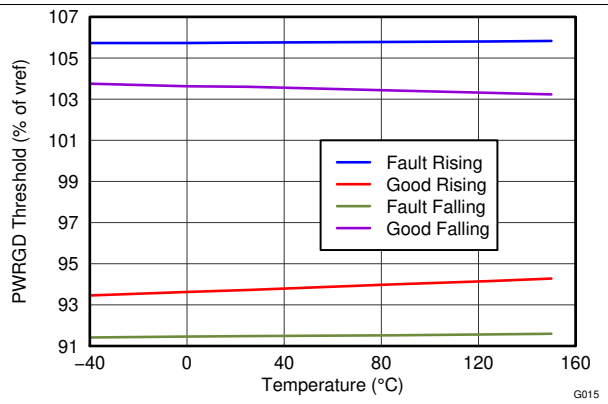


Figure 15. PWRGD Threshold vs Junction Temperature

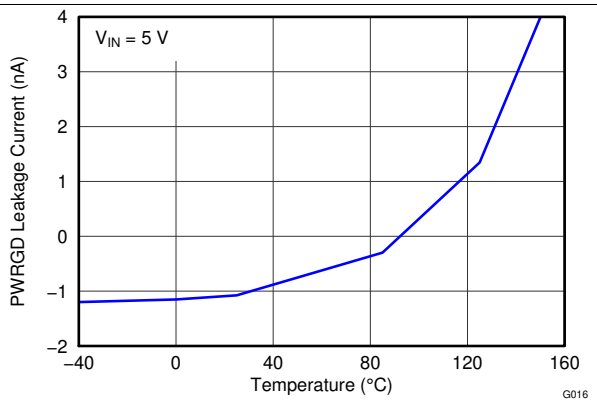


Figure 16. PWRGD Leakage Current vs Junction Temperature

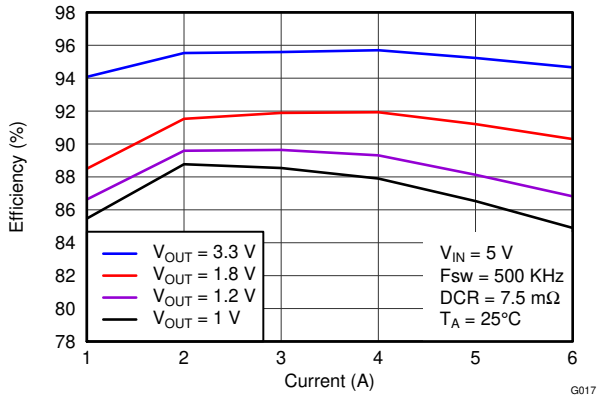


Figure 17. Efficiency vs Load Current

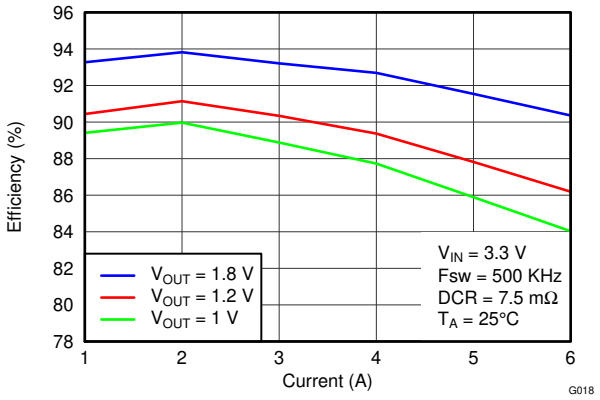


Figure 18. Efficiency vs Load Current

Typical Characteristics (continued)

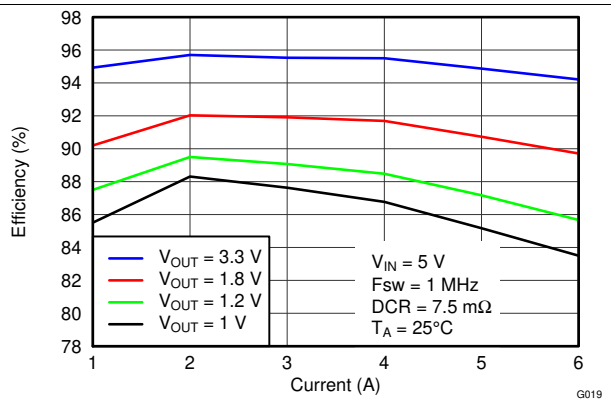


Figure 19. Efficiency vs Load Current

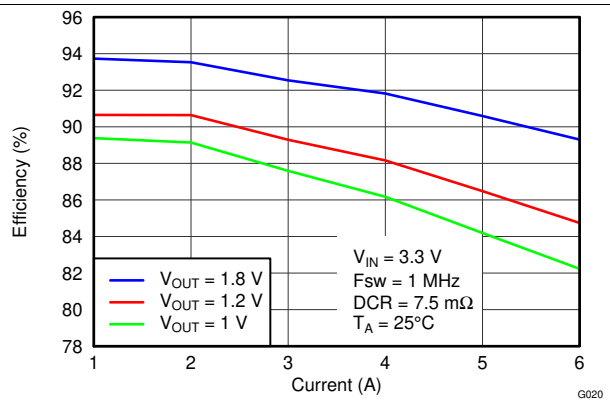


Figure 20. Efficiency vs Load Current

8 Detailed Description

8.1 Overview

The TPS54678 is a 6-V, 6-A, synchronous step-down (buck) converter with two integrated N-channel MOSFETs. To improve the performance during line and load transients the device implements a constant frequency, peak current mode control which reduces output capacitance and simplifies external frequency compensation design. The wide switching frequency range of 200 kHz to 2000 kHz allows for efficiency and size optimization when selecting the output filter components. The switching frequency is adjusted using a resistor to ground on the RT/CLK pin. The device has an internal phase lock loop (PLL) on the RT/CLK pin that is used to synchronize the power switch turn on to a falling edge of an external system clock.

The TPS54678 has a typical default start-up voltage of 2.4 V. The EN pin has an internal pullup current source that can be used to adjust the input voltage undervoltage lockout (UVLO) with two external resistors. In addition, the pullup current provides a default condition when the EN pin is floating for the device to operate. The total operating current for the TPS54678 is typically 570 µA when not switching and under no load. When the device is disabled, the supply current is less than 3 µA.

The integrated 12-mΩ MOSFETs allow for high-efficiency power supply designs with continuous output currents up to 6 amperes. The TPS54678 reduces the external component count by integrating the boot recharge diode. The bias voltage for the integrated high-side MOSFET is supplied by a capacitor between the BOOT and PH pins. The boot capacitor voltage is monitored by an UVLO circuit and turns off the high-side MOSFET when the voltage falls below a preset threshold. This BOOT circuit allows the TPS54678 to operate approaching 100%. The output voltage can be stepped down to as low as the 0.60-V reference.

TPS54678 features monotonic start-up under prebias conditions. The low-side FET turns on for a short time period every cycle before the output voltage reaches the prebiased voltage. This ensures the boot cap has enough charge to turn on the top FET when the output voltage reaches the prebiased voltage.

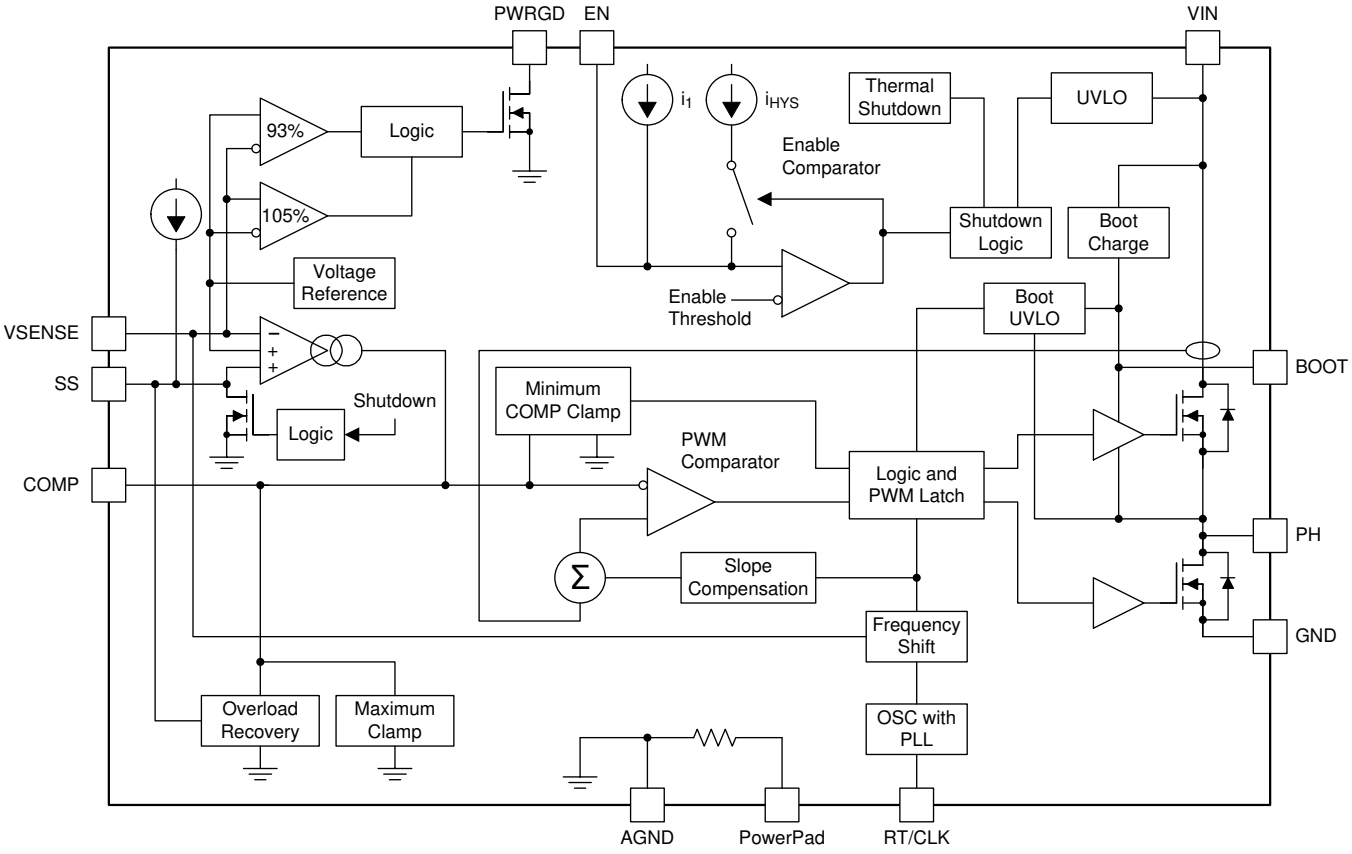
The TPS54678 has a power good comparator (PWRGD) with 2% hysteresis.

The TPS54678 minimizes excessive output overvoltage transients by taking advantage of the overvoltage power good comparator. When the regulated output voltage is greater than 105% of the nominal voltage, the overvoltage comparator is activated, and the high-side MOSFET is turned off and masked from turning on until the output voltage is lower than 103%.

The SS/TR (slow-start or tracking) pin is used to minimize inrush currents or provide power supply sequencing during power up. A small value capacitor should be coupled to the pin for slow-start. The SS/TR pin is discharged before the output power up to ensure a repeatable restart after an overtemperature fault, UVLO fault or disabled condition. To optimize the output startup waveform, two levels of SS current are implemented.

To reduce the power dissipation of TPS54678 during overcurrent event, the hiccup protection is implemented beyond the cycle-by-cycle protection.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Fixed Frequency PWM Control

The TPS54678 uses a settable fixed frequency, peak current mode control. The output voltage is compared through external resistors on the VSENSE pin to an internal voltage reference by an error amplifier which drives the COMP pin. An internal oscillator initiates the turn on of the high-side power switch. The error amplifier output is compared to the high-side power switch current. When the power switch current reaches the COMP voltage level the high-side power switch is turned off and the low-side power switch is turned on. The COMP pin voltage will increase and decrease as the output current increases and decreases. The device implements a current limit by clamping the COMP pin voltage to a maximum level and implements a sleep mode with a minimum clamp.

8.3.2 Slope Compensation and Output Current

The TPS54678 adds a compensating ramp to the switch current signal. This slope compensation prevents sub-harmonic oscillations. The available peak inductor current maintains constant over the full duty cycle range.

8.3.3 Bootstrap Voltage (Boot) and Low Dropout Operation

The TPS54678 has an integrated boot regulator and requires a small ceramic capacitor between the BOOT and PH pin to provide the gate drive voltage for the high-side MOSFET. The value of the ceramic capacitor should be 0.1 µF. A ceramic capacitor with an X7R or X5R grade dielectric is recommended because of the stable characteristics over temperature and voltage.

To improve dropout, the TPS54678 is designed to operate at 100% duty cycle as long as the BOOT to PH pin voltage is greater than 2.2 V. The high-side MOSFET is turned off using an UVLO circuit, allowing for the low-side MOSFET to conduct, when the voltage from BOOT to PH drops below 2.2 V. Because the supply current sourced from the BOOT pin is low, the high-side MOSFET can remain on for more switching cycles than are required to refresh the capacitor, thus the effective duty of the switching regulator is high.

Feature Description (continued)

8.3.4 Error Amplifier

The TPS54678 has a transconductance amplifier for the error amplifier. The error amplifier compares the VSENSE voltage to the lower of the SS/TR pin voltage or the internal 0.6-V voltage reference. The transconductance of the error amplifier is 245 µA/V during normal operation. During the slow-start operation, the transconductance is a fraction of the normal operating gm. The frequency compensation components are added to the COMP pin to ground.

8.3.5 Voltage Reference

The voltage reference system produces a precise ±1% voltage reference over temperature by scaling the output of a temperature stable bandgap circuit. During production, the bandgap and scaling circuits are trimmed to produce 0.6 V at the amplifier output.

8.3.6 Adjusting the Output Voltage

The output voltage is set with a resistor divider from the output node to the VSENSE pin. TI recommends using 1% tolerance or better divider resistors. Start with a 20-kΩ resistor for R1 and use Equation 1 to calculate R2. To improve efficiency at light loads, consider using larger value resistors. If the values are too high, the regulator will be more susceptible to noise and voltage errors from the VSENSE input current will be noticeable.

$$R2 = R1 \times \left(\frac{0.6\ V}{V_O - 0.6\ V} \right) \quad (1)$$

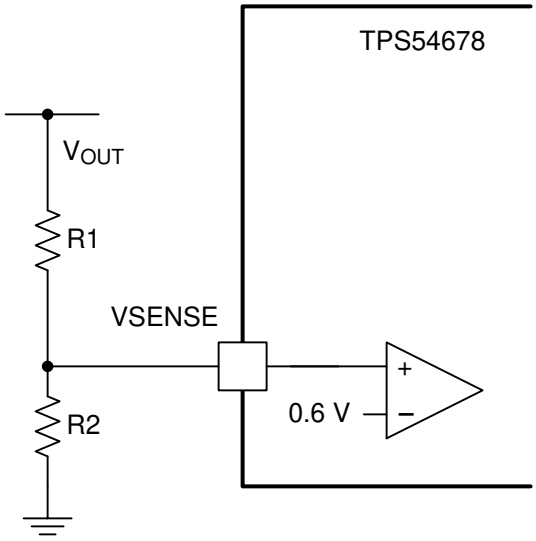


Figure 21. Voltage Divider Circuit

8.3.7 Enable and Adjusting Undervoltage Lockout

The EN pin provides electrical on and off control of the device. Once the EN pin voltage exceeds the threshold voltage, the device starts operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters low Iq state. If an application requires controlling the EN pin, use open drain or open collector output logic to interface with the pin.

For input undervoltage lockout (UVLO), use the EN pin as shown in Figure 22 to set up the UVLO by using the two external resistors. Once the EN pin voltage exceeds 1.3 V, an additional 2.8 µA of hysteresis is added. This additional current facilitates input voltage hysteresis. Use Equation 2 to set the external hysteresis for the input voltage. Use Equation 3 to set the input startup voltage. TI recommends that the minimum input shutdown voltage be set at 2.45 V or higher to ensure proper operation before shutdown.

Feature Description (continued)

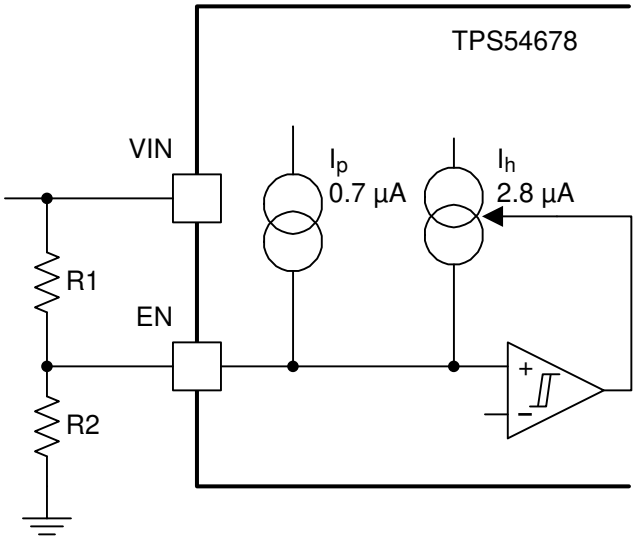


Figure 22. Set Up Input Undervoltage Lockout.

$$R1 = \frac{V_{START}\left(\frac{V_{EN\_FALLING}}{V_{EN\_RISING}}\right) - V_{STOP}}{I_p\left(1 - \frac{V_{EN\_FALLING}}{V_{EN\_RISING}}\right) + I_h} \quad (2)$$

$$R2 = \frac{R1 \times V_{EN\_FALLING}}{V_{STOP} - V_{EN\_FALLING} + R1 \times (I_p + I_h)}$$

where

- R_1 and R_2 are in Ω
- I_h = 2.8 µA
- I_p = 0.7 µA
- V_{EN_RISING} = 1.3 V
- $V_{EN\_FALLING}$ = 1.18 V (3)

8.3.8 Soft-Start Pin

TPS54678 effectively uses the lower voltage of the internal voltage reference or the SS/TR pin voltage as the reference voltage of the power supply and regulates the output accordingly. A capacitor on the SS/TR pin to ground will implement a slow-start time. The TPS54678 has an internal pullup current source of 47 µA when $V_{(SS/TR)}$ is less than 0.15 V and 2.2 µA when $V_{(SS/TR)}$ is higher than 0.15 V. The I_{SS} charges the external slow-start capacitor. The equation for the slow-start time is shown in Equation 4 considering the fact the first 47 µA charges the SS to 0.15 V. The 2.2 µA then charges the SS from 0.15 V to about 0.8 V for the handoff of the SS voltage to reference voltage.

$$Css(nF) = 3 \times Tss(mS) \quad (4)$$

If during normal operation, the VIN UVLO is exceeded, EN pin pulled below 1.2 V, or a thermal shutdown event occurs, the TPS54678 will stop switching and the SS/TR must be discharged to about 60 mV before reinitiating a powering-up sequence.

The VSENSE voltage will follow the SS/TR pin voltage up to 90% of the internal voltage reference. When the SS/TR voltage is greater than 90% of the internal voltage, the effective system reference voltage will transit from the SS/TR voltage to the internal voltage reference.

Feature Description (continued)

8.3.9 Sequencing

Many of the common power supply sequencing methods can be implemented using the SS/TR, EN and PWRGD pins. The sequential method can be implemented using an open-drain or collector output of a power on reset pin of another device. The sequential method is shown in Figure 23. The power good is coupled to the EN pin on the TPS54678, which will enable the second power supply once the primary supply reaches regulation.

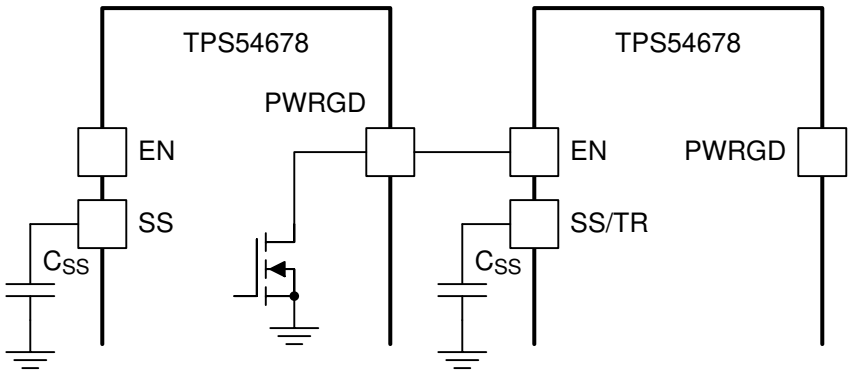


Figure 23. Sequential Start-Up Sequence

8.3.10 Constant Switching Frequency and Timing Resistor (RT/CLK Pin)

The switching frequency of the TPS54678 is adjustable over a wide range from approximately 200 kHz to 2000 kHz by placing a maximum of 210 kΩ and minimum of 18 kΩ, respectively, on the RT/CLK pin. The RT/CLK is typically 0.5 V. To determine the timing resistance for a given switching frequency, use the curve in Figure 24. To reduce the solution size one would typically set the switching frequency as high as possible, but tradeoffs of the supply efficiency, maximum input voltage and minimum controllable on time should be considered.

The minimum controllable on time is typically 85 ns at 3-A current load and 100 ns at no load, and will limit the maximum operating input voltage or output voltage.

$$R_T(k\Omega) = \frac{56183}{\left[F_{SW}(KHz)\right]^{1.052}} \quad (5)$$

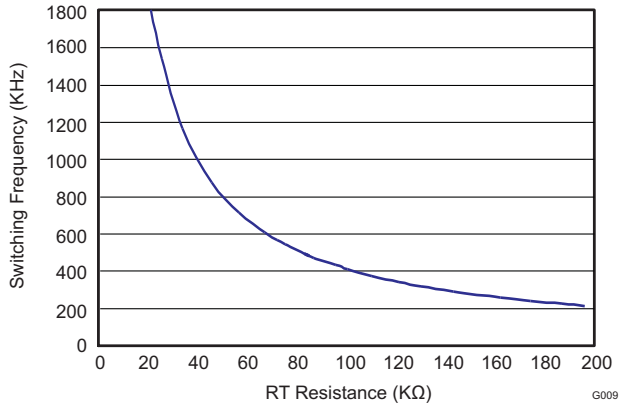


Figure 24. Switching Frequency vs RT Set Resistor

Feature Description (continued)

8.3.11 Overcurrent Protection

The TPS54678 implements current mode control which uses the COMP pin voltage to turn off the high-side MOSFET and turn on the low-side MOSFET on a cycle-by-cycle basis. Each cycle the switch current and the COMP pin voltage are compared, when the peak switch current intersects the COMP voltage the high-side switch is turned off.

8.3.11.1 High-Side Overcurrent Protection

During overcurrent conditions that pull the output voltage low, the error amplifier will respond by driving the COMP pin high, increasing the switch current. The error amplifier output is clamped internally. This clamp functions as a high-side switch current limit. When the high-side switch current limit occurs consecutively for 512 CLK cycles, the converter enters hiccup mode in which no switching action happens for about 16000 cycles. This helps to reduce the power consumption during an overcurrent event.

8.3.11.2 Low-Side Overcurrent Protection

The conduction current of the low-side MOSFET is also monitored by TPS54678. During normal operation, the low-side sources current into the load. When the sourcing current reaches the internally set low-side sourcing (forward) current limit, the high-side is not turned on and skipped during the next clock cycle. Under this condition, the low-side is kept on until the sourcing current becomes less than the internally set current limit and then the high-side is turned on at the beginning of the following clock cycle. This ensures protection under an output short condition; thereby, preventing current run-away.

The low-side can also sink current from the load. If the low-side sinking (reverse) current limit is exceeded, the low-side is turned off immediately for the rest of the clock cycle. Under this condition, both the high-side and low-side are off until the start of the next cycle.

8.3.12 Safe Start-Up into Prebiased Outputs

The TPS54678 allows monotonic start-up into prebiased output. The low-side FET turns on for a short time period every cycle before the output voltage reaches the prebiased voltage. This ensures the boot cap has enough charge to turn on the top FET when the output voltage reaches the prebiased voltage.

The TPS54678 also implements low-side current protection by detecting the voltage over the low-side MOSFET. When the converter sinks current through the low side FET and if the current exceeds 4 A, the control circuit turns the low-side FET off. Due to the implemented prebias function, the low-side FET reverse current protection should not be reached, but it provides another layer of protection.

8.3.13 Synchronize Using the RT/CLK Pin

The RT/CLK pin is used to synchronize the converter to an external system clock. See Figure 25. To implement the synchronization feature in a system connect a square wave to the RT/CLK pin with on time at least 75 ns. The square wave amplitude at this pin must transition lower than 0.6 V and higher than 1.6 V. The synchronization frequency range is 300 kHz to 2000 kHz. The rising edge of the PH will be synchronized to the falling edge of RT/CLK pin.

Feature Description (continued)

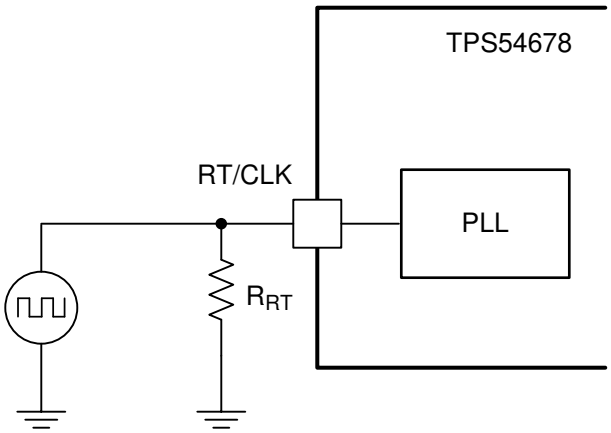


Figure 25. Synchronizing to a System Clock

8.3.14 Power Good (PWRGD Pin)

The PWRGD pin is an open-drain output and pulls the PWRGD pin low when the VSENSE voltage is less than 91% or greater than 105% of the nominal internal reference voltage.

There is a 2% hysteresis, so once the VSENSE pin is within 93% to 103% of the internal voltage reference the PWRGD pin is de-asserted and the pin floats. TI recommends to use a pullup resistor between the values of 1 kΩ and 100 kΩ to a voltage source that is 5.5 V or less. The PWRGD is in a valid state once the VIN input voltage is greater than 1.2 V.

8.3.15 Overvoltage Transient Protection

The TPS54678 incorporates an overvoltage transient protection (OVTP) circuit to minimize voltage overshoot when recovering from output fault conditions or strong unload transients. The OVTP feature minimizes the output overshoot by implementing a circuit to compare the VSENSE pin voltage to OVTP threshold which is 105% of the internal voltage reference. If the VSENSE pin voltage is greater than the OVTP threshold, the high-side MOSFET is disabled preventing current from flowing to the output and minimizing output overshoot. When the VSENSE voltage drops lower than the OVTP threshold the high-side MOSFET is allowed to turn on the next clock cycle.

8.3.16 Thermal Shutdown

The device implements an internal thermal shutdown to protect itself if the junction temperature exceeds 170°C. The thermal shutdown forces the device to stop switching when the junction temperature exceeds thermal trip threshold. When the die temperature decreases below 155°C, the device reinitiates the power-up sequence by discharging the SS/TR pin to about 60 mV. The thermal shutdown hysteresis is 15°C.

8.4 Device Functional Modes

8.4.1 Small Signal Model for Loop Response

The Figure 26 shows an equivalent model for the TPS54678 control loop that can be modeled in a circuit simulation program to check frequency response and dynamic load response. The error amplifier is a transconductance amplifier with a gm of 245 µA/V. The error amplifier can be modeled using an ideal voltage controlled current source. The resistor R_O and capacitor C_O model the open loop gain and frequency response of the amplifier.

Device Functional Modes (continued)

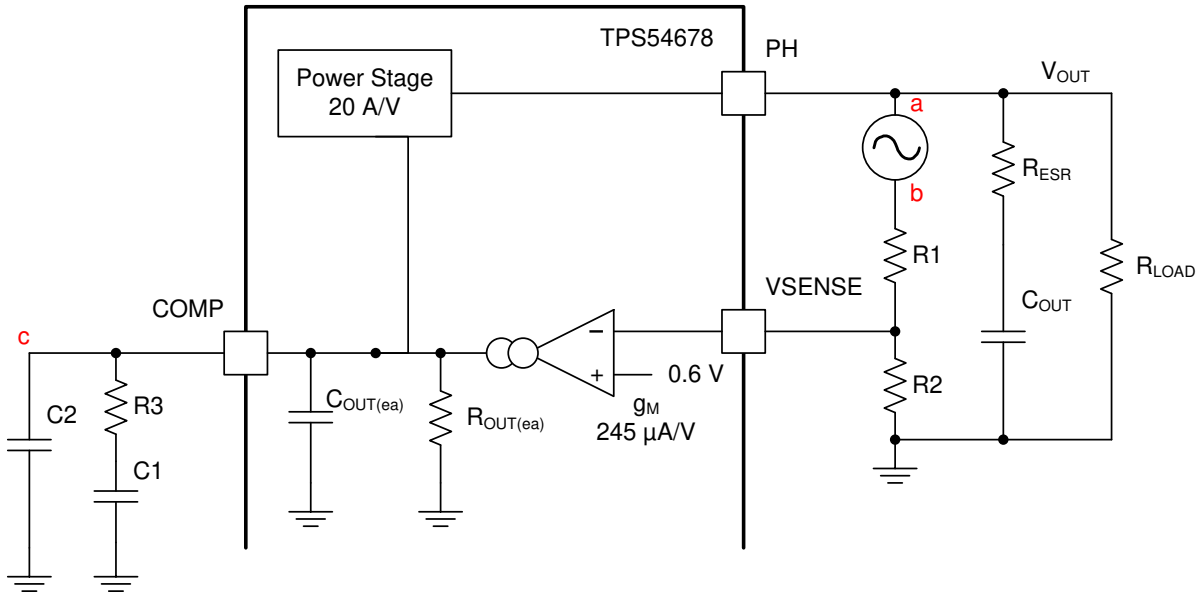


Figure 26. Small Signal Model for Loop Response

8.4.2 Simple Small Signal Model for Peak Current Mode Control

Figure 26 is a simple small signal model that can be used to understand how to design the frequency compensation. The TPS54678 power stage can be approximated to a voltage controlled current source (duty cycle modulator) supplying current to the output capacitor and load resistor. The control to output transfer function is shown in Equation 6 and consists of a DC gain, one dominant pole and one ESR zero. The quotient of the change in switch current and the change in COMP pin voltage (node c in Figure 26) is the power stage transconductance. The gm for the TPS54678 is 20 A/V. The low-frequency gain of the power stage frequency response is the product of the transconductance and the load resistance as shown in Equation 7. As the load current increases and decreases, the low-frequency gain decreases and increases, respectively. This variation with load may seem problematic at first glance, but fortunately the dominant pole moves with load current (see Equation 8). The combined effect is highlighted by the dashed line in Figure 28. As the load current decreases, the gain increases and the pole frequency lowers, keeping the 0-dB crossover frequency the same for the varying load conditions, which makes it easier to design the frequency compensation.

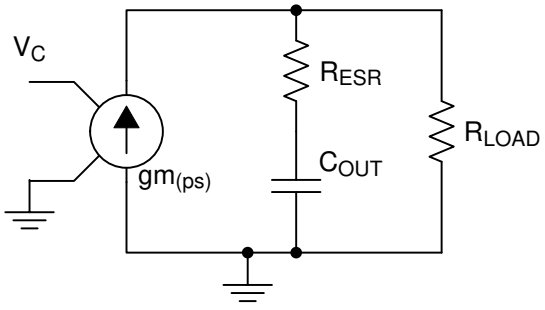


Figure 27. Small Signal Model For Peak Current Mode Control

Device Functional Modes (continued)

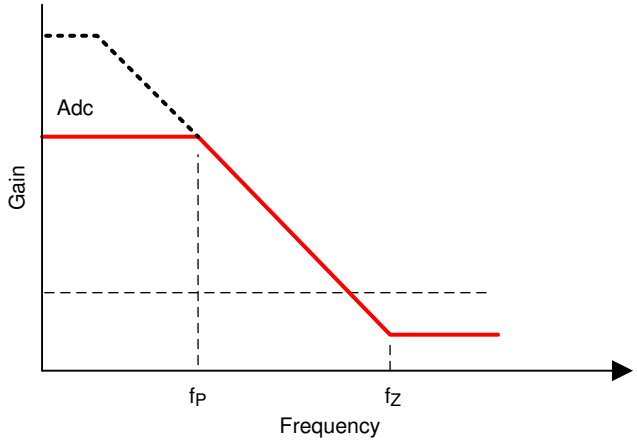


Figure 28. Frequency Response Model for Peak Current Mode Control

$$\frac{V_O}{V_C} = Adc \times \frac{\left(1 + \frac{s}{2\pi \times fz}\right)}{\left(1 + \frac{s}{2\pi \times fp}\right)} \quad (6)$$

$$Adc = gm_{ps} \times R_L \quad (7)$$

$$fp = \frac{1}{C_{OUT} \times R_L \times 2\pi} \quad (8)$$

$$fz = \frac{1}{C_{OUT} \times R_{ESR} \times 2\pi} \quad (9)$$

8.4.3 Small Signal Model for Frequency Compensation

The TPS54678 uses a transconductance amplifier for the error amplifier and readily supports two of the commonly used frequency compensation circuits. The compensation circuits are shown in Figure 29. The Type 2 circuits are normally implemented in high-bandwidth power supply designs using low ESR output capacitors. In Type 2A, one additional high-frequency pole is added to attenuate high-frequency noise.

Device Functional Modes (continued)

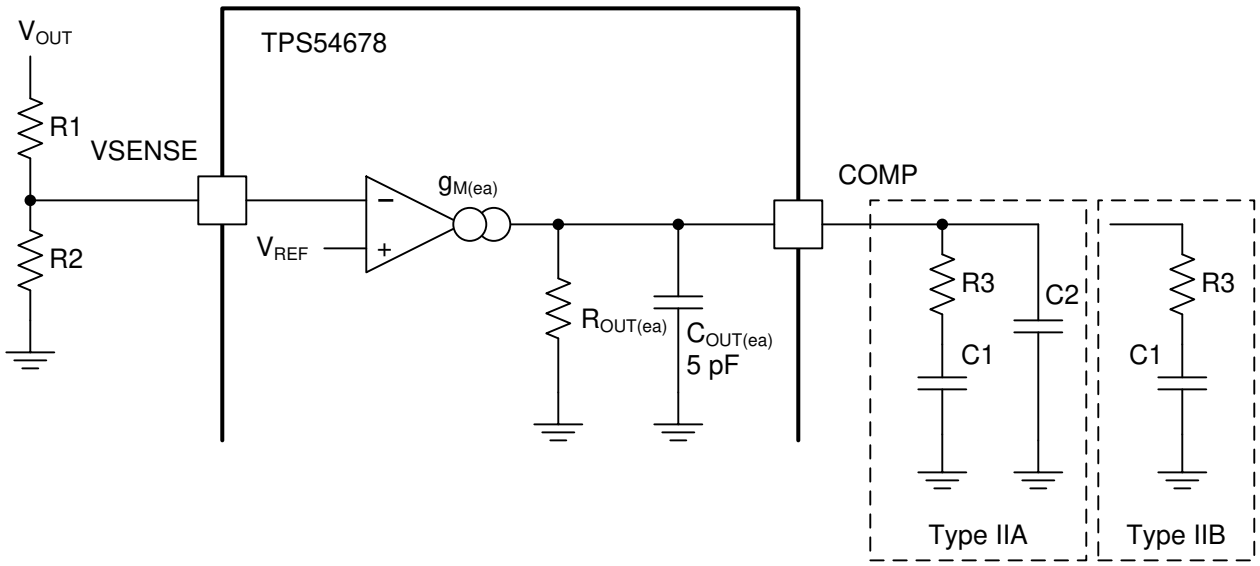


Figure 29. Types of Frequency Compensation

The design guidelines for TPS54678 loop compensation are as follows:

1. Set up crossover frequency fc.
2. R3 can be determined by Equation 10:

$$R3 = \frac{2\pi \times fc \times V_O \times C_{OUT}}{gm_{ea} \times V_{REF} \times gm_{ps}} \quad (10)$$

where

- gm_{ea} is the GM amplifier gain,
- gm_{PS} is the power stage gain (20 A/V).

3. Place a compensation zero at the dominant pole $fp = \frac{1}{C_{OUT} \times R_L \times 2\pi}$ C1 can be determined by Equation 11:

$$C1 = \frac{R_L \times C_{OUT}}{R3} \quad (11)$$

4. C2 is optional. It can be used to cancel the zero from ESR of the Co in Equation 12:

$$C2 = \frac{R_{ESR} \times C_{OUT}}{R3} \quad (12)$$

9 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This example details the design of a high-frequency switching regulator design using ceramic output capacitors. This design is available as the TPS54678EVM-155 (PWR155) evaluation module (EVM).

9.2 Typical Application

This section details a high-frequency, 1.2-V output power supply design application with adjusted UVLO.

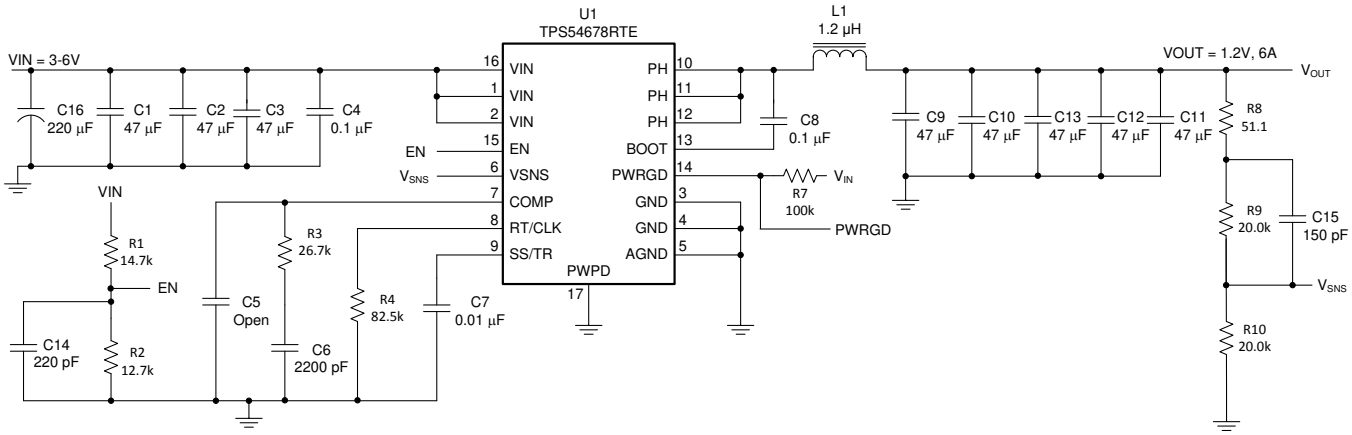


Figure 30. Typical Application Schematic, TPS54678

9.2.1 Design Requirements

Table 1 lists the design parameters of the TPS54678.

Table 1. Design Parameters

PARAMETER		NOTES AND CONDITIONS	MIN	TYP	MAX	UNIT
V_{IN}	Input voltage	Operating	3	5	6	V
V_{OUT}	Output voltage			1.2		V
ΔV_{OUT}	Transient response	3-A load step		5%		
$I_{OUT(max)}$	Maximum output current				6	A
$V_{OUT(ripple)}$	Output voltage ripple				30	mV_{P-P}
f_{SW}	Switching frequency			500		kHz

9.2.2 Detailed Design Procedure

9.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS54678 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost using the optimizer dial.
3. Compare the generated design with other possible solutions from Texas Instruments.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Run thermal simulations to understand board thermal performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

9.2.2.2 Step One: Select the Switching Frequency

The first step is to decide on a switching frequency for the regulator. Typically, it is desirable to choose the highest switching frequency possible since this produces the smallest component solution size. The high switching frequency allows for lower value inductors and smaller output capacitors compared to a power supply that switches at a lower frequency. However, the higher switching frequency causes extra switching losses, which degrade the performance of the converter. This SWIFT™ converter is capable of running from 200 kHz to 2 MHz. Unless a small solution size is the top priority, a moderate switching frequency of 500 kHz is selected to achieve both a small solution size and high-efficiency operation. Using Equation 13, R_T is calculated to be 81.34 kΩ. A standard 1% 82.5-kΩ value was chosen for the design.

$$R_T(k\Omega) = \frac{56183}{(F_{SW})^{1.052}} = \frac{56183}{(500)^{1.052}} = 81.34\ k\Omega \quad (13)$$

where

- R_T is in kΩ
- F_{SW} is in kHz

9.2.2.3 Step Two: Select the Output Inductor

The inductor selected works for the entire TPS54678 input voltage range. To calculate the value of the output inductor, use Equation 14. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high-inductor ripple currents impacts the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer, however K_{IND} is usually chosen between 0.1 to 0.3 for the majority of applications.

For this design example, a value of K_{IND} = 0.3 was used at 6 V_{IN} and 6 A_{OUT}, and the inductor value is calculated to be 1.06 µH. For this design, the nearest standard value of 1.2 µH was chosen. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The RMS and peak inductor current can be found from Equation 16 and Equation 17.

For this design, the RMS inductor current is 6.02 A and the peak inductor current is 6.8 A. The chosen inductor is a Coilcraft XAL5030-122ME. It has a saturation current rating 0f 11.8 A (20% inductance loss) and a RMS current rating of 8.7 A (20°C temperature rise). The series resistance is 6.78 mΩ typical.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

$$L1 = \frac{V_{IN\_MAX} - V_{OUT}}{I_o \times K_{IND}} \times \frac{V_{OUT}}{V_{IN\_MAX} \times F_{SW}} \quad (14)$$

$$I_{RIPPLE} = \frac{V_{IN\_MAX} - V_{OUT}}{L1} \times \frac{V_{OUT}}{V_{IN\_MAX} \times F_{SW}} \quad (15)$$

$$I_{IND\_RMS} = \sqrt{I_o^2 + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN\_MAX} - V_{OUT} \right)}{V_{IN\_MAX} \times L1 \times F_{SW}} \right)^2} \quad (16)$$

$$I_{IND\_peak} = I_o + \frac{I_{RIPPLE}}{2} \quad (17)$$

9.2.2.4 Step Three: Choose the Output Capacitor

There are three primary considerations for selecting the value of the output capacitor. Along with the inductor, the output capacitor determines the output voltage ripple, and also how the regulator responds to a large change in load current. The output capacitance needs to be selected based on the more stringent of these two criteria.

The desired response to a large change in the load current is the first criteria. The output capacitor needs to supply the load with current when the regulator can not due to limited control speed. The regulator is temporarily not able to supply sufficient change in output current if there is a large, fast increase or decrease in the current needs of the load such as transitioning from no load to full load. The regulator usually needs two or more clock cycles for the control loop to see the change in load current and output voltage and adjust the duty cycle to react to the change. The output capacitor must be sized to supply the extra current to the load until the control loop responds to the load change, or conversely, absorb the excess current from the inductor. Because the output voltage is less than half the input voltage, the worst-case deviation in output voltage occurs when the load has an extremely rapid reduction in current, or a load dump. The desired specification is a 50% or 3-A load step, and a resulting voltage deviation of no more than 5%, or 60mV. When a load dump occurs, the excess stored current in the inductor will tend to charge the output capacitors, and the best the converter can achieve to limit the increase in output voltage is to fold back the duty cycle to zero. Under these circumstances, the amount of rise in output voltage is defined by the energy from the choke being fully absorbed by the capacitor bank. Equation 18 through Equation 20 can be used to calculate the required capacitor bank value.

For this example, the transient load response is specified as a 5% change in Vout for a 50% load step from 3 A to 0 A. So, ΔI_{OUT} = 3 A and ΔV_{OUT} = 0.05 × 1.2 = 0.06 V. Using these numbers gives a minimum capacitance of 73.2 µF. This calculation does not take the ESR of the output capacitor into account in the output voltage change, and it does not account for latency in control loop speed. For ceramic capacitors, the ESR is usually small enough to ignore in this calculation.

$$Energy_{IND} = 0.5 \times L \times I^2 = 0.5 \times 1.2\mu \times 3^2 = 5.4\mu Joule \quad (18)$$

$$Energy_{CAP\,Initial} = 0.5 \times C \times V^2 = 0.5 \times C \times 1.2^2$$

$$Energy_{CAP\,Final} = 0.5 \times C \times 1.2^2 + Energy_{IND} = 0.5 \times C \times (1.2 + 0.06)^2 \quad (19)$$

Solving for C:

$$C_{Bank} = \frac{5.4\mu J}{(0.7938 - 0.72)} = 73.17\mu F \quad (20)$$

This 73.17 µF defines the minimum capacitance required to meet the transient spec; however, because the control loop speed is finite, more capacitance than this is required to meet desired performance.

Equation 21 calculates the minimum output capacitance needed to meet the output voltage ripple specification. In this case, the maximum output voltage ripple is 60 mV. Under this requirement, Equation 21 yields 13.33 µF.

$$C_{Bank} = \frac{1}{(8 \times F_{SW})} \times \frac{1}{\frac{V_{RIPPLE}}{I_{RIPPLE}}} = 13.33 \mu F$$

where

- F_{SW} is the switching frequency,
- V_{RIPPLE} is the maximum allowable output voltage ripple,
- and Iripple is the inductor ripple current. (21)

Equation 22 calculates the maximum ESR for the capacitor bank to meet the output voltage ripple specification. Equation 22 indicates the ESR should be less than 37.5 mΩ. In this case, the ESR of the ceramic capacitor bank is less than 37.5 mΩ.

$$R_{ESR} < \frac{V_{RIPPLE}}{I_{RIPPLE}} \quad (22)$$

Additional capacitance de-ratings for aging, temperature and DC bias should be factored in which increases the minimum value calculated in Equation 20. For this example, five 47-µF 10-V X5R ceramic capacitors with 3 mΩ of ESR are used. The estimated capacitance after derating is 5 × 47 µF × 0.9 = 211.5 µF.

9.2.2.5 Step Four: Select the Input Capacitor

The TPS54678 requires a high-quality ceramic, type X5R or X7R, input-decoupling capacitor of at least 10 µF of effective capacitance and in some applications a bulk capacitance. The effective capacitance includes any DC bias effects. The voltage rating of the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the TPS54678. The input ripple current can be calculated using Equation 23.

$$I_{RMS} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN\_MIN}} \times \frac{\left(V_{IN\_MIN} - V_{OUT}\right)}{V_{IN\_MIN}}} \quad (23)$$

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance to volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases.

For this example design, a ceramic capacitor with at least a 10-V voltage rating is required to support the maximum input voltage. For this example, three 47-µF and one 0.10-µF 10-V capacitors in parallel have been selected. In addition to these low ESR capacitors, an input bulk cap of 220-µF electrolytic is included so as to provide low source impedance at low frequencies for instances where the input voltage source is connected with a lossy feed.

The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using Equation 24. Using the design example values, I_{OUT_MAX} = 6 A, C_{IN} = 141 µF (neglecting the electrolytic due to high ESR), F_{SW} = 500 kHz, yields an input voltage ripple of 21.3 mV and an rms input ripple current of 2.94 A.

$$\Delta V_{IN} = \frac{I_{OUT\_MAX} \times 0.25}{C_{IN} \times F_{SW}} \quad (24)$$

9.2.2.6 Step Five: Choose the Soft-Start Capacitor

The slow-start capacitor determines the minimum amount of time it takes for the output voltage to reach the nominal programmed value during power up. This is useful if a load requires a controlled voltage slew rate. This is also used if the output capacitance is very large and would require large amounts of current to quickly charge the capacitor to the output voltage level. The large currents necessary to charge the capacitor may cause the TPS54678 to trip OCP, or excessive current draw from the input power supply may cause the input voltage rail to sag. Limiting the output voltage slew rate mitigates both of these issues.

The slow-start capacitor value can be calculated using Equation 25. For the example circuit, the slow-start time is not critical because the output capacitor value is 5 × 47 µF which does not require much current to charge to 1.2 V. The example circuit has the slow-start time set to an arbitrary value of 3.33 ms, which requires a 10-nF capacitor.

$$C_{SS} = 3 \times T_{SS} \tag{25}$$

9.2.2.7 Step Six: Select the Bootstrap Capacitor

A 0.1-µF ceramic capacitor must be connected between the BOOT and PH pins for proper operation. TI recommends to use a ceramic capacitor with X5R or better grade dielectric. The capacitor should have 10 V or higher voltage rating.

9.2.2.8 Step Eight: Select Output Voltage and Feedback Resistors

For the example design, 20 kΩ was selected for R10. Using Equation 26, R9 is calculated also as 20 kΩ.

$$R_9 = R_{10} \times \left(\frac{V_{OUT}}{V_{REF}} - 1 \right) \tag{26}$$

9.2.2.8.1 Output Voltage Limitations

Due to the internal design of the TPS54678, there is a minimum output voltage limit for any given input voltage. The output voltage can never be lower than the internal voltage reference of 0.6 V. Above 0.6 V, the output voltage may be limited by the minimum controllable ON-time. The minimum output voltage in this case is given by Equation 27.

$$V_{OUT\_MIN} = t_{ON\_MIN} \times F_{SW\_MAX} \left(V_{IN\_MAX} - I_{OUT\_MIN} \times R_{DS(ON)MIN} \right) - I_{OUT\_MIN} \times \left(R_L + R_{DS(ON)MIN} \right) \tag{27}$$

where

- V_{OUT_MIN} = minimum achievable output voltage
- t_{ON_MIN} = minimum controllable ON-time (100 ns typical, 120 ns no load)
- F_{SW_MAX} = maximum switching frequency including tolerance
- V_{IN_MAX} = maximum input voltage
- I_{OUT_MIN} = minimum load current
- $R_{DS(ON)\_MIN}$ = minimum high-side MOSFET ON-resistance (see *Electrical Characteristics*)
- R_L = series resistance of output inductor

There is also a maximum achievable output voltage which is limited by the minimum off time. The maximum output voltage is given by Equation 28.

$$V_{OUT\_MAX} = V_{IN} \times \left(1 - \frac{t_{OFF\_MAX}}{Period}\right) - I_{OUT\_MAX} \times \left(R_{DS(ON)MAX} + R_L\right) - \left(0.7 - I_{OUT\_MAX} \times R_{DS(ON)MAX}\right) \times \left(\frac{t_{DEAD}}{Period}\right)$$

where

- V_{OUT_MAX} = maximum achievable output voltage
- V_{IN} = minimum input voltage
- t_{OFF_MAX} = maximum OFF-time (180 ns typical for adequate margin)
- Period = 1/Fs
- I_{OUT_MAX} = maximum current
- $R_{DS(ON)\_MAX}$ = maximum high-side MOSFET ON-resistance (see *Electrical Characteristics*)
- R_L = DCR of the inductor
- t_{DEAD} = dead time (40 ns) (28)

9.2.2.9 Step Nine: Select Loop Compensation Components

There are several possible methods to design closed-loop compensation for DC/DC converters. For the ideal current mode control, the design equations can be easily simplified. The power stage gain is constant at low frequencies, and rolls off at –20 dB/decade above the modulator pole frequency. The power stage phase is zero degrees at low frequencies and starts to fall one decade below the modulator pole frequency reaching a minimum of –90 degrees one decade above the modulator pole frequency. In this case the modulator pole is a simple pole shown in Equation 29.

$$F_{PMOD} = \frac{1}{2\pi C_{OUT} R_{LOAD}} \quad (29)$$

For the TPS54678 most circuits will have relatively high amounts of slope compensation. As more slope compensation is applied, the power stage characteristics will deviate from the ideal approximations. The phase loss of the power stage will extend beyond –90 degrees and can approach –180 degrees, making compensation more difficult. The power stage transfer function can be solved but it is a tedious hand calculation that does not lend itself to simple approximations. It is easier to either simulate the circuit or to actually measure the plant transfer function so that a reliable compensation circuit can be designed. The latter technique used in this design procedure. The power stage plant was measured and is shown in Figure 31.

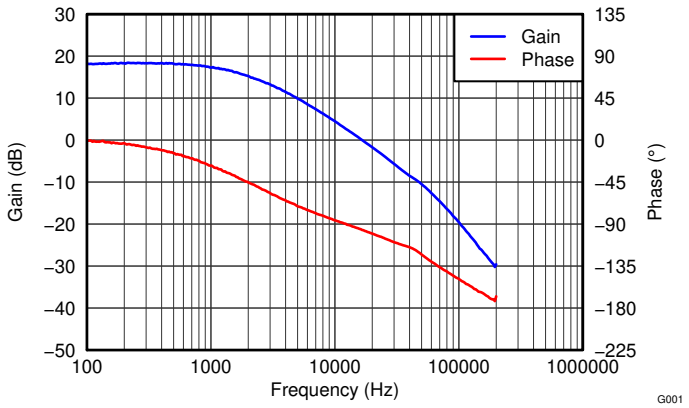


Figure 31. Measured Plant Bode

For this design, the desired crossover frequency Fc is 50 kHz. From the power stage gain and phase plot above, the gain at 50 kHz is –10.6 dB and the phase is –123.3 degrees. Because the plant phase loss is greater than –90 degrees, to achieve at least 60 degrees of phase margin, additional phase boost from a feedforward capacitor in parallel with the upper resistor of the voltage set point divider is required.

See the schematic in Figure 30. R3 sets the gain of the compensated error amplifier to be equal and opposite (in dB) to the power stage gain at Fc, so 10.6 dB is needed. The required value of R3 can be calculated from Equation 30.

$$R_3 = \frac{10^{\left(\frac{-G_{Plant}}{20}\right)}}{gm_{EA}} \times \sqrt{\frac{V_{OUT}}{V_{REF}}} \tag{30}$$

The compensator zero formed by R3 and C6 is placed at the plant pole, as shown approximately 2.5 kHz. The required value for C6 is given by Equation 31.

$$C_6 = \frac{1}{2\pi R_3 F_{plant\,pole}} \tag{31}$$

The high-frequency noise pole formed by C5 and R3 is not used in this design. If the resulting design shows noise susceptibility, the value of C5 can be calculated per Equation 32.

$$C_5 = \frac{1}{2\pi R_3 F_{pole}} \tag{32}$$

To avoid a penalty in loop phase, the Fpole in Equation 32 should be placed a decade above Fc or higher, and is intended to reject noise at F_{SW}.

The feedforward capacitor C15 is used to increase the phase boost at crossover above what is normally available from Type II compensation. It places an additional zero/pole pair with the zero located at Equation 33 and the pole at Equation 34.

$$F_z = \frac{1}{2\pi C_{15} R_9} \tag{33}$$

$$F_p = \frac{1}{2\pi C_{15} \left(R_9 \,||\, R_{10}\right)} \tag{34}$$

This zero and pole pair is not independent since R9 and R10 are set by the desired V_{OUT}. Once the zero location is chosen, the pole is fixed as well. For optimum performance, the zero and pole should be located symmetrically about the intended crossover frequency. The required value for C15 can be calculated from Equation 35.

$$C_{15} = \frac{1}{2\pi R_9 F_c \sqrt{\frac{V_{REF}}{V_{OUT}}}} \tag{35}$$

Table 2 lists the values the compensation equations yield.

Table 2. Frequency Compensation Component Values

REF DES	CALCULATED VALUE	CHOSEN VALUE
R3	19.6 kΩ	26.7 kΩ
C6	2.38 nF	2.2 nF
C15	225 pF	150 pF

9.2.3 Application Curves

Figure 32 through Figure 47 were measured on the TPS54678 Evaluation Module. More explanation of waveforms, as well as a schematic document can be found in the *TPS54678EVM-155 6-A, SWIFT™ Regulator Evaluation Module* user guide, SLVU747.

9.2.3.1 Additional Information About Application Curves

9.2.3.1.1 Efficiency

System efficiency may be lower than shown in Figure 32 at higher ambient temperatures, due to temperature variation in the drain-to-source resistance $R_{DS(ON)}$ of the internal MOSFETs.

9.2.3.1.2 Voltage Ripple Measurements

Probe placement and noise pickup can give unreliable voltage ripple results. Figure 37 and Figure 38 show the output voltage ripple of the converter, measured directly across the output capacitors. Likewise, Figure 39 and Figure 40 show the input voltage ripple of the converter, measured directly across the input capacitors.

9.2.3.1.3 Start-Up and Shutdown Waveforms

Figure 41 and Figure 42 show the start-up waveforms for the TPS54678EVM-155. In Figure 41, the output voltage ramps up as soon as the input voltage reaches the UVLO threshold as set by the R1 and R2 resistor divider network. In Figure 42, the input voltage is initially applied and the output is inhibited by using a jumper at JP1 to tie EN to GND. When the jumper is removed, EN is released. When the EN voltage reaches the enable-threshold voltage, the start-up sequence begins and the output voltage ramps up to the externally set value of 1.2 V.

The TPS54678 is designed to start up into prebiased outputs. Figure 43 shows the output voltage start-up waveform when the output is prebiased with 550 mV at no load.

Figure 44 and Figure 45 show the shutdown waveforms for the TPS54678EVM-155. In Figure 44, the output voltage ramps down as soon as the input voltage falls below the UVLO stop threshold as set by the R1 and R2 resistor divider network. At the point of shutdown, the input voltage rises slightly due to the resistive drop in the input feed impedance. In Figure 45, the output is inhibited by using a jumper at JP1 to tie EN to GND.

9.2.3.1.4 Hiccup Mode Current Limit

The TPS54678 has hiccup mode current limit. When the peak switch current exceeds the current limit threshold, the device shuts down and restarts. Hiccup mode current limit operation is shown in Figure 46 and Figure 47. Figure 46 shows the hiccup mode current limit with a slight resistive overload. When the peak current limit is exceeded, the output voltage is disabled. Figure 47 shows the operation of the TPS54678 with the output shorted to ground. The device continuously resets until the fault condition is removed.

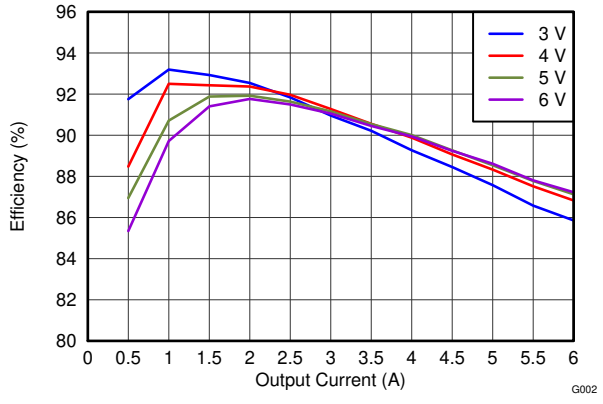


Figure 32. Efficiency vs Load Current

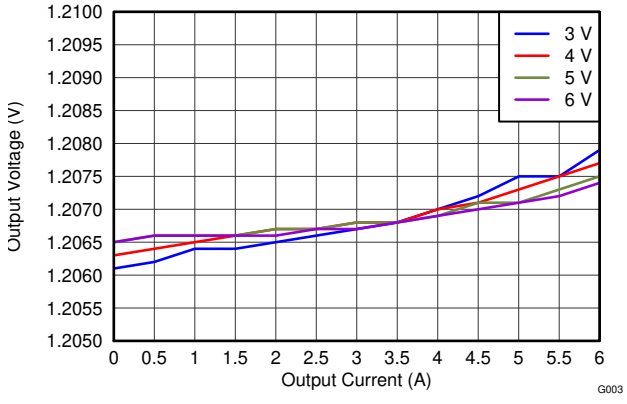


Figure 33. Load Regulation

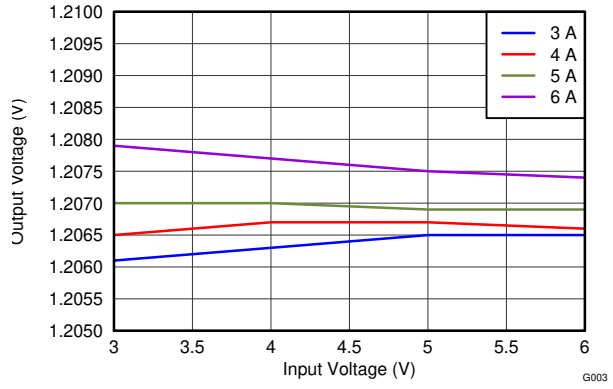


Figure 34. Line Regulation

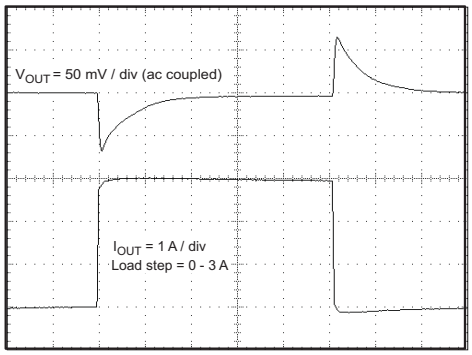


Figure 35. Transient Response

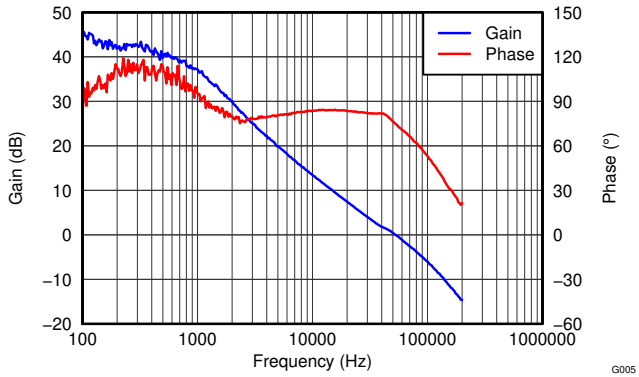
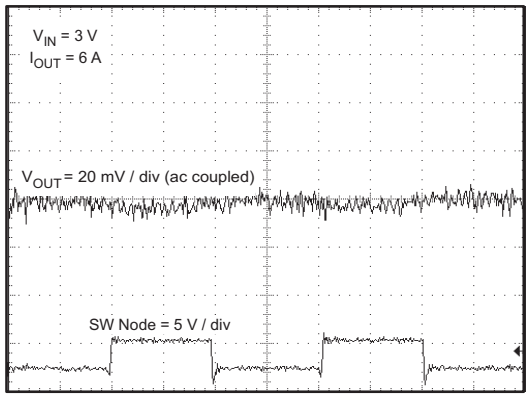
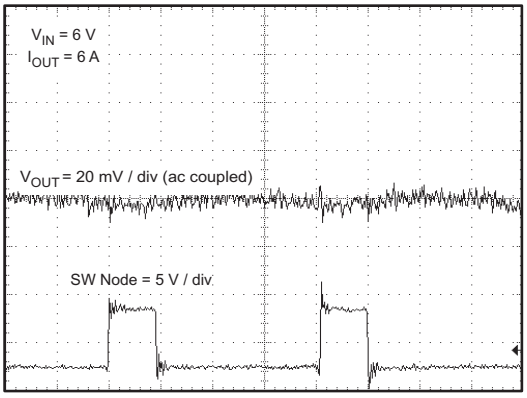


Figure 36. Loop Response



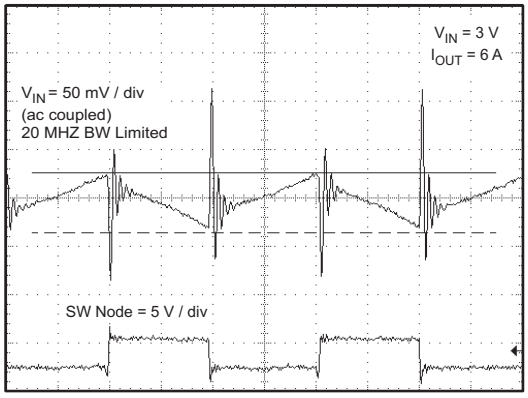
V_{IN} = 3 V, I_{OUT} = 6 A

Figure 37. Output Ripple



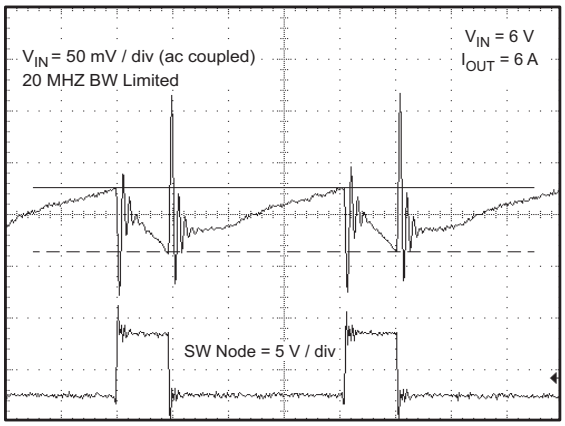
V_{IN} = 6 V, I_{OUT} = 6 A

Figure 38. Output Ripple



V_{IN} = 3 V, I_{OUT} = 6 A

Figure 39. Input Ripple



V_{IN} = 6 V, I_{OUT} = 6 A

Figure 40. Input Ripple

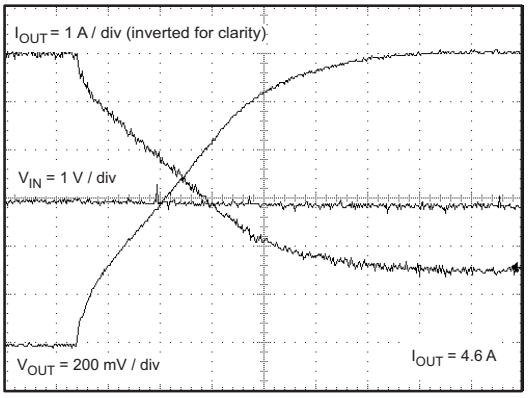


Figure 41. Start-Up Relative to V_{IN}

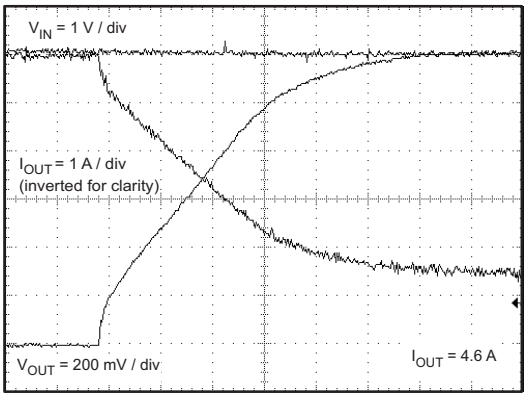


Figure 42. Start-Up Relative to Enable

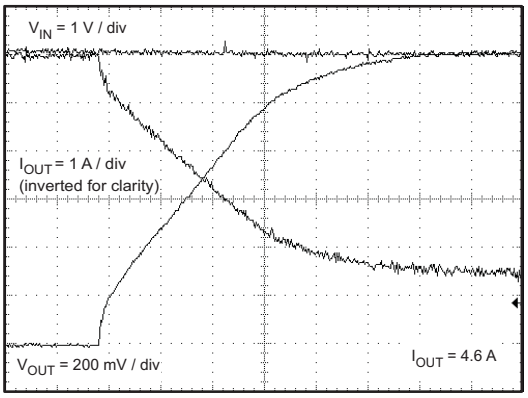


Figure 43. Start-Up into Prebias

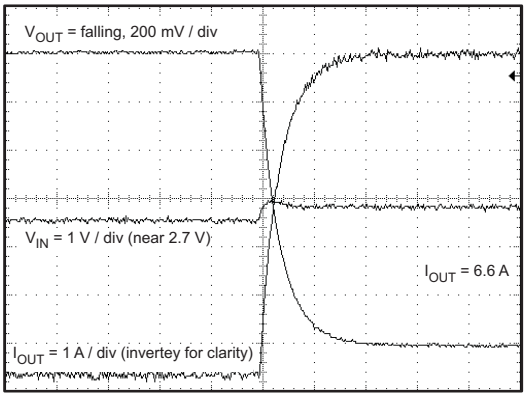


Figure 44. Shutdown Relative to V_{IN}

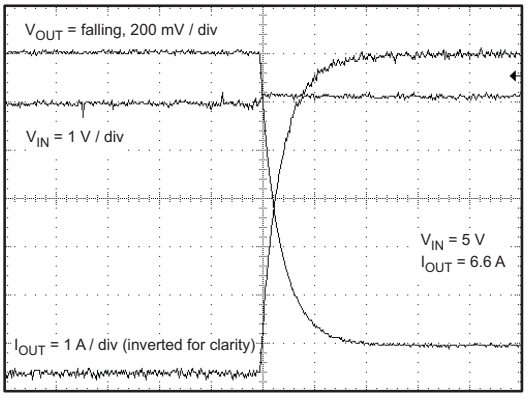


Figure 45. Shutdown Relative to Enable

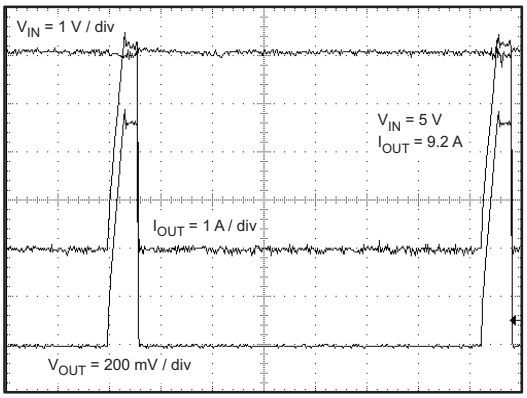


Figure 46. Hiccup Mode Current Limit Shutdown

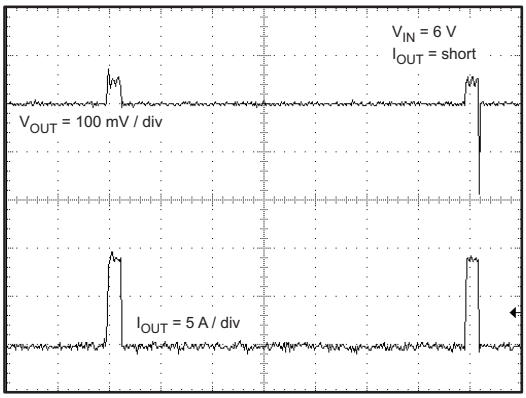


Figure 47. Hiccup Mode Current Limit Restart into Short Circuit

10 Power Supply Recommendations

These devices are designed to operate from an input voltage supply between 2.95 V and 6 V. This supply must be well regulated. Proper bypassing of input supplies and internal regulators is also critical for noise performance, as is PCB layout and grounding scheme. See the recommendations in the *Layout Guidelines* section.

11 Layout

11.1 Layout Guidelines

Layout is a critical portion of good power supply design. There are several signal paths that conduct fast changing currents or voltages that can interact with stray inductance or parasitic capacitance to generate noise or degrade the power supplies performance.

- Minimize the loop area formed by the bypass capacitor connections and the VIN pins. See Figure 48 for a PCB layout example.
- Tie the GND pins and AGND pin directly to the thermal pad under the TPS54678 device. Connect the thermal pad to any internal PCB ground planes using multiple vias directly under the device. Additional vias can be used to connect the top-side ground area to the internal planes near the input and output capacitors. For operation at full rated load, the top-side ground area along with any additional internal ground planes must provide adequate heat dissipating area.
- Place the input bypass capacitor as close as possible to the device.
- Route the PH pin to the output inductor. Because the PH connection is the switching node, place the output inductor close to the PH pins. Minimize the area of the PCB conductor to prevent excessive capacitive coupling.
- The boot capacitor must also be located close to the device.
- The sensitive analog ground connections for the feedback voltage divider, compensation components, soft-start capacitor and frequency set resistor must be connected to a separate analog ground trace as shown in Figure 48.
- The RT/CLK pin is particularly sensitive to noise so the RT resistor should be located as close as possible to the device and routed with minimal trace lengths.
- The additional external components can be placed approximately as shown. It is possible to obtain acceptable performance with alternate PCB layouts, however, this layout has been shown to produce good results and can be used as a guide.

11.2 Layout Example

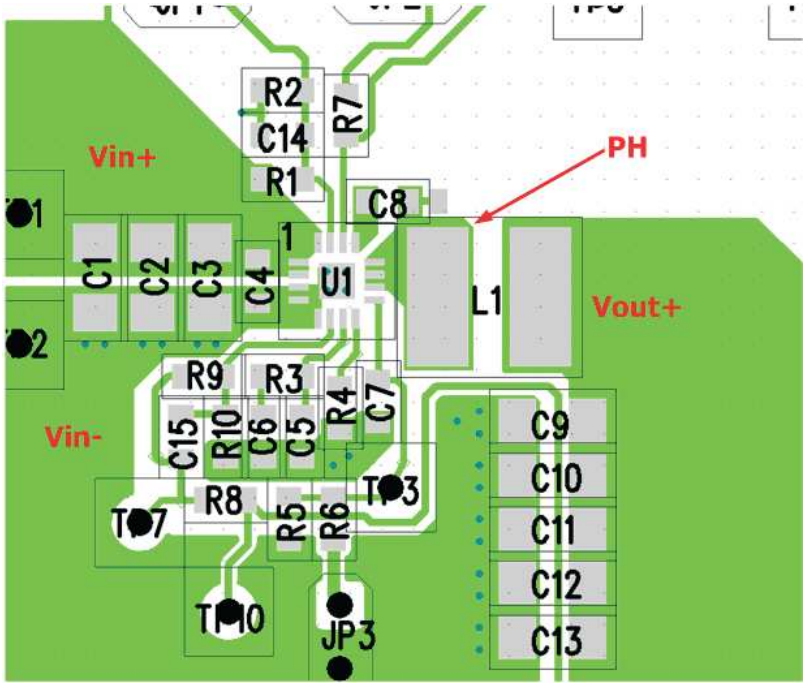


Figure 48. TPS54678 Layout Example

11.3 Power Dissipation Estimate

The following formulas show how to estimate the IC power dissipation under continuous conduction mode (CCM) operation. The power dissipation of the IC (Ptot) includes conduction loss (P_{con}), dead time loss (P_d), switching loss (P_{sw}), gate drive loss (P_{gd}) and supply current loss (P_q).

$P_{con} = I_O^2 \times R_{DS(on)}$ (temperature dependent)

where

- I_O is the output current (A)
- $R_{DS(on)}$ is the on-resistance of the high-side MOSFET with given temperature (Ω) (36)

$Pd = f_{sw} \times I_O \times 0.7 \times (20\ nS + 20\ nS)$

where

- I_O is the output current (A)
- f_{sw} is the switching frequency (Hz) (37)

$P_{sw} = 0.5 \times V_{IN} \times I_O \times f_{sw} \times 7 \times 10^{-9}$

where

- I_O is the output current (A)
- V_{IN} is the input voltage (V)
- f_{sw} is the switching frequency (Hz) (38)

$P_{gd} = 2 \times V_{IN} \times f_{sw} \times 6 \times 10^{-9}$

where

- V_{IN} is the input voltage (V)
- f_{sw} is the switching frequency (Hz) (39)

$P_q = V_{IN} \times 500 \times 10^{-6}$

where

- V_{IN} is the input voltage (V) (40)

Power Dissipation Estimate (continued)

So

$$P_{tot} = P_{con} + P_d + P_{sw} + P_{gd} + P_q$$

where

- P_{tot} is the total device power dissipation (W)

(41)

For given T_A,

$$T_J = T_A + R_{th} \times P_{tot}$$

where

- P_{tot} is the total device power dissipation (W)
- T_A is the ambient temperature (°C)
- T_J is the junction temperature (°C)
- Rth is the thermal resistance of the package (°C/W)

(42)

For given T_J max = 150°C

$$T_A \text{ max} = T_J \text{ max} – R_{th} \times P_{tot}$$

where

- P_{tot} is the total device power dissipation (W)
- Rth is the thermal resistance of the package (°C/W)
- T_J max is maximum junction temperature (°C)
- T_A max is maximum ambient temperature (°C)

(43)

There are additional power losses in the regulator circuit due to the inductor AC and DC losses and trace resistance that impact the overall efficiency of the regulator.

12 デバイスおよびドキュメントのサポート

12.1 デバイス・サポート

12.1.1 デベロッパー・ネットワークの製品に関する免責事項

デベロッパー・ネットワークの製品またはサービスに関するTIの出版物は、単独またはTIの製品、サービスと一緒に提供される場合に関係なく、デベロッパー・ネットワークの製品またはサービスの適合性に関する是認、デベロッパー・ネットワークの製品またはサービスの是認の表明を意味するものではありません。

12.1.2 開発サポート

SWIFT™の他のドキュメントについては、TI Webサイトのwww.ti.com/swiftを参照してください。

12.1.2.1 WEBENCH®ツールによるカスタム設計

ここをクリックすると、WEBENCH® Power Designer により、TPS54678 デバイスを使用するカスタム設計を作成できます。

1. 最初に、入力電圧(V_{IN})、出力電圧(V_{OUT})、出力電流(I_{OUT})の要件を入力します。
2. オプティマイザのダイヤルを使用して、効率、占有面積、コストなどの主要なパラメータについて設計を最適化します。
3. 生成された設計を、テキサス・インスツルメンツが提供する他の方式と比較します。

WEBENCH Power Designerでは、カスタマイズされた回路図と部品リストを、リアルタイムの価格と部品の在庫情報と併せて参照できます。

通常、次の操作を実行可能です。

- 電気的なシミュレーションを実行し、重要な波形と回路の性能を確認する。
- 熱シミュレーションを実行し、基板の熱特性を把握する。
- カスタマイズされた回路図やレイアウトを、一般的なCADフォーマットで出力する。
- 設計のレポートをPDFで印刷し、設計を共有する。

WEBENCHツールの詳細は、www.ti.com/WEBENCHでご覧になれます。

12.2 ドキュメントのサポート

12.2.1 関連資料

関連資料については、以下を参照してください。

『TPS54678EVM-155 6-A, SWIFT™ Regulator Evaluation Module』(英語)

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.5 商標

SWIFT, E2E are trademarks of Texas Instruments.
WEBENCH is a registered trademark of Texas Instruments.
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12.6 静電気放電に関する注意事項

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12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS54678RTER	ACTIVE	WQFN	RTE	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54678	Samples
TPS54678RTET	ACTIVE	WQFN	RTE	16	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 150	54678	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

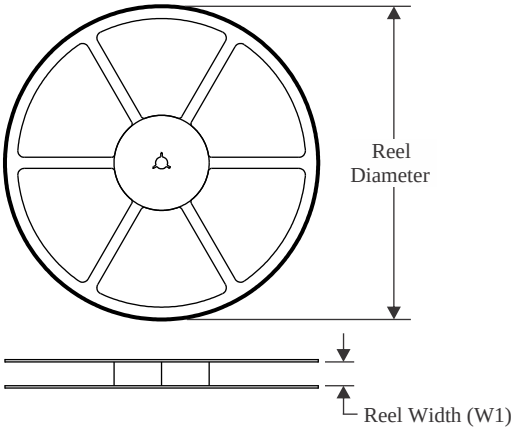
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

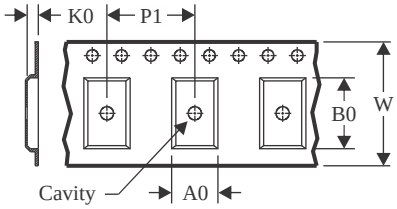
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

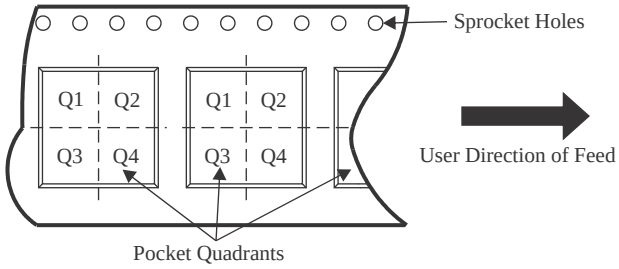


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

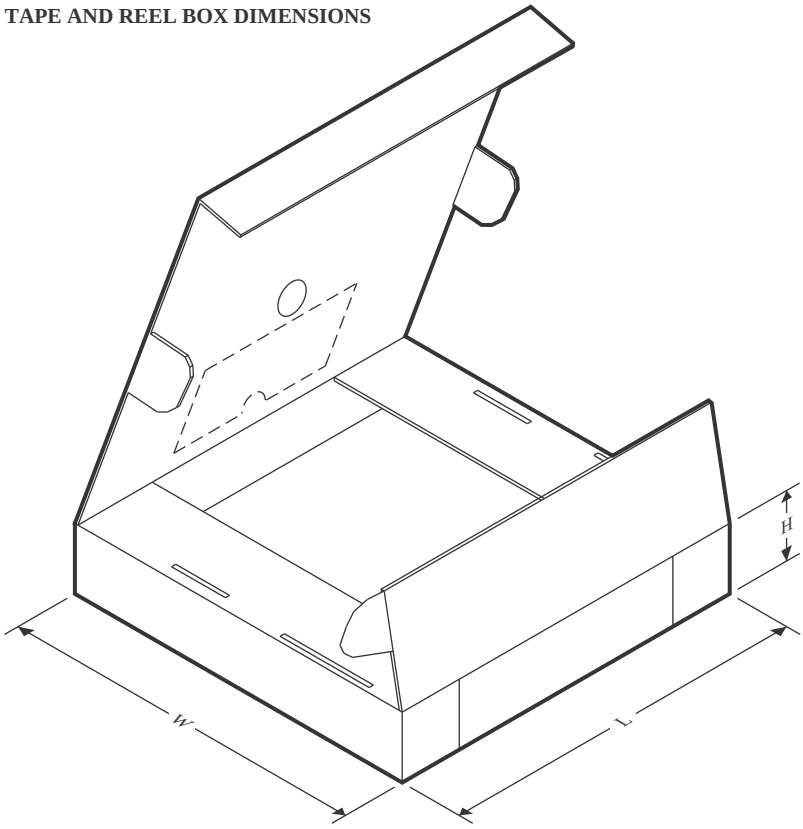
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS54678RTER	WQFN	RTE	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS54678RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS54678RTET	WQFN	RTE	16	250	180.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS54678RTER	WQFN	RTE	16	3000	346.0	346.0	33.0
TPS54678RTET	WQFN	RTE	16	250	210.0	185.0	35.0
TPS54678RTET	WQFN	RTE	16	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

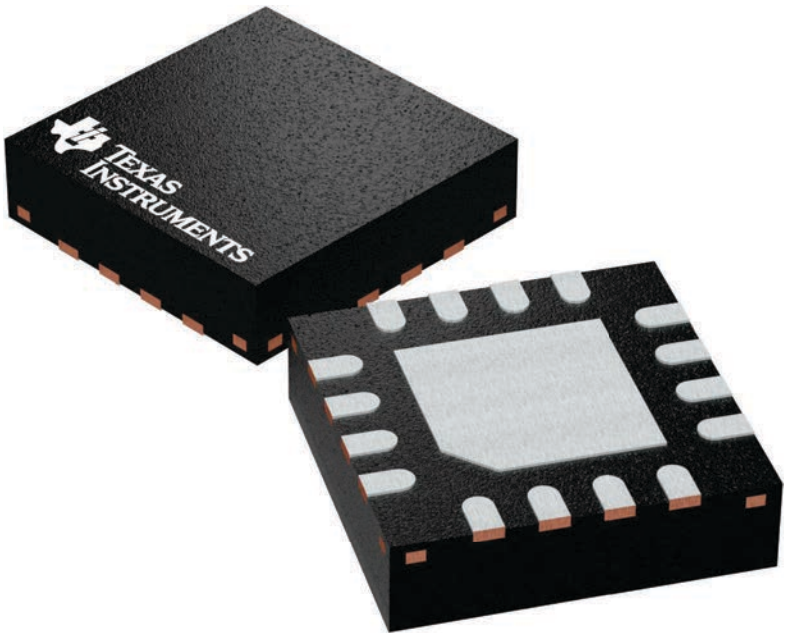
RTE 16

WQFN - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC QUAD FLATPACK - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

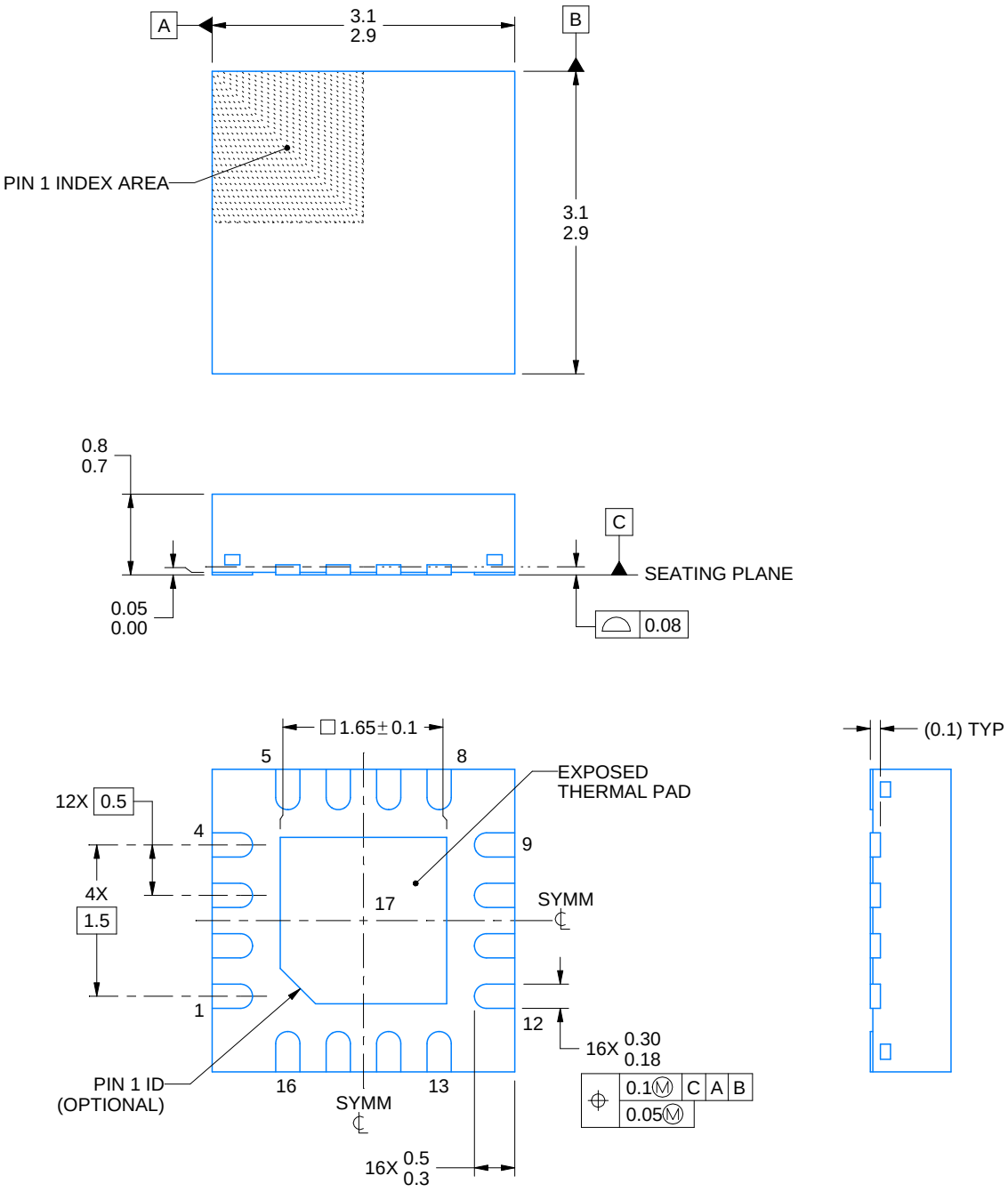


RTE0016F

PACKAGE OUTLINE

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

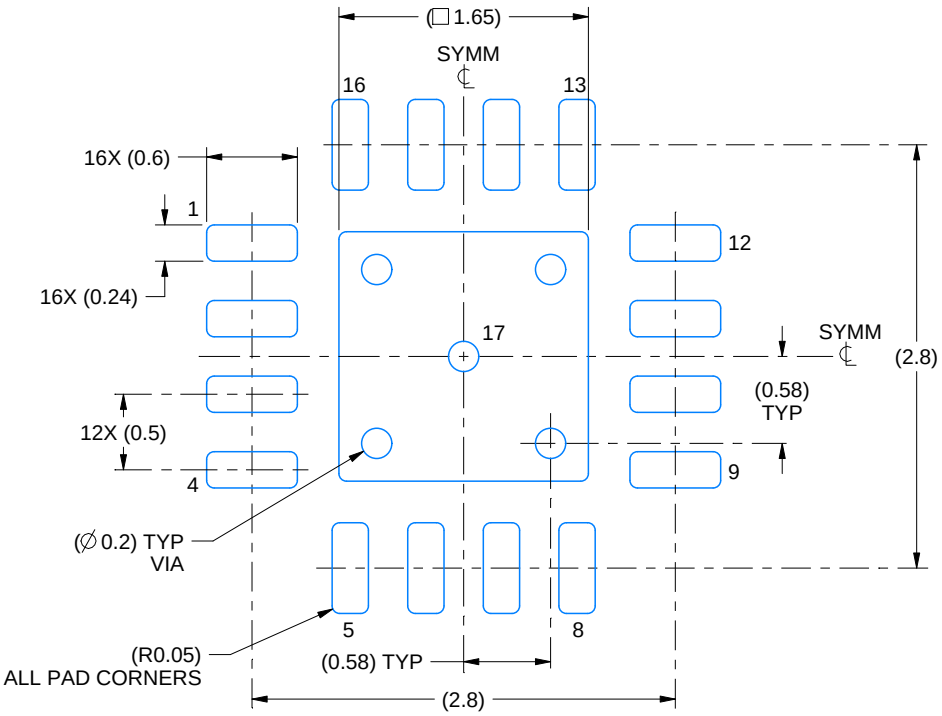
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

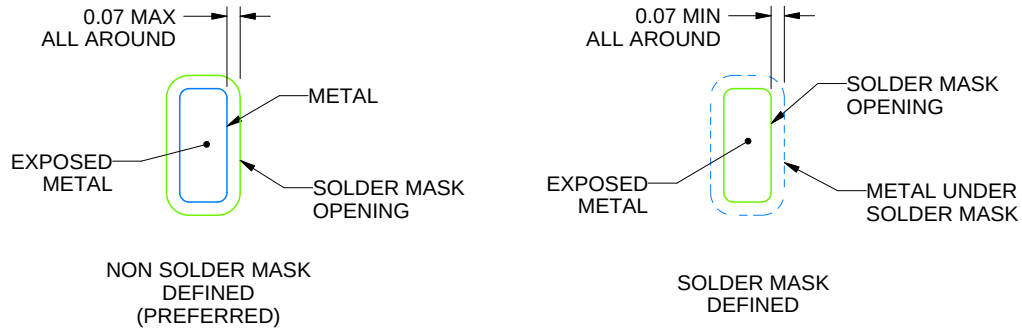
RTE0016F

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

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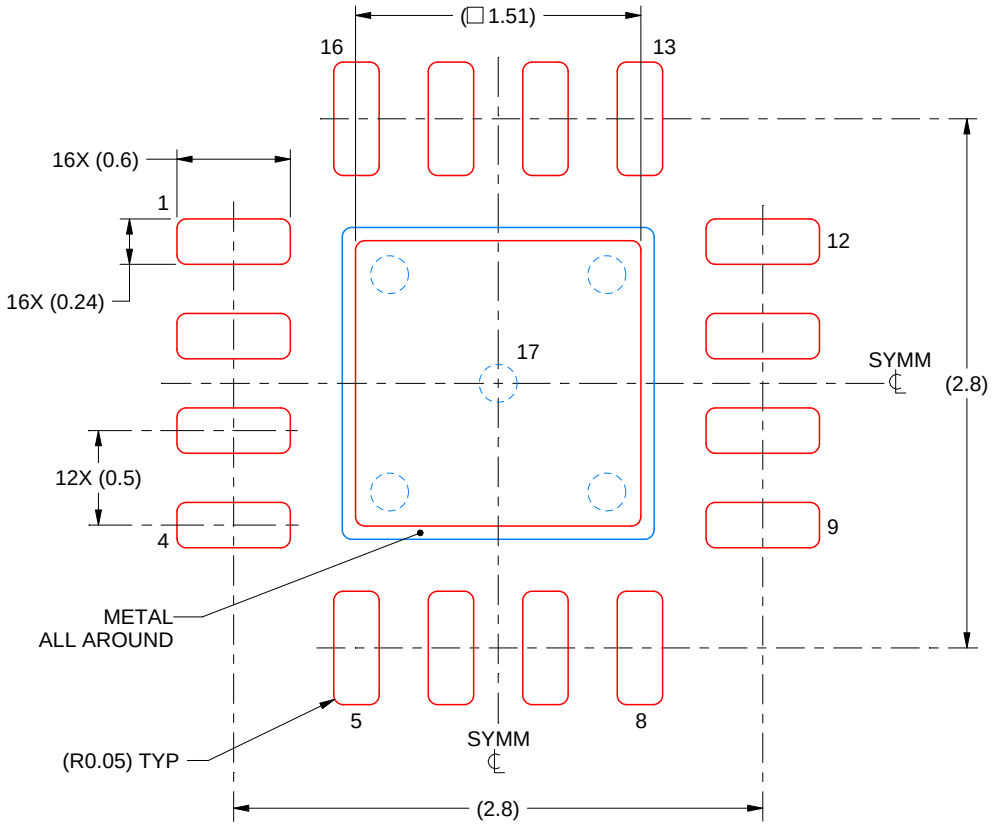
NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
84% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

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NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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