TEXAS INSTRUMENTS
TPS563211
JAJSJX7A – SEPTEMBER 2020 – REVISED AUGUST 2021

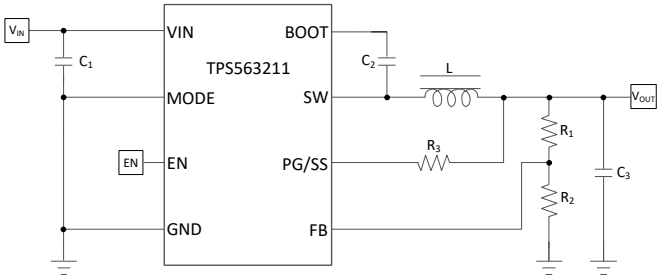
TPS563211 4.2V~18V 入力、3A 同期整流降圧コンバータ、SOT583 パッケージ

1 特長

- 入力電圧:4.2V～18V
- 出力電圧:0.6V～7V
  - 最大 3A の連続出力電流
  - 最小スイッチング・オン時間:45ns
  - 最大デューティ・サイクル:98%
- 高効率
  - 66mΩ および 33mΩ の MOSFET を内蔵
  - 静止電流:120μA (標準値)
- きわめてフレキシブルで優れた使いやすさ
  - Eco-mode または FCCM での動作を選択可能
  - パワー・グッド・インジケータまたは外部ソフト・スタートを選択可能
  - 高精度のイネーブル入力
- 高精度
  - 基準電圧精度:±1% (25°C)
  - スイッチング周波数許容値:±8.5%
- 小型ソリューション・サイズ
  - 設計を容易にする内部補償
  - SOT583 パッケージ
  - 外付け部品が最小限
- ハイサイドとローサイド両方の MOSFET でサイクル単位の電流制限
- ラッチなしの OVP、UVP、UVLO、TSD の保護
- WEBENCH® Power Designer により、TPS563211 を使用するカスタム設計を作成

2 アプリケーション

- セットトップ・ボックス (STB)、デジタル TV
- スマート・スピーカ
- 有線ネットワーク、ブロードバンド
- 監視機器



概略回路図

3 概要

TPS563211 は 、コスト効率が優れた柔軟性の高い同期整流降圧コンバータで、Eco-mode 動作または FCCM (強制連続導通モード) 動作を選択できます。選択可能なパワー・グッド・インジケータまたは外部ソフト・スタートも MODE ピンにより設定できます。イネーブル、パワー・グッド・インジケータ、または外部ソフト・スタートを適切に構成することにより、電源シーケンスが可能になります。入力電圧範囲が 4.2V~18V と広く、12V や 15V など広い範囲にわたる一般的な入力レールに対応できます。 0.6V~7V の出力電圧範囲で、最大 3A の連続出力電流をサポートしています。

高度なエミュレート電流モード (AECM) 制御トポロジを使用することで、高速過渡応答と真の固定スイッチング周波数を実現します。スマート・ループ帯域幅制御を内蔵しているため、外付け補償は不要で、広い出力電圧範囲にわたって高速な過渡応答が得られます。

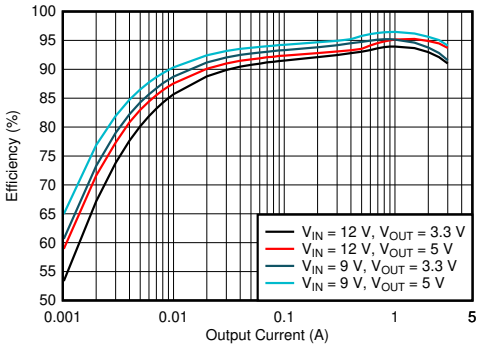
ハイサイド・ピーク電流にサイクル単位の電流制限を適用することで過負荷状態からデバイスを保護し、ローサイドのバレー電流制限により電流暴走を防止します。過電圧保護 (OVP)、低電圧保護 (UVP)、UVLO 保護、サーマル・シャットダウンの下で、ヒカップ・モードがトリガされます。

このデバイスは、1.6mm × 2.1mm の SOT583 パッケージで供給されます。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
TPS563211	SOT583 (8)	1.2mm × 2.1mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



効率と出力電流との関係

英語版の TI 製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.com で閲覧でき、その内容が常に優先されます。TI では翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (September 2020) to Revision A (August 2021)	Page
• ドキュメントのステータスを事前情報から量産データに変更	1

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5 Pin Configuration and Functions

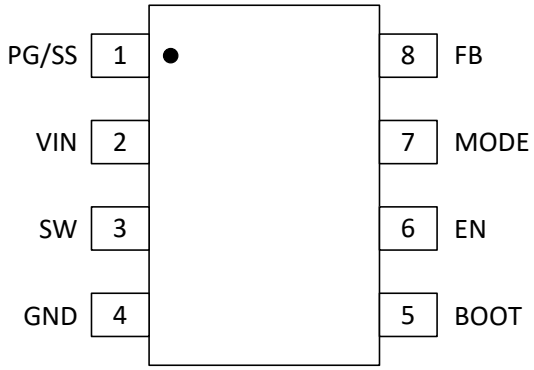

図 5-1. 8-Pin SOT583 DRL Package (Top View)

表 5-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NAME	NO.		
PG/SS	1	I/O	This pin can be selected as Power-Good function or Soft-Start function, depending on device MODE pin configuration. • If the Power-Good function is selected, this is an open-drain power-good indicator. • If the Soft-Start function is selected, an external capacitor connected from this pin to GND defines the rise time for the internal reference voltage.
VIN	2	P	Input voltage supply pin for the control circuitry. Connect the input decoupling capacitors between VIN and GND.
SW	3	P	Switch node terminal. Connect the output inductor to this pin.
GND	4	G	GND terminal for the controller circuit and the internal circuitry
BOOT	5	P	Supply input for the high-side MOSFET gate drive circuit. Connect a 0.1-µF capacitor between BOOT and SW pins.
EN	6	I/O	Enable input control. Driving EN high or leaving this pin floating enables the converter. An external resistor divider can be used to imply an adjustable VIN UVLO function.
MODE	7	I/O	Device operation mode in light load (Eco-mode operation or FCCM operation) and pin 1 function (Power-Good pin or Soft-Start pin) selection pin. Connect a resistor from MODE to GND to configure the device according to 表 7-1.
FB	8	I	Converter feedback input. Connect to output voltage with feedback resistor divider.

(1) I = Input, O = Output, I/O = Input or Output, G = Ground, P = Power

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6 Specifications

6.1 Absolute Maximum Ratings

Over the recommended operating junction temperature range of –40°C to +125°C (unless otherwise noted)(1)

		MIN	MAX	UNIT
Pin voltage(2)	VIN	–0.3	20	V
	SW, DC	–0.3	20	
	SW, transient < 10 ns	–3	22	
	VIN – SW, DC	–0.3	20	
	VIN – SW, transient < 10 ns	–3	22	
	BOOT	–0.3	25	
	BOOT – SW	–0.3	6	
	EN, FB, PG/SS, MODE	–0.3	6	
T_J	Operating junction temperature(3)	–40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under Recommended Operating Conditions. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to the network ground terminal.
(3) Operating at junction temperatures greater than 125°C, although possible, degrades the lifetime of the device.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

Over the recommended operating junction temperature range of –40°C to +125°C (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{IN}	Input supply voltage range		4.2	18	V
V_{OUT}	Output voltage range		0.6	7	
Pin voltage		SW, DC	–0.1	18	
		SW, transient < 10 ns	–3	20	
		VIN - SW, DC	–0.1	18	
		VIN - SW, transient < 10 ns	–3	20	
		BOOT	–0.1	23.5	
		BOOT - SW	–0.1	5.5	
		EN, FB, PG/SS, MODE	–0.1	5.5	
I_{OUT}	Output current range		0	3	A
T_J	Operating junction temperature		–40	125	°C

(1) Recommended Operating Conditions indicate conditions for which the device is intended to be functional, but do not guarantee specific performance limits. For ensured specifications, see the Electrical Characteristics.

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6.4 Thermal Information

THERMAL METRIC(1)		TPS563211 DRL (SOT583) 8 PINS	UNIT
$R_{\theta JA}$ (2)	Junction-to-ambient thermal resistance	116.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	41.7	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	20.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	20.8	°C/W
$R_{\theta JA(EVM)}$ (3)	Junction-to-ambient thermal resistance on TPS563211EVM	70	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report, SPRA953
(2) The value of $R_{\theta JA}$ given in this table is only valid for comparison with other packages and can not be used for design purposes. These values were simulated on a standard JEDEC board. They do not represent the performance obtained in an actual application.
(3) The real $R_{\theta JA}$ on the TPS563211EVM is about 70 ℃/W, test condition: V_{IN} = 12 V, V_{OUT} = 5 V, I_{OUT} = 3 A, T_A = 25 ℃.

6.5 Electrical Characteristics

Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 4.2 V to 18 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY						
V_{IN}	Operation input voltage		4.2		18	V
$I_{Q(VIN)}$	VIN quiescent current at power save mode	Nonswitching, V_{EN} = 1.2 V, V_{FB} = 0.65 V, I_{OUT} = 0 mA		120		µA
	VIN quiescent current at FCCM	Nonswitching, V_{EN} = 1.2 V, V_{FB} = 0.65 V, I_{OUT} = 0 mA		450		µA
$I_{SD(VIN)}$	VIN shutdown supply current	V_{IN} = 12 V, V_{EN} = 0 V		3	10	µA
UVLO						
$V_{UVLO(R)}$	VIN UVLO rising threshold	V_{IN} rising	3.8	4	4.2	V
$V_{UVLO(F)}$	VIN UVLO falling threshold	V_{IN} falling	3.4	3.6	3.8	V
ENABLE						
$V_{EN(R)}$	EN voltage rising threshold	EN rising, enable switching	1.05	1.15	1.25	V
$V_{EN(F)}$	EN voltage falling threshold	EN falling, disable switching	0.91	1.01	1.10	V
$I_{EN(P1)}$	EN pin sourcing current pre EN rising threshold	V_{EN} = 1.0 V	0.93	1.2	1.5	µA
$I_{EN(H)}$	EN pin sourcing current hysteresis		2.4	3.1	3.81	µA
REFERENCE VOLTAGE						
V_{FB}	FB voltage	T_J = 25°C	0.594	0.6	0.606	V
		T_J = –40°C to 125°C, V_{IN} = 12 V	0.591	0.6	0.609	V
$I_{FB(LKG)}$	FB input leakage current	V_{FB} = 0.65 V, T_J = 25°C	–0.1	0	0.1	µA
STARTUP						
I_{SS}	Soft-start charge current	V_{SS} = 0 V	4.5	6.6	8.3	µA
t_{SS}	Internal fixed soft-start time	From 1st switching pulse until target V_{OUT}	1.5	2	2.6	ms
SWITCHING FREQUENCY						
$f_{SW(FCCM)}$	Switching frequency, FCCM operation		550	600	650	kHz
POWER STAGE						

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Limits apply over the recommended operating junction temperature (T_J) range of –40°C to +125°C, unless otherwise stated. Minimum and maximum limits are specified through test, design or statistical correlation. Typical values represent the most likely parametric norm at T_J = 25°C, and are provided for reference purposes only. Unless otherwise stated, the following conditions apply: V_{IN} = 4.2 V to 18 V.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$R_{DSON(HS)}$	High-side MOSFET on-resistance	T_J = 25°C, V_{IN} = 12 V, $V_{BOOT-SW}$ = 5 V		66		mΩ
$R_{DSON(LS)}$	Low-side MOSFET on-resistance	T_J = 25°C, V_{IN} = 12 V		33		mΩ
$t_{ON(min)}$ (1)	Minimum ON pulse width			45		ns
$t_{ON(max)}$	Maximum ON pulse width			6		µs
$t_{OFF(min)}$	Minimum OFF pulse width			105		ns
OVERCURRENT PROTECTION						
$I_{HS(OC)}$	High-side peak current limit	Peak current limit on the HS MOSFET	4.25	5	5.75	A
$I_{LS(OC)}$	Low-side valley current limit	Valley current limit on the LS MOSFET, V_{IN} = 12 V	3.0	4	4.9	A
$I_{LS(NOC)}$	Low-side negative current limit for FCCM	Sinking current limit on the LS MOSFET, V_{IN} = 12 V	1.1	1.5	2.2	A
$t_{HIC(WAIT)}$	Wait time before entering Hiccup			108		µs
$t_{HIC(RE)}$	Hiccup time before re-start			6		Cycles
OUTPUT OVP AND UVP						
V_{UVP}	Undervoltage-protection (UVP) threshold voltage	V_{FB} falling		62.5%		
		UVP hysteresis		5%		
V_{OVP}	Overvoltage-protection (OVP) threshold voltage	V_{FB} rising	107%	112.0%	114%	
		OVP hysteresis		5%		
POWER GOOD						
V_{PGTH}	Power-good threshold	FB falling, PG from high to low	82%	87%	92%	
		FB rising, PG from low to high	87%	92%	97%	
		FB falling, PG from low to high	101%	107%	112%	
		FB rising, PG from high to low	107%	112%	114%	
$V_{PG(OL)}$	PG pin output low-level voltage	I_{PG} = 0.6 mA			0.3	V
$I_{PG(LKG)}$	PG pin leakage current when open drain output is high	V_{PG} = 5.5 V	–1		1	µA
$t_{PG(R)}$	PG delay going from low to high			112		µs
$t_{PG(F)}$	PG delay going from high to low			48		µs
	Minimum VIN for valid output(1)	$V_{PG/SS}$ < 0.5 V at 100 µA		2	2.5	V
THERMAL SHUTDOWN						
$T_{J(SD)}$ (1)	Thermal shutdown threshold			150		°C
$T_{J(HYS)}$ (1)	Thermal shutdown hysteresis			20		°C

(1) Not production tested

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6.6 Typical Characteristics

V_{IN} = 12 V, T_A = 25°C, unless otherwise noted.

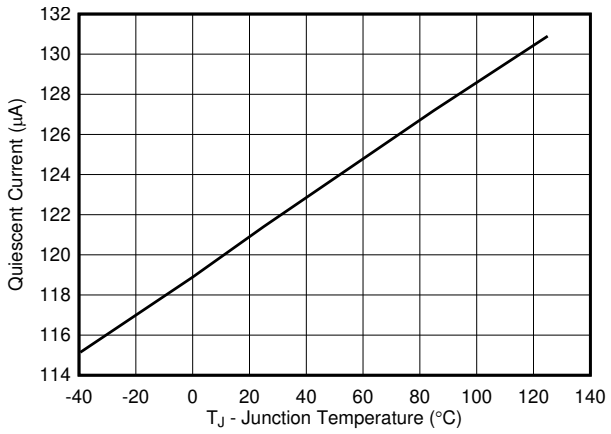

図 6-1. Quiescent Current (Eco Mode) vs Junction Temperature

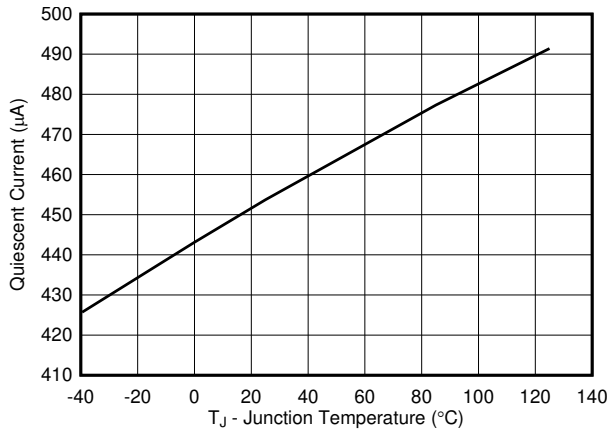

図 6-2. Quiescent Current (FCCM) vs Junction Temperature

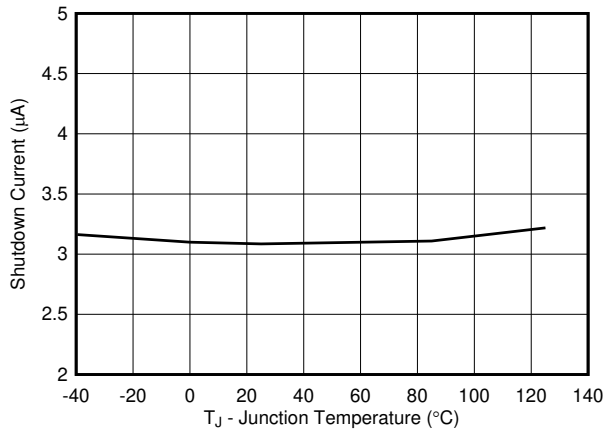

図 6-3. Shutdown Current vs Junction Temperature

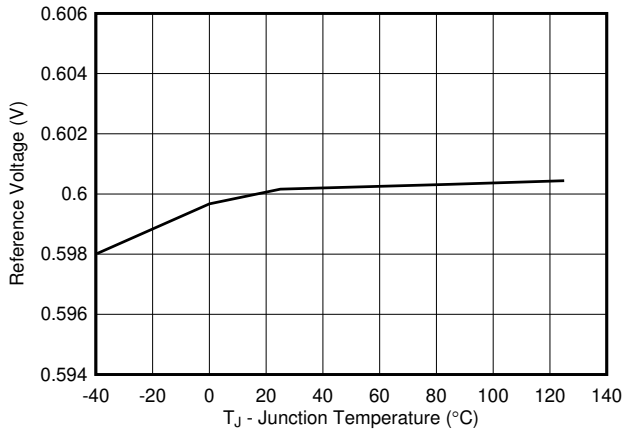

図 6-4. Reference Voltage vs Junction Temperature

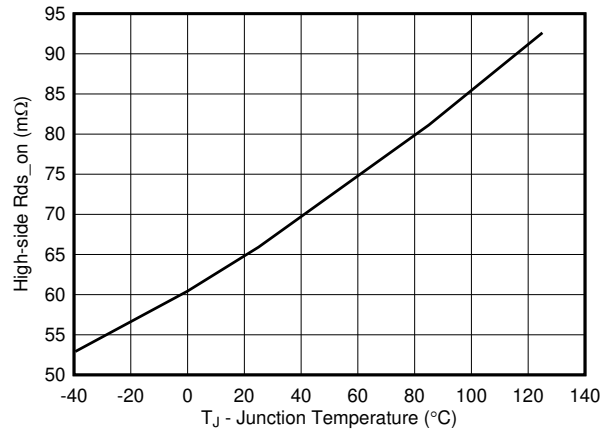

図 6-5. High-Side MOSFET On-Resistance vs Junction Temperature

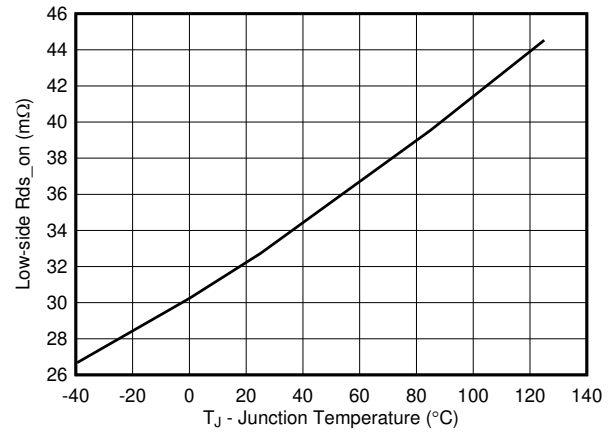

図 6-6. Low-Side MOSFET On-Resistance vs Junction Temperature

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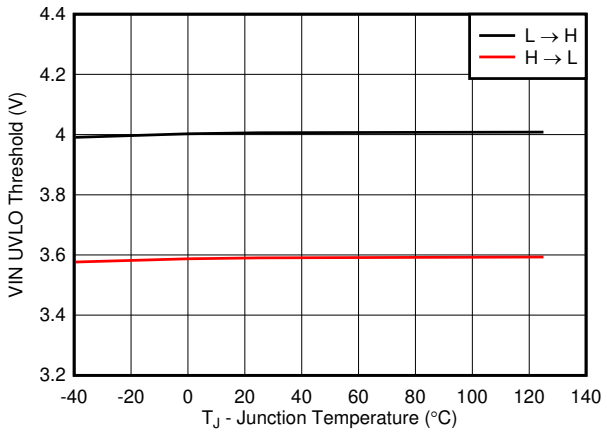

図 6-7. VIN UVLO Threshold vs Junction Temperature

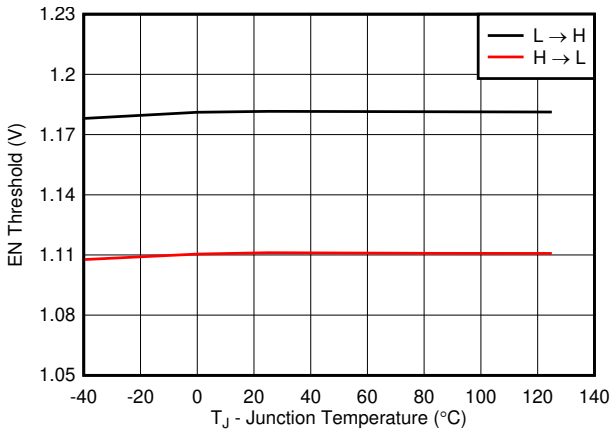

図 6-8. EN Threshold vs Junction Temperature

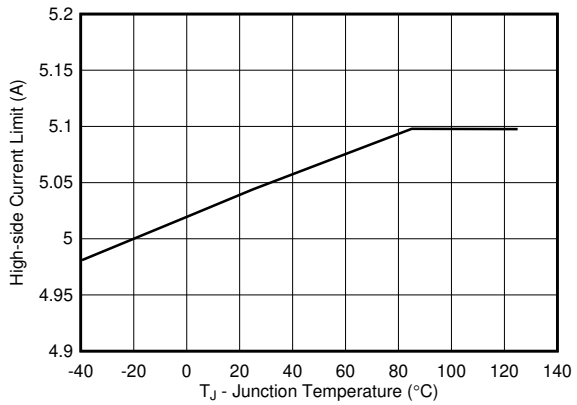

図 6-9. High-Side Current Limit Threshold vs Junction Temperature

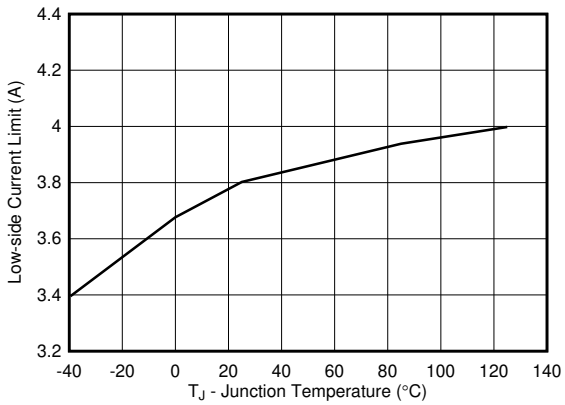

図 6-10. Low-Side Current Limit Threshold vs Junction Temperature

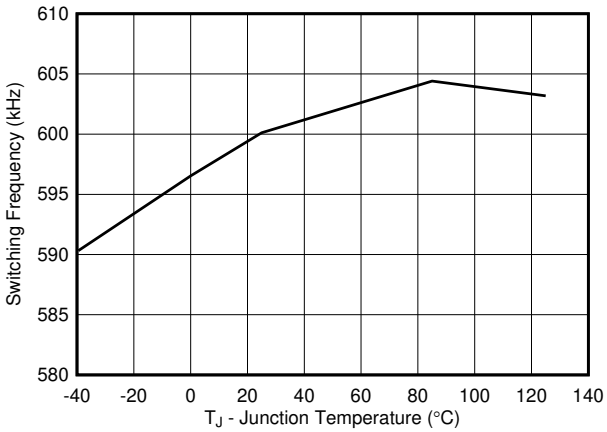

図 6-11. Switching Frequency vs Junction Temperature

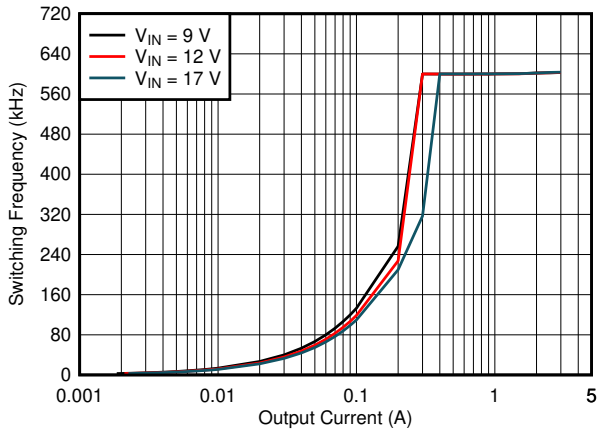

図 6-12. Switching Frequency vs Output Current, V_{OUT} = 3.3 V, L = 3.3 µH

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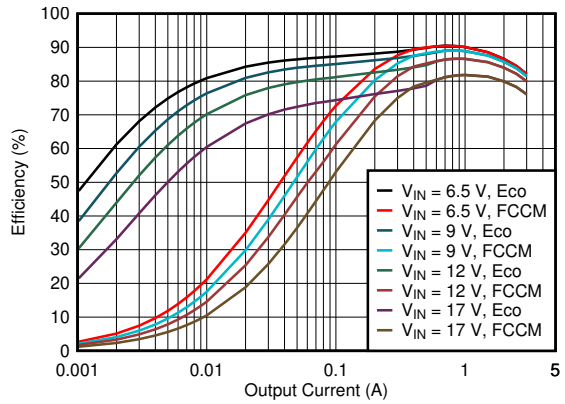

図 6-13. V_{OUT} = 1.05-V Efficiency, L = 1.5 µH

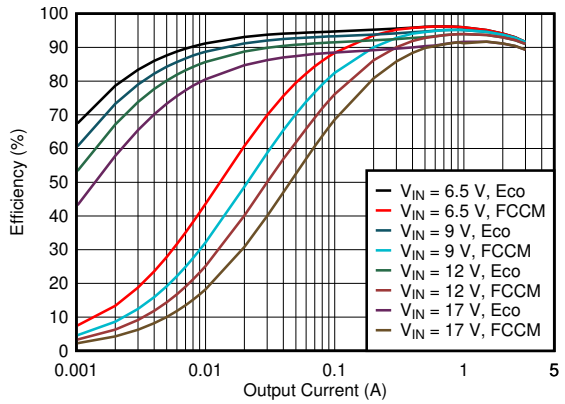

図 6-14. V_{OUT} = 3.3-V Efficiency, L = 3.3 µH

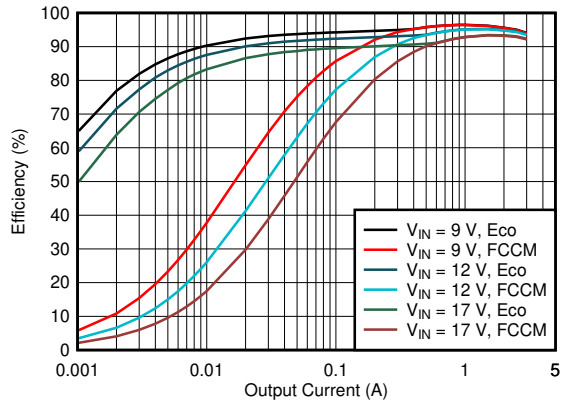

図 6-15. V_{OUT} = 5-V Efficiency, L = 4.7 µH

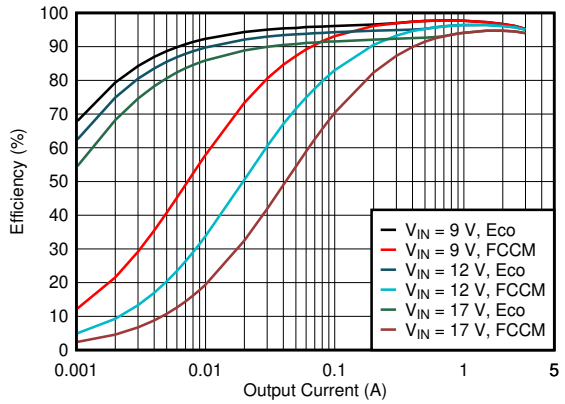

図 6-16. V_{OUT} = 7-V Efficiency, L = 4.7 µH

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7 Detailed Description

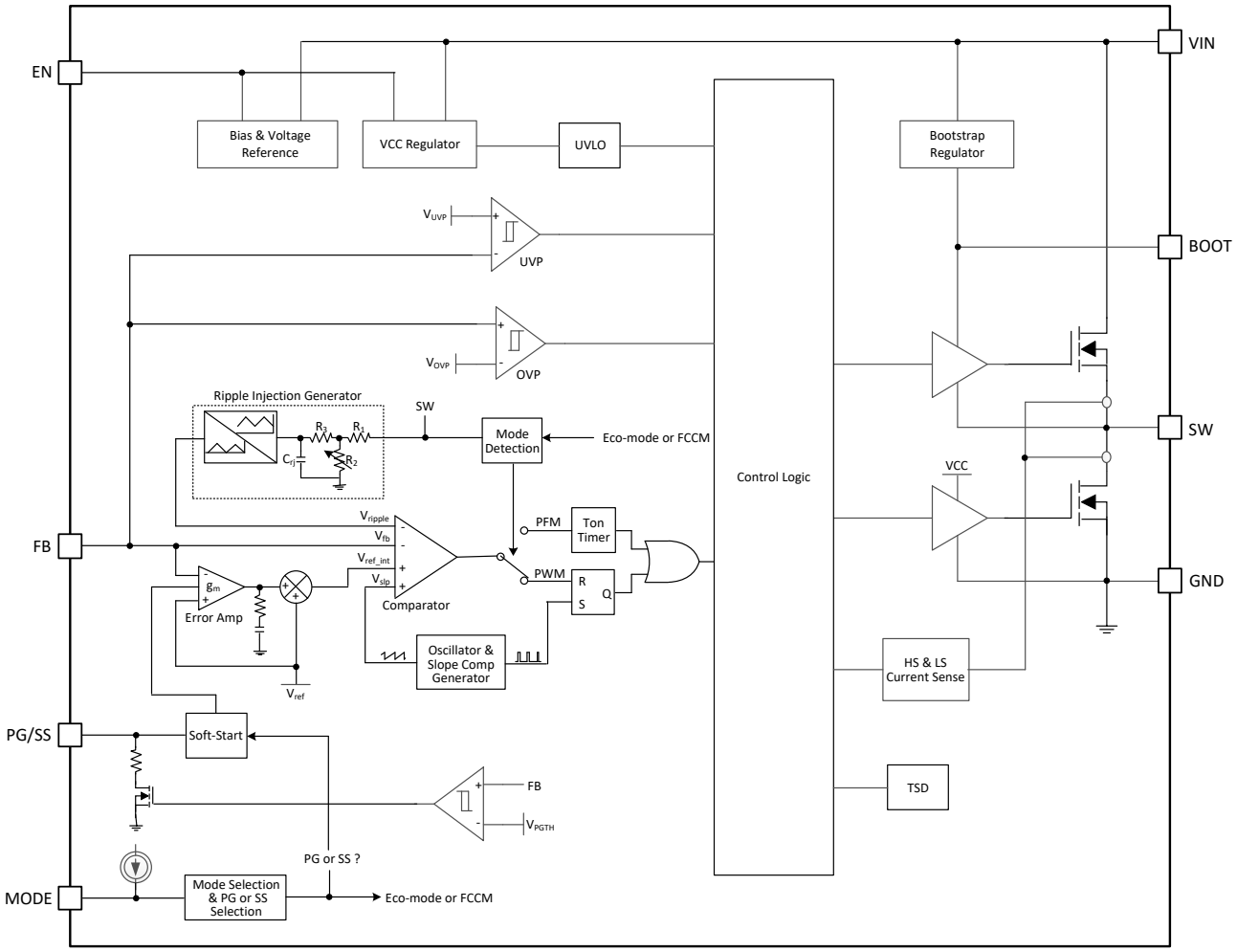
7.1 Overview

The device is a 3-A synchronous buck converter that operates from a 4.2-V to 18-V input voltage and 0.6-V to 7-V output voltage. The device employs AECM control, an emulated current control topology that combines the advantages of peak current mode control and D-CAP2 control, providing fast transient response with true fixed switching frequency.

With the proper MODE configurations, the device supports selectable Eco-mode operation or FCCM operation and a selectable power-good indicator or external soft start.

With an on-time extension function, the device supports a maximum duty cycle of 98%.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Advanced Emulated Current Mode Control

The device employs AECM control, an emulated current control based topology that combines the advantages of peak current mode control and D-CAP2 control, providing fast transient response with true fixed switching frequency. The AECM control topology supports two basic regulation modes, which are PFM regulation mode and PWM regulation mode. During PWM, it operates at its nominal switching frequency in CCM or DCM. The frequency is typically about 600 kHz with a controlled frequency variation. If the load current decreases, it enters PFM to sustain high efficiency down to very light loads. In PFM, the switching frequency decreases with the load

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current. With the internal adaptive loop adjustment, the device eliminates the need for external compensation to provide a fast transient response over a wide output voltage range.

7.3.2 Mode Selection and PG/SS Pin Function Configuration

The device requires a mode resistor to select the operations mode under light load and configure the function of pin 1. 表 7-1 shows the MODE pin settings.

表 7-1. MODE Pin Settings

MODE RESISTOR RANGE	RECOMMENDED MODE RESISTOR VALUE	OPERATION MODE IN LIGHT LOAD	FUNCTION OF PG/SS PIN
[0, 12] kΩ	0	Eco-mode	Power Good
[30, 50] kΩ	47 kΩ	Eco-mode	Soft Start
[83, 120] kΩ	100 kΩ	FCCM	Soft Start
[180, ∞] kΩ	Float	FCCM	Power Good

図 7-1 shows the typical start-up sequence of the device once the enable signal triggers the EN turn-on threshold. After the voltage of VIN crosses the UVLO rising threshold, it takes approximately 110 µs to finish reading and setting of the MODE pin. After this process, the MODE status is latched and does not change until VIN or EN toggles to restart-up this device. Then, the soft-start function begins to ramp up the reference voltage to the PWM comparator.

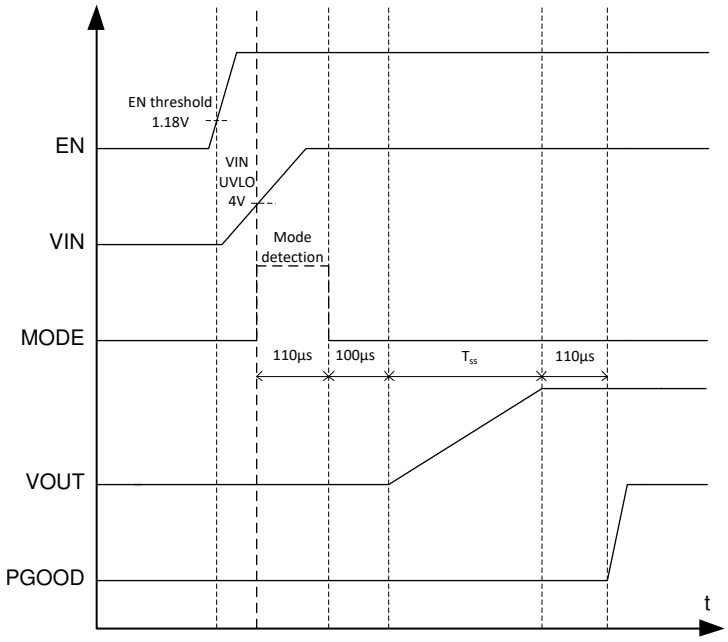

図 7-1. Power-Up Sequence

7.3.3 Power Good (PG)

This is an optional function configured by the MODE pin.

The device has a built-in power good (PG) function to indicate whether the output voltage has reached its appropriate level or not. The PG signal can be used for start-up sequencing of multiple rails. The PG/SS pin works as an open-drain output that requires a pullup resistor (to any voltage below 5.5 V). A pullup resistor of 10 kΩ is recommended to pull it up to a 5-V voltage. It can sink 0.8 mA of current and maintain its specified logic low level. Once the FB pin voltage is between 92% and 112% of the internal reference voltage (VREF) and after a deglitch time of 112 µs, the PG/SS is high impedance. The PG/SS pin is pulled low after a deglitch time of 48 µs when the FB pin voltage is lower than UVP or greater than OVP threshold, or in events of thermal shutdown, EN shutdown, or UVLO conditions. VIN must remain present for the PG/SS pin to stay low.

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If the power-good output is not used when PG function is selected, it is recommended to tie to GND to get better thermal performance.

表 7-2. Power Good Indicator Logic Table

LOGIC SIGNALS				PG LOGIC STATUS
V_{IN}	EN	TSD	V_{OUT}	
V_{IN} > UVLO	High	Not triggered	V_{OUT} on target	High
			V_{OUT} > Target	Low
			V_{OUT} < Target	Low
		Triggered	×	Low
	Low	×	×	Low
2.5 V < V_{IN} < UVLO	×	×	×	Low
V_{IN} < 2.5 V	×	×	×	Undefined

7.3.4 Soft Start and Pre-Biased Soft Start

This is an optional function configured by MODE pin.

If the PG function is selected, the device works with an internal soft-start time of 2 ms. If the SS function is selected, the device has the adjustable soft-start function. When the EN pin becomes high, the soft-start charge current, I_{SS}, begins charging the capacitor, which is connected from the PG/SS pin to GND (C_{SS}). Smooth control of the output voltage is maintained during start-up. Use 式 1 to calculate the soft-start time.

$$t_{ss}(ms) = \frac{3.5 \times C_{ss}(nF) \times V_{REF}(V)}{I_{ss}(uA)} \quad (1)$$

where

- V_{REF} = 0.6 V, I_{SS} = 6.6 µA

The value of the external soft-start capacitor must not be lower than 4 nF typical to make sure the user has good start-up behavior.

If the output capacitor is pre-biased at start-up, the device initiates switching and starts ramping up only after the internal reference voltage becomes greater than the feedback voltage. This scheme makes sure that the converters ramp up smoothly into regulation point.

7.3.5 Output Discharge through PG/SS Pin

If the PG function is selected, the device pulls the PG/SS pin low when the device is shut down by EN, OVP, UVP, UVLO, or thermal shutdown. Connecting PG/SS to VOUT through a resistor can be used to discharge VOUT in those cases (see 図 7-2). The discharge rate can be adjusted by R3, which is also used to pull up the PG/SS pin in normal operation. The minimum supply voltage required for the discharge function to remain active is typically 2.5 V. For reliability, keep the maximum current into the PG/SS pin less than 1.8 mA. Given an output voltage, the minimum resistance of R3 can be calculated in 式 2.

$$R_{3_MIN}(k\Omega) = \frac{V_{OUT}(V)}{1.8} - 0.4 \quad (2)$$

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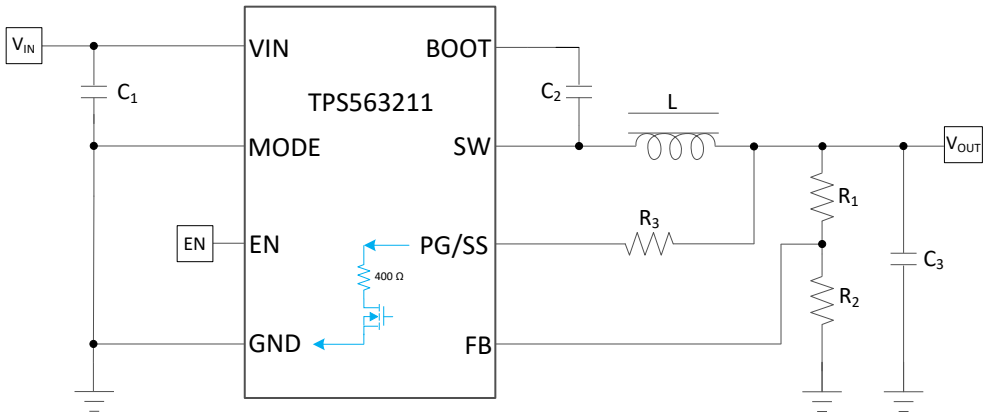

図 7-2. Discharge VOUT through PG/SS Pin with TPS563211

7.3.6 Precise Enable and Adjusting Undervoltage Lockout

The EN pin provides electrical on and off control for the device. When the EN pin voltage exceeds the threshold voltage, the device begins operation. If the EN pin voltage is pulled below the threshold voltage, the regulator stops switching and enters the shutdown mode.

The EN pin has an internal pullup source current, which allows the user to float the EN pin to enable the device. If an application requires control of the EN pin, use external control logic interface to the EN the pin like the open-drain or open-collector output logic.

The device implements internal undervoltage-lockout (UVLO) circuitry on the VIN pin. The device is disabled when the VIN pin voltage falls below the internal VIN UVLO threshold. The internal VIN UVLO threshold has a hysteresis of 400 mV.

If an application requires a higher UVLO threshold on the VIN pin, the EN pin can be configured as shown in 図 7-3. When using the external UVLO function, setting the hysteresis at a value greater than 400 mV is recommended.

The EN pin has a small pullup current, I_p, which sets the default state of the EN pin to enable when no external components are connected. The pullup current is also used to control the voltage hysteresis for the external UVLO function because it increases by I_h when the EN pin crosses the enable threshold. Use 式 3 and 式 4 to calculate the values of R1 and R2 for a specified UVLO threshold. Once R1 and R2 have settled down, the EN voltage can be calculated by 式 5, which must be lower than 5.5 V with the maximum VIN.

$$R_1 = \frac{V_{START} \cdot \frac{V_{EN_FALL}}{V_{EN_RISE}} - V_{STOP}}{I_p\left(1 - \frac{V_{EN_FALL}}{V_{EN_RISE}}\right) + I_h} \tag{3}$$

$$R_2 = \frac{R_1 \cdot V_{EN_FALL}}{V_{STOP} - V_{EN_FALL} + R_1 \cdot \left(I_p + I_h\right)} \tag{4}$$

$$V_{EN} = \frac{R_2 \cdot V_{IN} + R_1 R_2 \left(I_p + I_h\right)}{R_1 + R_2} \tag{5}$$

where

- I_p = 1.2 µA
- I_h = 3.1 µA
- V_{EN_FALL} = 1.15 V
- V_{EN_RISE} = 1.01 V
- V_{START}, the expected input voltage enabling the device
- V_{STOP}, the expected input voltage disabling the device

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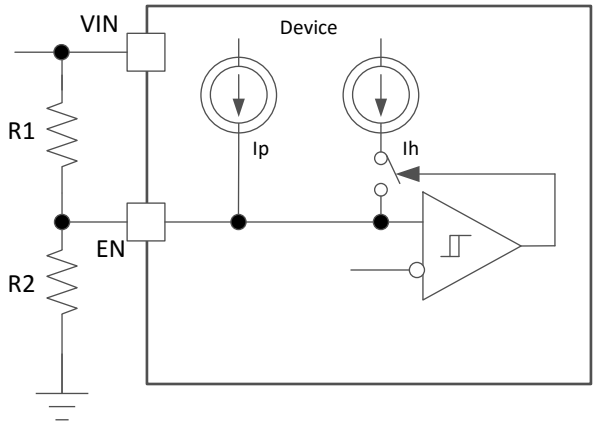

図 7-3. Adjustable VIN Undervoltage Lockout

7.3.7 Overcurrent Limit and Undervoltage Protection

The device is protected from overcurrent conditions by cycle-by-cycle current limiting on both the peak and valley of the inductor current.

During the on time of the high-side MOSFET switch, the inductor current flows through the high-side MOSFET and increases at a linear rate determined by VIN, VOUT, the on time, and the output inductor value. The high-side switch current is sensed when the high-side MOSFET is turned on after a set of blanking time and then compared with the high-side MOSFET current limit threshold in every switching cycle. If the cross-limit event is detected after the minimum on time, the high-side MOSFET is turned off immediately. The high-side MOSFET current is limited by a clamped maximum peak current threshold I_{HS_LIMIT}, which is constant.

The current going through low-side MOSFET is also sensed and monitored. When the low-side MOSFET is turned on, the inductor current begins ramping down. The low-side MOSFET is not turned off at the end of a switching cycle if its current is above the low-side current limit, I_{LS_LIMIT}. The low-side MOSFET is kept on for the next cycle so that inductor current keeps ramping down, until the inductor current ramps below the low-side current limit, I_{LS_LIMIT}, and the subsequent switching cycle comes, the low-side MOSFET is turned off and the high-side MOSFET is turned on after a dead time.

There are some important considerations for this type of overcurrent protection. The load current is higher than the overcurrent threshold by one-half of the peak-to-peak inductor ripple current. Also, when the current is being limited, the output voltage tends to fall as the demanded load current can be higher than the current available from the converter. When the VFB voltage falls below the UVP threshold voltage, the UVP comparator detects it. The device shuts down after the UVP delay time (typically 108 µs) and re-starts after the hiccup time (six times of soft-start time). The hiccup behavior helps reduce the device power dissipation under severe overcurrent conditions.

When the overcurrent condition is removed, the output voltage returns to the regulated value.

7.3.8 Overvoltage Protection

The device detects overvoltage condition by monitoring the feedback voltage. When the feedback voltage becomes higher than 112% of the target voltage, the OVP comparator output goes high and both the high-side MOSFET and low-side MOSFET turns off. This function is a non-latch operation.

7.3.9 Thermal Shutdown

The internal thermal shutdown circuitry forces the device to stop switching if the junction temperature exceeds 150°C typically. The device re-initiates the power-up sequence when the junction temperature drops below 130°C typically.

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7.4 Device Functional Modes

7.4.1 Shutdown Mode

The EN pin provides electrical on and off control for the device. When VEN is below 1.12 V (typical), the device is in Shutdown mode with a shutdown current of 3 µA (typical). The device also employs VIN UVLO protection. If VIN voltage is below their respective UVLO level, the regulator is turned off.

7.4.2 Active Mode

The device is Active mode when VEN is above the precision enable threshold voltage and VIN is above its respective UVLO level. The simplest way to enable the device is to float the EN pin. This allows self-start-up when the input voltage is in the operating range 4.2 V to 18 V.

In Active mode, depending on the load current and the configuration of MODE pin, the device is in one of the following modes:

1. Continuous Conduction Mode (CCM) operation with fixed switching frequency. When load current is above half of the peak-to-peak inductor current ripple. The device works with PWM regulation.
2. Force Continuous Conduction Mode (FCCM) operation with fixed switching frequency. No matter what the load current is, the device works with PWM regulation.
3. Discontinuous Conduction Mode (DCM) operation with fixed switching frequency. When load current is lower than half of the peak-to-peak inductor current ripple in CCM operation, the device works with PWM regulation.
4. Eco-mode operation with switching frequency decreased at very light load, the device works with PFM regulation.

7.4.3 CCM Operation

CCM operation is employed in the device when the load current is higher than half of the peak-to-peak inductor current. In CCM operation, the frequency of operation is fixed, output voltage ripple is at a minimum in this mode, and the maximum continuous output current of 3 A can be supplied by the device.

7.4.4 FCCM Operation

If FCCM operation is selected by MODE pin, the device is set to operate in FCCM operation in light load conditions and allows the inductor current to become negative. In FCCM, the device switches with a fixed frequency over the entire load range, which is suitable for applications requiring tight control of the switching frequency and output voltage ripple.

7.4.5 DCM Operation and Eco-Mode Operation

The light load running includes DCM operation and Eco-mode operation.

As the output current decreases from heavy load condition, the inductor current reduces as well and eventually comes to a point that its rippled valley touches zero level, which is the boundary between CCM and DCM. The low-side MOSFET is turned off when the zero inductor current is detected. As the load current further decreases, the converter runs into DCM.

At even lighter current loads, Eco-mode is activated to maintain high efficiency operation. The on time is kept almost the same as it was in CCM so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. This makes the switching frequency lower, proportional to the load current, and keeps the light load efficiency high. The transition point to the light load operation, $I_{OUT(LL)}$, current can be calculated in 式 6.

$$I_{OUT(LL)} = \frac{0.85^2}{2 \cdot L_1 \cdot f_{sw}} \cdot \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{V_{IN}} \quad (6)$$

7.4.6 On-Time Extension for Large Duty Cycle Operation

Minimum on time, T_{ON_MIN}, is the smallest duration of time that the high-side MOSFET can be on. T_{ON_MIN} is typically 45 ns in the device. Minimum off time, T_{OFF_MIN}, is the smallest duration that the high-side MOSFET can

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be off. T_{OFF_MIN} is typically 105 ns in the device. In CCM operation, T_{ON_MIN} and T_{OFF_MIN} limit the voltage conversion range given a fixed switching frequency.

The minimum duty cycle allowed is:

$$D_{MIN} = T_{ON_MIN} \times f_{SW} \tag{7}$$

The maximum duty cycle allowed is:

$$D_{MAX} = 1 - T_{OFF_MIN} \times f_{SW} \tag{8}$$

In the device, a frequency foldback scheme is employed to extend the maximum duty cycle when T_{OFF_MIN} is reached. The switching frequency decreases once longer duty cycle is needed under low VIN conditions. With the duty increased, the on-time is extended until up to the maximum on-time, 6 µs. Wide range of frequency foldback allows the device output voltage stay in regulation with a much lower supply voltage VIN. This leads to a lower effective dropout voltage.

Given an output voltage, the maximum operation supply voltage can be found by:

$$V_{IN_MAX} = \frac{V_{OUT}}{f_{SW} \cdot T_{ON_MIN}} \tag{9}$$

At lower supply voltage, the switching frequency decreases once T_{OFF_MIN} is triggered. The minimum VIN without frequency foldback can be approximated by:

$$V_{IN_MIN} = \frac{V_{OUT}}{(1\text{-}f_{SW} \cdot T_{OFF_MIN})} \tag{10}$$

Taking considerations of power losses in the system with heavy load operation, V_{IN_MAX} is higher than the result calculated in 式 9. With frequency foldback, V_{IN_VIN} is lowered by decreased f_{SW}, as shown in 図 7-4.

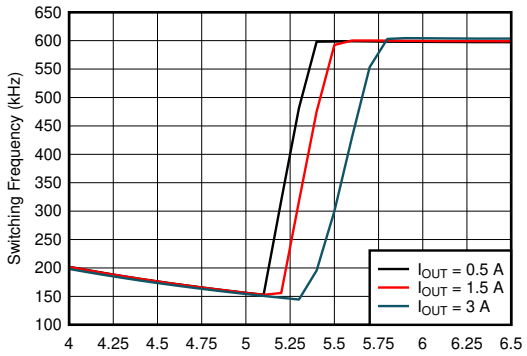

図 7-4. Frequency Foldback at Dropout (V_{OUT} = 5 V)

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8 Application and Implementation

Note

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

8.1 Application Information

The device is a highly integrated, synchronous buck converter. This device is used to convert a higher DC input voltage to a lower DC output voltage, with a maximum output current of 3 A. Alternately, the WEBENCH® software may be used to generate a complete design. The WEBENCH software uses an iterative design procedure and accesses a comprehensive database of components when generating a design. This section presents a simplified discussion of the design process.

8.2 Typical Application

The application schematic of 図 8-1 was developed to meet the requirements of the device. This circuit is available as the TPS563211EVM evaluation module. The design procedure is given in this section.

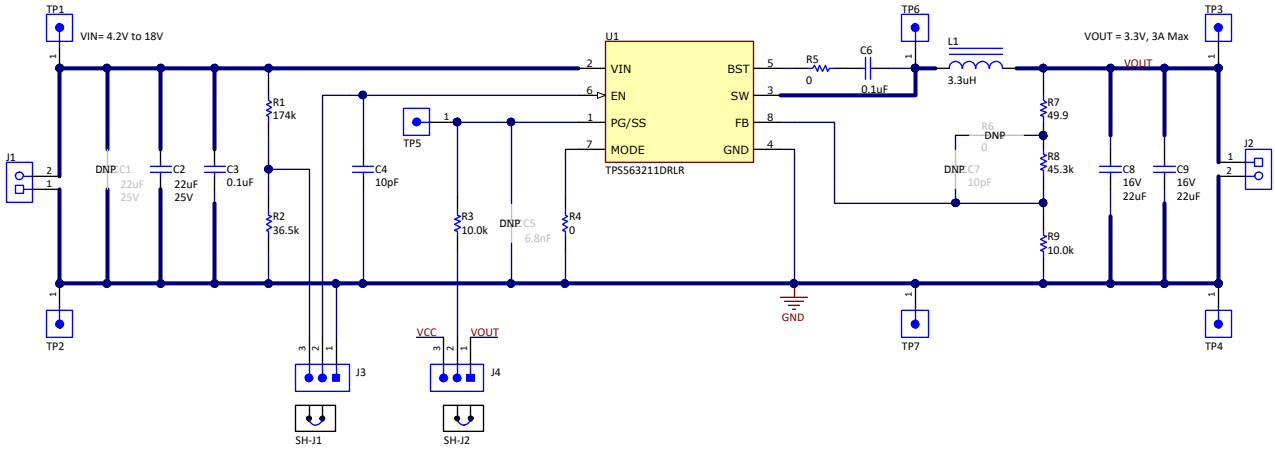

図 8-1. TPS563211 3.3-V, 3-A Reference Design

8.2.1 Design Requirements

表 8-1 shows the design parameters for this application.

表 8-1. Design Parameters

PARAMETER	EXAMPLE VALUE
Input voltage range	4.2 to 18 V
Output voltage	3.3 V
Output current rating	3 A
Transient response, 1.5-A load step	ΔVout / Vout = ±5%
Input ripple voltage	300 mV
Output ripple voltage	30 mV
Operating frequency	600 kHz

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8.2.2 Detailed Design Procedure

8.2.2.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS563211 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost.
3. Open the advanced tab to optimize for output voltage ripple.
4. Once in a TPS563211 design, you can enable the second stage L-C filter and change other settings from the drop-down on the left.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

8.2.2.2 Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the FB pin. TI recommends using 1% tolerance or better divider resistors. Referring to the application schematic of 図 8-1, start with 10 kΩ or 20 kΩ for R9 and use 式 11 to calculate R8. To improve efficiency at light loads, consider using larger value resistors. If the values are too high, the regulator is more susceptible to noise and voltage errors from the FB input current are noticeable.

$$R_8 = \frac{V_{OUT} - V_{REF}}{V_{REF}} \cdot R_9 \tag{11}$$

表 8-2 shows the recommended components value for common output voltages.

8.2.2.3 Output Inductor Selection

To calculate the minimum value of the output inductor, use 式 12. K_{IND} is a coefficient that represents the amount of inductor ripple current relative to the maximum output current. The inductor ripple current is filtered by the output capacitor. Therefore, choosing high inductor ripple currents impact the selection of the output capacitor because the output capacitor must have a ripple current rating equal to or greater than the inductor ripple current. In general, the inductor ripple value is at the discretion of the designer. For this part, TI recommends the range of K_{IND} from 25% to 55%.

$$L_{MIN} = \frac{V_{OUT}}{V_{IN_MAX}} \cdot \frac{V_{IN_MAX} - V_{OUT}}{K_{IND} \cdot I_{OUT} \cdot f_{SW}} \tag{12}$$

where

- I_{OUT} = 3 A

For this design example, use K_{IND} = 50%. The inductor value is calculated to be 2.99 µH. For this design, a nearest standard value was chosen: 3.3 µH. For the output filter inductor, it is important that the RMS current and saturation current ratings not be exceeded. The inductor peak-to-peak ripple current, peak current, and RMS current are calculated using 式 13, 式 14, and 式 15.

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$$I_{RIPPLE} = \frac{V_{OUT}}{V_{IN_MAX}} \cdot \frac{V_{IN_MAX} - V_{OUT}}{L_1 \cdot f_{SW}} \quad (13)$$

$$I_{LPEAK} = I_{OUT} + \frac{I_{RIPPLE}}{2} \quad (14)$$

$$I_{LRMS} = \sqrt{I_{OUT}^2 + \frac{1}{12} I_{RIPPLE}^2} \quad (15)$$

For this design example, the calculated peak current is 3.68 A and the calculated RMS current is 3.02 A. The chosen inductor is a Wurth Elektronik 74437349033 3.3-µH. It has a saturation current rating of 12 A and a RMS current rating of 6 A.

The current flowing through the inductor is the inductor ripple current plus the output current. During power up, faults, or transient load conditions, the inductor current can increase above the calculated peak inductor current level calculated above. In transient conditions, the inductor current can increase up to the switch current limit of the device. For this reason, the most conservative approach is to specify an inductor with a saturation current rating equal to or greater than the switch current limit rather than the peak inductor current.

8.2.2.4 Output Capacitor Selection

After selecting the inductor, the output capacitor needs to be optimized. The LC filter used as the output filter has double pole at:

$$f_P = \frac{1}{2\pi\sqrt{L_1 \cdot C_{OUT_E}}} \quad (16)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the device. The low frequency phase is 180°. At the output filter pole frequency, the gain rolls off at a –40 dB per decade rate and the phase drops rapidly. A high frequency zero introduced by internal circuit that reduces the gain roll off to –20 dB per decade and increases the phase to 90° one decade above the zero frequency. The inductor and capacitor for the output filter must be selected so that the double pole of fp is located below the high frequency zero but close enough. The phase boost provided by the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement, make sure that the $L1 \cdot C_{OUT_E}$ value meets the range of $L1 \cdot C_{OUT_E}$ value recommended in 表 8-2.

表 8-2. Recommended Component Values

OUTPUT VOLTAGE(1) (V)	R8(2) (kΩ)	R9 (kΩ)	L1(3) (µH)	C_{OUT} (4) (µF)	RANGE OF $L1 \cdot C_{OUT_E}$ (5) (µH×µF)
0.76	5.36	20.0	1	3×22	60 to 160
1.05	15.0	20.0	1.5	2×22	60 to 160
1.8	40.0	20.0	2.2	2×22	50 to 200
2.5	31.6	10.0	3.3	2×22	50 to 200
3.3	45.3	10.0	3.3	2×22	50 to 200
5	73.2	10.0	4.7	2×22	50 to 200

(1) Use the recommended L1 and C_{OUT} combination of the higher and closest output rail for the unlisted output rails.
(2) R8 = 10 kΩ and R9 = Float for V_{OUT} = 0.6 V
(3) Inductance values are calculated based on V_{IN}=18 V, but they can also be used for other input voltages. Users can calculate their preferred inductance value per 式 12.
(4) C_{OUT} is the sum of nominal output capacitance. 22-µF, 0805, 10-V or higher specifications capacitors are recommended.

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(5) C_{OUT_E} is the effective value after derating. The value of $L1 \cdot C_{OUT_E}$ must be within in the range.

The capacitor value and ESR determines the amount of output voltage ripple. The device is intended for use with ceramic or other low-ESR capacitors. Use 式 17 to determine the required RMS current rating for the output capacitor.

$$I_{CORMS} = \frac{V_{OUT} \cdot (V_{IN_MAX} - V_{OUT})}{\sqrt{12} \cdot V_{IN_MAX} \cdot L_1 \cdot f_{SW}} \quad (17)$$

Two Murata GRM21BR61C226ME44L 22-µF, 0805, 16-V output capacitors are used for this design. From the data sheet, the estimated DC derating rate is 66.8% at room temperature with AC voltage of 0.2 V. The total output effective capacitance is approximately 29.4 µF. The value of $L1 \cdot C_{OUT_E}$ is 97 µH×µF, which is within the recommended range.

8.2.2.5 Input Capacitor Selection

The device requires an input decoupling capacitor. A bulk capacitor is needed depending on the application. TI recommends a ceramic capacitor over 10 µF for the decoupling capacitor. An additional 0.1-µF capacitor (C3) from VIN pin to ground is recommended to provide additional high frequency filtering. The capacitor voltage rating needs to be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the device. The input ripple current can be calculated using 式 18.

$$I_{CIRMS} = I_{OUT} \cdot \sqrt{\frac{V_{OUT}}{V_{IN_MIN}} \cdot \frac{V_{IN_MIN} - V_{OUT}}{V_{IN_MIN}}} \quad (18)$$

The value of a ceramic capacitor varies significantly over temperature and the amount of DC bias applied to the capacitor. The capacitance variations due to temperature can be minimized by selecting a dielectric material that is stable over temperature. X5R and X7R ceramic dielectrics are usually selected for power regulator capacitors because they have a high capacitance-to-volume ratio and are fairly stable over temperature. The output capacitor must also be selected with the DC bias taken into account. The capacitance value of a capacitor decreases as the DC bias across a capacitor increases. For this example design, a ceramic capacitor with at least a 25-V voltage rating is required to support the maximum input voltage. For this design, one Murata GRM21BR61E226ME44L (10-µF, 25-V, 0805, X5R) capacitor has been selected. The effective capacitance under input voltage of 12 V is 0.18 × 22 = 4 µF. The input capacitance value determines the input ripple voltage of the regulator. The input voltage ripple can be calculated using 式 19. Using the design example values, I_{OUT_MAX} = 3 A, C_{IN_E} = 4 µF, f_{SW} = 600 kHz, yields an input voltage ripple of 313 mV and a RMS input ripple current of 1.23 A.

$$\Delta V_{IN} = \frac{I_{OUT_MAX} \cdot 0.25}{C_{IN} \cdot f_{SW}} + (I_{OUT_MAX} \cdot R_{ESR_MAX}) \quad (19)$$

where

- R_{ESR_MAX} = the maximum series resistance of the input capacitor

8.2.2.6 Bootstrap Capacitor Selection

A 0.1-µF ceramic capacitor must be connected between the BOOT to SW pin for proper operation. TI recommends to use a ceramic capacitor with X5R or better grade dielectric. The capacitor must have a 10-V or higher voltage rating.

8.2.2.7 Undervoltage Lockout Set Point

The undervoltage lockout (UVLO) can be adjusted using the external voltage divider network of R1 and R2. R1 is connected between VIN and the EN pin of the TPS563211 and R2 is connected between EN and GND. The

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UVLO has two thresholds, one for power up when the input voltage is rising and one for power down or brownouts when the input voltage is falling. For the example design, the supply should turn on and start switching when the input voltage increases above 6.6 V (UVLO start or enable). After the regulator starts switching, it must continue to do so until the input voltage falls below 5.7 V (UVLO stop or disable). 式 3 and 式 4 can be used to calculate the values for the upper and lower resistor values. For the stop voltages specified, the nearest standard resistor value for R1 is 174 kΩ and for R2 is 36.5 kΩ.

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8.2.3 Application Curves

V_{IN} = 12 V, L_1= 3.3 µH, C_{OUT} = 44 µF, T_A = 25°C. (unless otherwise noted)

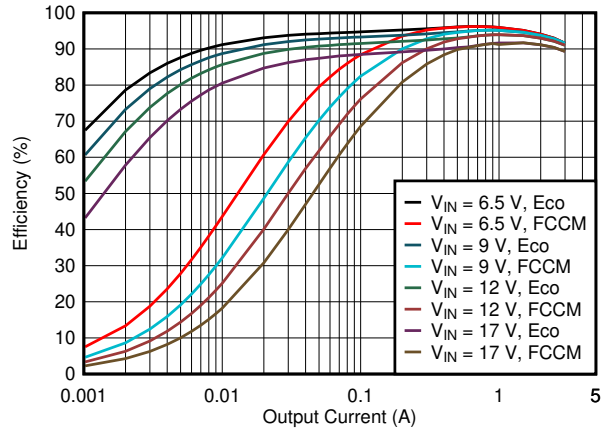

図 8-2. Efficiency

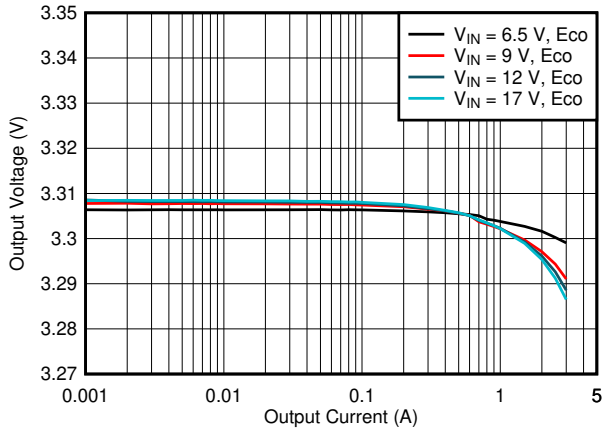

図 8-3. Load Regulation

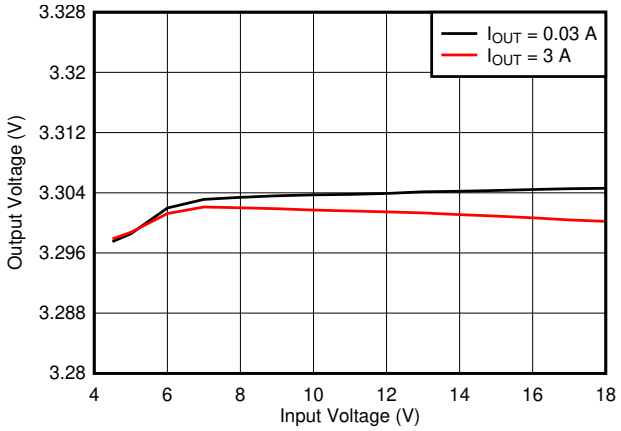

図 8-4. Line Regulation

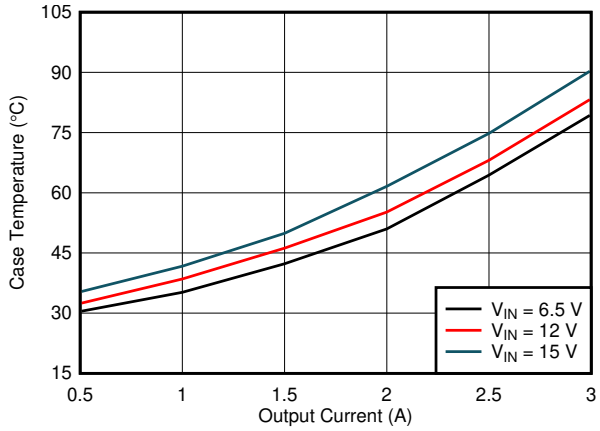

図 8-5. Case Temperature Rise vs Load Current

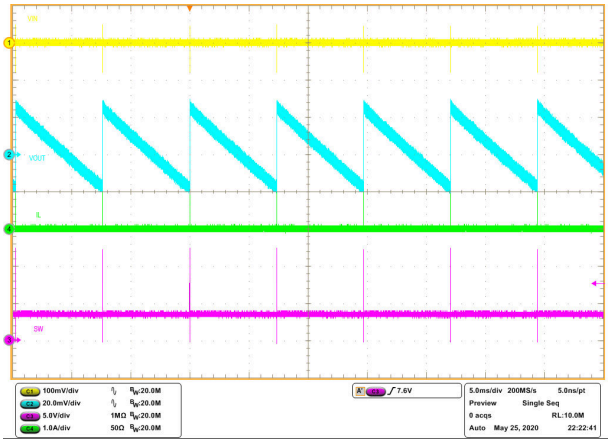

図 8-6. Steady State Waveforms, I_{OUT} = 0 A

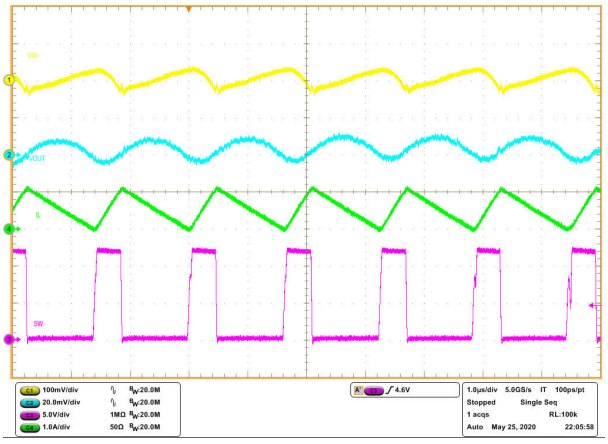

図 8-7. Steady State Waveforms, I_{OUT} = 0.5 A

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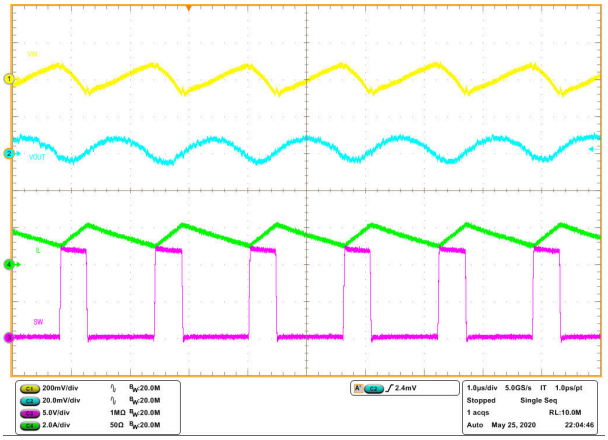

図 8-8. Steady State Waveforms, I_{OUT} = 1.5 A

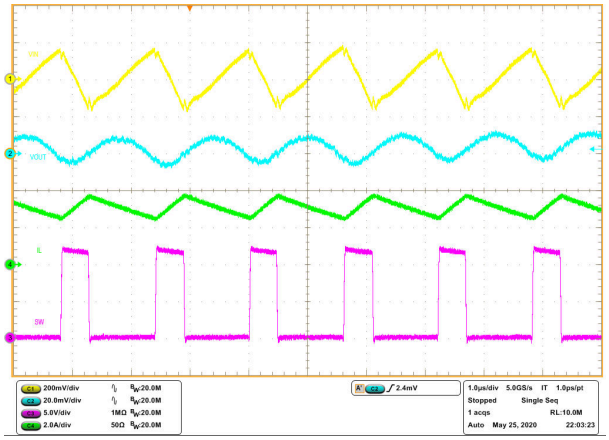

図 8-9. Steady State Waveforms, I_{OUT} = 3 A

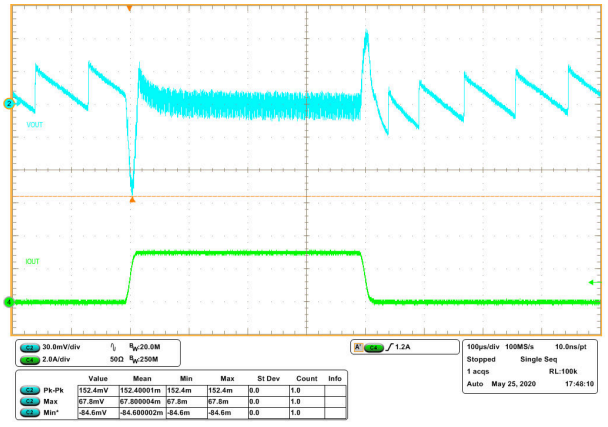

図 8-10. Transient Response 0 to 3 A with Slew Rate of 0.25 A/µs (Eco-Mode)

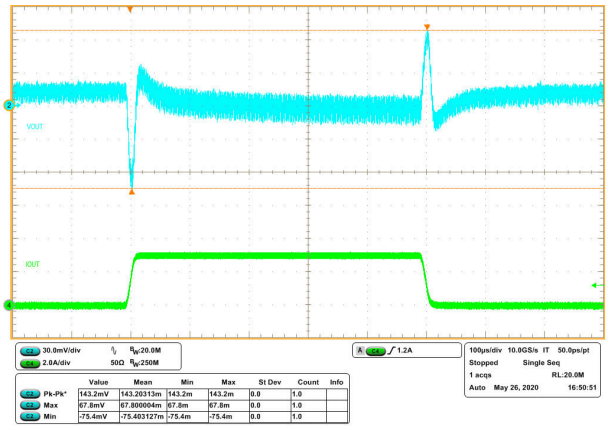

図 8-11. Transient Response 0 to 3 A with Slew Rate of 0.25 A/µs (FCCM)

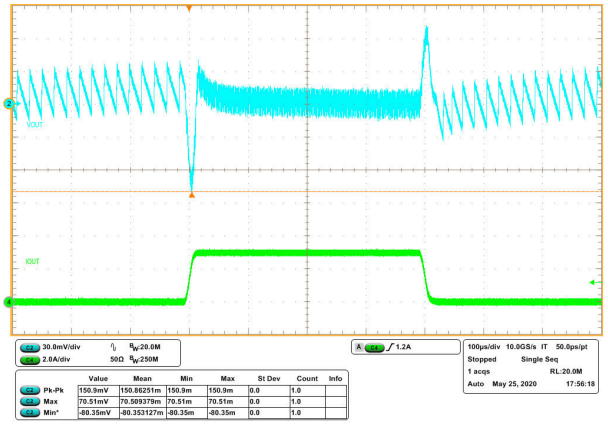

図 8-12. Transient Response 0.03 to 3 A with Slew Rate of 0.25 A/µs (Eco-Mode)

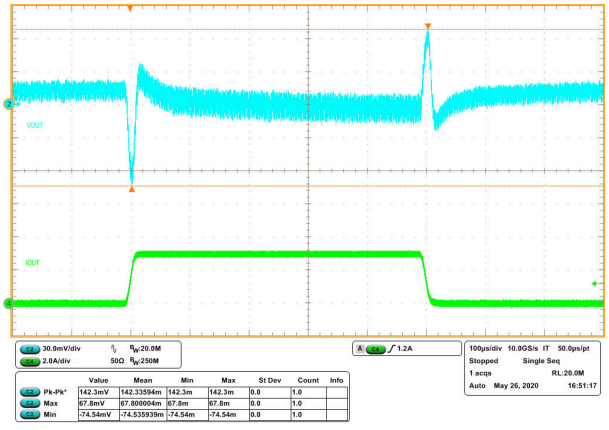

図 8-13. Transient Response 0.03 to 3 A with Slew Rate of 0.25 A/µs (FCCM)

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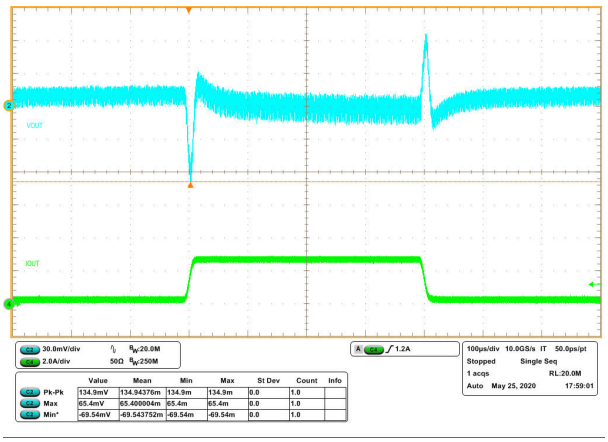

図 8-14. Transient Response 0.3 to 2.7 A with Slew Rate of 0.25 A/µs

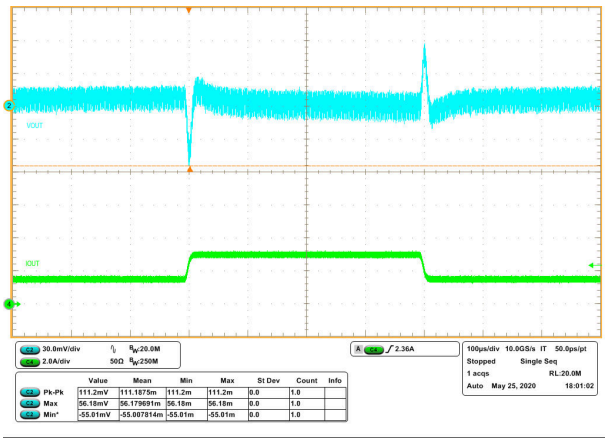

図 8-15. Transient Response 1.5 to 3 A with Slew Rate of 0.25 A/µs

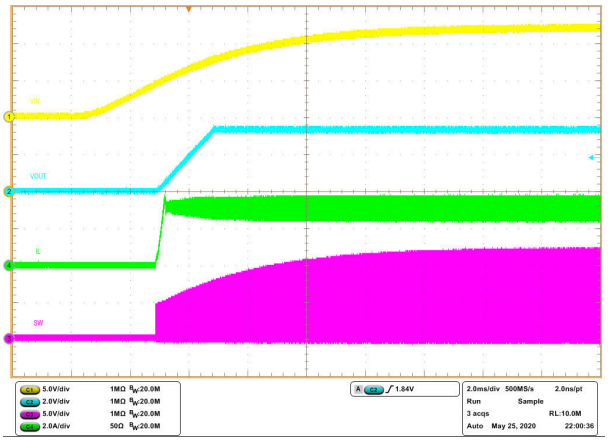

図 8-16. Start-Up Relative to VIN

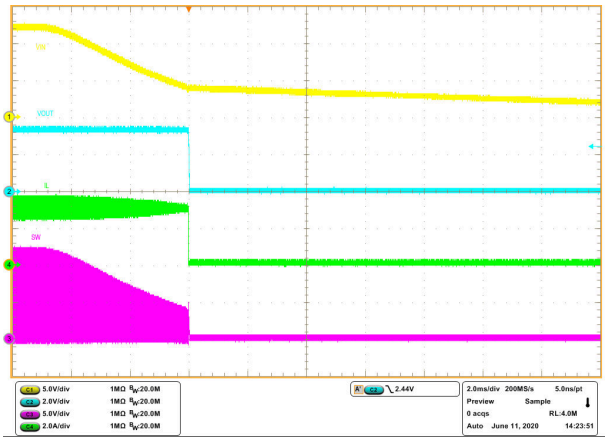

図 8-17. Shutdown Relative to VIN

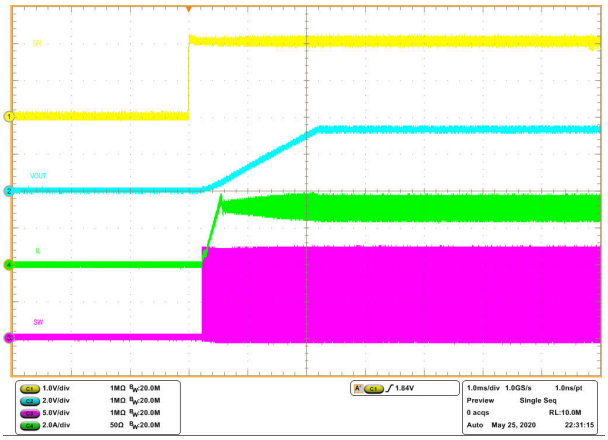

図 8-18. Enable Relative to EN

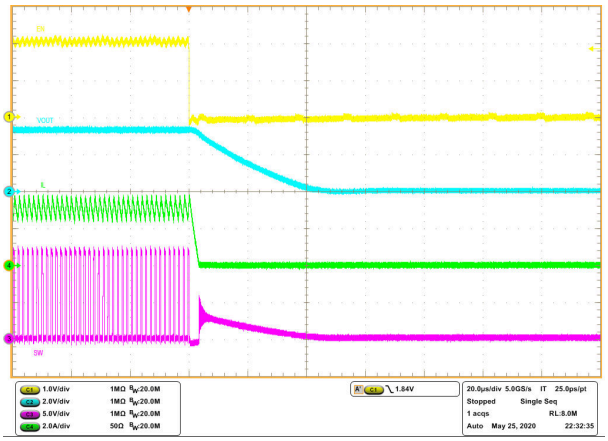

図 8-19. Disable Relative to EN

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図 8-20. Output Short Protection

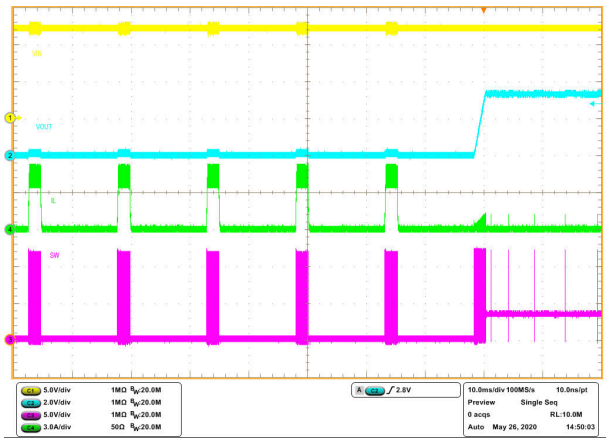

図 8-21. Output Short Recovery

9 Power Supply Recommendations

The devices are designed to operate from an input voltage supply range between 4.2 V and 18 V. This input supply must be well regulated. If the input supply is located more than a few inches from the device or converter, additional bulk capacitance can be required in addition to the ceramic bypass capacitors. An electrolytic capacitor with a value of 47 µF is a typical choice.

10 Layout

10.1 Layout Guidelines

1. VIN and GND traces should be as wide as possible to reduce trace impedance. The wide areas are also of advantage from the view point of heat dissipation.
2. The input capacitor and output capacitor should be placed as close to the device as possible to minimize trace impedance.
3. Provide sufficient vias for the input capacitor and output capacitor.
4. Keep the SW trace as physically short and wide as practical to minimize radiated emissions.
5. Do not allow switching current to flow under the device.
6. A separate VOUT path should be connected to the upper feedback resistor.
7. Make a Kelvin connection to the GND pin for the feedback path.
8. Voltage feedback loop should be placed away from the high-voltage switching trace, and preferably has ground shield.
9. The trace of the FB node should be as small as possible to avoid noise coupling.
10. The GND trace between the output capacitor and the GND pin should be as wide as possible to minimize its trace impedance.

10.2 Layout Example

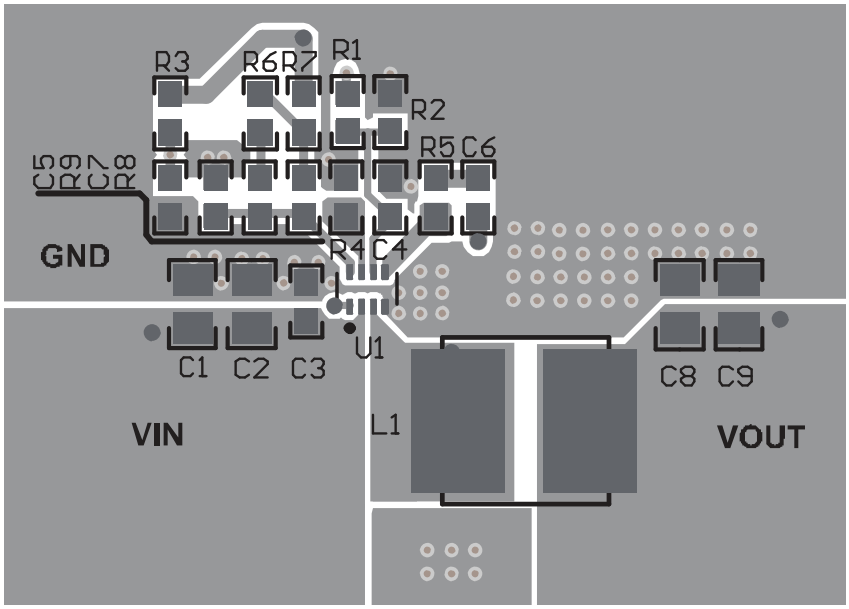

図 10-1. Top Layout Example

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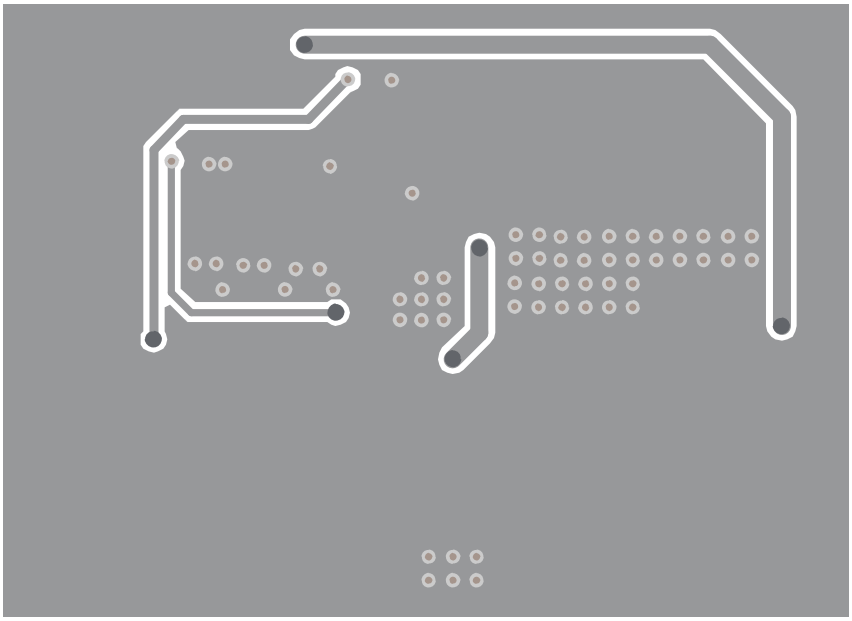

図 10-2. Bottom Layout Example

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11 Device and Documentation Support

11.1 Device Support

11.1.1 Development Support

11.1.1.1 Custom Design With WEBENCH® Tools

Click here to create a custom design using the TPS563211 device with the WEBENCH® Power Designer.

1. Start by entering the input voltage (V_{IN}), output voltage (V_{OUT}), and output current (I_{OUT}) requirements.
2. Optimize the design for key parameters such as efficiency, footprint, and cost.
3. Open the advanced tab to optimize for output voltage ripple.
4. Once in a TPS563211 design, you can enable the second stage L-C filter and change other settings from the drop-down on the left.

The WEBENCH Power Designer provides a customized schematic along with a list of materials with real-time pricing and component availability.

In most cases, these actions are available:

- Run electrical simulations to see important waveforms and circuit performance
- Export customized schematic and layout into popular CAD formats
- Print PDF reports for the design, and share the design with colleagues

Get more information about WEBENCH tools at www.ti.com/WEBENCH.

11.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.3 サポート・リソース

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WEBENCH® is a registered trademark of Texas Instruments.
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11.5 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

11.6 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS563211DRLR	ACTIVE	SOT-5X3	DRL	8	4000	RoHS & Green	Call TI | SN	Level-1-260C-UNLIM	-40 to 125	3211	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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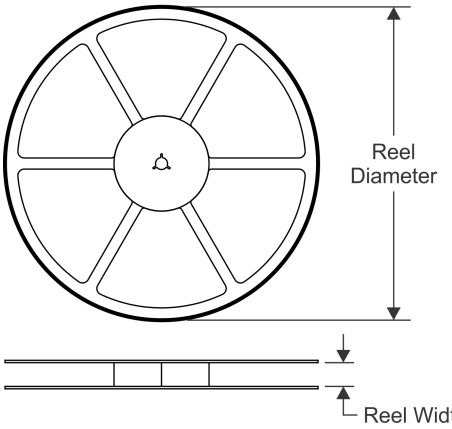
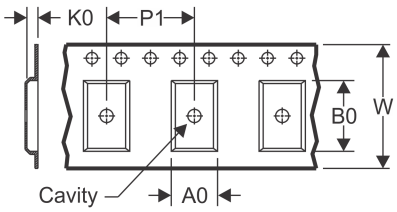
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

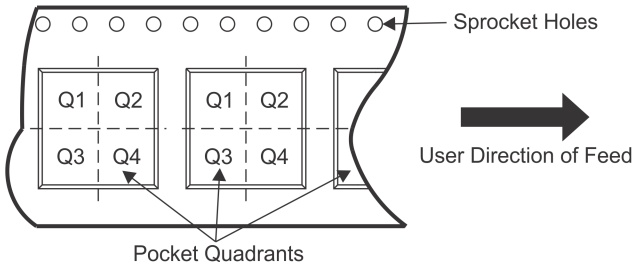


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

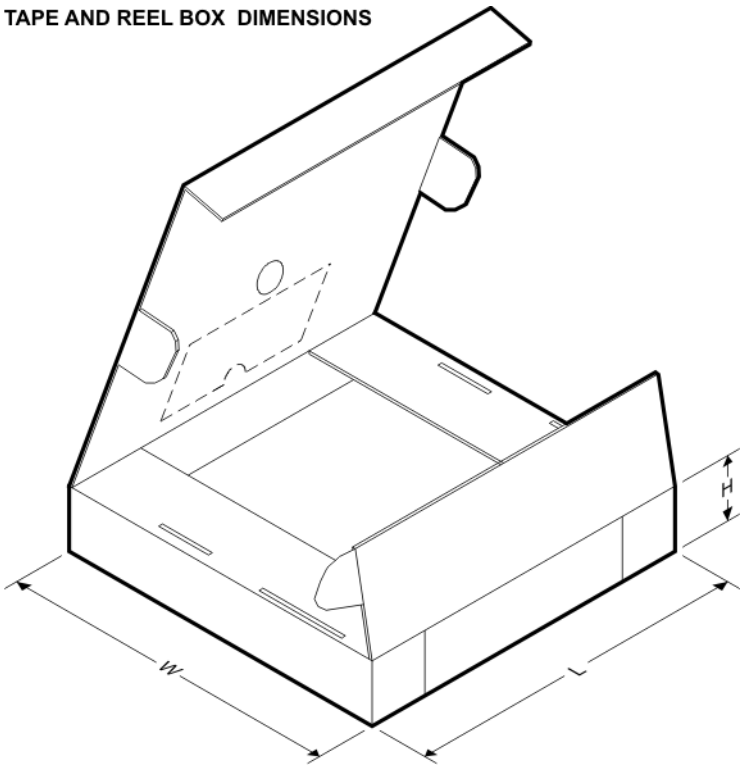
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS563211DRLR	SOT-5X3	DRL	8	4000	180.0	8.4	2.75	1.9	0.8	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

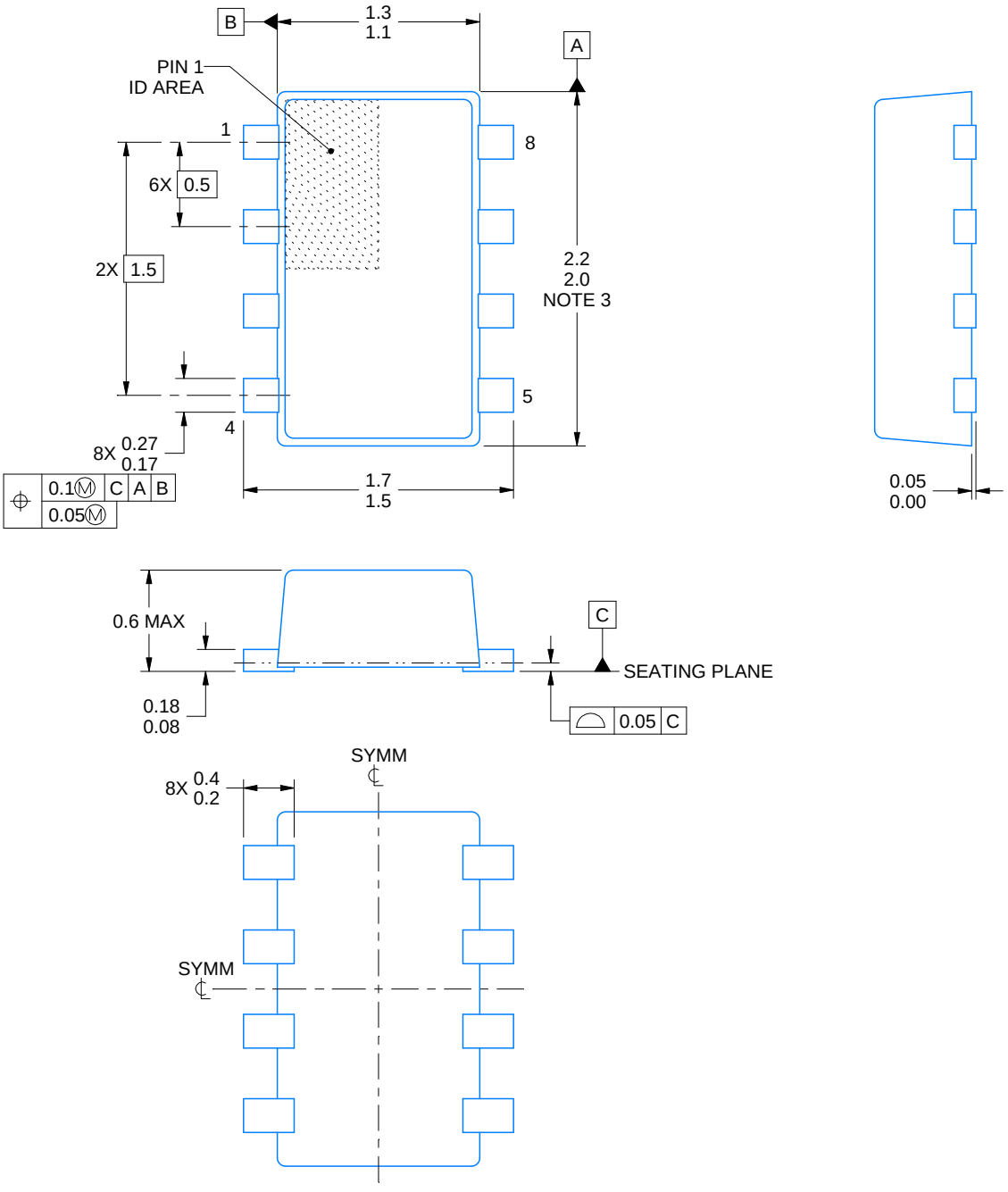
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS563211DRLR	SOT-5X3	DRL	8	4000	210.0	185.0	35.0

PACKAGE OUTLINE

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



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NOTES:

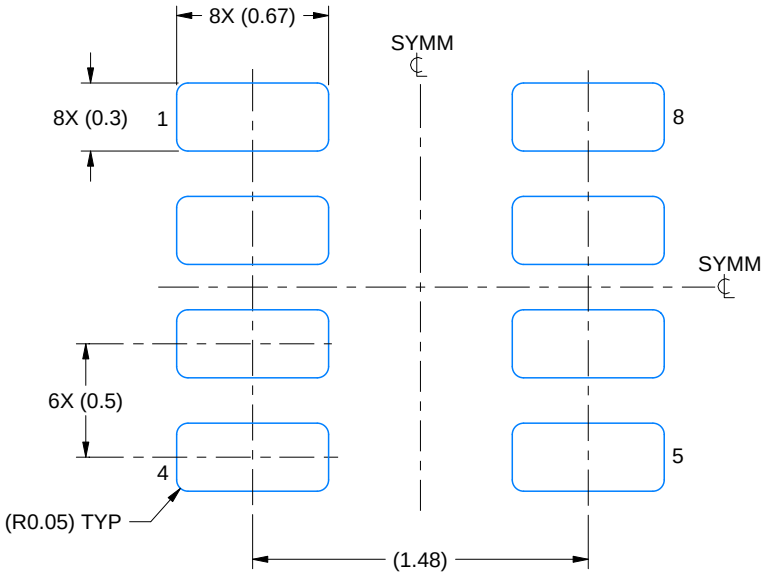
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, interlead flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC Registration MO-293, Variation UDAD

EXAMPLE BOARD LAYOUT

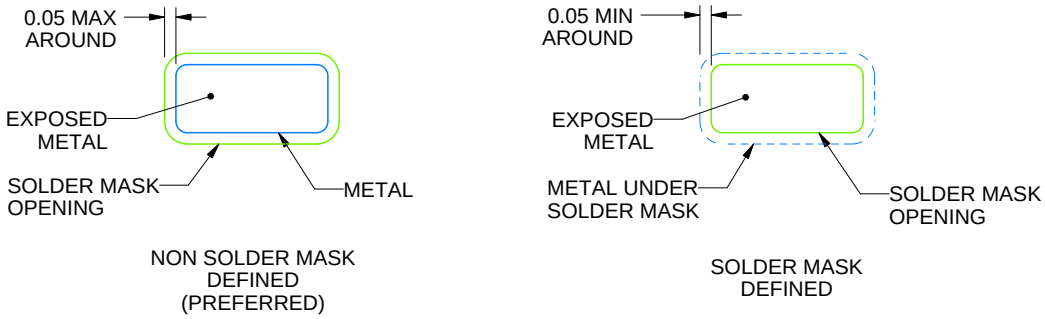
DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:30X



SOLDERMASK DETAILS

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NOTES: (continued)

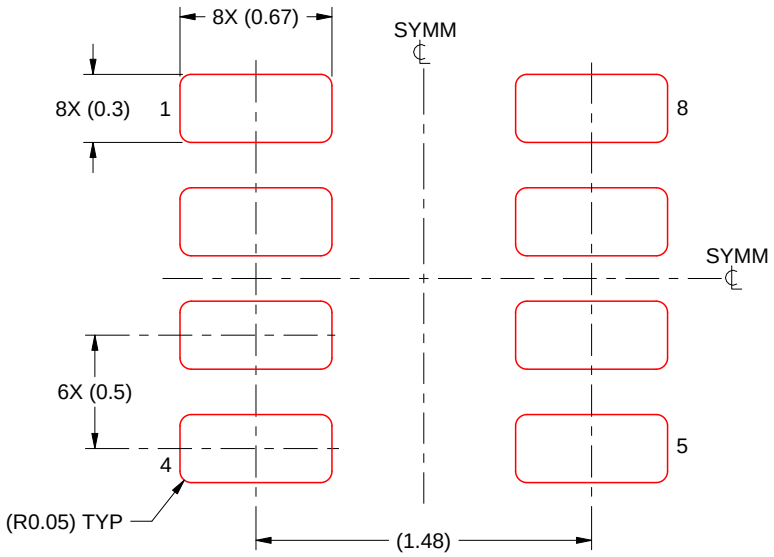
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
7. Land pattern design aligns to IPC-610, Bottom Termination Component (BTC) solder joint inspection criteria.

EXAMPLE STENCIL DESIGN

DRL0008A

SOT-5X3 - 0.6 mm max height

PLASTIC SMALL OUTLINE



SOLDER PASTE EXAMPLE
BASED ON 0.1 mm THICK STENCIL
SCALE:30X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

重要なお知らせと免責事項

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