TPS568215 4.5V～17V 入力、8A 同期整流降圧型 SWIFT™ コンバータ

1 特長

- 19mΩ / 9.4mΩ の MOSFET を内蔵
- F_{SW} として 400kHz、800kHz、1.2MHz を選択可能
- 可変電流制限設定、ヒカップ再起動機能付き
- 温度範囲全体にわたって ±1% 精度の 0.6V 基準電圧
- 外部の 5V バイアスのサポートによる効率向上 (オプション)
- D-CAP3™ 制御モードによる高速過渡応答
- 厳しい出力電圧リップルに対応する強制連続導通モード (FCCM) と、軽負荷時に効率性を上げる自動スキップ Eco-mode™ から選択可能
- 0.6V～5.5V の出力電圧範囲
- すべてのセラミック・コンデンサに対応
- プリバイアスされた出力への単調なスタートアップ
- 可変ソフトスタート、デフォルトのソフトスタート時間は 1ms
- 動作時接合部温度:-40℃～150℃
- 小型の 3.5mm × 3.5mm HotRod™ QFN パッケージ
- 8A の TPS568231 および 12-A TPS56C231 および TPS56C215 とピン互換
- WEBENCH® 設計センターでのサポート

2 アプリケーション

- サーバーおよびストレージ
- セットトップ・ボックス、ハイエンド DTV
- テレコムおよびネットワーキング、ポイント・オブ・ロード (POL)
- IPC、ファクトリ・オートメーション

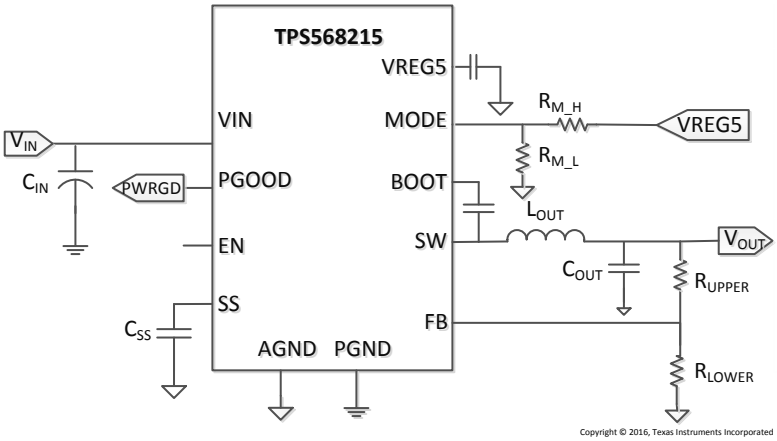
3 概要

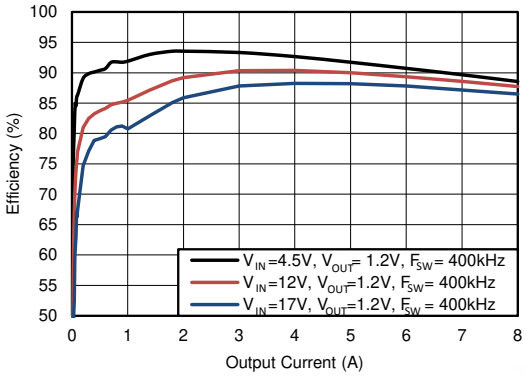
TPS568215 はテキサス・インスツルメンツで最小のモノリシック、8A 同期整流降圧型コンバータで、アダプティブ・オンタイム D-CAP3™ 制御モードが搭載されています。このデバイスは、低 $R_{DS(on)}$ のパワー MOSFET を内蔵して高効率を実現し、外付け部品数が最小になるため、スペースの制約が厳しい電力システムでも使いやすくなっています。主要な機能として、非常に正確な基準電圧、高速負荷過渡応答、自動スキップ・モードの動作による軽負荷時の高効率、可変の電流制限、外部補償が不要なことが挙げられます。強制連続導通モードにより、高性能 DSP や FPGA に求められる厳しい電圧レギュレーション精度要件を満たすことができます。TPS568215 は放熱特性の優れた 18 ピン HotRod QFN パッケージで供給され、–40℃～150℃の接合部温度で動作するよう設計されています。TPS568215 は TPS56C215 とピン互換性があり、同じ占有面積で 6A～12A のソリューションを柔軟に選択できます。

パッケージ情報

部品番号	パッケージ (1)	本体サイズ (公称)
TPS568215	RNN (VQFN、18)	3.5mm × 3.5mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。





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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision B (August 2023) to Revision C (August 2023) — **Page**

- 「特長」一覧にピン互換のデータシートのリンクを追加 ... 1

Changes from Revision A (October 2016) to Revision B (August 2023) — **Page**

- ドキュメント全体にわたって表、図、相互参照の採番方法を更新 ... 1
- 「特長」一覧を、ピン互換デバイスで更新 ... 1

Changes from Revision * (October 2016) to Revision A (October 2016) — **Page**

- 「製品プレビュー」から「量産データ」のリリースに変更 ... 1
- Changed 図 7-1 image ... 14

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5 Pin Configuration and Functions

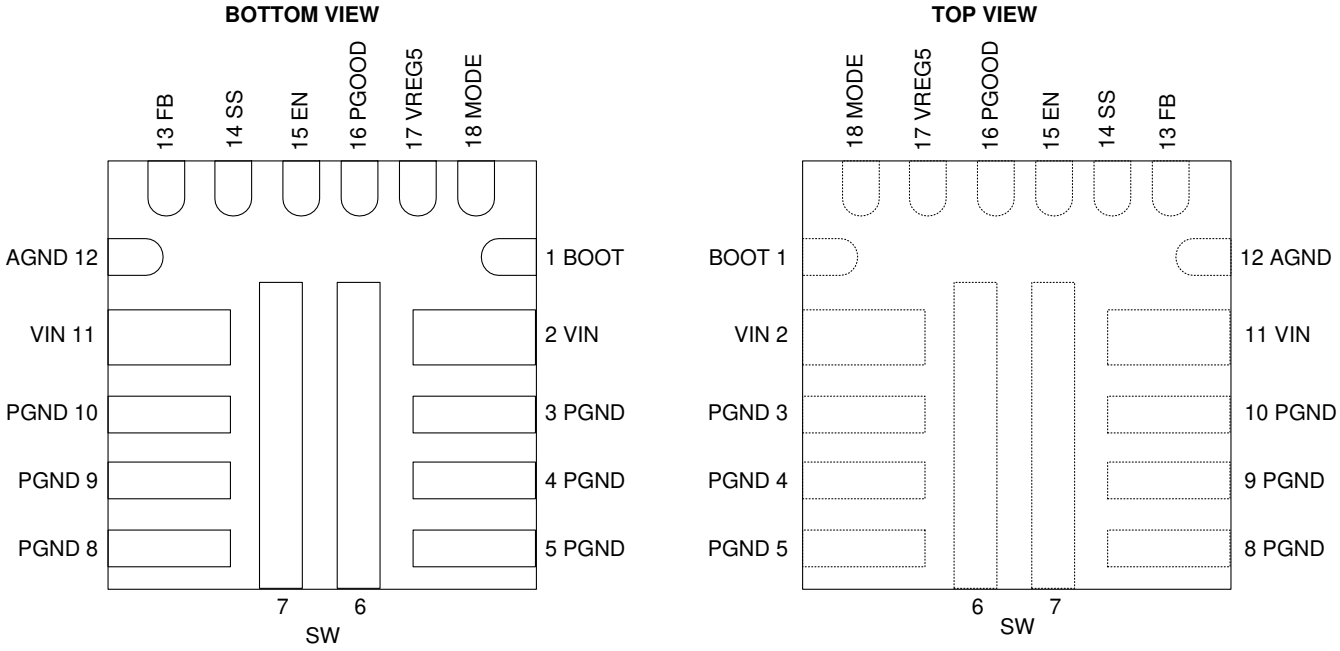


図 5-1. RNN Package 18-Pin VQFN

表 5-1. Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	BOOT	I	Supply input for the gate drive voltage of the high-side MOSFET. Connect a 0.1-µF bootstrap capacitor between BOOT and SW.
2,11	VIN	P	Input voltage supply pin for the control circuitry. Connect the input decoupling capacitors between VIN and PGND.
3, 4, 5, 8, 9, 10	PGND	G	Power GND terminal for the controller circuit and the internal circuitry.
6, 7	SW	O	Switch node terminal. Connect the output inductor to this pin.
12	AGND	G	Ground of internal analog circuitry. Connect AGND to PGND plane.
13	FB	I	Converter feedback input. Connect to the resistor divider between output voltage and AGND.
14	SS	O	Soft-Start time selection pin. Connecting an external capacitor sets the soft-start time and if no external capacitor is connected, the soft-start time in 1ms.
15	EN	I	Enable input control, leaving this pin floating enables the converter. It can also be used to adjust the input UVLO by connecting to the resistor divider between VIN and EN.
16	PGOOD	O	Open Drain Power Good Indicator, it is asserted low if output voltage is out of PGOOD threshold, Overvoltage or if the device is under thermal shutdown, EN shutdown or during soft start.
17	VREG5	I/O	4.7-V internal LDO output which can also be driven externally with a 5V input. This pin supplies voltage to the internal circuitry and gate driver. Bypass this pin with a 4.7-µF capacitor.
18	MODE	I	Switching Frequency, Current Limit selection and Light load operation mode selection pin. Connect this pin to a resistor divider from VREG5 and AGND for different MODE options shown in table 4.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
Input Voltage	VIN	–0.3	20	V
	SW	–2	19	
	SW(10 ns transient)	–3	20	
	EN	–0.3	6.5	
	BOOT –SW	–0.3	6.5	
	BOOT	–0.3	25.5	
	SS, MODE, FB	–0.3	6.5	
	VREG5	–0.3	6	
Output Voltage	PGOOD	–0.3	6.5	V
Output Current(2)	I_{OUT}		10	A
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) To be consistent with the TI reliability requirement of 100k Power-On-Hours at 105°C junction temperature, the output current must not exceed 10A continuously under 100% duty operation as to prevent electromigration failure in the solder. Higher junction temperature or longer power-on hours are achievable at lower than 10A continuos output current.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
Input Voltage	V_{IN}	4.5		17	V
	SW	–1.8		17	
	BOOT	–0.1		23.5	
	VREG5	–0.1		5.2	
Output Current	I_{LOAD}	0		8	A
Operating junction temperature	T_J	-40		150	°C

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6.4 Thermal Information

THERMAL METRIC(1)		RNN PACKAGE 18 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	42.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.0	°C/W
ψ_{JT}	Junction-to-top characterization parameter	0.5	°C/W
ψ_{JB}	Junction-to-board characterization parameter	10.0	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	0.5	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

6.5 Electrical Characteristics

T_J = –40°C to 150°C, VIN=12V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
I_{IN}	V_{IN} supply current	T_J = 25°C, V_{EN}=5 V, non switching		600	700	µA
I_{VINSDN}	V_{IN} shutdown current	T_J = 25°C, V_{EN}=0 V		7		µA
LOGIC THRESHOLD						
V_{ENH}	EN H-level threshold voltage		1.175	1.225	1.3	V
V_{ENL}	EN L-level threshold voltage		1.025	1.104	1.15	V
V_{ENHYS}				0.121		V
I_{ENp1}	EN pull-up current	V_{EN} = 1.0 V	0.35	1.91	2.95	µA
I_{ENp2}		V_{EN} = 1.3 V	3	4.197	5.5	µA
FEEDBACK VOLTAGE						
V_{FB}	FB voltage	T_J = 25°C	598	600	602	mV
		T_J = 0°C to 85°C	597.5	600	602.5	mV
		T_J = –40°C to 85°C	594	600	602.5	mV
		T_J = –40°C to 150°C	594	600	606	mV
LDO VOLTAGE						
VREG5	LDO Output voltage	T_J = –40°C to 150°C	4.58	4.7	4.83	V
ILIM5	LDO Output Current limit	T_J = –40°C to 150°C	100	150	200	mA
MOSFET						
$R_{DS(on)H}$	High side switch resistance	T_J = 25°C, V_{VREG5} = 4.7 V		19		mΩ
$R_{DS(on)L}$	Low side switch resistance	T_J = 25°C, V_{VREG5} = 4.7 V		9.4		mΩ
SOFT START						
I_{ss}	Soft start charge current	T_J = -40°C to 150°C	4.9	6	7.1	µA
CURRENT LIMIT						
I_{OCL}	Current Limit (Low side sourcing)	ILIM-1 option, Valley Current	6	7.1	8.15	A
		ILIM option, Valley Current	8	9.4	10.8	A
	Current Limit (Low side negative)	Valley Current		3		A
POWER GOOD						
$V_{PGOODTH}$	PGOOD threshold	V_{FB} falling (fault)		84%		%V_{REF}
		V_{FB} rising (good)		93%		%V_{REF}
		V_{FB} rising (fault)		116%		%V_{REF}
		V_{FB} falling (good)		107%		%V_{REF}
OUTPUT UNDERVOLTAGE PROTECTION						

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T_J = –40°C to 150°C, VIN=12V (unless otherwise noted)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{UVP}	Output UVP threshold	Hiccup detect		68% x V_{FB}		
THERMAL SHUTDOWN						
T_{SDN}	Thermal shutdown threshold	Shutdown temperature		160		°C
		Hysteresis		15		°C
$T_{SDN\ VREG5}$	VREG5 thermal shutdown threshold	Shutdown temperature		171		°C
		Hysteresis		18		°C
UVLO						
UVLO	UVLO threshold	VREG5 rising voltage	4.1	4.3	4.5	V
		VREG5 falling voltage	3.34	3.57	3.8	V
		VREG5 hysteresis		730		mV

6.6 Timing Requirements

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
ON-TIME TIMER CONTROL						
t_{ON}	SW On Time	V_{IN} = 12 V, V_{OUT}=3.3 V, F_{SW} = 800 kHz	310	340	380	ns
$t_{ON\ min}$	SW Minimum on time	V_{IN} = 17 V, V_{OUT}=0.6 V, F_{SW}= 1200 kHz		54		ns
t_{OFF}	SW Minimum off time	25°C, V_{FB}=0.5 V			310	ns
SOFT START						
t_{SS}	Soft start time	Internal soft start time		1.045		ms
OUTPUT UNDERVOLTAGE AND OVERVOLTAGE PROTECTION						
t_{UVPDEL}	Output Hiccup delay relative to SS time	UVP detect		1		cycle
t_{UVPEN}	Output Hiccup enable delay relative to SS time	UVP detect		7		cycle

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6.7 Typical Characteristics

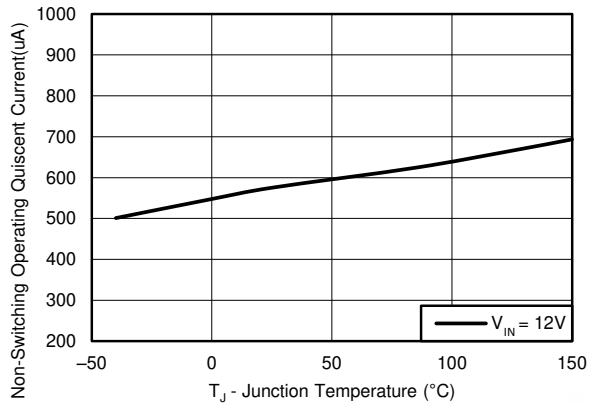


図 6-1. Quiescent Current vs Temperature

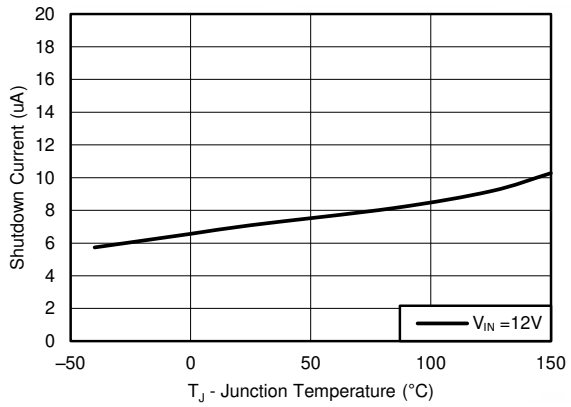


図 6-2. Shutdown Current vs Temperature

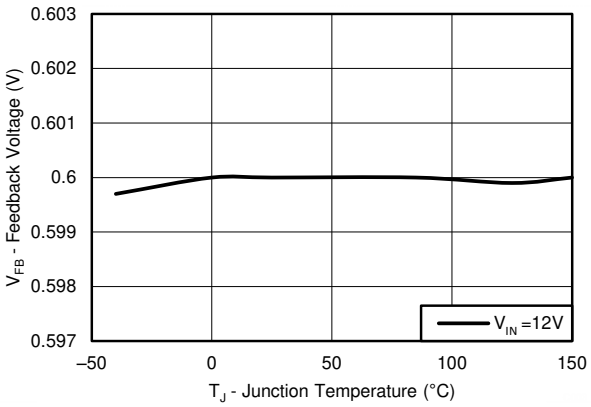


図 6-3. Feedback Voltage vs Temperature

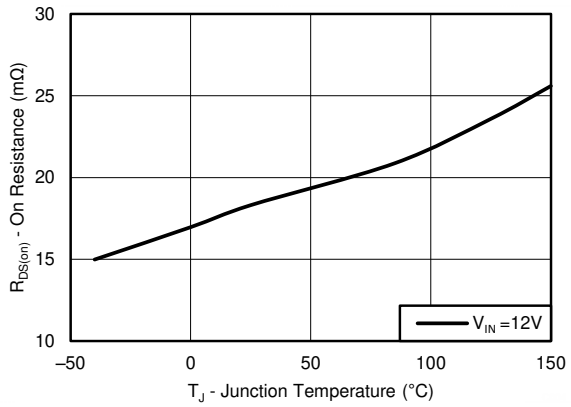


図 6-4. High-side R_{dson} vs Temperature

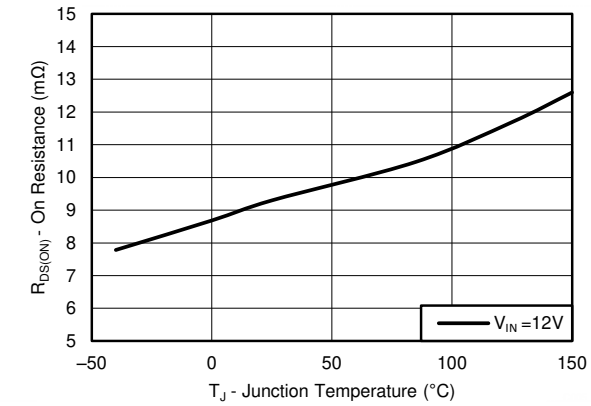


図 6-5. Low-side R_{dson} vs Temperature

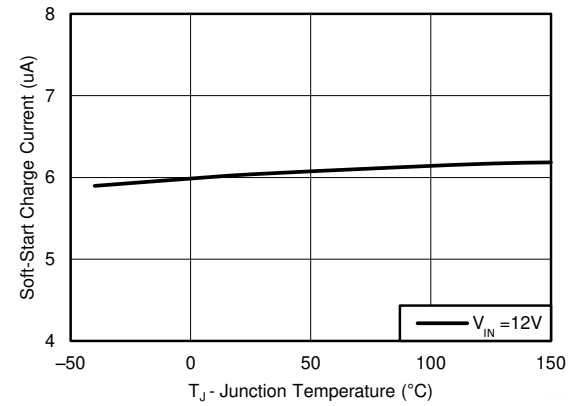


図 6-6. Soft-Start Charge Current vs Temperature

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6.7 Typical Characteristics (continued)

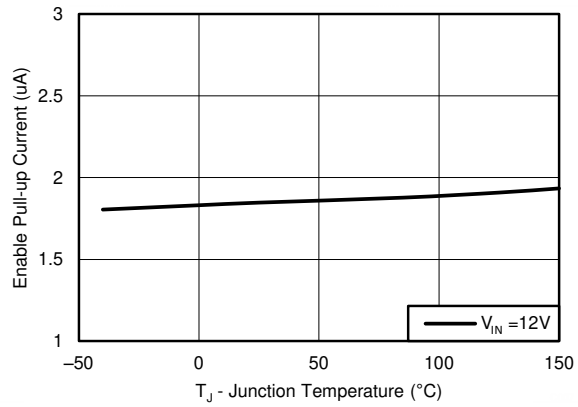


図 6-7. Enable Pull-Up Current, V_{EN} =1.0V

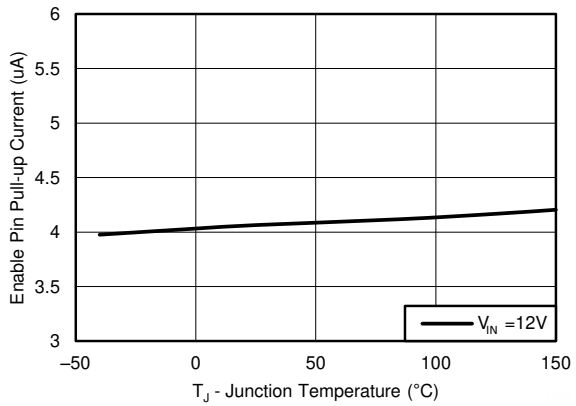


図 6-8. Enable Pull-Up Current, V_{EN} =1.3V

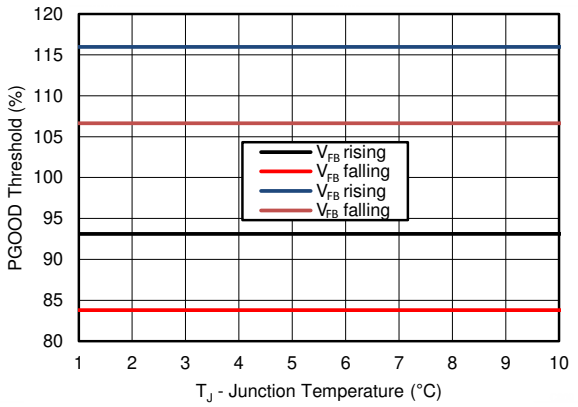


図 6-9. PGOOD Threshold vs Temperature

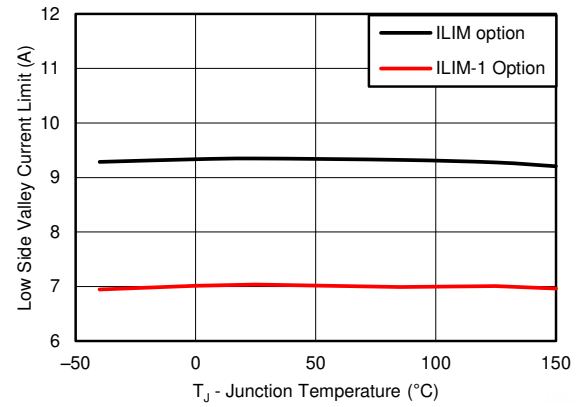


図 6-10. Valley Current Limit vs Temperature

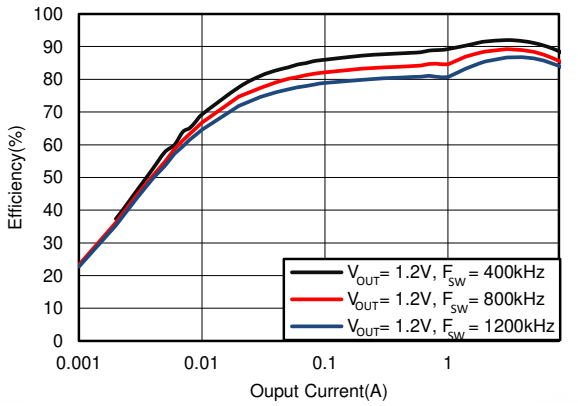


図 6-11. Efficiency with Internal VREG5 = 4.7 V, V_{IN} = 12 V

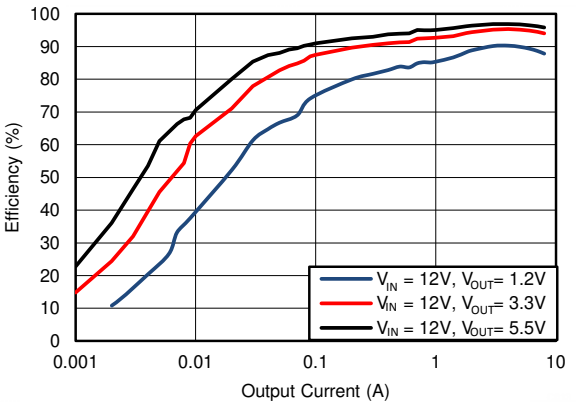


図 6-12. Efficiency, Mode = DCM, F_{SW} = 400kHz

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6.7 Typical Characteristics (continued)

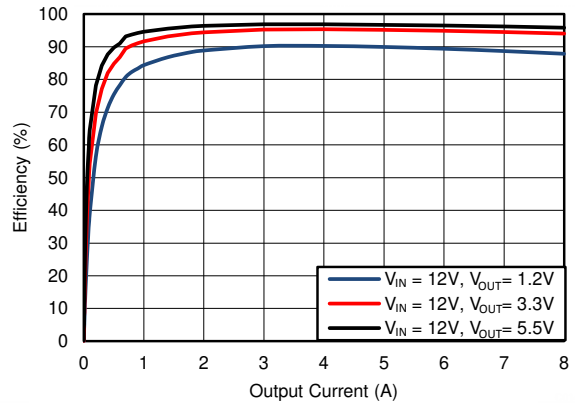


図 6-13. Efficiency, Mode = FCCM, F_{SW} = 400kHz

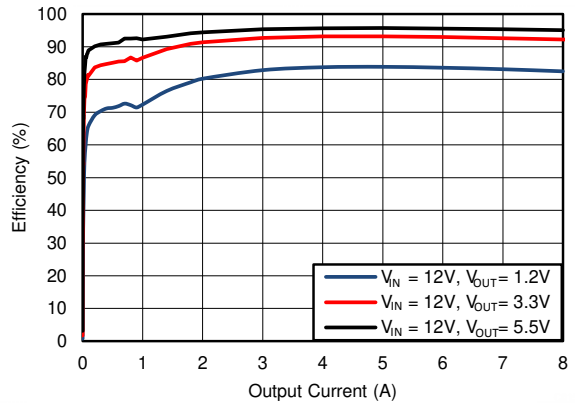


図 6-14. Efficiency, Mode = DCM, F_{SW} = 1200kHz

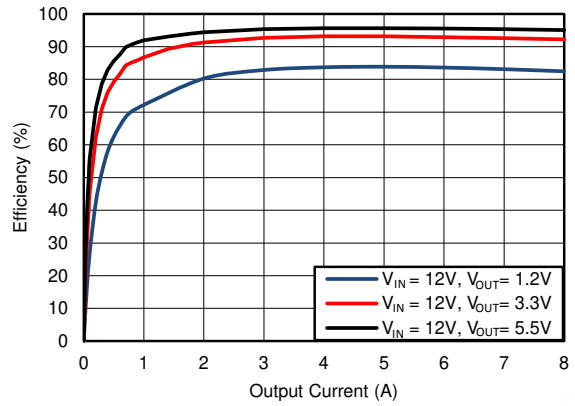


図 6-15. Efficiency, Mode = FCCM, F_{SW} = 1200kHz

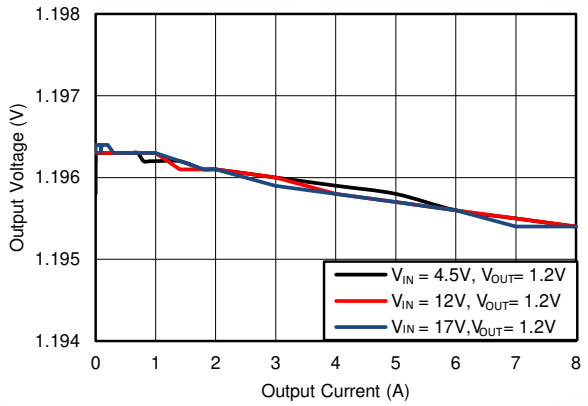


図 6-16. Load Regulation, F_{SW} = 400kHz

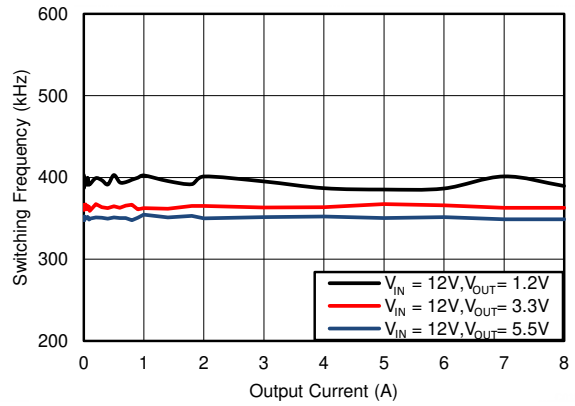


図 6-17. F_{SW} Load Regulation, Mode = FCCM, F_{SW} = 400kHz

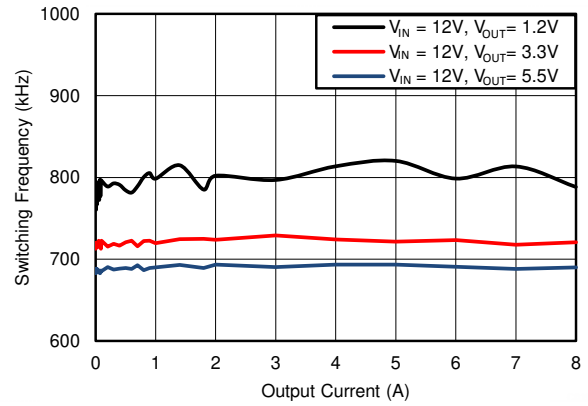


図 6-18. F_{SW} Load Regulation, Mode = FCCM, F_{SW} = 800kHz

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6.7 Typical Characteristics (continued)

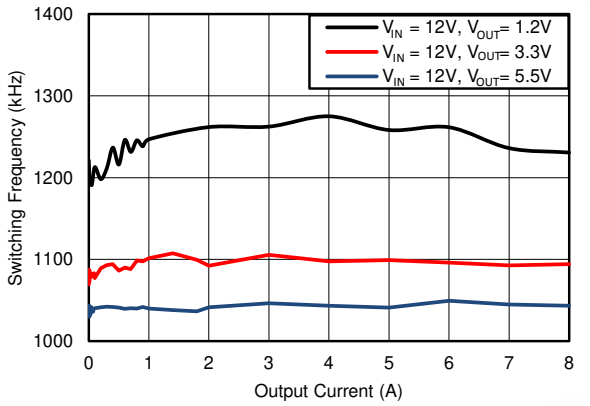


図 6-19. F_{SW} Load Regulation, Mode = FCCM, F_{SW} = 1200kHz

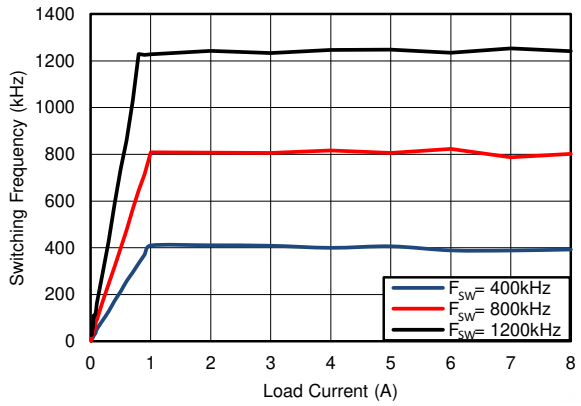


図 6-20. F_{SW} Load Regulation, Mode = DCM, V_{IN} = 12V, V_{OUT}=1.2V

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7 Detailed Description

7.1 Overview

The TPS568215 is a high-density, synchronous, step-down buck converter which can operate from 4.5-V to 17-V input voltage (V_{IN}). The device has 19-mΩ and 9-mΩ integrated MOSFETs that enable high efficiency up to 8 A. The device employs D-CAP3™ control mode that provides fast transient response with no external compensation components and an accurate feedback voltage. The control topology provides seamless transition between FCCM operating mode at higher load condition and DCM/Eco-mode™ operation at lighter load condition. DCM/Eco-mode™ allows the TPS568215 to maintain high efficiency at light load. The TPS568215 is able to adapt to both low equivalent series resistance (ESR) output capacitors such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors.

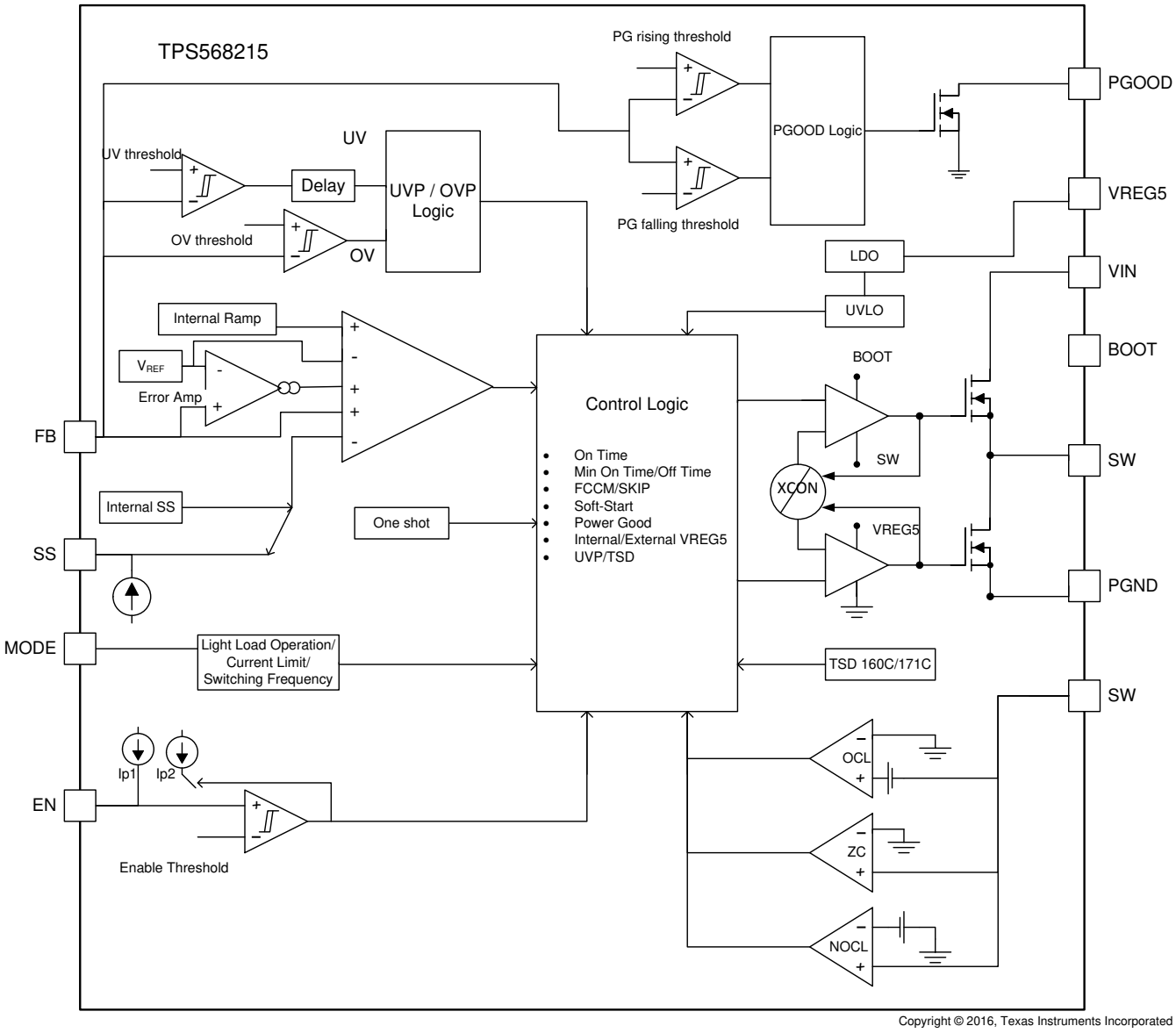
The TPS568215 has three selectable switching frequencies (F_{SW}) 400 kHz, 800 kHz, and 1200 kHz which gives the flexibility to optimize the design for higher efficiency or smaller size. There are two selectable current limits. All these options are configured by choosing the right voltage on the MODE pin.

The TPS568215 has a 4.7-V internal LDO that creates bias for all internal circuitry. There is a feature to overdrive this internal LDO with an external voltage on the VREG5 pin which improves the converter efficiency. The undervoltage lockout (UVLO) circuit monitors the VREG5 pin voltage to protect the internal circuitry from low input voltages. The device has an internal pullup current source on the EN pin which can enable the device even with the pin floating.

Soft-start time can be selected by connecting a capacitor to the SS pin. The device is protected from output short, undervoltage, and overtemperature conditions.

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7.2 Functional Block Diagram



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7.3 Feature Description

7.3.1 PWM Operation and D-CAP3™ Control Mode

The TPS568215 operates using the adaptive on-time PWM control with a proprietary D-CAP3 control mode which enables low external component count with a fast load transient response while maintaining a good output voltage accuracy. At the beginning of each switching cycle the high side MOSFET is turned on for an on-time set by an internal one shot timer. This on-time is set based on the converter's input voltage, output voltage and the pseudo-fixed frequency hence this type of control topology is called an adaptive on-time control. The one shot timer resets and turns on again after the feedback voltage (V_{FB}) falls below the internal reference voltage (V_{REF}). An internal ramp is generated which is fed to the FB pin to simulate the output voltage ripple. This enables the use of very low-ESR output capacitors such as multi-layered ceramic caps (MLCC). No external current sense network or loop compensation is required for DCAP3™ control topology.

The TPS568215 includes an error amplifier that makes the output voltage very accurate. This error amplifier is absent in other flavors of D-CAP3 control mode. For any control topology that is compensated internally, there is a range of the output filter it can support. The output filter used with the TPS568215 is a low pass L-C circuit. This L-C filter has double pole that is described in

$$f_P = \frac{1}{2 \times \pi \times \sqrt{L_{OUT} \times C_{OUT}}} \quad (1)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS568215. The low frequency L-C double pole has a 180 degree in phase. At the output filter frequency, the gain rolls off at a –40dB per decade rate and the phase drops rapidly. The internal ripple generation network introduces a high-frequency zero that reduces the gain roll off from –40dB to –20dB per decade and increases the phase to 90 degree one decade above the zero frequency. The internal ripple injection high frequency zero is changed according to the switching frequency selected as shown in table below. The inductor and capacitor selected for the output filter must be such that the double pole is located close enough to the high-frequency zero so that the phase boost provided by this high-frequency zero provides adequate phase margin for the stability requirement. The crossover frequency of the overall system must usually be targeted to be less than one-fifth of the switching frequency (F_{SW}).

表 7-1. Ripple Injection Zero

Switching Frequency (kHz)	Zero Location (kHz)
400	7.1
800	14.3
1200	21.4

表 7-2 lists the inductor values and part numbers that are used to plot the efficiency curves in the セクション 6.7 section.

表 7-2. Inductor Values

V_{OUT}(V)	F_{SW}(kHz)	L_{OUT}(uH)	Würth Part Number(1)
1.2	400	1.2	744325120
	800	0.68	744311068
	1200	0.47	744314047
3.3	400	2.4	744325240
	800	1.5	744314150
	1200	1.1	744314110

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表 7-2. Inductor Values (continued)

V_{OUT}(V)	F_{SW}(kHz)	L_{OUT}(uH)	Würth Part Number(1)
5.5	400	3.3	744325330
	800	2.4	744325240
	1200	1.2	744325120

(1) See *Third-Party Products* disclaimer

7.3.2 Eco-mode™ Control

The TPS568215 is designed with Eco-mode™ control to increase efficiency at light loads. This option can be chosen using the MODE pin as shown in table 3. As the output current decreases from heavy load condition, the inductor current is also reduced. If the output current is reduced enough, the valley of the inductor current reaches the zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The low-side MOSFET is turned off when a zero inductor current is detected. As the load current further decreases the converter runs into discontinuous conduction mode. The on-time is kept approximately the same as it is in continuous conduction mode. The off-time increases as it takes more time to discharge the output with a smaller load current. The light load current where the transition to Eco-mode™ operation happens ($I_{OUT(LL)}$) can be calculated from 式 2.

$$I_{OUT(LL)} = \frac{1}{2 \times L_{OUT} \times F_{SW}} \times \frac{(V_{IN} - V_{OUT}) \times V_{OUT}}{V_{IN}} \quad (2)$$

After identifying the application requirements, design the output inductance so that the inductor peak-to-peak ripple current is approximately between 20% and 30% of the $I_{CC(max)}$ (peak current in the application). it is also important to size the inductor properly so that the valley current doesn't hit the negative low side current limit.

7.3.3 4.7 V LDO and External Bias

The VREG5 pin is the output of the internal 4.7-V linear regulator that creates the bias for all the internal circuitry and MOSFET gate drivers. The VREG5 pin needs to be bypassed with a 4.7-µF capacitor. An external voltage that is above the LDO's internal output voltage can override the internal LDO, switching it to the external rail after a higher voltage is detected. This enhances the efficiency of the converter because the quiescent current now runs off this external rail instead of the input power supply. The UVLO circuit monitors the VREG5 pin voltage and disables the output when VREG5 falls below the UVLO threshold. When using an external bias on the VREG5 rail, any power-up and power-down sequencing can be applied but it is important to understand that if there is a discharge path on the VREG5 rail that can pull a current higher than the internal LDO's current limit (ILIM5) from the VREG5, then the VREG5 LDO turns off thereby shutting down the output of TPS568215. If such condition does not exist and if the external VREG5 rail is turned off, the VREG5 voltage switches over to the internal LDO voltage which is 4.7 V typically in a few nanoseconds. Figure 26 below shows this transition of the VREG5 voltage from an external bias of 5.5 V to the internal LDO output of 4.7 V when the external bias to VREG5 is disabled while the output of TPS568215 remains unchanged.

7.3.4 MODE Selection

TPS568215 has a MODE pin that can offer 12 different states of operation as a combination of Current Limit, Switching Frequency and Light Load operation. The device can operate at two different current limits ILIM-1 and ILIM to support an output continuous current of 6 A, 8 A respectively. The TPS568215 is designed to compare the valley current of the inductor against the current limit thresholds so understand that the output current is half the ripple current above the valley current. TPS568215 can operate at three different frequencies of 400 kHz, 800 kHz and 1200 kHz and also can choose between Eco-mode™ and FCCM mode. The device reads the voltage on the MODE pin during start-up and latches onto one of the MODE options listed below in table 3. The voltage on the MODE pin can be set by connecting this pin to the center tap of a resistor divider connected between VREG5 and AGND. A guideline for the top resistor (R_{M_H}) and the bottom resistor (R_{M_L}) as 5% resistors is shown in Table 3. It is important that the voltage for the MODE pin is derived from the VREG5 rail

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only must internally this voltage is referenced to detect the MODE option. The MODE pin setting can be reset only by a VIN power cycling.

表 7-3. Mode Pin Resistor Settings

R_{M_L} (kΩ)	R_{M_H} (kΩ)	Light Load Operation	Current Limit	Frequency (kHz)
5.1	300	FCCM	ILIM-1	400
10	200	FCCM	ILIM	400
20	160	FCCM	ILIM-1	800
20	120	FCCM	ILIM	800
51	200	FCCM	ILIM-1	1200
51	180	FCCM	ILIM	1200
51	150	DCM	ILIM-1	400
51	120	DCM	ILIM	400
51	91	DCM	ILIM-1	800
51	82	DCM	ILIM	800
51	62	DCM	ILIM-1	1200
51	51	DCM	ILIM	1200

図 7-1 below shows the typical start-up sequence of the device after the enable signal crosses the EN turn-on threshold. After the voltage on VREG5 crosses the rising UVLO threshold it takes about 500 us to read the first mode setting and approximately 100 us from there to finish the last mode setting. The output voltage starts ramping after the mode reading is done.

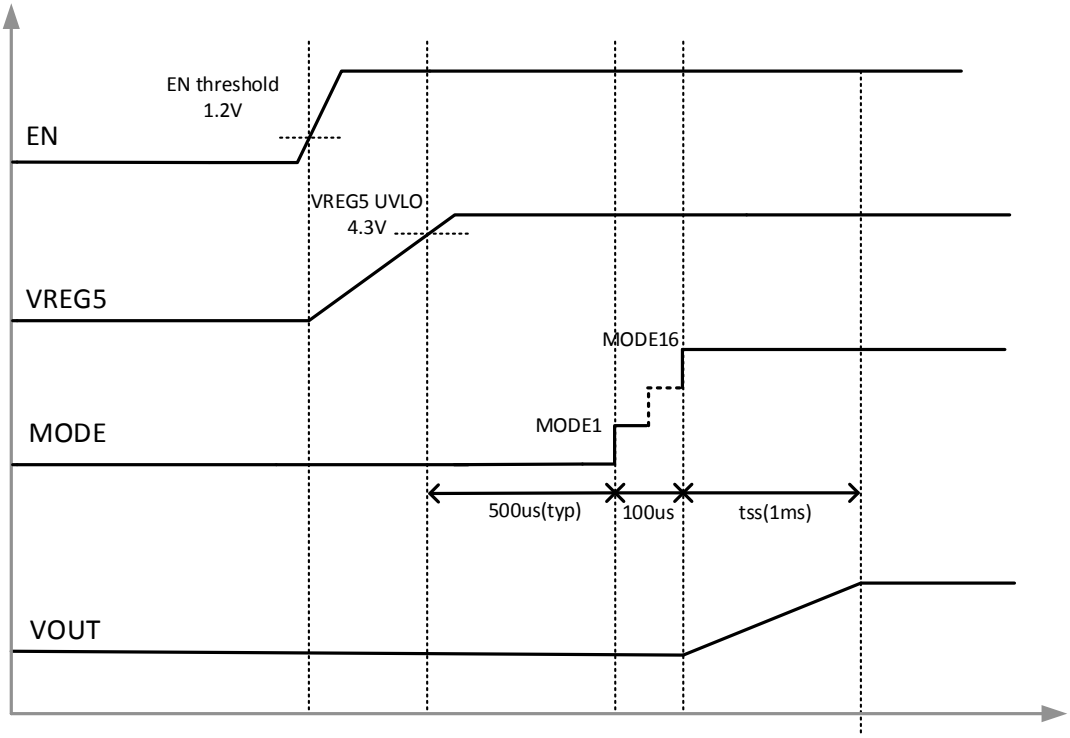


図 7-1. Power-Up Sequence

7.3.5 Soft Start and Pre-biased Soft Start

The TPS568215 has an adjustable soft-start time that can be set by connecting a capacitor on SS pin. When the EN pin becomes high, the soft-start charge current (I_{SS}) begins charging the external capacitor (C_{SS}) connected

between SS and AGND. The devices tracks the lower of the internal soft-start voltage or the external soft-start voltage as the reference. The equation for the soft-start time (T_{SS}) is shown in 式 3:

$$T_{SS(S)} = \frac{C_{SS} \times V_{REF}}{I_{SS}} \quad (3)$$

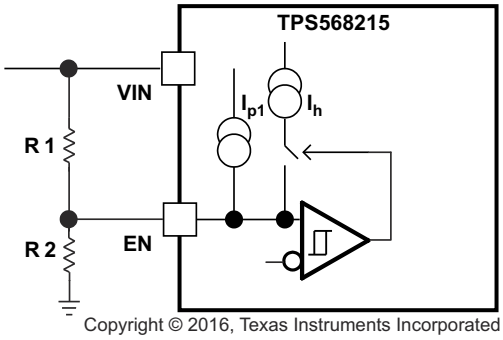
where

- V_{REF} is 0.6 V and I_{SS} is 6 µA

If the output capacitor is pre-biased at startup, the device initiates switching and starts ramping up only after the internal reference voltage becomes greater than the feedback voltage V_{FB}. This scheme ensures that the converters ramp up smoothly into regulation point.

7.3.6 Enable and Adjustable UVLO

The EN pin controls the turn-on and turn-off of the device. When EN pin voltage is above the turn-on threshold which is around 1.2 V, the device starts switching and when the EN pin voltage falls below the turn-off threshold which is around 1.1V it stops switching. If the user application requires a different turn-on (V_{START}) and turn-off thresholds (V_{STOP}) respectively, the EN pin can be configured as shown in 図 7-2 by connecting a resistor divider between VIN and EN. The EN pin has a pull-up current I_{p1} that sets the default state of the pin when it is floating. This current increases to I_{p2} when the EN pin voltage crosses the turn-on threshold. The UVLO thresholds can be set by using 式 4 and 式 5.



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図 7-2. Adjustable VIN Under Voltage Lock Out

$$R1 = \frac{V_{START}\left(\frac{V_{ENFALLING}}{V_{ENRISING}}\right) - V_{STOP}}{I_{p1}\left(1 - \frac{V_{ENFALLING}}{V_{ENRISING}}\right) + I_h} \quad (4)$$

$$R2 = \frac{R1 \times V_{ENFALLING}}{V_{STOP} - V_{ENFALLING} + R1\ I_{p2}} \quad (5)$$

where

- I_{p2} = 4.197 µA
- I_{p1} = 1.91 µA
- I_h = 2.287 µA
- $V_{ENRISING}$ = 1.225 V
- $V_{ENFALLING}$ = 1.104 V

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7.3.7 Power Good

The Power-Good (PGOOD) pin is an open drain output. After the FB pin voltage is between 93% and 107% of the internal reference voltage (V_{REF}) the PGOOD is de-asserted and floats after a 200 µs de-glitch time. TI recommends a pullup resistor of 10 kΩ to pull it up to VREG5. The PGOOD pin is pulled low when the FB pin voltage is lower than V_{UVP} or greater than V_{OVP} threshold; or, in an event of thermal shutdown or during the soft-start period.

7.3.8 Overcurrent Protection and Undervoltage Protection

The output overcurrent limit (OCL) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored during the OFF state by measuring the low-side FET drain to source voltage. This voltage is proportional to the switch current. During the on time of the high-side FET switch, the switch current increases at a linear rate determined by input voltage , output voltage, the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{OUT}. If the measured drain to source voltage of the low-side FET is above the voltage proportional to current limit, the low side FET stays on until the current level becomes lower than the OCL level which reduces the output current available. When the current is limited the output voltage tends to drop because the load demand is higher than what the converter can support. When the output voltage falls below 68% of the target voltage, the UVP comparator detects it and shuts down the device after a wait time of 1ms, the device re-starts after a hiccup time of 7ms. In this type of valley detect control the load current is higher than the OCL threshold by one half of the peak to peak inductor ripple current. When the overcurrent condition is removed, the output voltage returns to the regulated value. If an OCL condition happens during start-up then the device enters hiccup-mode immediately without a wait time of 1 ms.

7.3.9 Out-of-Bounds Operation

The device has an out-of-bounds (OOB) overvoltage protection that protects the output load at a much lower overvoltage threshold of 8% above the target voltage. OOB protection does not trigger an overvoltage fault, OOB protection operates as an early no-fault overvoltage protection mechanism. During the OOB operation, the controller operates in forced PWM mode only by turning on the low-side FET. Turning on the low-side FET beyond the zero inductor current quickly discharges the output capacitor thus causing the output voltage to fall quickly toward the setpoint. During the operation, the cycle-by cycle negative current limit is also activated to ensure the safe operation of the internal FETs.

7.3.10 UVLO Protection

Under voltage lock out protection (UVLO) monitors the internal VREG5 regulator voltage. When the VREG5 voltage is lower than UVLO threshold voltage, the device is shut off. This protection is non-latching.

7.3.11 Thermal Shutdown

The device monitors the internal die temperature. If this temperature exceeds the thermal shutdown threshold value (T_{SDN} typically 160°C) the device shuts off. This is a non-latch protection. During start up, if the device temperature is higher than 160°C the device does not start switching and does not load the MODE settings. If the device temp goes higher than T_{SDN} threshold after startup, it stops switching with SS reset to ground and an internal discharge switch turns on to quickly discharge the output voltage. The device re-starts switching when the temperature goes below the thermal shutdown threshold but the MODE settings are not re-loaded again. There is a second higher thermal protection on the device $T_{SDN\ VREG5}$ which protects it from over temperature conditions not caused by the switching of the device itself. This threshold is at typically 170°C. Even under nonswitching condition of the device after exceeding T_{SDN} threshold, if it still continues to heat up the VREG5 output shuts off after temperature goes beyond $T_{SDN\ VREG5}$, thereby shutting down the device completely.

7.3.12 Output Voltage Discharge

The device has a 500ohm discharge switch that discharges the output V_{OUT} through SW node during any event of fault like output overvoltage, output undervoltage , TSD , if VREG5 voltage below the UVLO and when the EN pin voltage (V_{EN}) is below the turn-on threshold.

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7.4 Device Functional Modes

7.4.1 Light Load Operation

When the MODE pin is selected to operate in FCCM mode, the converter operates in continuous conduction mode (FCCM) during light-load conditions. During FCCM, the switching frequency (F_{SW}) is maintained at an almost constant level over the entire load range which is suitable for applications requiring tight control of the switching frequency and output voltage ripple at the cost of lower efficiency under light load. If the MODE pin is selected to operate in DCM/Eco-mode™, the device enters pulse skip mode after the valley of the inductor ripple current crosses zero. The Eco-mode™ maintains higher efficiency at light load with a lower switching frequency.

7.4.2 Standby Operation

The TPS568215 can be placed in standby mode by pulling the EN pin low. The device operates with a shutdown current of 7uA when in standby condition.

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8 Application and Implementation

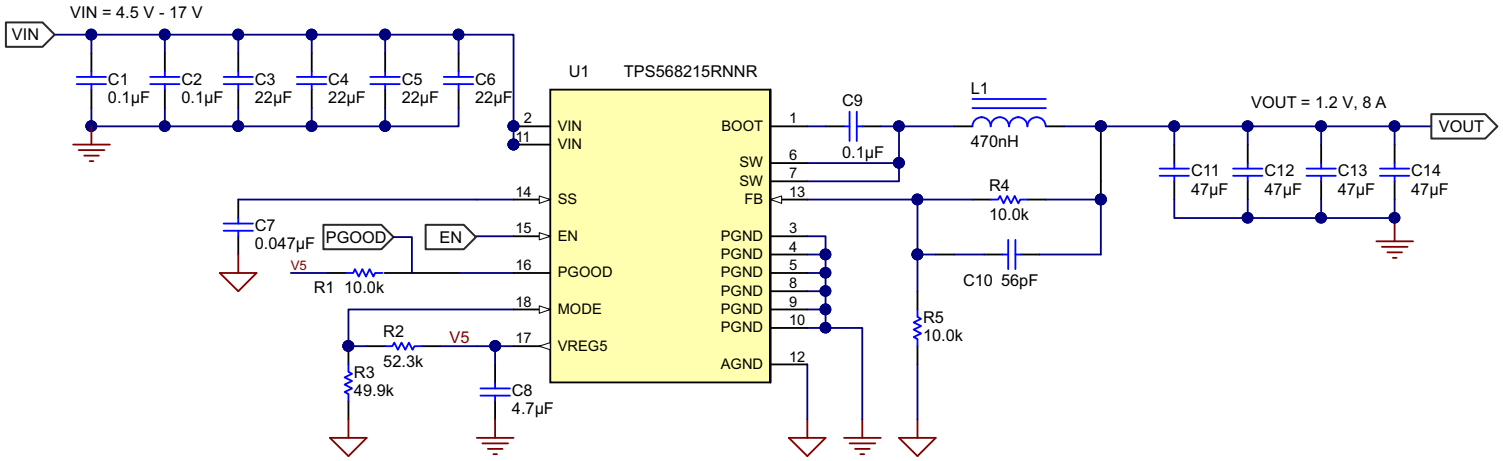
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8.1 Application Information

The schematic of 図 8-1 shows a typical application for TPS568215. This design converts an input voltage range of 4.5 V to 17 V down to 1.2 V with a maximum output current of 8 A.

8.2 Typical Application



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図 8-1. Application Schematic

8.2.1 Design Requirements

表 8-1. Design Parameters

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNIT
V_{OUT}	Output voltage			1.2		V
I_{OUT}	Output current			8		A
ΔV_{OUT}	Transient response	4-A load step		±30		mV
V_{IN}	Input voltage		4.5	12	17	V
$V_{OUT(ripple)}$	Output voltage ripple			<10		$mV_{(P-P)}$
	Start input voltage	Input voltage rising		Internal UVLO		V
	Stop input voltage	Input voltage falling		Internal UVLO		V
f_{SW}	Switching frequency			1.2		MHz
Operating Mode				DCM		
T_A	Ambient temperature			25		°C

8.2.2 Detailed Design Procedure

8.2.2.1 External Component Selection

8.2.2.1.1 Output Voltage Set Point

To change the output voltage of the application, it is necessary to change the value of the upper feedback resistor. By changing this resistor the user can change the output voltage above 0.6 V. See 式 6

$$V_{OUT} = 0.6 \times \left(1 + \frac{R_{UPPER}}{R_{LOWER}}\right) \tag{6}$$

8.2.2.1.2 Switching Frequency and Mode Selection

Switching Frequency, current limit and switching mode (DCM or FCCM) are set by a voltage divider from VREG5 to GND connected to the MODE pin. See 表 7-3 for possible MODE pin configurations. Switching frequency selection is a tradeoff between higher efficiency and smaller system solution size. Lower switching frequency yields higher overall efficiency but relatively bigger external components. Higher switching frequencies cause additional switching losses which impact efficiency and thermal performance. For this design 1.2 MHz is chosen as the switching frequency, the switching mode is DCM and the output current is 8 A.

8.2.2.1.3 Inductor Selection

The inductor ripple current is filtered by the output capacitor. A higher inductor ripple current means the output capacitor must have a ripple current rating higher than the inductor ripple current. See 表 8-2 for recommended inductor values.

The RMS and peak currents through the inductor can be calculated using 式 7 and 式 8. It is important that the inductor is rated to handle these currents.

$$I_{L(rms)} = \sqrt{\left(I^2_{OUT} + \frac{1}{12} \times \left(\frac{V_{OUT} \times \left(V_{IN(max)} - V_{OUT}\right)}{V_{IN(max)} \times L_{OUT} \times F_{SW}}\right)^2\right)} \tag{7}$$

$$I_{L(peak)} = I_{OUT} + \frac{I_{OUT(ripple)}}{2} \tag{8}$$

During transient/short circuit conditions the inductor current can increase up to the current limit of the device so it is safe to choose an inductor with a saturation current higher than the peak current under current limit condition.

8.2.2.1.4 Output Capacitor Selection

After selecting the inductor the output capacitor needs to be optimized. In D-CAP3 control mode, the regulator reacts within one cycle to the change in the duty cycle so the good transient performance can be achieved without needing large amounts of output capacitance. The recommended output capacitance range is given in 表 8-2

Ceramic capacitors have very low ESR, otherwise the maximum ESR of the capacitor must be less than $V_{OUT(ripple)}/I_{OUT(ripple)}$

表 8-2. Recommended Component Values

V_{OUT} (V)	R_{LOWER} (kΩ)	R_{UPPER} (kΩ)	F_{SW} (kHz)	L_{OUT} (µH)	$C_{OUT(min)}$ (µF)	$C_{OUT(max)}$ (µF)	C_{FF} (pF)
0.6	10	0	400	0.68	300	500	–
			800	0.47	100	500	–
			1200	0.33	88	500	–
1.2		10	400	1.2	100	500	–
			800	0.68	88	500	–
			1200	0.47	88	500	–

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表 8-2. Recommended Component Values (continued)

V_{OUT} (V)	R_{LOWER} (kΩ)	R_{UPPER} (kΩ)	F_{SW} (kHz)	L_{OUT} (µH)	$C_{OUT(min)}$ (µF)	$C_{OUT(max)}$ (µF)	C_{FF} (pF)
3.3		45.3	400	2.4	88	500	100–220
			800	1.5	88	500	100–220
			1200	1.1	88	500	100–220
5.5		82.5	400	3.3	88	500	100–220
			800	2.4	88	500	100–220
			1200	1.2	88	700	100–220

8.2.2.1.5 Input Capacitor Selection

The minimum input capacitance required is given in 式 9.

$$C_{IN(min)} = \frac{I_{OUT} \times V_{OUT}}{V_{INripple} \times V_{IN} \times F_{SW}} \quad (9)$$

TI recommends using a high quality X5R or X7R input decoupling capacitors of 40 µF on the input voltage pin. The voltage rating on the input capacitor must be greater than the maximum input voltage. The capacitor must also have a ripple current rating greater than the maximum input current ripple of the application. The input ripple current is calculated by 式 10 below:

$$I_{CIN(rms)} = I_{OUT} \times \sqrt{\frac{V_{OUT}}{V_{IN(min)}} \times \frac{(V_{IN(min)} - V_{OUT})}{V_{IN(min)}}} \quad (10)$$

8.2.3 Application Curves

図 8-2 through 図 8-18 apply to the circuit of 図 8-1. V_{IN} = 12 V. T_a = 25 °C unless otherwise specified.

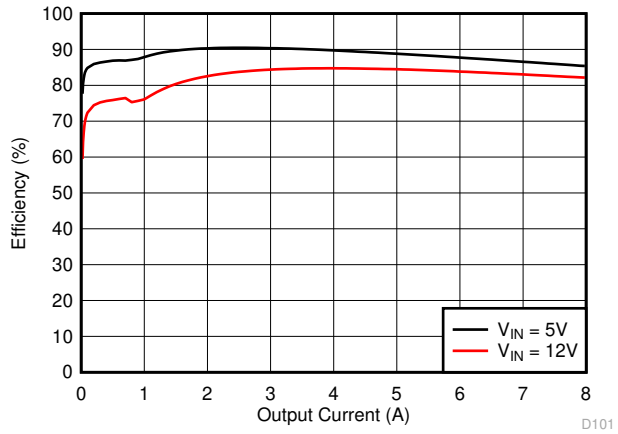


図 8-2. Efficiency

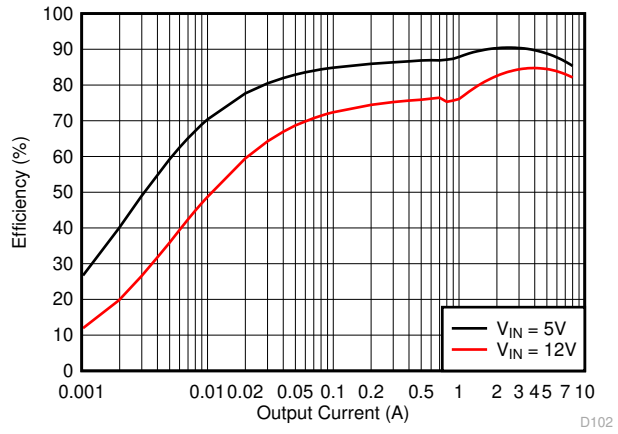


図 8-3. Light Load Efficiency

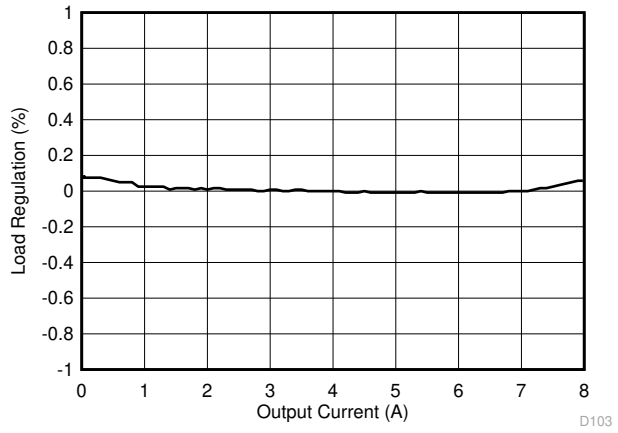


図 8-4. Load Regulation, V_{IN} = 5 V

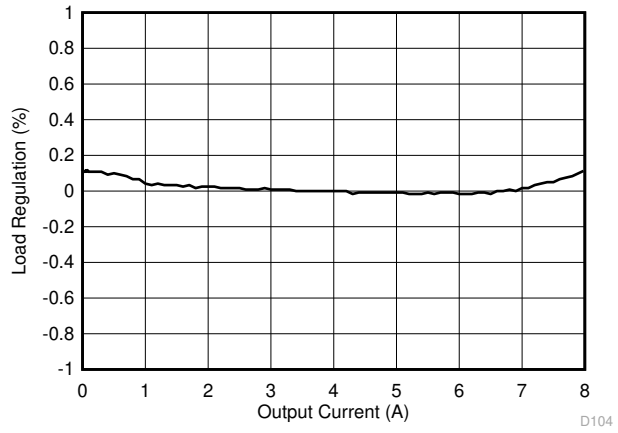


図 8-5. Load Regulation, V_{IN} = 12 V

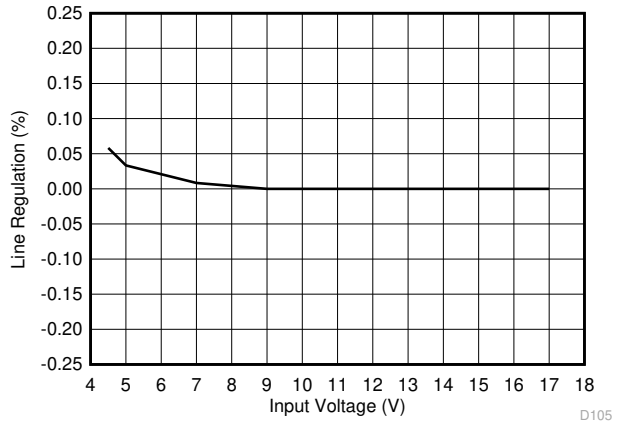


図 8-6. Line Regulation, I_{OUT} = 6 A

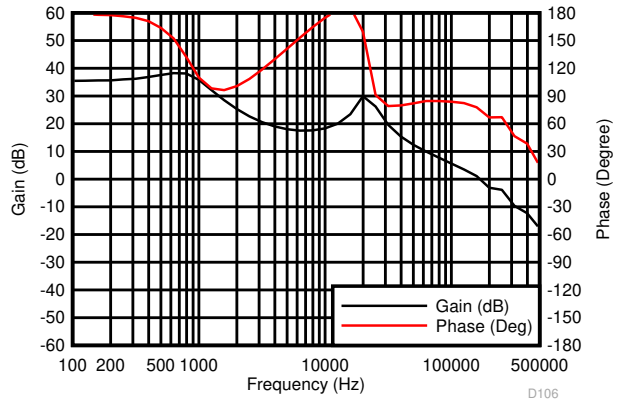


図 8-7. Loop Response, I_{OUT} = 6 A

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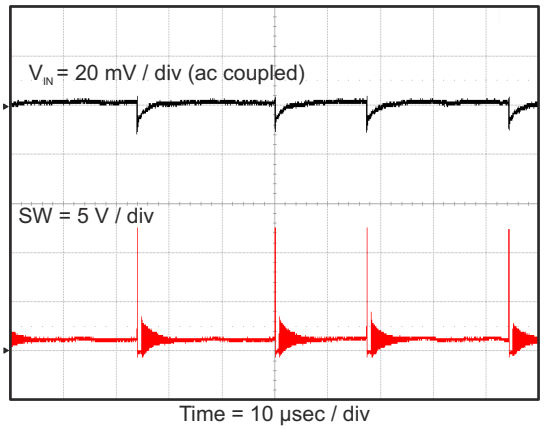


図 8-8. Input Voltage Ripple, I_{OUT} = 10 mA

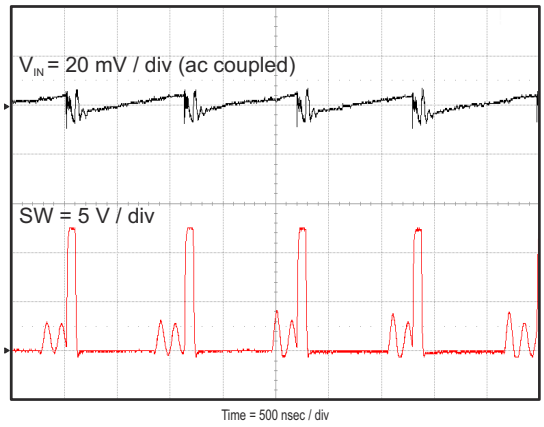


図 8-9. Input Voltage Ripple, I_{OUT} = 700 mA

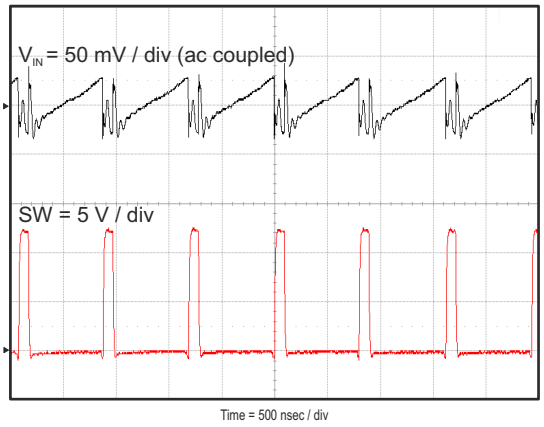


図 8-10. Input Voltage Ripple, I_{OUT} = 8 A

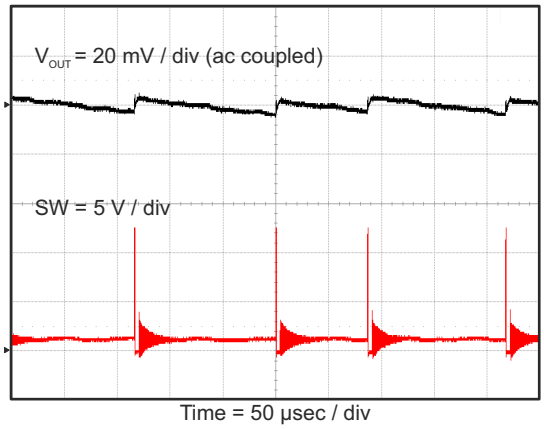


図 8-11. Output Voltage Ripple, I_{OUT} = 10 mA

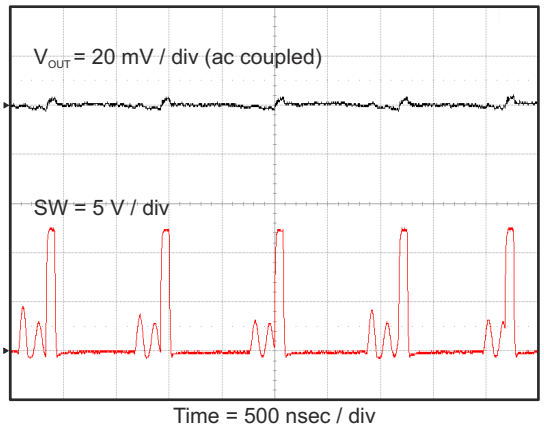


図 8-12. Output Voltage Ripple, I_{OUT} = 700 mA

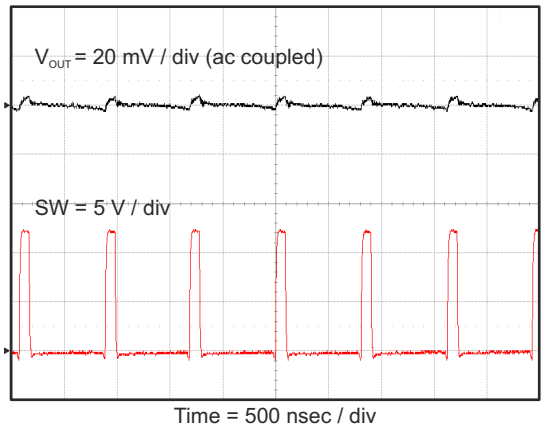


図 8-13. Output Voltage Ripple, I_{OUT} = 8 A

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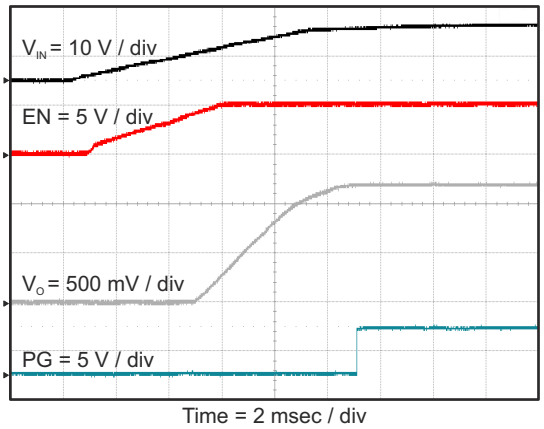


図 8-14. Start Up Relative to V_{IN} Rising

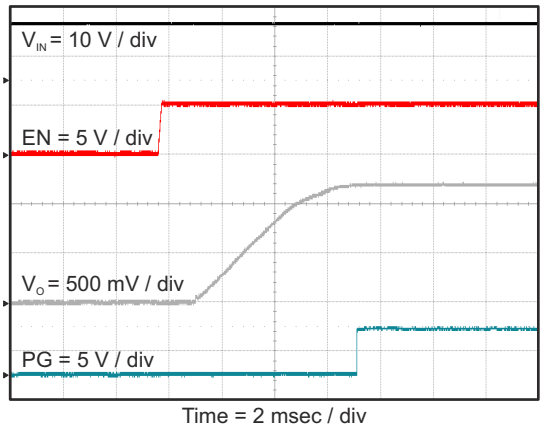


図 8-15. Start Up Relative to EN Rising

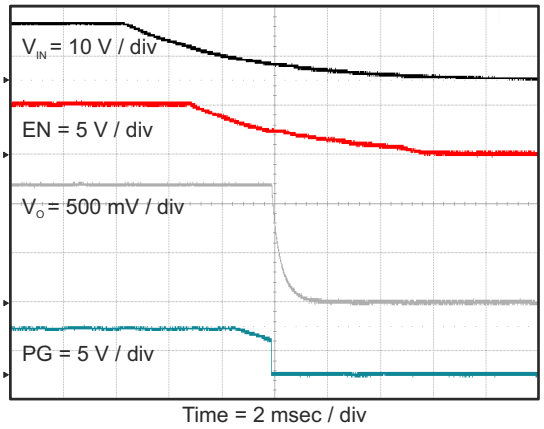


図 8-16. Shut Down Relative to V_{IN} Falling

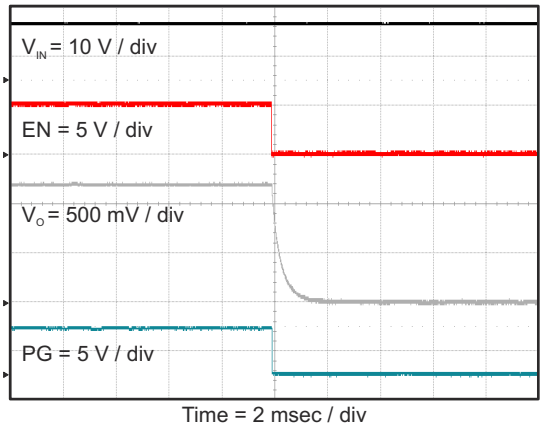


図 8-17. Shut Down Relative to EN Falling

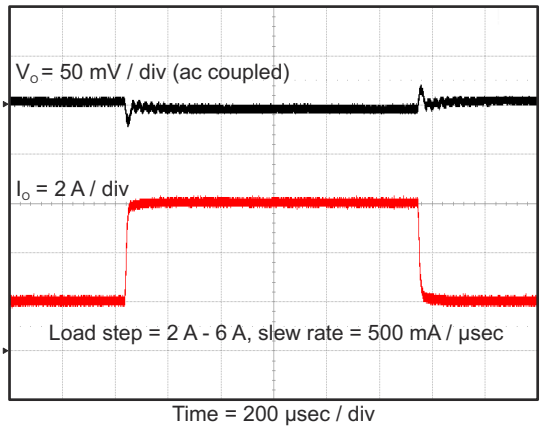


図 8-18. Transient Response

8.3 Power Supply Recommendations

The TPS568215 is intended to be powered by a well regulated dc voltage. The input voltage range is 4.5 to 17 V. TPS568215 is a buck converter. The input supply voltage must be greater than the desired output voltage for proper operation. Input supply current must be appropriate for the desired output current. If the input voltage supply is located far from the TPS568215 circuit, TI recommends some additional input bulk capacitance. Typical values are 100 µF to 470 µF.

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8.4 Layout

8.4.1 Layout Guidelines

- Recommend a four-layer or six-layer PCB for good thermal performance and with maximum ground plane. 3" × 3", four-layer PCB with 2-oz. copper used as example.
- Recommend having equal caps on each side of the IC. Place them right across VIN as close as possible.
- Inner layer 1 is ground with the PGND to AGND net tie.
- Inner layer 2 has VIN copper pour that has vias to the top layer VIN. *Place multiple vias under the device near VIN and GND and near input capacitors* to reduce parasitic inductance and improve thermal performance
- Bottom later is GND with the BOOT trace routing.
- Reference feedback to the quite AGND and routed away from the switch node.
- Make VIN trace wide to reduce the trace impedance.

8.4.2 Layout Example

図 8-19 shows the recommended top side layout. Component reference designators are the same as the circuit shown in 図 8-1. Resistor divider for EN is not used in the circuit of 図 8-1, but are shown in the layout for reference.

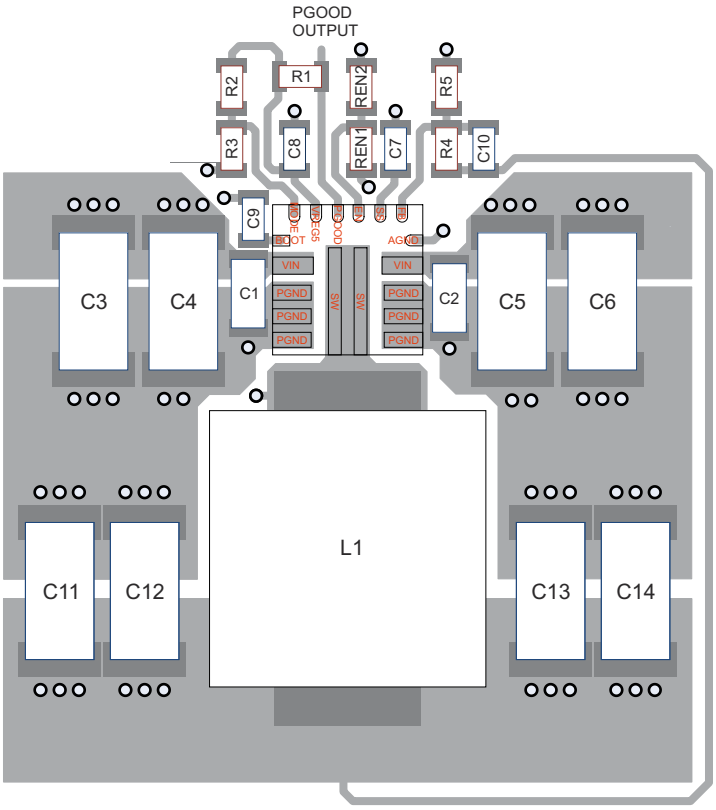


図 8-19. Top Side Layout

図 8-20 shows the recommended layout for the first internal layer. It is comprised of a large PGND plane and a smaller ANGD island. AGND and PGND are connected at a single point to reduce circulating currents.

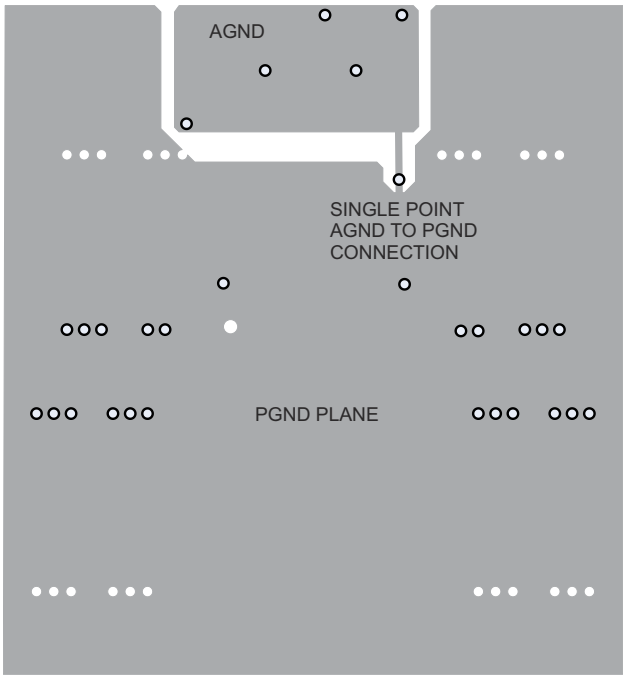


図 8-20. Mid Layer 1 Layout

図 8-21 shows the recommended layout for the second internal layer. It is comprised of a large PGND plane, a smaller copper fill area to connect the two top side V_{IN} copper areas and a second V_{OUT} copper fill area.

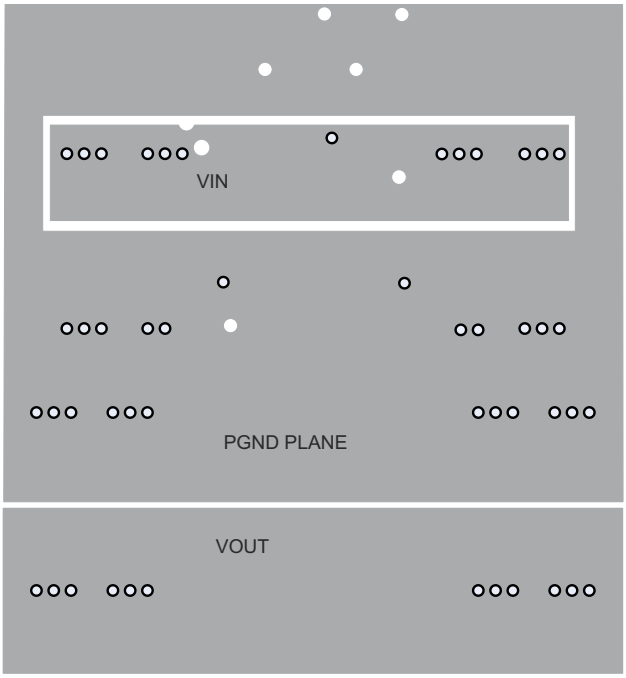


図 8-21. Mid Layer 2 Layout

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図 8-22 shows the recommended layout for the bottom layer. It is comprised of a large PGND plane and a trace to connect the BOOT capacitor to the SW node.

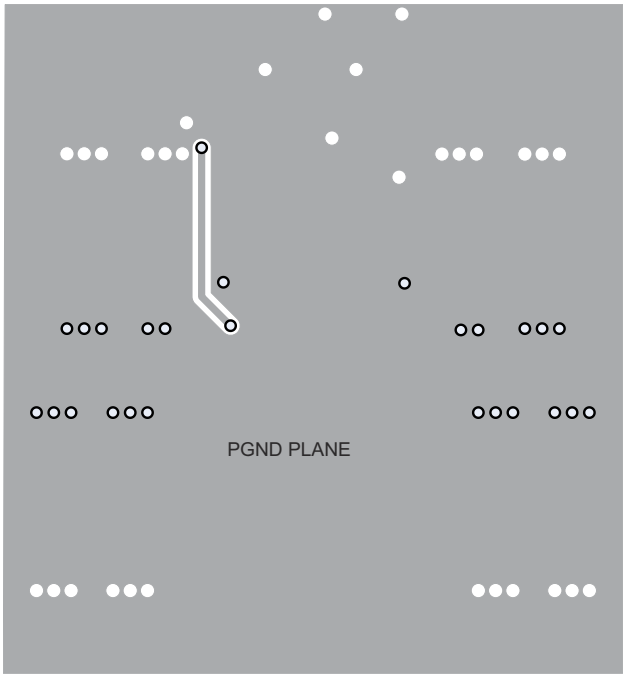


図 8-22. Bottom Layer Layout

9 Device and Documentation Support

9.1 Device Support

9.1.1 サード・パーティ製品に関する免責事項

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9.1.2 Development Support

- *TPS568215EVM-762 8-A, SWIFT™ Regulator Evaluation Module User's Guide*

9.2 ドキュメントの更新通知を受け取る方法

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ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

9.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS568215RNNR	ACTIVE	VQFN-HR	RNN	18	3000	RoHS & Green	Call TI | NIPDAU	Level-2-260C-1 YEAR	-40 to 125	568215	Samples
TPS568215RNNT	ACTIVE	VQFN-HR	RNN	18	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	568215	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

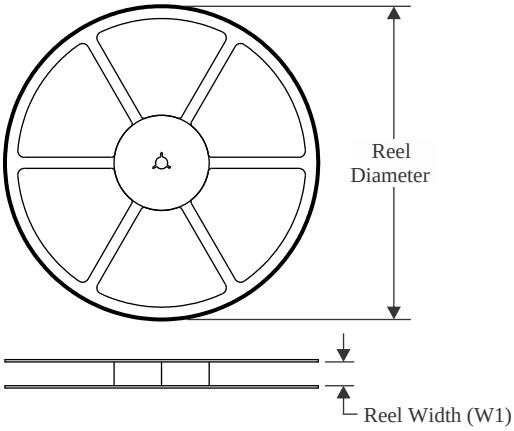
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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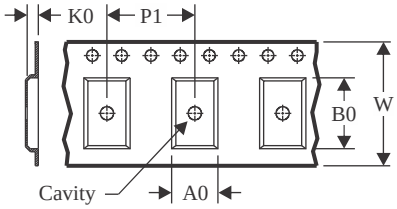
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

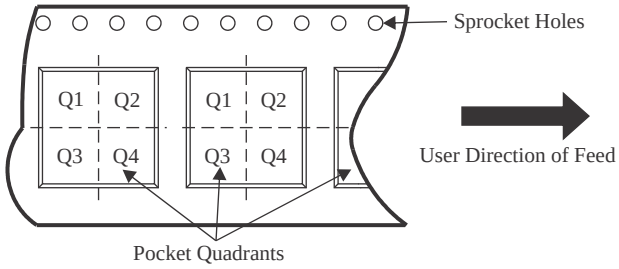


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

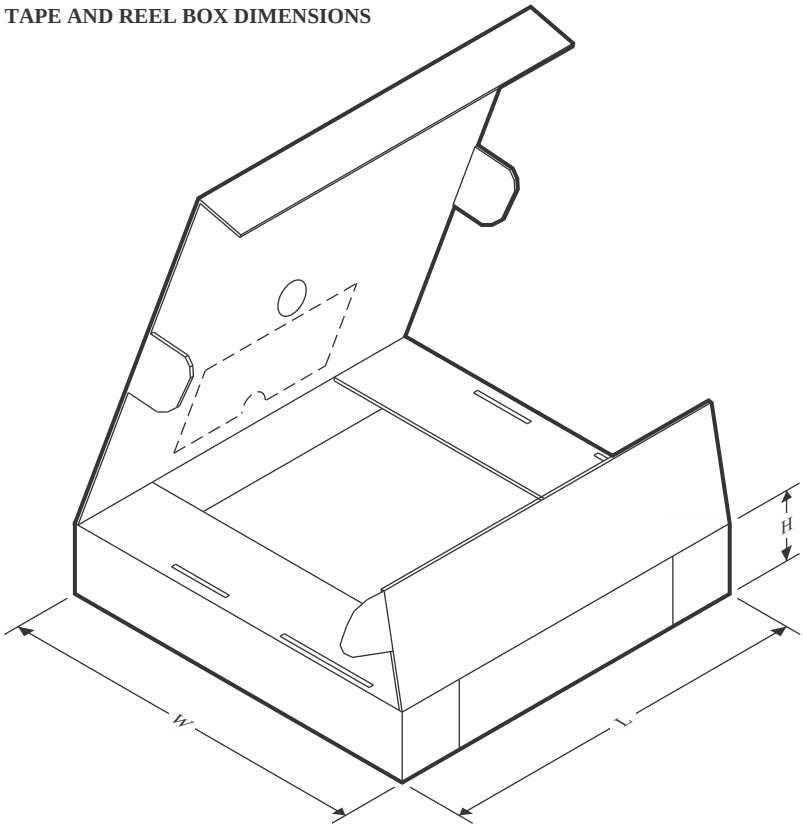
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS568215RNNR	VQFN-HR	RNN	18	3000	330.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2
TPS568215RNNT	VQFN-HR	RNN	18	250	180.0	12.4	3.75	3.75	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

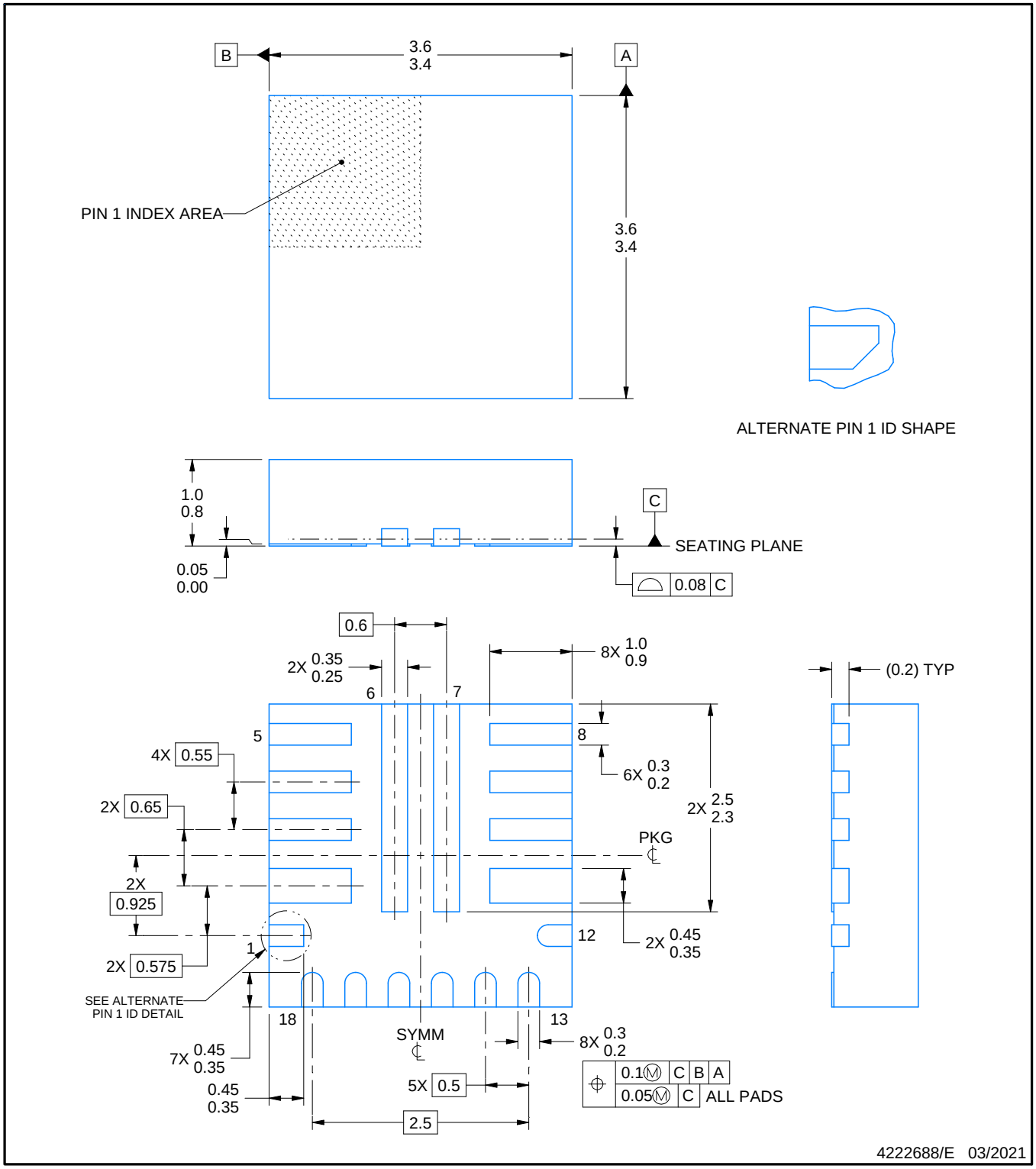
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS568215RNNR	VQFN-HR	RNN	18	3000	346.0	346.0	33.0
TPS568215RNNT	VQFN-HR	RNN	18	250	210.0	185.0	35.0

PACKAGE OUTLINE

RNN0018A

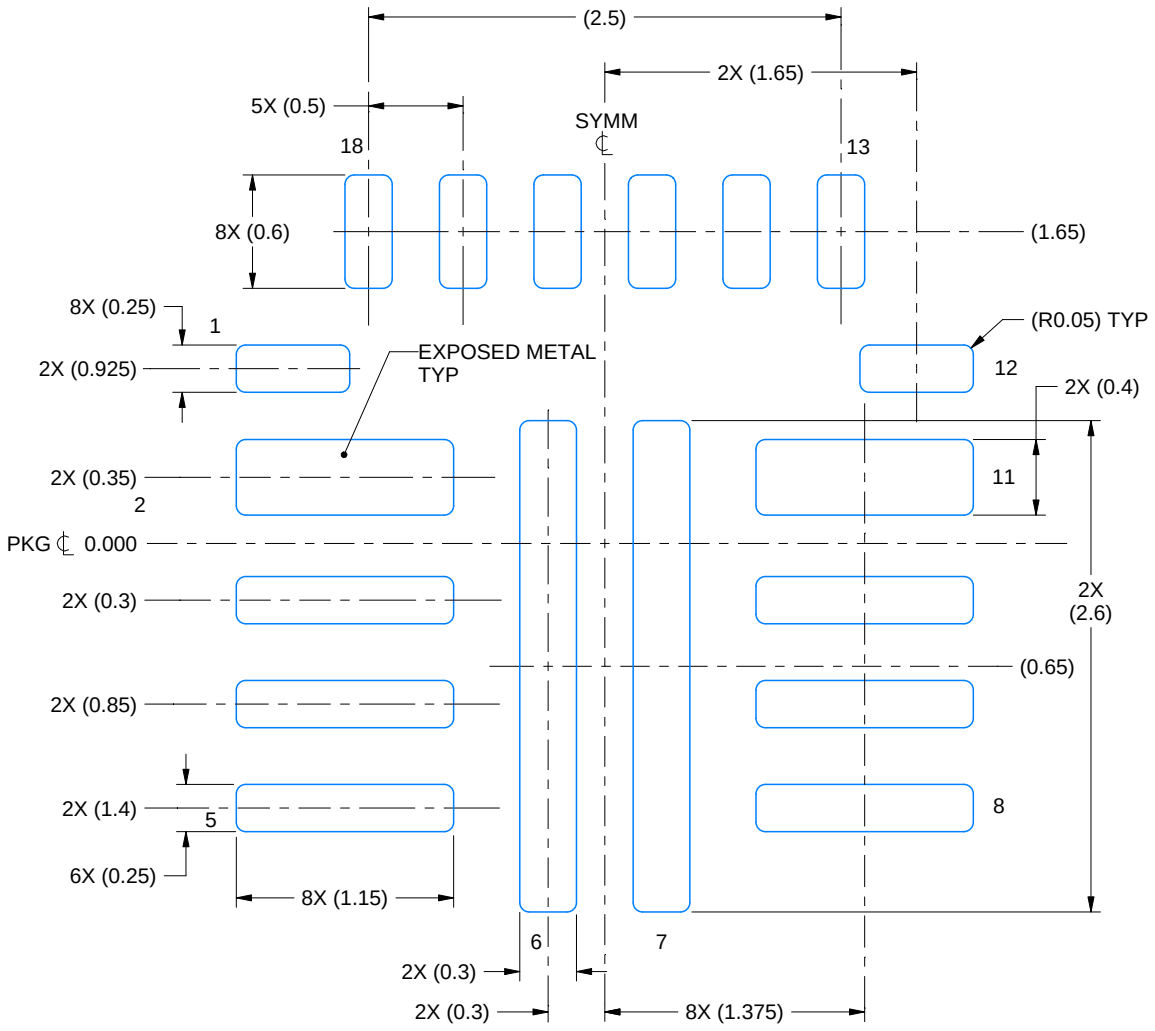
VQFN-HR - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD

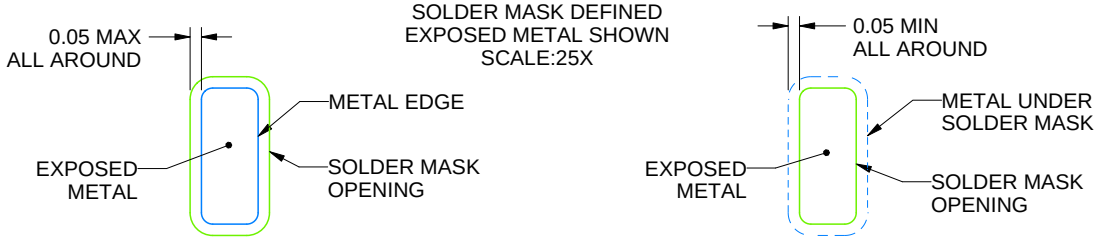


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.



LAND PATTERN EXAMPLE
SOLDER MASK DEFINED
EXPOSED METAL SHOWN
SCALE:25X



NON SOLDER MASK DEFINED (PREFERRED)

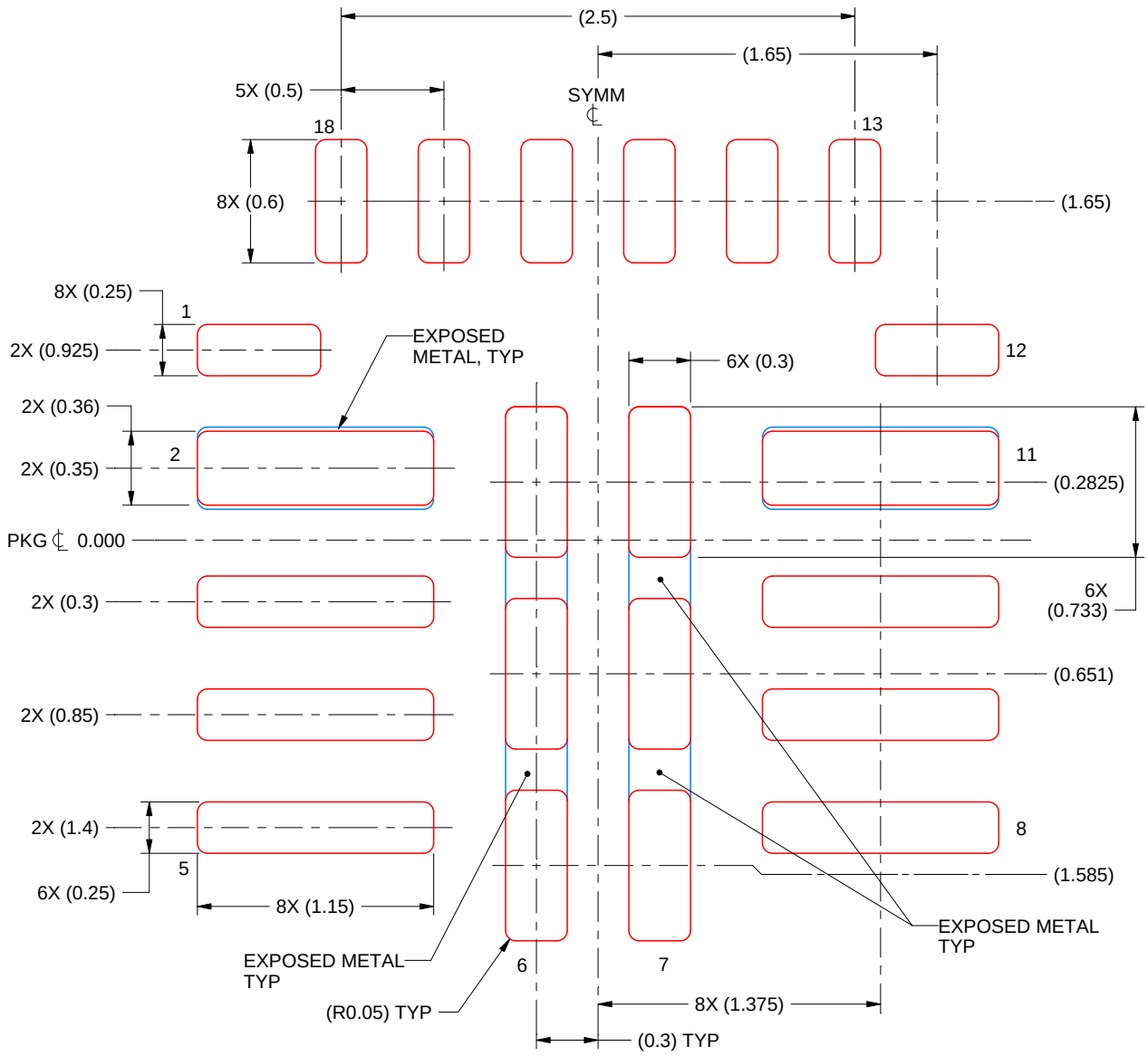
SOLDER MASK DEFINED

SOLDER MASK DETAILS

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NOTES: (continued)

3. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
4. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
PADS 6 & 7: 83% - PADS 2 & 11: 90%
SCALE:30X

4222688/E 03/2021

NOTES: (continued)

5. For alternate stencil design recommendations, see IPC-7525 or board assembly site preference.

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