TEXAS INSTRUMENTS
TPS61160, TPS61161
JAJS285E – NOVEMBER 2007 – REVISED JULY 2016

TPS6116x デジタルおよびPWM輝度制御搭載、2mm×2mm WSONパッケージ 白色LEDドライバ

1 特長

- 入力電圧範囲: 2.7V～18V
- LED断線過電圧保護: 26V (TPS61160)
- LED断線過電圧保護: 38V (TPS61161)
- 基準電圧200mV、精度±2%
- 柔軟なデジタルおよびPWM輝度制御
- ソフト·スタート内蔵
- 最大90%の効率

2 アプリケーション

- 携帯電話
- 携帯用メディア·プレーヤー
- UMD (Ultra Mobile Device)
- GPS受信機
- メディア・フォーム・ファクタ・ディスプレイ用の白色LEDバックライト

3 概要

TPS61160およびTPS61161は、40V定格のFETスイッチを内蔵しており、直列LEDを駆動できる昇圧型コンバータです。この昇圧型コンバータは600kHzの固定スイッチング周波数で動作するため、出力リップルの低減と変換効率の改善を実現し、小型の外付け部品を使用できます。

白色LEDの電流の初期値は、外付けのセンサ抵抗R_{SET}により設定され、フィードバック電圧は「*代表的なアプリケーション*」に示すように200mVにレギュレートされます。動作中のLED電流は、単線デジタル・インターフェイス(EasyScale™ プロトコル)を使用して、CTRLピンにより制御可能です。または、パルス幅変調(PWM)信号をCTRLピンに印加し、ディーティ・サイクルを使用して帰還基準電圧を決定することもできます。デジタルまたはPWMモードでは、TPS61160およびTPS61161はLED電流のバーストを行わないため、出力コンデンサから可聴域のノイズが発生しません。最大限の保護を可能にするため、デバイスにはLED断線過電圧保護機能が搭載されています。この機能は、LED断線条件が発生したときにTPS61160/TPS61161をディセーブルし、出力電圧がデバイスの絶対最大定格を超えることを防止します。

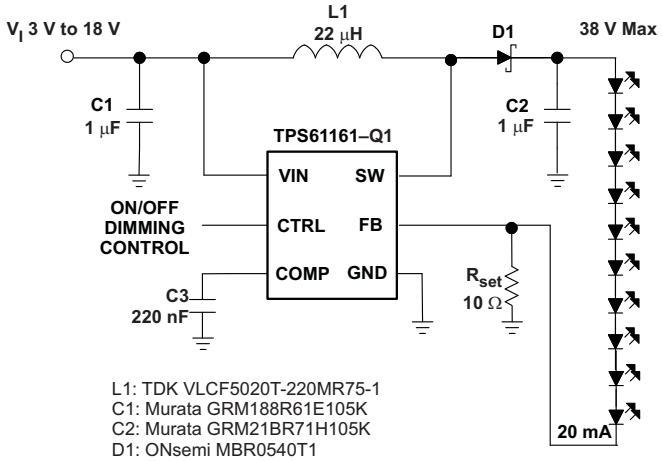
TPS61160およびTPS61161は、サーマル・パッドを搭載した省スペースの2mm×2mm WSONパッケージで利用可能です。

製品情報(1)

型番	パッケージ	LED断線過電圧保護
TPS61160	WSON (6)	TPS61160では26V (標準値)
TPS61161		TPS61161では38V (標準値)

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

代表的なアプリケーション



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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision D (June 2015) から **Revision E** に変更 — **Page**

- ドキュメント全体を通してパッケージ名を「SON」から「WSON」へ 変更 ... 1
- Deleted the "Duty" rows the *Recommended Operating Conditions*; added "t_{PWM_MIN}" row ... 4

Revision C (April 2012) から **Revision D** に変更 — **Page**

- パッケージ名をQFNからSONへ変更、「注文情報」表を削除(POAに重複情報あり)、「*ピン構成および機能*」セクション、「*ESD 定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウトの必須事項と禁止事項*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクションを 追加 ... 1
- Deleted Dissipation Ratings table - replaced by updated *Thermal Information*. ... 4
- Added paragraph re: not using EasyScale to change feedback voltage from 0 mV ... 13

Revision B (July 2011) から **Revision C** に変更 — **Page**

- Changed the Maximum duty cycle MIN value From: 90% To: 93% and the TYP value From: 93% To: 95% ... 5
- Changed position of V_I = 5 V and V_I = 3.6 V in Figure 3 ... 7

Revision A (September 2008) から **Revision B** に変更 — **Page**

- 特長の項目を「6 LEDでのLED断線過電圧保護: 26V (TPS61160)」から「LED断線過電圧保護: 26V (TPS61160)」へ 変更 ... 1
- 特長の項目を「10 LEDでのLED断線過電圧保護: 38V(TPS61161)」から「LED断線過電圧保護: 38V(TPS61161)」へ 変更 ... 1
- 代表的なアプリケーションの図に最大値38Vを追加 ... 1
- Changed the COMP and CTRL Description in the *Terminal Function Table* ... 3
- Changed text to clarify the "Open LED Protection" description. ... 11
- Changed Figure 13 ... 13

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- Changed the COMPENSATION CAPACITOR SELECTION section 20

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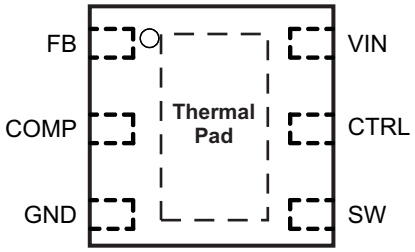
5 Pin Configuration and Functions

DRV Package
6-Pin WSON with Exposed Thermal Pad
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COMP	2	O	Output of the transconductance error amplifier. Connect an external capacitor to this pin to compensate the converter.
CTRL	5	I	Control pin of the boost converter. It is a multi-functional pin which can be used for enable control, PWM and digital dimming.
FB	1	I	Feedback pin for current. Connect the sense resistor from FB to GND.
GND	3	O	Ground
SW	4	I	This is the switching node of the device. Connect the inductor between the VIN and SW pin. This pin is also used to sense the output voltage for open LED protection
VIN	6	I	The input supply pin for the device. Connect VIN to a supply voltage between 2.7 V and 18 V.
Thermal Pad	—	—	Solder the thermal pad to the analog ground plane. If possible, use thermal via to connect to ground plane for ideal power dissipation.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
V_I	Supply voltages on VIN(2)	–0.3	20	V
	Voltages on CTRL(2)	–0.3	20	V
	Voltage on FB and COMP(2)	–0.3	3	V
	Voltage on SW(2)	–0.3	40	V
T_J	Operating junction temperature	40	150	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to network ground pin.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±4000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

		MIN	NOM	MAX	UNIT
V_I	Input voltage	2.7		18	V
V_O	Output voltage	V_{IN}		38	V
L	Inductor(1)	10		22	µH
f_{dim}	PWM dimming frequency	5		100	kHz
t_{PWM_MIN}	Minimum pulse width at PWM input		50		ns
C_{IN}	Input capacitor	1			µF
C_O	Output capacitor(1)	0.47		10	µF
T_A	Operating ambient temperature	–40		85	°C
T_J	Operating junction temperature	–40		125	°C

(1) These values are recommended values that have been successfully tested in several applications. Other values may be acceptable in other applications but should be fully tested by the user.

6.4 Thermal Information

THERMAL METRIC(1)		TPS61160, TPS61161 DRV (WSON) 6 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	96.1	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	89	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	65.9	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	66.3	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	40.8	°C/W

(1) For more information about traditional and new thermal metrics, see *Semiconductor and IC Package Thermal Metrics*.

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6.5 Electrical Characteristics

V_{IN} = 3.6 V, CTRL = V_{IN}, T_A = –40°C to +85°C, typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
V_I	Input voltage		2.7		18	V
I_Q	Operating quiescent current into VIN	Device PWM switching no load			1.8	mA
I_{SD}	Shutdown current	CRTL=GND, V_{IN} = 4.2 V			1	µA
UVLO	Undervoltage lockout threshold	V_{IN} falling		2.2	2.5	V
V_{hys}	Undervoltage lockout hysterisis			70		mV
ENABLE AND REFERENCE CONTROL						
$V_{(CTRLh)}$	CTRL logic high voltage	V_{IN} = 2.7 V to 18 V	1.2			V
$V_{(CTRLl)}$	CTRL logic low voltage	V_{IN} = 2.7 V to 18 V			0.4	V
$R_{(CTRL)}$	CTRL pull down resistor		400	800	1600	kΩ
VOLTAGE AND CURRENT CONTROL						
V_{REF}	Voltage feedback regulation voltage		196	200	204	mV
$V_{(REF_PWM)}$	Voltage feedback regulation voltage under brightness control	V_{FB} = 50 mV	47	50	53	mV
		V_{FB} = 20 mV	17	20	23	
I_{FB}	Voltage feedback input bias current	V_{FB} = 200 mV			2	µA
f_S	Oscillator frequency		500	600	700	kHz
D_{max}	Maximum duty cycle	V_{FB} = 100 mV, measured on the drive signal of the switching FET	93%	95%		
t_{min_on}	Minimum on pulse width			40		ns
I_{sink}	Comp pin sink current			100		µA
I_{source}	Comp pin source current			100		µA
G_{ea}	Error amplifier transconductance		240	320	400	µmho
R_{ea}	Error amplifier output resistance			6		MΩ
f_{ea}	Error amplifier crossover frequency	5 pF connected to COMP		500		kHz
POWER SWITCH						
$R_{DS(on)}$	N-channel MOSFET on-resistance	V_{IN} = 3.6 V		0.3	0.6	Ω
		V_{IN} = 3 V			0.7	
I_{LN_NFET}	N-channel leakage current	V_{SW} = 35 V, T_A = 25°C			1	µA

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Electrical Characteristics (continued)

V_{IN} = 3.6 V, CTRL = V_{IN}, T_A = –40°C to +85°C, typical values are at T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
OC and OLP						
I_{LIM}	N-Channel MOSFET current limit	D = D_{max}	0.56	0.7	0.84	A
I_{LIM_Start}	Start up current limit	D = D_{max}		0.4		A
t_{Half_LIM}	Time step for half current limit			5		ms
V_{ovp}	Open LED protection threshold	Measured on the SW pin, TPS61160 TPS61161	25 37	26 38	27 39	V
$V_{(FB_OVP)}$	Open LED protection threshold on FB	Measured on the FB pin, percentage of V_{REF} V_{REF}= 200 mV and 20 mV		50%		
V_{ACKNL}	Acknowledge output voltage low	Open drain, R_{pullup} =15 kΩ to V_{IN}			0.4	V
THERMAL SHUTDOWN						
$T_{shutdown}$	Thermal shutdown threshold			160		°C
$T_{hysteresis}$	Thermal shutdown threshold hysteresis			15		°C

6.6 Timing Requirements

		MIN	NOM	MAX	UNIT
OC and OLP					
t_{REF}	V_{REF} filter time constant		180		µs
t_{step}	V_{REF} ramp up time		213		µs
EasyScale					
$t_{valACKN}$	Acknowledge valid time(1)			2	µs
t_{ACKN}	Duration of acknowledge condition(1)			512	µs
t_{off}	CTRL pulse width to shutdown, CTRL high to low	2.5			ms
t_{es_det}	Easy Scale detection time(2)	260			µs
t_{es_delay}	EasyScale detection delay, Measured from CTRL high	100			µs
t_{es_win}	EasyScale detection window time	1			ms
t_{START}	Start time of program stream	2			µs
t_{EOS}	End time of program stream	2		360	µs
t_{H_LB}	High time low bit, logic 0	2		180	µs
t_{L_LB}	Low time low bit, logic 0	2 × t_{H_LB}		360	µs
t_{H_HB}	High time high bit, logic 1	2 × t_{L_HB}		360	µs
t_{L_HB}	Low time high bit, logic 1	2		180	µs

(1) Acknowledge condition active 0, this condition will only be applied in case the RFA bit is set. Open drain output, line needs to be pulled high by the host with resistor load.
(2) To select EasyScale mode, the CTRL pin has to be low for more than t_{es_det} during t_{es_win}.

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6.7 Typical Characteristics

6.7.1 Table Of Graphs

		FIGURE
Efficiency TPS61160/1	V_{IN} = 3.6 V; 4, 6, 8, 10 LEDs; L = 22 µH	Figure 1
Efficiency TPS61160		Figure 2
Efficiency TPS61161		Figure 3
Current limit	T_A = 25°C	Figure 4
Current limit		Figure 5
EasyScale step		Figure 6
PWM dimming linearity	V_{IN} = 3.6 V; PWM Freq = 10 kHz and 40 kHz	Figure 6
Output ripple at PWM dimming	8 LEDs; V_{IN} = 3.6 V; I_{LOAD} = 20 mA; PWM Freq = 10 kHz	Figure 8
Switching waveform	8 LEDs; V_{IN} = 3.6 V; I_{LOAD} = 20 mA; L = 22 µH	Figure 9
Start-up	8 LEDs; V_{IN} = 3.6 V; I_{LOAD} = 20 mA; L =22 µH	Figure 10
Open LED protection	8 LEDs; V_{IN} = 3.6 V; I_{LOAD} = 20 mA; L = 22 µH	Figure 11

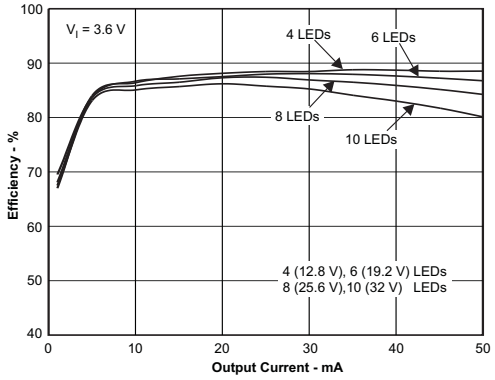

Figure 1. Efficiency vs Output Current

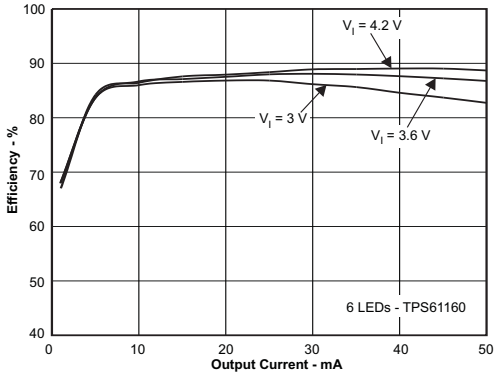

Figure 2. Efficiency vs Output Current

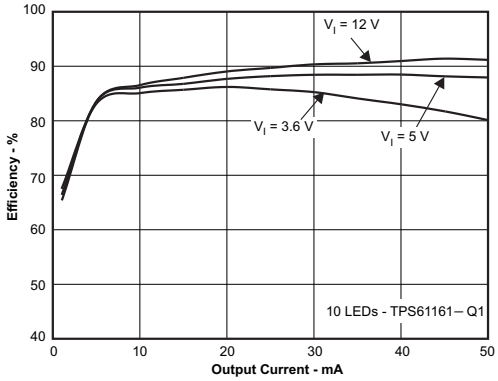

Figure 3. Efficiency vs Output Current

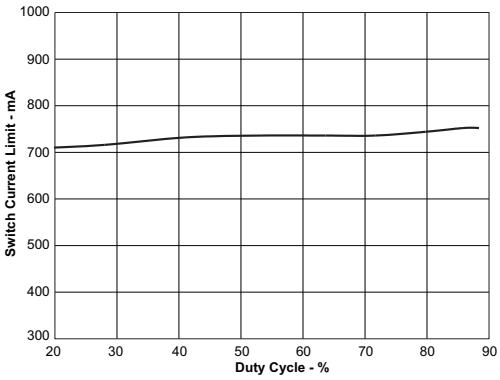

Figure 4. Switch Current Limit vs Duty Cycle

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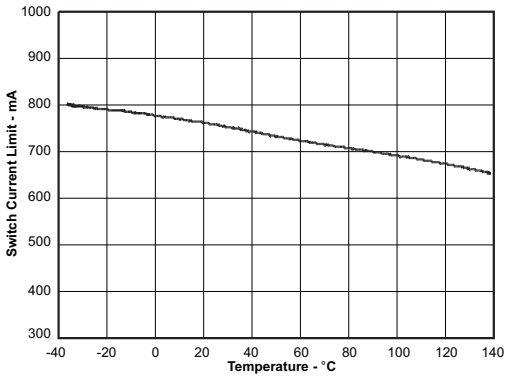

Figure 5. Switch Current Limit vs Temperature

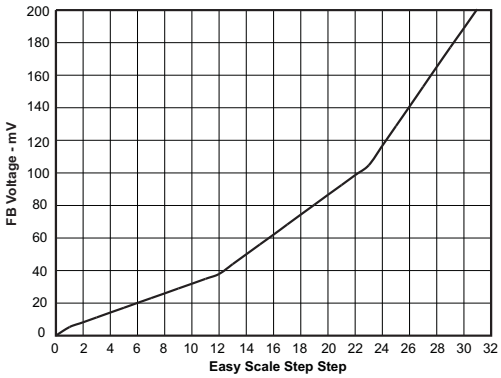

Figure 6. FB Voltage vs EasyScale Step

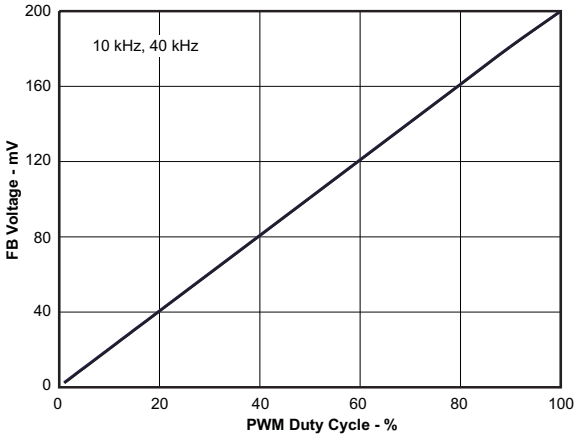

Figure 7. FB Voltage vs PWM Duty Cycle

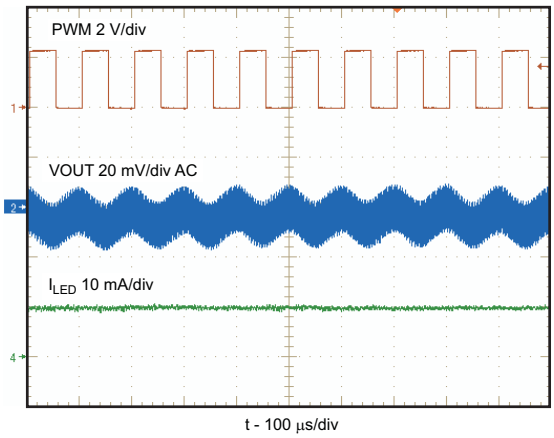

Figure 8. Output Ripple At PWM Dimming

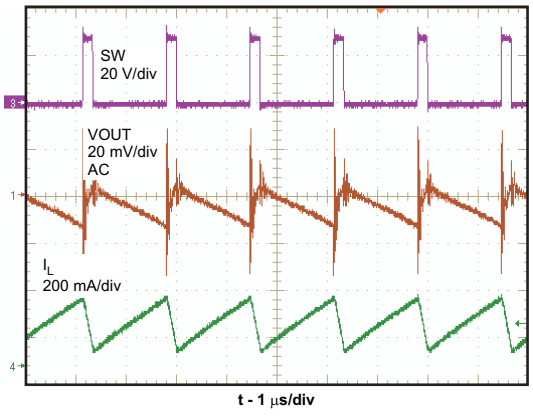

Figure 9. Switching Waveform

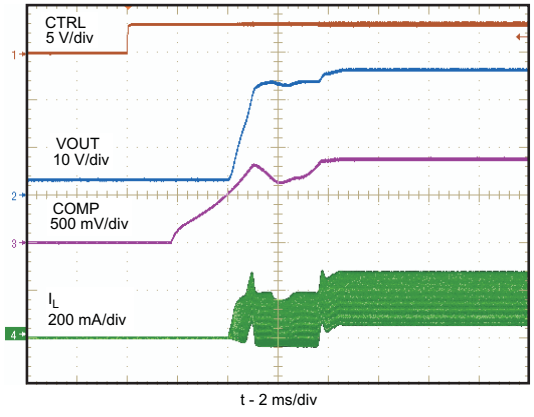

Figure 10. Start-Up

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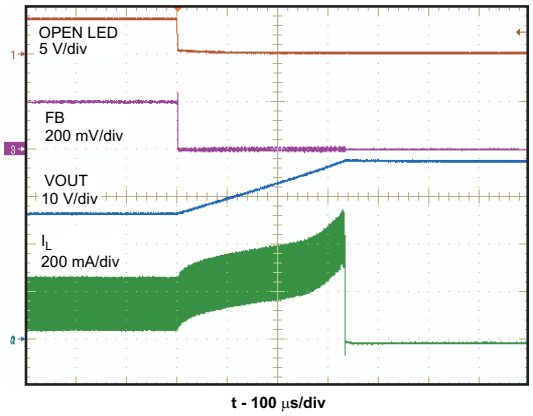

Figure 11. Open LED Protection

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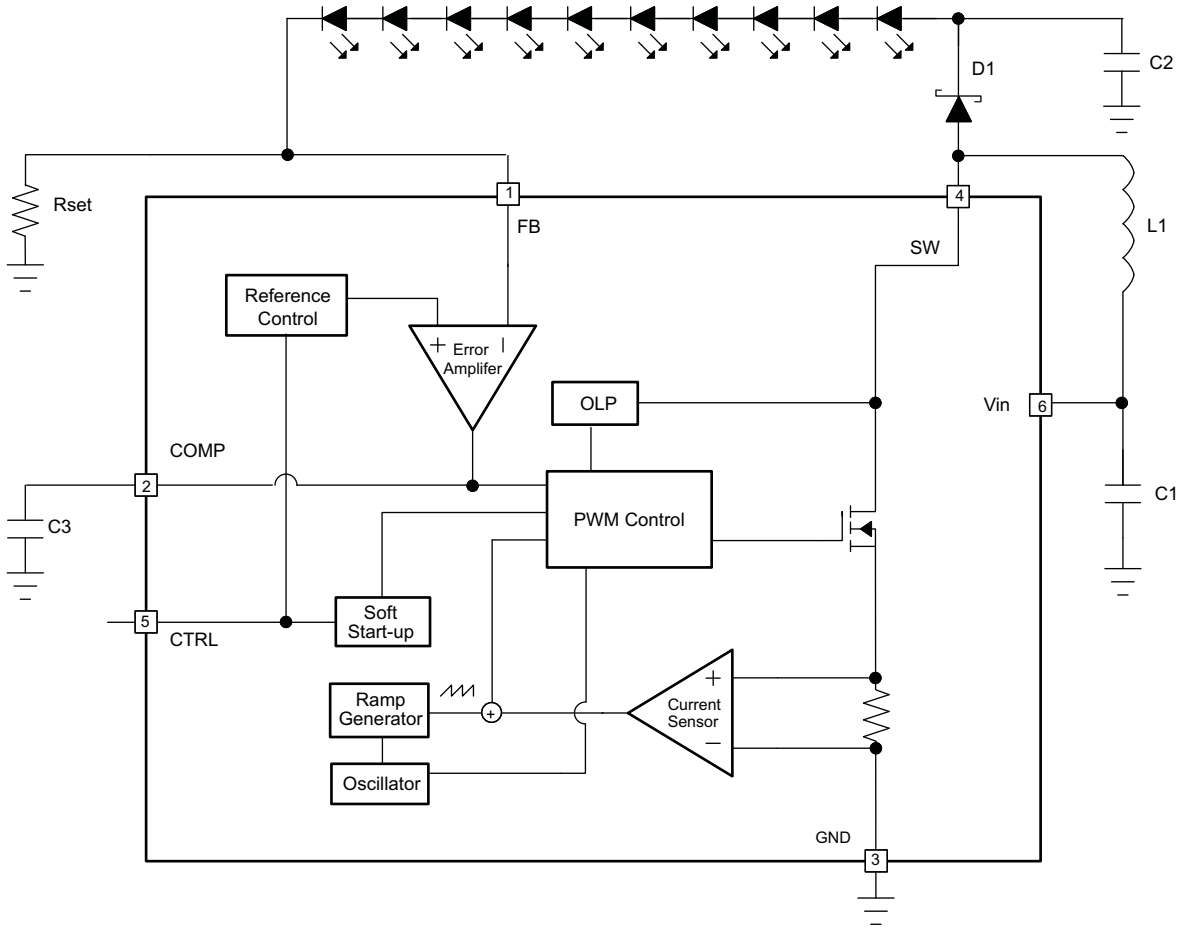
7 Detailed Description

7.1 Overview

The TPS61160 and TPS61161 are high-efficiency, high-output voltage boost converters in a small package size. These devices are ideal for driving white LED in series. The serial LED connection provides even illumination by sourcing the same output current through all LEDs, eliminating the need for expensive factory calibration. Each device integrate a 40-V, 0.7-A switch FET and operatea in pulse width modulation (PWM) with 600-kHz fixed switching frequency. For operation see the block diagram. The duty cycle of the converter is set by the error amplifier output and the current signal applied to the PWM control comparator. The control architecture is based on traditional current-mode control; therefore, a slope compensation is added to the current signal to allow stable operation for duty cycles larger than 50%. The feedback loop regulates the FB pin to a low reference voltage (200 mV typical), reducing the power dissipation in the current sense resistor.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Soft Start-Up

Soft-start circuitry is integrated into the device to avoid a high inrush current during start-up. After the device is enabled, the voltage at FB pin ramps up to the reference voltage in 32 steps with each step taking 213 μs. This ensures that the output voltage rises slowly to reduce the input current. Additionally, for the first 5 msec after the COMP voltage ramps, the current limit of the switch is set to half of the normal current limit spec. During this period, the input current is kept below 400 mA (typical). See the start-up waveform of a typical example, Figure 10.

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Feature Description (continued)

7.3.2 Open LED Protection

Open LED protection circuitry prevents device damage as the result of white LED disconnection. The TPS61160 and TPS61161 monitor the voltage at the SW pin and FB pin during each switching cycle. The circuitry turns off the switch FET and shuts down the device when both of the following conditions persist for 8 switching clock cycles:

1. The SW voltage exceeds the V_{OVP} threshold; and
2. The FB voltage is less than half of regulation voltage.

As a result, the output voltage falls to the level of the input supply. The device remains in shutdown mode until it is enabled by toggling the CTRL pin logic. To allow the use of inexpensive low-voltage output capacitor, the TPS61160/1 has different open lamp protection thresholds. The threshold is set at 26 V for the TPS61160 and 38 V for the TPS61161. Select the appropriate device so that the product of the number of external LEDs and each LED's maximum forward voltage plus the 200 mV reference voltage does not exceed the minimum OVP threshold or ($n_{LEDS} \times V_{LED(MAX)}$) + 200 mV ≤ $V_{OVP(MIN)}$.

7.3.3 Current Program

The FB voltage is regulated by a low 0.2-V reference voltage. The LED current is programmed externally using a current-sense resistor in series with the LED string. The value of the R_{SET} is calculated using Equation 1:

$$I_{LED} = \frac{V_{FB}}{R_{SET}} \quad (1)$$

where

- I_{LED} = output current of LEDs
- V_{FB} = regulated voltage of FB
- R_{SET} = current sense resistor

The output current tolerance depends on the FB accuracy and the current sensor resistor accuracy.

7.3.4 LED Brightness Dimming Mode Selection

The CTRL pin is used for the control input for both dimming modes, PWM dimming and one-wire dimming. The dimming mode for the TPS61160 or TPS61161 is selected each time the device is enabled. The default dimming mode is PWM dimming. To enter the one-wire mode, the following digital pattern on the CTRL pin must be recognized by the device every time the device starts from the shutdown mode.

1. Pull CTRL pin high to enable the TPS61160 or TPS61161 and to start the one-wire detection window.
2. After the EasyScale detection delay (t_{es_delay}, 100 μs) expires, drive CTRL low for more than the EasyScale detection time (t_{es_detect}, 260 μs).
3. The CTRL pin has to be low for more than EasyScale detection time before the EasyScale detection window (t_{es_win}, 1 msec) expires. EasyScale detection window starts from the first CTRL pin low to high transition.

The device immediately enters the one-wire mode once the above three conditions are met. the EasyScale communication can start before the detection window expires. Once the dimming mode is programmed, it can not be changed without another start-up. This means the device needs to be shutdown by pulling the CTRL low for 2.5 ms and restarts. See Figure 12 for a graphical explanation.

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Feature Description (continued)

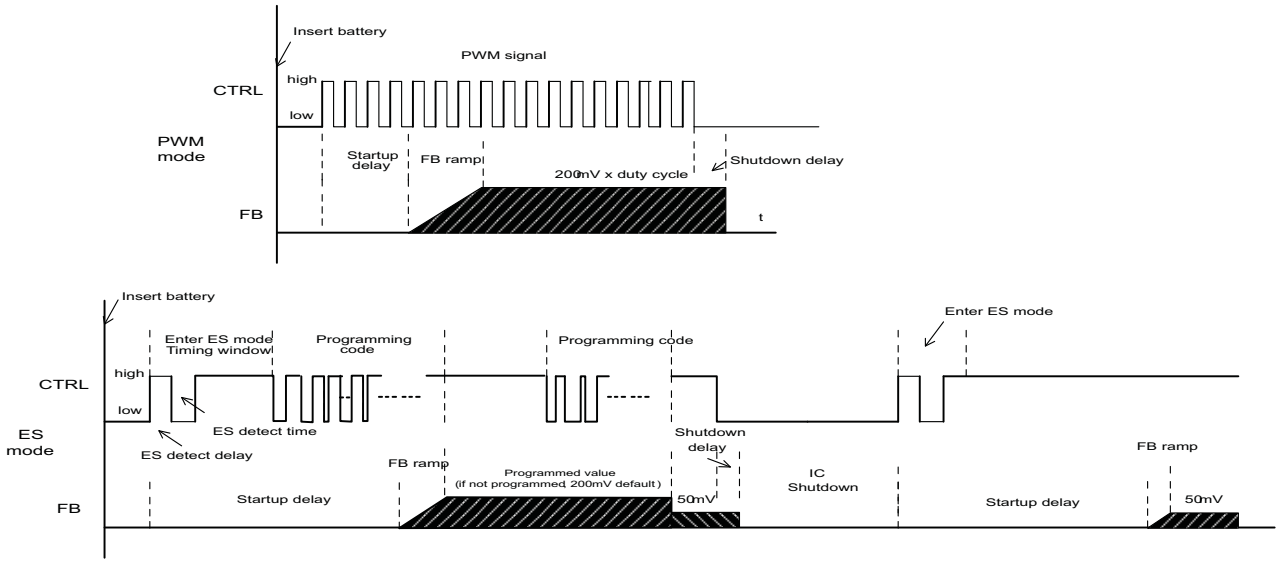

Figure 12. Dimming Mode Detection and Soft Start PWM Brightness Dimming

7.3.5 Undervoltage Lockout

An undervoltage lockout prevents operation of the device at input voltages below typical 2.2 V. When the input voltage is below the undervoltage threshold, the device is shutdown and the internal switch FET is turned off. If the input voltage rises by undervoltage lockout hysteresis, the device restarts.

7.3.6 Thermal Shutdown

An internal thermal shutdown turns off the device when the typical junction temperature of 160°C is exceeded. The device is released from shutdown automatically when the junction temperature decreases by 15°C.

7.4 Device Functional Modes

7.4.1 Shutdown

The TPS61160 or TPS61161 enters shutdown mode when the CTRL voltage is logic low for more than 2.5 ms. During shutdown, the input supply current for the device is less than 1 μA (maximum). Although the internal FET does not switch in shutdown, there is still a DC current path between the input and the LEDs through the inductor and Schottky diode. The minimum forward voltage of the LED array must exceed the maximum input voltage to ensure that the LEDs remain off in shutdown. However, in the typical application with two or more LEDs, the forward voltage is large enough to reverse bias the Schottky and keep leakage current low.

7.4.2 PWM Brightness Dimming

When the CTRL pin is constantly high, the FB voltage is regulated to 200 mV typically. However, the CTRL pin allows a PWM signal to reduce this regulation voltage; therefore, it achieves LED brightness dimming. The relationship between the duty cycle and FB voltage is given by Equation 2.

$$V_{FB} = \text{Duty} \times 200\ \text{mV} \quad (2)$$

where

- Duty = duty cycle of the PWM signal
- 200 mV = internal reference voltage

Device Functional Modes (continued)

As shown in Figure 13, the device chops up the internal 200-mV reference voltage at the duty cycle of the PWM signal. The pulse signal is then filtered by an internal low pass filter. The output of the filter is connected to the error amplifier as the reference voltage for the FB pin regulation. Therefore, although a PWM signal is used for brightness dimming, only the WLED DC current is modulated, which is often referred as analog dimming. This eliminates the audible noise which often occurs when the LED current is pulsed in replica of the frequency and duty cycle of PWM control. Unlike other scheme which filters the PWM signal for analog dimming, TPS61160, TPS61161 regulation voltage is independent of the PWM logic voltage level which often has large variations.

For optimum performance, use the PWM dimming frequency in the range of 5 kHz to 100 kHz. The requirement of minimum dimming frequency comes from the EasyScale detection delay and detection time specification in the dimming mode selection. Since the CTRL pin is logic only pin, adding an external RC filter applied to the pin does not work.

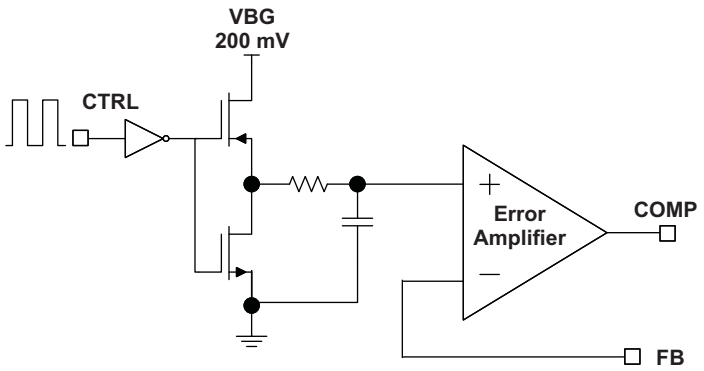

Figure 13. Block Diagram of Programmable FB Voltage Using PWM Signal

To use lower PWM dimming, add an external RC network connected to the FB pin as shown in Figure 19.

7.4.3 Digital One-Wire Brightness Dimming

The CTRL pin features a simple digital interface to allow digital brightness control. The digital dimming can save the processor power and battery life as it does not require a PWM signal all the time, and the processor can enter idle mode if available.

The TPS61160 or TPS61161 adopts the EasyScale protocol for the digital dimming, which can program the FB voltage to any of the 32 steps with single command. The step increment increases with the voltage to produce pseudo logarithmic curve for the brightness step. See the Table 1 for the FB pin voltage steps. The default step is full scale when the device is first enabled (V_{FB} = 200 mV). The programmed reference voltage is stored in an internal register. A power reset clears the register value and reset it to default.

Do not use EasyScale to change the feedback voltage from 0 mV, effectively disabling the device, to any other voltage. One alternative is to start with V_{FB} = 10 mV and go to a higher voltage. Another alternative is to disable the device by taking the CTRL pin low for 2.5 ms and then re-enter EasyScale to force a soft start from V_{FB} = 0 mV to the default 200 mV.

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Device Functional Modes (continued)

7.4.4 External PWM Dimming

For assistance in selecting the proper values for R_{SET}, R1-R3, RFLTR, CFLTR and D2 for the specific application, refer to *How to Use Analog Dimming With the TPS6116x* (SLVA471) and/or *Design Tool for Analog Dimming Using a PWM Signal* (SLVC366). Also see *Choosing Component Values*.

7.5 Programming

7.5.1 EasyScale: One-Wire Digital Dimming

EasyScale is a simple but flexible one pin interface to configure the FB voltage. The interface is based on a master-slave structure, where the master is typically a microcontroller or application processor. Figure 14 and Table 2 give an overview of the protocol. The protocol consists of a device specific address byte and a data byte. The device specific address byte is fixed to 72 hex. The data byte consists of five bits for information, two address bits, and the RFA bit. The RFA bit set to high indicates the *Request for Acknowledge* condition. The Acknowledge condition is only applied if the protocol was received correctly. The advantage of EasyScale compared with other one-pin interfaces is that its bit detection is in a large extent independent from the bit transmission rate. It can automatically detect bit rates from 1.7 kBit/sec and up to 160 kBit/sec.

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Table 1. Selectable FB Voltages(1)

	FB voltage (mV)	D4	D3	D2	D1	D0
0	0	0	0	0	0	0
1	5	0	0	0	0	1
2	8	0	0	0	1	0
3	11	0	0	0	1	1
4	14	0	0	1	0	0
5	17	0	0	1	0	1
6	20	0	0	1	1	0
7	23	0	0	1	1	1
8	26	0	1	0	0	0
9	29	0	1	0	0	1
10	32	0	1	0	1	0
11	35	0	1	0	1	1
12	38	0	1	1	0	0
13	44	0	1	1	0	1
14	50	0	1	1	1	0
15	56	0	1	1	1	1
16	62	1	0	0	0	0
17	68	1	0	0	0	1
18	74	1	0	0	1	0
19	80	1	0	0	1	1
20	86	1	0	1	0	0
21	92	1	0	1	0	1
22	98	1	0	1	1	0
23	104	1	0	1	1	1
24	116	1	1	0	0	0
25	128	1	1	0	0	1
26	140	1	1	0	1	0
27	152	1	1	0	1	1
28	164	1	1	1	0	0
29	176	1	1	1	0	1
30	188	1	1	1	1	0
31	200	1	1	1	1	1

(1) See *Digital One-Wire Brightness Dimming*.

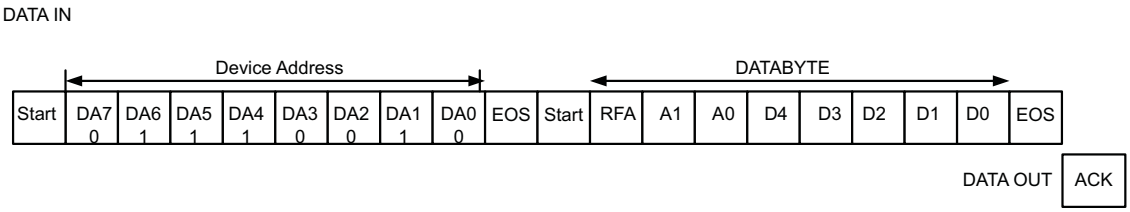

Figure 14. EasyScale Protocol Overview

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Table 2. EasyScale Bit Descriptions

BYTE	BIT NUMBER	NAME	TRANSMISSION DIRECTION	DESCRIPTION
Device Address Byte 72 hex	7	DA7	IN	0 MSB device address
	6	DA6		1
	5	DA5		1
	4	DA4		1
	3	DA3		0
	2	DA2		0
	1	DA1		1
	0	DA0		0 LSB device address
Data byte	7 (MSB)	RFA	IN	Request for acknowledge. If high, acknowledge is applied by device
	6	A1		0 Address bit 1
	5	A0		0 Address bit 0
	4	D4		Data bit 4
	3	D3		Data bit 3
	2	D2		Data bit 2
	1	D1		Data bit 1
	0 (LSB)	D0		Data bit 0
		ACK	OUT	Acknowledge condition active 0, this condition will only be applied in case RFA bit is set. Open drain output, Line needs to be pulled high by the host with a pullup resistor. This feature can only be used if the master has an open drain output stage. In case of a push pull output stage Acknowledge condition may not be requested!

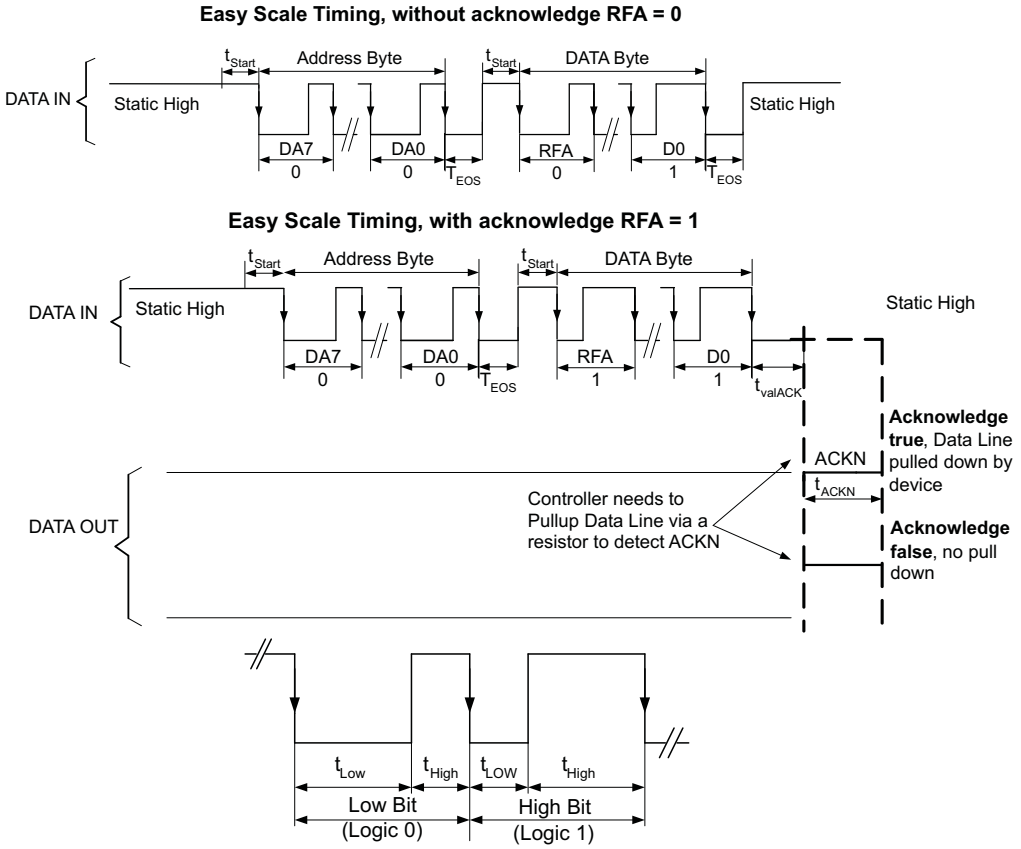

Figure 15. EasyScale Bit Coding

All bits are transmitted MSB first and LSB last. Figure 15 shows the protocol without acknowledge request (Bit RFA = 0) as well as the with acknowledge (Bit RFA = 1) request. Prior to both bytes, device address byte and data byte, a start condition must be applied. For this, the CTRL pin must be pulled high for at least t_{start} (2 µs) before the bit transmission starts with the falling edge. If the CTRL pin is already at high level, no start condition is needed prior to the device address byte. The transmission of each byte is closed with an End-of-Stream condition for at least t_{EOS} (2 µs).

The bit detection is based on a Logic Detection scheme, where the criterion is the relation between t_{LOW} and t_{HIGH}. It can be simplified to:

High Bit: $t_{HIGH} > t_{LOW}$, but with t_{HIGH} at least 2 × t_{LOW}, see Figure 15.

Low Bit: $t_{HIGH} < t_{LOW}$, but with t_{LOW} at least 2 × t_{HIGH}, see Figure 15.

The bit detection starts with a falling edge on the CTRL pin and ends with the next falling edge. Depending on the relation between t_{HIGH} and t_{LOW}, the logic 0 or 1 is detected.

The acknowledge condition is only applied if:

- Acknowledge is requested by a set RFA bit.
- The transmitted device address matches with the device address of the device.
- 16 bits is received correctly.

If the device turns on the internal ACKN-MOSFET and pulls the CTRL pin low for the time t_{ACKN}, which is 512 µs maximum then the Acknowledge condition is valid after an internal delay time t_{valACK}. This means that the internal ACKN-MOSFET is turned on after t_{valACK}, when the last falling edge of the protocol was detected. The master controller keeps the line low in this period. The master device can detect the acknowledge condition with its input by releasing the CTRL pin after t_{valACK} and read back a logic 0. The CTRL pin can be used again after the acknowledge condition ends.

Note that the acknowledge condition may only be requested in case the master device has an open drain output. For a push-pull output stage, the use a series resistor in the CRTL line to limit the current to 500 µA is recommended to for such cases as:

- an accidentally requested acknowledge, or
- to protect the internal ACKN-MOSFET.

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8 Application and Implementation Information

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS61160 and TPS61161 provide a complete high-performance LED lighting solution for mobile devices supporting a single string of 6 (TPS61160) or 10 (TPS61161) white LEDs.

8.2 Typical Applications

8.2.1 Typical Application of TPS61161

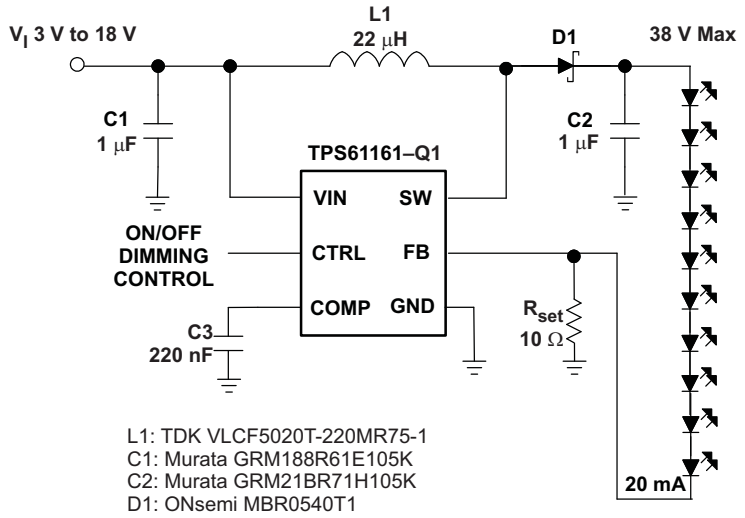

Figure 16. Typical Application of TPS61161

8.2.1.1 Design Requirements

Example requirements for white-LED-driver applications:

Table 3. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Inductor	22 µH
Minimum input voltage	3 V
Number of series LED	10
LED maximum forward voltage (Vf)	3.2 V
Schottky diode forward voltage (Vf)	0.2 V
Efficiency (η)	85%
Switching frequency (SW)	600 kHz

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Applying Equation 3 and Equation 4, when V_{IN} is 3 V, 10 LEDs output equivalent to V_{OUT} of 32.2 V, the inductor is 22 μH, the Schottky forward voltage is 0.2 V, the maximum output current is 47 mA in typical condition.

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 Maximum Output Current

The overcurrent limit in a boost converter limits the maximum input current and thus maximum input power for a given input voltage. Maximum output power is less than maximum input power due to power conversion losses. Therefore, the current limit setting, input voltage, output voltage and efficiency can all change maximum current output. The current limit clamps the peak inductor current; therefore, the ripple has to be subtracted to derive maximum DC current. The ripple current is a function of switching frequency, inductor value and duty cycle. Equation 3 and Equation 4 take into account of all the above factors for maximum output current calculation.

$$I_P = \frac{1}{\left[L \times F_S \times \left(\frac{1}{V_{OUT} + V_F + V_{IN}} + \frac{1}{V_{IN}}\right)\right]}$$

where

- I_p = inductor peak-to-peak ripple
- L = inductor value
- V_f = Schottky diode forward voltage
- Fs = switching frequency
- V_{out} = output voltage of the boost converter. It is equal to the sum of VFB and the voltage drop across LEDs.

(3)

$$I_{OUT_MAX} = \frac{V_{IN} \times \left(I_{LIM} - \frac{I_P}{2}\right) \times \eta}{V_{OUT}}$$

where

- I_{out_max} = maximum output current of the boost converter
- I_{lim} = overcurrent limit
- η = efficiency

(4)

For instance, when V_{IN} is 3 V, 8 LEDs output equivalent to V_{OUT} of 26 V, the inductor is 22 μH, the Schottky forward voltage is 0.2 V; and then the maximum output current is 65 mA in typical condition. When V_{IN} is 5 V, 10 LEDs output equivalent to V_{OUT} of 32 V, the inductor is 22 μH, the Schottky forward voltage is 0.2 V; and then the maximum output current is 85 mA in typical condition.

8.2.1.2.2 Inductor Selection

The selection of the inductor affects steady state operation as well as transient behavior and loop stability. These factors make it the most important component in power regulator design. There are three important inductor specifications, inductor value, DC resistance and saturation current. Considering inductor value alone is not enough.

The inductor value determines the inductor ripple current. Choose an inductor that can handle the necessary peak current without saturating, according to half of the peak-to-peak ripple current given by Equation 3, pause the inductor DC current given by:

$$I_{IN_DC} = \frac{V_{OUT} \times I_{OUT}}{V_{IN} \times \eta}$$

(5)

Inductor values can have ±20% tolerance with no current bias. When the inductor current approaches saturation level, its inductance can decrease 20% to 35% from the 0A value depending on how the inductor vendor defines saturation current. Using an inductor with a smaller inductance value forces discontinuous PWM when the inductor current ramps down to zero before the end of each switching cycle. This reduces the boost converter's maximum output current, causes large input voltage ripple and reduces efficiency. Large inductance value

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provides much more output current and higher conversion efficiency. For these reasons, a 10-μH to 22-μH inductor value range is recommended. A 22-μH inductor optimized the efficiency for most application while maintaining low inductor peak-to-peak ripple. Table 4 lists the recommended inductor for the TPS61160 or TPS61161. When recommending inductor value, the factory has considered –40% and 20% tolerance from its nominal value.

The TPS61160 and TPS61161 have built-in slope compensation to avoid sub-harmonic oscillation associated with current mode control. If the inductor value is lower than 10 μH, the slope compensation may not be adequate, and the loop can be unstable. Therefore, customers need to verify the inductor in their application if it is different from the recommended values.

Table 4. Recommended Inductors for TPS61160 and TPS61161

PART NUMBER	L (μH)	DCR MAX (Ω)	SATURATION CURRENT (mA)	SIZE (L × W × H mm)	VENDOR
LQH3NPN100NM0	10	0.3	750	3 ×3 ×1.5	Murata
VLCF5020T-220MR75-1	22	0.4	750	5 ×5 × 2.0	TDK
CDH3809/SLD	10	0.3	570	4 × 4 × 1.0	Sumida
A997AS-220M	22	0.4	510	4 × 4 × 1.8	TOKO

8.2.1.2.3 Schottky Diode Selection

The high switching frequency of the TPS61160, TPS61161 demands a high-speed rectification for optimum efficiency. Ensure that the diode average and peak current rating exceeds the average output current and peak inductor current. In addition, the diode's reverse breakdown voltage must exceed the open LED protection voltage. The ONSemi MBR0540 and the ZETEX ZHCS400 are recommended for TPS61160 and TPS61161.

8.2.1.2.4 Compensation Capacitor Selection

The compensation capacitor C3 (see the *Functional Block Diagram*), connected from COMP pin to GND, is used to stabilize the feedback loop of the TPS61160, TPS61161. A 220-nF ceramic capacitor for C3 is suitable for most applications.

8.2.1.2.5 Input and Output Capacitor Selection

The output capacitor is mainly selected to meet the requirements for the output ripple and loop stability. This ripple voltage is related to the capacitor's capacitance and its equivalent series resistance (ESR). Assuming a capacitor with zero ESR, the minimum capacitance needed for a given ripple can be calculated by:

$$C_{OUT} = \frac{(V_{OUT} - V_{IN})I_{OUT}}{V_{OUT} \times F_S \times V_{RIPPLE}}$$

where

- V_{ripple} = peak-to-peak output ripple (6)

The additional output ripple component caused by ESR is calculated using:

$$V_{RIPPLE_ESR} = I_{OUT} \times R_{ESR} \quad (7)$$

Due to its low ESR, V_{ripple_ESR} can be neglected for ceramic capacitors, but must be considered if tantalum or electrolytic capacitors are used.

Care must be taken when evaluating a ceramic capacitor's derating under DC bias, aging and AC signal. For example, larger form factor capacitors (in 1206 size) have a resonant frequencies in the range of the switching frequency. So the effective capacitance is significantly lower. The DC bias can also significantly reduce capacitance. Ceramic capacitors can loss as much as 50% of its capacitance at its rated voltage. Therefore, leave the margin on the voltage rating to ensure adequate capacitance at the required output voltage.

The capacitor in the range of 1 μF to 4.7 μF is recommended for input side. The output requires a capacitor in the range of 0.47 μF to 10 μF. The output capacitor affects the loop stability of the boost regulator. If the output capacitor is below the range, the boost regulator can potentially become unstable. For example, when using an output capacitor of 0.1 μF, a 470-nF compensation capacitor has to be used for the loop stable.

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The popular vendors for high value ceramic capacitors are:

TDK (http://www.component.tdk.com/components.php)

Murata (http://www.murata.com/cap/index.html)

8.2.1.3 Application Curves

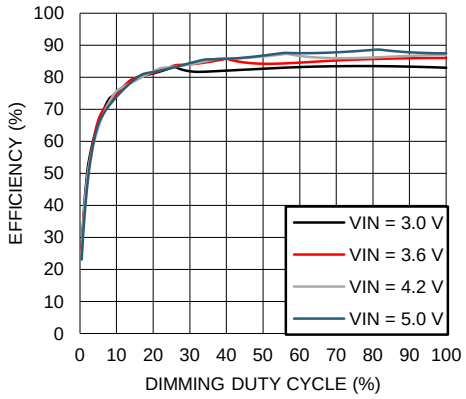

Figure 17. Efficiency vs Dimming Duty Cycle

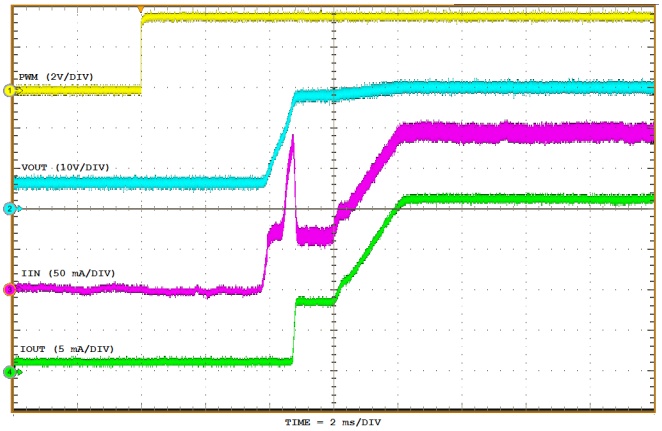

Figure 18. Start-Up with 10 Series LEDs (D_{PWM} = 100%)

8.2.2 Li-Ion Driver for 6 White LEDs with External PWM Dimming Network

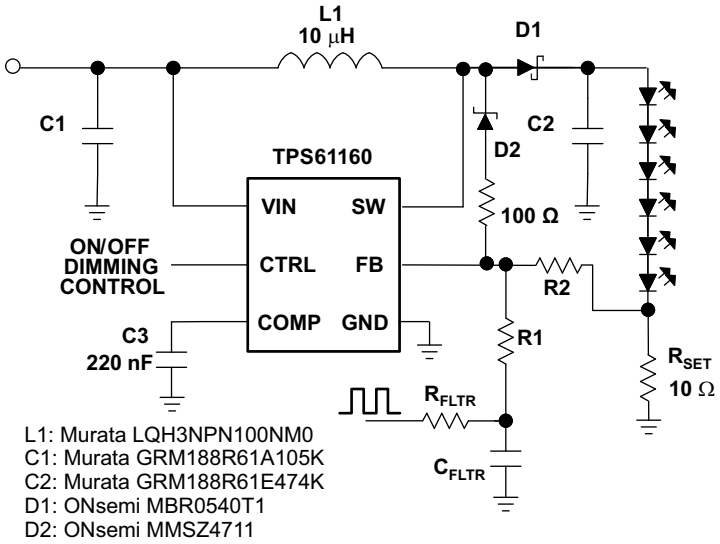

Figure 19. Li-Ion Driver for 6 White LEDs with External PWM Dimming

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8.2.2.1 Design Requirements

Example parameters for white LEDs with external PWM dimming:

Table 5. Design Parameters for White LEDs with External PWM Dimming

DESIGN PARAMETER	EXAMPLE VALUE
Inductor	10 µH
Minimum input voltage	3.6 V
Number of series LED	6
LED maximum forward voltage (Vf)	3.2 V
Schottky diode forward voltage (Vf)	0.2 V
Efficiency	90%
Switching frequency (f_{SW})	600 kHz
External PWM output voltage	3 V
External PWM frequency	20 kHz

Applying Equation 3 and Equation 4 when V_{IN} is 3 V, 6 LEDs output equivalent to V_{OUT} of 19.4 V, the inductor is 10 µH, the Schottky forward voltage is 0.2 V, the maximum output current is 76 mA in typical condition.

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Choosing Component Values

As per SLVA471, the values of R_{FLTR}, C_{FLTR}, R_1, R_2, and R_{SET} are determined by the system parameters and error tolerance. The main source of LED current error is leakage current from the FB pin. The error gets worse as the LED current decreases. The error due to leakage current is given by *Functional Block Diagram*, where the impedance seen by the FB pin has a major impact. To reduce error due to the leakage current, the impedance seen by the FB pin needs to be small. Because R_2 is much smaller than $R_1 + R_{FLTR}$, R_2 must be chosen to be small to minimize the impedance seen by the FB pin. In general, R_2 must be chosen to be 1 kΩ or less. If greater accuracy at smaller currents is needed, then R_2 must be chosen to be even smaller.

$$\%\text{error} = \frac{I_{FB}}{\frac{V_{FB}}{(R_1 + R_{FLTR}) // R_2} - \frac{D \times V_{PWM(H)} + (1-D)V_{PWM(L)}}{R_1 + R_{FLTR}}} \quad (8)$$

Once R_2 has been chosen, the value of R_{SET} and $R_1 + R_{FLTR}$ can be calculated using Equation 9, Equation 10, Equation 11, and Equation 12. The individual values of R_1 and R_{FLTR} can be any combination that sums up to $R_1 + R_{FLTR}$. In general, choosing R_1 and R_{FLTR} to be the same value gives a minimum requirement for C_{FLTR}.

$$V_{PWM(min)} = D_{(min)}V_{PWM(H)} + (1 - D_{(min)})V_{PWM(L)} \quad (9)$$

$$V_{PWM(max)} = D_{(max)}V_{PWM(H)} + (1 - D_{(max)})V_{PWM(L)} \quad (10)$$

$$R_{SET} = \frac{V_{FB}\left(V_{PWM(max)} - V_{PWM(min)}\right)}{V_{PWM(max)}I_{LED(max)} - V_{FB}I_{LED(max)} + V_{FB}I_{LED(min)} - V_{PWM(min)}I_{LED(min)}} \quad (11)$$

$$R_1 + R_{FLTR} = \frac{R_2(I_{LED(max)}(V_{PWM(max)} - V_{FB}) - I_{LED(min)}(V_{PWM(min)} - V_{FB}))}{V_{FB}(I_{LED(max)} - I_{LED(min)})} + \frac{V_{PWM(max)} - V_{PWM(min)}}{I_{LED(max)} - I_{LED(min)}} \quad (12)$$

Finally, C_{FLTR} can be chosen based on the amount of filtering desired or to provide a gradual dimming effect that is popular in many lighting products. At a minimum, C_{FLTR} must be chosen to provide at least 20 dB of attenuation at the PWM frequency. Equation 13 can be used to calculate the minimum capacitor value to provide this attenuation.

$$C_{FLTR} = \frac{1}{2\pi\,(R_{FLTR} // R_1)\frac{f_{pwm}}{10}} \quad (13)$$

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To provide gradual dimming, a large capacitor must be chosen to provide a long transient time when changing the PWM duty cycle. Equation 14 shows how to calculate the recommended corner frequency of the RC filter based on the 10% to 90% rise time. Once the corner frequency is known, it can be used to calculate the required capacitor using Equation 15.

$$f_{RC} = \frac{0.35}{t_r} \quad (14)$$

$$C_{FLTR} = \frac{1}{2\pi \left(R_{FLTR} \,//\, R_1\right) f_{RC}} \quad (15)$$

For example, a design with R_{FLTR} and R_1 equal to 10 kΩ and a desired rise time of 500 ms requires a corner frequency of 0.7 Hz and a capacitor of 47 µF.

8.2.2.3 Application Curves

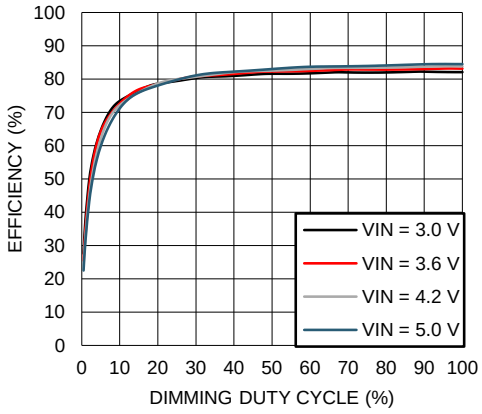

Figure 20. Efficiency vs Dimming Duty Cycle

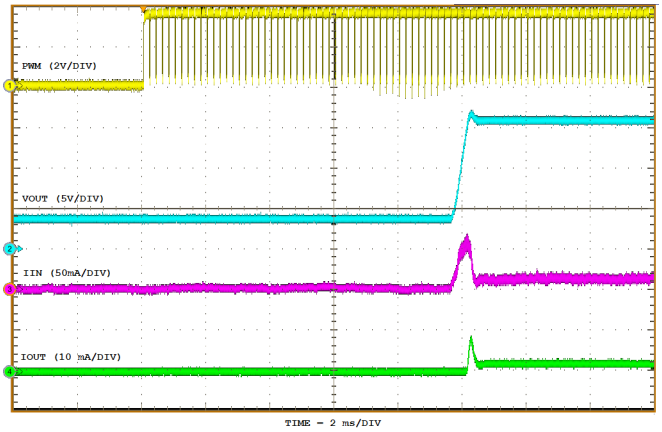

Figure 21. Start-Up with 6 Series LEDs (External PWM, D_{PWM} = 50%)

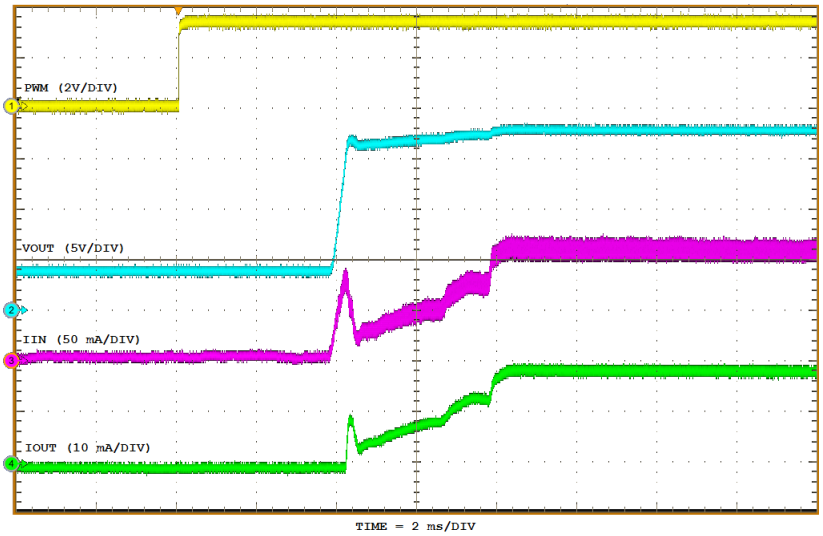

Figure 22. Start-Up with 6 Series LEDs (External PWM, D_{PWM} = 100%)

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8.2.3 Li-Ion Driver for 6 White LEDs

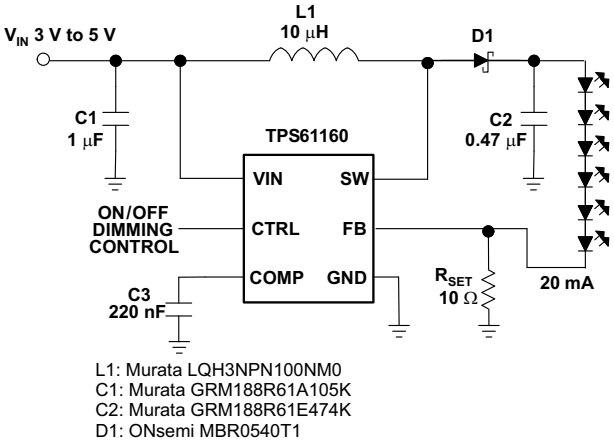

Figure 23. Li-Ion Driver for 6 White LEDs

8.2.3.1 Design Requirements

Example parameters for Li-Ion drivers with 6 white LEDs:

Table 6. Design Parameters for Li-Ion Driver with 6 White LEDs

DESIGN PARAMETER	EXAMPLE VALUE
Inductor	10 µH
Minimum input voltage	3 V
Number of series LED	6
LED maximum forward voltage (Vf)	3.2 V
Schottky diode forward voltage (Vf)	0.6 V
Efficiency (η)	88%
Switching frequency	600 kHz

Applying Equation 3 and Equation 4, when V_{IN} is 3 V, 6 LEDs output equivalent to V_{OUT} of 19.4 V, the inductor is 10 µH, the Schottky forward voltage is 0.2 V, the maximum output current is 66 mA in typical condition.

8.2.3.2 Detailed Design Procedure

See *Detailed Design Procedure*.

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8.2.3.3 Application Curves

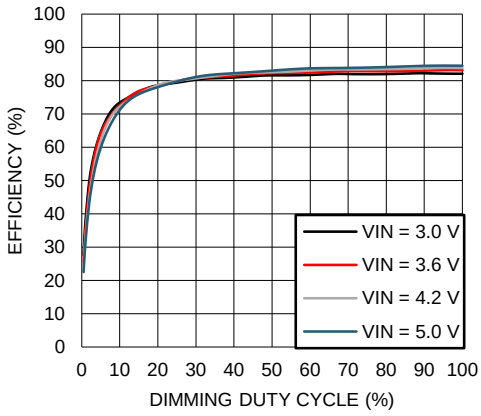

Figure 24. Efficiency vs Duty Cycle

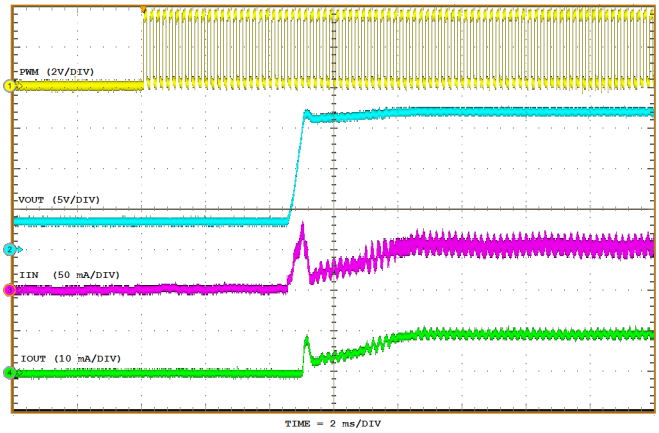

Figure 25. Start-Up with 6 Series LEDs (D_{PWM} = 50%)

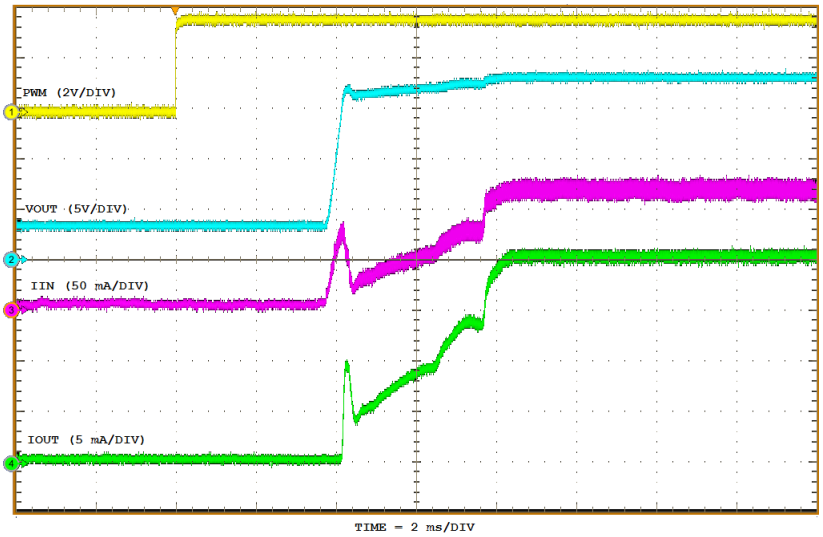

Figure 26. Start-Up with 6 Series LEDs (D_{PWM} = 100%)

8.2.4 Li-Ion Driver for 8 White LEDs

For assistance in selecting the proper values for R_{SET}, R1-R3, RFLTR, CFLTR and D2 for the specific application, refer to SLVA471 and/or SLVC366.

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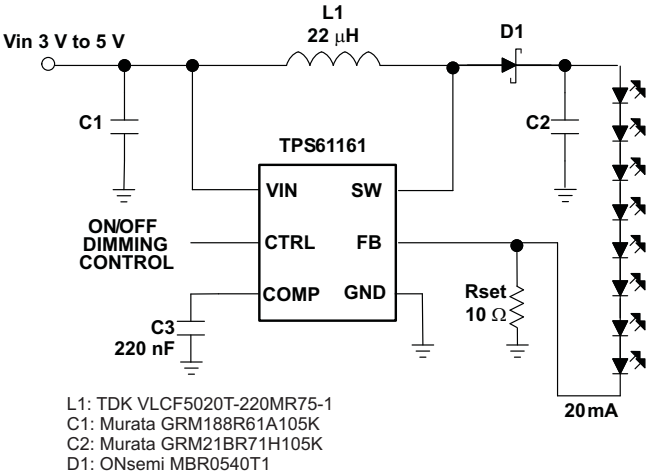

Figure 27. Li-Ion Driver for 8 White LEDs

8.2.4.1 Design Requirements

Example parameters for Li-Ion driver with 8 white LEDs:

Table 7. Design Parameters for Li-Ion Driver with 8 White LEDs

DESIGN PARAMETER	EXAMPLE VALUE
Inductor	22 µH
Minimum input voltage	3 V
Number of series LED	8
LED maximum forward voltage (Vf)	3.2 V
Schottky diode forward voltage	0.2 V
Efficiency (η)	85%
Switching frequency	600 kHz

Applying Equation 3 and Equation 4, when V_{IN} is 3 V, 8 LEDs output equivalent to V_{OUT} of 25.8 V, the inductor is 22 µH, the Schottky forward voltage is 0.2 V, the maximum output current is 60 mA in typical condition.

8.2.4.2 Detailed Design Procedure

See *Detailed Design Procedure*.

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8.2.4.3 Application Curves

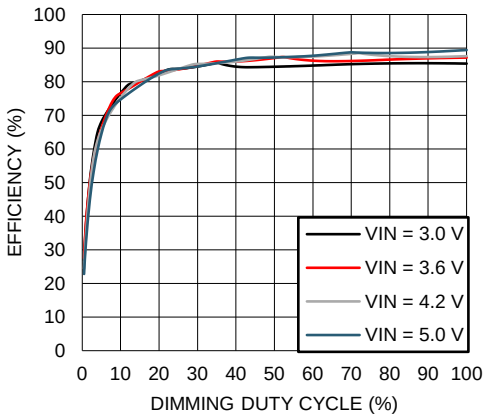

Figure 28. Efficiency vs Duty Cycle

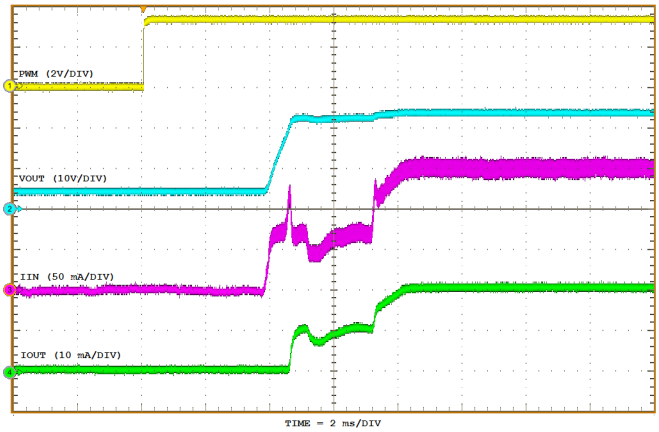

Figure 29. Start-Up with 8 Series LEDs (D_{PWM} = 100%)

9 Power Supply Recommendations

The TPS61160 and TPS61161 are designed to operate from an input supply range of 2.7 V to 18 V. This input supply must be well regulated and be able to provide the peak current required by the LED configuration and inductor selected without voltage drop under load transients (start-up or rapid brightness change). The resistance of the input supply rail must be low enough such that the input current transient does not cause the TPS61160 and TPS61161 supply voltage to droop more than 5%. Additional bulk decoupling located close to the input capacitor (C_{IN}) may be required to minimize the impact of the input supply rail resistance.

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10 Layout

10.1 Layout Guidelines

As for all switching power supplies, especially those high frequency and high current ones, layout is an important design step. If layout is not carefully done, the regulator could suffer from instability as well as noise problems. To reduce switching losses, the SW pin rise and fall times are made as short as possible. To prevent radiation of high frequency resonance problems, proper layout of the high frequency switching path is essential. Minimize the length and area of all traces connected to the SW pin and always use a ground plane under the switching regulator to minimize inter-plane coupling. The loop including the PWM switch, Schottky diode, and output capacitor, contains high current rising and falling in nanosecond and must be kept as short as possible. The input capacitor must not only be close to the VIN pin, but also to the GND pin in order to reduce the device supply ripple. Figure 30 shows a sample layout.

10.2 Layout Example

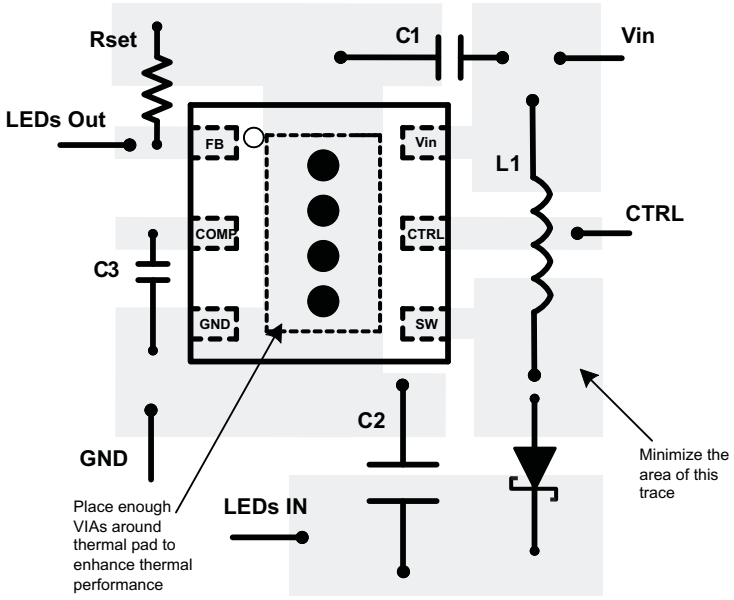

Figure 30. TPS6116x Sample Layout

10.3 Thermal Considerations

The maximum device junction temperature should be restricted to 125°C under normal operating conditions. This restriction limits the power dissipation of the TPS61160 or TPS61161. Calculate the maximum allowable dissipation, $P_{D(max)}$, and keep the actual dissipation less than or equal to $P_{D(max)}$. The maximum-power-dissipation limit is determined using values in *Equation 16*:

$$P_{D(max)} = \frac{125°C - T_A}{R_{\theta JA}} \quad (16)$$

where

- T_A is the maximum ambient temperature for the application
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient given in *Thermal Information*.

The TPS61160 and TSP61161 come in a thermally enhanced WSON package. This package includes a thermal pad that improves the thermal capabilities of the package. The $R_{\theta JA}$ of the WSON package greatly depends on the PCB layout and thermal pad connection. The thermal pad must be soldered to the analog ground on the PCB. Using thermal vias underneath the thermal pad as illustrated in the layout example. Also see the *QFN/SON PCB Attachment* application report (SLUA271).

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11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

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11.2 ドキュメントのサポート

11.2.1 関連資料

関連資料については、以下を参照してください。

- *『QFN/SONのPCB実装』*
- *『TPS6116xでアナログ調光を使用する方法』*
- *『PWM信号を使用するアナログ調光の設計ツール』*

11.3 関連リンク

11.3.1 関連リンク

表 8 に、クイック・アクセス・リンクの一覧を示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびサンプル注文またはご購入へのクイック・アクセスが含まれます。

表 8. 関連リンク

製品	プロダクト・フォルダ	サンプルとご購入	技術資料	ツールとソフトウェア	サポートとコミュニティ
TPS61160	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
TPS61161	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

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11.5 コミュニティ・リソース

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Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

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11.8 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。これらの情報は、指定のデバイスに対して提供されている最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS61160DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BZQ	Samples
TPS61160DRVRG4	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BZQ	Samples
TPS61160DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BZQ	Samples
TPS61161DRVR	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BZR	Samples
TPS61161DRVRG4	ACTIVE	WSON	DRV	6	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BZR	Samples
TPS61161DRVT	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BZR	Samples
TPS61161DRVTG4	ACTIVE	WSON	DRV	6	250	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 85	BZR	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS61161 :

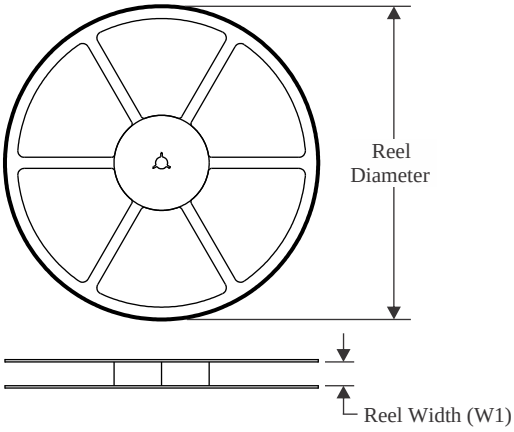
- Automotive : TPS61161-Q1

NOTE: Qualified Version Definitions:

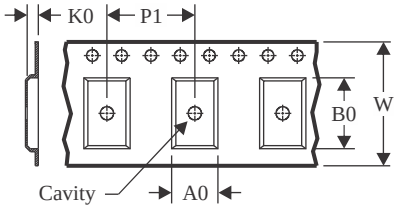
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

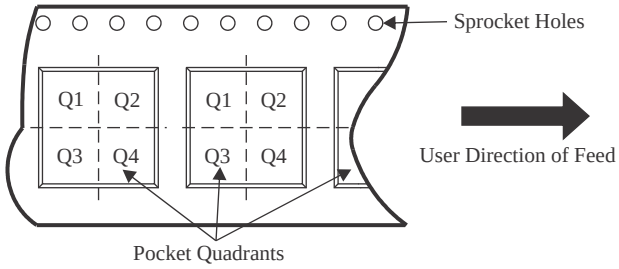


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

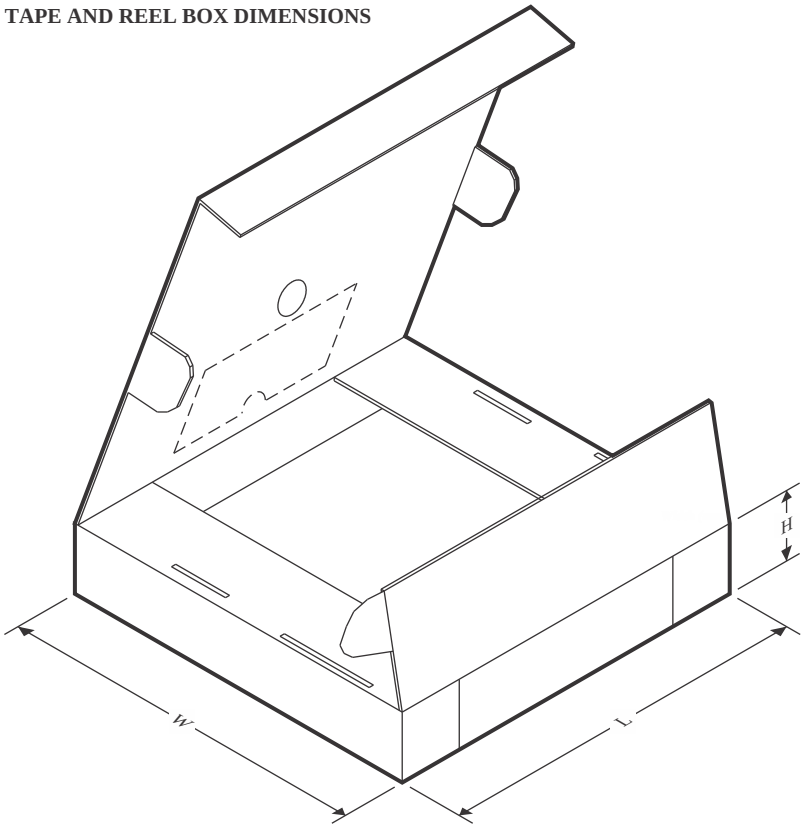
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS61160DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS61160DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS61160DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS61161DRVR	WSON	DRV	6	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS61161DRVT	WSON	DRV	6	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS

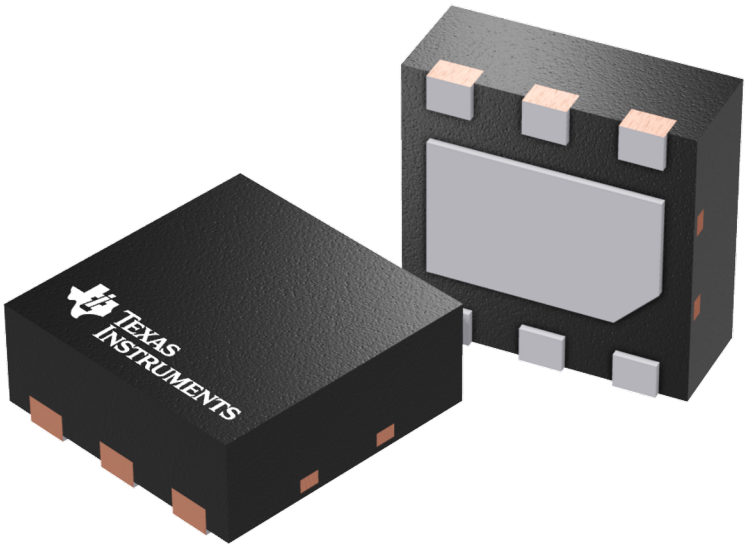


*All dimensions are nominal

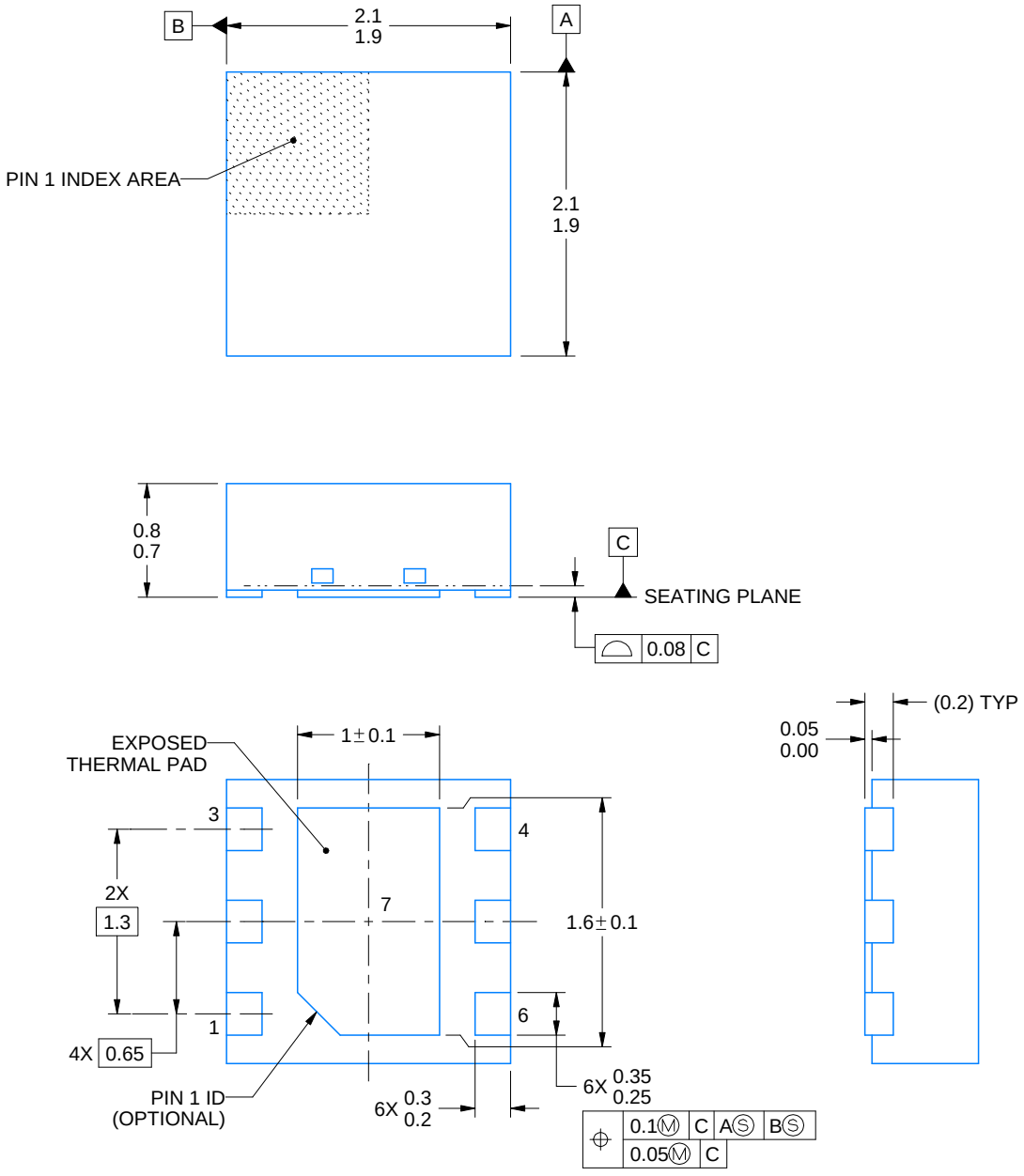
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS61160DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS61160DRVT	WSON	DRV	6	250	210.0	185.0	35.0
TPS61160DRVT	WSON	DRV	6	250	210.0	185.0	35.0
TPS61161DRVR	WSON	DRV	6	3000	210.0	185.0	35.0
TPS61161DRVT	WSON	DRV	6	250	210.0	185.0	35.0

DRV 6 WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

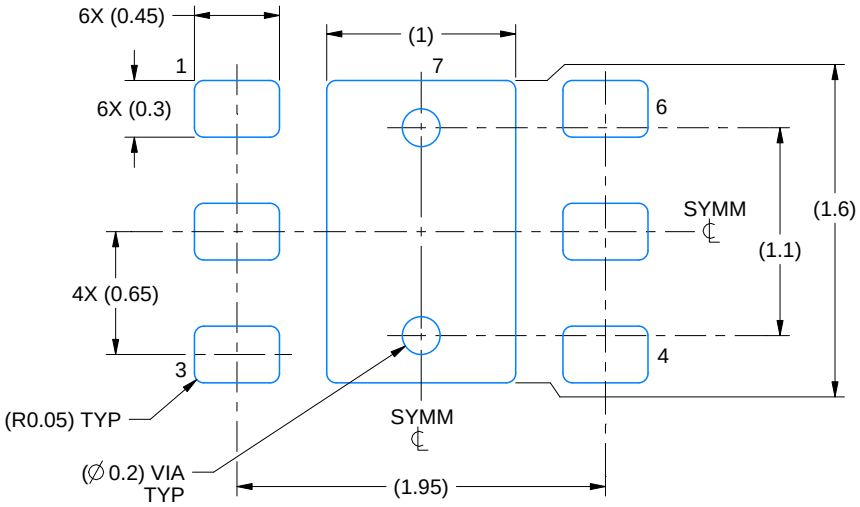


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

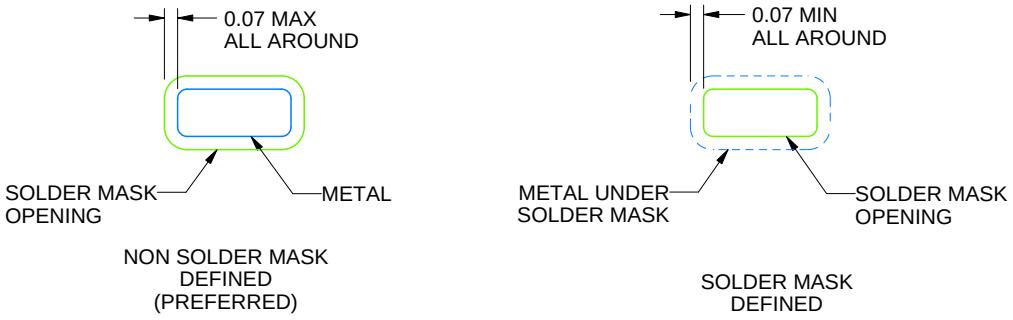


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:25X

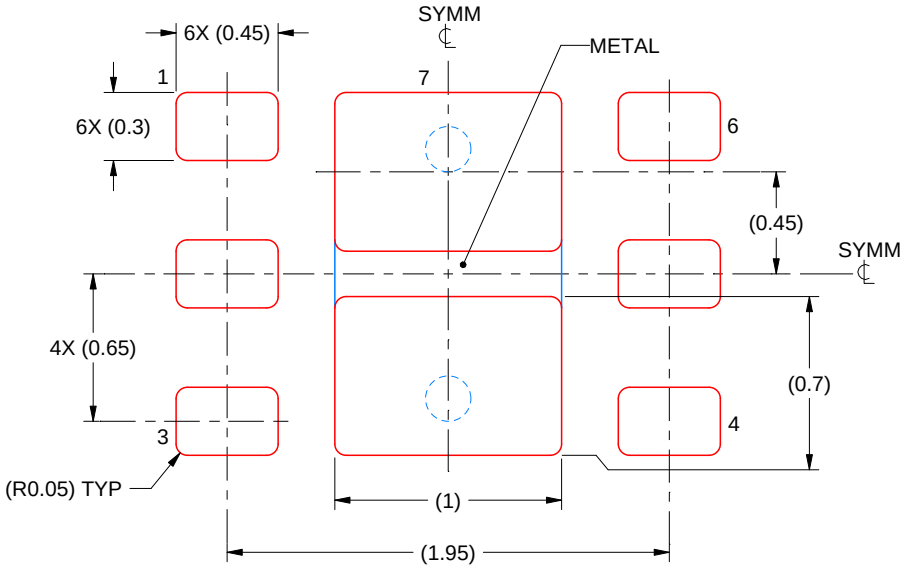


SOLDER MASK DETAILS

4222173/B 04/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If some or all are implemented, recommended via locations are shown.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD #7
88% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:30X

4222173/B 04/2018

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

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