TPS732-Q1 Cap-Free NMOS 250-mA Low-Dropout Regulator With Reverse-Current Protection

1 Features

- Qualified for Automotive Applications
- AEC-Q100 Qualified With the Following Results
  - Device Temperature Grade 0: –40°C to 150°C Ambient Operating Temperature Range
  - Device HBM Classification Level 2
  - Device CDM Classification Level C4B
  - Device MM Classification Level M2
- Stable With No Output Capacitor or Any Value or Type of Capacitor
- Input Voltage Range: 1.7 V to 5.5 V
- Ultra-Low Dropout Voltage: 40-mV Typical at 250 mA
- Excellent Load Transient Response—With or Without Optional Output Capacitor
- New NMOS Topology Provides Low Reverse Leakage Current
- Low Noise: 30-μV_{RMS} Typical (10 kHz to 100 kHz)
- 0.5% Initial Accuracy
- 1% Overall Accuracy (Line, Load, and Temperature)
- Less Than 1-µA Maximum I_Q in Shutdown Mode
- Thermal Shutdown and Specified Minimum and Maximum Current Limit Protection
- Available in Multiple Output Voltage Versions
  - Fixed Outputs of 1.2 V, 1.5 V, 1.6 V, 1.8 V, 2.5 V, 3 V, 3.3 V, and 5 V
  - Adjustable Outputs From 1.2 V to 5.5 V
  - Custom Outputs Available

2 Applications

- Portable and Battery-Powered Equipment
- Post-Regulation for Switching Supplies
- Noise-Sensitive Circuitry Such as VCOs
- Point of Load Regulation for DSPs, FPGAs, ASICs, and Microprocessors

3 Description

The TPS732-Q1 family of low-dropout (LDO) voltage regulators uses a new topology: an NMOS pass element in a voltage-follower configuration. This topology is stable using output capacitors with low ESR, and even allows operation without a capacitor. The topology also provides high reverse blockage (low reverse current) and ground pin current that is nearly constant over all values of output current.

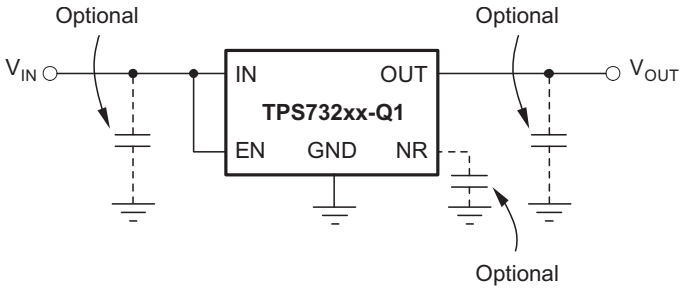
The TPS732-Q1 family of devices uses an advanced BiCMOS process to yield high precision while delivering low dropout voltages and low ground pin current. Current consumption, when not enabled, is under 1 µA and ideal for portable applications. The extremely low output noise (30 μV_{RMS} with 0.1-µF C_{NR}) is ideal for powering VCOs. These devices are protected by thermal shutdown and foldback current limit.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TPS73201-Q1	SOT-23 (5)	2.90 mm × 1.60 mm
	VSON (8)	3.00 mm × 3.00 mm

(1) For all available packages, see the orderable addendum at the end of the datasheet.

Typical Application Circuit for Fixed Voltage Versions



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4 Revision History

Changes from Revision E (August 2013) to Revision F **Page**

- Added *Device Information* table, *Table of Contents*, *Specifications* section, *ESD Ratings* table, *Recommended Operating Conditions* table, *Detailed Description* section, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

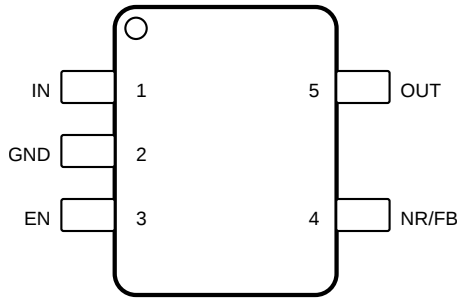
Changes from Revision D (March 2009) to Revision E **Page**

- Deleted TPS73215-Q1, TPS73216-Q1, TPS73218-Q1, TPS73230-Q1, TPS73233-Q1, and TPS73250-Q1 from the data sheet ... 1

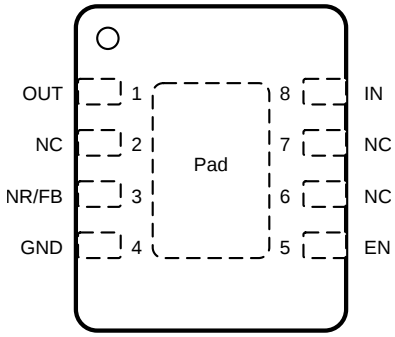
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5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



DRB Package
8-Pin VSON With Exposed Thermal Pad
Top View



NC: No internal connection

Pin Functions

PIN			TYPE	DESCRIPTION
NAME	NO.			
	SOT-23	VSON		
EN	3	5	I	Driving the enable pin (EN) high turns on the regulator. Driving this pin low puts the regulator into shutdown mode. See *Shutdown* for more details. EN can be connected to IN if not used.
FB(1)	4	3	I	Input to the control loop error amplifier, and is used to set the output voltage of the device.
GND	2	4	—	Ground
IN	1	8	I	Unregulated input supply
NR(2)	4	3	—	Connecting an external capacitor to this pin bypasses noise generated by the internal bandgap. This allows output noise to be reduced to low levels.
OUT	5	1	O	Output of the regulator. There are no output capacitor requirements for stability.
Pad	—	Pad	—	Ground
NC	—	2, 6, 7	—	No internal connection

(1) Adjustable voltage versions only.
(2) Fixed voltage versions only.

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6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
V_{IN}	–0.3	6	V
V_{EN}	–0.3	6	V
V_{OUT}	–0.3	5.5	V
Peak output current	Internally limited		
Output short-circuit duration	Indefinite		
Junction temperature, T_J	–55	150	°C
Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1)	±4000	V
		Charged-device model (CDM), per AEC Q100-011	±1000	
		Machine model (MM)	±200	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_{IN}	Input voltage(1)	1.7	5.5	V
I_{OUT}	Output current	0	250	mA
T_J	Operating junction temperature	–40	125	°C

(1) Minimum $V_{IN} = V_{OUT} + V_{DO}$ or 1.7 V, whichever is greater.

6.4 Thermal Information

THERMAL METRIC(1)		TPS732-Q1		UNIT
		DBV (SOT-23)	DRB (VSON)	
		5 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	180	47.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	64	83	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	35	—	°C/W
ψ_{JT}	Junction-to-top characterization parameter	—	2.1	°C/W
ψ_{JB}	Junction-to-board characterization parameter	—	17.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	12.1	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

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6.5 Electrical Characteristics

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V(1), I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted. Typical values are at T_J = 25°C

PARAMETER			TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{FB}	Internal reference (TPS73201-Q1)		T_J = 25°C	1.198	1.2	1.21	V
V_{OUT}	Output voltage range (TPS73201-Q1)(2)			V_{FB}		5.5 – V_{DO}	V
	Accuracy(1)	Nominal	T_J = 25°C	–0.5%		0.5%	
		V_{IN}, I_{OUT}, and T_J	(V_{OUT} + 0.5 V) ≤ V_{IN} ≤ 5.5 V, 10 mA ≤ I_{OUT} ≤ 250 mA	–1%	±0.5%	1%	
$\Delta V_{OUT}\%/\Delta V_{IN}$	Line regulation(1)		($V_{OUT(nom)}$ + 0.5 V) ≤ V_{IN} ≤ 5.5 V		0.06		%/V
$\Delta V_{OUT}\%/\Delta I_{OUT}$	Load regulation		1 mA ≤ I_{OUT} ≤ 250 mA		0.002		%/mA
			10 mA ≤ I_{OUT} ≤ 250 mA		0.0008		
V_{DO}	Dropout voltage (V_{IN} = V_{OUT} (nom) – 0.1 V)		I_{OUT} = 250 mA		40	150	mV
Z_O(DO)	Output impedance in dropout		1.7 V ≤ V_{IN} ≤ (V_{OUT} + V_{DO})		0.25		Ω
I_{CL}	Output current limit		V_{OUT} = 0.9 × $V_{OUT(nom)}$	250	425	600	mA
I_{SC}	Short-circuit current		V_{OUT} = 0 V		300		mA
I_{REV}	Reverse leakage current(3) ($-I_{IN}$)		V_{EN} ≤ 0.5 V, 0 V ≤ V_{IN} ≤ V_{OUT}		0.1	10	µA
I_{GND}	Ground pin current		I_{OUT} = 10 mA (I_Q)		400	550	µA
			I_{OUT} = 250 mA		650	950	
I_{SHDN}	Shutdown current (I_{GND})		V_{EN} ≤ 0.5 V, V_{OUT} ≤ V_{IN} ≤ 5.5		0.02	1	µA
PSRR	Power-supply rejection ratio (ripple rejection)		f = 100 Hz, I_{OUT} = 250 mA		58		dB
			f = 10 kHz, I_{OUT} = 250 mA		37		
V_N	Output noise voltage BW = 10 Hz – 100 kHz		C_{OUT} = 10 µF, No C_{NR}		27 × V_{OUT}		μV_{RMS}
			C_{OUT} = 10 µF, C_{NR} = 0.01 µF		8.5 × V_{OUT}		
V_{EN}(HI)	Enable high (enabled)			1.7		V_{IN}	V
V_{EN}(LO)	Enable low (shutdown)			0		0.5	V
I_{EN}(HI)	Enable pin current (enabled)		V_{EN} = 5.5 V		0.02	0.1	µA
T_{SD}	Thermal shutdown temperature		Shutdown, temperature increasing		160		°C
			Reset, temperature decreasing		140		

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 1.7 V, whichever is greater.
(2) TPS73201-Q1 is tested at V_{OUT} = 2.5 V.
(3) Fixed-voltage versions only; see *Reverse Current* for more information.

6.6 Switching Characteristics

Over operating temperature range (T_J = –40°C to 125°C), V_{IN} = $V_{OUT(nom)}$ + 0.5 V(1), I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted. Typical values are at T_J = 25°C

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{STR}	Start-Up time	V_{OUT} = 3 V, R_L = 30 Ω C_{OUT} = 1 µF, C_{NR} = 0.01 µF		600		µs

(1) Minimum V_{IN} = V_{OUT} + V_{DO} or 1.7 V, whichever is greater.

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6.7 Typical Characteristics

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted

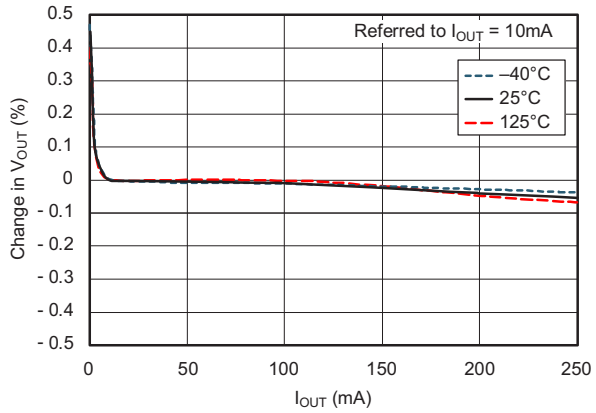


Figure 1. Load Regulation

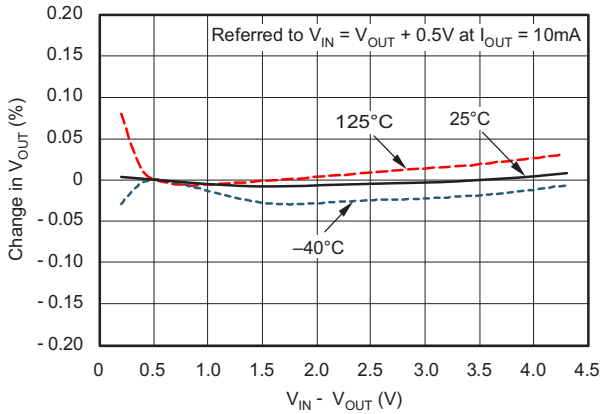


Figure 2. Line Regulation

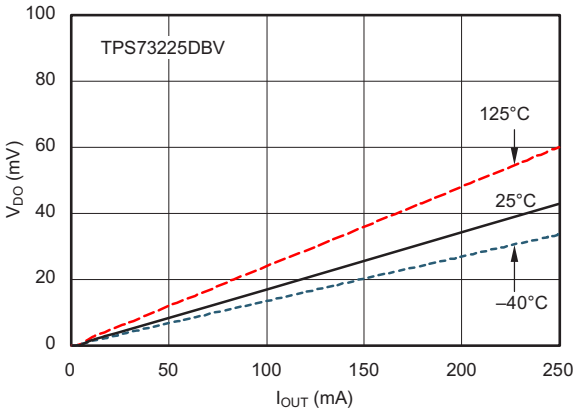


Figure 3. Dropout Voltage vs Output Current

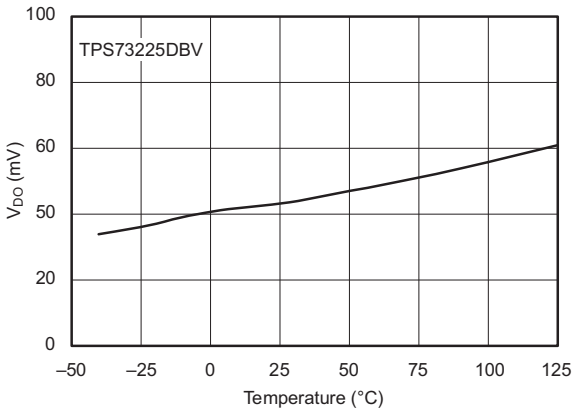


Figure 4. Dropout Voltage vs Temperature

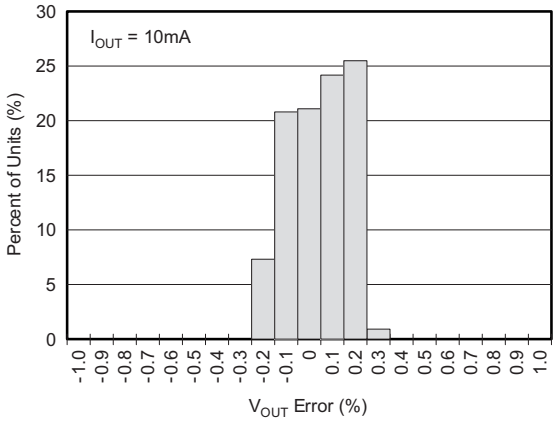


Figure 5. Output Voltage Accuracy Histogram

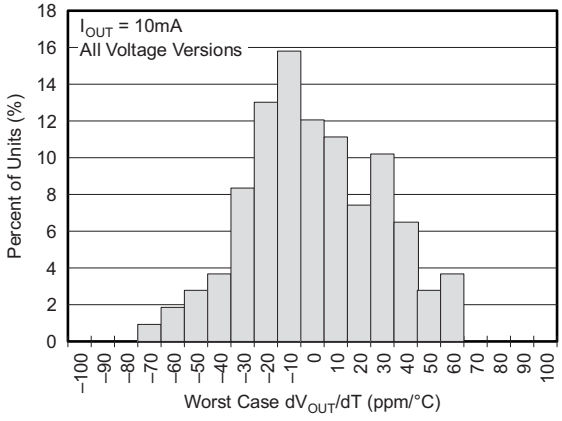


Figure 6. Output Voltage Drift Histogram

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Typical Characteristics (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted

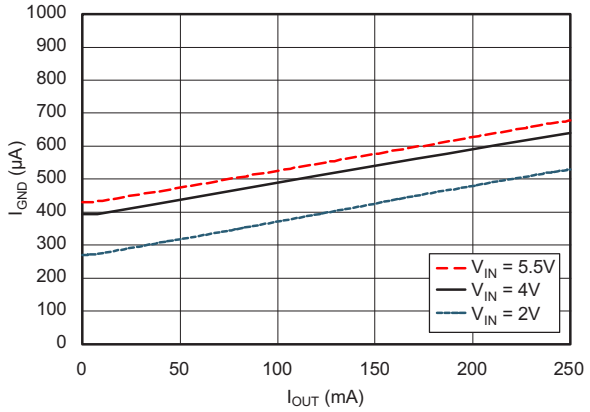


Figure 7. Ground Pin Current vs Output Current

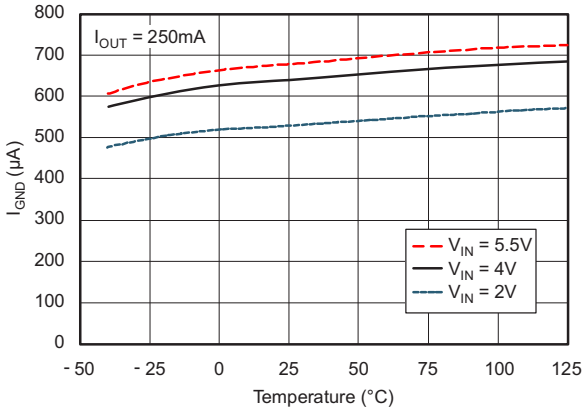


Figure 8. Ground Pin Current vs Temperature

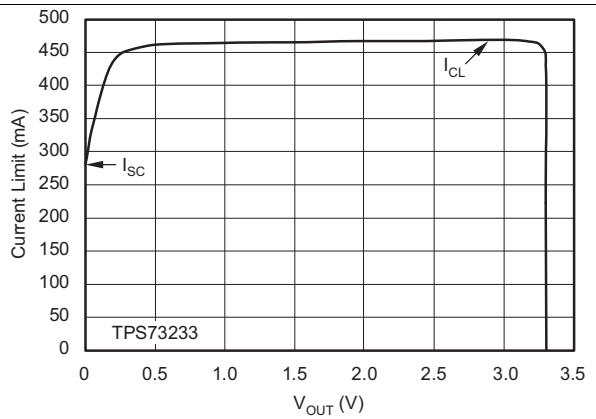


Figure 9. Current Limit vs V_{OUT} (FOLDBACK)

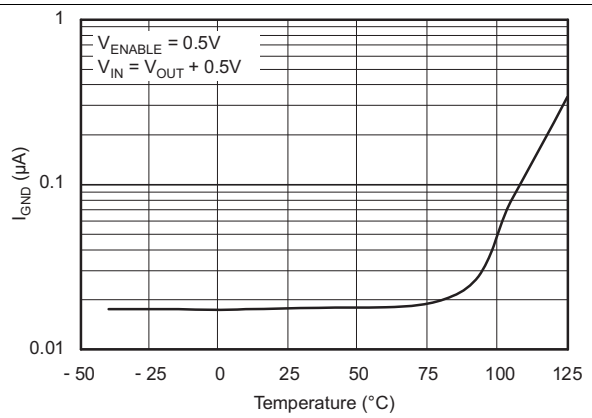


Figure 10. Ground Pin Current in Shutdown vs Temperature

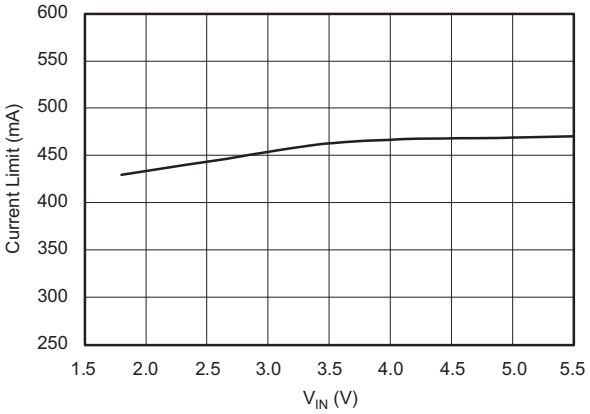


Figure 11. Current Limit vs V_{IN}

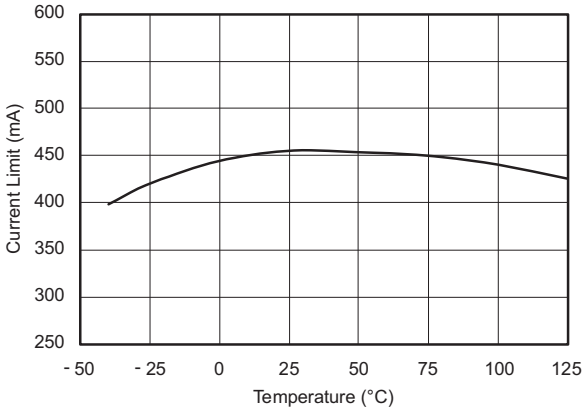


Figure 12. Current Limit vs Temperature

Typical Characteristics (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted

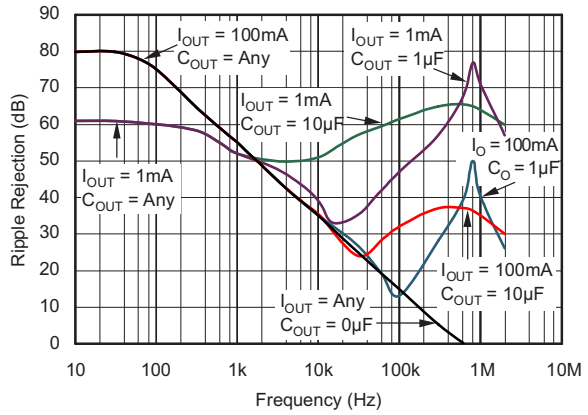


Figure 13. PSRR (Ripple Rejection) vs Frequency

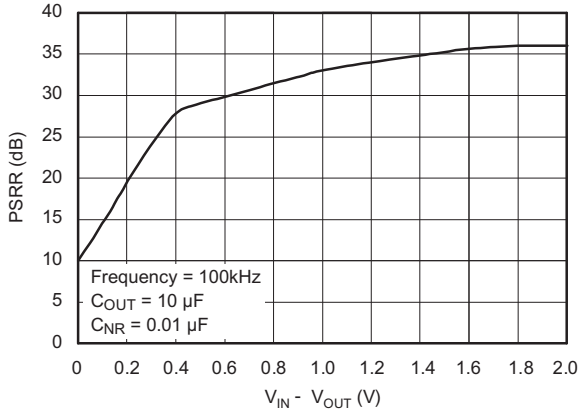


Figure 14. PSRR (Ripple Rejection) vs V_{IN} – V_{OUT}

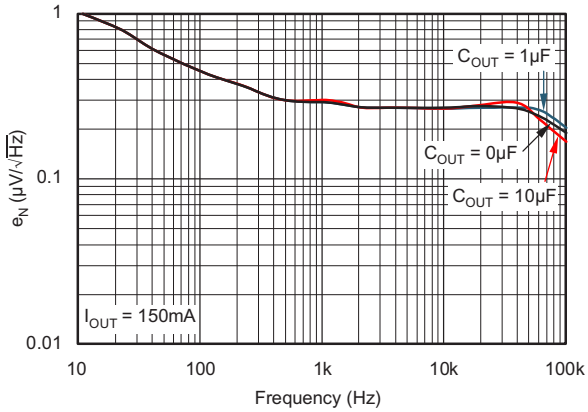


Figure 15. Noise Spectral Density vs C_{NR} = 0 µF

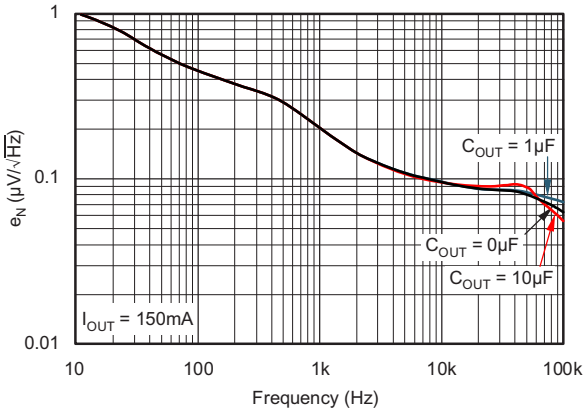


Figure 16. Noise Spectral Density vs C_{NR} = 0.01 µF

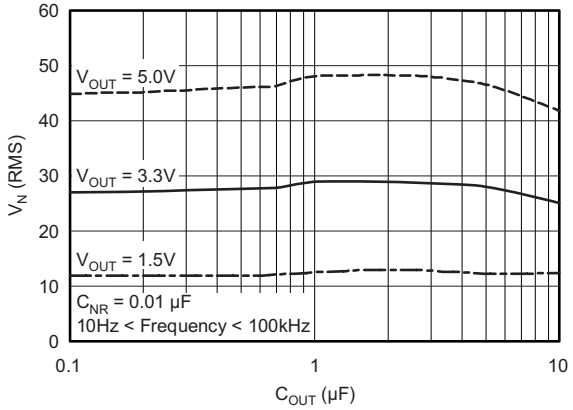


Figure 17. RMS Noise Voltage vs C_{OUT}

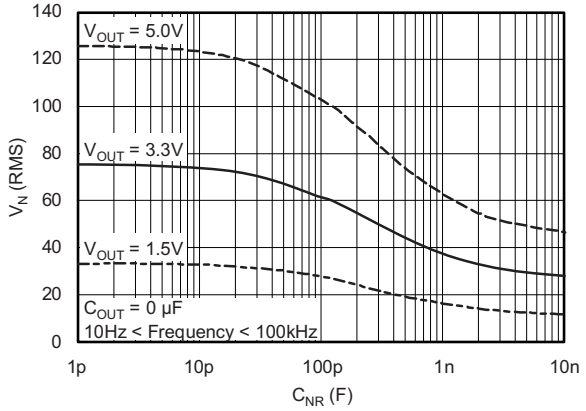


Figure 18. RMS Noise Voltage vs C_{NR}

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Typical Characteristics (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted

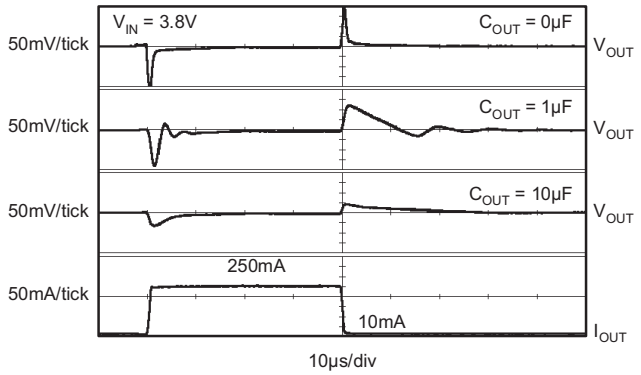


Figure 19. TPS73233-Q1 – Load Transient Response

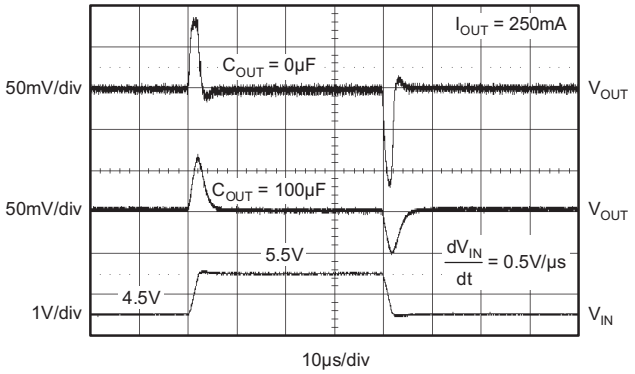


Figure 20. TPS73233-Q1 – Line Transient Response

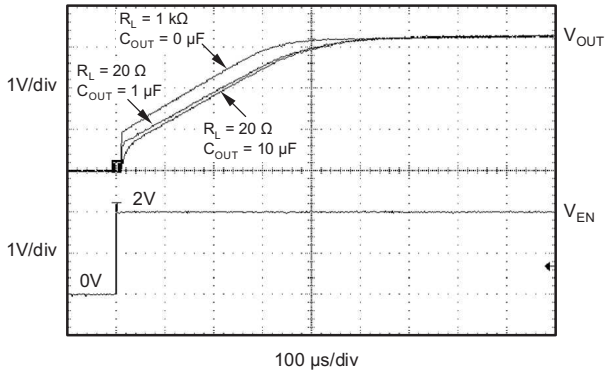


Figure 21. TPS73233-Q1 – Turnon Response

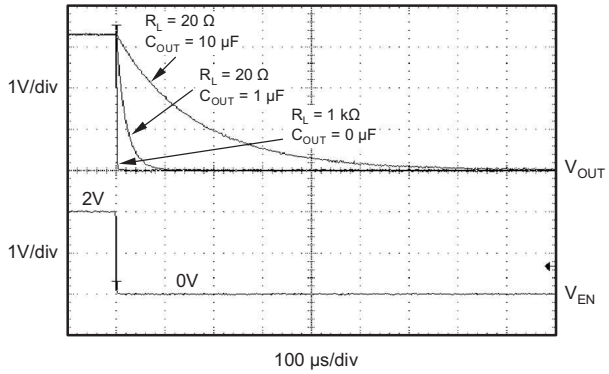


Figure 22. TPS73233-Q1 – Turnoff Response

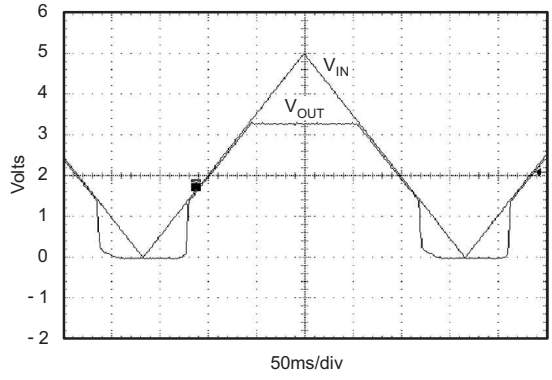


Figure 23. TPS73233-Q1 – Power Up and Power Down

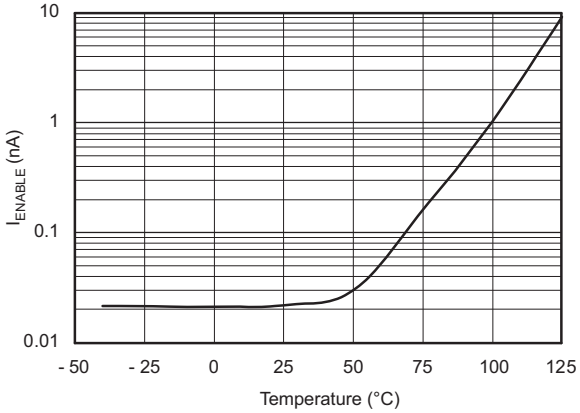


Figure 24. I_{ENABLE} vs Temperature

Typical Characteristics (continued)

For all voltage versions at T_J = 25°C, V_{IN} = $V_{OUT(nom)}$ + 0.5 V, I_{OUT} = 10 mA, V_{EN} = 1.7 V, and C_{OUT} = 0.1 µF, unless otherwise noted

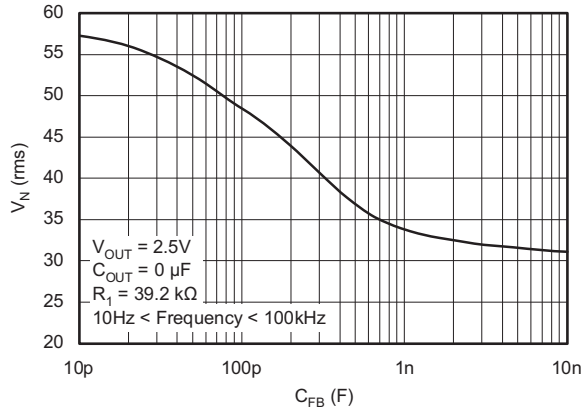


Figure 25. TPS73201-Q1 – RMS Noise Voltage vs C_{ADJ}

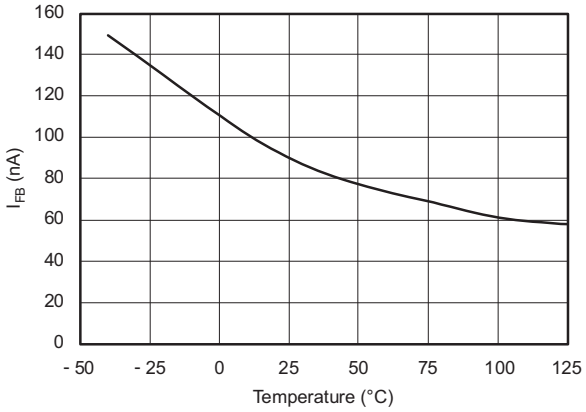


Figure 26. TPS73201-Q1 – I_{FB} vs Temperature

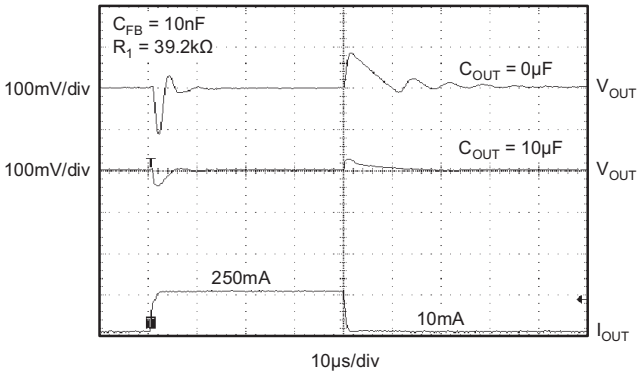


Figure 27. TPS73201-Q1 – Load Transient, Adjustable Version

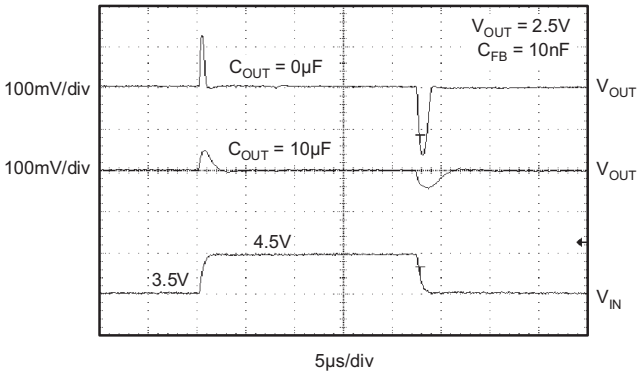


Figure 28. TPS73201-Q1 – Line Transient, Adjustable Version

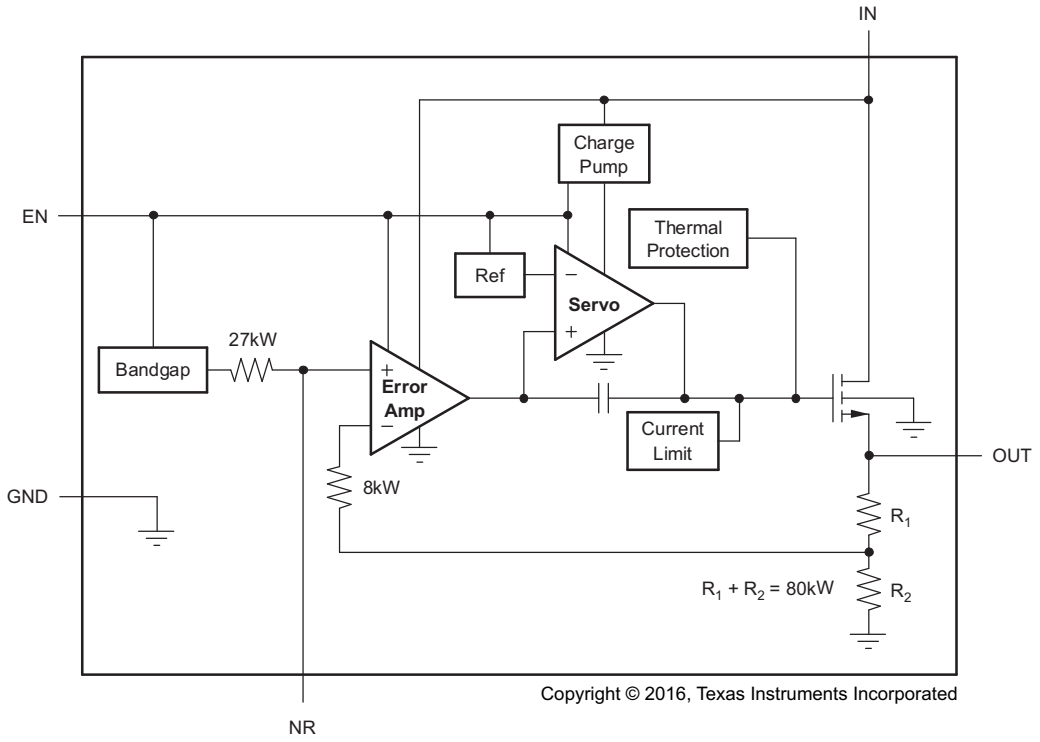
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7 Detailed Description

7.1 Overview

The TPS732-Q1 low-dropout linear regulator devices operate with an input voltage down to 1.7 V and support output voltages down to 1.2 V while sourcing up to 500 mA of load current. These linear regulators use an NMOS pass element with an integrated 4-MHz charge pump to provide a dropout voltage of less than 250 mV at full load current. This unique architecture also permits stable regulation over a wide range of output capacitors. In fact, the TPS732-Q1 family of devices does not require any output capacitor for stability. The increased insensitivity to the output capacitor value and type makes this family of linear regulators an ideal choice when powering a load where the effective capacitance is unknown. The TPS732-Q1 family of devices also features a noise reduction (NR) pin that allows for additional reduction of the output noise. The low noise output featured by the TPS732-Q1 family makes the device well-suited for powering VCOs or any other noise-sensitive load.

7.2 Functional Block Diagram



Fixed voltage version.

7.3 Feature Description

7.3.1 Internal Current Limit

The TPS732-Q1 internal current limit helps protect the regulator during fault conditions. Foldback helps to protect the regulator from damage during output short-circuit conditions by reducing current limit when V_{OUT} drops below 0.5 V. See Figure 9.

7.3.2 Shutdown

The enable pin is active high and is compatible with standard TTL-CMOS levels. V_{EN} below 0.5 V (maximum) turns the regulator off and drops the ground pin current to approximately 10 nA. When shutdown capability is not required, the Enable pin can be connected to V_{IN}. When a pullup resistor is used, and operation down to 1.8 V is required, use pullup resistor values below 50 kΩ.

Feature Description (continued)

7.3.3 Dropout Voltage

The TPS732-Q1 family of devices uses an NMOS pass transistor to achieve extremely low dropout. When (V_{IN} – V_{OUT}) is less than the dropout voltage (V_{DO}), the NMOS pass device is in its linear region of operation and the input-to-output resistance is the R_{DS-ON} of the NMOS pass element.

For large step changes in load current, the TPS732-Q1 family of devices requires a larger voltage drop from V_{IN} to V_{OUT} to avoid degraded transient response. The boundary of this transient dropout region is approximately twice the dc dropout. Values of V_{IN} – V_{OUT} above this line ensure normal transient response.

Operating in the transient dropout region can cause an increase in recovery time. The time required to recover from a load transient is a function of the magnitude of the change in load current rate, the rate of change in load current, and the available headroom (V_{IN} to V_{OUT} voltage drop). Under worst-case conditions [full-scale instantaneous load change with (V_{IN} – V_{OUT}) close to dc dropout levels], the TPS732-Q1 family of devices can take a couple of hundred microseconds to return to the specified regulation accuracy.

7.3.4 Transient Response

The low open-loop output impedance provided by the NMOS pass element in a voltage follower configuration allows operation without an output capacitor for many applications. As with any regulator, the addition of a capacitor (nominal value 1 µF) from the output pin to ground will reduce undershoot magnitude but increase duration. In the adjustable version, the addition of a capacitor, C_{FB}, from the output to the adjust pin will also improve the transient response.

The TPS732-Q1 family of devices does not have active pulldown when the output is over-voltage. This allows applications that connect higher voltage sources, such as alternate power supplies, to the output. This also results in an output overshoot of several percent if the load current quickly drops to zero when a capacitor is connected to the output. The duration of overshoot can be reduced by adding a load resistor. The overshoot decays at a rate determined by output capacitor C_{OUT} and the internal and external load resistance. The rate of decay is given by Equation 1 and Equation 2:

(Fixed voltage version)

$$dV / dt = \frac{V_{OUT}}{C_{OUT} \times 80\ k\Omega} \quad (1)$$

(Adjustable voltage version)

$$dV / dt = \frac{V_{OUT}}{C_{OUT} \times 80\ k\Omega \,||\, (R_1 + R_2)} \quad (2)$$

7.3.5 Reverse Current

The NMOS pass element of the TPS732-Q1 family of devices provides inherent protection against current flow from the output of the regulator to the input when the gate of the pass device is pulled low. To ensure that all charge is removed from the gate of the pass element, the enable pin must be driven low before the input voltage is removed. If this is not done, the pass element may be left on due to stored charge on the gate.

After the enable pin is driven low, no bias voltage is needed on any pin for reverse current blocking. Note that reverse current is specified as the current flowing out of the IN pin due to voltage applied on the OUT pin. There will be additional current flowing into the OUT pin due to the 80-kΩ internal resistor divider to ground (see the *Functional Block Diagram* and Figure 31).

For the TPS73201-Q1, reverse current may flow when V_{FB} is more than 1 V above V_{IN}.

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Feature Description (continued)

7.3.6 Thermal Protection

Thermal protection disables the output when the junction temperature rises to approximately 160°C, allowing the device to cool. When the junction temperature cools to approximately 140°C, the output circuitry is again enabled. Depending on power dissipation, thermal resistance, and ambient temperature, the thermal protection circuit may cycle on and off. This limits the dissipation of the regulator, protecting it from damage due to overheating.

Any tendency to activate the thermal protection circuit indicates excessive power dissipation or an inadequate heatsink. For reliable operation, junction temperature should be limited to 125°C maximum. To estimate the margin of safety in a complete design (including heatsink), increase the ambient temperature until the thermal protection is triggered; use worst-case loads and signal conditions. For good reliability, thermal protection should trigger at least 35°C above the maximum expected ambient condition of your application. This produces a worst-case junction temperature of 125°C at the highest expected ambient temperature and worst-case load.

The internal protection circuitry of the TPS732-Q1 family of devices has been designed to protect against overload conditions. It was not intended to replace proper heatsinking. Continuously running the TPS732-Q1 family of devices into thermal shutdown will degrade device reliability.

7.4 Device Functional Modes

7.4.1 Normal Operation

The TPS632-Q1 family of devices require an input voltage of at least 1.7 V to function properly and attempt to maintain regulation.

When operating the device near 5.5 V, take care to suppress any transient spikes that may exceed the 6-V absolute maximum voltage rating. The device must never operate at a DC voltage greater than 5.5 V.

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8 Application and Implementation

NOTE

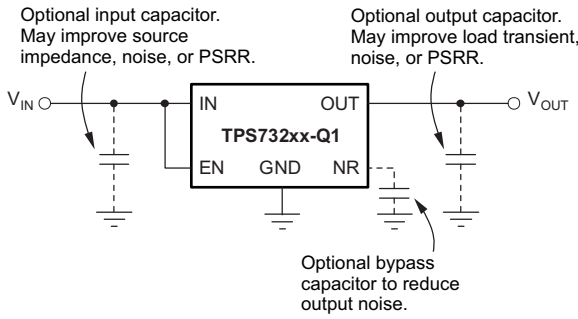
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The TPS732-Q1 belongs to a family of new generation LDO regulators that use an NMOS pass transistor to achieve ultra-low-dropout performance, reverse current blockage, and freedom from output capacitor constraints. These features, combined with low noise and an enable input, make the TPS732-Q1 family of devices ideal for portable applications. This regulator family offers a wide selection of fixed output voltage versions and an adjustable output version. All versions have thermal and overcurrent protection, including foldback current limit.

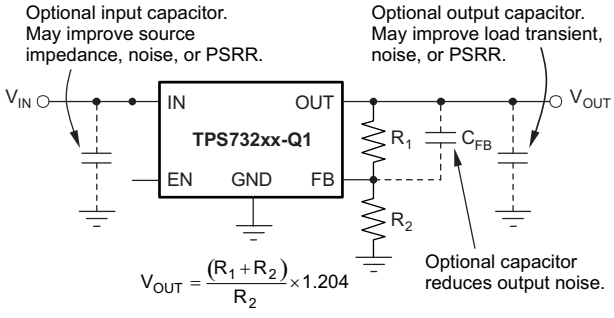
8.2 Typical Application

Figure 29 shows the basic circuit connections for the fixed voltage models. Figure 30 gives the connections for the adjustable output version (TPS73201-Q1).



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Figure 29. Typical Application Circuit for Fixed-Voltage Versions



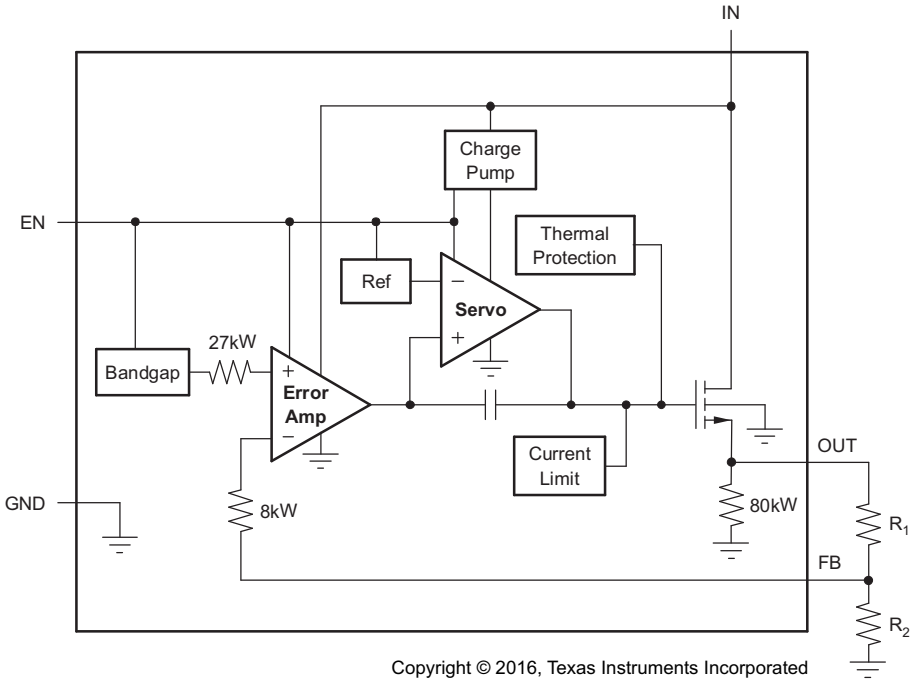
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Figure 30. Typical Application Circuit for Adjustable-Voltage Versions

Typical Application (continued)

8.2.1 Design Requirements

R_1 and R_2 can be calculated for any output voltage using the formula shown in Figure 30. Sample resistor values for common output voltages are shown in Figure 31. For best accuracy, make the parallel combination of R_1 and R_2 approximately 19 kΩ.



$V_{OUT} = (R_1 + R_2) / R_2 \times 1.204$
$R_1 \parallel R_2 \cong 19$ kΩ for best accuracy.

Figure 31. Adjustable Voltage Version

Table 1. Standard 1% Resistor Values for Common Output Voltages

V_{OUT}	R_1	R_2
1.2 V	Short	Open
1.5 V	23.2 kW	95.3 kW
1.8 V	28 kW	56.2 kW
2.5 V	39.2 kW	36.5 kW
2.8 V	44.2 kW	33.2 kW
3 V	46.4 kW	30.9 kW
3.3 V	52.3 kW	30.1 kW
5 V	78.7 kW	24.9 kW

8.2.2 Detailed Design Procedure

8.2.2.1 Input and Output Capacitor Requirements

Although an input capacitor is not required for stability, it is good analog design practice to connect a 0.1-µF to 1-µF low ESR capacitor across the input supply near the regulator. This counteracts reactive input sources and improves transient response, noise rejection, and ripple rejection. A higher-value capacitor may be necessary if large, fast rise-time load transients are anticipated or the device is located several inches from the power source.

The TPS732-Q1 family of devices does not require an output capacitor for stability and has maximum phase margin with no capacitor. It is designed to be stable for all available types and values of capacitors. In applications where $V_{IN} – V_{OUT} < 0.5$ V and multiple low ESR capacitors are in parallel, ringing may occur when the product of C_{OUT} and total ESR drops below 50 nF. Total ESR includes all parasitic resistances, including capacitor ESR and board, socket, and solder joint resistance. In most applications, the sum of capacitor ESR and trace resistance will meet this requirement.

8.2.2.2 Output Noise

A precision band-gap reference is used to generate the internal reference voltage, V_{REF}. This reference is the dominant noise source within the TPS732-Q1 family of devices and it generates approximately 32 μV_{RMS} (10 Hz to 100 kHz) at the reference output (NR). The regulator control loop gains up the reference noise with the same gain as the reference voltage, so that the noise voltage of the regulator is approximately given by:

$$V_N = 32\mu V_{RMS} \times \frac{(R_1 + R_2)}{R_2} = 32\mu V_{RMS} \times \frac{V_{OUT}}{V_{REF}} \tag{3}$$

Because the value of V_{REF} is 1.2 V, this relationship reduces to:

$$V_N(\mu V_{RMS}) = 27\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V)$$

where

- C_{NR} does not exist (4)

An internal 27-kΩ resistor in series with the noise reduction pin (NR) forms a low-pass filter for the voltage reference when an external noise reduction capacitor, C_{NR}, is connected from NR to ground. For C_{NR} = 10 nF, the total noise in the 10-Hz to 100-kHz bandwidth is reduced by a factor of approximately 3.2, giving the approximate relationship:

$$V_N(\mu V_{RMS}) = 8.5\left(\frac{\mu V_{RMS}}{V}\right) \times V_{OUT}(V)$$

where

- C_{NR} = 10 nF (5)

This noise reduction effect is shown as *RMS Noise Voltage vs C_{NR}* in *Typical Characteristics*.

The TPS73201-Q1 adjustable version does not have the noise-reduction pin available. However, connecting a feedback capacitor, C_{FB}, from the output to the FB pin will reduce output noise and improve load transient performance.

The TPS732-Q1 family of devices uses an internal charge pump to develop an internal supply voltage sufficient to drive the gate of the NMOS pass element above V_{OUT}. The charge pump generates approximately 250 µV of switching noise at approximately 2 MHz; however, charge-pump noise contribution is negligible at the output of the regulator for most values of I_{OUT} and C_{OUT}.

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8.2.3 Application Curves

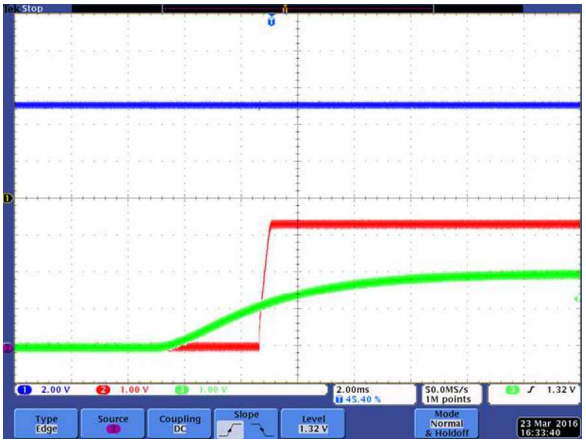


Figure 32. Start-Up

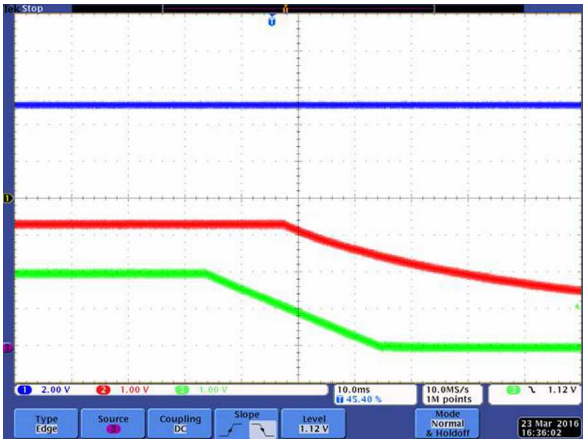


Figure 33. Shutdown

9 Power Supply Recommendations

These devices are designed to operate from an input voltage supply range from 1.7 V to 5.5 V. The input voltage range provides adequate headroom for the device to have a regulated output. This input supply must be well regulated. If the input supply is noisy, additional input capacitors with low ESR can help improve the output noise performance.

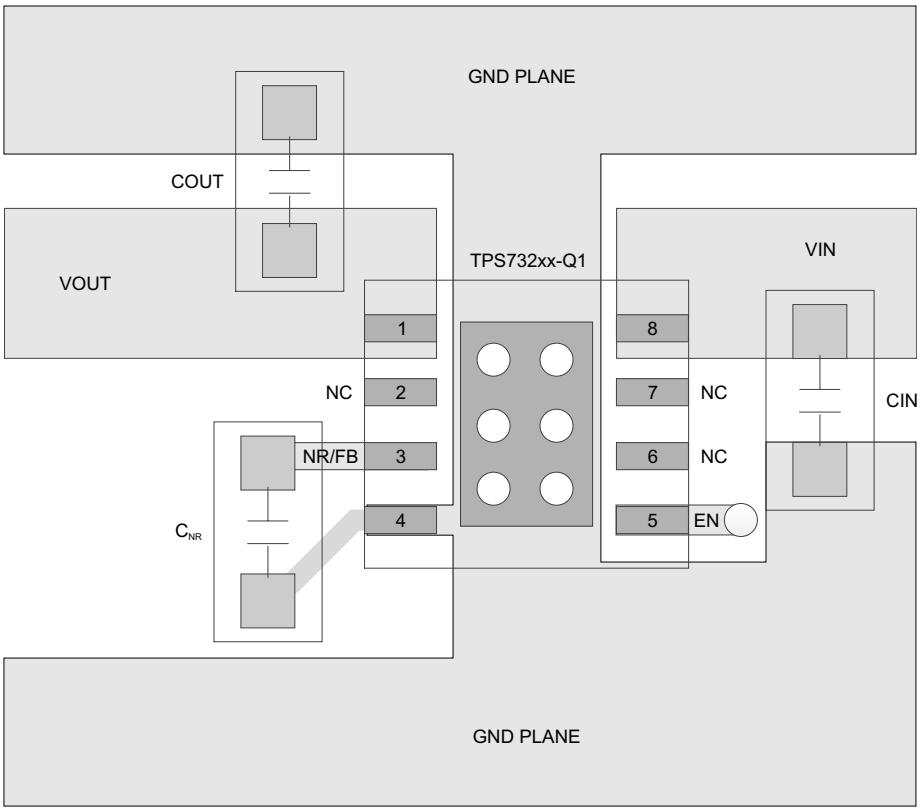
10 Layout

10.1 Layout Guidelines

To improve ac performance such as PSRR, output noise, and transient response, TI recommends designing the PCB with separate ground planes for V_{IN} and V_{OUT}, with each ground plane connected only at the GND pin of the device. In addition, the ground connection for the bypass capacitor should connect directly to the GND pin of the device.

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10.2 Layout Example



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Figure 34. Layout Diagram

10.3 Power Dissipation

The ability to remove heat from the die is different for each package type, presenting different considerations in the PCB layout. The PCB area around the device that is free of other components moves the heat from the device to the ambient air. Using heavier copper will increase the effectiveness in removing heat from the device. The addition of plated through-holes to heat-dissipating layers will also improve the heat-sink effectiveness.

Power dissipation depends on input voltage and load conditions. Power dissipation is equal to the product of the output current times the voltage drop across the output pass element (V_{IN} to V_{OUT}):

$$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (6)$$

Power dissipation can be minimized by using the lowest possible input voltage necessary to assure the required output voltage.

10.4 Package Mounting

Solder pad footprint recommendations for the TPS732-Q1 family of devices are presented in the *Solder Pad Recommendations for Surface-Mount Devices* (SBFA015) application bulletin.

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11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

Solder Pad Recommendations for Surface-Mount Devices, SBFA015

11.2 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.3 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.4 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS73201QDBVRQ1	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PJOQ	Samples
TPS73201QDRBRQ1	ACTIVE	SON	DRB	8	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	PSAQ	Samples
TPS73218QDCQRQ1	ACTIVE	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	73218Q	Samples
TPS73250QDCQRQ1	LIFEBUY	SOT-223	DCQ	6	2500	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	73250Q	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS732-Q1 :

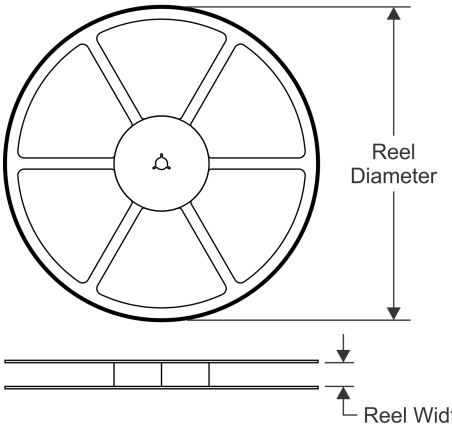
- Catalog : TPS732

NOTE: Qualified Version Definitions:

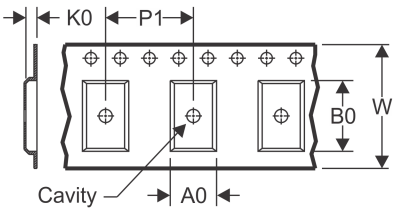
- Catalog - TI's standard catalog product

TAPE AND REEL INFORMATION

REEL DIMENSIONS

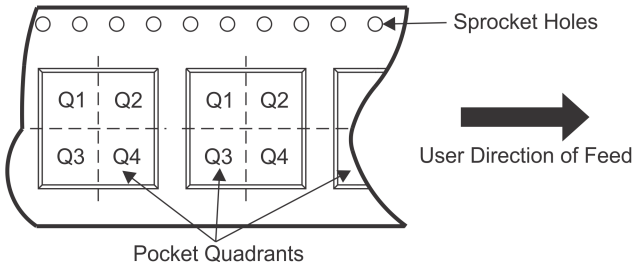


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

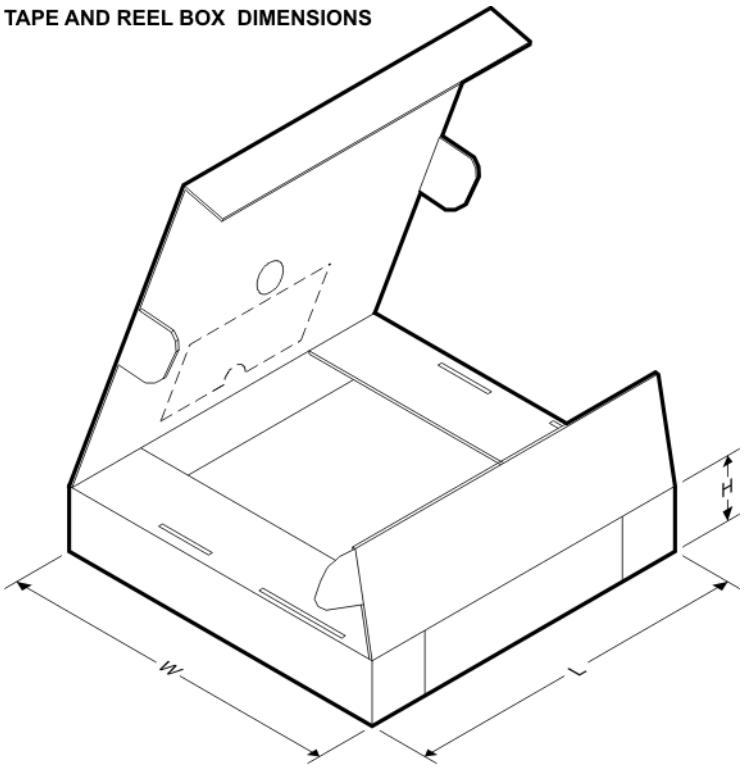
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS73201QDBVRQ1	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS73201QDRBRQ1	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPS73218QDCQRQ1	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3
TPS73250QDCQRQ1	SOT-223	DCQ	6	2500	330.0	12.4	7.1	7.45	1.88	8.0	12.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

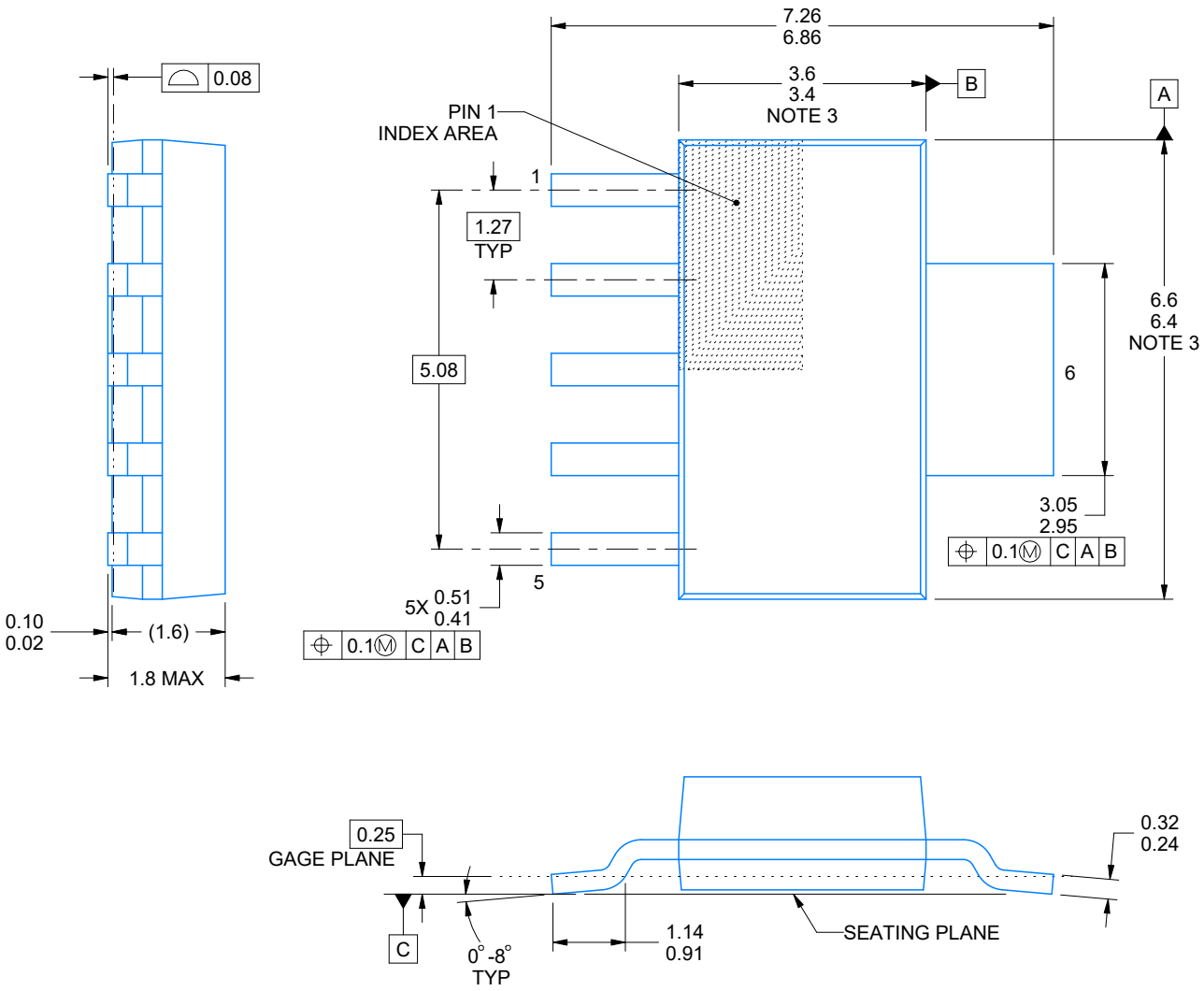
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS73201QDBVRQ1	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS73201QDRBRQ1	SON	DRB	8	3000	367.0	367.0	35.0
TPS73218QDCQRQ1	SOT-223	DCQ	6	2500	346.0	346.0	29.0
TPS73250QDCQRQ1	SOT-223	DCQ	6	2500	346.0	346.0	29.0

PACKAGE OUTLINE

DCQ0006A

SOT - 1.8 mm max height

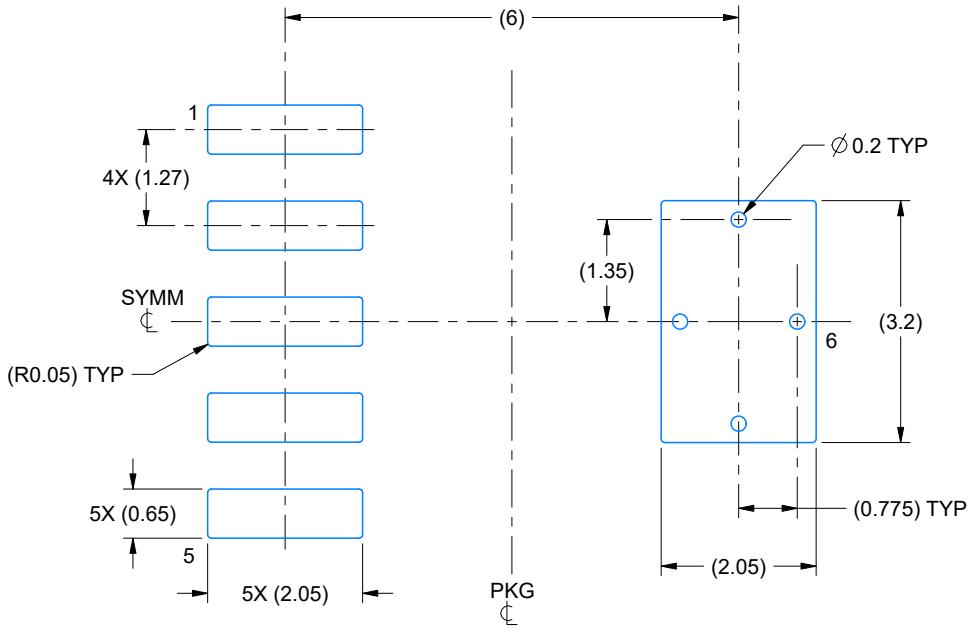
PLASTIC SMALL OUTLINE



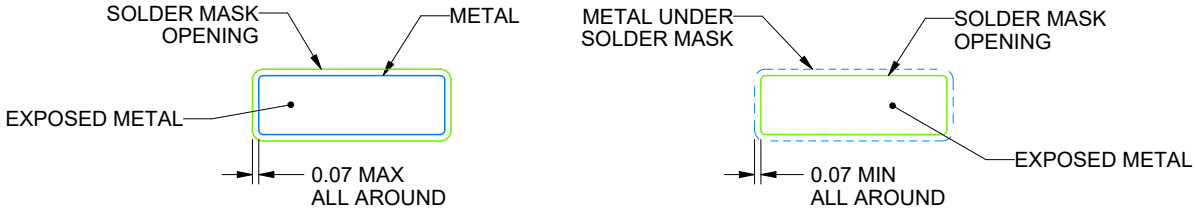
4214845/C 11/2021

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

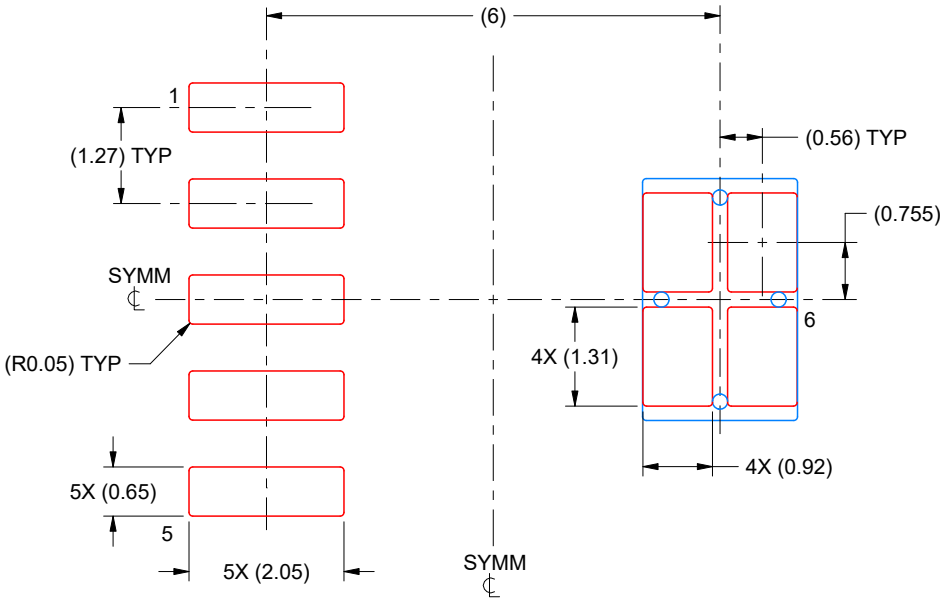


SOLDER MASK DETAILS

4214845/C 11/2021

NOTES: (continued)

4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
6. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214845/C 11/2021

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

DRB 8

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

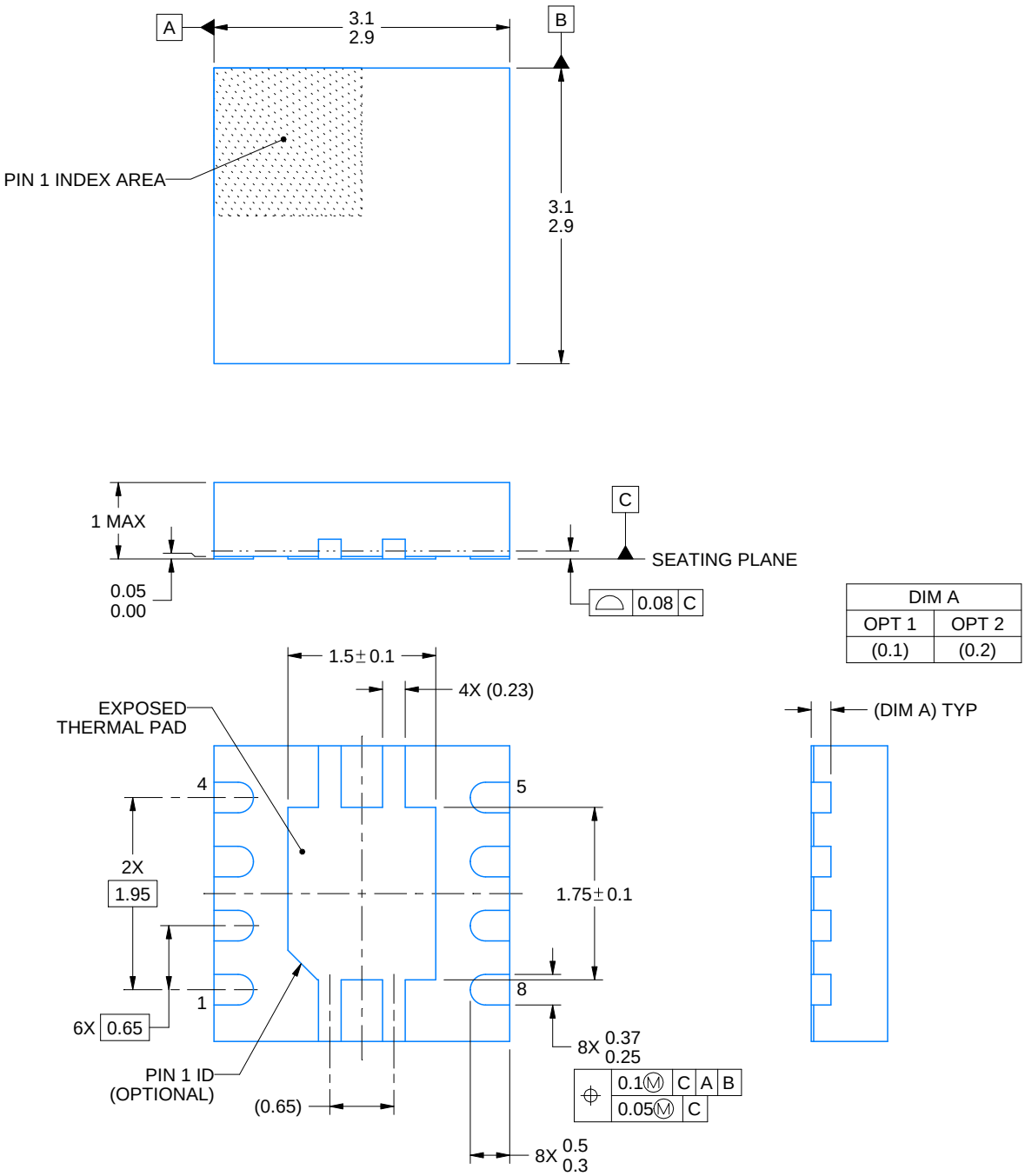
4203482/L

PACKAGE OUTLINE

DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



NOTES:

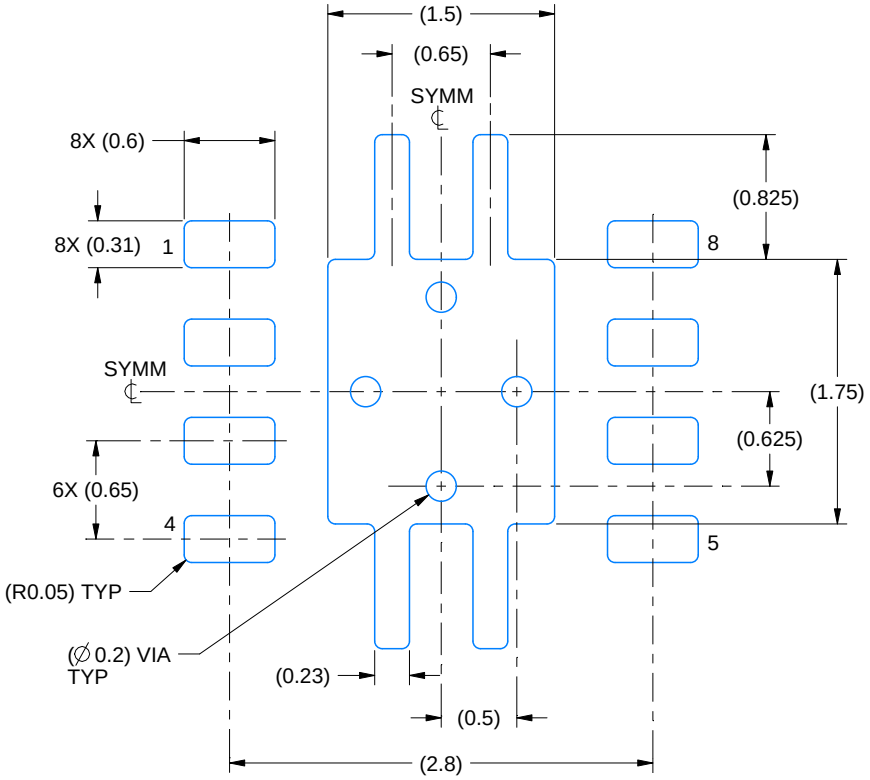
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

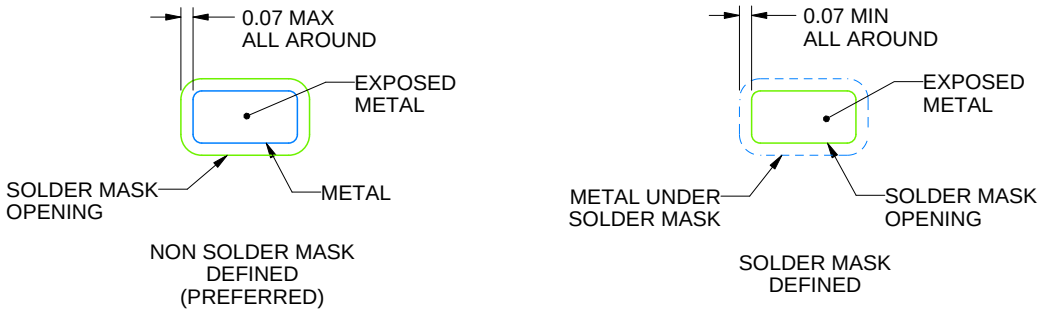
DRB0008A

VSON - 1 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X

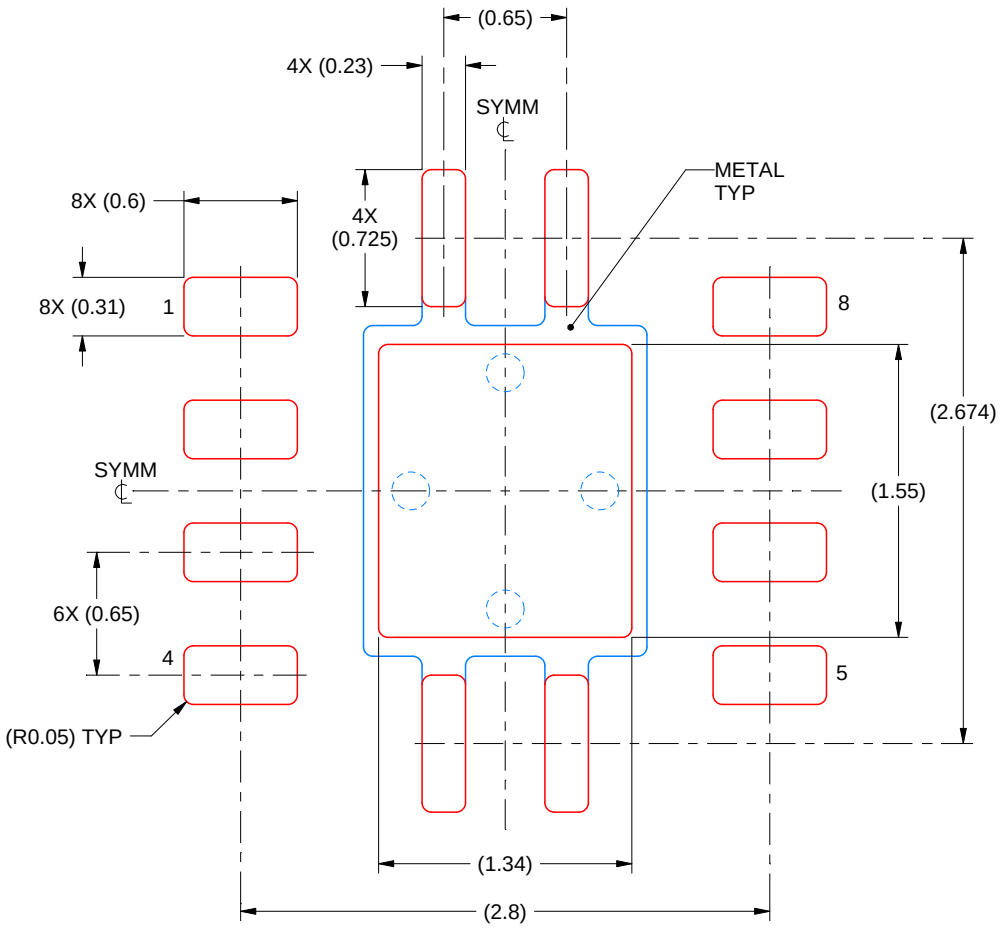


SOLDER MASK DETAILS

4218875/A 01/2018

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD
84% PRINTED SOLDER COVERAGE BY AREA
SCALE:25X

4218875/A 01/2018

NOTES: (continued)

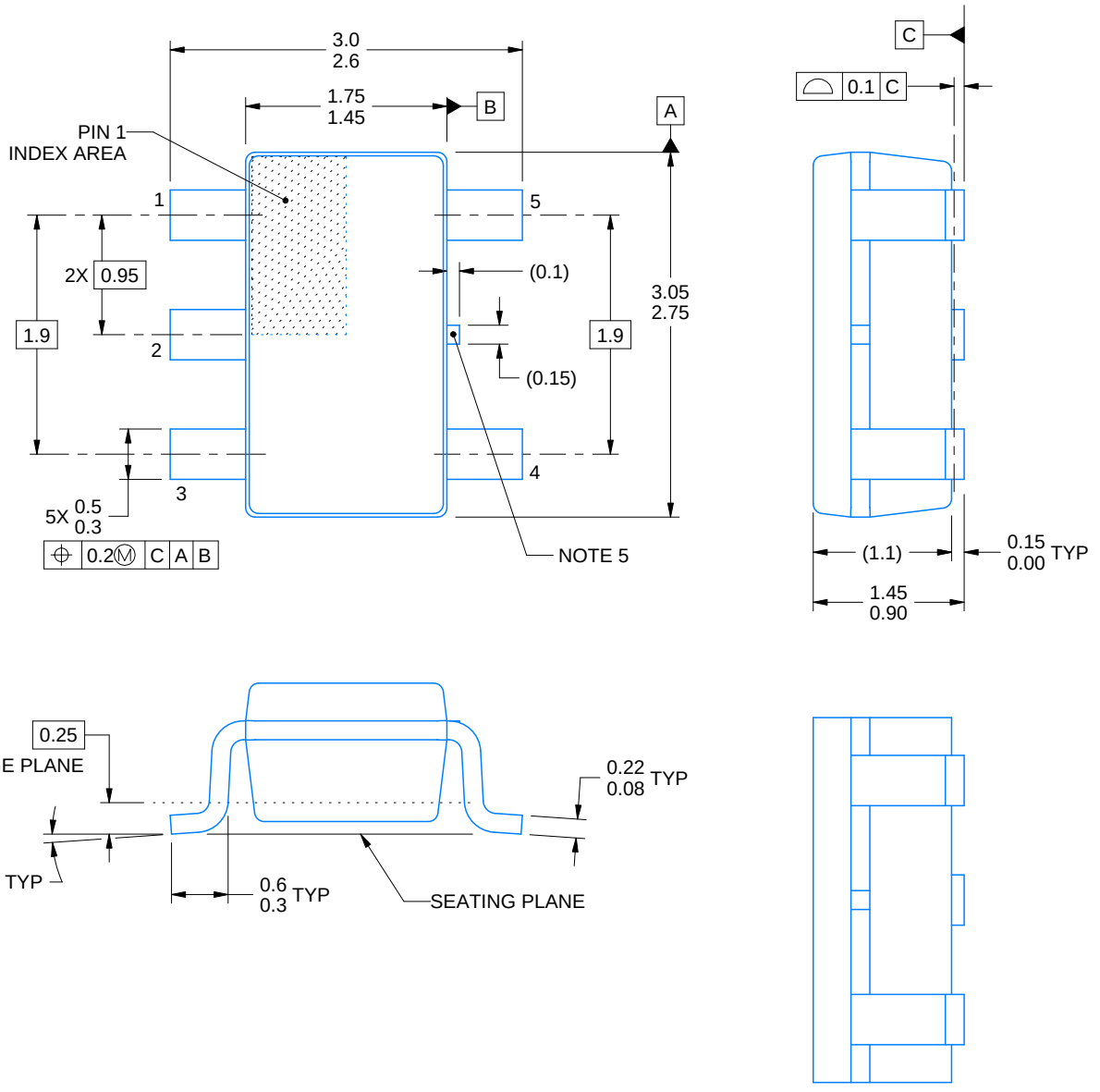
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

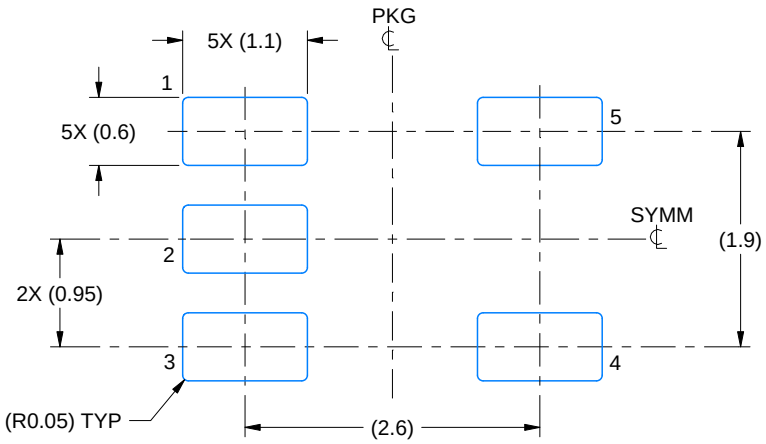


ALTERNATIVE PACKAGE SINGULATION VIEW

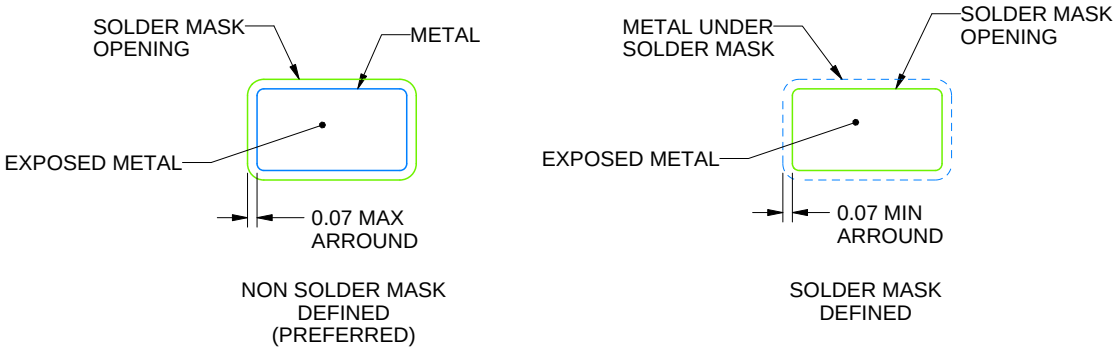
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

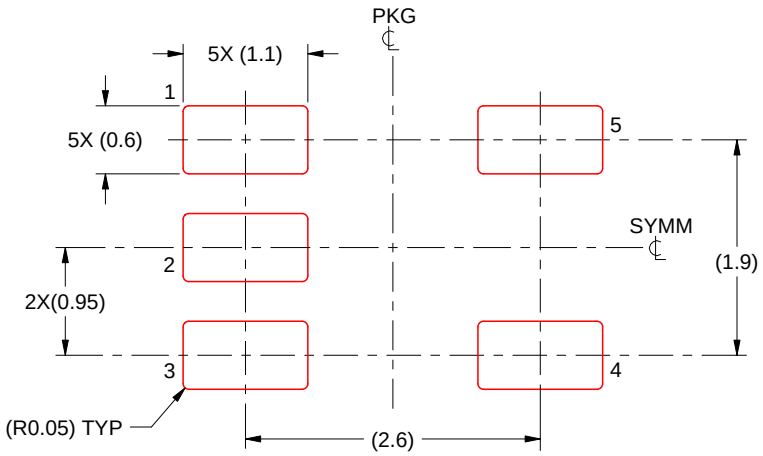


SOLDER MASK DETAILS

4214839/J 02/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/J 02/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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