TPS763 低消費電力、150mA、低ドロップアウト・リニア・レギュレータ

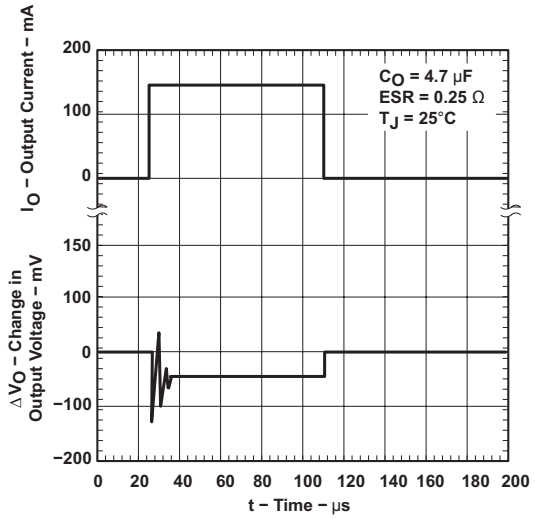
1 特長

- 150mA の低ドロップアウト・レギュレータ
- 出力電圧：5V、3.8V、3.3V、3V、2.8V、2.7V、2.5V、1.8V、1.6V、可変
- ドロップアウト電圧：300mV (標準値、150mA の場合)
- 過熱保護機能
- 過電流制限
- シャットダウン時の静止電流：2µA 未満
- 動作時の接合部温度範囲：-40℃～125℃
- 5 ピン SOT-23 (DBV) パッケージ

2 アプリケーション

- 電気メータ
- 太陽光インバータ
- HVAC システム
- サーボ・ドライブおよびモーション・コントロール
- センサ・トランスミッタ

TPS76350 の負荷過渡応答



3 概要

TPS763xx ファミリの低ドロップアウト (LDO) 電圧レギュレータは、低ドロップアウト電圧、低消費電力動作、小型パッケージという利点を兼ね備えています。これらのレギュレータは、従来型の LDO レギュレータと比べてドロップアウト電圧が低く、静止電流が小さいことが特長です。5 ピンの小型 SOT-23 集積回路パッケージで提供する TPS763xx シリーズのデバイスは、コスト制約の厳しい設計や基板スペースを重視するアプリケーションに理想的です。

新しい回路設計と革新的なプロセスの組み合わせにより、通常の PNP パス・トランジスタを PMOS パス素子に置き換えることができました。PMOS パス素子は低抵抗として振る舞うため、ドロップアウト電圧は低く (TPS76333 の場合、負荷電流 150mA で標準値 300mV)、負荷電流に正比例します。PMOS パス素子は電圧駆動デバイスであるため、静止電流は小さく (140µA 以下)、出力負荷電流 (0mA～150mA) の全範囲にわたって安定しています。ノートPCや携帯電話などの携帯型システムでの使用を意図した低ドロップアウト電圧特性と低消費電力動作により、システムのバッテリ動作時間を大幅に伸ばすことができます。

TPS763xx は、レギュレータをシャットダウンするためのロジック制御のスリープ・モードも備えており、静止電流を 1µA 以下 (T_J = 25℃時) に低減できます。TPS763xx には 1.6V、1.8V、2.5V、2.7V、2.8V、3V、3.3V、3.8V、5V の固定電圧バージョンと可変バージョン (1.5V～6.5V の範囲でプログラム可能) があります。

製品情報(1)

型番	パッケージ	本体サイズ (公称)
TPS763xx	SOT-23 (5)	2.90mm×1.60mm

(1) 提供されているすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision I (December 2016) から **Revision J** に変更 **Page**

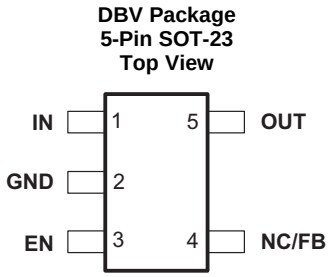
- Changed minimum specification from 4.75 V to 4.85 V in V_O parameter for TPS76350, I_O = 1 mA to 150 mA row in *Electrical Characteristics* table ... 5

Revision H (January 2004) から **Revision I** に変更 **Page**

- 「*ESD 定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1
- 「*アプリケーション*」からレガシー・アプリケーションとセラミック以外のコンデンサでの安定性を 削除 ... 1
- 「*アプリケーション*」に電気メータ、太陽光インバータ、HVAC システム、サーボ・ドライブおよびモーション・コントロール、センサ・トランスミッタを 追加 ... 1
- Deleted *Dissipation Ratings* table ... 3
- Added *Thermal Information* table ... 4

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5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	IN	I	Input supply voltage
2	GND	—	Ground
3	EN	I	Enable input
4	NC/FB	—/I	No connection (fixed-voltage option only) or feedback voltage (TPS76301 only)
5	OUT	O	Regulated output voltage

6 Specifications

7 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Input voltage	–0.3	10	V
Voltage at EN	–0.3	V_I + 0.3	V
Voltage on OUT, FB		7	V
Peak output current	Internally limited		
Operating junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

8 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±250	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

9 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	MAX	UNIT
V_I	Input voltage(1)	2.7	10	V
I_O	Continuous output current	0	150	mA
T_J	Operating junction temperature	–40	125	°C

(1) To calculate the minimum input voltage for your maximum output current, use the following equation: $V_{I(min)} = V_{O(max)} + V_{DO(max\ load)}$

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10 Thermal Information

THERMAL METRIC(1)		TPS763xx DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	205.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	125.1	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	34.6	°C/W
ψ_{JT}	Junction-to-top characterization parameter	15.2	°C/W
ψ_{JB}	Junction-to-board characterization parameter	33.8	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

11 Electrical Characteristics

over recommended operating free-air temperature range, $V_I = V_{O(typ)} + 1$ V, $I_O = 1$ mA, EN = IN, and $C_O = 4.7$ µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage	TPS76301	3.25 V > V_I ≥ 2.7 V, 2.5 V ≥ V_O ≥ 1.5 V, I_O = 1 mA to 75 mA, T_J = 25°C	0.98 × V_O	V_O	1.02 × V_O	V
			3.25 V > V_I ≥ 2.7 V, 2.5 V ≥ V_O ≥ 1.5 V, I_O = 1 mA to 75 mA	0.97 × V_O	V_O	1.03 × V_O	
			V_I ≥ 3.25 V, 5 V ≥ V_O ≥ 1.5 V, I_O = 1 mA to 100 mA, T_J = 25°C	0.98 × V_O	V_O	1.02 × V_O	
			V_I ≥ 3.25 V, 5 V ≥ V_O ≥ 1.5 V, I_O = 1 mA to 100 mA	0.97 × V_O	V_O	1.03 × V_O	
			V_I ≥ 3.25 V, 5 V ≥ V_O ≥ 1.5 V, I_O = 1 mA to 150 mA, T_J = 25°C	0.975 × V_O	V_O	1.025 × V_O	
			V_I ≥ 3.25 V, 5 V ≥ V_O ≥ 1.5 V, I_O = 1 mA to 150 mA	0.9625 × V_O	V_O	1.0375 × V_O	
		TPS76316	V_I = 2.7 V, 1 mA < I_O < 75 mA, T_J = 25°C	1.568	1.6	1.632	
			V_I = 2.7 V, 1 mA < I_O < 75 mA	1.552	1.6	1.648	
			V_I = 3.25 V, 1 mA < I_O < 100 mA, T_J = 25°C	1.568	1.6	1.632	
			V_I = 3.25 V, 1 mA < I_O < 100 mA	1.552	1.6	1.648	
			V_I = 3.25 V, 1 mA < I_O < 150 mA, T_J = 25°C	1.56	1.6	1.64	
			V_I = 3.25 V, 1 mA < I_O < 150 mA	1.536	1.6	1.664	
		TPS76318	V_I = 2.7 V, 1 mA < I_O < 75 mA, T_J = 25°C	1.764	1.8	1.836	
			V_I = 2.7 V, 1 mA < I_O < 75 mA	1.746	1.8	1.854	
			V_I = 3.25 V, 1 mA < I_O < 100 mA, T_J = 25°C	1.764	1.8	1.836	
			V_I = 3.25 V, 1 mA < I_O < 100 mA	1.746	1.8	1.854	
			V_I = 3.25 V, 1 mA < I_O < 150 mA, T_J = 25°C	1.755	1.8	1.845	
			V_I = 3.25 V, 1 mA < I_O < 150 mA	1.733	1.8	1.867	

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Electrical Characteristics (continued)

over recommended operating free-air temperature range, $V_I = V_{O(typ)} + 1$ V, $I_O = 1$ mA, EN = IN, and $C_O = 4.7$ µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
V_O	Output voltage (continued)	TPS76325	I_O = 1 mA to 100 mA, T_J = 25°C	2.45	2.5	2.55	V
			I_O = 1 mA to 100 mA	2.425	2.5	2.575	
			I_O = 1 mA to 150 mA, T_J = 25°C	2.438	2.5	2.562	
			I_O = 1 mA to 150 mA	2.407	2.5	2.593	
		TPS76327	I_O = 1 mA to 100 mA, T_J = 25°C	2.646	2.7	2.754	
			I_O = 1 mA to 100 mA	2.619	2.7	2.781	
			I_O = 1 mA to 150 mA, T_J = 25°C	2.632	2.7	2.767	
			I_O = 1 mA to 150 mA	2.599	2.7	2.801	
		TPS76328	I_O = 1 mA to 100 mA, T_J = 25°C	2.744	2.8	2.856	
			I_O = 1 mA to 100 mA	2.716	2.8	2.884	
			I_O = 1 mA to 150 mA, T_J = 25°C	2.73	2.8	2.87	
			I_O = 1 mA to 150 mA	2.695	2.8	2.905	
		TPS76330	I_O = 1 mA to 100 mA, T_J = 25°C	2.94	3	3.06	
			I_O = 1 mA to 100 mA	2.91	3	3.09	
			I_O = 1 mA to 150 mA, T_J = 25°C	2.925	3	3.075	
			I_O = 1 mA to 150 mA	2.888	3	3.112	
		TPS76333	I_O = 1 mA to 100 mA, T_J = 25°C	3.234	3.3	3.366	
			I_O = 1 mA to 100 mA	3.201	3.3	3.399	
			I_O = 1 mA to 150 mA, T_J = 25°C	3.218	3.3	3.382	
			I_O = 1 mA to 150 mA	3.177	3.3	3.423	
		TPS76338	I_O = 1 mA to 100 mA, T_J = 25°C	3.724	3.8	3.876	
			I_O = 1 mA to 100 mA	3.705	3.8	3.895	
			I_O = 1 mA to 150 mA, T_J = 25°C	3.686	3.8	3.914	
			I_O = 1 mA to 150 mA	3.667	3.8	3.933	
		TPS76350	I_O = 1 mA to 100 mA, T_J = 25°C	4.875	5	5.125	
			I_O = 1 mA to 100 mA	4.825	5	5.175	
			I_O = 1 mA to 150 mA, T_J = 25°C	4.85	5	5.15	
			I_O = 1 mA to 150 mA	4.8	5	5.2	
$I_{(Q)}$	Quiescent current (GND pin current)	I_O = 1 mA to 150 mA, T_J = 25°C(1)			85	100	µA
		I_O = 1 mA to 150 mA(2)				140	
	Standby current	EN < 0.5 V, T_J = 25°C			0.5	1	µA
		EN < 0.5 V				2	
V_n	Output noise voltage	BW = 300 Hz to 50 kHz, T_J = 25°C, C_O = 10 µF(2)			140		µV
PSRR	Ripple rejection	f = 1 kHz, C_O = 10 µF, T_J = 25°C(2)			60		dB
	Current limit	T_J = 25°C(3)		0.5	0.8	1.5	A
	Output voltage line regulation ($\Delta V_O/V_O$)(3)	V_O + 1 V < V_I ≤ 10 V, V_I ≥ 3.5 V, T_J = 25°C			0.04%	0.07%	V
		V_O + 1 V < V_I ≤ 10 V, V_I ≥ 3.5 V				0.1%	
V_{IH}	EN high level input(2)				1.4	2	V
V_{IL}	EN low level input(2)			0.5	1.2		V

(1) Minimum IN operating voltage is 2.7 V or $V_{O(typ)}$ + 1 V, whichever is greater.

(2) Test conditions includes output voltage V_O = 0 V (for variable device FB is shorted to V_O), and pulse duration = 10 mS.

(3) If V_O < 2.5 V and V_{Imax} = 10 V, V_{Imin} = 3.5 V:

$$\text{Line Reg. (mV)} = (\%/\text{V}) \times \frac{V_O(V_{Imax} - 3.5\ \text{V})}{100} \times 1000$$

If V_O > 2.5 V and V_{Imax} = 10 V, V_{Imin} = VO + 1 V:

$$\text{Line Reg. (mV)} = (\%/\text{V}) \times \frac{V_O(V_{Imax} - (V_O + 1))}{100} \times 1000$$

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Electrical Characteristics (continued)

over recommended operating free-air temperature range, $V_I = V_{O(typ)} + 1$ V, $I_O = 1$ mA, EN = IN, and $C_O = 4.7$ µF (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
I_I	EN input current	EN = 0 V			–0.01	–0.5	µA
		EN = IN			–0.01	–0.5	
V_{DO}	Dropout voltage	TPS76325	I_O = 0 mA, T_J = 25°C		0.2		mV
			I_O = 1 mA, T_J = 25°C		3		
			I_O = 50 mA, T_J = 25°C		120	150	
			I_O = 50 mA			200	
			I_O = 75 mA, T_J = 25°C		180	225	
			I_O = 75 mA			300	
			I_O = 100 mA, T_J = 25°C		240	300	
			I_O = 100 mA			400	
			I_O = 150 mA, T_J = 25°C		360	450	
			I_O = 150 mA			600	
		TPS76333	I_O = 0 mA, T_J = 25°C		0.2		
			I_O = 1 mA, T_J = 25°C		3		
			I_O = 50 mA, T_J = 25°C		100	125	
			I_O = 50 mA			166	
			I_O = 75 mA, T_J = 25°C		150	188	
			I_O = 75 mA			250	
			I_O = 100 mA, T_J = 25°C		200	250	
			I_O = 100 mA			333	
			I_O = 150 mA, T_J = 25°C		300	375	
			I_O = 150 mA			500	
		TPS76350	I_O = 0 mA, T_J = 25°C		0.2		
			I_O = 1 mA, T_J = 25°C		2		
			I_O = 50 mA, T_J = 25°C		60	75	
			I_O = 50 mA			100	
			I_O = 75 mA, T_J = 25°C		90	113	
			I_O = 75 mA			150	
			I_O = 100 mA, T_J = 25°C		120	150	
			I_O = 100 mA			200	
			I_O = 150 mA, T_J = 25°C		180	225	
			I_O = 150 mA			300	

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11.1 Typical Characteristics

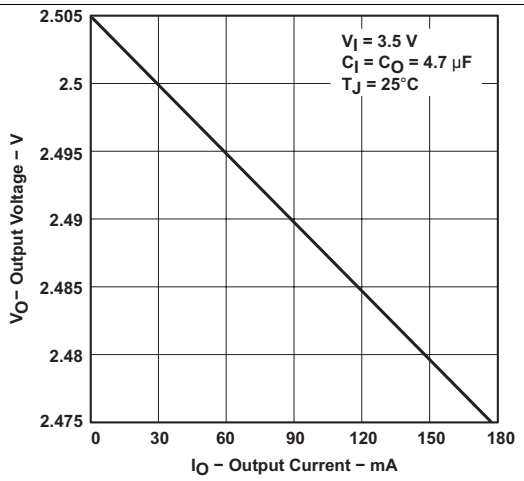


Figure 1. TPS76325 Output Voltage vs Output Current

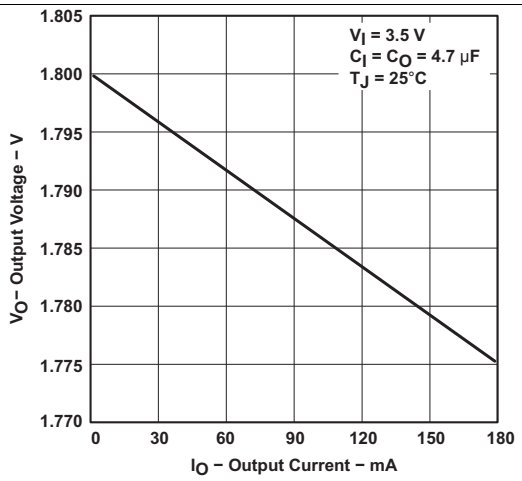


Figure 2. TPS76318 Output Voltage vs Output Current

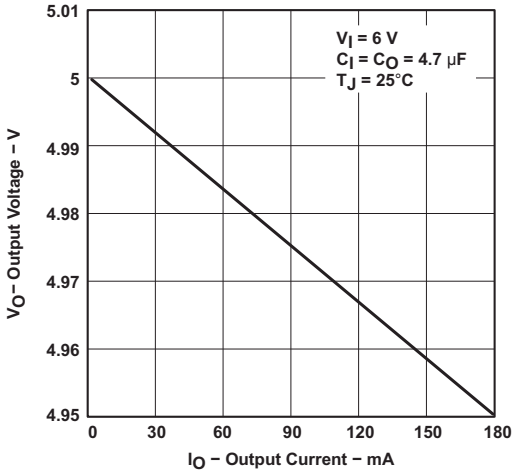


Figure 3. TPS76350 Output Voltage vs Output Current

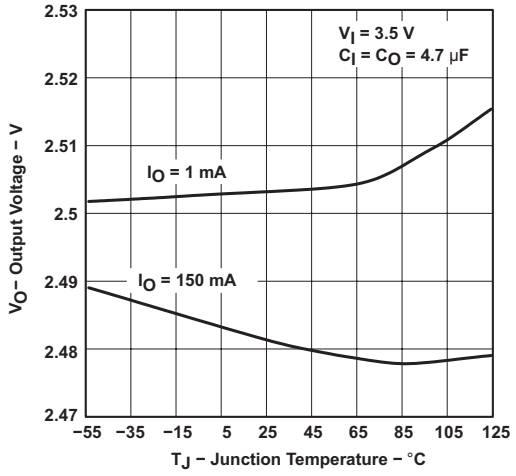


Figure 4. TPS76325 Output Voltage vs Output Current

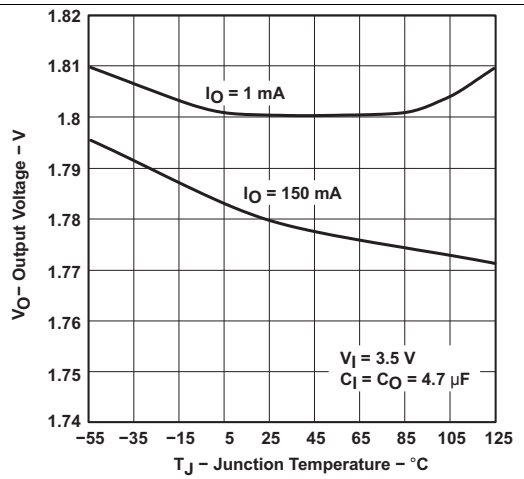


Figure 5. TPS76318 Output Voltage vs Free-Air Temperature

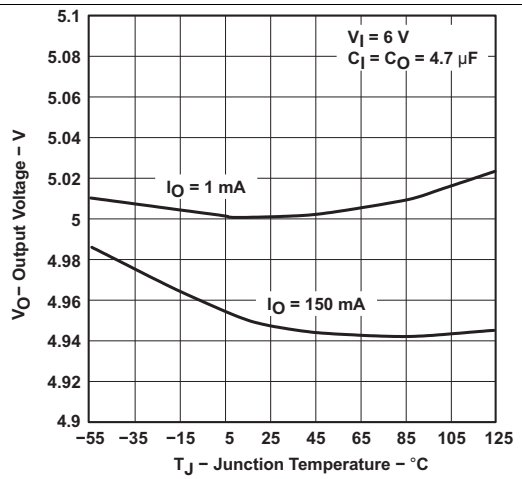


Figure 6. TPS76350 Output Voltage vs Free-Air Temperature

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Typical Characteristics (continued)

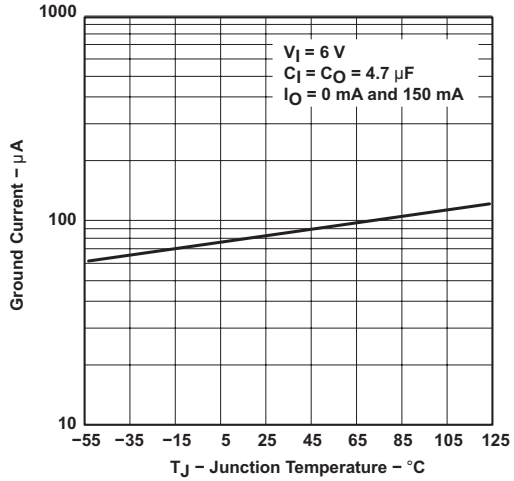


Figure 7. TPS76350 Ground Current vs Free-Air Temperature

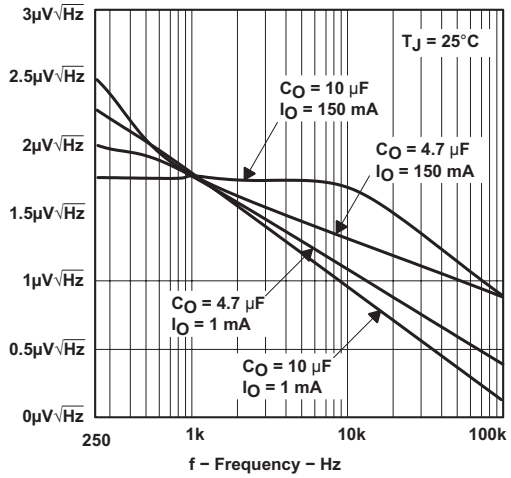


Figure 8. Output Noise vs Frequency

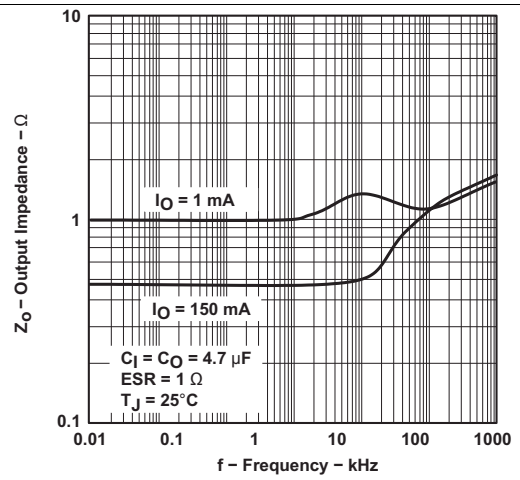


Figure 9. Output Impedance vs Frequency

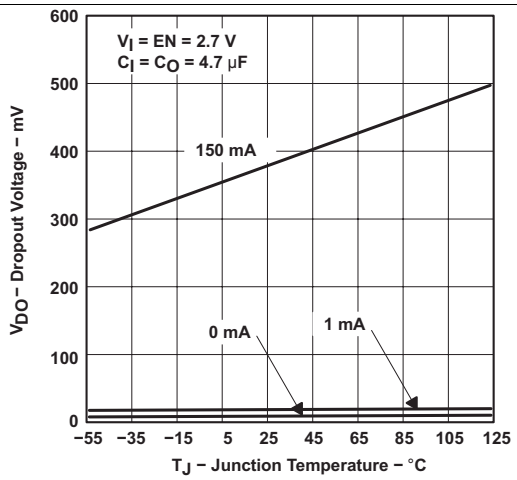


Figure 10. TPS76325 Dropout Voltage vs Free-Air Temperature

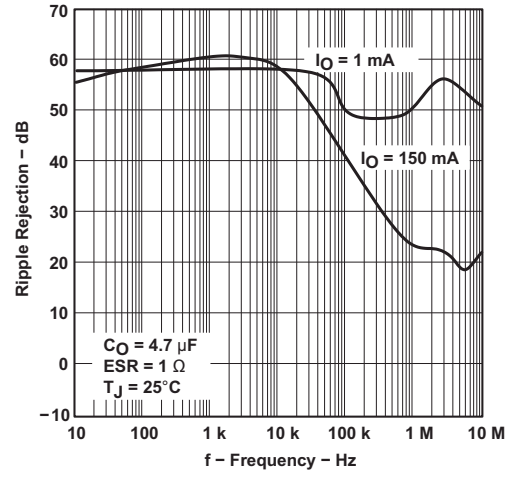


Figure 11. TPS76325 Ripple Rejection vs Frequency

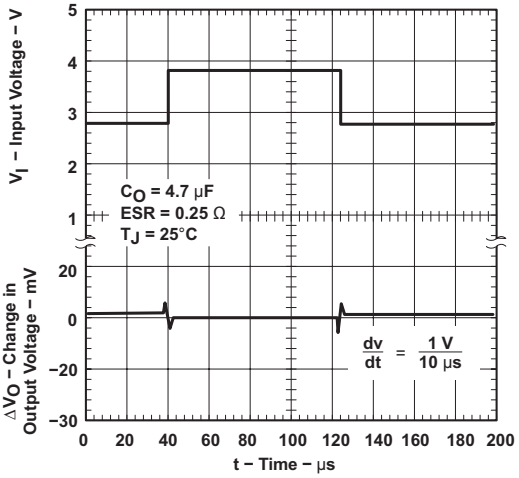


Figure 12. TPS76318 Line Transient Response

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Typical Characteristics (continued)

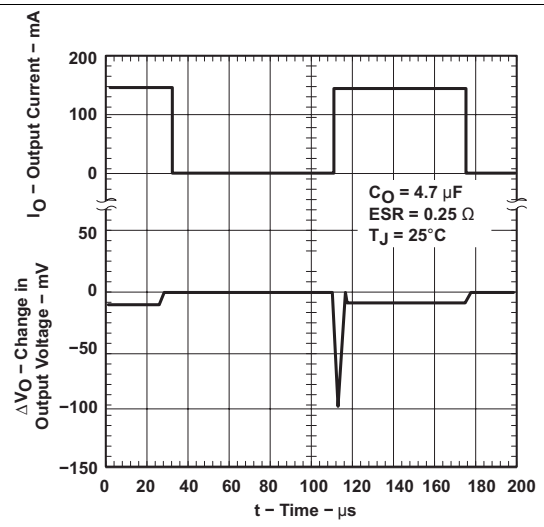


Figure 13. TPS76318 Load Transient Response

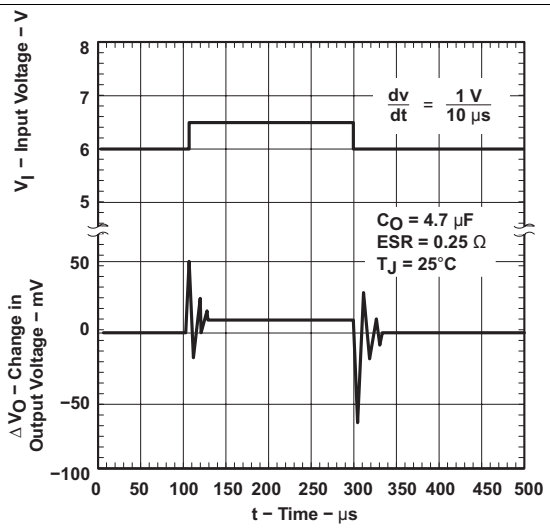


Figure 14. TPS76350 Line Transient Response

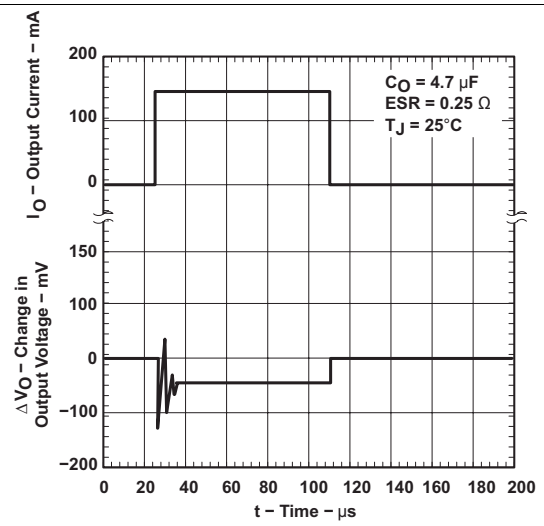


Figure 15. TPS76350 Load Transient Response

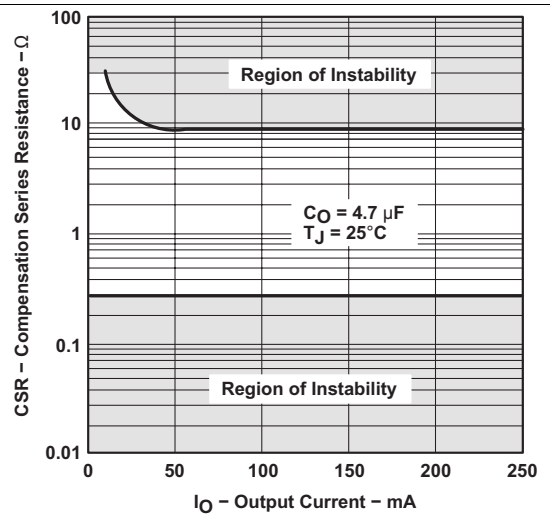


Figure 16. Compensation Series Resistance (CSR) vs Output Current

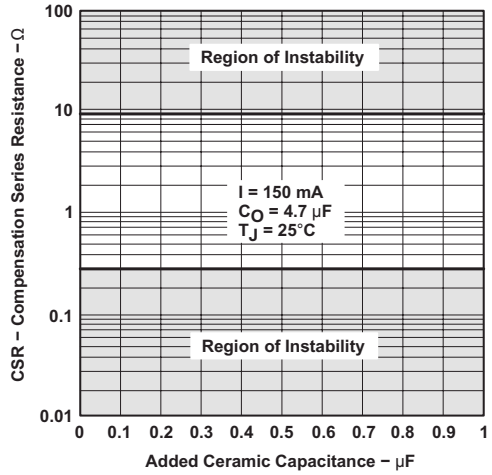


Figure 17. Compensation Series Resistance (CSR) vs Added Ceramic Capacitance

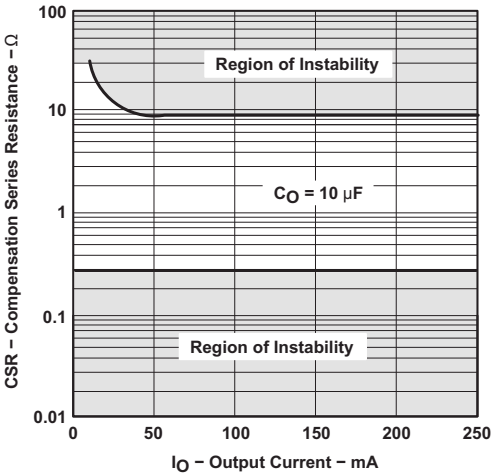


Figure 18. Compensation Series Resistance (CSR) vs Output Current

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Typical Characteristics (continued)

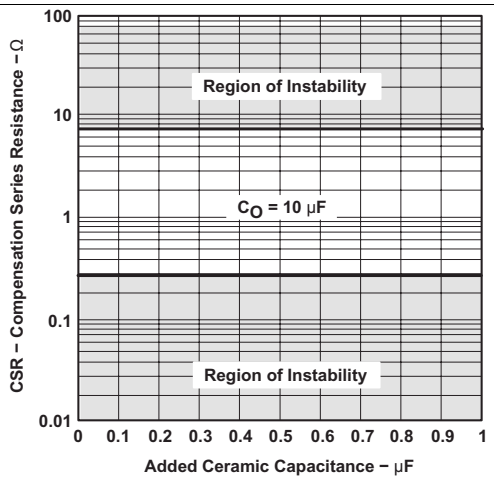


Figure 19. Compensation Series Resistance (CSR) vs Added Ceramic Capacitance

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12 Detailed Description

12.1 Overview

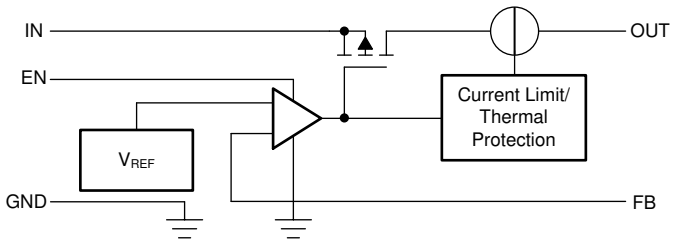
The TPS763xx devices uses a PMOS pass element to dramatically reduce both dropout voltage and supply current over more conventional PNP pass element LDO designs. The PMOS pass element is a voltage-controlled device that, unlike a PNP transistor, does not require increased drive current as output current increases. Supply current in the TPS763xx is essentially constant from no-load to maximum load.

Current limiting and thermal protection prevent damage by excessive output current and/or power dissipation. The device switches into a constant-current mode at approximately 1 A; further load reduces the output voltage instead of increasing the output current. The thermal protection shuts the regulator off if the junction temperature rises above 165°C. Recovery is automatic when the junction temperature drops approximately 25°C below the high temperature trip point. The PMOS pass element includes a back diode that safely conducts reverse current when the input voltage level drops below the output voltage level.

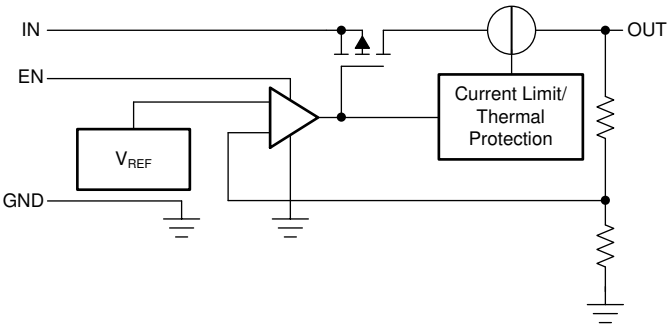
A logic low on the enable input, EN shuts off the output and reduces the supply current to less than 2 µA. EN must be tied high in applications where the shutdown feature is not used.

12.2 Functional Block Diagram

TPS76301



TPS76316/ 18/ 25/ 27/ 28/ 30/ 33/ 38/ 50



12.3 Feature Description

12.3.1 Regulator Protection

The TPS763xx features internal current limiting and thermal protection. During normal operation, the TPS763xx limits output current to approximately 800 mA. When current limiting engages, the output voltage scales back linearly until the overcurrent condition ends. While current limiting is designed to prevent gross device failure, take care not to exceed the power dissipation ratings of the package. If the temperature of the device exceeds 165°C, thermal-protection circuitry shuts it down. Once the device has cooled down to below 140°C, regulator operation resumes.

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Feature Description (continued)

12.3.2 Enable

The enable signal (V_{EN}) is an active-high digital control that enables the LDO when the enable voltage is past the rising threshold ($V_{EN} \geq V_{IH(EN)}$) and disables the LDO when the enable voltage is below the falling threshold ($V_{EN} \leq V_{IL(EN)}$). The exact enable threshold is between $V_{IH(EN)}$ and $V_{IL(EN)}$ because EN is a digital control. In applications that do not use the enable control, connect EN to V_{IN}.

12.4 Device Functional Modes

Table 1 provides a quick comparison between the regulation and disabled operation.

Table 1. Device Functional Modes Comparison

OPERATING MODE	PARAMETER			
	V_{IN}	EN	I_{OUT}	T_J
Regulation(1)	$V_{IN} > V_{OUT(nom)} + V_{DO}$	$V_{EN} > V_{IH(EN)}$	$I_{OUT} < I_{CL}$	$T_J < T_{sd}$
Disabled(2)	—	$V_{EN} < V_{IL(EN)}$	—	$T_J > T_{sd}$

(1) All table conditions must be met.
(2) The device is disabled when any condition is met.

12.4.1 Regulation

The device regulates the output to the targeted output voltage when all the conditions in Table 1 are met.

12.4.2 Disabled

When disabled, the pass device is turned off, the internal circuits are shutdown.

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13 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

13.1 Application Information

The TPS763xx low-dropout (LDO) regulators are part of a family of regulators which have been optimized for use in battery-operated equipment and feature extremely low dropout voltages, low quiescent current (140 µA), and an enable input to reduce supply currents to less than 2 µA when the regulator is turned off.

13.2 Typical Application

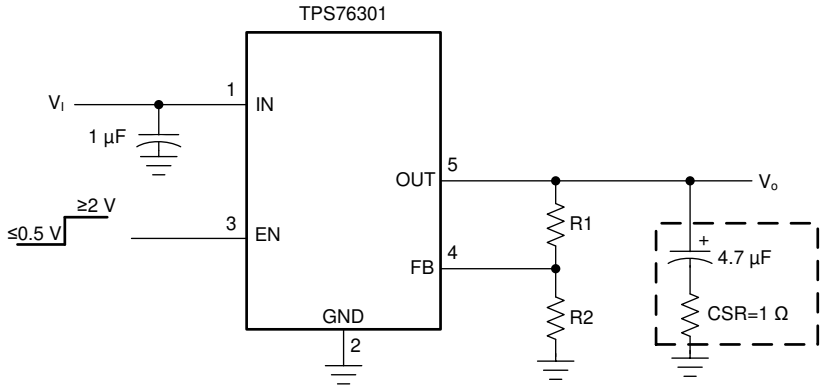


Figure 20. Typical Application Circuit

13.2.1 Design Requirements

Although not required, TI recommends a 0.047-µF or larger ceramic bypass input capacitor, connected between IN and GND and placed close to the TPS763xx, to improve transient response and noise rejection. A higher-value electrolytic input capacitor may be necessary if large, fast-rise-time load transients are anticipated and the device is placed several inches from the power source. Follow the programming guidelines from Table 2.

Table 2. Output Voltage Programming Guide

OUTPUT VOLTAGE (V)	DIVIDER RESISTANCE (kΩ)(1)	
	R1	R2
2.5	187	169
3.3	301	169
3.6	348	169
4	402	169
5	549	169
6.45	750	169

(1) 1% values shown

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13.2.2 Detailed Design Procedure

13.2.2.1 Capacitor Selection

Like all low dropout regulators, the TPS763xx requires an output capacitor connected between OUT and GND to stabilize the internal loop control. The minimum recommended capacitance value is 4.7 µF and the ESR (equivalent series resistance) must be between 0.3 Ω and 10 Ω. Capacitor values 4.7 µF or larger are acceptable, provided the ESR is less than 10 Ω. Solid tantalum electrolytic, aluminum electrolytic, and multilayer ceramic capacitors are all suitable, provided they meet the requirements described above. Most of the commercially available 4.7 µF surface-mount solid tantalum capacitors, including devices from Sprague, Kemet, and Nichico, meet the ESR requirements stated above (see Table 3).

Table 3. Capacitor Selection

PART NO.	MFR	VALUE	MAX ESR	SIZE (H × L × W)
T494B475K016AS	Kemet	4.7 µF	1.5 Ω	1.9 × 3.5 × 2.8
195D106x0016x2T	Sprague	10 µF	1.5 Ω	1.3 × 7 × 2.7
695D106x003562T	Sprague	10 µF	1.3 Ω	2.5 × 7.6 × 2.5
TPSC475K035R0600	AVX	4.7 µF	0.6 Ω	2.6 × 6 × 3.2

13.2.2.2 Output Voltage Programming

The output voltage of the TPS76301 adjustable regulator is programmed using an external resistor divider as shown in Figure 21. The output voltage is calculated using Equation 1.

$$V_O = 0.995 \times V_{ref} \times \left(1 + \frac{R1}{R2}\right) \quad (1)$$

where

- Vref = 1.192 V typical (the internal reference voltage)
- 0.995 is a constant used to center the load regulator (1%)

Resistors R1 and R2 must be chosen for approximately 7-µA divider current. Lower value resistors can be used but offer no inherent advantage and waste more power. Higher values must be avoided as leakage currents at FB increase the output voltage error. TI recommends choosing a design procedure of R2 = 169 kΩ to set the divider current at 7 µA and then calculate R1 using Equation 2.

$$R1 = \left(\frac{V_O}{0.995 \times V_{ref}} - 1\right) \times R2 \quad (2)$$

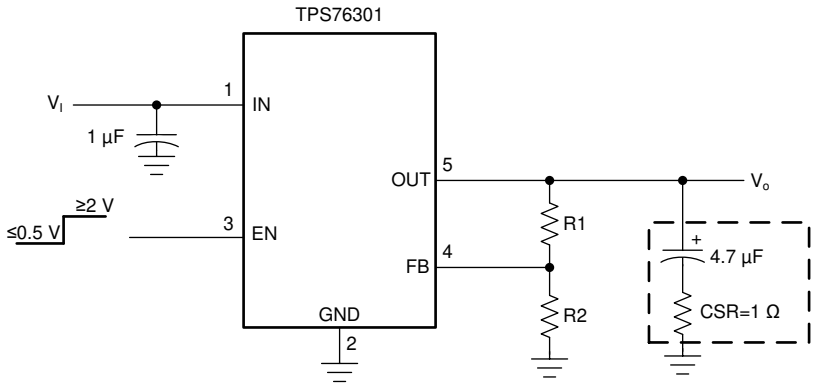


Figure 21. TPS76301 Adjustable LDO Regulator Programming

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13.2.2.3 Reverse Current

The TPS763xx pass element has a built-in back diode that safely conducts reverse currents when the input voltage drops below the output voltage (for example, during power down). Current is conducted from the output to the input and is not internally limited. If extended reverse voltage is anticipated, external limiting might be appropriate.

13.2.3 Application Curves

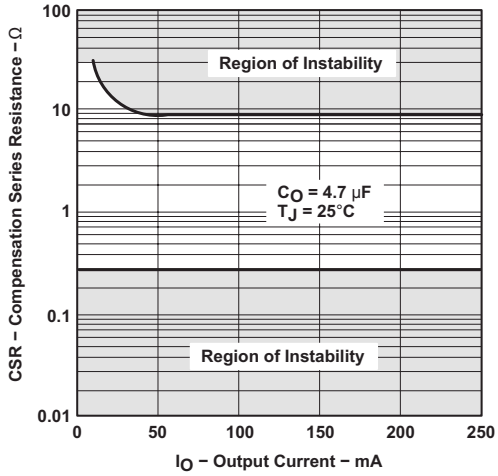


Figure 22. Compensation Series Resistance (CSR) vs Output Current

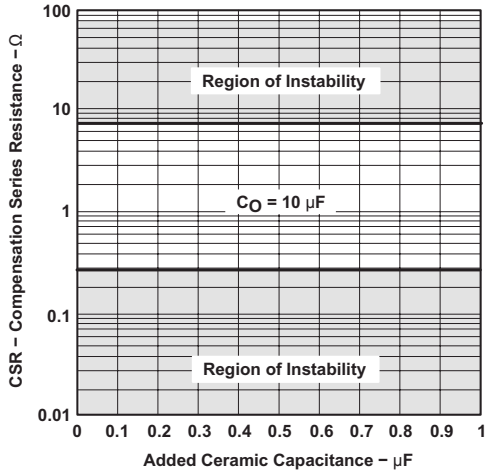


Figure 23. Compensation Series Resistance (CSR) vs Added Ceramic Capacitance

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14 Power Supply Recommendations

A 1-µF or larger input capacitor must be used.

14.1 Power Dissipation and Junction Temperature

Specified regulator operation is assured to a junction temperature of 125°C; the maximum junction temperature allowable to avoid damaging the device is 150°C. This restriction limits the power dissipation the regulator can handle in any given application. To ensure the junction temperature is within acceptable limits, calculate the maximum allowable dissipation, $P_{D(max)}$, and the actual dissipation, P_D, which must be less than or equal to $P_{D(max)}$.

The maximum-power-dissipation limit is determined using Equation 3.

$$P_{D(max)} = \frac{T_J max - T_A}{R_{\theta JA}} \quad (3)$$

where

- $T_J$max is the maximum allowable junction temperature
- $R_{\theta JA}$ is the thermal resistance junction-to-ambient for the package, see *Thermal Information*
- T_A is the ambient temperature

The regulator dissipation is calculating using Equation 4.

$$P_D = (V_I - V_O) \times I_O \quad (4)$$

Power dissipation resulting from quiescent current is negligible.

15 Layout

15.1 Layout Guidelines

- Place input and output capacitors as close to the device as possible.
- Use copper planes for device connections to optimize thermal performance.
- Place thermal vias around the device to distribute the heat.

15.2 Layout Example

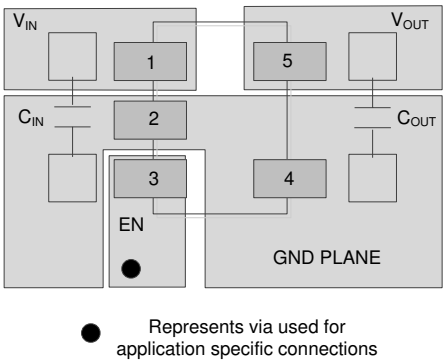


Figure 24. Layout Example for DBV Package

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16 デバイスおよびドキュメントのサポート

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16.5 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

17 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS76301DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAZI	Samples
TPS76301DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAZI	Samples
TPS76301DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PAZI	Samples
TPS76316DBVR	LIFEBUY	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBHI	
TPS76316DBVRG4	LIFEBUY	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBHI	
TPS76316DBVT	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBHI	
TPS76318DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBAI	Samples
TPS76318DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBAI	Samples
TPS76318DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBAI	Samples
TPS76318DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBAI	Samples
TPS76325DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBBI	Samples
TPS76325DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBBI	Samples
TPS76325DBVT	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBBI	
TPS76328DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBDI	Samples
TPS76330DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBII	Samples
TPS76330DBVT	LIFEBUY	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBII	
TPS76333DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBEI	Samples
TPS76333DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBEI	Samples
TPS76333DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBEI	Samples
TPS76333DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBEI	Samples
TPS76338DBVR	LIFEBUY	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBFI	
TPS76338DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBFI	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS76350DBVR	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBGI	Samples
TPS76350DBVRG4	ACTIVE	SOT-23	DBV	5	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBGI	Samples
TPS76350DBVT	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBGI	Samples
TPS76350DBVTG4	ACTIVE	SOT-23	DBV	5	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	PBGI	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

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RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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OTHER QUALIFIED VERSIONS OF TPS763 :

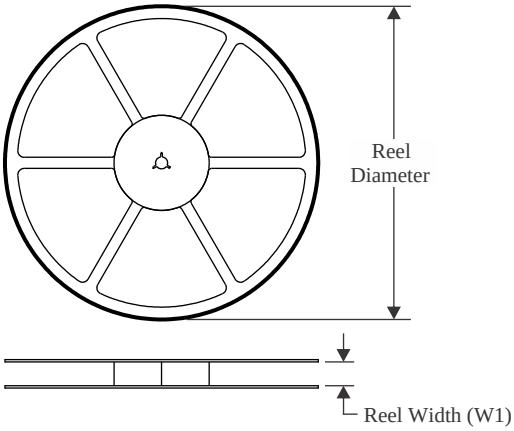
- Automotive : TPS763-Q1

NOTE: Qualified Version Definitions:

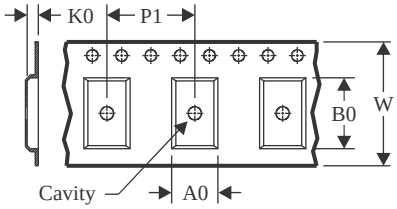
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS

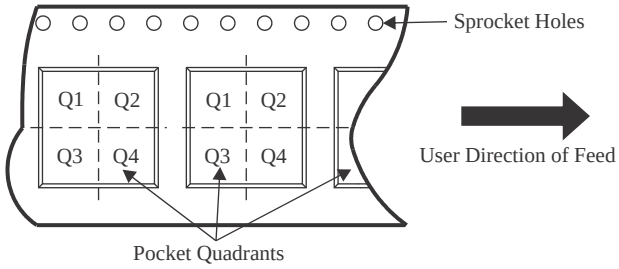


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

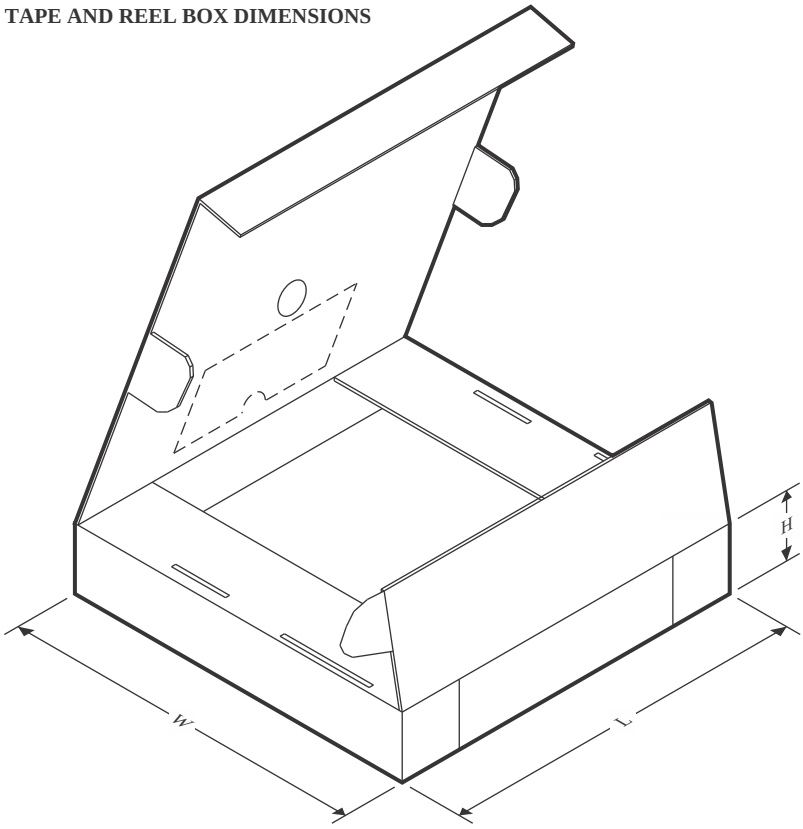


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS76301DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76301DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS76301DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS76301DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76316DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76316DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76318DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS76318DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3
TPS76318DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS76318DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76325DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76325DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76328DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76330DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76330DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76333DBVR	SOT-23	DBV	5	3000	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS76333DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76333DBVT	SOT-23	DBV	5	250	179.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
TPS76333DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76338DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76338DBVT	SOT-23	DBV	5	250	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76350DBVR	SOT-23	DBV	5	3000	178.0	9.0	3.23	3.17	1.37	4.0	8.0	Q3
TPS76350DBVT	SOT-23	DBV	5	250	178.0	9.0	3.3	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS76301DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76301DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS76301DBVT	SOT-23	DBV	5	250	200.0	183.0	25.0
TPS76301DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS76316DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76316DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS76318DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS76318DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76318DBVT	SOT-23	DBV	5	250	200.0	183.0	25.0
TPS76318DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS76325DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76325DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS76328DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76330DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76330DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS76333DBVR	SOT-23	DBV	5	3000	200.0	183.0	25.0
TPS76333DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76333DBVT	SOT-23	DBV	5	250	200.0	183.0	25.0

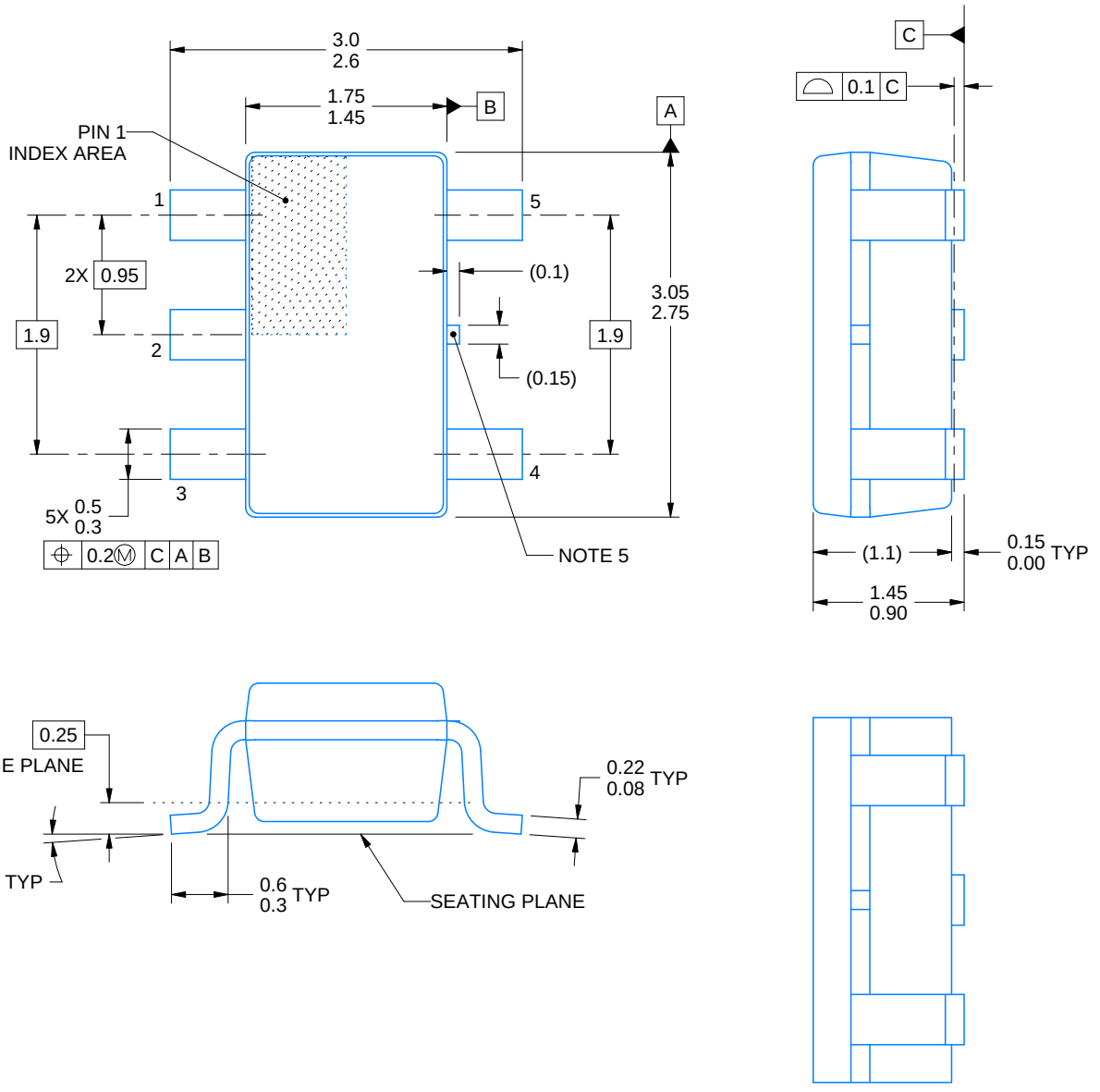
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS76333DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS76338DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76338DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0
TPS76350DBVR	SOT-23	DBV	5	3000	180.0	180.0	18.0
TPS76350DBVT	SOT-23	DBV	5	250	180.0	180.0	18.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR

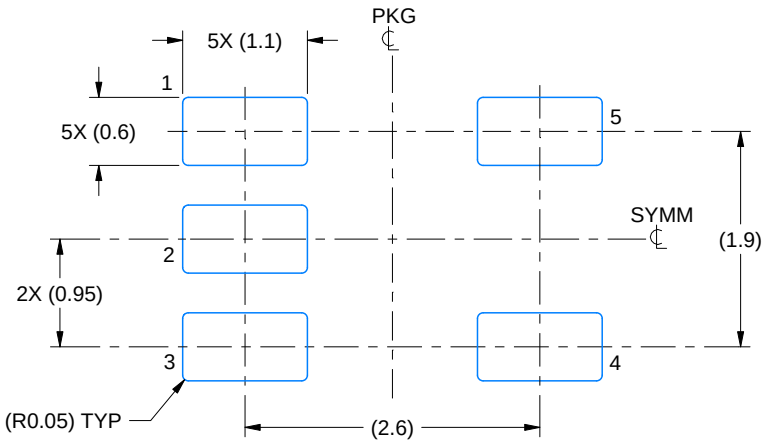


ALTERNATIVE PACKAGE SINGULATION VIEW

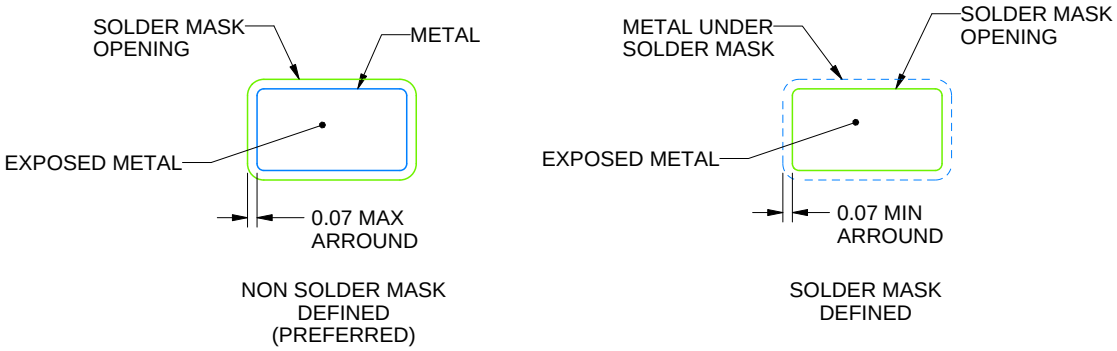
4214839/J 02/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

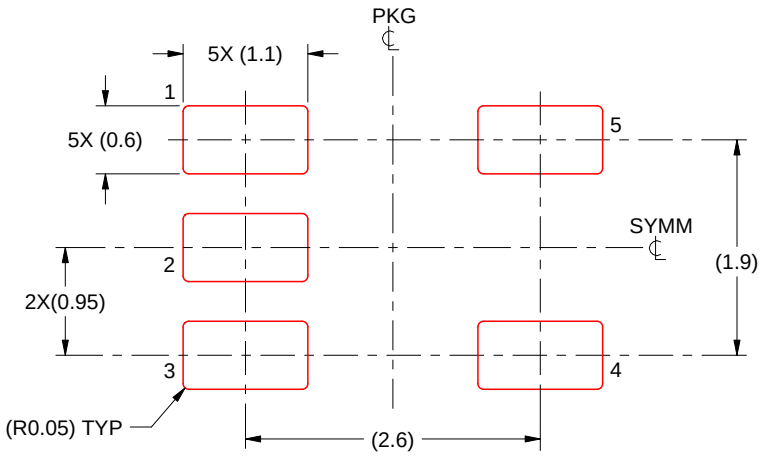


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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