TEXAS INSTRUMENTS

TPS7H2221-SEP
JAJSNL4A – AUGUST 2022 – REVISED OCTOBER 2022

TPS7H2221-SEP 耐放射線特性、5.5V、1.25A、115mΩ のロード・スイッチ

1 特長

- VID (Vendor Item Drawing) V62/22609 が利用可能
- 総照射線量 (TID) 耐性 = 30krad (Si)
  - すべてのウェハー・ロットについて、20krad(Si) までの TID RLAT (放射線ロット受け入れテスト)
- シングル・イベント効果 (SEE) の特性
  - シングル・イベント・ラッチアップ (SEL)、シングル・イベント・バーンアウト (SEB)、シングル・イベント・ゲート・ラプチャー (SEGR) の、実効線エネルギー付与 (LET_{EFF}) に対する耐性 = 43MeV-cm$_2$/mg。
  - シングル・イベント過渡 (SET) およびシングル・イベント機能割り込み (SEFI) の、LET_{EFF} に対する耐性 = 43MeV-cm^2/mg。
- 動作入力電圧範囲 (V_{IN})：1.6～5.5V
- 推奨連続電流 (I_{MAX})：1.25A
- オン抵抗 (R_{ON})
  - V_{IN} = 5V で 116mΩ (標準値)
  - V_{IN} = 3.3V で 115mΩ (標準値)
  - V_{IN} = 1.8V で 133mΩ (標準値)
- 出力短絡保護 (I_{SC})：3A (標準値)
- 低い消費電力：
  - オン状態 (I_Q)：8.3µA (標準値)
  - オフ状態 (I_{SD})：3nA (標準値)
- 低速のターンオン・タイミングによる突入電流制限 (t_{ON})：
  - 5V 時の t_{ON} = 1.68ms (3.61mV/µs 時)
  - 3.3V 時の t_{ON} = 1.51ms (2.91mV/µs 時)
  - 1.8V 時の t_{ON} = 1.32ms (2.15 mV/µs 時)
- 出力放電および立ち下がり時間を変更可能
  - V_{IN} = 3.3V での内部 QOD 抵抗 = 9.2Ω（標準値）
- 宇宙向け強化プラスチック (SEP)
  - 管理されたベースライン
  - 金ボンド・ワイヤ
  - NiPdAu リード仕上げ
  - 単一のアセンブリ / テスト施設
  - 単一の製造施設
  - 軍用温度範囲：-55℃～125℃
  - 長い製品ライフ・サイクル
  - 製品変更通知期間 (PCN) の延長
  - 製品のトレーサビリティ
  - モールド・コンパウンドの改良による低いガス放出

2 アプリケーション

- 人工衛星の電源管理および分配
- 放射線耐性を持つ電源ツリー・アプリケーション
- コントローラの電源オンと電源オフに使用するスイッチング電源レールを有効化

- 衛星用電源システム (EPS)

3 概要

TPS7H2221-SEP デバイスは、スルー・レート制御機能付きの小型シングル・チャネル負荷スイッチです。このデバイスは、1.6V～5.5V の入力電圧範囲で動作できる N チャネル MOSFET を内蔵し、最大 1.25A の連続電流をサポートします。
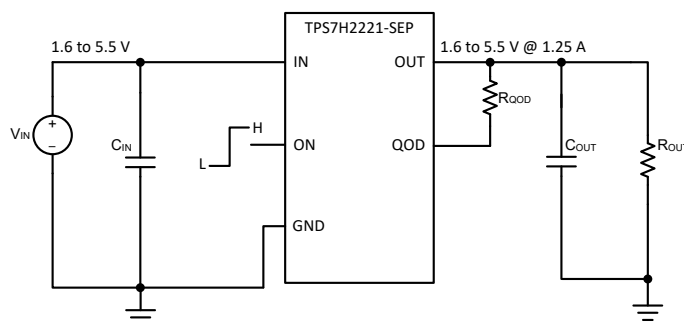
スイッチのオン状態はデジタル入力により制御され、この入力は低電圧の制御信号と直接接続できます。電源が最初に印加されたときには、スマート・プルダウンを使用して、システムのシーケンシングが完了するまで、ON ピンがフローティング状態になることが防止されます。ピンが意図的に High ($V_{ON} > V_{IH}$) に駆動されると、不必要な電力損失を避けるため、スマート・プルダウンは切断されます。

また、TPS7H2221-SEP 負荷スイッチには自己保護機能があり、デバイスの出力が短絡した場合も自身を保護できます。

TPS7H2221-SEP は標準の SC-70 パッケージで供給され、-55℃～125℃の接合部温度範囲で仕様が規定されています。

部品番号[1]	グレード	パッケージ [2]
TPS7H2221MDCKTSEP	20krad(Si) RLAT、30krad(Si) 特性	SC-70 (6) 2.10mm × 2.00mm 質量 = 6.9mg
TPS7H2221EVM	評価ボード	EVM

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。
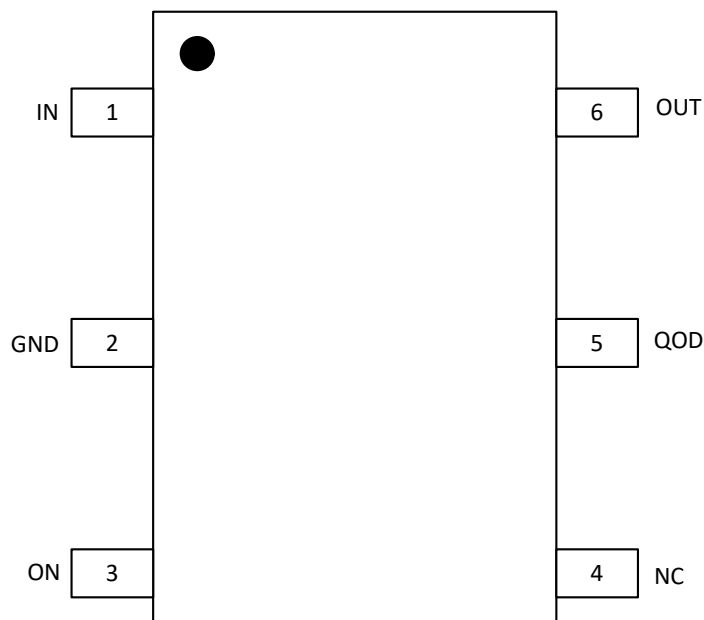(2) 寸法と質量は公称値です。

代表的なアプリケーション回路図

English Data Sheet: SLVSGP1

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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

5 Pin Configuration and Functions

図 5-1. DCK Package
6-Pin SC-70
(Top View)

表 5-1. Pin Functions

PIN		I/O[1]	DESCRIPTION
NO.	NAME		
1	IN	I	Switch input.
2	GND	—	Device ground.
3	ON	I	Active high switch control input. Do not leave floating.
4	NC	—	No connect. This pin is not internally connected. It is recommended to connect this pin to GND to prevent charge buildup; however, this pin can also be left open or tied to any voltage between GND and IN.
5	QOD	O	Quick Output Discharge pin. This pin can be utilized in one of three ways: • Placing an external resistor between V_{OUT} and QOD • Tying QOD directly to V_{OUT} and using the internal resistor value (R_{PD}) • Disabling QOD by leaving pin floating See the *Fall Time (t_{FALL}) and Quick Output Discharge (QOD)* section for more information.
6	OUT	O	Switch output.

(1)   I = Input, O = Output, — = Other

6 Specifications

6.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)[1]

		MIN	MAX	UNIT
V_{IN}	Maximum Input Voltage Range (IN to GND)	−0.3	6	V
V_{OUT}	Maximum Output Voltage Range (OUT to GND)	−0.3	6	V
V_{ON}	Maximum ON Pin Voltage Range (ON to GND)	−0.3	6	V
V_{QOD}	Maximum QOD Pin Voltage Range (QOD to GND)	−0.3	6	V
I_{MAX}	Maximum Continuous Current		1.5	A
I_{PLS}	Maximum Pulsed Current (ts=2 ms, 2% Duty Cycle)		2.5	A
T_J	Junction temperature	-55	150	°C
T_{STG}	Storage temperature	−65	150	°C

(1)   Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001[1]	±2000	V
		Charged device model (CDM), per per ANSI/ESDA/JEDEC JS-002[2]	±1000	

(1)   JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2)   JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	TYP	MAX	UNIT
V_{IN}	Input Voltage Range (IN to GND)	1.6		5.5	V
V_{OUT}	Output Voltage Range (OUT to GND)	0		5.5	
V_{ON}	ON Voltage Range (ON to GND)	0		5.5	
I_{MAX}	Maximum Continuous Current	0		1.25	A
T_J	Junction temperature	−55		125	°C

6.4 Thermal Information

	THERMAL METRIC[1]	TPS7H2221-SEP	UNIT
		DCK (SC-70)	
		6 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	237.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	173.7	
$R_{\theta JB}$	Junction-to-board thermal resistance	93.9	
Ψ_{JT}	Junction-to-top characterization parameter	74.4	
Ψ_{JB}	Junction-to-board characterization parameter	93.6	

(1)   For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.5 Electrical Characteristics

Over V_{IN} = 1.6 to 5.5 -V, $V_{ON} \geq V_{IH}$, over the temperature range (T_A=-55 ℃ to 125 ℃), unless otherwise specified. All voltage levels are reference to GND.

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
Input Supply (VIN)							
$I_{Q, VIN}$	V_{IN} Quiescent Current	V_{OUT} = Open,	25 ℃		8.3	15	µA
		V_{OUT} = Open,			8.7	20	
$I_{SD, VIN}$	V_{IN} Shutdown Current	$V_{ON} \leq V_{IL}$, V_{OUT} = GND	25 ℃		3	20	nA
		$V_{ON} \leq V_{IL}$, V_{OUT} = GND				800	
ON-Resistance (RON)							
R_{ON}	ON-State Resistance	V_{IN} = 5 V, I_{OUT} = -200 mA	-55 ℃		90	150	mΩ
			25 ℃		116	150	
			125 ℃		150	200	
		V_{IN} = 3.3 V, I_{OUT} = -200 mA	-55 ℃		89	150	mΩ
			25 ℃		115	150	
			125 ℃		150	250	
		V_{IN} = 1.8 V, I_{OUT} = -200 mA	-55 ℃		103	300	mΩ
			25 ℃		133	300	
			125 ℃		173	350	
Output Short Protection (ISC)							
I_{SC}	Short Circuit Current Limit	$V_{OUT} \leq V_{IN}$ - 1.5 V			3		A
		$V_{OUT} \leq V_{SC}$		30	512	900	mA
V_{SC}	Output Short Detection Threshold	25 ℃		0.22	0.36	0.57	V
T_{SD}	Thermal Shutdown	Rising			180		℃
		Falling			145		
Enable Pin (ON)							
I_{ON}	ON Pin Leakage	$V_{ON} \geq V_{IH}$				100	nA
$R_{PD, ON}$	Smart Pull Down Resistance	$V_{ON} \leq V_{IL}$			499		kΩ
$V_{IH,ON}$	ON Pin Input High (V_{IH} Rising)			1			V
$V_{IL,ON}$	ON Pin Input Low (V_{IL} Falling)					0.35	
Quick-output Discharge (QOD)							
$R_{PD, QOD}$	QOD Pin Internal Discharge Resistance	$V_{ON} \leq V_{IL}$	V_{IN} = 1.8-V		45.4		Ω
			V_{IN} = 3.3-V		8.5		
			V_{IN} = 5-V		6		

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6.6 Switching Characteristics

Unless otherwise noted, the typical characteristics in the following table apply to an input voltage of 3.3V, an ambient temperature of 25°C, R_{QOD}= 0 Ω and a load of C_{OUT}= 0.1 µF, R_{OUT} = 100 Ω. See 図 7-2

	PARAMETER	TEST CONDITIONS		MIN	TYP	MAX	UNIT
t_{ON}	Turn ON Time	V_{IN} = 5.0 V			1680		µs
		V_{IN} = 3.3 V			1510		
		V_{IN} = 1.8 V			1320		
t_R	Output Rise Time	V_{IN} = 5.0 V			1120		µs
		V_{IN} = 3.3 V			915		
		V_{IN} = 1.8 V			674		
SR_{ON}	Turn ON Slew Rate	V_{IN} = 5.0 V			3.61		mV/µs
		V_{IN} = 3.3 V			2.91		
		V_{IN} = 1.8 V			2.15		
t_{OFF}	Turn OFF Time	V_{IN} = 1.8 V to 5.0V	R_{OUT} = 100Ω, C_{OUT} = 0.1uF		5.22		µs
t_{FALL}	Output Fall Time [1]	R_{OUT} = Open [2]			9.6		µs
			C_{OUT} = 10uF, R_{QOD}=0 Ω		0.35		ms
			C_{OUT} = 10uF, R_{QOD}=100 Ω		3.12		ms
			C_{OUT} = 100uF; R_{QOD}=0 Ω		4.3		ms

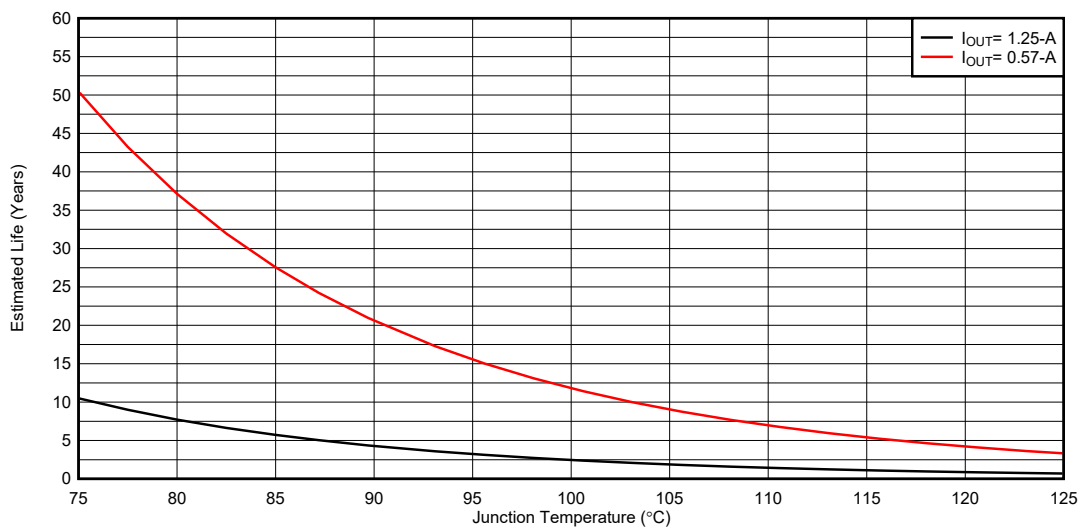(1)   Output may not discharge completely if QOD is not connected to V_{OUT}
(2)   See the *Timing Application* section for information on how R_{OUT} and C_{OUT} affect Fall Time.

6.7 Derating Curves
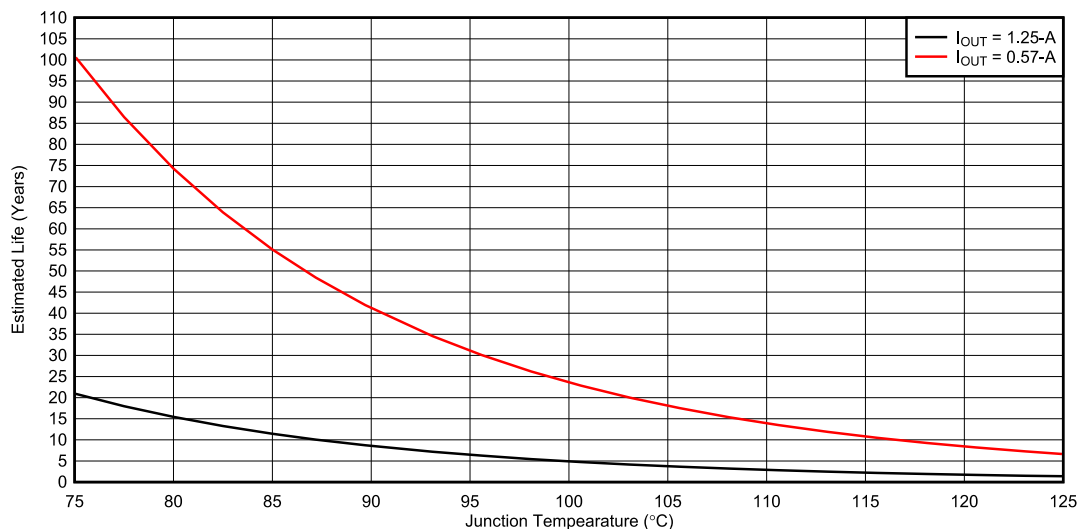
FIT = 50

図 6-1. Estimated Life Rating Due to Electromigration vs Junction Temperature at 50% Duty Cycle

FIT=50

図 6-2. Estimated Life Rating Due to Electromigration vs Junction Temperature at 100% Duty Cycle

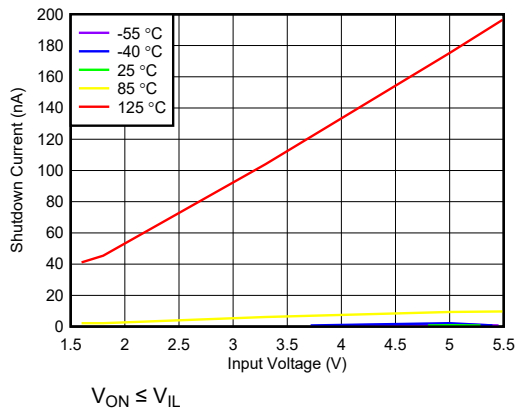Product Folder Links: *TPS7H2221-SEP*

6.8 Typical Characteristics

$V_{ON} \leq V_{IL}$

図 6-3. Shutdown Current vs Input Voltage

$V_{ON} \geq V_{IH}$
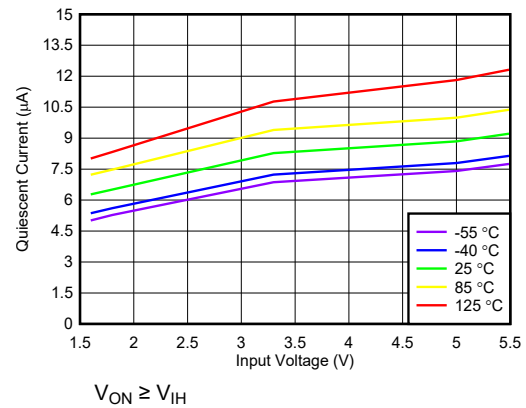
図 6-4. Quiescent Current vs Input Voltage

$I_{LOAD} = -200 \text{ mA}$
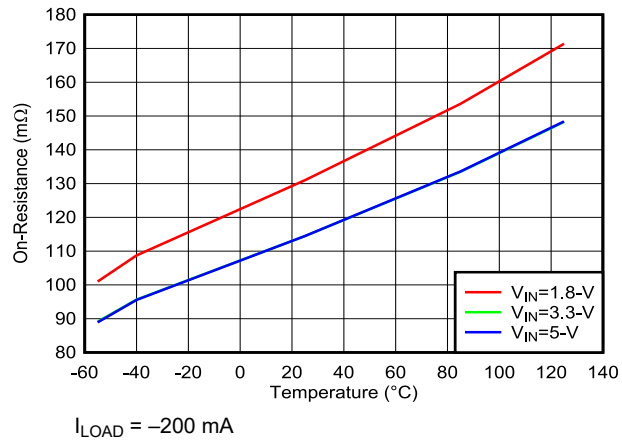
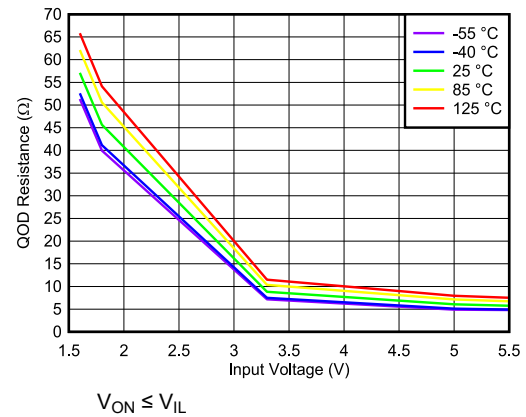**図 6-5. On-Resistance vs Junction Temperature**

$V_{ON} \leq V_{IL}$

図 6-6. QOD Resistance vs Input Voltage
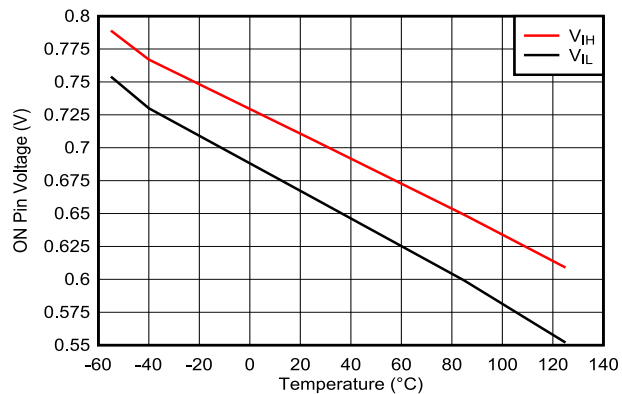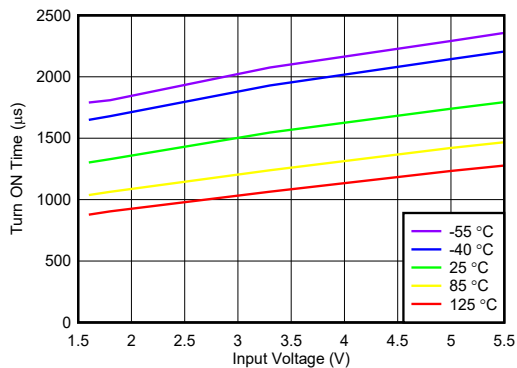

図 6-7. V_{IH}/V_{IL} vs Junction Temperature

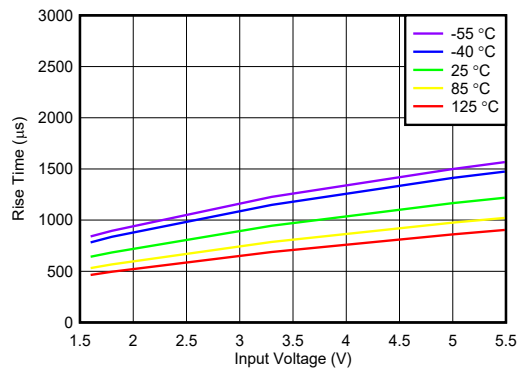
$V_{ON} \leq V_{IL}$
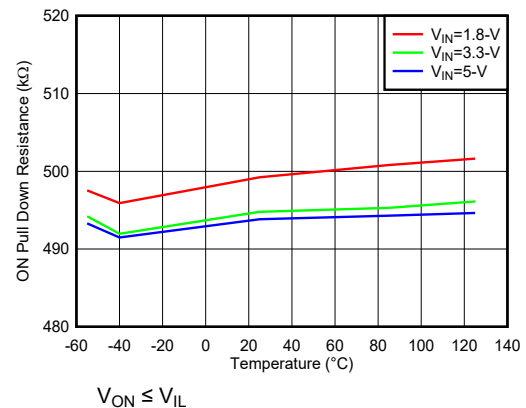
図 6-8. ON Pull Down Resistance vs Junction Temperature

Product Folder Links: *TPS7H2221-SEP*

図 6-9. Turn ON Time vs Input Voltage

C_{OUT} = 0.1 µF R_{OUT} = 100 Ω R_{QOD} = 0 Ω

図 6-10. Rise Time vs Input Voltage

C_{OUT} = 0.1 µF R_{OUT} = 100 Ω R_{QOD} = 0 Ω
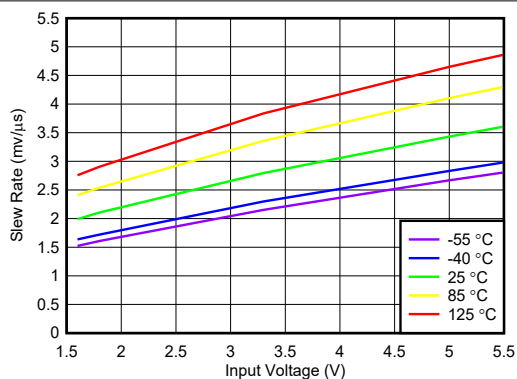
図 6-11. Output Slew Rate vs Input Voltage

C_{OUT} = 0.1 µF R_{OUT} = 100 Ω R_{QOD} = 0 Ω
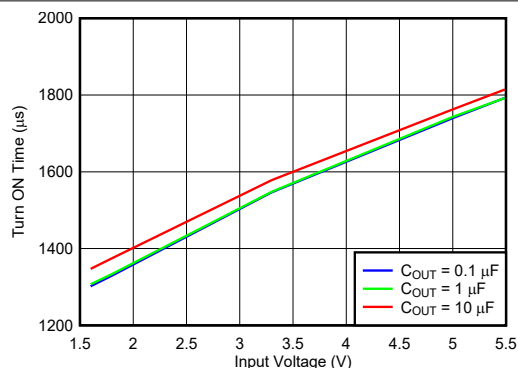
図 6-12. Turn ON Time vs Input Voltage Across Load Capacitance
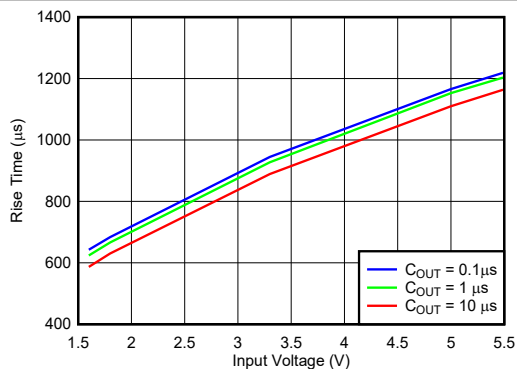
R_{OUT} = 100 Ω T_J = 25°C R_{QOD} = 0 Ω

図 6-13. Rise Time vs Input Voltage Across Load Capacitance
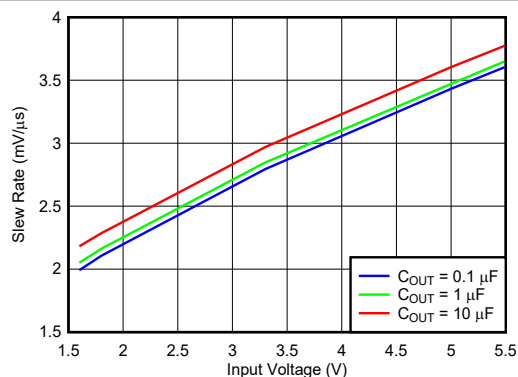
R_{OUT} = 100 Ω T_J = 25°C R_{QOD} = 0 Ω

図 6-14. Slew Rate vs Input Voltage Across Load Capacitance

R_{OUT} = 100 Ω T_J = 25°C R_{QOD} = 0 Ω
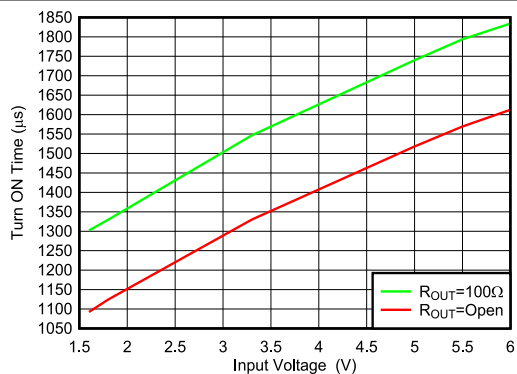
C_OUT = 0.1 μF   T_J = 25°C   R_QOD = 0 Ω

図 6-15. Turn ON Time vs Input Voltage Across Load Resistance
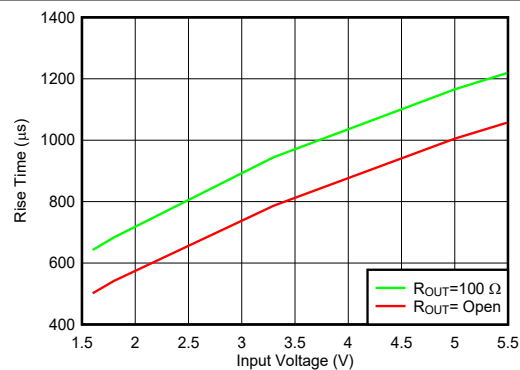
C_OUT = 0.1 μF   T_J = 25°C   R_QOD = 0 Ω

図 6-16. Rise Time vs Input Voltage Across Load Resistance
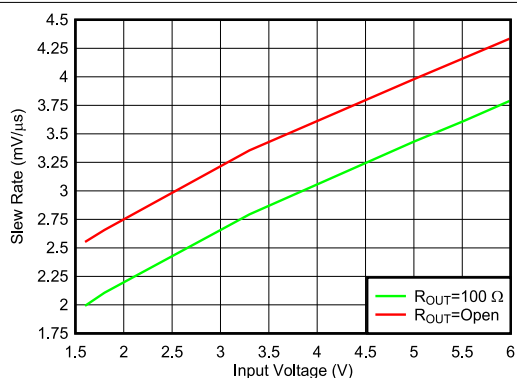
C_OUT = 0.1 μF   T_J = 25°C R_QOD = 0 Ω

図 6-17. Output Slew Rate vs Input Voltage Across Load Resistance

C_OUT = 0.1 μF   R_OUT = 100 Ω   R_QOD = 0 Ω
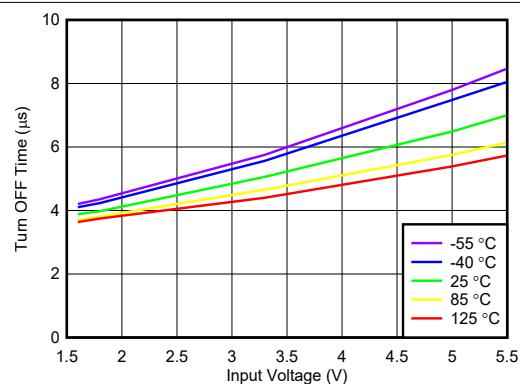
図 6-18. Turn OFF Time vs Input Voltage

C_OUT = 0.1 μF   R_OUT = 100 Ω   R_QOD = 0 Ω
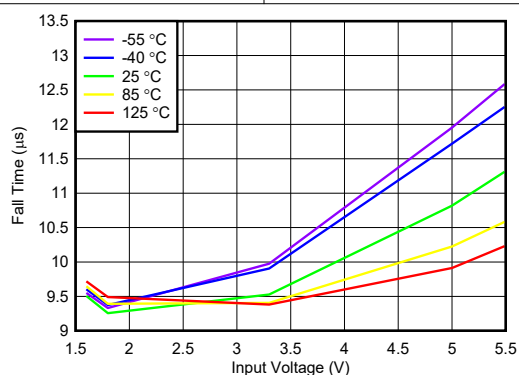
図 6-19. Fall Time vs Input Voltage

Product Folder Links: *TPS7H2221-SEP*

C_{IN} = 1 µF R_{OUT} = 100 Ω R_{QOD} = 0 Ω
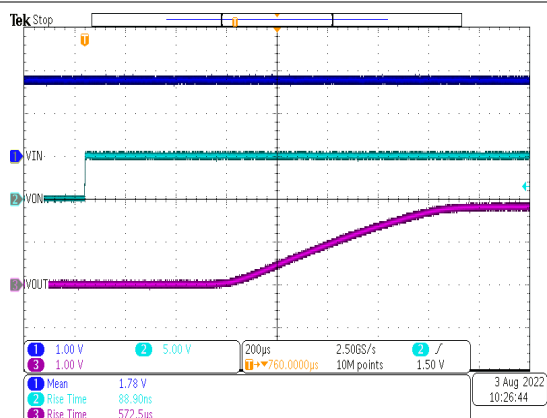
C_{OUT} = 0.1 µF

図 6-20. Rise Time with V_{IN} = 1.8 V

C_{IN} = 1 µF R_{OUT} = 100 Ω R_{QOD} = 0 Ω
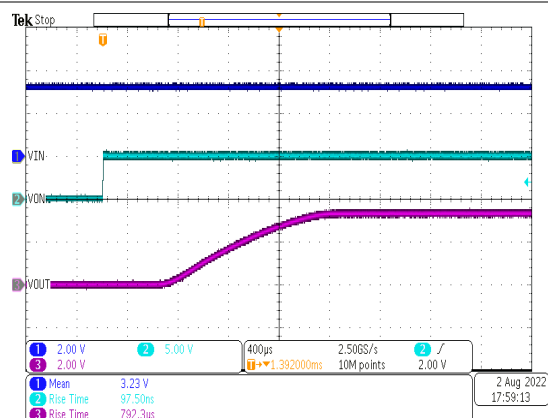
C_{OUT} = 0.1 µF

図 6-21. Rise Time with V_{IN} = 3.3 V

C_{IN} = 1 µF R_{OUT} = 100 Ω R_{QOD} = 0 Ω
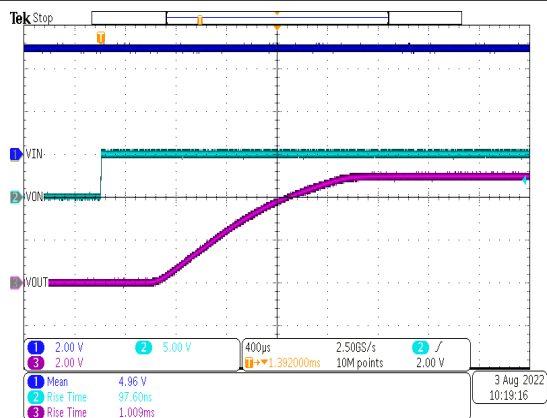
C_{OUT} = 0.1 µF

図 6-22. Rise Time with V_{IN} = 5 V

C_{IN} = 1 µF R_{OUT} = 100 Ω R_{QOD} = 2k Ω
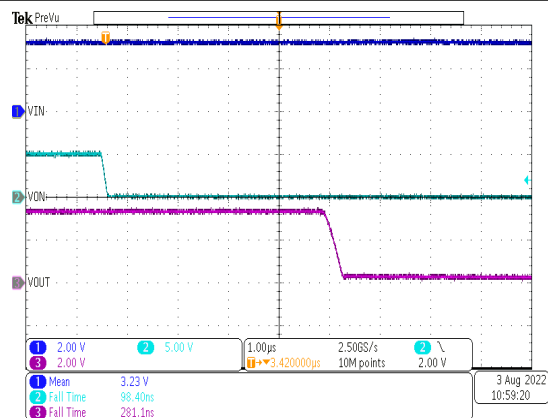
C_{OUT} = Open

図 6-23. Turn Off with a Small Load Capacitance

C_{IN} = 1 µF R_{OUT} = 100 Ω R_{QOD} = 2k Ω
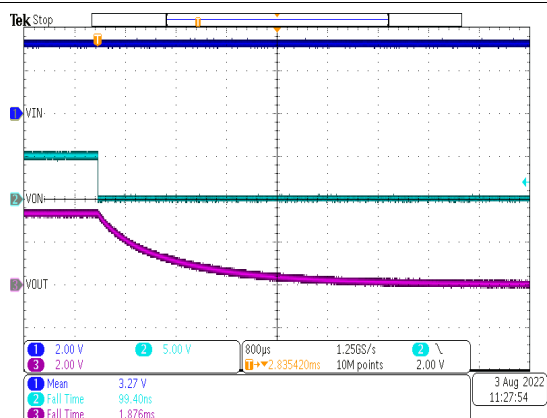
C_{OUT} = 10 µF

図 6-24. Turn Off with a Large Load Capacitance

C_{IN} = 58 µF R_{OUT} = 4m Ω R_{QOD} = 0 Ω
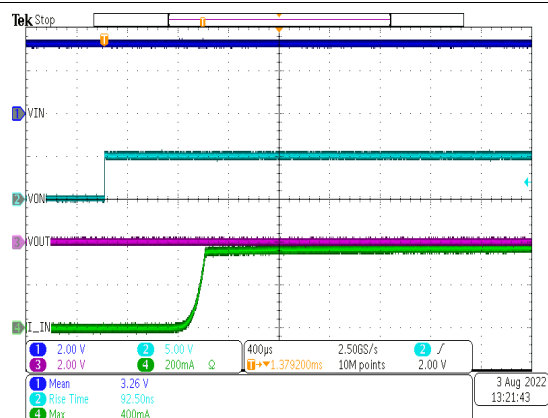
C_{OUT} = 10 µF V_{IN} = 3.3 V

図 6-25. Turn On Into an Output Short

Product Folder Links: TPS7H2221-SEP

C_{IN} = 58 μF R_{OUT} = 300m Ω R_{QOD} = 0 Ω
C_{OUT} = 10 μF V_{IN} = 3.3 V V_{ON}=V_{IN}

図 **6-26. Hot Short Event when ON**

C_{IN} = 58 μF R_{OUT} = 300m Ω R_{QOD} = 0 Ω
C_{OUT} = 10 μF V_{IN} = 3.3 V V_{ON}=V_{IN}

図 **6-27. Hot Short Event when ON and Recovery**

Product Folder Links: *TPS7H2221-SEP*
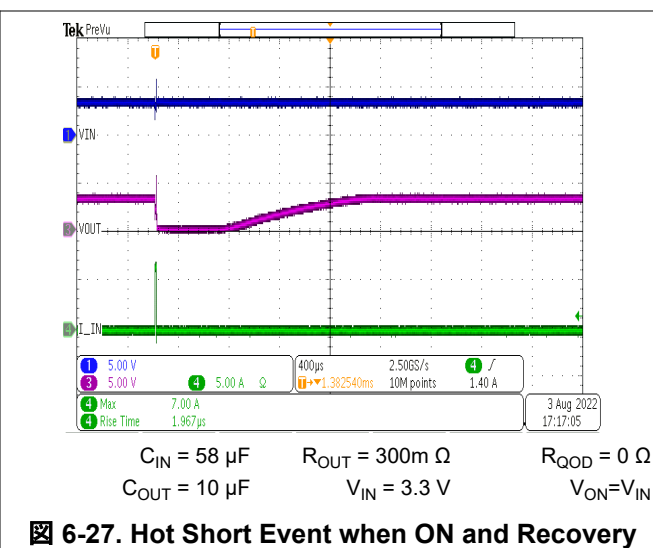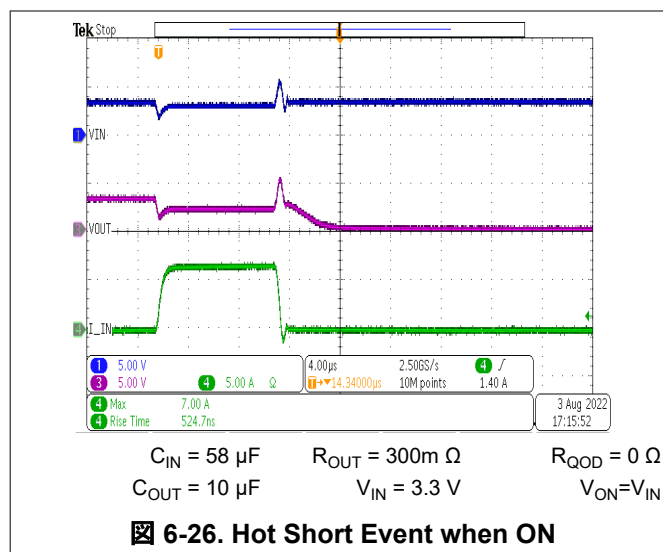
7 Parameter Measurement Information

7.1 Test Circuit and Timing Waveforms Diagrams
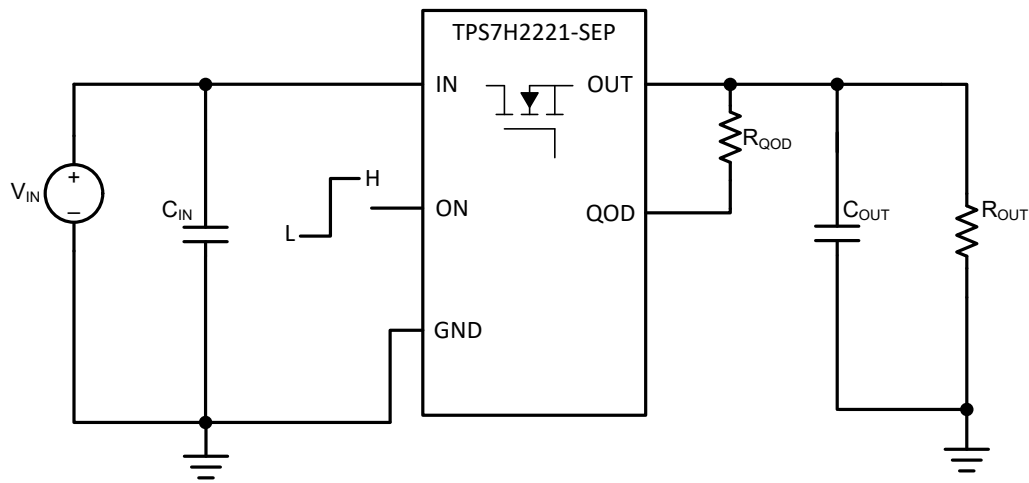
A. Rise and fall times of the control signal are 100 ns.

B. Turn-off times and fall times are dependent on the time constant at the load. For the TPS7H2221-SEP, the internal pull-down resistance QOD is enabled when the switch is disabled. When QOD is connected to OUT using a resistor (R_{QOD}), the time constant is (R_{QOD} + $R_{PD,QOD}$ || R_{OUT}) × C_{OUT}.

図 7-1. Test Circuit
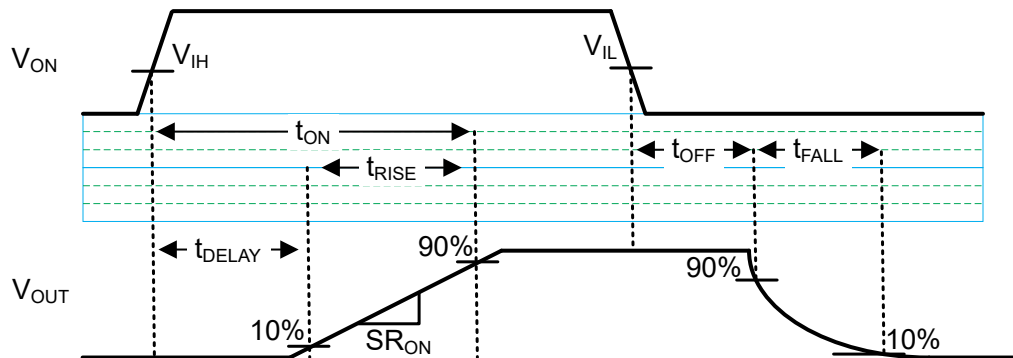
図 7-2. Timing Waveforms

8 Detailed Description

8.1 Overview

The TPS7H2221-SEP device is a 5.5-V, 1.25-A load switch in a 6-pin SOT-23 package. To reduce voltage drop for low voltage and high current rails, the device implements a low resistance N-channel MOSFET that reduces the drop out voltage across the device.

The TPS7H2221-SEP device has a slow slew rate, which helps reduce or eliminate power supply droop because of large inrush currents during power up. Furthermore, the device features a Quick-Output-Discharge (QOD) pin, which allows the configuration of the discharge rate of V_{OUT} once the switch is disabled. During shutdown, the device has very low leakage currents, thereby reducing unnecessary leakages for downstream devices during standby. Integrated control logic, driver, charge pump, and output discharge FET eliminates the need for any external components, which reduces solution size and bill of materials (BOM) count.

The TPS7H2221-SEP load switch is also self-protected, meaning that it will protect from short circuit events on the output of the device. It also has thermal shutdown to prevent thermal runaway.

8.2 Functional Block Diagram

Product Folder Links: *TPS7H2221-SEP*
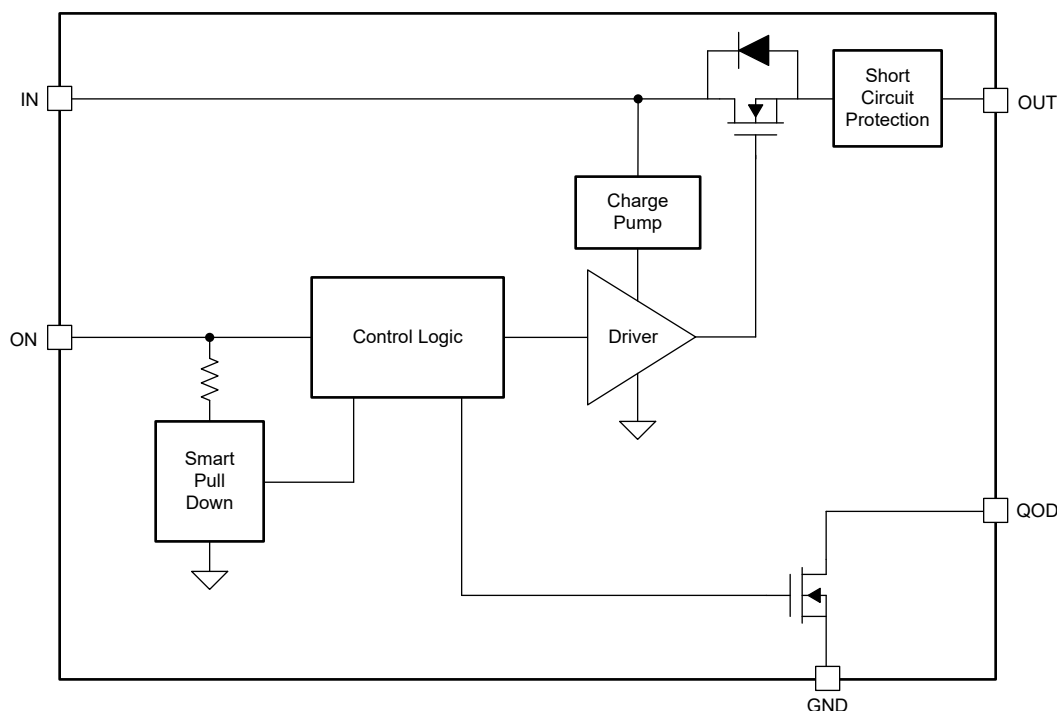
8.3 Feature Description

表 8-1. Smart-ON Pull Down

VON	PULL DOWN
≤ $V_{IL,ON}$	Connected
≥ $V_{IH,ON}$	Disconnected

8.3.1 On and Off Control

The ON pin controls the state of the switch. The ON pin is compatible with standard CMOS logic threshold so it can be used in a wide variety of applications. When power is first applied to V_{IN} a Smart Pull Down is used to keep the ON pin from floating until the system sequencing is complete. Once the ON pin is deliberately driven high (≥$V_{IH,ON}$), the Smart Pull Down is disconnected to prevent unnecessary power loss. See 表 8-1 to determine the state of the ON Pin Smart Pull Down state as function of ON pin voltage.

8.3.2 Output Short Circuit Protection (I_{SC})

The device will limit current to the output in case of output shorts. When a short occurs, the large V_{IN} to V_{OUT} voltage drop causes the switch to limit the output current (I_{SC}). When the output is below the hard short threshold (V_{SC}), a lower limit is used to minimize the power dissipation while the fault is present. The device will continue to limit the current until it reaches thermal shutdown temperature. At this time, the device will turn off until its temperature has lowered by the thermal hysteresis (35°C typical) before turning on again.
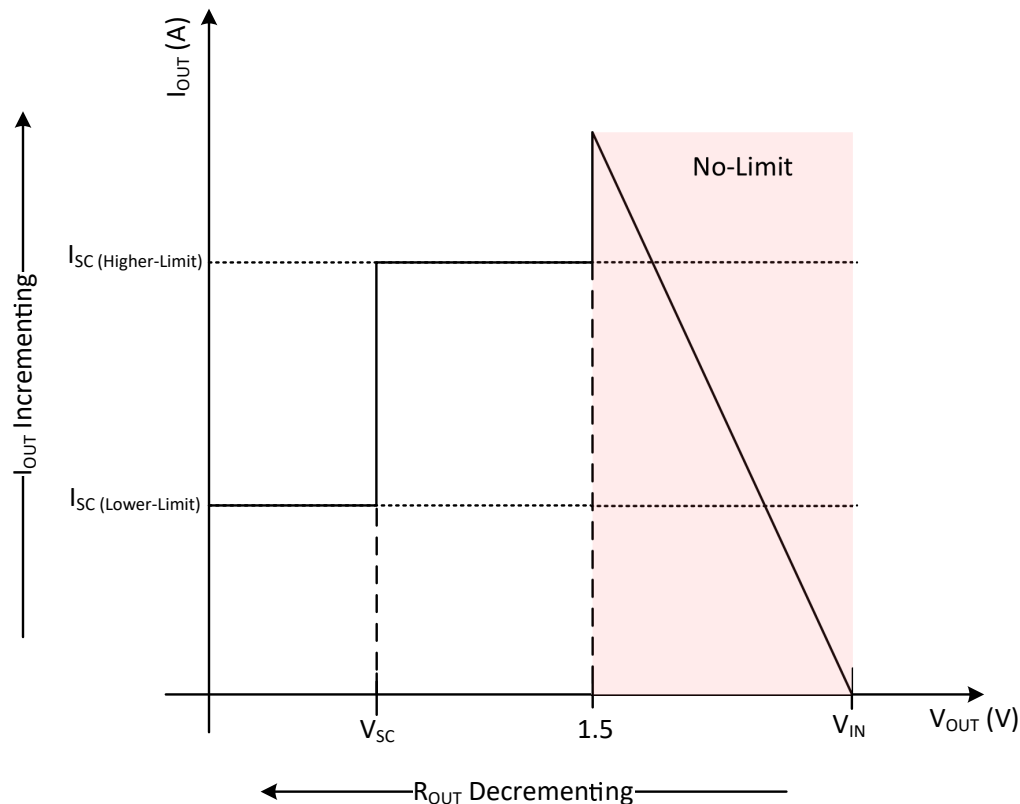

図 8-1. Output Short Circuit Current Limit

Product Folder Links: *TPS7H2221-SEP*

8.3.3 Fall Time (t$_{FALL}$) and Quick Output Discharge (QOD)

The TPS7H2221-SEP device includes a QOD pin that can be configured in one of three ways:

- QOD pin shorted to V$_{OUT}$ pin. Using this method, after the switch becomes disabled the discharge rate is controlled with the value of the internal resistance QOD (R$_{PD,QOD}$).
- QOD pin connected to V$_{OUT}$ pin using an external resistor R$_{QOD}$. After the switch becomes disabled, the discharge rate is controlled by the value of the total discharge resistance. To adjust the total discharge resistance, 式 1 can be used:

$$R_{DIS} = R_{PD,QOD} + R_{QOD} \qquad\qquad (1)$$

where:

- – R$_{DIS}$ is the total output discharge resistance (Ω)
- – R$_{PD,QOD}$ (6 Ω typ.) is the internal pulldown resistance (Ω)
- – R$_{QOD}$ is the external resistance placed between the V$_{OUT}$ and QOD pins (Ω)
- QOD pin is unused and left floating. Using this method, there will be no quick output discharge functionality and the output will remain floating after the switch is disabled.

The fall times of the device depend on many factors including the total discharge resistance (R$_{DIS}$) and the output capacitance (C$_{OUT}$). To calculate the approximate fall time of V$_{OUT}$ use 式 2.

$$t_{FALL} = 2.2 \times (R_{DIS} \| R_{OUT}) \times C_{OUT} \qquad\qquad (2)$$

where:

- t$_{FALL}$ is the output fall time from 90% to 10% (µs)
- R$_{DIS}$ is the total QOD + R$_{QOD}$ resistance (Ω)
- R$_{OUT}$ is the output load resistance (Ω)
- C$_{OUT}$ is the output load capacitance (µF)

8.3.3.1 QOD When System Power is Removed

The adjustable QOD can be used to control the power down sequencing of a system even when the system power supply is removed. When the power is removed, the input capacitor discharges at V$_{IN}$. Past a certain V$_{IN}$ level, the strength of the R$_{PD}$ will be reduced. If there is still remaining charge on the output capacitor, this will result in longer fall times. For further information regarding this condition, see the *Setting Fall Time for Shutdown Power Sequencing* section.

8.4 Device Functional Modes

表 8-2 describes the connection of the V$_{OUT}$ pin depending on the logical state of the ON pin as well as the various QOD pin configurations.

表 8-2. V$_{OUT}$ Connection

ON	QOD CONFIGURATION	V$_{OUT}$
Low	QOD pin connected to VOUT with R$_{QOD}$	Pull-down with (R$_{PD, QOD}$ + R$_{QOD}$)
Low	QOD pin tied to VOUT directly	Pull-down with (R$_{PD, QOD}$)
Low	QOD pin left open	Floating
High	N/A	V$_{IN}$

9 Application and Implementation

> 注
>
> Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

This section highlights some of the design considerations when implementing this device in various applications.

9.2 Typical Application

This typical application demonstrates how the TPS7H2221-SEP devices can be used to power downstream modules.
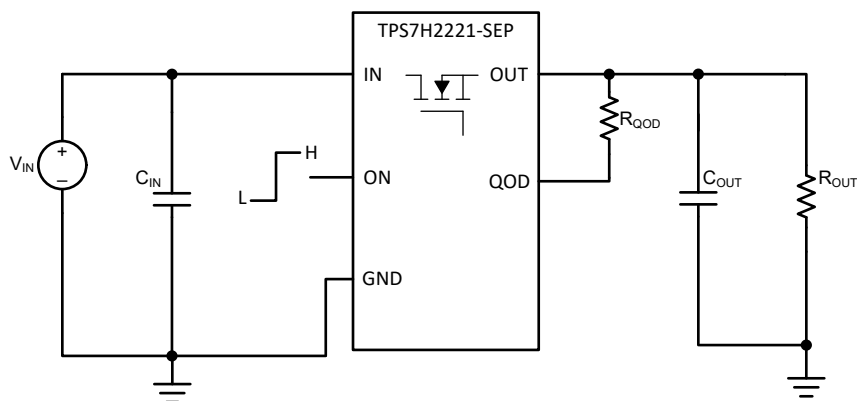
図 9-1. Typical Application Schematic

9.2.1 Design Requirements

For this design example, use the values listed in Design Parameters as the design parameters:

表 9-1. Design Parameters

DESIGN PARAMETER	EXAMPLE VALUE
Input voltage (V_{IN})	3.3 V
Load current resistance (R_{OUT})	1 kΩ
Load capacitance (C_{OUT})	47 µF
Minimum fall time (t_F)	40 ms
Maximum inrush current (I_{RUSH})	150 mA

9.2.2 Detailed Design Procedure

9.2.2.1 Limiting Inrush Current

Use 式 3 to find the maximum slew rate value to limit inrush current for a given capacitance:

$$\text{(Slew Rate)} = I_{RUSH} \div C_{OUT} \tag{3}$$

where

- I_{INRUSH} = maximum acceptable inrush current (mA)
- C_{OUT} = capacitance on V_{OUT} (µF)
- Slew Rate = Output Slew Rate during turn on (mV/µs)

Based on 式 3, the required slew rate to limit the inrush current to 150 mA is 3.2 mV/µs. The TPS7H2221-SEP has a slew rate of 2.3 mV/µs, so the inrush current will be below 150 mA.

9.2.2.2 Setting Fall Time for Shutdown Power Sequencing

Microcontrollers and processors often have a specific shutdown sequence in which power must be removed. Using the adjustable Quick Output Discharge function of the TPS7H2221-SEP device, adding a load switch to each power rail can be used to manage the power down sequencing. To determine the QOD values for each load switch, first confirm the power down order of the device you wish to power sequence. Be sure to check if there are voltage or timing margins that must be maintained during power down.

Once the required fall time is determined, the maximum external discharge resistance (R_{DIS}) value can be found using 式 2:

$$t_{FALL(min)} = 2.2 \times (R_{DIS} \parallel R_{OUT}) \times C_{OUT} \tag{4}$$

$$R_{DIS(min)} = 630\ \Omega \tag{5}$$

式 1 can then be used to calculate the R_{QOD} resistance needed to achieve a particular discharge value:

$$R_{DIS} = QOD + R_{QOD} \tag{6}$$

$$R_{QOD} = 624\ \Omega \tag{7}$$

To ensure a fall time greater than, choose an R_{QOD} value greater than 624 Ω.

9.2.2.3 Application Curves

C_IN = 58.1 µF   C_OUT = 47.1 µF   R_OUT = 1 kΩ

図 9-2. Fall Time (R_QOD = 1 kΩ)

9.3 Application Curves

C_IN = 58.1 µF   C_OUT = 47.1 µF   R_OUT = 1 kΩ
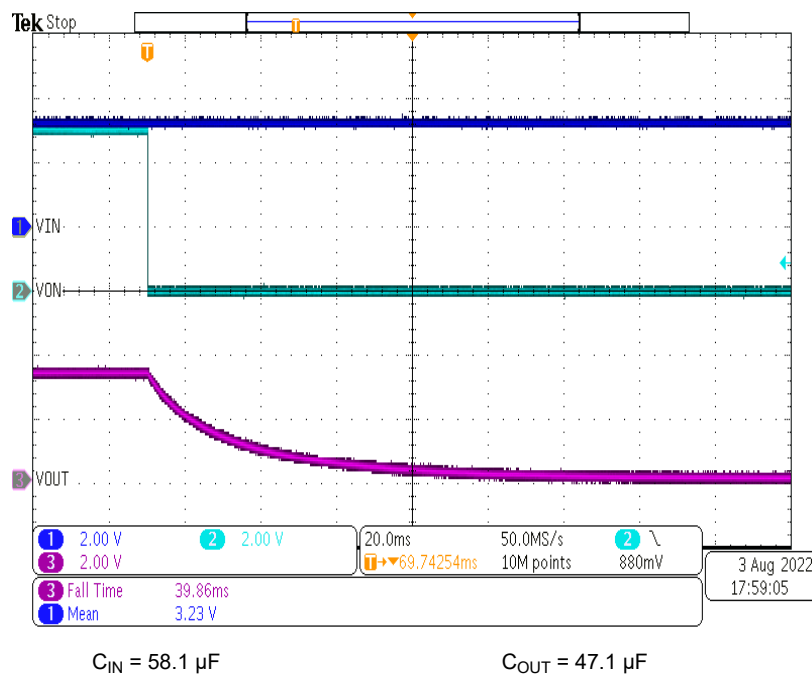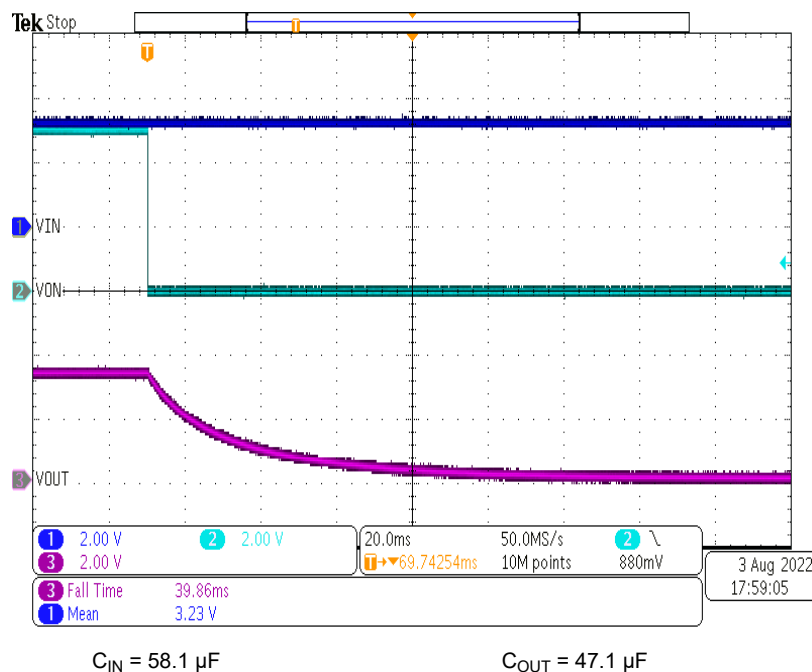
図 9-3. Fall Time (R_QOD = 1 kΩ)

9.4 Power Supply Recommendations

The device is designed to operate with a V_{IN} range of 1.6 V to 5.5 V. The V_{IN} power supply must be well regulated. The power supply must be able to withstand all transient load current steps. In most situations, using an minimum input capacitance (C_{IN}) of 1 μF is sufficient to prevent the supply voltage from dipping when the switch is turned on. In cases where the power supply is slow to respond to a large transient current or large load current step, additional bulk capacitance may be required on the input.

9.5 Layout

9.5.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for IN, OUT, and GND helps minimize the parasitic electrical effects.

9.5.2 Layout Example
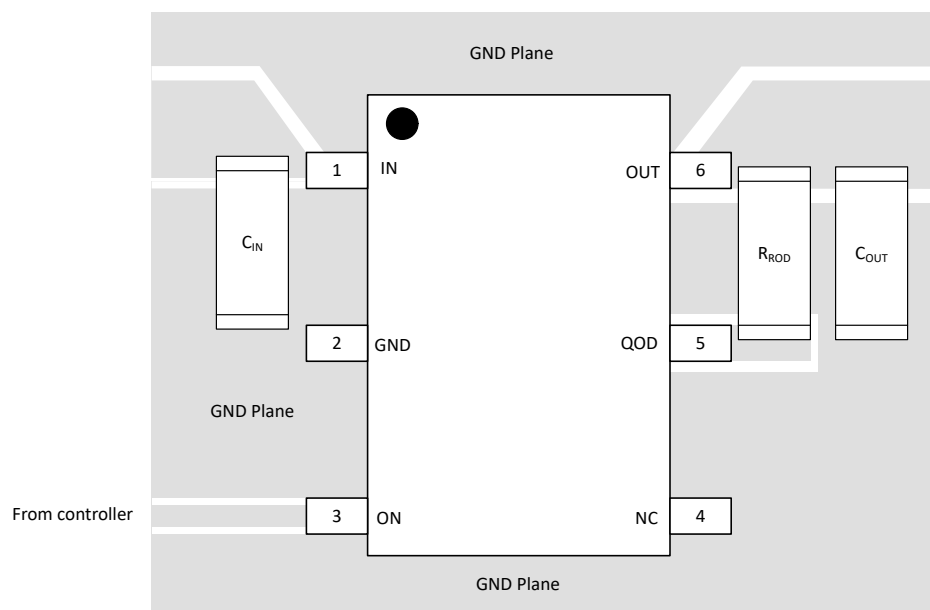
図 9-4. Recommended Board Layout

Product Folder Links: *TPS7H2221-SEP*

10 Device and Documentation Support

10.1 Related Documentation

For related documentation see the following:

- Texas Intruments, TPS7H2221-SEP Total Ionizing Dose (TID)
- Texas Intruments, TPS7H2221-SEP Single-Event Effects (SEE) Test Report
- Texas Intruments, TPS7H2221-SEP Neutron Displacement Damage (NDD) Characterization
- Texas Intruments, TPS7H2221-SEP Evaluation Module (EVM)
- Texas Intruments, TPS7H2221-SEP PSpice Transient Model
- Texas Intruments, Basics of Load Switches

10.2 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.3 サポート・リソース

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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary   This glossary lists and explains terms, acronyms, and definitions.

10.6 Export Control Notice

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11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

Product Folder Links: *TPS7H2221-SEP*

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS7H2221MDCKTSEP	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-55 to 125		Samples
V62/22609-01XE	ACTIVE	SC70	DCK	6	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM			Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) RoHS: TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

REEL DIMENSIONS

TAPE DIMENSIONS

A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS7H2221MDCKTSEP	SC70	DCK	6	250	180.0	8.4	2.47	2.3	1.25	4.0	8.0	Q3

PACKAGE MATERIALS INFORMATION

TAPE AND REEL BOX DIMENSIONS

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS7H2221MDCKTSEP	SC70	DCK	6	250	202.0	201.0	28.0

DCK (R−PDSO−G6)   PLASTIC SMALL−OUTLINE PACKAGE
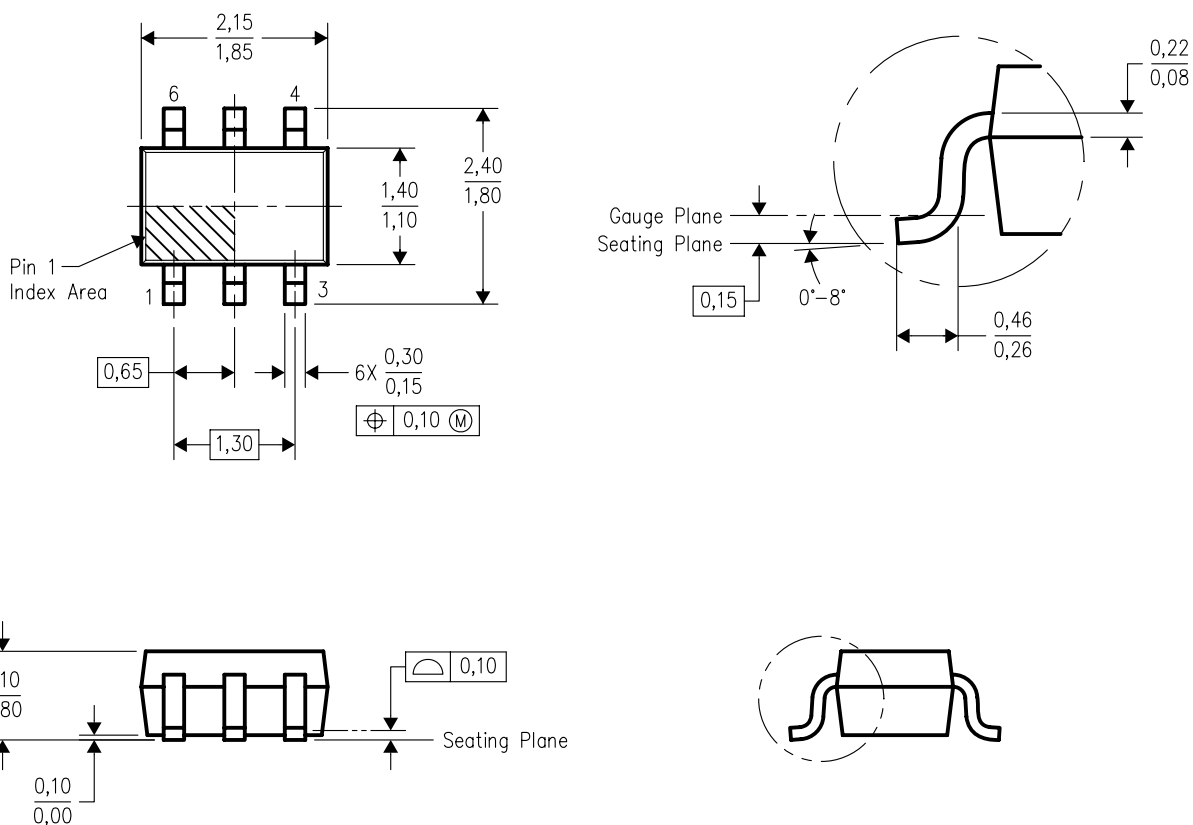
4093553−4/G   01/2007

NOTES: A.   All linear dimensions are in millimeters.
         B.   This drawing is subject to change without notice.
         C.   Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
         D.   Falls within JEDEC MO−203 variation AB.

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DCK (R−PDSO−G6)   PLASTIC SMALL OUTLINE

Example Board Layout

Stencil Openings
Based on a stencil thickness
of .127mm (.005inch).

6x0,35

0,85

2,2

2,2

4x0,65

2x1,30

4x0,65

2x1,30

Solder Mask Opening

0,4

1,0   0,9

Pad Geometry

0,05

0,50

4210356−3/C 07/11

NOTES: A. All linear dimensions are in millimeters.
         B. This drawing is subject to change without notice.
         C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
         D. Publication IPC−7351 is recommended for alternate designs.
         E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should
             contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric
             metal load solder paste. Refer to IPC−7525 for other stencil recommendations.