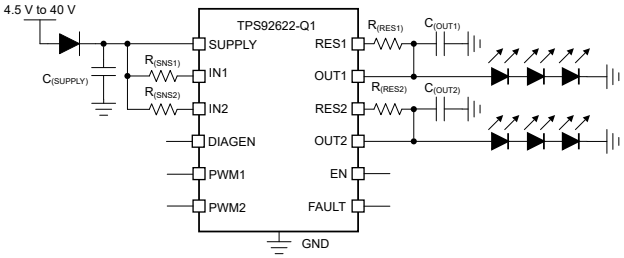
TEXAS INSTRUMENTS
TPS92622-Q1
JAJSOK9A – NOVEMBER 2022 – REVISED NOVEMBER 2023

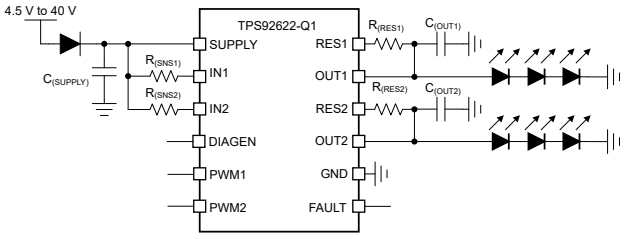
TPS92622-Q1 2 チャネル、車載用、ハイサイド LED ドライバ、熱共有機能付き

1 特長

- 車載アプリケーション用に AEC-Q100 認定済み:
  - 温度グレード 1:-40℃～125℃、T_A
- 広い入力電圧範囲:4.5V～40V
- 外部シャント抵抗による熱均衡
- フォルト・モード時の Low 電源電流
- スリープ モードでの超低シャットダウン電流 (HVSSOP パッケージのみ)
- 2 つの高精度電流レギュレーション:
  - チャネルあたり最大 150mA の電流出力
  - 全温度範囲にわたって ±5% の精度
  - 抵抗による独立した電流設定
  - 輝度制御用の独立した PWM ピン
- Low ドロップアウト電圧:
  - 最大ドロップアウト:150mA で 350mV
- 診断および保護機能
  - LED の開路検出と自動回復
  - LED のグランドへの短絡検出と自動回復
  - スレッショルドを調整可能な診断機能
  - 1 つの障害で全体を障害とする方式と、障害の発生したチャネルのみをオフにする方式 (N-1) のどちらかに構成可能なフォルト・バス
  - サーマル・シャットダウン
- 動作時の接合部温度範囲:–40℃～150℃



代表的なアプリケーション図 (HVSSOP パッケージ)



代表的なアプリケーション図 (WSON パッケージ)

2 アプリケーション

- 車載用外部テール・ライト:リア・ランプ、センター・ハイマウント・ストップ・ランプ、サイド・マーカー
- 車載用外部小型ライト:ドア・ハンドル、ブラインド・スポット検出インジケータ、充電口
- 車内照明:オーバーヘッド・コンソール、マップ・ランプ
- 汎用 LED ドライバ・アプリケーション

3 概要

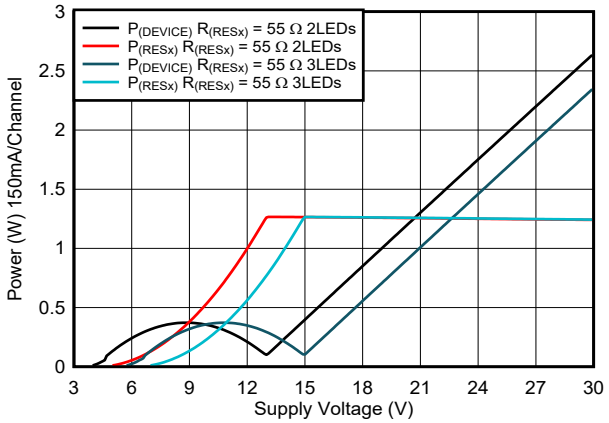
TPS92622-Q1 2 チャネル LED ドライバには、デバイスの温度上昇を低減するための独自の熱管理設計が組み込まれています。TPS92622-Q1 は、チャネルあたり最大 150mA の全負荷電流を出力するために、電圧変動が大きい自動車のバッテリから直接給電するリニア・ドライバです。外付けシャント抵抗を利用して出力電流を分配し、ドライバの外で電力を消費します。本デバイスの豊富な診断機能には、LED 開放、LED グランド短絡、デバイス過熱保護が含まれます。

TPS92622-Q1 のどれか 1 つに障害が発生すれば全体を障害とする機能は、TPS9261x-Q1、TPS9262x-Q1、TPS9263x-Q1、TPS92830-Q1 といった他の LED ドライバとの連係が可能であるため、さまざまな要求に対応できます。

パッケージ情報

部品番号	パッケージ(1)	本体サイズ (公称)
TPS92622-Q1	DGN (HVSSOP、12)	3.00mm × 4.00mm
	DRR (WSON、12)	3.00mm × 3.00mm

(1) 利用可能なすべてのパッケージについては、データシートの末尾にある注文情報を参照してください。



デバイスの消費電力

Table of Contents

4 Pin Configuration and Functions

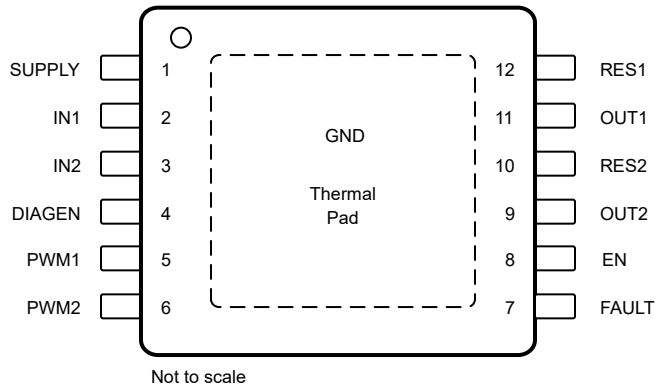


図 4-1. DGN Package 12-Pin HVSSOP With PowerPAD™ Integrated Circuit Package (Top View)

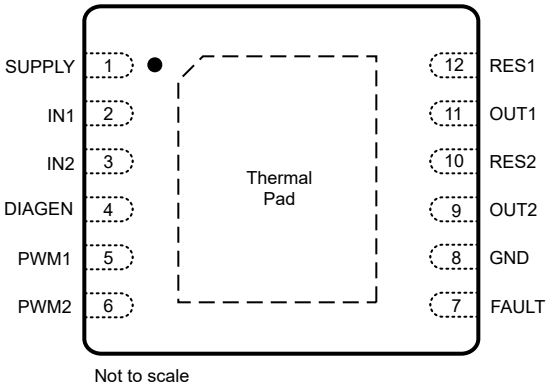


図 4-2. DRR Package 12-Pin WSON With PowerPAD™ Integrated Circuit Package (Top View)

表 4-1. HVSSOP Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
SUPPLY	1	I	Device power supply
IN1	2	I	Current input for channel 1
IN2	3	I	Current input for channel 2
DIAGEN	4	I	Enable pin for LED open-circuit detection to avoid false open diagnostics during low-dropout operation.
PWM1	5	I	PWM input for OUT1 and RES1 current output ON and OFF control
PWM2	6	I	PWM input for OUT2 and RES2 current output ON and OFF control
$\overline{\text{FAULT}}$	7	I/O	Fault output, support one-fails–all-fail fault bus
EN	8	I	Device enable pin
OUT2	9	O	Current output for channel 2
RES2	10	O	Current output for channel 2 with external thermal resistor
OUT1	11	O	Current output for channel 1
RES1	12	O	Current output for channel 1 with external thermal resistor
DAP	13	-	GND/ Thermal Pad

表 4-2. WSON Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
SUPPLY	1	I	Device power supply
IN1	2	I	Current input for channel 1
IN2	3	I	Current input for channel 2
DIAGEN	4	I	Enable pin for LED open-circuit detection to avoid false open diagnostics during low-dropout operation.
PWM1	5	I	PWM input for OUT1 and RES1 current output ON and OFF control
PWM2	6	I	PWM input for OUT2 and RES2 current output ON and OFF control
$\overline{\text{FAULT}}$	7	I/O	Fault output, support one-fails–all-fail fault bus
GND	8	-	Ground
OUT2	9	O	Current output for channel 2
RES2	10	O	Current output for channel 2 with external thermal resistor
OUT1	11	O	Current output for channel 1
RES1	12	O	Current output for channel 1 with external thermal resistor

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
Supply	SUPPLY	–0.3	45	V
High-voltage input	DIAGEN, IN1, IN2, PWM1, PWM2, EN	–0.3	$V_{(SUPPLY)}$ + 0.3	V
High-voltage output	OUT1, OUT2, RES1, RES2	–0.3	$V_{(SUPPLY)}$ + 0.3	V
Fault bus	$\overline{FAULT}$	–0.3	$V_{(SUPPLY)}$ + 0.3	V
T_J	Operating junction temperature	–40	150	°C
T_{stg}	Storage temperature	–40	150	°C

(1) Operation outside the Absolute Maximum Ratings may cause permanent device damage. Absolute Maximum Ratings do not imply functional operation of the device at these or any other conditions beyond those listed under Recommended Operating Conditions. If used outside the Recommended Operating Conditions but within the Absolute Maximum Ratings, the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

5.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per AEC Q100-002(1) HBM ESD Classification Level 1C		±2000	V
		Charged-device model (CDM), per AEC Q100-011 CDM ESD Classification Level C4B	All pins	±500	
			Corner pins (SUPPLY, RES1, $\overline{FAULT}$, PWM2)	±750	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

5.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
SUPPLY	Device supply voltage	4.5		40	V
IN1, IN2	Sense voltage	$V_{(SUPPLY)}$ - $V_{(CS\_REG)}$			V
EN	Device EN pin	0		$V_{(SUPPLY)}$	V
PWM1, PWM2	PWM inputs	0		$V_{(SUPPLY)}$	V
DIAGEN	Diagnostics enable pin	0		$V_{(SUPPLY)}$	V
OUT1, OUT2, RES1, RES2	Driver output	0		$V_{(SUPPLY)}$	V
$\overline{FAULT}$	Fault bus	0		$V_{(SUPPLY)}$	V
Operating ambient temperature, T_A		–40		125	°C

5.4 Thermal Information

THERMAL METRIC(1)		TPS92622-Q1		UNIT
		DRR (WSON)	DGN (HVSSOP)	
		12 PINS	12 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	51.2	39.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	50.7	60.9	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	25.2	15.5	°C/W
ψ_{JT}	Junction-to-top characterization parameter	1.3	2.6	°C/W
ψ_{JB}	Junction-to-board characterization parameter	25.2	15.5	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	9.4	2.6	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.5 Electrical Characteristics

$V_{(SUPPLY)}$ = 5 V to 40 V, $V_{(EN)}$ = 3.3 V, T_J = –40°C to +150°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
BIAS						
$V_{(POR\_rising)}$	Supply voltage POR rising threshold			3.6	4.0	V
$V_{(POR\_falling)}$	Supply voltage POR falling threshold		3.0	3.4		V
$I_{(SD)}$	Device shutdown current	$V_{(EN)}$ = 0 V		13.5	18.0	uA
$I_{(Quiescent)}$	Device standby ground current	PWM = HIGH		1.2	1.6	mA
$I_{(FAULT)}$	Device supply current in fault mode	PWM = HIGH, $\overline{FAULT}$ externally pulled LOW	0.21	0.32	0.45	mA
LOGIC INPUTS (DIAGEN, PWM, EN)						
$V_{IL(EN)}$	Input logic-low voltage, EN				0.7	V
$V_{IH(EN)}$	Input logic-high voltage, EN		2.0			V
$I_{(EN\_pulldown)}$	EN pull down current	$V_{(EN)}$ = 12 V	1.5	3.0	4.5	uA
$V_{IL(DIAGEN)}$	Input logic-low voltage, DIAGEN		1.045	1.1	1.155	V
$V_{IH(DIAGEN)}$	Input logic-high voltage, DIAGEN		1.14	1.2	1.26	V
$V_{IL(PWM)}$	Input logic-low voltage, PWM		1.045	1.1	1.155	V
$V_{IH(PWM)}$	Input logic-high voltage, PWM		1.14	1.2	1.26	V
CONSTANT-CURRENT DRIVER						
$I_{(OUTx\_Tot)}$	Device output-current for each channel	100% duty cycle	5		150	mA
$V_{(CS\_REG)}$	Sense-resistor regulation voltage	T_A = –40°C to +125°C	144	150	156	mV
ALL $\Delta V_{(CS\_c2c)}$	Channel to channel mismatch	$\Delta V_{(CS\_c2c)} = 1 - V_{(CS\_REGx)} / V_{avg(CS\_REG)}$	–3		+3	%
ALL $\Delta V_{(CS\_d2d)}$	Device to device mismatch	$\Delta V_{(CS\_d2d)} = 1 - V_{avg(CS\_REG)} / V_{nom(CS\_REG)}$	–4		+4	%
$R_{(CS\_REG)}$	Sense-resistor range		0.96		31.2	Ω
$V_{(DROPOUT)}$	Voltage dropout from INx to OUTx, RESx open	current setting of 100 mA		120	250	mV
		current setting of 150 mA		180	350	mV
	Voltage dropout from INx to RESx, OUTx open	current setting of 100 mA		230	450	mV
		current setting of 150 mA		350	700	mV
$I_{(RESx)}$	Ratio of RESx current to total current	$I_{(RESx)}/I_{(OUTx\_Tot)}$, $V_{(INx)} - V_{(RESx)} > 1$ V, Itotal=150mA	95			%
DIAGNOSTICS						
$V_{(OPEN\_th\_rising)}$	LED open rising threshold, $V_{(IN)} - V_{(OUT)}$		180	300	420	mV
$V_{(OPEN\_th\_falling)}$	LED open falling threshold, $V_{(IN)} - V_{(OUT)}$			450		mV
$V_{(SG\_th\_rising)}$	Channel output short-to-ground rising threshold		1.14	1.2	1.26	V
$V_{(SG\_th\_falling)}$	Channel output short-to-ground falling threshold		0.855	0.9	0.945	V
$I_{(Retry\_OUTx)}$	Channel output $V_{(OUT)}$ short-to-ground retry current		0.64	1.14	1.528	mA
$I_{(Retry\_RESx)}$	Channel output $V_{(RES)}$ short-to-ground retry current		0.64	1.14	1.528	mA
FAULT						
$V_{IL(FAULT)}$	Logic input low threshold				0.7	V
$V_{IH(FAULT)}$	Logic input high threshold		2			V
$t_{(FAULT\_rising)}$	Fault detection rising edge deglitch time			10		µs
$t_{(FAULT\_falling)}$	Fault detection falling edge deglitch time			20		µs
$I_{(FAULT\_pulldown)}$	$\overline{FAULT}$ internal pulldown current	$V_{(\overline{FAULT})}$ = 0.4 V	2	3	4	mA
$I_{(FAULT\_pullup)}$	$\overline{FAULT}$ internal pullup current		6	10	14	µA
$I_{(FAULT\_leakage)}$	$\overline{FAULT}$ leakage current	$V_{(\overline{FAULT})}$ = 40 V		0.01	2	µA
TIMING						
$t_{(PWM\_delay\_rising)}$	PWM rising edge delay to 10% of output current, t_1 as shown in 図 6-1	$V_{(SUPPLY)}$ = 12 V, $V_{(OUT)}$ = 6 V, $V_{(CS\_REG)}$ = 150 mV, $R_{(SNSx)}$ = 1 Ω, and $R_{(RESx)}$ = 68 Ω		3.7		µs
		$V_{(SUPPLY)}$ = 12 V, $V_{(OUT)}$ = 6 V, $V_{(CS\_REG)}$ = 150 mV, $R_{(SNSx)}$ = 30 Ω and $R_{(RESx)}$ = 56 Ω		2.2		µs

5.5 Electrical Characteristics (続き)

$V_{(SUPPLY)}$ = 5 V to 40 V, $V_{(EN)}$ = 3.3 V, T_J = –40°C to +150°C unless otherwise noted

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$t_{(PWM\_delay\_falling)}$	PWM falling edge delay to 90% of output current, t_2 as shown in 図 6-1	$V_{(SUPPLY)}$ = 12 V, $V_{(OUT)}$ = 6 V, $V_{(CS\_REG)}$ = 150 mV, $R_{(SNSx)}$ = 1 Ω, and $R_{(RESx)}$ = 68 Ω		4.0		µs
		$V_{(SUPPLY)}$ = 12 V, $V_{(OUT)}$ = 6 V, $V_{(CS\_REG)}$ = 150 mV, $R_{(SNSx)}$ = 30 Ω and $R_{(RESx)}$ = 56 Ω		3.6		µs
$t_{(Current\_rising)}$	Output current rising from 10% to 90%, t_3 as shown in 図 6-1	$V_{(SUPPLY)}$ = 12 V, $V_{(OUT)}$ = 6 V, $V_{(CS\_REG)}$ = 150 mV, $R_{(SNSx)}$ = 1 Ω, and $R_{(RESx)}$ = 68 Ω		1.8		µs
		$V_{(SUPPLY)}$ = 12 V, $V_{(OUT)}$ = 6 V, $V_{(CS\_REG)}$ = 150 mV, $R_{(SNSx)}$ = 30 Ω and $R_{(RESx)}$ = 56 Ω		1.8		µs
$t_{(Current\_falling)}$	Output current falling from 90% to 10%, t4 as shown in 図 6-1	$V_{(SUPPLY)}$ = 12 V, $V_{(OUT)}$ = 6 V, $V_{(CS\_REG)}$ = 150 mV, $R_{(SNSx)}$ = 1 Ω, and $R_{(RESx)}$ = 68 Ω		5.7		µs
		$V_{(SUPPLY)}$ = 12 V, $V_{(OUT)}$ = 6 V, $V_{(CS\_REG)}$ = 150 mV, $R_{(SNSx)}$ = 30 Ω and $R_{(RESx)}$ = 56 Ω		0.3		µs
$t_{(STARTUP)}$	SUPPLY rising edge to 10% output current, t_5 as shown in 図 6-1	$V_{(SUPPLY)}$ = 12 V, $V_{(OUT)}$ = 6 V, $V_{(CS\_REG)}$ = 150 mV, $R_{(SNSx)}$ = 1 Ω, and $R_{(RESx)}$ = 68 Ω		96		µs
		$V_{(SUPPLY)}$ = 12 V, $V_{(OUT)}$ = 6 V, $V_{(CS\_REG)}$ = 150 mV, $R_{(SNSx)}$ = 30 Ω and $R_{(RESx)}$ = 56 Ω		85		µs
$t_{(OPEN\_deg)}$	LED-open fault detection deglitch time, t_6 as shown in 図 6-4			125		µs
$t_{(SG\_deg)}$	Output short-to-ground detection deglitch time, t_7 as shown in 図 6-3			125		µs
$t_{(Recover\_deg)}$	Open and Short fault recovery deglitch time, t_8 as shown in 図 6-3 and 図 6-4			125		µs
$t_{(FAULT\_deg)}$	Fault pin deglitch time			20		µs
$t_{(FAULT\_recovery)}$	Fault recovery delay time, t_9 as shown in 図 6-3 and 図 6-4			50		µs
$t_{(TSD\_deg)}$	Thermal over temperature deglitch time			50		µs
THERMAL PROTECTION						
$T_{(TSD)}$	Thermal shutdown junction temperature threshold		157	172	187	°C
$T_{(TSD\_HYS)}$	Thermal shutdown junction temperature hysteresis			15		°C

5.6 Typical Characteristics

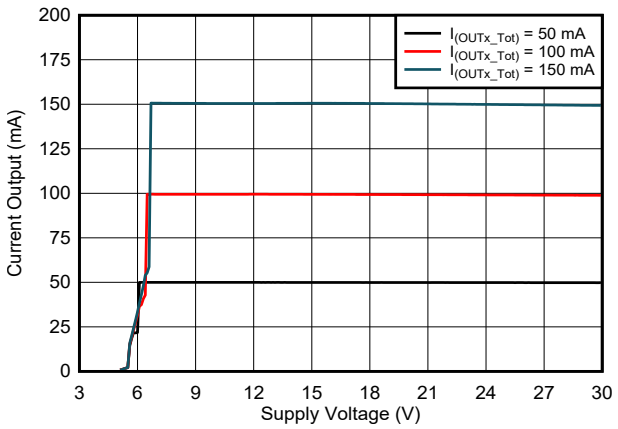


図 5-1. Output Current vs Supply Voltage

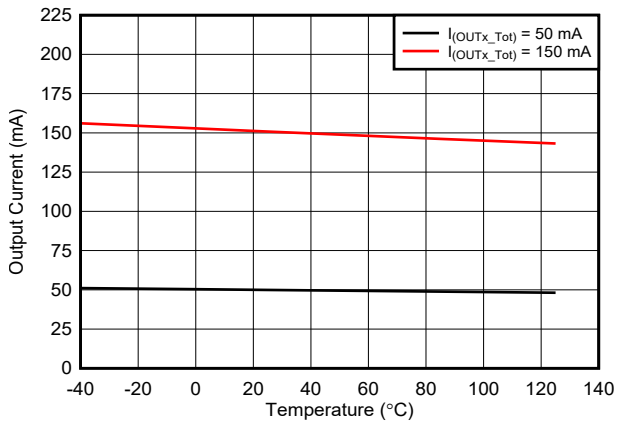


図 5-2. Output Current vs Temperature

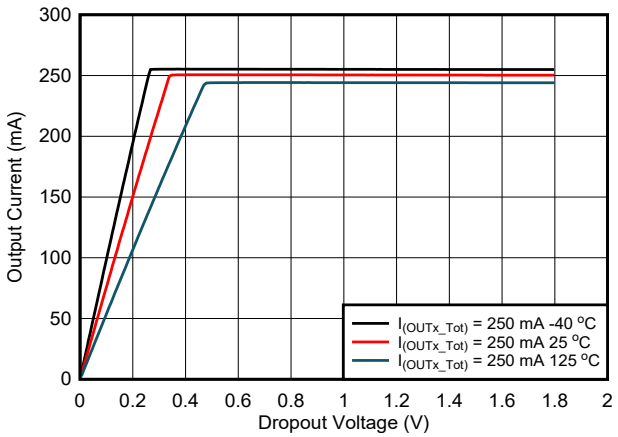


図 5-3. Output Current vs Dropout Voltage

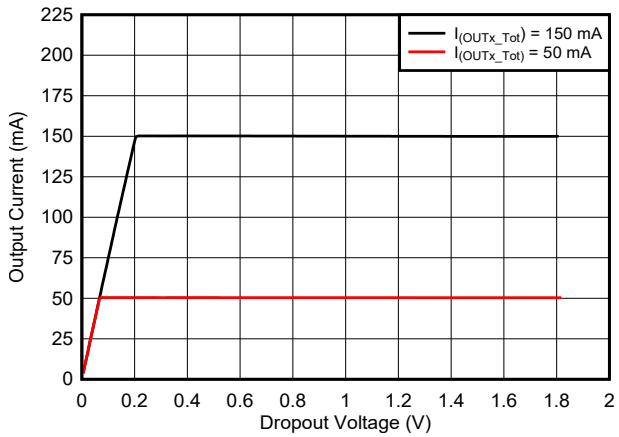


図 5-4. Output Current vs Dropout Voltage

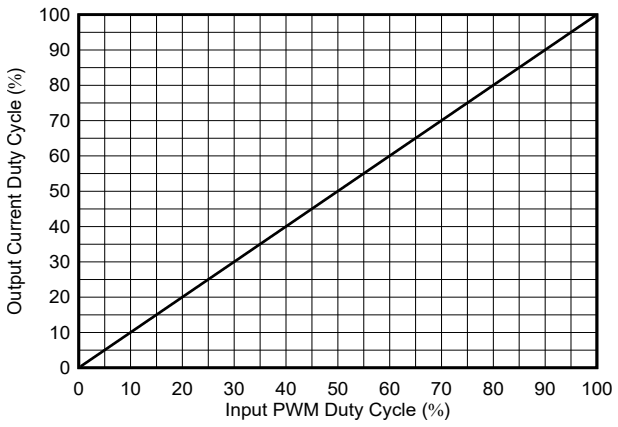


図 5-5. PWM Output Duty Cycle vs PWM Input Duty Cycle

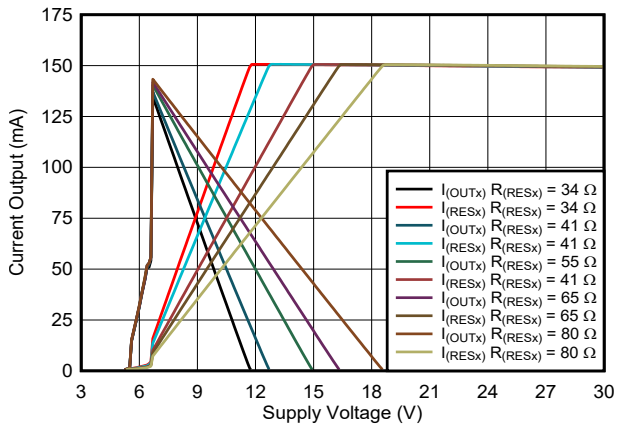


図 5-6. Output Current Distribution vs Supply Voltage

5.6 Typical Characteristics (continued)

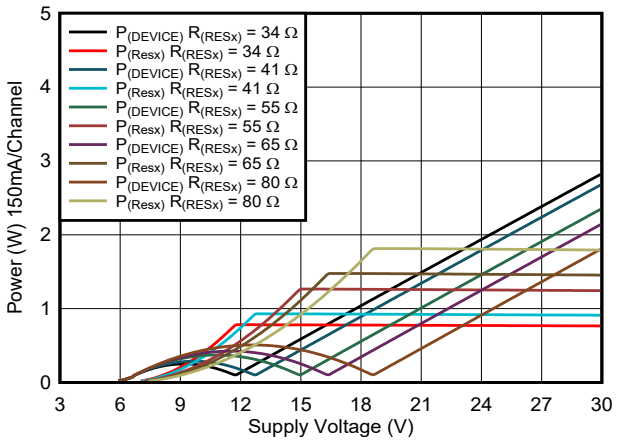


図 5-7. Power Dissipation vs Supply Voltage

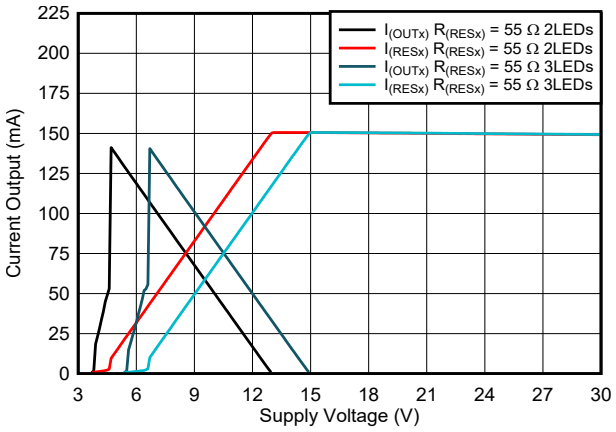


図 5-8. Output Current Distribution vs Supply Voltage

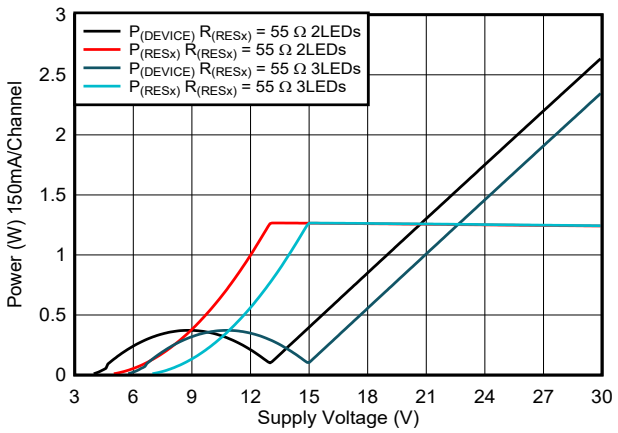
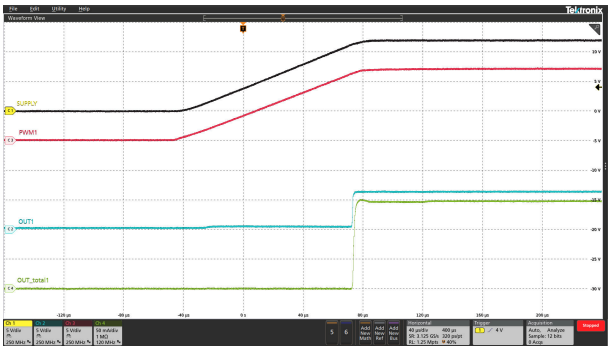
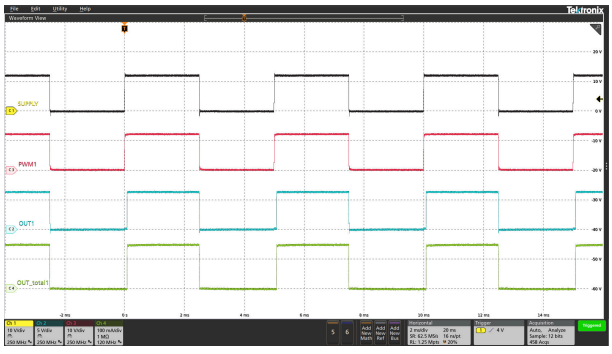


図 5-9. Power Dissipation vs Supply Voltage



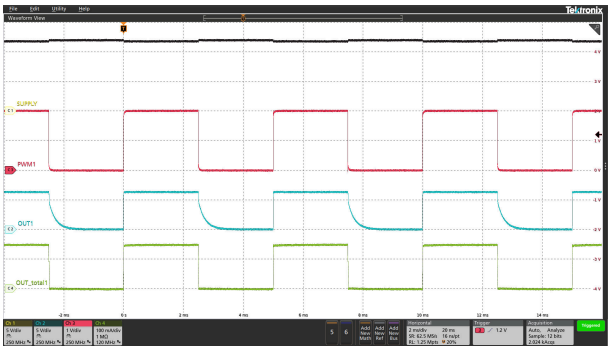
Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(OUT1)}$ Ch3 = $V_{(PWM1)}$
Ch4 = $I_{(OUT\_Tot)}$

図 5-10. Power-Up Sequence



Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(OUT1)}$ Ch3 = $V_{(PWM1)}$
Ch4 = $I_{(OUT\_Tot)}$

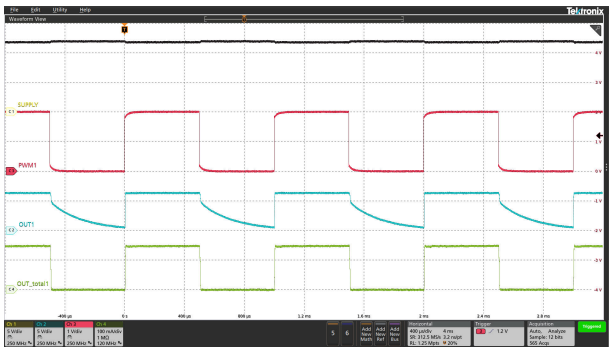
図 5-11. Supply Dimming at 200 Hz



Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(OUT1)}$ Ch3 = $V_{(PWM1)}$
Ch4 = $I_{(OUT\_Tot)}$

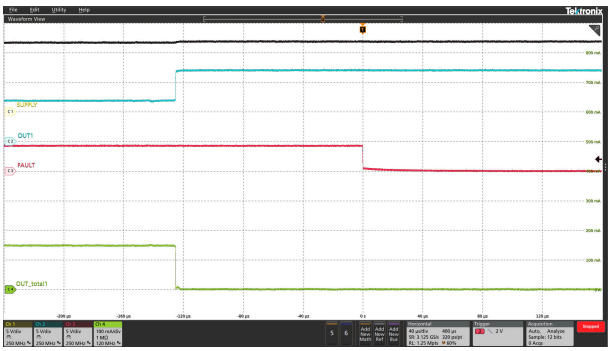
図 5-12. PWM Dimming at 200 Hz

5.6 Typical Characteristics (continued)



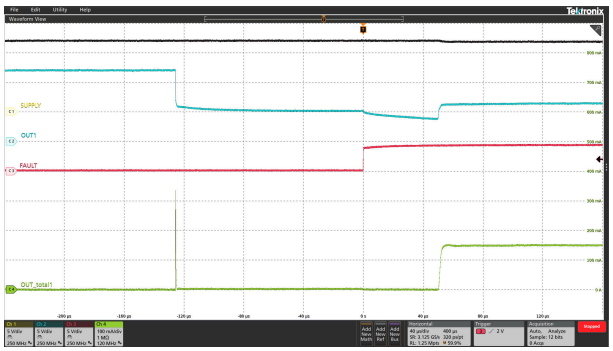
Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(OUT1)}$ Ch3 = $V_{(PWM1)}$
Ch4 = $I_{(OUT\_Tot)}$

図 5-13. PWM Dimming at 1 kHz



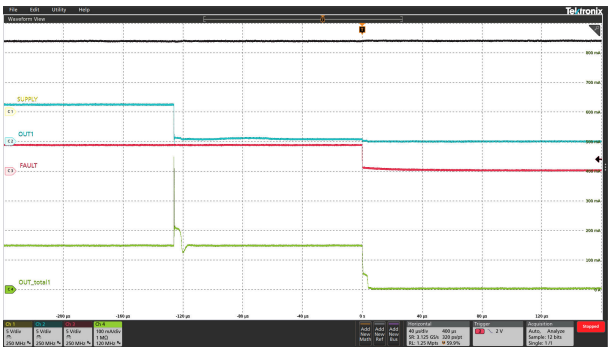
Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(OUT1)}$ Ch3 = $V_{(\overline{FAULT})}$
Ch4 = $I_{(OUT\_Tot)}$

図 5-14. LED Open Protection



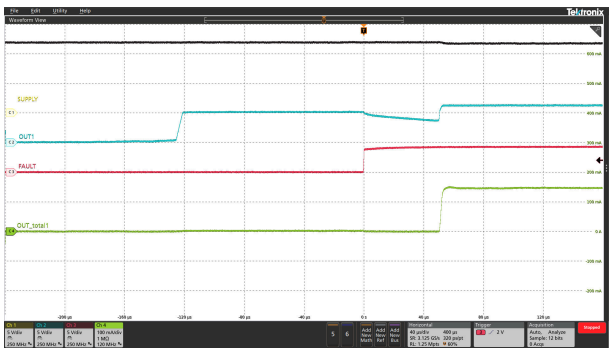
Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(OUT1)}$ Ch3 = $V_{(\overline{FAULT})}$
Ch4 = $I_{(OUT\_Tot)}$

図 5-15. LED Open Protection Recovery



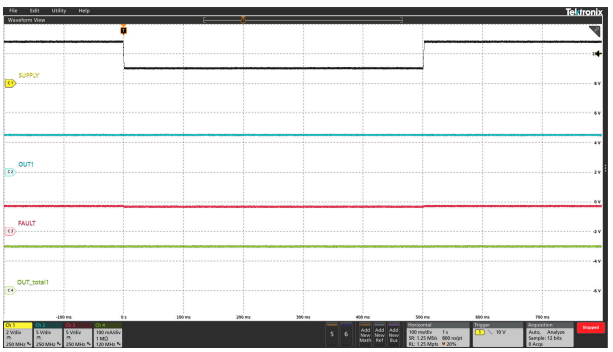
Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(OUT1)}$ Ch3 = $V_{(\overline{FAULT})}$
Ch4 = $I_{(OUT\_Tot)}$

図 5-16. LED Short-Circuit Protection



Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(OUT1)}$ Ch3 = $V_{(\overline{FAULT})}$
Ch4 = $I_{(OUT\_Tot)}$

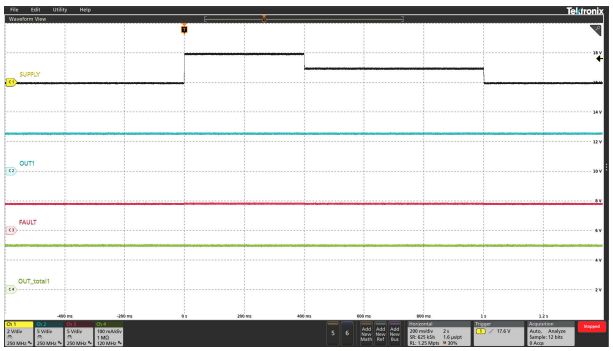
図 5-17. LED Short-Circuit Protection Recovery



Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(OUT1)}$ Ch3 = $V_{(\overline{FAULT})}$
Ch4 = $I_{(OUT\_Tot)}$ DIAGEN = High when Supply > 8 V

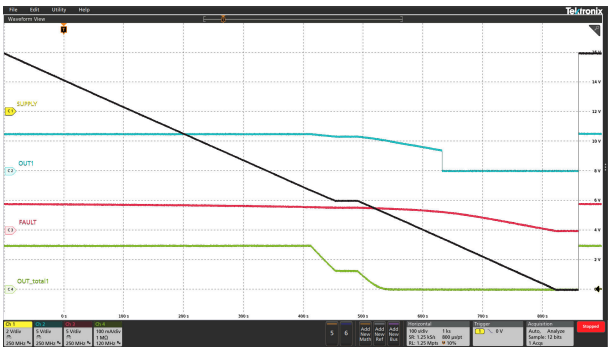
図 5-18. Transient Undervoltage

5.6 Typical Characteristics (continued)



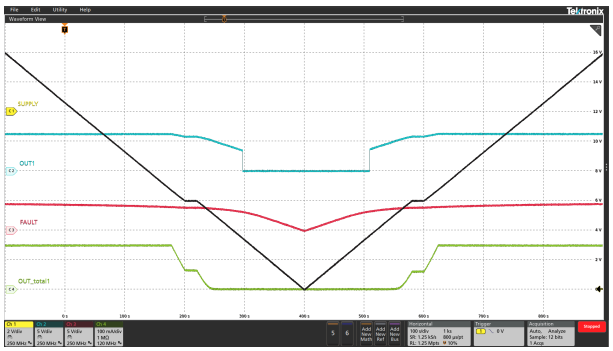
Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(OUT1)}$ Ch3 = $V_{(\overline{FAULT})}$
Ch4 = $I_{(OUT\_Tot)}$ DIAGEN = High when Supply > 8 V

図 5-19. Transient Overvoltage



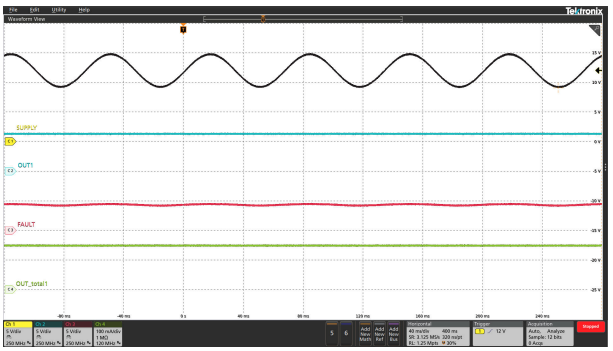
Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(OUT1)}$ Ch3 = $V_{(\overline{FAULT})}$
Ch4 = $I_{(OUT\_Tot)}$ DIAGEN = High when Supply > 8 V

図 5-20. Slow Decrease and Quick Increase of Supply Voltage



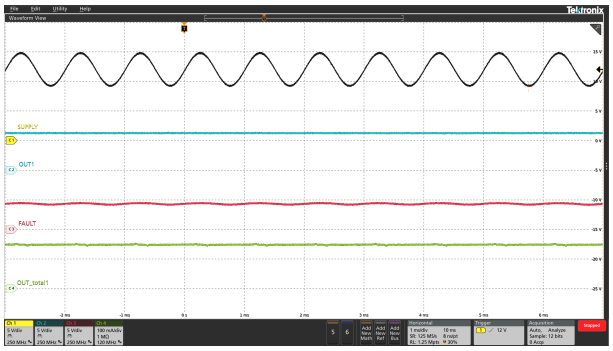
Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(OUT1)}$ Ch3 = $V_{(\overline{FAULT})}$
Ch4 = $I_{(OUT\_Tot)}$ DIAGEN = High when Supply > 8 V

図 5-21. Slow Decrease and Slow Increase of Supply Voltage



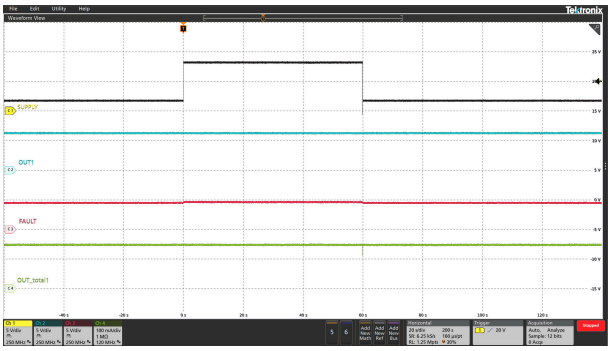
Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(OUT1)}$ Ch3 = $V_{(\overline{FAULT})}$
Ch4 = $I_{(OUT\_Tot)}$ DIAGEN = High when Supply > 8 V

図 5-22. Superimposed Alternating Voltage 15 Hz



Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(OUT1)}$ Ch3 = $V_{(\overline{FAULT})}$
Ch4 = $I_{(OUT\_Tot)}$ DIAGEN = High when Supply > 8 V

図 5-23. Superimposed Alternating Voltage 1 kHz



Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(OUT1)}$ Ch3 = $V_{(\overline{FAULT})}$
Ch4 = $I_{(OUT\_Tot)}$ DIAGEN = High when Supply > 8 V

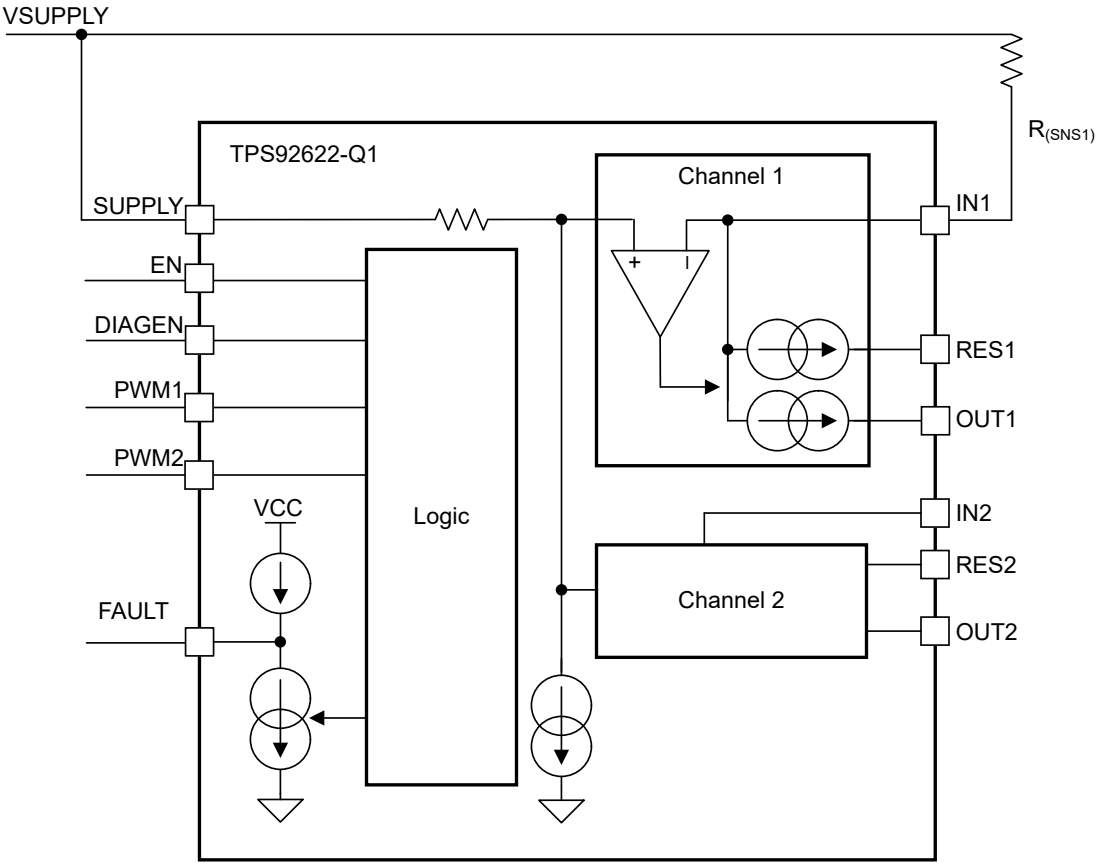
図 5-24. Jump Start

6 Detailed Description

6.1 Overview

The TPS92622-Q1 is a two-channel, high-side linear LED driver supporting external thermal sharing resistor to achieve the controllable junction temperature rising. The device can be directly powered by automotive battery and output full load up to 300-mA current to LED with limited power dissipation on the device. The current output at each channel can be independently set by external $R_{(SNSx)}$ resistors. Current flows from the supply through the $R_{(SNSx)}$ resistor into the integrated current regulation circuit and to the LEDs through OUTx pin and RESx pin. TPS92622-Q1 device supports both supply control and EN/PWM control to turn LED ON and OFF. The LED brightness is also adjustable by voltage duty cycle applied on either SUPPLY or EN/PWM pins with frequency above 100 Hz. The TPS92622-Q1 provides full diagnostics to keep the system operating reliably including LED open and short-circuit detection, supply POR and thermal shutdown protection. The TPS92622-Q1 can be used with other TPS9261x-Q1, TPS9262x-Q1, TPS9263x-Q1 and TPS92830-Q1 family devices together to achieve one-fails-all-fail protection by tying all $\overline{\text{FAULT}}$ pins together as a fault bus.

6.2 Functional Block Diagram



6.3 Feature Description

6.3.1 Power Supply (SUPPLY)

6.3.1.1 Power-On Reset (POR)

The TPS92622-Q1 device has an internal power-on-reset (POR) function. When power is applied to the SUPPLY pin, the internal POR circuit holds the device in reset state until $V_{(SUPPLY)}$ is above $V_{(POR\_rising)}$.

6.3.1.2 Suppply Current in Fault Mode

The TPS92622-Q1 device consumes minimal quiescent current, $I_{(FAULT)}$, into SUPPLY when the $\overline{FAULT}$ pin is externally pulled LOW. At the same time, the device shuts down all three output drivers.

If device detects an internal fault, it pulls down the $\overline{FAULT}$ pin by an internal typical 3-mA constant current as a fault indication to the fault bus.

6.3.2 Enable and Shutdow(EN)

The TPS92622-Q1 device with HVSSOP package has an enable input. When EN is low, the device is in sleep mode with ultra low shutdown current $I_{(SD)}$. This low current helps to save system-level current consumption in applications where battery voltage directly connects to the device without high-side switches.

The TPS92622-Q1 device with WSON package has no EN pin.The device starts to operate as long as the SUPPLY voltage is higher than $V_{(POR\_rising)}$. The TPS92622-Q1 shuts down when SUPPLY voltage is lower than $V_{(POR\_falling)}$.

6.3.3 Constant-Current Output and Setting (INx)

The TPS92622-Q1 device is a high-side current driver for driving LEDs. The device controls each output current through regulating the voltage drop on an external high-side current-sense resistor, $R_{(SNSx)}$ independently for each channel. An integrated error amplifier drives an internal power transistor to maintain the voltage drop on the current-sense resistor $R_{(SNSx)}$ to $V_{(CS\_REG)}$ and therefore regulates the current output to target value. When the output current is in regulation, use 式 1 to calculate the current value for each channel.

$$I_{(OUTx\_Tot)} = \frac{V_{(CS\_REG)}}{R_{(SNSx)}} \tag{1}$$

where

- $V_{(CS\_REG)}$ = 150 mV
- x = 1, or 2 for output channel 1 or 2

When the supply voltage drops below total LED string forward voltage plus required headroom voltage, the sum of $V_{(DROPOUT)}$ and $V_{(CS\_REG)}$, the TPS92622-Q1 is not able to deliver enough current output as set by the value of $R_{(SNSx)}$, and the voltage across the current-sense resistor $R_{(SNSx)}$ is less than $V_{(CS\_REG)}$.

6.3.4 Thermal Sharing Resistor (OUTx and RESx)

The TPS92622-Q1 device provides two current output paths for each channel. Current flows from the supply through the $R_{(SNSx)}$ resistor into the integrated current regulation circuit and to the LEDs through OUTx pin and RESx pin. The current output on both OUTx pin and RESx pin is independently regulated to achieve total required current output. The summed current of OUTx and RESx is equal to the current through the $R_{(SNSx)}$ resistor in the channel. The OUTx connects to anode of LEDs load in serial directly, however RESx connects to the LEDs through an external resistor to share part of the power dissipation and reduce the thermal accumulation in TPS92622-Q1.

The integrated independent current regulation in TPS92622-Q1 dynamically adjusts the output current on both OUTx and RESx output to maintain the stable summed current for LED. The TPS92622-Q1 always regulates the current output to the RESx pin as much as possible until the RESx current path is saturated, and the rest of required current is regulated out of the OUTx. As a result, the most of the current to LED outputs through the

RESx pin when the voltage dropout is large between SUPPLY and LED required total forward voltage. In the opposite case, the most of the current to LED outputs through the OUTx pin when the voltage headroom is relative low between SUPPLY and LED required forward voltage.

6.3.5 PWM Control (PWMx)

The pulse width modulation (PWM) input of the TPS92622-Q1 functions as enable for the output current. When the voltage applied on the PWM pin is higher than $V_{IH(PWM)}$, the relevant output current is enabled. When the voltage applied on PWM pin is lower than $V_{IL(PWM)}$, the output current is disabled as well as the diagnostic features. Besides output current enable and disable function, the PWM input of TPS92622-Q1 also supports adjustment of the average current output for brightness control if the frequency of applied PWM signal is higher than 100 Hz, which is out of visible frequency range of human eyes. TI recommends a 200-Hz PWM signal with 1% to 100% duty cycle input for brightness control. Please refer to 図 7-4 for typical PWM dimming application.

The TPS92622-Q1 device has two PWM input pins: PWM1, PWM2 to control each of current output channel independently. PWM1 input controls the output channel 1 for both OUT1 and RES1, PWM2 input controls the output channel 2 for both OUT2 and RES2. 図 6-1 illustrates the timing for PWM input and current output.

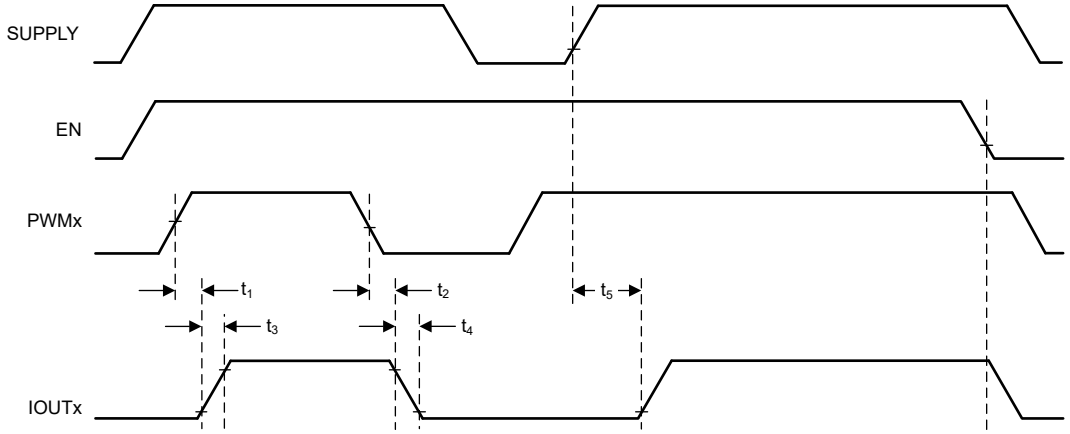


図 6-1. Power-On Sequence and PWM Dimming Timing

The detailed information and value of each time period in 図 6-1 is described in TIMING section of the *Electrical Characteristics*.

6.3.6 Supply Control

The TPS92622-Q1 can support supply control to turn ON and OFF output current. When the voltage applied on the SUPPLY pin is higher than the LED string forward voltage plus needed headroom voltage at required current, and the PWM pin voltage is high, the output current is turned ON and well regulated. However, if the voltage applied on the SUPPLY pin is lower than $V_{(POR\_falling)}$, the output current is turned OFF. With this feature, the power supply voltage in designed pattern can control the output current ON and OFF. The brightness is adjustable if the ON and OFF frequency is fast enough. Because of the high accuracy design of PWM threshold in TPS92622-Q1, TI recommends a resistor divider on the PWM pin to set the SUPPLY threshold higher than LED forward voltage plus required headroom voltage as shown in 図 6-2. The headroom voltage is basically the summation of $V_{(DROPOUT)}$ and $V_{(CS\_REG)}$. When the voltage on the PWM pin is higher than $V_{IH(PWM)}$, the output current is turned ON. However, when the voltage on the PWM is lower than $V_{IL(PWM)}$, the output current is turned OFF. Use 式 2 to calculate the SUPPLY threshold voltage.

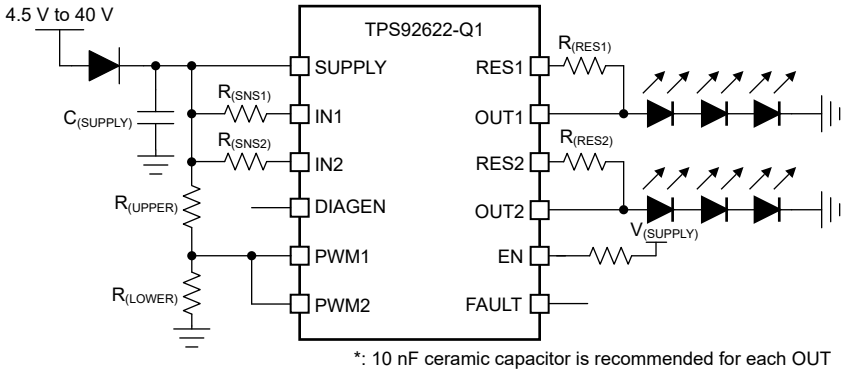


図 6-2. Application Schematic for Supply Control LED Brightness

$$V_{(SUPPLY\_PWM\_th\_rising)} = V_{IH(PWM)} \times \left(1 + \frac{R_{(UPPER)}}{R_{(LOWER)}}\right) \quad (2)$$

where

- $V_{IH(PWM)}$ = 1.26 V (maximum)

6.3.7 Diagnostics

The TPS92622-Q1 device provides advanced diagnostics and fault-protection features for automotive exterior lighting systems. The device can detect and protect fault from LED-string short-to-GND, LED-string open-circuit and junction overtemperature scenarios. The device also supports a one-fails–all-fail fault bus design that can flexibly fit different regulatory requirements.

6.3.7.1 LED Short-to-GND Detection

The TPS92622-Q1 device has LED short-to-GND detection. The LED short-to-GND detection monitors the output voltage when the output current is enabled. After a short-to-GND LED failure is detected, the device turns off the faulty channel and retries automatically, regardless of the state of the PWM input. If the retry mechanism detects the removal of the LED short-to-GND fault, the device resumes to normal operation.

The TPS92622-Q1 monitors both $V_{(OUTx)}$ voltage and $V_{(RESx)}$ voltage of each channel and compares it with the internal reference voltage to detect a short-to-GND failure. If $V_{(OUTx)}$ or $V_{(RESx)}$ voltage falls below $V_{(SG\_th\_falling)}$ longer than the deglitch time of $t_{(SG\_deg)}$, the device asserts the short-to-GND fault and pulls low the $\overline{FAULT}$ pin. During the deglitching time period, if $V_{(OUTx)}$ and $V_{(RESx)}$ rises above $V_{(SG\_th\_rising)}$, the timer is reset.

After the TPS92622-Q1 has asserted a short-to-GND fault, the device turns off the faulty output channel and retries automatically with a small current. During retrying, the device sources a small current $I_{(Retry)}$ from SUPPLY to OUT and RES to pull up the LED loads continuously. After auto-retry detects output voltage rising above $V_{(SG\_th\_rising)}$, it clears the short-to-GND fault and resumes to normal operation. 図 6-3 illustrates the timing for LED short-circuit detection, protection, retry and recovery.

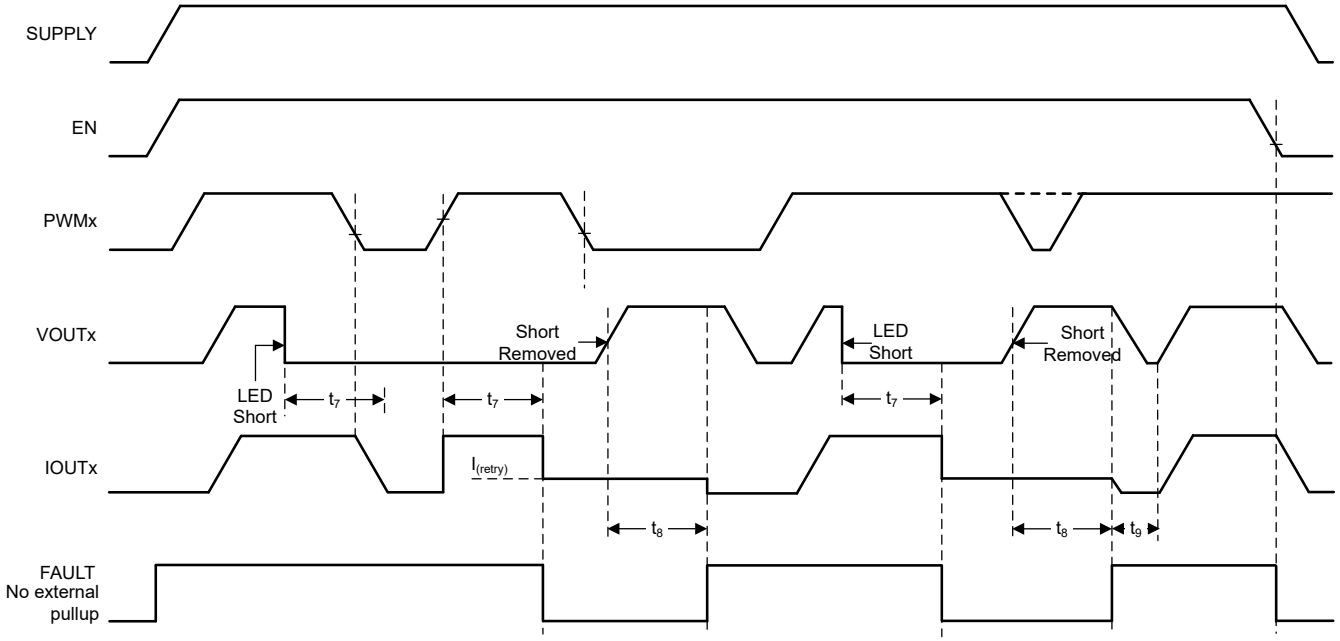


図 6-3. LED Short-to-GND Detection and Recovery Timing Diagram

The detailed information and value of each time period in 図 6-3 is described in TIMING section of the *Electrical Characteristics*.

6.3.7.2 LED Open-Circuit Detection

The TPS92622-Q1 device has LED open-circuit detection. The LED open-circuit detection monitors the output voltage when the current output is enabled. The LED open-circuit detection is only enabled when DIAGEN is HIGH. A short-to-battery fault is also detected and recognized as an LED open-circuit fault.

The TPS92622-Q1 monitors dropout-voltage differences between the IN and OUT pins for each LED channel when PWM is HIGH. The voltage difference $V_{(INx)} – V_{(OUTx)}$ is compared with the internal reference voltage $V_{(OPEN\_th\_rising)}$ to detect an LED open-circuit incident. If $V_{(OUTx)}$ rises and causes $V_{(INx)} – V_{(OUTx)}$ less than the $V_{(OPEN\_th\_rising)}$ voltage longer than the deglitch time of $t_{(OPEN\_deg)}$, the device asserts an open-circuit fault. After a LED open-circuit failure is detected, the internal constant-current sink pulls down the $\overline{FAULT}$ pin voltage. During the deglitch time period, if $V_{(OUTx)}$ falls and makes $V_{(INx)} – V_{(OUTx)}$ larger than $V_{(OPEN\_th\_falling)}$, the deglitch timer is reset.

The TPS92622-Q1 shuts down the output current regulation for the error channel after LED open-circuit fault is detected. The device sources a small current $I_{(Retry)}$ from SUPPLY to OUT and RES when DIAGEN input is logic High. After the fault condition is removed, the device resumes normal operation and releases the $\overline{FAULT}$ pin. 図 6-4 illustrates the timing for LED open-circuit detection, protection, retry and recovery.

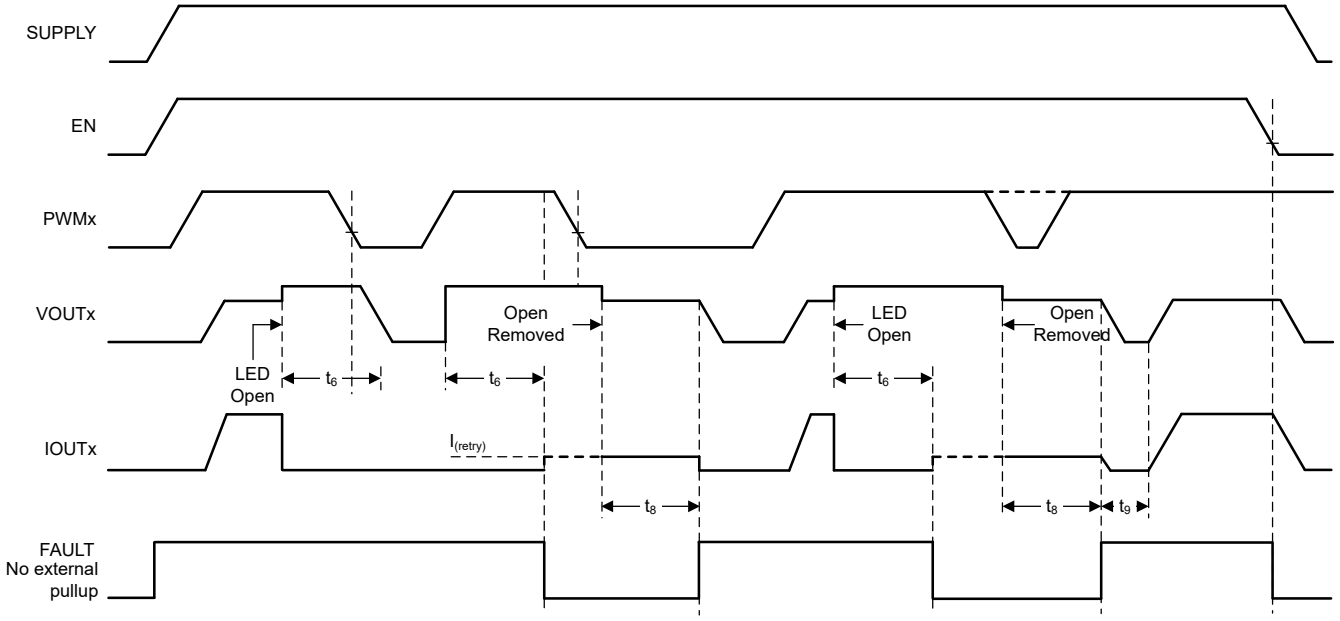


図 6-4. LED Open-Circuit Detection and Recovery Timing Diagram

The detailed information and value of each time period in 図 6-4 is described in TIMING section of the *Electrical Characteristics*.

6.3.7.3 LED Open-Circuit Detection Enable (DIAGEN)

The TPS92622-Q1 device supports the DIAGEN pin with an accurate threshold to disable the LED open-circuit. The DIAGEN pin can be used to enable or disable LED open-circuit detection based on SUPPLY pin voltage sensed by an external resistor divider as illustrated in 図 6-5. When the voltage applied on DIAGEN pin is higher than the threshold $V_{IH(DIAGEN)}$, the device enables LED open-circuit detection. When $V_{(DIAGEN)}$ is lower than the threshold $V_{IL(DIAGEN)}$, the device disables LED open-circuit detection.

Only LED open-circuit detection can be disabled by pulling down the DIAGEN pin. The LED short-to-GND detection and overtemperature protection cannot be turned off by pulling down the DIAGEN pin. Use 式 3 to calculate the SUPPLY threshold voltage.

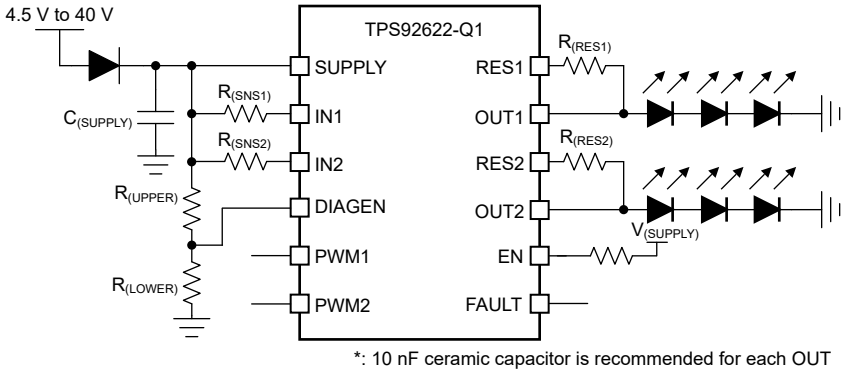


図 6-5. Application Schematic For DIAGEN

$$V_{(SUPPLY\_DIAGEN\_th\_falling)} = V_{IL(DIAGEN)} \times \left(1 + \frac{R_{(UPPER)}}{R_{(LOWER)}}\right) \quad (3)$$

where

- $V_{IL(DIAGEN)}$ = 1.045 V (minimum)

6.3.7.4 Overtemperature Protection

The TPS92622-Q1 device monitors device junction temperature. When the junction temperature reaches thermal shutdown threshold $T_{(TSD)}$, the output shuts down. After the junction temperature falls below $T_{(TSD)}$ – $T_{(TSD\_HYS)}$, the device recovers to normal operation. During overtemperature protection, the $\overline{FAULT}$ pin is pulled low.

6.3.7.5 Low Dropout Operation

When the supply voltage drops below LED string total forward voltage plus headroom voltage at required current, the TPS92622-Q1 device operates in low-dropout conditions to deliver current output as close as possible to target value. The actual current output is less than preset value due to insufficient headroom voltage for power transistor. As a result, the voltage across the sense resistor fails to reach the regulation target. The headroom voltage is the summation of $V_{(DROPOUT)}$ and $V_{(CS\_REG)}$.

If the TPS92622-Q1 is designed to operate in low-dropout condition, the open-circuit diagnostics must be disabled by pulling the DIAGEN pin voltage lower than $V_{IL(DIAGEN)}$. Otherwise, the TPS92622-Q1 detects an open-circuit fault and reports a fault on the $\overline{FAULT}$ pin. The DIAGEN pin is used to avoid false diagnostics due to low supply voltage.

6.3.8 FAULT Bus Output With One-Fails-All-Fail

During normal operation, The $\overline{FAULT}$ pin of TPS92622-Q1 is weakly pulled up by an internal pullup current source, $I_{(FAULT\_pullup)}$. If any fault scenario occurs, the $\overline{FAULT}$ pin is strongly pulled low by the internal pulldown current sink, $I_{(FAULT\_pulldown)}$ to report out the fault alarm.

Meanwhile, the TPS92622-Q1 also monitors the $\overline{FAULT}$ pin voltage internally. If the $\overline{FAULT}$ pin of the TPS92622-Q1 is pulled low by external current sink below $V_{IL(FAULT)}$, the current output is turned off even though there is no fault detected on owned outputs. The device does not resume to normal operation until the $\overline{FAULT}$ pin voltage rises above $V_{IH(FAULT)}$.

Based on this feature, the TPS92622-Q1 device is able to construct a FAULT bus by tying $\overline{FAULT}$ pins from multiple TPS92622-Q1 devices to achieve one-fails-all-fail function as 図 6-6 showing. The lower side TPS92622-Q1 (B) detects any kind of LED fault and pulls low the $\overline{FAULT}$ pin. The low voltage on $\overline{FAULT}$ pin is detected by upper side TPS92622-Q1 (A) because the $\overline{FAULT}$ pins are connected of two devices. The upper side TPS92622-Q1 (A) turns off all output current for each channel as a result. If the $\overline{FAULT}$ pins of each TPS92622-Q1 are all connected to drive the base of an external PNP transistor as illustrated in 図 6-7, the one-fails–all-fail function is disabled and only the faulty channel device is turned off.

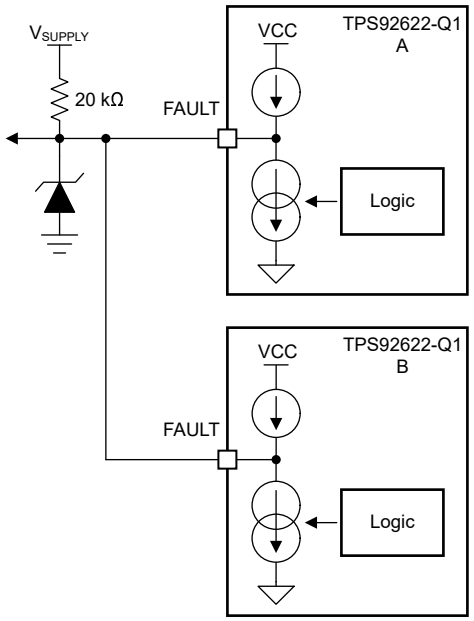


図 6-6. FAULT Bus for One-Fails-All-Fail Application

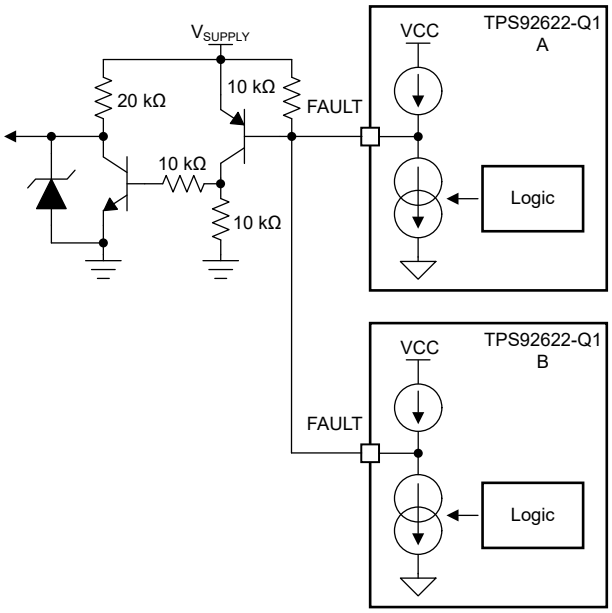


図 6-7. FAULT Bus for One-Fails-Others-On Application

6.3.9 FAULT Table

表 6-1. Fault Table With DIAGEN = HIGH (Full Function)

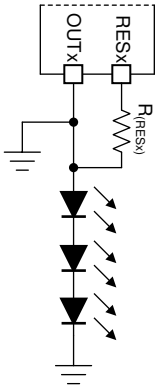
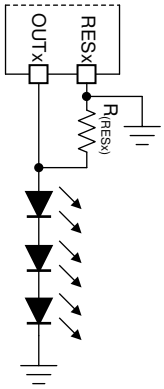
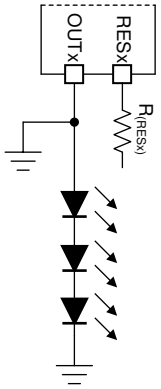
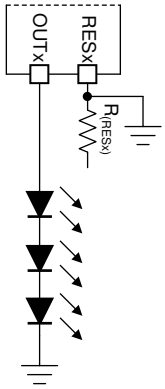
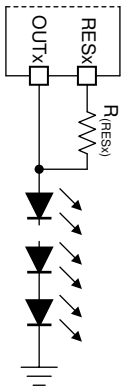
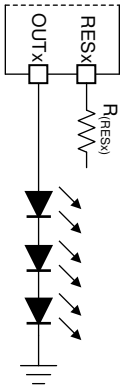
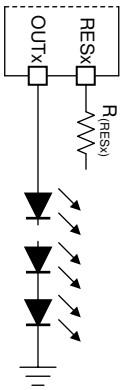
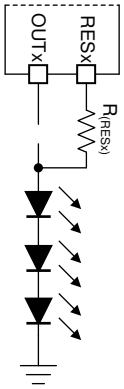
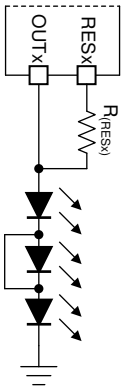
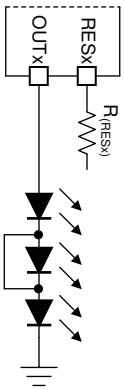
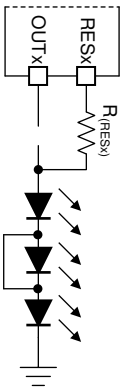
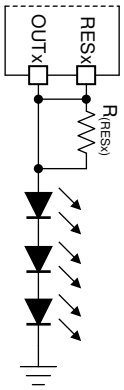
FAULT BUS STATUS	FAULT TYPE	DETECTION MECHANISM	CONTROL INPUT	DEGLITCH TIME	FAULT BUS	FAULT HANDLING ROUTINE	FAULT RECOVERY
$\overline{FAULT}$ = H	Open circuit or short-to-supply	$V_{(IN)} - V_{(OUT)} < V_{(OPEN\_th\_rising)}$	EN = H and PWMx = H	$t_{(OPEN\_deg)}$	Constant-current pulldown	Device turns failed output off and retries with constant current $I_{(retry)}$, ignoring the PWM input.	Auto recovery
	Short-to-ground	$V_{(OUT)} < V_{(SG\_th\_falling)}$ OR $V_{(RES)} < V_{(SG\_th\_falling)}$	EN = H and PWMx = H	$t_{(SG\_deg)}$	Constant-current pulldown	Device turns failed output off and retries with constant current $I_{(retry)}$, ignoring the PWM input.	Auto recovery
	Overtemperature	$T_J > T_{(TSD)}$	EN = H	$t_{(TSD\_deg)}$	Constant-current pulldown	Device turns all output channels off.	Auto recovery
$\overline{FAULT}$ = L	Fault is detected	Device turns all remained channels off and keeps retry on the failed channels. After the $\overline{Fault}$ pin is released, all channels are turned on after $t_{(FAULT\_recovery)}$ time.					
	No fault is detected	Device turns all output channels off.					

表 6-2. Fault Table With DIAGEN = LOW (Full Function)

FAULT BUS STATUS	FAULT TYPE	DETECTION MECHANISM	CURRENT OUTPUT	DEGLITCH TIME	FAULT BUS	FAULT HANDLING ROUTINE	FAULT RECOVERY
$\overline{FAULT}$ = H	Open circuit or short-to-supply	Ignored					
	Short-to-ground	$V_{(OUT)} < V_{(SG\_th\_falling)}$ OR $V_{(OUT)} < V_{(SG\_th\_falling)}$	EN = H and PWMx = H	$t_{(SG\_deg)}$	Constant-current pulldown	Device turns output off and retries with constant current $I_{(retry)}$, ignoring the PWM input.	Auto recovery
	Overtemperature	$T_J > T_{(TSD)}$	EN = H	$t_{(TSD\_deg)}$	Constant-current pulldown	Device turns all output channels off.	Auto recovery
$\overline{FAULT}$ = L	Fault is detected	Device turns all remained channels off and keeps retry on the failed channels. After the $\overline{Fault}$ pin is released, all channels are turned on after $t_{(FAULT\_recovery)}$ time.					
	No fault is detected	Device turns all output channels off.					

6.3.10 LED Fault Summary

表 6-3. LED Connection Fault Summary

Case 1	Case 2	Case 3	Case 4
			
LED Short-to-GND Fault	LED Short-to-GND Fault	LED Short-to-GND Fault	LED Short-to-GND Fault
Case 5	**Case 6**	**Case 7**	**Case 8**
			
LED Open Fault	No Fault	LED Open Fault	LED Open Fault
Case 9	**Case 10**	**Case 11**	**Case 12**
			
No Fault	No Fault	LED Open Fault	No Fault

6.3.11 IO Pins Inner Connection

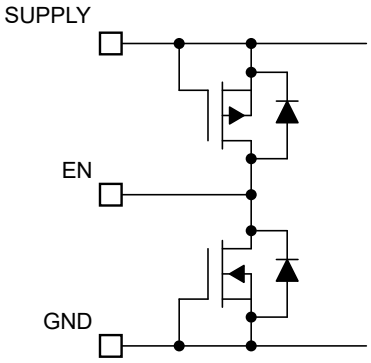


図 6-8. EN Pin

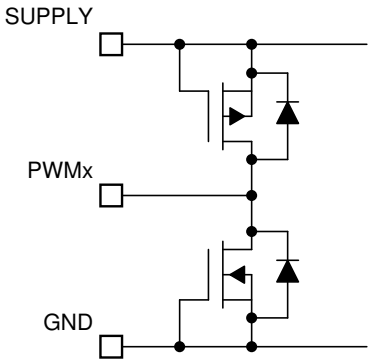


図 6-9. PWMx Pins

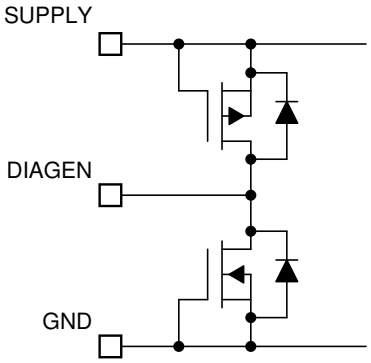


図 6-10. DIAGEN Pin

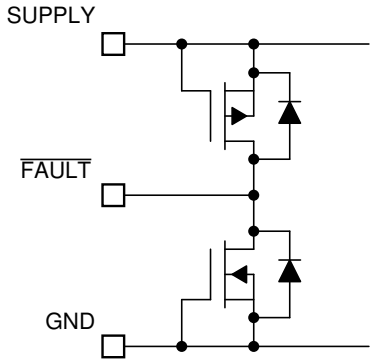


図 6-11. $\overline{\text{FAULT}}$ Pin

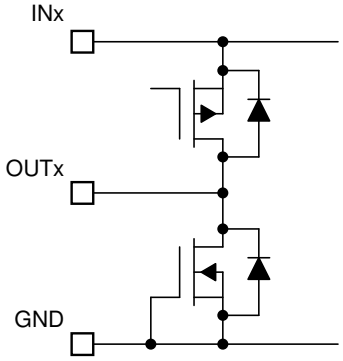


図 6-12. OUTx Pins

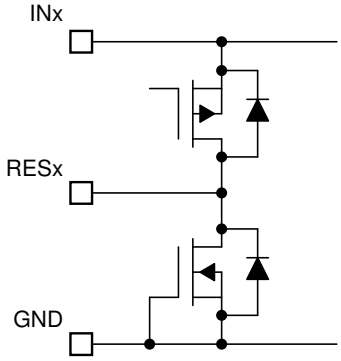


図 6-13. RESx Pins

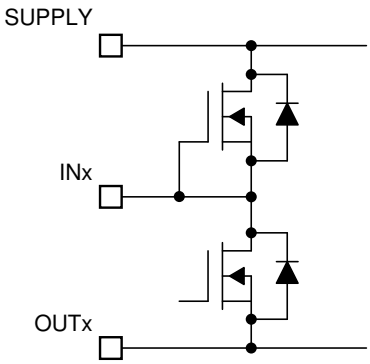


図 6-14. INx Pins

6.4 Device Functional Modes

6.4.1 Undervoltage Lockout, $V_{(SUPPLY)} < V_{(POR\_rising)}$

When the device is in undervoltage lockout status, the TPS92622-Q1 device disables all functions until the supply rises above the $V_{(POR\_rising)}$ threshold.

6.4.2 Normal Operation $V_{(SUPPLY)} \geq 4.5$ V

The device drives an LED string in normal operation. With enough voltage drop across SUPPLY and OUT, the device can drive the output in constant-current mode.

6.4.3 Low-Voltage Dropout Operation

When the device drives an LED string in low-dropout operation, if the $V_{(DROPOUT)}$ is less than the open-circuit detection threshold, the device can report a false open-circuit fault. TI recommends only enabling the open-circuit detection when the voltage across the IN and OUTx is higher than the maximum voltage of LED open rising threshold to avoid a false open-circuit detection.

6.4.4 Fault Mode

When the TPS92622-Q1 detects a fault, the device tries to pull down the $\overline{\text{FAULT}}$ pin with a constant current. If the FAULT bus is pulled down, the device switches to fault mode and consumes a fault current of $I_{(FAULT)}$.

7 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

7.1 Application Information

In automotive lighting applications, thermal performance and LED diagnostics are always design challenges for linear LED drivers.

The TPS92622-Q1 device is capable of detecting LED open-circuit and LED short-circuits. To increase current driving capability, the TPS92622-Q1 device supports using an external shunt resistor to help dissipate heat as the following section, *Thermal Sharing Resistor (OUTx and RESx)*, describes. This method provides a low-cost solution of using external resistors to minimize thermal accumulation on the device itself due to large voltage difference between input voltage and LED string forward voltage, while still keeping high accuracy of the total current output.

7.2 Typical Applications

7.2.1 BCM Controlled Rear Lamp With One-Fails-All-Fail Setup

The multiple TPS92622-Q1 devices are capable of driving different functions for automotive rear lamp including stop, turn indicator, tail, fog, reverse and center-high-mounted-stop-lamp. The one-fails-all-fail single lamp mode can be easily achieved by FAULT bus by shorting the $\overline{\text{FAULT}}$ pins.

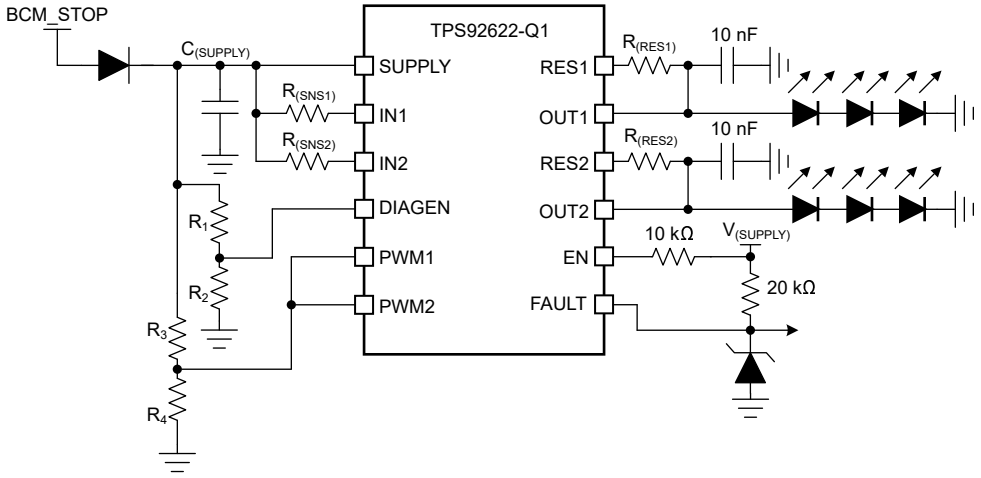


図 7-1. Typical Application Schematic

7.2.1.1 Design Requirements

Input voltage range is from 9 V to 16 V, and a total 6 strings with 3 LEDs in each string are required to achieve stop function. The LED maximum forward voltage, V_{F_MAX} is 2.5 V for each LED, while the minimum forward voltage, V_{F_MIN} is 1.9 V. The current requirement for each LED, $I_{(LED)}$ is 130 mA. The LED brightness and ON and OFF control is manipulated by body control module (BCM) directly by connecting and disconnecting the power supply to the LED load.

7.2.1.2 Detailed Design Procedure

Step 1: Use 式 4 to determine the current sensing resistor, $R_{(SNSx)}$.

$$R_{(SNSx)} = \frac{V_{(CS\_REG)}}{I_{(OUTx\_Tot)}} \quad (4)$$

where

- $V_{(CS\_REG)}$ = 150 mV (typical)
- $I_{(OUTx\_Tot)}$ = 130 mA

According to design requirements, output current for each channel is same so that the $R_{(SNS1)} = R_{(SNS2)}$ = 1.15 Ω. Two resistors in parallel can be used to achieve equivalent resistance when sense resistor is not a standard decade resistance value.

Step 2: Design the current distribution between $I_{(OUTx)}$ and $I_{(RESx)}$, and use 式 5 to calculate the current sharing resistor, $R_{(RESx)}$. The $R_{(RESx)}$ value actually decides the current distribution for $I_{(OUTx)}$ path and $I_{(RESx)}$ path. TI recommends the current sharing resistor $R_{(RESx)}$ to consume 50% of the total current at typical supply operating voltage.

$$R_{(RESx)} = \frac{V_{(SUPPLY)} - V_{(OUTx)}}{I_{(OUTx\_Tot)} \times 0.5} \quad (5)$$

where

- $V_{(SUPPLY)}$ = 12 V (typical)
- $I_{(OUTx\_Tot)}$ = 130 mA

The calculated result for $R_{(RESx)}$ resistor value including $R_{(RES1)}$, $R_{(RES2)}$ is 85.4 Ω when $V_{(OUTx)}$ is typical 3 × 2.15 V = 6.45 V.

Step 3: Design the threshold voltage of SUPPLY to enable the LED open-circuit diagnostics, and calculate voltage divider resistor value for *R1* and *R2* on DIAGEN pin.

The maximum forward voltage of LED-string is 3 × 2.5 V = 7.5 V. To avoid the open-circuit fault reported in low-dropout operation conditions, additional headroom between SUPPLY and OUTx must be considered. The TPS92622-Q1 device must disable open-circuit detection when the supply voltage is below LED-string maximum forward voltage plus $V_{(OPEN\_th\_rising)}$ and $V_{(CS\_REG)}$. Use 式 6 to calculate the voltage divider resistor, R1 and R2 value.

$$R_1 = \left(\frac{V_{(OPEN\_th\_rising)} + V_{(CS\_REG)} + V_{(OUTx)}}{V_{IL(DIAGEN)}} - 1 \right) \times R_2 \quad (6)$$

where

- $V_{(OPEN\_th\_rising)}$ = 420 mV (maximum)
- $V_{(CS\_REG)}$ = 156 mV
- $V_{IL(DIAGEN)}$ = 1.045 V (minimum)
- R_2 = 10 kΩ (recommended)

The calculated result for R1 is 67.3 kΩ when $V_{(OUTx)}$ maximum voltage is 7.5 V and $V_{(CS\_REG)}$ is 156 mV.

Step 4: Design the threshold voltage of SUPPLY to turn on and off each channel of LED, and calculate voltage divider resistor value for *R3* and *R4* on PWM input pin.

The minimum forward voltage of LED string is 3 × 1.9 V = 5.7 V. To make sure the current output on each of LED-string is normal, each LED-string must be turned off when SUPPLY voltage is lower than LED minimum

required forward voltage plus dropout voltage between INx to OUTx and $V_{(CS\_REG)}$. Use 式 7 to calculate the voltage divider resistor, R3 and R4 value.

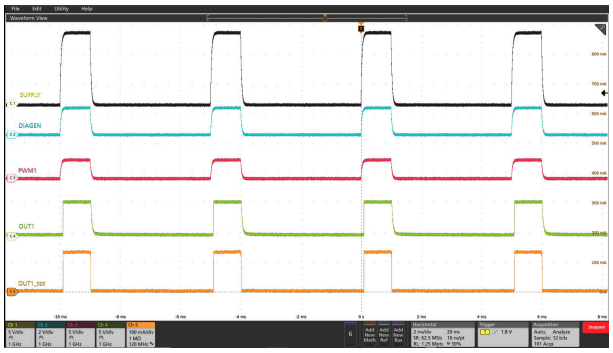
$$R_3 = \left(\frac{V_{(DROPOUT)} + V_{(CS\_REG)} + V_{(OUTx)}}{V_{IH(PWM)}} - 1 \right) \times R_4 \quad (7)$$

where

- $V_{(DROPOUT)}$ = 300 mV (typical)
- $V_{(CS\_REG)}$ = 156 mV (maximum)
- $V_{IH(PWM)}$ = 1.26 V (maximum)
- R_4 = 10 kΩ (recommended)

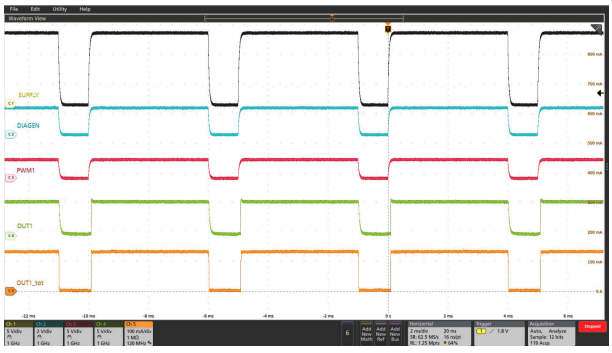
The calculated result for R3 is 38.9 kΩ when $V_{(OUTx)}$ minimum voltage is 5.7 V and $V_{(CS\_REG)}$ is 156 mV.

7.2.1.3 Application Curves



Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(DIAGEN)}$ Ch3 = $V_{(PWM1)}$
Ch4 = $V_{(OUT1)}$ Ch5 = $I_{(OUT\_Tot)}$

図 7-2. 200-Hz Supply Dimming 20% Brightness



Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(DIAGEN)}$ Ch3 = $V_{(PWM1)}$
Ch4 = $V_{(OUT1)}$ Ch5 = $I_{(OUT\_Tot)}$

図 7-3. 200-Hz Supply Dimming 80% Brightness

7.2.2 Independent PWM Controlled Rear Lamp By MCU

The TPS92622-Q1 device can drive the each current output channel independently by PWM input at PWM1, PWM2 and PWM3 pins. The PWM input signals comes from MCU to achieve sequential turn indicator feature.

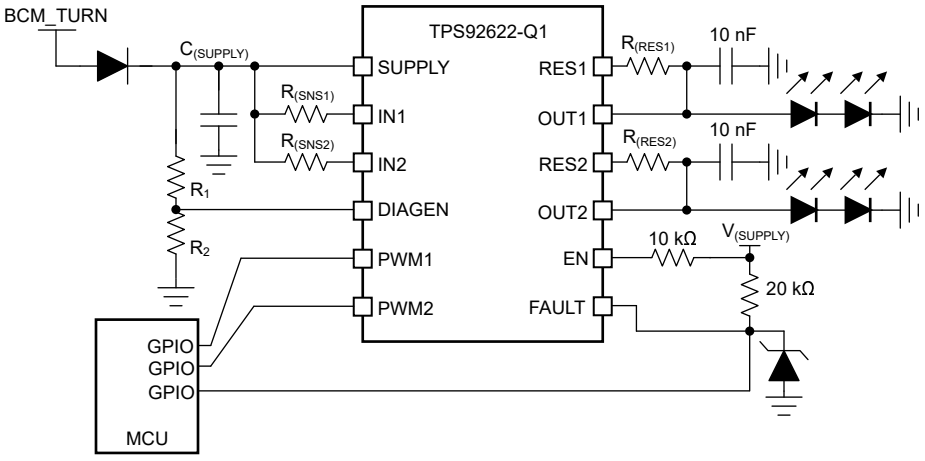


図 7-4. Typical Application Schematic

7.2.2.1 Design Requirements

Input voltage range is from 9 V to 16 V, and a total 2 strings with 2 LEDs in each string are required to achieve turn indicator function. The LED maximum forward voltage, V_{F_MAX} is 2.5 V for each LED, however the minimum forward voltage, V_{F_MIN} is 1.9 V. Each LED current is 130 mA and each output channel is independent controlled by MCU through individual GPIO.

7.2.2.2 Detailed Design Procedure

Step 1: Use 式 8 to determine the current sensing resistor, $R_{(SNSx)}$.

$$R_{(SNSx)} = \frac{V_{(CS\_REG)}}{I_{(OUTx\_Tot)}} \tag{8}$$

where

- $V_{(CS\_REG)}$ = 150 mV (typical)
- $I_{(OUTx\_Tot)}$ = 130 mA

According to design requirements, output current for each channel is same so that the calculated $R_{(SNS1)}$ = $R_{(SNS2)}$ = 1.15 Ω.

Step 2: Design the current distribution between $I_{(OUTx)}$ and $I_{(RESx)}$, and use 式 9 to calculate the current sharing resistor, $R_{(RESx)}$. The $R_{(RESx)}$ value actually decides the current distribution for $I_{(OUTx)}$ path and $I_{(RESx)}$ path, basic principle is to design the $R_{(RESx)}$ to consume appropriate 50% total power dissipation at typical supply operating voltage.

$$R_{(RESx)} = \frac{V_{(SUPPLY)} - V_{(OUTx)}}{I_{(OUTx\_Tot)} \times 0.5} \tag{9}$$

where

- $V_{(SUPPLY)}$ = 12 V (typical)
- $I_{(OUTx\_Tot)}$ = 130 mA (maximum)

The calculated result for $R_{(RESx)}$ resistor value including $R_{(RES1)}$, $R_{(RES2)}$ is 117 Ω when $V_{(OUTx)}$ is typical 2 × 2.2 V = 4.4 V.

Step 3: Design the threshold voltage of SUPPLY to enable the LED open circuit, and calculate voltage divider resistor value for *R1* and *R2* on the DIAGEN pin.

The maximum forward voltage of LED-string is 2 × 2.5 V = 5 V. To avoid the open-circuit fault reported in low-dropout operation conditions, additional headroom between SUPPLY and OUTx must be considered. The TPS92622-Q1 device must disable open-circuit detection when the supply voltage is below LED-string maximum forward voltage plus $V_{(OPEN\_th\_rising)}$ and $V_{(CS\_REG)}$. Use 式 10 to calculate the voltage divider resistor, R1 and R2 value.

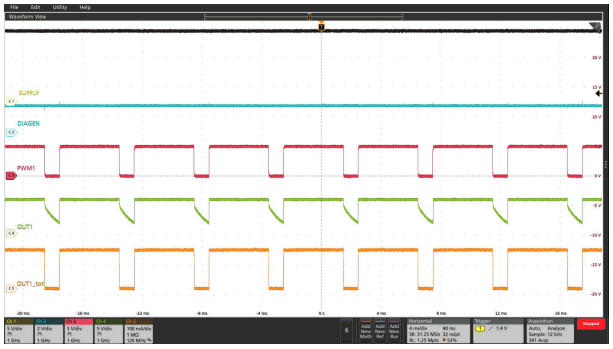
$$R_1 = \left(\frac{V_{(OPEN\_th\_rising)} + V_{(CS\_REG)} + V_{(OUTx)}}{V_{IL(DIAGEN)}} - 1 \right) \times R_2 \tag{10}$$

where

- $V_{(OPEN\_th\_rising)}$ = 420 mV (maximum)
- $V_{(CS\_REG)}$ = 156 mV (maximum)
- $V_{IL(DIAGEN)}$ = 1.045 V (minimum)
- R_2 = 10 kΩ (recommended)

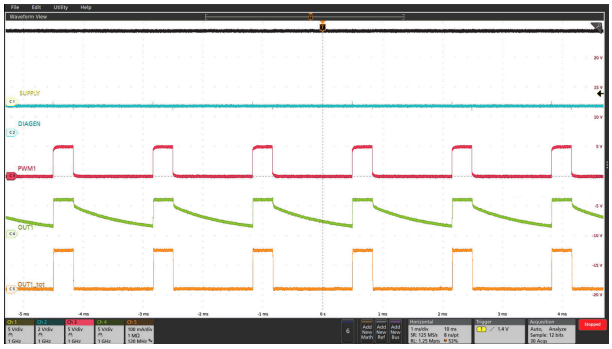
The calculated result for R1 is 43.4 kΩ when $V_{(OUTx)}$ maximum voltage is 5 V and $V_{(CS\_REG)}$ is 156 mV.

7.2.2.3 Application Curves



Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(DIAGEN)}$ Ch3 = $V_{(PWM1)}$
Ch4 = $V_{(OUT1)}$ Ch5 = $I_{(OUT\_Tot)}$

図 7-5. 200-Hz PWM Dimming at 80% Duty Cycle



Ch1 = $V_{(SUPPLY)}$ Ch2 = $V_{(DIAGEN)}$ Ch3 = $V_{(PWM1)}$
Ch4 = $V_{(OUT1)}$ Ch5 = $I_{(OUT\_Tot)}$

図 7-6. 600-Hz PWM Dimming at 20% Duty Cycle

7.3 Power Supply Recommendations

The TPS92622-Q1 is designed to operate from an automobile electrical power system within the range specified in *Power Supply*. The $V_{(SUPPLY)}$ input must be protected from reverse voltage and voltage dump condition over 40 V. The impedance of the input supply rail must be low enough that the input current transient does not cause drop below LED string required forward voltage. If the input supply is connected with long wires, additional bulk capacitance can be required in addition to normal input capacitor.

7.4 Layout

7.4.1 Layout Guidelines

Thermal dissipation is the primary consideration for TPS92622-Q1 layout.

- TI recommends large thermal dissipation area in both top and bottom layers of PCB. The copper pouring area in same layer with TPS92622-Q1-Q1 footprint must directly cover the thermal pad land of the device with wide connection as much as possible. The copper pouring in opposite PCB layer or inner layers must be connected to thermal pad directly through multiple thermal vias.
- TI recommends to place $R_{(RESx)}$ resistors away from the TPS92622-Q1 device with more than 20-mm distance, because $R_{(RESx)}$ resistors are dissipating some amount of the power as well as the TPS92622-Q1. Place two heat source components apart to reduce the thermal accumulation concentrated at small PCB area. The large copper pouring area is also required surrounding the $R_{(RESx)}$ resistors for helping thermal dissipating.

The noise immunity is the secondary consideration for TPS92622-Q1 layout.

- TI recommends to place the noise decoupling capacitors for SUPPLY pin as close as possible to the pins.
- TI recommends to place the $R_{(SNSx)}$ resistor as close as possible to the INx pins with the shortest PCB track to SUPPLY pin.

7.4.2 Layout Example

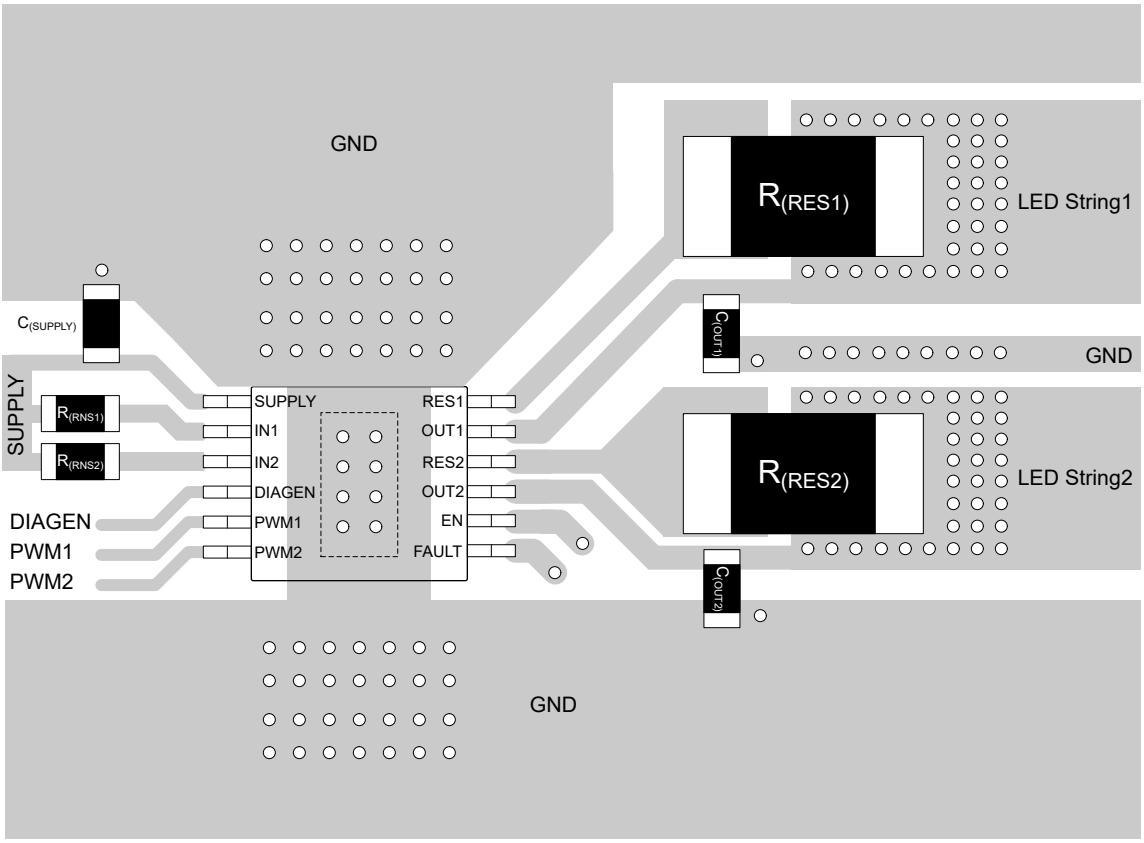


図 7-7. TPS92622-Q1 Example Layout Diagram

8 Device and Documentation Support

8.1 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、www.tij.co.jp のデバイス製品フォルダを開いてください。[通知] をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取ることができます。変更の詳細については、改訂されたドキュメントに含まれている改訂履歴をご覧ください。

8.2 サポート・リソース

テキサス・インスツルメンツ E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

リンクされているコンテンツは、各寄稿者により「現状のまま」提供されるものです。これらはテキサス・インスツルメンツの仕様を構成するものではなく、必ずしもテキサス・インスツルメンツの見解を反映したものではありません。テキサス・インスツルメンツの使用条件を参照してください。

8.3 Trademarks

PowerPAD™ and テキサス・インスツルメンツ E2E™ are trademarks of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

8.4 静電気放電に関する注意事項

この IC は、ESD によって破損する可能性があります。テキサス・インスツルメンツは、IC を取り扱う際には常に適切な注意を払うことを推奨します。正しい取り扱いおよび設置手順に従わない場合、デバイスを破損するおそれがあります。

ESD による破損は、わずかな性能低下からデバイスの完全な故障まで多岐にわたります。精密な IC の場合、パラメータがわずかに変化するだけで公表されている仕様から外れる可能性があるため、破損が発生しやすくなっています。

8.5 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

9 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision * (November 2022) to Revision A (November 2023)	Page
• HVSSOP パッケージのピン名を更新し、すべての適切な画像に対して GND ピンを EN ピンに変更	1
• HVSSOP パッケージの図を更新し、GND ピンを EN ピンに変更	1
• Updated HVSSOP package Information to include EN	3
• Removed HVSSOP package product preview note	3
• Updated Specifications to include EN pin information	5
• Updated Functional Block Diagram	12
• Updated Enable and Shutdow(EN) description	13
• Updated 図 6-1 with EN pin information	14
• Updated Application Schematic for Supply Control LED Brightness with EN pin information	14
• Updated LED Short-to-GND Detection and Recovery Timing Diagram to include EN pin information	15
• Updated LED Open-Circuit Detection and Recovery Timing Diagram to include EN pin information	16
• Updated Application Schematic For DIAGEN to include EN pin information	17
• Updated Fault Table With DIAGEN = HIGH (Full Function) to include EN logic information	20
• Updated Typical Application Schematic to include EN pin information	25
• Updated Typical Application Schematic to include EN pin information	27
• Updated TPS92622-Q1 Example Layout Diagram	30

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS92622QDGNRQ1	ACTIVE	HVSSOP	DGN	12	5000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	622Q	Samples
TPS92622QDRRRQ1	ACTIVE	WSON	DRR	12	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	92622Q	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

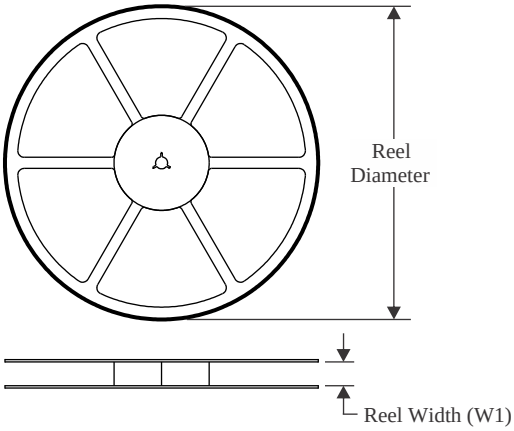
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

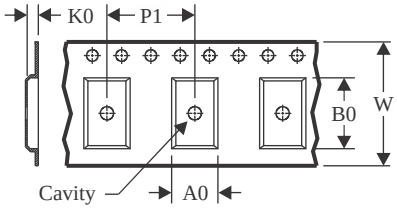
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

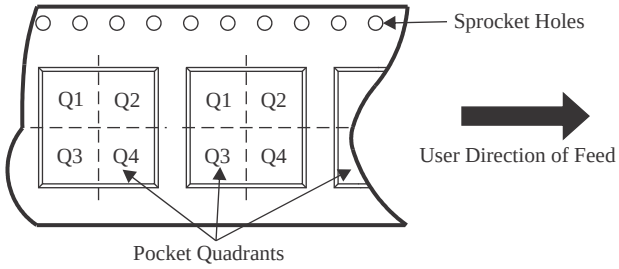


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

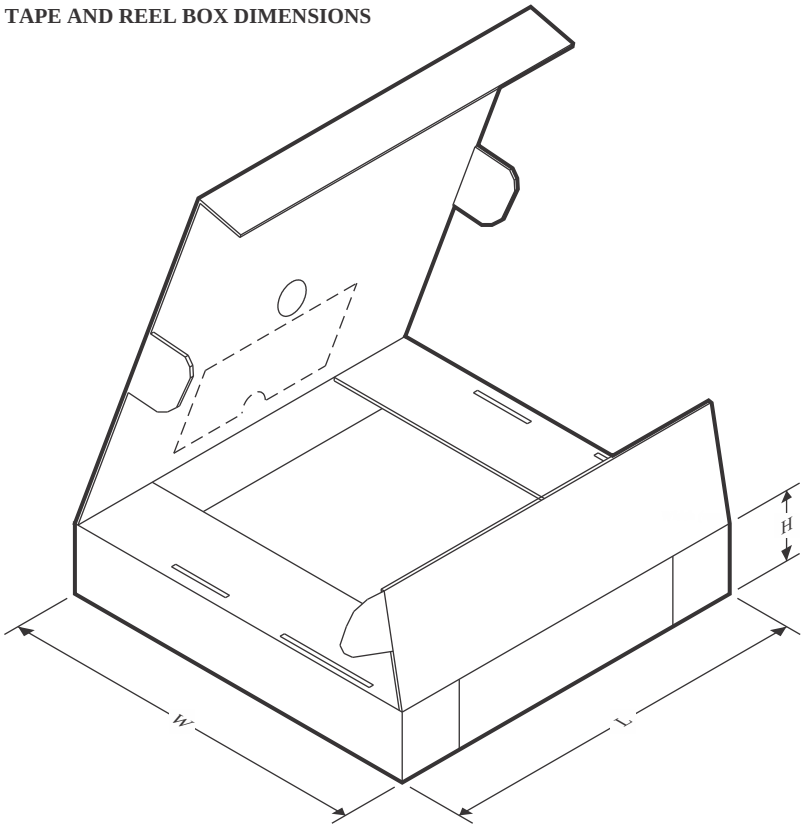
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS92622QDGNRQ1	HVSSOP	DGN	12	2500	330.0	12.4	5.2	4.3	1.45	8.0	12.0	Q1
TPS92622QDRRRQ1	WSON	DRR	12	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

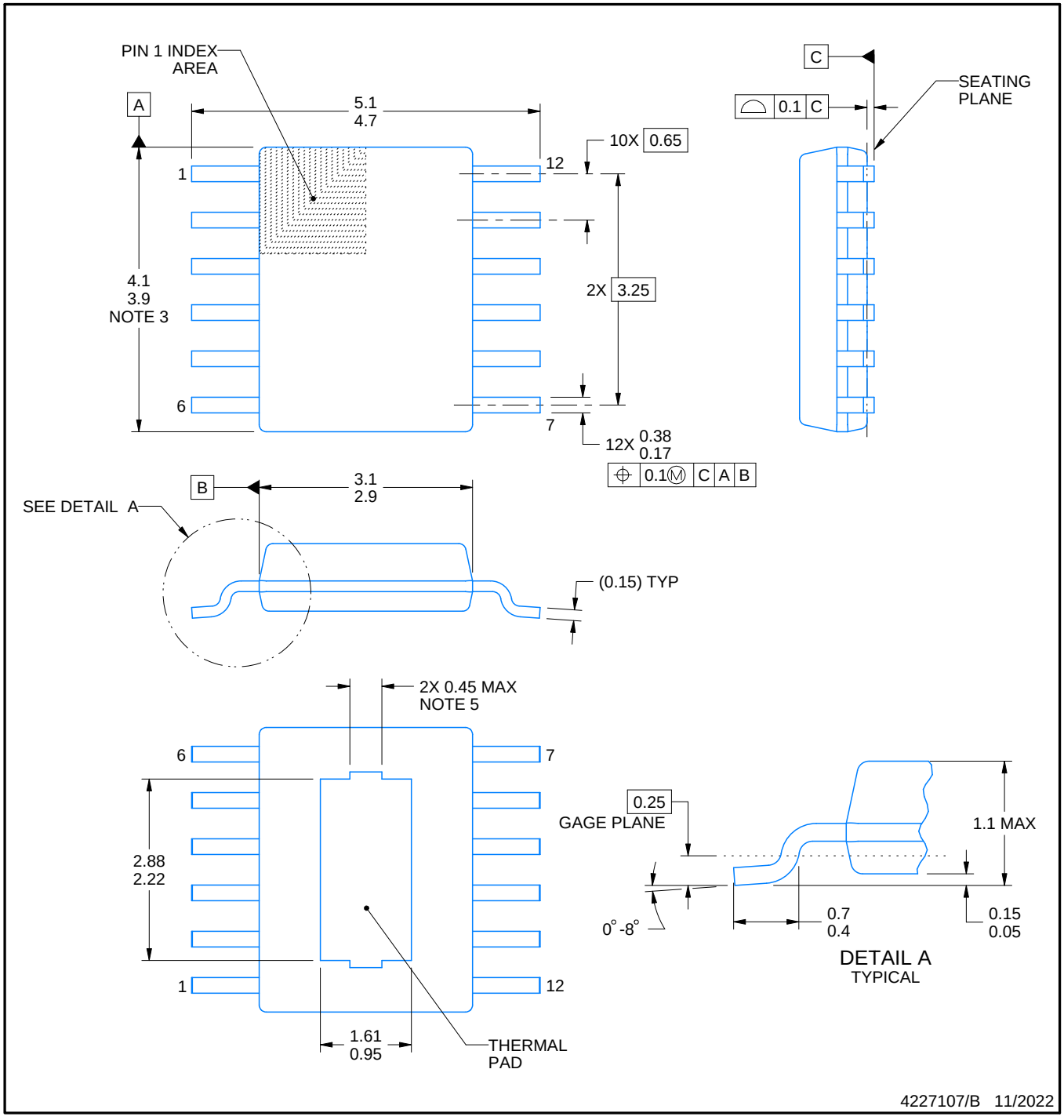
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS92622QDGNRQ1	HVSSOP	DGN	12	2500	356.0	356.0	35.0
TPS92622QDRRRQ1	WSON	DRR	12	3000	367.0	367.0	35.0

PACKAGE OUTLINE

DGN0012A

PowerPAD™ VSSOP - 1.1 mm max height

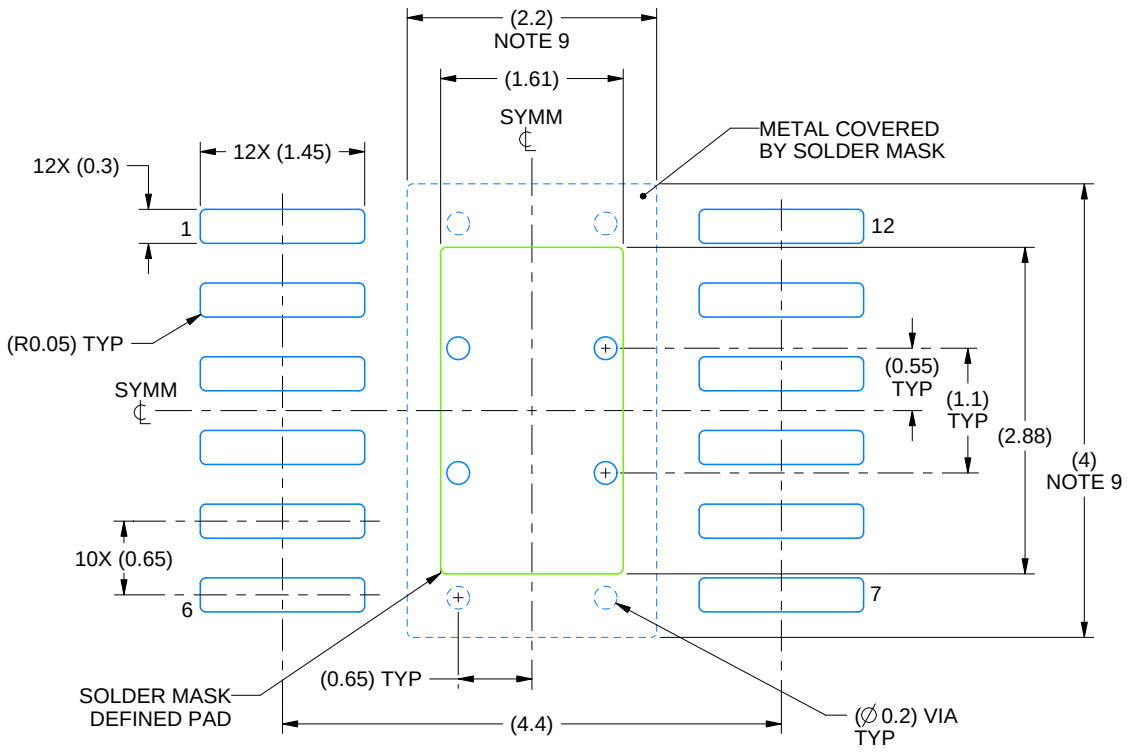
SMALL OUTLINE PACKAGE



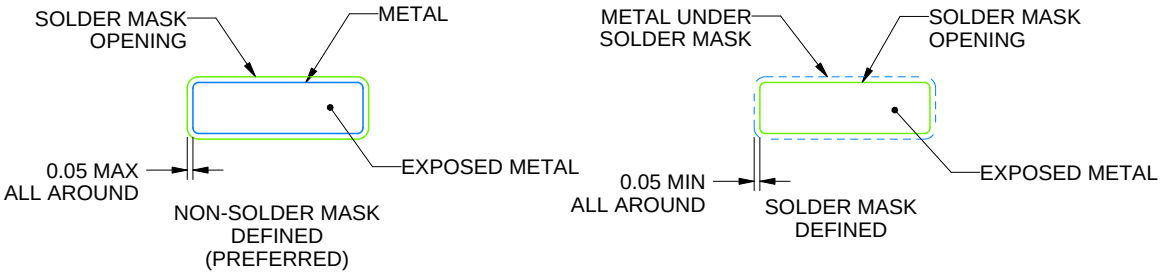
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. No JEDEC registration as of September 2020.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 15X

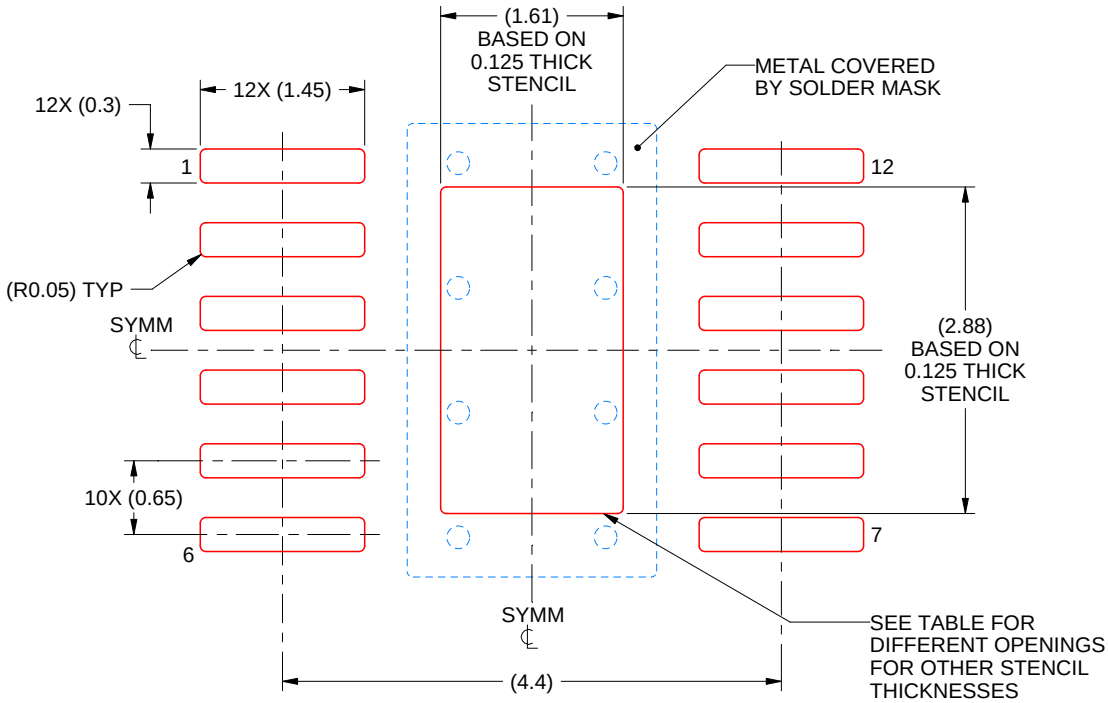


SOLDER MASK DETAILS

4227107/B 11/2022

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 15X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	1.80 X 3.22
0.125	1.61 X 2.88 (SHOWN)
0.15	1.47 X 2.63
0.175	1.36 X 2.43

4227107/B 11/2022

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

GENERIC PACKAGE VIEW

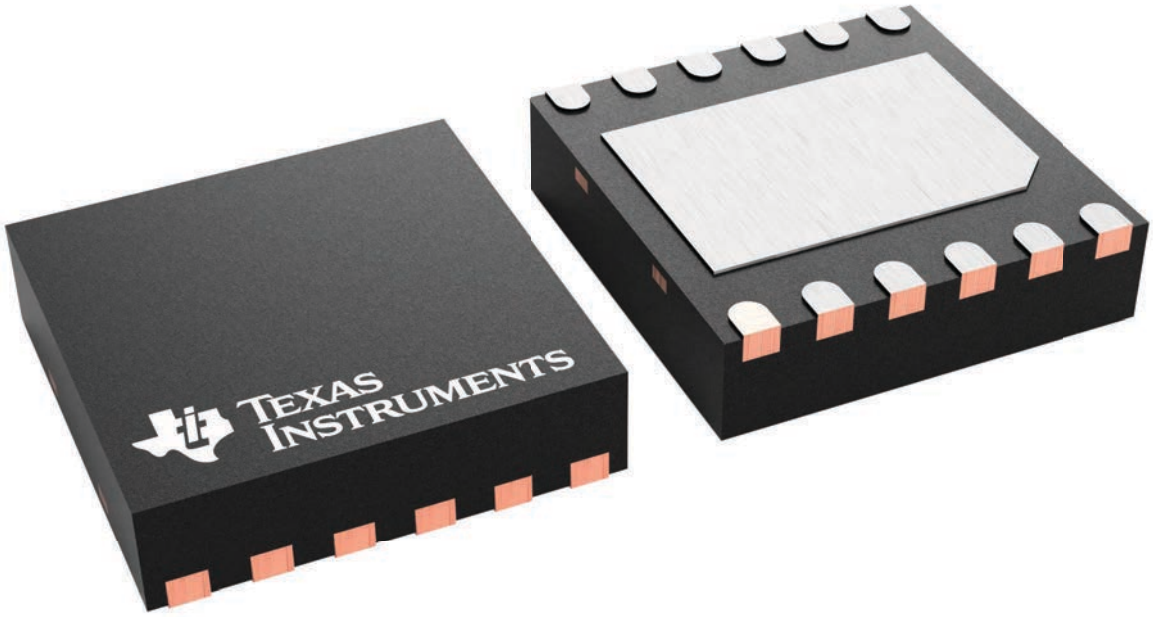
DRR 12

WSON - 0.8 mm max height

3 x 3, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



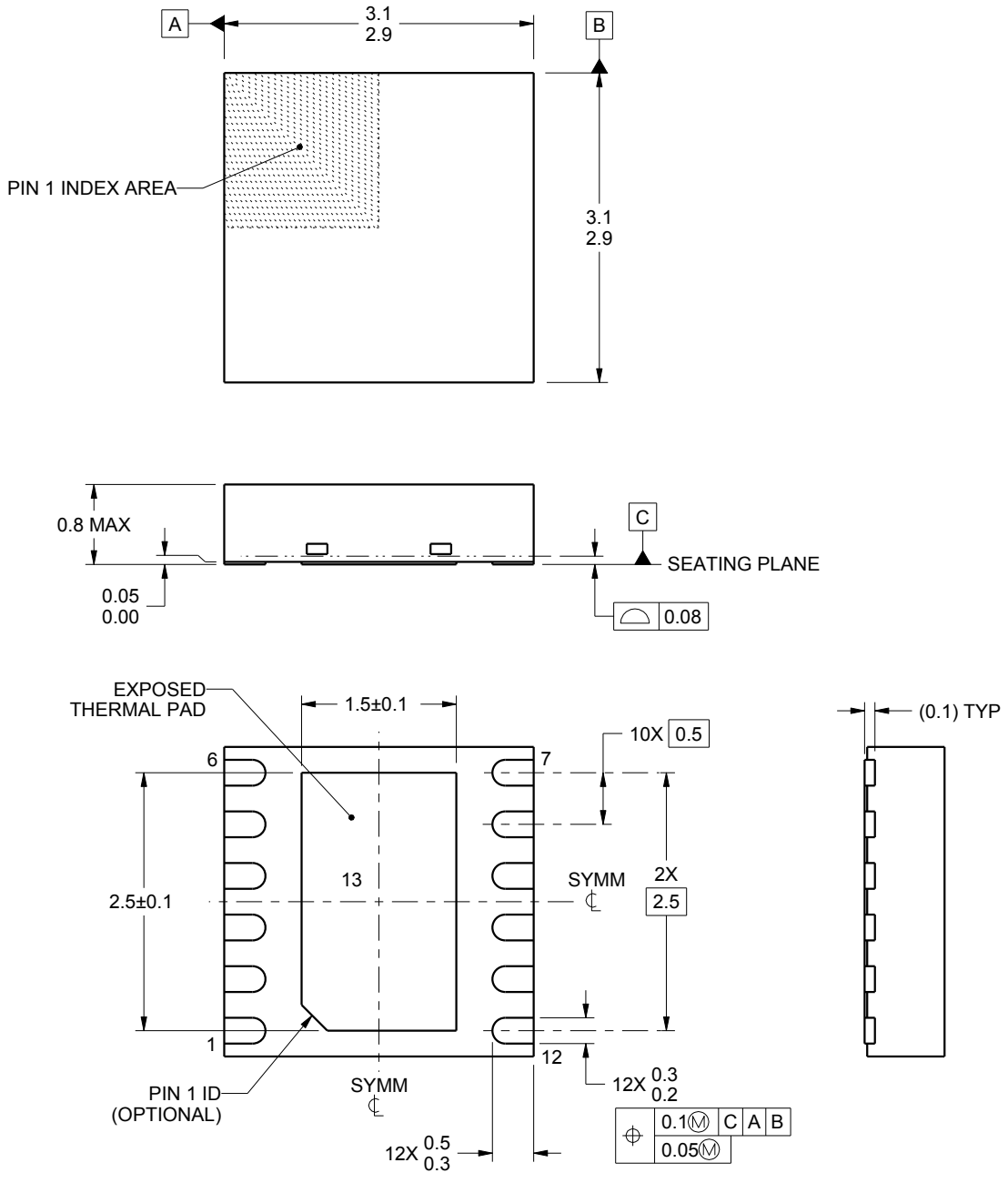
4223490/B

PACKAGE OUTLINE

DRR0012C

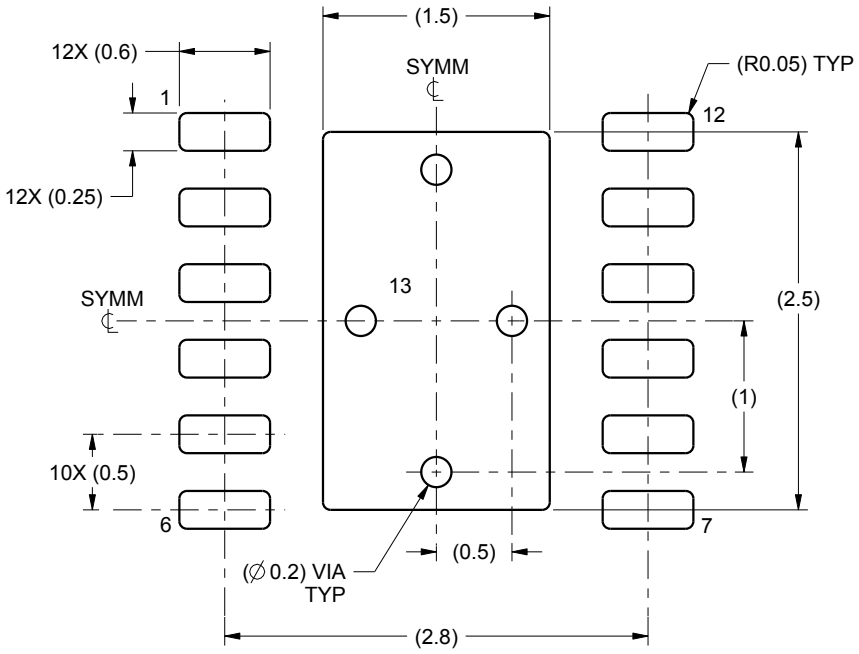
WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD

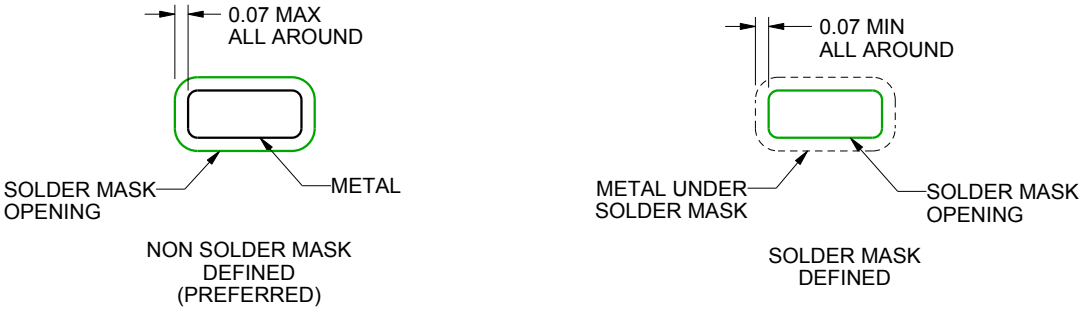


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X



SOLDER MASK DETAILS

4222932/A 05/2016

NOTES: (continued)

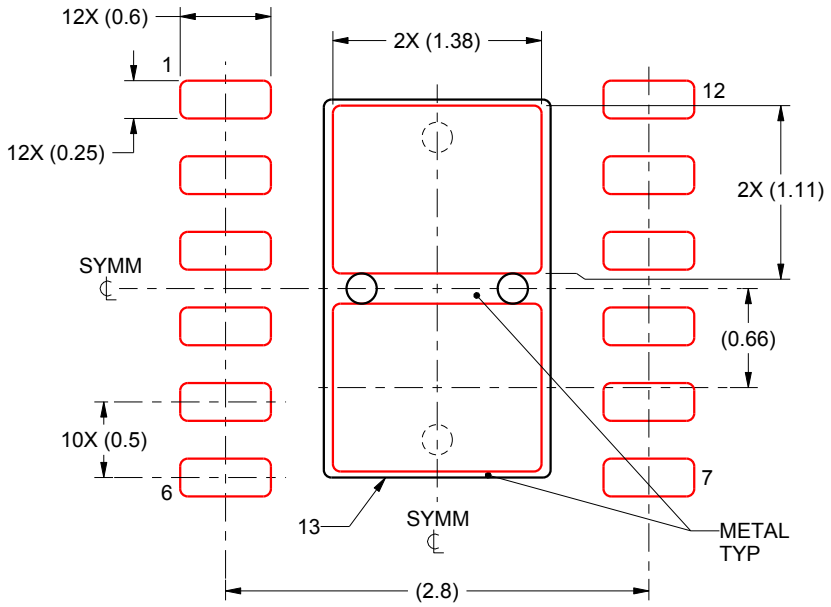
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

DRR0012C

WSON - 0.8 mm max height

PLASTIC SMALL OUTLINE - NO LEAD



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 13
81.7% PRINTED SOLDER COVERAGE BY AREA
SCALE:20X

4222932/A 05/2016

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

重要なお知らせと免責事項

TI は、技術データと信頼性データ (データシートを含みます)、設計リソース (リファレンス· デザインを含みます)、アプリケーションや設計に関する各種アドバイス、Web ツール、安全性情報、その他のリソースを、欠陥が存在する可能性のある「現状のまま」提供しており、商品性および特定目的に対する適合性の黙示保証、第三者の知的財産権の非侵害保証を含むいかなる保証も、明示的または黙示的にかかわらず拒否します。

これらのリソースは、TI 製品を使用する設計の経験を積んだ開発者への提供を意図したものです。(1) お客様のアプリケーションに適した TI 製品の選定、(2) お客様のアプリケーションの設計、検証、試験、(3) お客様のアプリケーションに該当する各種規格や、その他のあらゆる安全性、セキュリティ、規制、または他の要件への確実な適合に関する責任を、お客様のみが単独で負うものとします。

上記の各種リソースは、予告なく変更される可能性があります。これらのリソースは、リソースで説明されている TI 製品を使用するアプリケーションの開発の目的でのみ、TI はその使用をお客様に許諾します。これらのリソースに関して、他の目的で複製することや掲載することは禁止されています。TI や第三者の知的財産権のライセンスが付与されている訳ではありません。お客様は、これらのリソースを自身で使用した結果発生するあらゆる申し立て、損害、費用、損失、責任について、TI およびその代理人を完全に補償するものとし、TI は一切の責任を拒否します。

TI の製品は、TI の販売条件、または ti.com やかかる TI 製品の関連資料などのいずれかを通じて提供する適用可能な条項の下で提供されています。TI がこれらのリソースを提供することは、適用される TI の保証または他の保証の放棄の拡大や変更を意味するものではありません。

お客様がいかなる追加条項または代替条項を提案した場合でも、TI はそれらに異議を唱え、拒否します。

郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265