

TRSF3221E 3V~5.5V、シングル・チャンネル RS-232 1Mbit/s ライン・ドライバ / レシーバ、 ±15kV IEC ESD 保護機能搭載

1 特長

- RS-232 ピンの ESD 保護
 - ±15kV 人体モデル (HBM)
 - ±8kV IEC 61000-4-2 接触放電
 - ±15kV IEC 61000-4-2 エアギャップ放電
- 3V~5.5V の V_{CC} 電源で動作
- 最大 1Mbit/s で動作
 - 低速のピン互換デバイス (250kbit/s) – TRSF3221E
- ニア・チップスケール・パッケージ、16 ピン VQFN (RGT, TSSOP パッケージより 82% 小型) で供給
- 小さいスタンバイ電流: 1 μ A (標準値)
- 外付けコンデンサ: 4 × 0.1 μ F
- 3.3V 電源で 5V ロジック入力を受容
- 自動パワー・ダウン機能により、ドライバを自動的にディスエーブルすることで電力を節約

2 アプリケーション

- 産業用 PC
- 有線ネットワーク
- データ・センターおよびエンタープライズ・コンピューティング
- バッテリー駆動システム
- PDA
- ノートブック PC
- ノート PC
- パームトップ PC
- ハンドヘルド機器

3 概要

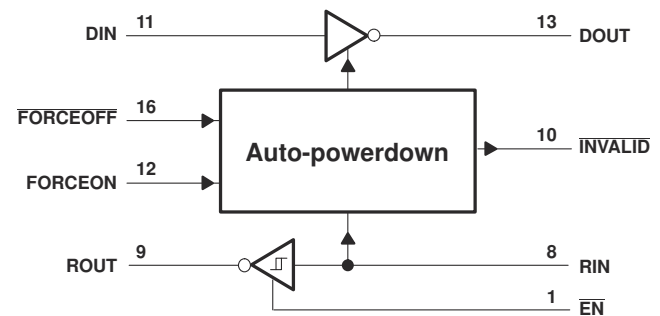
TRSF3221E デバイスは 1 つのライン・ドライバ、1 つのライン・レシーバ、1 つのデュアル・チャージ・ポンプ回路で構成されており、±15kV のピン間 (シリアル・ポート接続ピン、GND を含む) IEC ESD 保護機能を備えています。TRSF3221E は、非同期通信コントローラとシリアルポート・コネクタの間の電氣的インターフェイスとして機能します。チャージ・ポンプと 4 つの小さな外付けコンデンサにより、3V ~ 5.5V の単一電源で動作できます。TRSF3221E は最大 1Mbit/s のデータ信号速度、24V/ μ s ~ 150V/ μ s のドライバ出力スlewレートで動作します。

シリアル・ポートが使われていない際のパワー・マネージメントを柔軟に制御できます。FORCEON が LOW かつ FORCEOFF が HIGH の場合、自動パワー・ダウン機能が動作します。この動作モード中、TRSF3221E がレシーバ入力で有効な RS-232 信号を検出しない場合、ドライバ出力はディスエーブルになります。FORCEOFF を LOW に設定しかつイネーブル ($\overline{EN}$) 入力を HIGH に設定すると、ドライバとレシーバはどちらもシャットダウンされ、消費電流は 1 μ A に減少します。シリアル・ポートを切り離れた場合、またはペリフェラル・ドライバをオフにした場合、自動パワー・ダウン状態になります。FORCEON と FORCEOFF を HIGH にすると、自動パワー・ダウンを無効にできます。自動パワーダウンが有効な場合、レシーバの入力に有効な信号が印加されると、デバイスは自動的にアクティブになります。INVALID 出力は、レシーバの入力に RS-232 信号が存在するかどうかをユーザーに通知します。INVALID は、レシーバの入力電圧が 2.7V を上回っている場合、-2.7V を下回っている場合、-0.3V と 0.3V の間にあった期間が 30 μ s 未満である場合のいずれかの場合、HIGH (有効データ) になります。INVALID は、レシーバの入力電圧が 30 μ s を超える期間 -0.3V と 0.3V の間にある場合、LOW (無効データ) になります。レシーバの入力レベルについては、図 7-5 を参照してください。

製品情報

部品番号	パッケージ ⁽¹⁾	本体サイズ (公称)
TRSF3221E	DB (SSOP)	6.20mm × 5.30mm
	PW (TSSOP)	5.00mm × 4.40mm
	RGT (VQFN)	3.00mm × 3.00mm

- (1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



論理図 (正論理)



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4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (May 2021) to Revision B (July 2021)	Page
• 「アプリケーション」の一覧を変更.....	1
• Changed the table note for the <i>ESD Ratings - IEC Specifications</i> table to make it also applicable to PW package.....	4
• Changed the thermal information for PW package.....	5
Changes from Revision * (August 2007) to Revision A (May 2021)	Page
• 「製品情報」表、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加.....	1

5 Pin Configuration and Functions

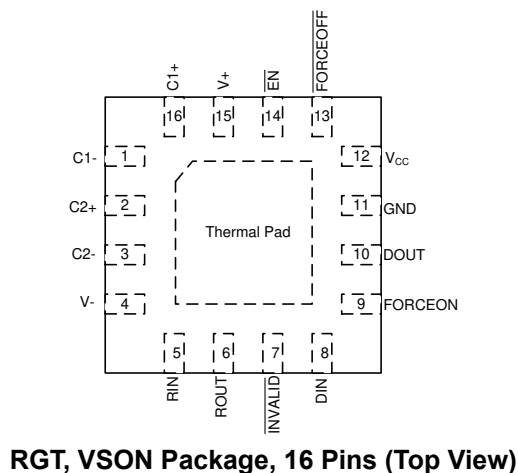
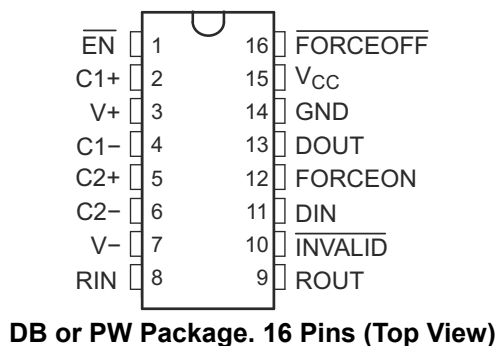


表 5-1. Pin Functions

NAME	PIN		I/O ⁽¹⁾	DESCRIPTION
	DB or PW	RGT		
EN	1	14	--	
C1+	2	16	-	Positive lead of C1 capacitor
V+	3	15	O	Positive charge pump output for storage capacitor only
C1-	4	1	-	Negative lead of C1 capacitor
C2+	5	2	-	Positive lead of C2 capacitor
C2-	6	3	-	Negative lead of C2 capacitor
V-	7	4	O	Negative charge pump output for storage capacitor only
RIN	8	5	I	RS232 line data input (from remote RS232 system)
ROUT	9	6	O	Logic data output (to UART)
INVALID	10	7		
DIN	11	8	I	Logic data input (from UART)
FORCEON	12	9		
DOUT	13	10	O	RS232 line data output (to remote RS232 system)
GRD	14	11	-	Ground
V _{CC}	15	12	-	Supply Voltage, Connect to external 3-V to 5.5-V power supply
FORCEOFF	16	13		
Thermal Pad	-	Yes	-	Exposed thermal pad. Can be connected to GND or left floating.

(1) Signal Types: I = Input, O = Output, I/O = Input or Output.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) See ⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage range ⁽²⁾		−0.3	6	V
V+	Positive output supply voltage range ⁽²⁾		−0.3	7	V
V−	Negative output supply voltage range ⁽²⁾		0.3	−7	V
V+ − V−	Supply voltage difference ⁽²⁾			13	V
V _I	Input voltage range	Driver (FORCEOFF, FORCEON, EN)	−0.3	6	V
		Receiver	−25	25	
V _O	Output voltage range	Driver	−13.2	13.2	V
		Receiver (INVALID)	−0.3	V _{CC} + 0.3	
T _J	Operating virtual junction temperature			150	°C
T _{stg}	Storage temperature range		−65	150	°C

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 ESD Ratings, IEC Specifications

PIN NAME	TEST CONDITIONS	TYP	UNIT
RIN, DOUT	HBM	±15	kV
	IEC 61000-4-2 Contact Discharge ⁽¹⁾	±8	
	IEC 61000-4-2 Air-Gap Discharge ⁽¹⁾	±15	

- (1) For the RGT and PW package only, a minimum of 1-μF capacitor is required between VCC and GND to meet the specified IEC-ESD level.

6.4 Recommended Operating Conditions

See [9-1](#) and ⁽¹⁾

				MIN	NOM	MAX	UNIT
Supply voltage			$V_{CC} = 3.3\text{ V}$	3	3.3	3.6	V
			$V_{CC} = 5\text{ V}$	4.5	5	5.5	
V_{IH}	Driver and control high-level input voltage	DIN, FORCEOFF, FORCEON, EN	$V_{CC} = 3.3\text{ V}$	2			V
			$V_{CC} = 5\text{ V}$	2.4			
V_{IL}	Driver and control low-level input voltage	DIN, FORCEOFF, FORCEON, EN				0.8	V
V_I	Driver and control input voltage	DIN, FORCEOFF, FORCEON		0		5.5	V
V_I	Receiver input voltage			−25		25	V
T_A	Operating free-air temperature	TRSF3221EI	−40		85		°C
		TRSF3221EC	0		70		

(1) Test conditions are C1–C4 = 0.1 μF at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; C1 = 0.047 μF , C2–C4 = 0.33 μF at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

6.5 Thermal Resistance Characteristics

THERMAL METRIC ⁽¹⁾		TRSF3221E			UNIT
		DB (SSOP)	PW (TSSOP)	RGT (VQFN)	
		16 Pins	16 Pins	16 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	82	110.9	58.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.7	41.7	55.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.4	57.2	23.8	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	11.0	4.2	1.7	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	43.8	56.6	23.7	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	9	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

6.6 Electrical Characteristics

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

(see [9-1](#))

PARAMETER		TEST CONDITIONS ⁽¹⁾	MIN	TYP ⁽²⁾	MAX	UNIT
I_I	Input leakage current	FORCEOFF, FORCEON, EN		± 0.01	± 1	μA
I_{CC}	Supply current ($T_A = 25^\circ\text{C}$)	Auto-powerdown disabled	No load, FORCEOFF and FORCEON at V_{CC}	0.3	1	μA
		Powered off	No load, FORCEOFF at GND	1	10	
		Auto-powerdown enabled	No load, FORCEOFF at V_{CC} , FORCEON at GND, All RIN are open or grounded	1	10	

(1) Test conditions are C1–C4 = 0.1 μF at $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$; C1 = 0.047 μF , C2–C4 = 0.33 μF at $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$.

(2) All typical values are at $V_{CC} = 3.3\text{ V}$ or $V_{CC} = 5\text{ V}$, and $T_A = 25^\circ\text{C}$.

6.7 Electrical Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

(see [9-1](#))

PARAMETER	TEST CONDITIONS ⁽¹⁾	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH} High-level output voltage	DOUT at R _L = 3 kΩ to GND, DIN = GND	5	5.4		V
V _{OL} Low-level output voltage	DOUT at R _L = 3 kΩ to GND, DIN = V _{CC}	–5	–5.4		V
I _{IH} High-level input current	V _I = V _{CC}		±0.01	±1	μA
I _{IL} Low-level input current	V _I at GND		±0.01	±1	μA
I _{OS} Short-circuit output current ⁽³⁾	V _{CC} = 3.6 V, V _O = 0 V		±35	±60	mA
	V _{CC} = 5.5 V, V _O = 0 V		±35	±90	
r _o Output resistance	V _{CC} , V ₊ , and V _– = 0 V, V _O = ±2 V	300	10M		Ω
I _{off} Output leakage current	FORCEOFF = GND	V _O = ±12 V, V _{CC} = 3 V to 3.6 V		±25	μA
		V _O = ±10 V, V _{CC} = 4.5 V to 5.5 V		±25	

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Short-circuit durations must be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output can be shorted at a time.

6.8 Switching Characteristics, Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)

(see [9-1](#))

PARAMETER	TEST CONDITIONS ⁽¹⁾	MIN	TYP ⁽²⁾	MAX	UNIT
Maximum data rate (see 7-1)	R _L = 3 kΩ	C _L = 1000 pF	250		kbit/s
		C _L = 250 pF, V _{CC} = 3 V to 4.5 V	1000		
		C _L = 1000 pF, V _{CC} = 4.5 V to 5.5 V	1000		
t _{sk(p)} Pulse skew ⁽³⁾	C _L = 250 pF	R _L = 3 kΩ 7-2 RGT Package	25		ns
	C _L = 150 pF to 2500 pF	R _L = 3 kΩ to 7 kΩ, See 7-2 DB or PW package	100		
SR(tr) Slew rate, transition region (see 7-1)	V _{CC} = 3.3 V, R _L = 3 kΩ to 7 kΩ, C _L = 150 pF to 1000 pF	18		150	V/μs

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

6.9 Electrical Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see [9-1](#))

PARAMETER	TEST CONDITIONS ⁽¹⁾	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH} High-level output voltage	I _{OH} = –1 mA	V _{CC} – 0.6 V	V _{CC} – 0.1 V		V
V _{OL} Low-level output voltage	I _{OL} = 1.6 mA			0.4	V
V _{IT+} Positive-going input threshold voltage	V _{CC} = 3.3 V		1.6	2.4	V
	V _{CC} = 5 V		1.9	2.4	
V _{IT–} Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.1		V
	V _{CC} = 5 V	0.8	1.4		
V _{hys} Input hysteresis (V _{IT+} – V _{IT–})			0.5		V
I _{off} Output leakage current	FORCEOFF = 0 V		±0.05	±10	μA
r _i Input resistance	V _i = ±3 V to ±25 V	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.10 Switching Characteristics, Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see [9-1](#))

PARAMETER		TEST CONDITIONS ⁽¹⁾		TYP ⁽²⁾	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 150 pF, See 7-3	RGT package	100	ns
			DB or PW package	150	
t _{PHL}	Propagation delay time, high- to low-level output	C _L = 150 pF, See 7-3	RGT package	125	ns
			DB or PW package	150	
t _{en}	Output enable time	C _L = 150 pF, R _L = 3 kΩ, See 7-4		200	ns
t _{dis}	Output disable time	C _L = 150 pF, R _L = 3 kΩ, See 7-4		200	ns
t _{sk(p)}	Pulse skew ⁽³⁾	See 7-3	RGT package	25	ns
			DB or PW package	50	

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} – t_{PHL}| of each channel of the same device.

6.11 Electrical Characteristics, Auto-Powerdown

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see [7-5](#))

PARAMETER	TEST CONDITIONS	MIN	MAX	UNIT
$V_{T+}(\text{valid})$	Receiver input threshold for INVALID high-level output voltage FORCEON = GND, FORCEOFF = V_{CC}		2.7	V
$V_{T-}(\text{valid})$	Receiver input threshold for INVALID high-level output voltage FORCEON = GND, FORCEOFF = V_{CC}	-2.7		V
$V_{T}(\text{invalid})$	Receiver input threshold for INVALID low-level output voltage FORCEON = GND, FORCEOFF = V_{CC}	-0.3	0.3	V
V_{OH}	INVALID high-level output voltage $I_{OH} = -1 \text{ mA}$, FORCEON = GND, FORCEOFF = V_{CC}	$V_{CC} - 0.6$		V
V_{OL}	INVALID low-level output voltage $I_{OL} = 1.6 \text{ mA}$, FORCEON = GND, FORCEOFF = V_{CC}		0.4	V

6.12 Switching Characteristics, Auto-Powerdown

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)
(see [7-5](#))

PARAMETER	TYP ⁽¹⁾	UNIT
t_{valid}	1	μs
t_{invalid}	30	μs
t_{en}	100	μs

(1) All typical values are at $V_{CC} = 3.3 \text{ V}$ or $V_{CC} = 5 \text{ V}$, and $T_A = 25^\circ\text{C}$.

6.13 Typical Characteristics

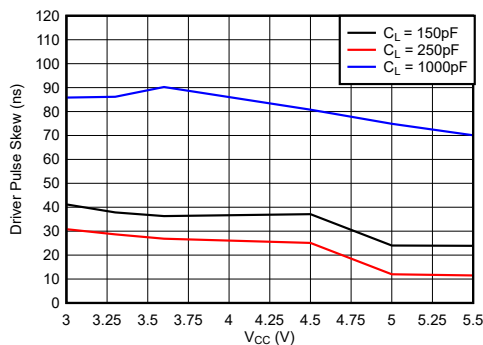


Figure 6-1. Driver Pulse Skew vs Load Capacitance and Supply Voltage at $T_A = 25^\circ\text{C}$ (RGT Package)

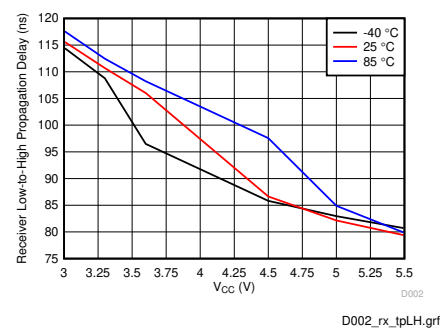


Figure 6-2. Receiver Path Low-to-High Propagation Delay vs T_A and Supply Voltage (RGT Package)

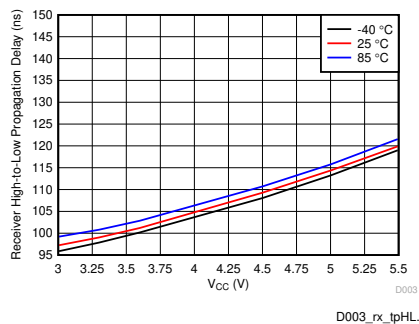


Figure 6-3. Receiver Path High-to-Low Propagation Delay vs T_A and Supply Voltage (RGT Package)

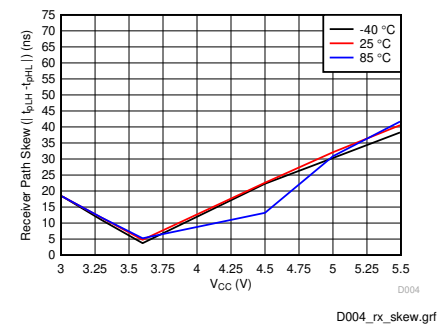
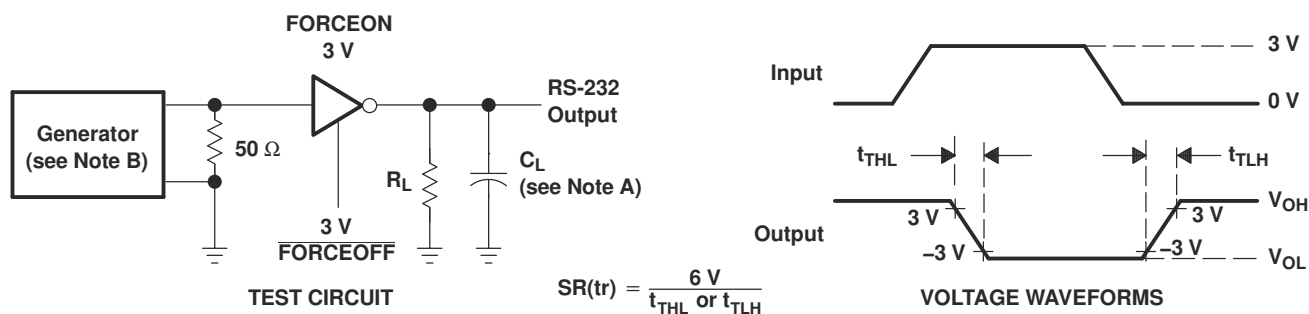


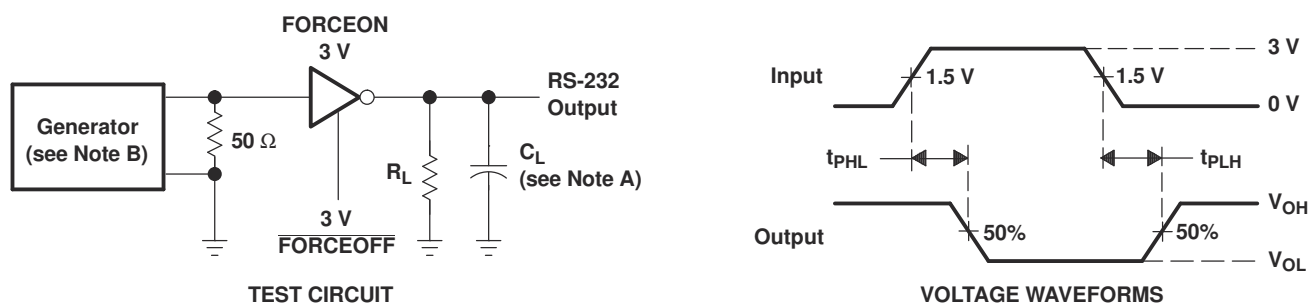
Figure 6-4. Receiver Pulse Skew ($t_{\text{pLH}} - t_{\text{pLH}}$) vs T_A and Supply Voltage (RGT Package)

7 Parameter Measurement Information



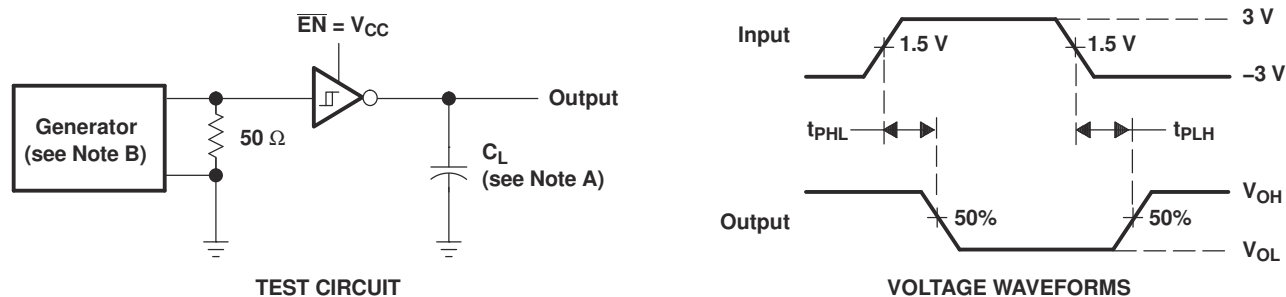
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

7-1. Driver Slew Rate



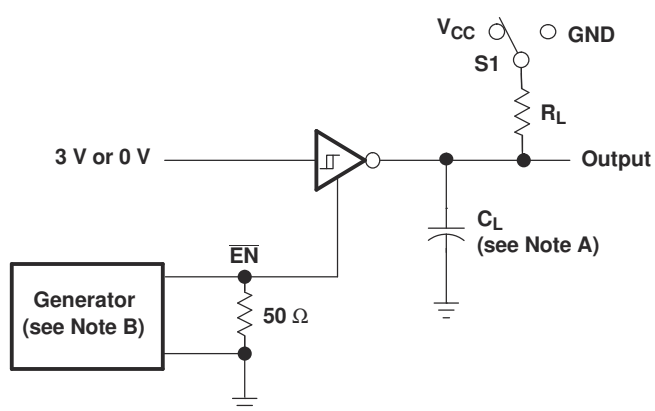
NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: PRR = 250 kbit/s, $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

7-2. Driver Pulse Skew

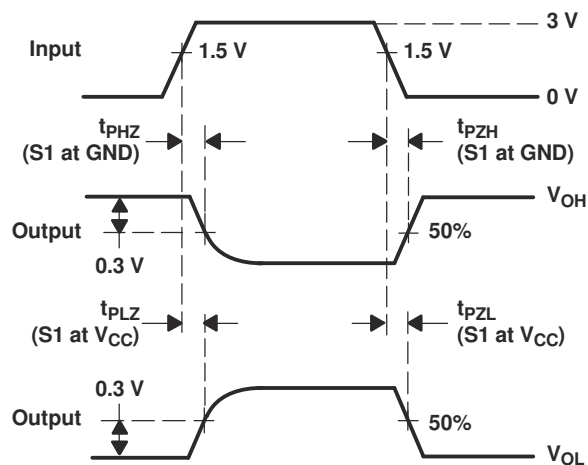


NOTES: A. C_L includes probe and jig capacitance.
B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.

7-3. Receiver Propagation Delay Times



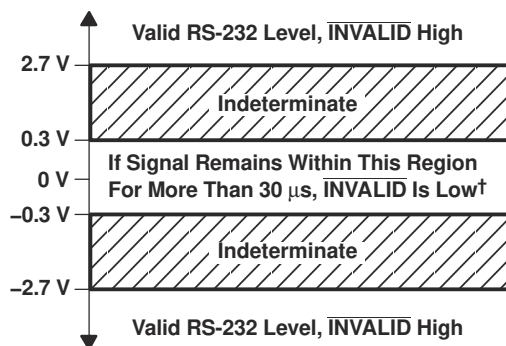
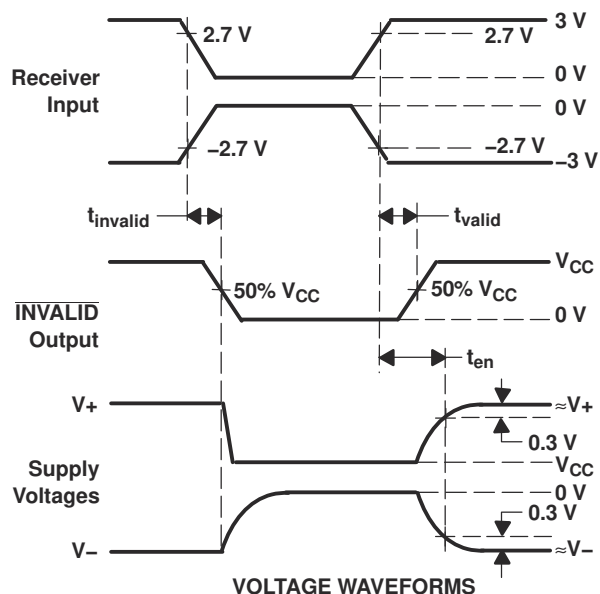
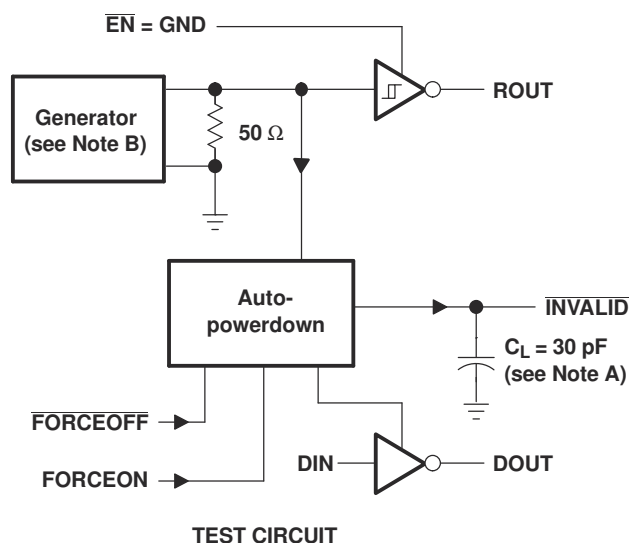
TEST CIRCUIT



VOLTAGE WAVEFORMS

- NOTES:
- A. C_L includes probe and jig capacitance.
 - B. The pulse generator has the following characteristics: $Z_O = 50\ \Omega$, 50% duty cycle, $t_r \leq 10\text{ ns}$, $t_f \leq 10\text{ ns}$.
 - C. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - D. t_{PZL} and t_{PZH} are the same as t_{en} .

7-4. Receiver Enable and Disable Times



† Auto-powerdown disables drivers and reduces supply current to 1 μA .

NOTES: A. C_L includes probe and jig capacitance.

B. The pulse generator has the following characteristics: PRR = 5 kbit/s, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

7-5. $\overline{\text{INVALID}}$ Propagation Delay Times and Driver Enabling Time

8 Detailed Description

8.1 Overview

The TRSF3221E consists of one line driver, one line receiver, and a dual charge-pump circuit with ± 15 -kV IEC ESD protection pin to pin (serial-port connection pins, including GND). The TRSF3221E provides the electrical interface between an asynchronous communication controller and the serial-port connector. The charge pump and four small external capacitors allow operation from a single 3-V to 5.5-V supply. The TRSF3221E operates at data signaling rates up to 1 Mbit/s and a driver output slew rate of 24 V/ μ s to 150 V/ μ s.

Flexible control options for power management are available when the serial port is inactive. The auto-powerdown feature functions when FORCEON is low and FORCEOFF is high. During this mode of operation, if the TRSF3221E does not sense a valid RS-232 signal on the receiver input, the driver output is disabled. If FORCEOFF is set low and the enable ($\overline{\text{EN}}$) input is high, both the driver and receiver are shut off, and the supply current is reduced to 1 μ A. Disconnecting the serial port or turning off the peripheral drivers causes the auto-powerdown condition to occur. Auto-powerdown can be disabled when FORCEON and FORCEOFF are high. With auto-powerdown enabled, the device is activated automatically when a valid signal is applied to the receiver input. The INVALID output notifies the user if an RS-232 signal is present at the receiver input. INVALID is high (valid data) if the receiver input voltage is greater than 2.7 V or less than -2.7 V, or has been between -0.3 V and 0.3 V for less than 30 μ s. INVALID is low (invalid data) if the receiver input voltage is between -0.3 V and 0.3 V for more than 30 μ s.

Outputs are protected against shorts to ground.

8.2 Functional Block Diagram

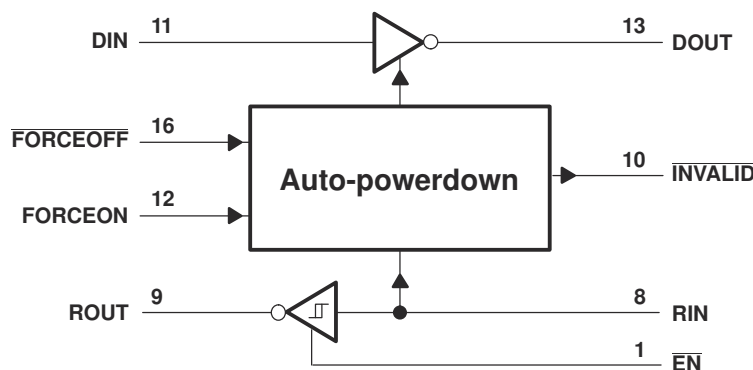


FIG 8-1. Logic Diagram (Positive Logic)

8.3 Feature Description

The power block increases, inverts, and regulates voltage at V+ and V– pins using a charge pump that requires four external capacitors. Auto-power-down feature for driver is controlled by FORCEON and FORCEOFF inputs. Receiver is controlled by $\overline{\text{EN}}$ input. When MAX3221E is unpowered, it can be safely connected to an active remote RS-232 device.

The driver interfaces the standard logic level to RS232 voltage levels. The DIN input must be valid high or low.

The receiver interfaces RS-232 levels to standard logic levels. An open input results in a high output on ROUT. RIN input includes an internal standard RS-232 load. A logic high input on the $\overline{\text{EN}}$ pin shuts down the receiver output.

8.4 Device Functional Modes

Functional Tables, Each Driver

INPUTS ⁽¹⁾				OUTPUT DOUT	DRIVER STATUS
DIN	FORCEON	FORCEOFF	VALID RIN RS-232 LEVEL		
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with auto-powerdown disabled
H	H	H	X	L	
L	L	H	Yes	H	Normal operation with auto-powerdown enabled
H	L	H	Yes	L	
L	L	H	No	Z	Powered off by auto-powerdown feature
H	L	H	No	Z	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance

Each Receiver

INPUTS ⁽¹⁾			OUTPUT ROUT
RIN	EN	VALID RIN RS-232 LEVEL	
L	L	X	H
H	L	X	L
X	H	X	Z
Open	L	No	H

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = disconnected input or connected driver off

9 Application and Implementation

Note

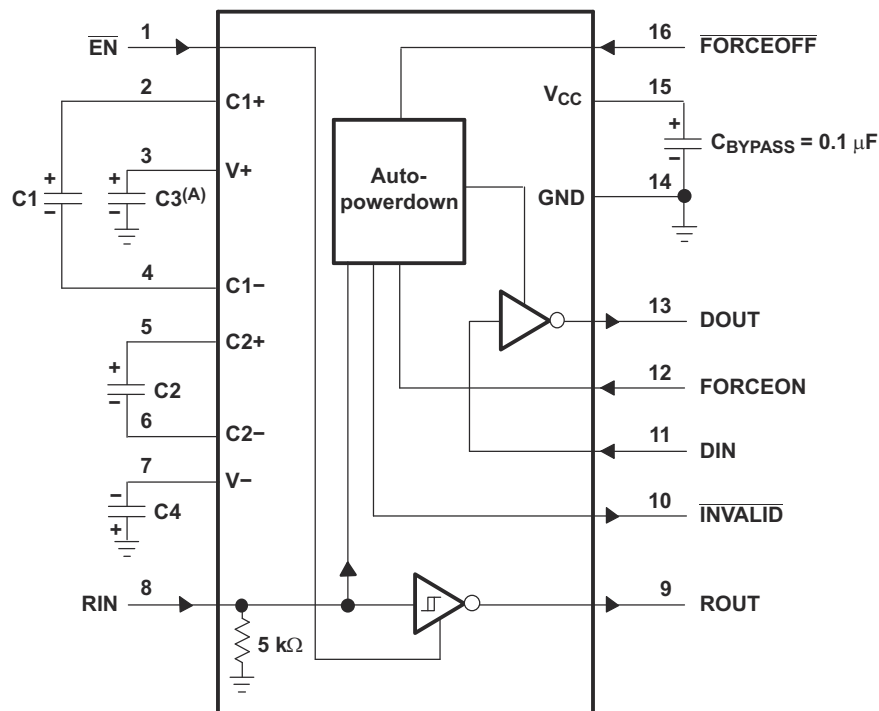
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

9.1 Application Information

The TRSF3221E line driver and receiver is a specialized device for 3-V to 5.5-V RS-232 communication applications. This application is a generic implementation of this device with all required external components. For proper operation, add capacitors as shown in 表 9-1.

9.1.1 Typical Application

ROUT and DIN connect to UART or general purpose logic lines. FORCEON and FORCEOFF may be connected to general purpose logic lines or tied to ground or VCC. INVALID may be connected to a general purpose logic line or left unconnected. RIN and DOUT lines connect to a RS-232 connector or cable. DIN, FORCEON, and FORCEOFF inputs must not be left unconnected.



- A. C3 can be connected to VCC or GND.
- B. Resistor values shown are nominal.
- C. Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they must be connected as shown.

图 9-1. Typical Operating Circuit and Capacitor Values

表 9-1. VCC vs Capacitor Values

VCC	C1	C2, C3, C4
3.3 V ± 0.3 V	0.1 μF	0.1 μF
5 V ± 0.5 V	0.047 μF	0.33 μF
3 V to 5.5 V	0.1 μF	0.47 μF

9.1.1.1 Design Requirements

- Recommended VCC is 3.3 V or 5 V – 3 V to 5.5 V is also possible
- Maximum recommended bit rate is 1 Mbps
- Use capacitors as shown in 図 9-1 and 表 9-1

9.1.1.2 Detailed Design Procedure

For proper operation:

- DIN, $\overline{\text{FORCEOFF}}$ and FORCEON inputs must be connected to valid low or high logic levels
- Select capacitor values based on VCC level for best performance

ROUT and DIN connect to UART or general purpose logic lines. FORCEON and $\overline{\text{FORCEOFF}}$ may be connected general purpose logic lines or tied to ground or VCC. $\overline{\text{INVALID}}$ may be connected to a general purpose logic line or left unconnected. RIN and DOUT lines connect to a RS232 connector or cable. DIN, FORCEON, and $\overline{\text{FORCEOFF}}$ inputs must not be left unconnected.

9.1.2 Application Performance Plot

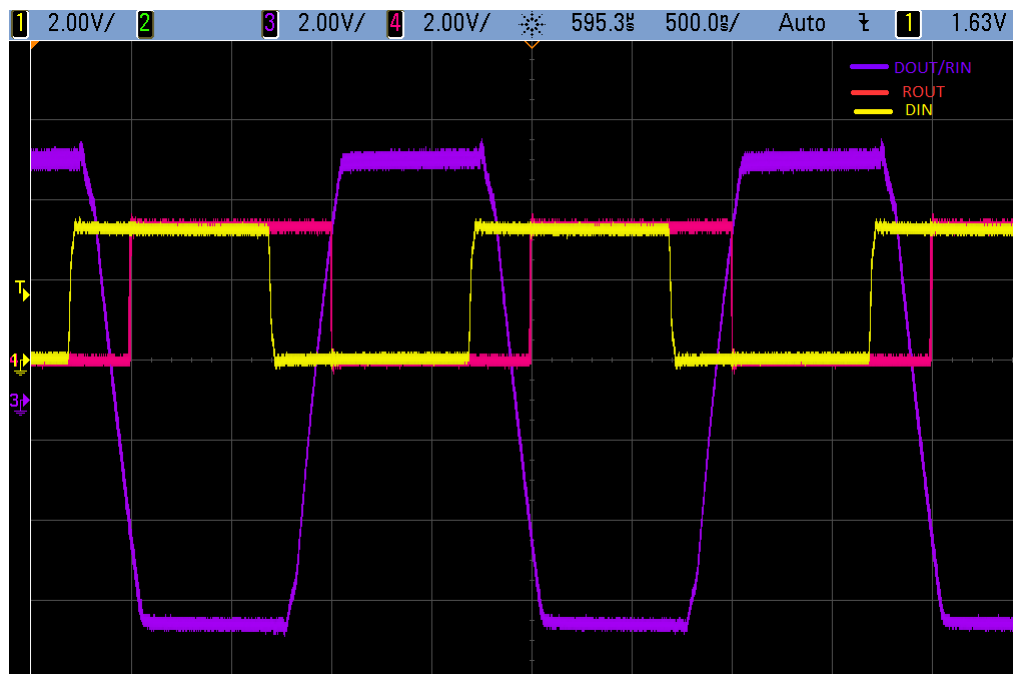


図 9-2. 1 Mbps Driver to Receiver Loopback Timing Waveform, VCC = 3.3 V

10 Power Supply Recommendations

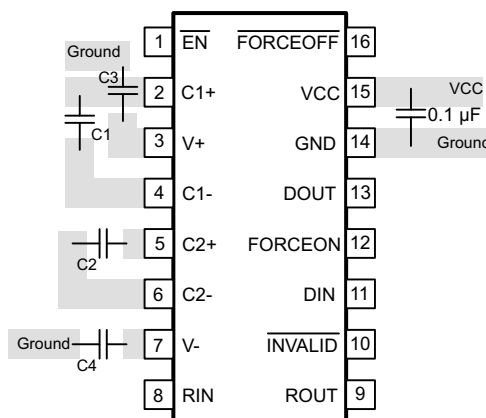
VCC must be between 3 V and 5.5 V. Charge pump capacitors must be chosen using [VCC vs Capacitor Values](#).

11 Layout

11.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes, which have the fastest rise and fall times.

11.2 Layout Example



✎ 11-1. Layout Diagram

12 Device and Documentation Support

12.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on [ti.com](https://www.ti.com). Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

12.2 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

リンクされているコンテンツは、該当する貢献者により、現状のまま提供されるものです。これらは TI の仕様を構成するものではなく、必ずしも TI の見解を反映したものではありません。TI の[使用条件](#)を参照してください。

12.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

12.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

12.5 Glossary

[TI Glossary](#) This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRSF3221ECDBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	RT21EC	Samples
TRSF3221ECPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	RT21EC	Samples
TRSF3221EIDBR	ACTIVE	SSOP	DB	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT21EI	Samples
TRSF3221EIPWR	ACTIVE	TSSOP	PW	16	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	RT21EI	Samples
TRSF3221EIRGTR	ACTIVE	VQFN	RGT	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	F3221	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

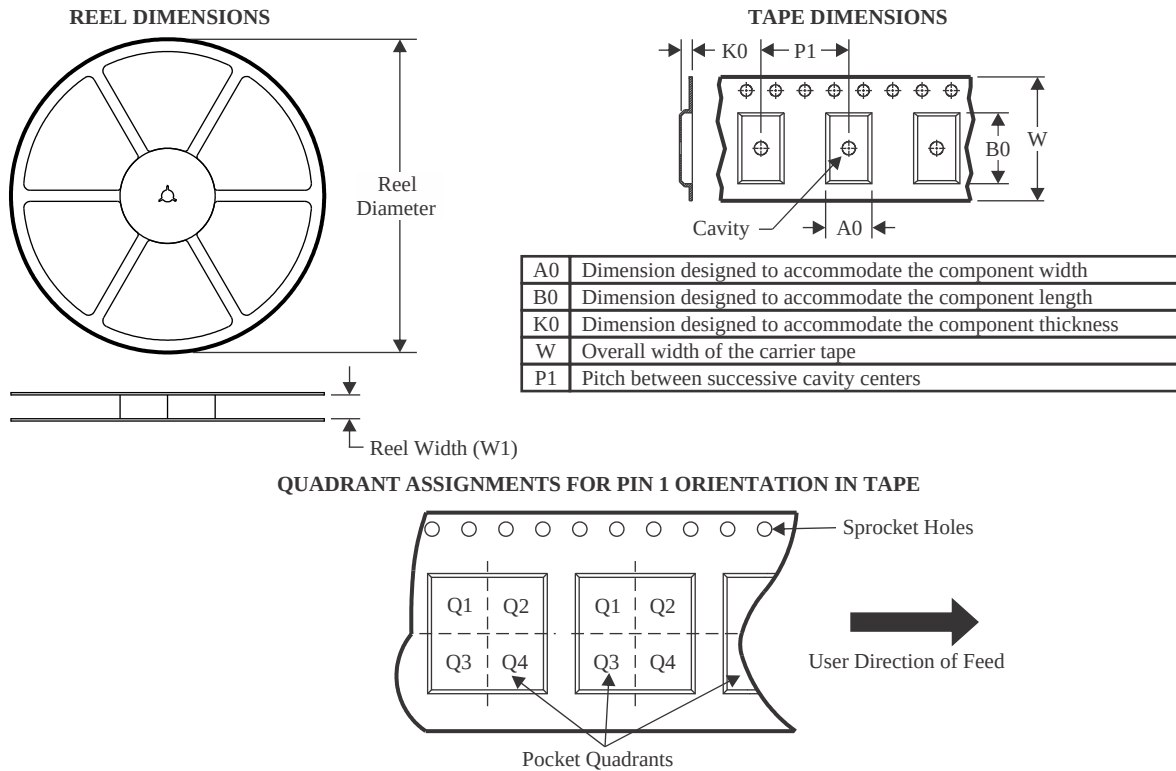
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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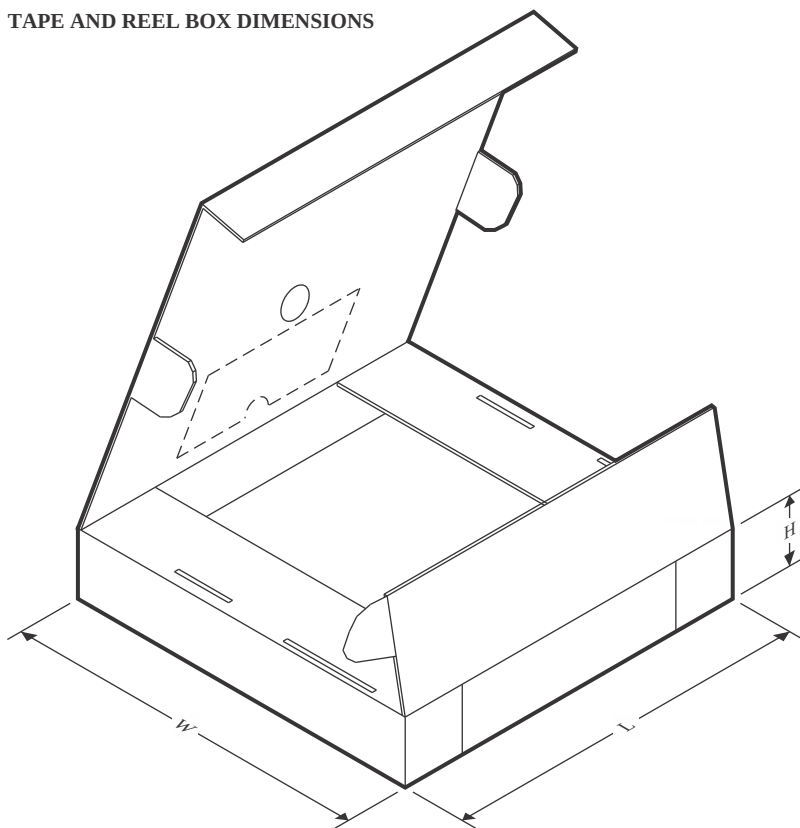
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRSF3221ECDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TRSF3221ECPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRSF3221EIDBR	SSOP	DB	16	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
TRSF3221EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRSF3221EIPWR	TSSOP	PW	16	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
TRSF3221EIRGTR	VQFN	RGT	16	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

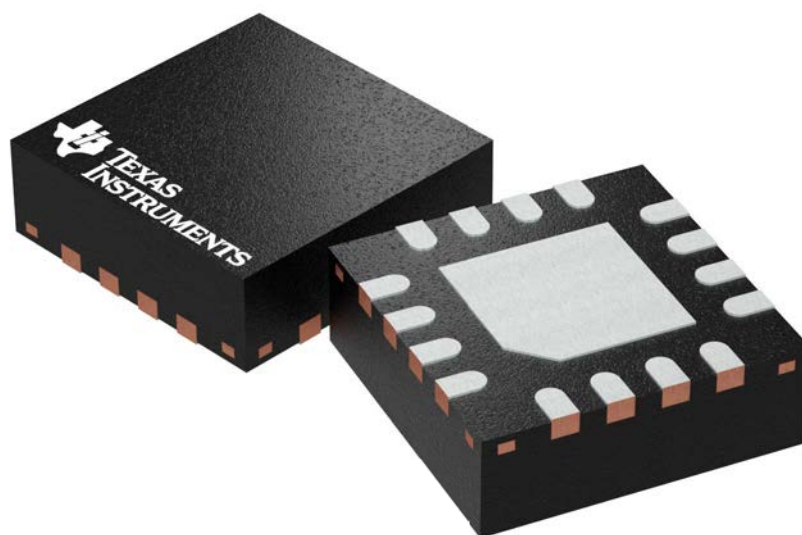
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRSF3221ECDBR	SSOP	DB	16	2000	356.0	356.0	35.0
TRSF3221ECPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TRSF3221EIDBR	SSOP	DB	16	2000	356.0	356.0	35.0
TRSF3221EIPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TRSF3221EIPWR	TSSOP	PW	16	2000	356.0	356.0	35.0
TRSF3221EIRGTR	VQFN	RGT	16	3000	367.0	367.0	35.0

RGT 16

GENERIC PACKAGE VIEW

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



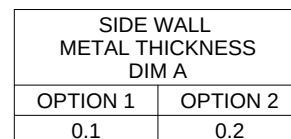
Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4203495/1



VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



4222419/D 04/2022

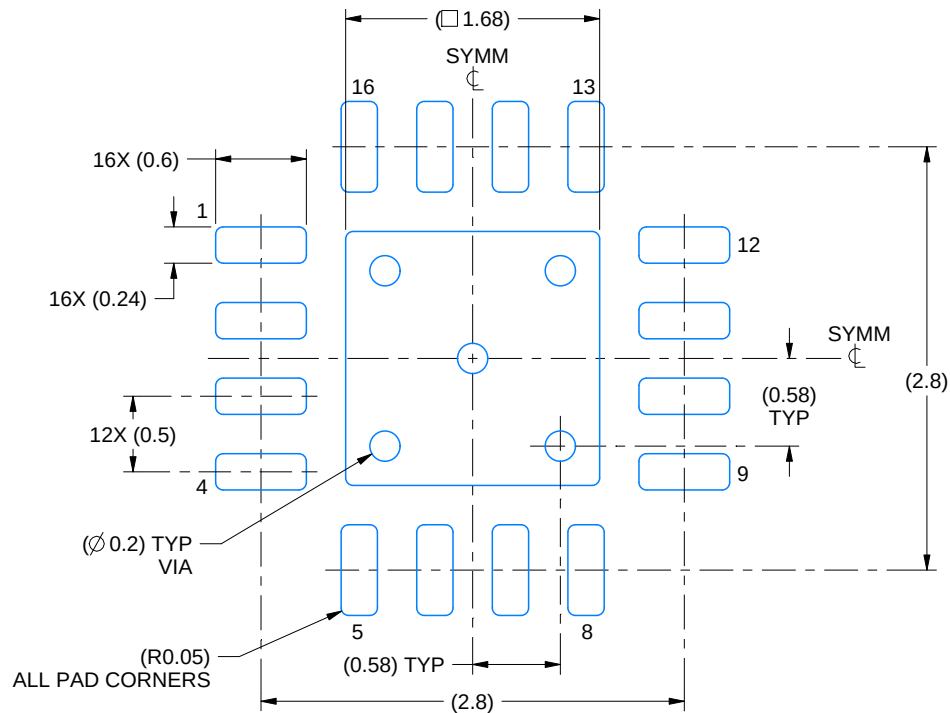
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

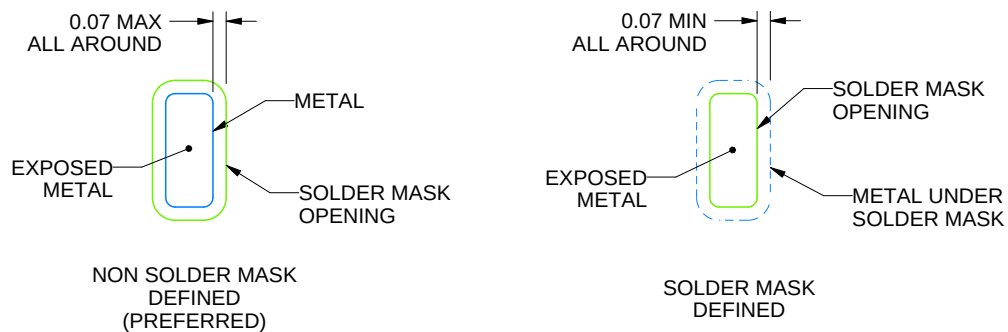
RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:20X



SOLDER MASK DETAILS

4222419/D 04/2022

NOTES: (continued)

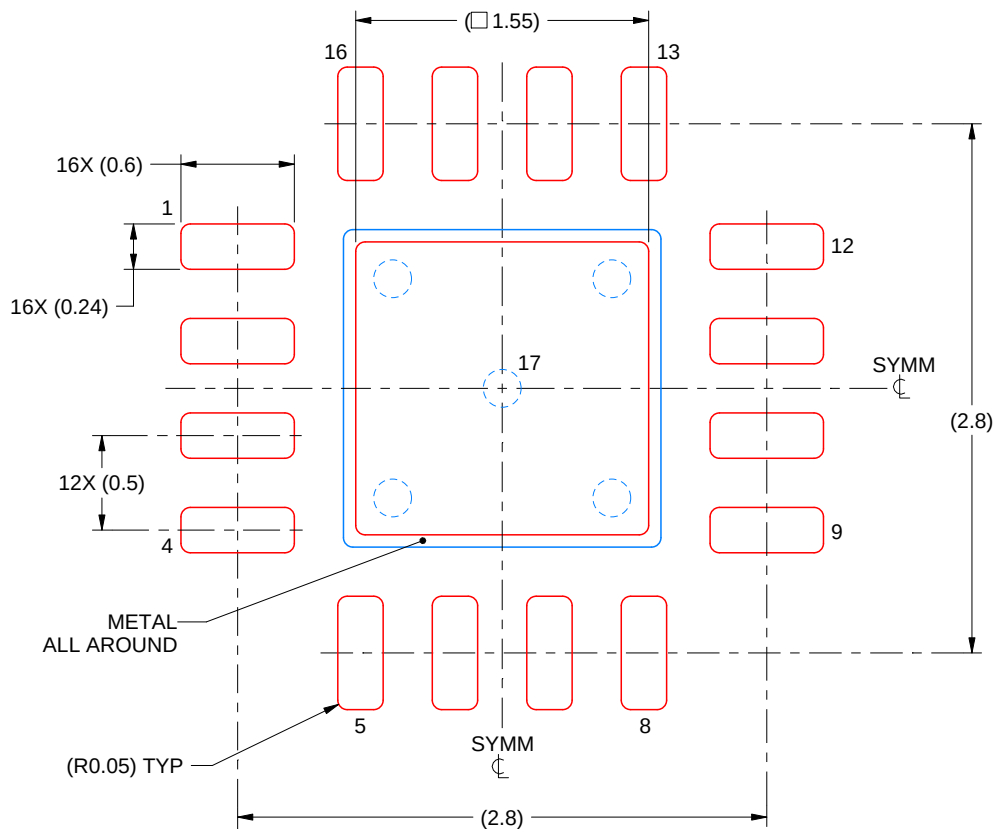
4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/sluea271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.

EXAMPLE STENCIL DESIGN

RGT0016C

VQFN - 1 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



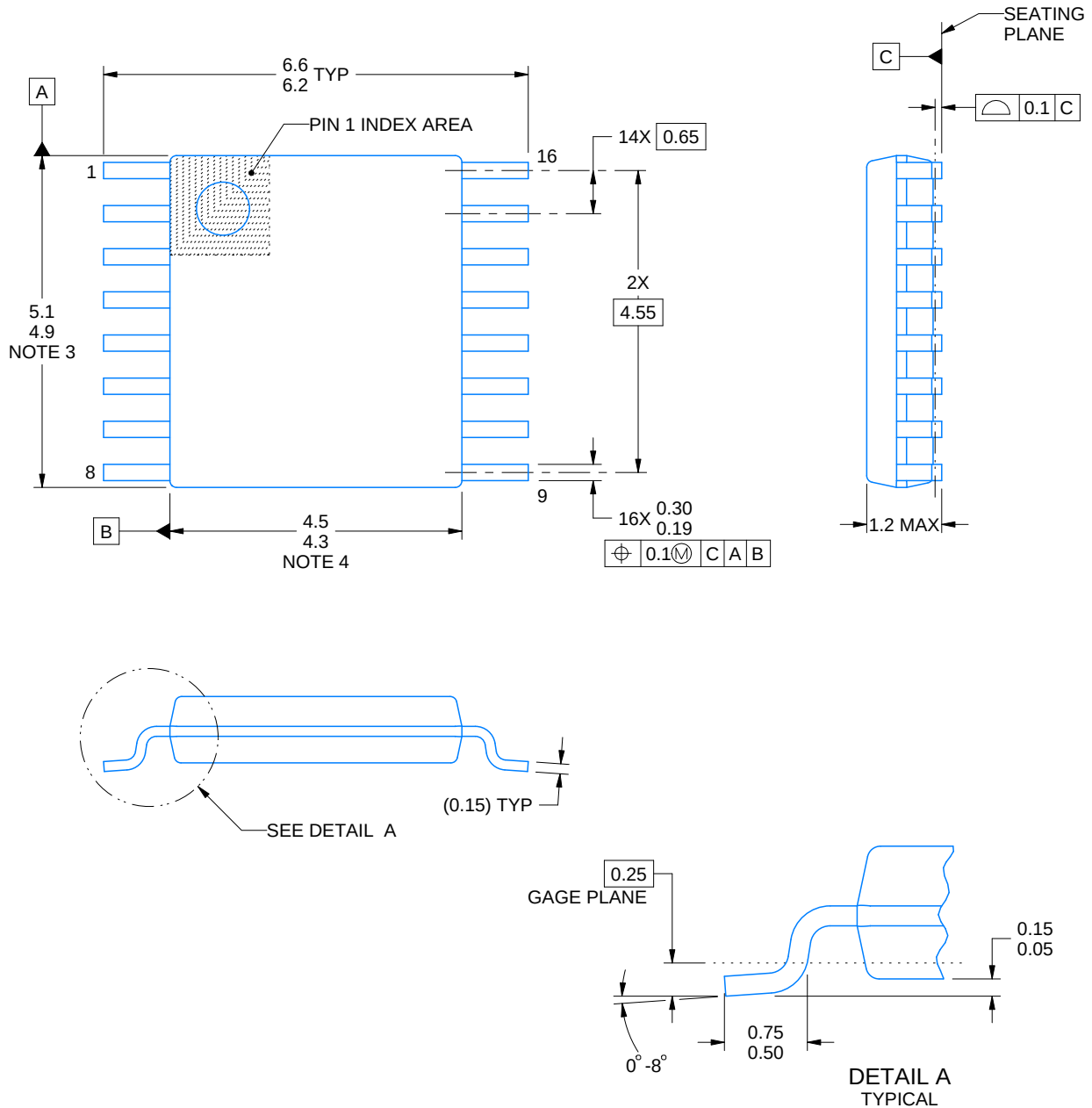
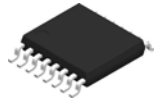
SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 17:
85% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4222419/D 04/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.



4220204/A 02/2017

NOTES:

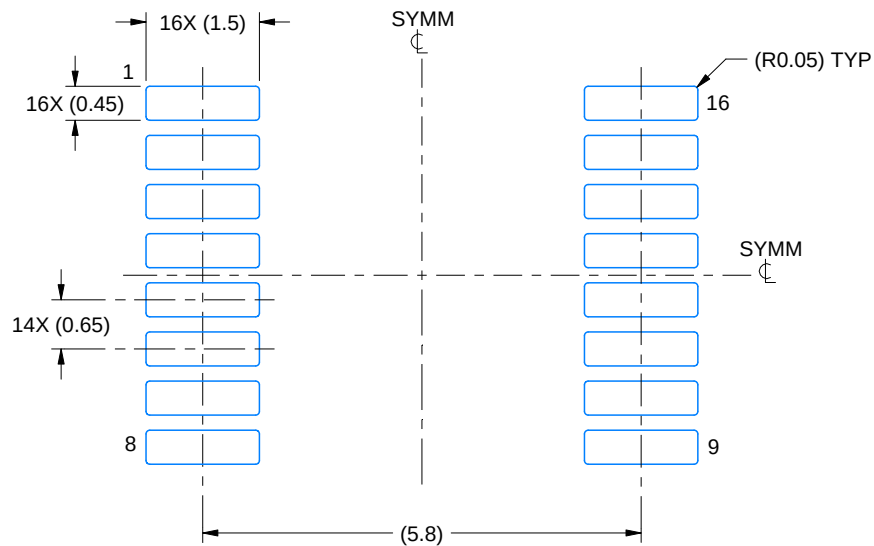
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

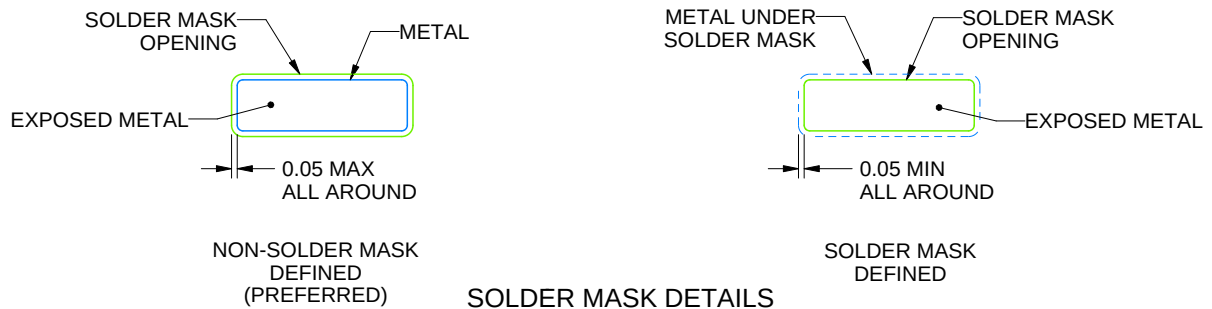
PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

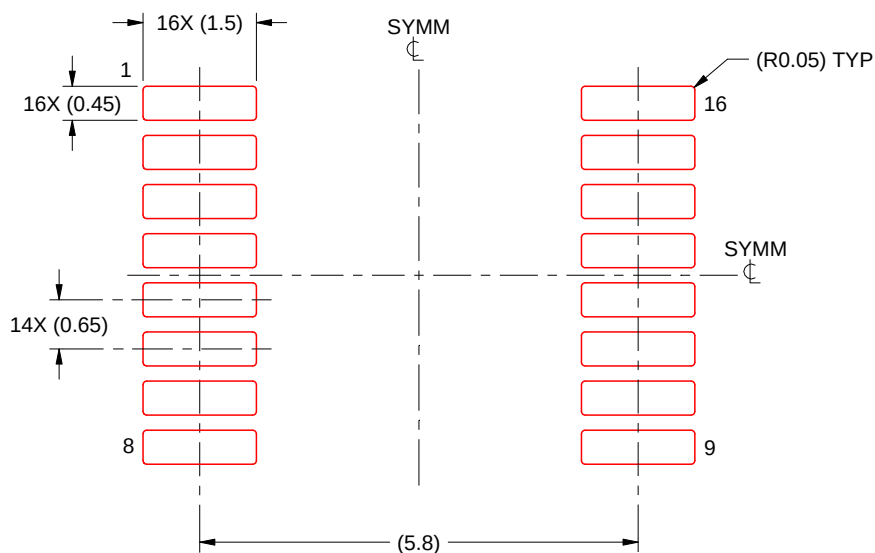
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0016A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

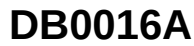


SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



SSOP - 2 mm max height

Technical drawing of a connector housing, showing three views: Top View, Side View, and Detail A (Typical).

Top View:

- Overall dimensions: 8.2 TYP (7.4) width, 5.6 (5.0) width, 6.5 (5.9) height.
- Pin 1 Index Area: A circular area on the left side.
- Pin 16: A pin on the right side.
- Pin 8: A pin on the left side.
- Pin 9: A pin on the right side.
- Pin 14: A pin on the right side.
- Pin 2: A pin on the right side.
- Pin 4: A pin on the right side.
- Pin 6: A pin on the right side.
- Pin 10: A pin on the right side.
- Pin 12: A pin on the right side.
- Pin 14: A pin on the right side.
- Pin 16: A pin on the right side.
- Pin 18: A pin on the right side.
- Pin 20: A pin on the right side.
- Pin 22: A pin on the right side.
- Pin 24: A pin on the right side.
- Pin 26: A pin on the right side.
- Pin 28: A pin on the right side.
- Pin 30: A pin on the right side.
- Pin 32: A pin on the right side.
- Pin 34: A pin on the right side.
- Pin 36: A pin on the right side.
- Pin 38: A pin on the right side.
- Pin 40: A pin on the right side.
- Pin 42: A pin on the right side.
- Pin 44: A pin on the right side.
- Pin 46: A pin on the right side.
- Pin 48: A pin on the right side.
- Pin 50: A pin on the right side.
- Pin 52: A pin on the right side.
- Pin 54: A pin on the right side.
- Pin 56: A pin on the right side.
- Pin 58: A pin on the right side.
- Pin 60: A pin on the right side.
- Pin 62: A pin on the right side.
- Pin 64: A pin on the right side.
- Pin 66: A pin on the right side.
- Pin 68: A pin on the right side.
- Pin 70: A pin on the right side.
- Pin 72: A pin on the right side.
- Pin 74: A pin on the right side.
- Pin 76: A pin on the right side.
- Pin 78: A pin on the right side.
- Pin 80: A pin on the right side.
- Pin 82: A pin on the right side.
- Pin 84: A pin on the right side.
- Pin 86: A pin on the right side.
- Pin 88: A pin on the right side.
- Pin 90: A pin on the right side.
- Pin 92: A pin on the right side.
- Pin 94: A pin on the right side.
- Pin 96: A pin on the right side.
- Pin 98: A pin on the right side.
- Pin 100: A pin on the right side.

Side View:

- Overall dimensions: 0.65 (0.65) width, 4.55 (4.55) height, 0.38 (0.22) width.
- Seating Plane: A horizontal line indicating the seating plane.

Detail A (Typical):

- Overall dimensions: 0.25 (0.25) width, 0.09 (0.09) height, 0.05 MIN (0.05 MIN) width.
- Gage Plane: A horizontal line indicating the gage plane.
- Angle: 0° - 8°.

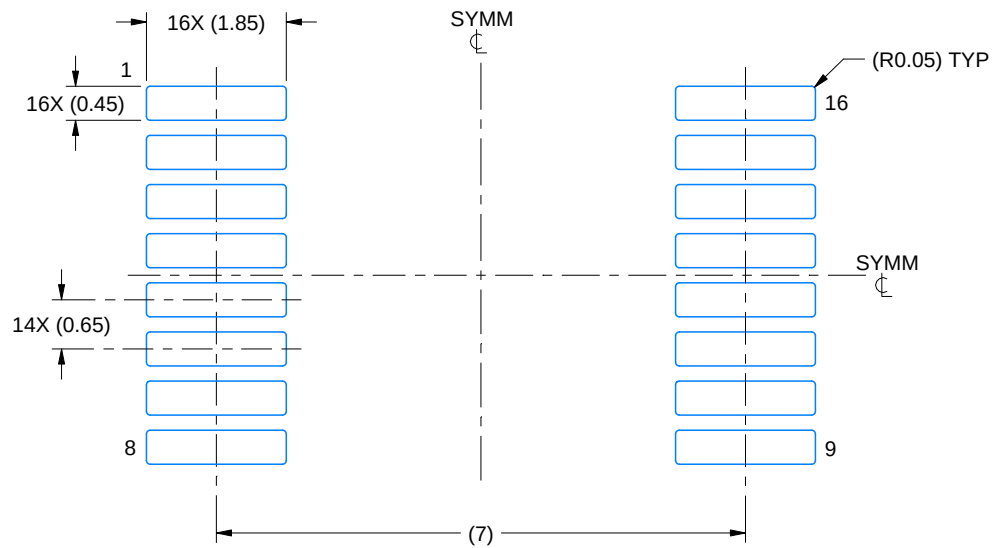
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

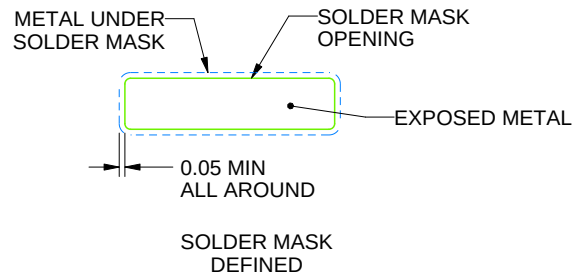
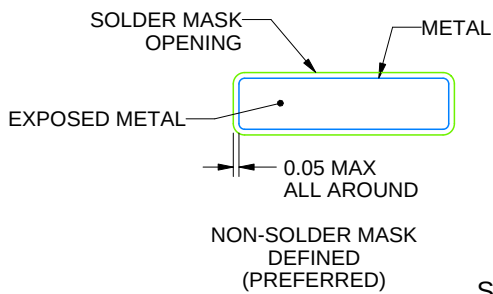
DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220763/A 05/2022

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.

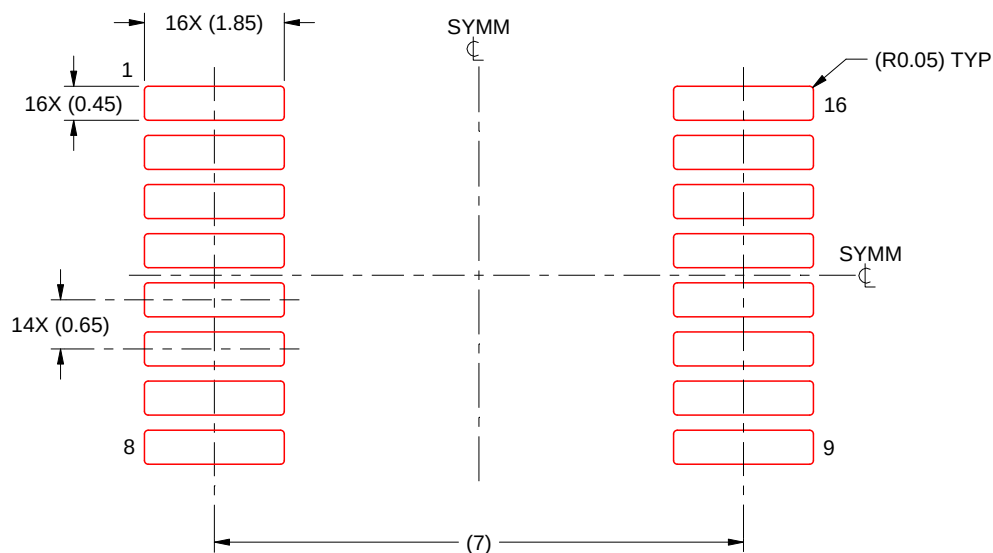
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0016A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220763/A 05/2022

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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郵送先住所：Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
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