参考資料

SNx5HVD1x 3.3V RS-485 トランシーバ

1 特長

- 3.3V 電源で動作
- 16kV HBM を超えるバス・ピンの ESD 保護
- 1/8 ユニット負荷オプション使用可能 (バス上に最大 256 個のノード)
- オプションの信号速度に対するドライバ出力の遷移時間 [1]
- ANSI TIA/EIA-485-A の要件を満たす、または超える性能
- –7V～12V のバス・ピンの短絡保護
- 低消費電力のスタンバイ・モード：1μA (標準値)
- 開回路、アイドル・バス、短絡バスのフェイルセーフ・レシーバ
- サーマル・シャットダウン保護機能
- 電源オンおよび電源オフ時のグリッチ・フリー保護によりホットプラグ・アプリケーションに対応
- SN75176 フットプリント

2 アプリケーション

- デジタル・モーター制御
- 公共料金メーター
- シャーシ間相互接続
- 電子セキュリティ・ステーション
- 産業用プロセス制御
- ビル・オートメーション
- POS 端末とネットワーク

3 概要

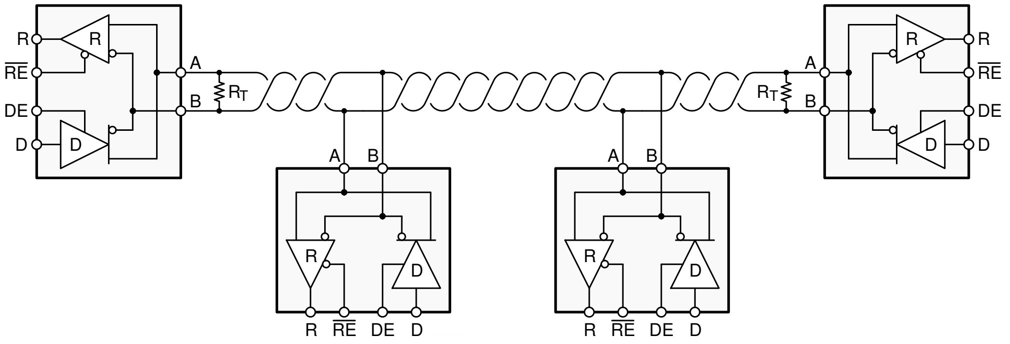
SN65HVD10 、SN75HVD10 、SN65HVD11 、SN75HVD11、SN65HVD12、SN75HVD12 バス・トランシーバは、いずれも 3.3V 単一電源で動作するスリー・ステート差動ライン・ドライバと、差動入力ライン・レシーバを組み合わせています。これらの製品は平衡伝送ラインを想定して設計されており、ANSI 規格の TIA/EIA-485-A および ISO 8482:1993 の要件を満たす、または超える性能を備えます。これらの差動バス・トランシーバは、モノリシック IC であり、マルチポイント・バス伝送ライン上での双方向データ通信を目的として設計されています。ドライバとレシーバはそれぞれアクティブ HIGH、アクティブ LOW のイネーブルを備えており、それらのイネーブルを外部で互いに接続することで、方向制御として機能させることができます。ドライバとレシーバをディスエーブルにすることにより、デバイスのスタンバイ時消費電流を非常に小さくできます。

ドライバの差動出力とレシーバの差動入力は、差動入出力 (I/O) バス・ポートを構成するように内部で接続されています。これらのポートは、ドライバがディセーブルされている場合、または V_{CC} = 0 の場合、バスへの負荷を最小化するように設計されています。これらのポートは広い正負の同相電圧範囲を持っているため、パーティライン・アプリケーションに適しています。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
SN65HVD10 SN65HVD11 SN65HVD12	SOIC (8)	4.90mm × 3.91mm
SN75HVD10 SN75HVD11 SN75HVD12	PDIP (8)	9.81mm × 6.35mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



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代表的なアプリケーションの図

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[1] ラインの信号速度は、1 秒あたりのビット数の bps 単位 (1Mbps、10Mbps、32Mbps) で表される電圧遷移回数

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English Data Sheet: SLLS505

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4 Revision History

Changes from Revision O (February 2017) to Revision P (February 2022)	Page
• Changed the *Thermal Information* table	5

Changes from Revision N (July 2015) to Revision O (February 2017)	Page
• Added MIN value of –55°C to the Storage temperature in *Absolute Maximum Ratings*	4

Changes from Revision M (July 2013) to Revision N (July 2015)	Page
• 「ピン構成および機能」セクション、「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1

Changes from Revision L (July 2013) to Revision M (July 2013)	Page
• Changed the V_{IT+} TYP value From: –0.65 V To: –0.065 V	6

Changes from Revision K (September 2011) to Revision L (July 2013)	Page
• Added TYP = –0.65 V to V_{IT+}	6
• Added TYP = –0.1 V to V_{IT-}	6

Changes from Revision J (February 2009) to Revision K (September 2011)	Page
• Added new section 'LOW-POWER STANDBY MODE', in the Application Information section	18

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5 Device Comparison Table

PART NUMBER		SIGNALING RATE	UNIT LOADS	T_A	SOIC MARKING
SOIC[(1)]	PDIP				
SN65HVD10D	SN65HVD10P	32 Mbps	1/2	–40°C to 85°C	VP10
SN65HVD11D	SN65HVD11P	10 Mbps	1/8		VP11
SN65HVD12D	SN65HVD12P	1 Mbps	1/8		VP12
SN75HVD10D	SN75HVD10P	32 Mbps	1/2	–0°C to 70°C	VN10
SN75HVD11D	SN75HVD11P	10 Mbps	1/8		VN11
SN75HVD12D	SN75HVD12P	1 Mbps	1/8		VN12
SN65HVD10QD	SN65HVD10QP	32 Mbps	1/2	–40°C to 125°C	VP10Q
SN65HVD11QD	SN65HVD11QP	10 Mbps	1/8		VP11Q

(1) The D package is available as a tape and reel. Add an R suffix to the part number (that is, SN75HVD11DR) for this option.

6 Pin Configuration and Functions

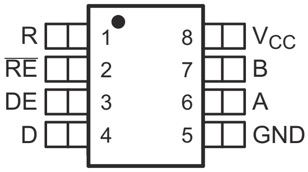

**図 6-1. D, JD, or HKJ Package
8-Pin SOIC or PDIP
(Top View)**

表 6-1. Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Driver output or receiver input (complementary to B)
B	7	Bus input/output	Driver output or receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Active-high driver enable
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Active-low receiver enable
V_{CC}	8	Supply	3-V to 3.6-V supply

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range unless otherwise noted (1) (2)

		MIN	MAX	UNIT
V_{CC}	Supply voltage	–0.3	6	V
	Voltage at A or B	–9	14	V
	Input voltage at D, DE, R, or $\overline{RE}$	–0.5	V_{CC} + 0.5	V
	Voltage input, transient pulse, A and B, through 100 Ω, see 図 8-12	–50	50	V
I_O	Receiver output current	–11	11	mA
	Continuous total power dissipation	See *セクション 7.10*		
T_J	Junction temperature		170	°C
T_{stg}	Storage temperature	–55	145	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *セクション 7.3* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	Pins 5, 6, and 7	±16000	V
			All pins	±4000	
		Charged device model (CDM), per JEDEC specification JESD22-C101(2)	All pins	±1000	
		Electrical fast transient/burst(3)	Pins 5, 6, and 7	±4000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.
(3) Tested in accordance with IEC 61000-4-4.

7.3 Recommended Operating Conditions

over operating free-air temperature range unless otherwise noted

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		3		3.6	V
V_I or V_{IC}	Voltage at any bus terminal (separately or common mode)		–7(1)		12	
V_{IH}	High-level input voltage	D, DE, $\overline{RE}$	2		V_{CC}	
V_{IL}	Low-level input voltage	D, DE, $\overline{RE}$	0		0.8	
V_{ID}	Differential input voltage	See 図 8-8	–12		12	
I_{OH}	High-level output current	Driver	–60			mA
		Receiver	–8			
I_{OL}	Low-level output current	Driver			60	mA
		Receiver			8	
R_L	Differential load resistance		54	60		Ω
C_L	Differential load capacitance			50		pF
	Signaling rate	HVD10			32	Mbps
		HVD11			10	
		HVD12			1	
T_J (2)	Junction temperature				145	°C

(1) The algebraic convention, in which the least positive (most negative) limit is designated as minimum is used in this data sheet.
(2) See thermal characteristics table for information regarding this specification.

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7.4 Thermal Information

THERMAL METRIC(1)		SNx5HVD1xx		UNIT
		D (SOIC)	P (PDIP)	
		8 Pins	8 Pins	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	116.7	84.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	56.3	65.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	63.4	62.1	°C/W
ψ_{JT}	Junction-to-top characterization parameter	8.8	31.3	°C/W
ψ_{JB}	Junction-to-board characterization parameter	62.6	60.4	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.

7.5 Driver Electrical Characteristics

Over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
V_{IK}	Input clamp voltage		$I_I = –18$ mA		–1.5			V
$\|V_{OD}\|$	Differential output voltage(2)		$I_O = 0$		2		V_{CC}	V
			R_L = 54 Ω, See 図 8-1		1.5			
			V_{test} = –7 V to 12 V, See 図 8-2		1.5			
$\Delta\|V_{OD}\|$	Change in magnitude of differential output voltage		See 図 8-1 and 図 8-2		–0.2		0.2	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage		See 図 8-3			400		mV
$V_{OC(SS)}$	Steady-state common-mode output voltage				1.4		2.5	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage				–0.05		0.05	V
I_{OZ}	High-impedance output current		See receiver input currents					
I_I	Input current	D			–100		0	µA
		DE			0		100	
I_{OS}	Short-circuit output current		$–7\text{ V} \le V_O \le 12\text{ V}$		–250		250	mA
$C_{(OD)}$	Differential output capacitance		V_{OD} = 0.4 sin(4E6πt) + 0.5 V, DE at 0 V			16		pF
I_{CC}	Supply current		$\overline{RE}$ at V_{CC}, D and DE at V_{CC}, No load	Receiver disabled and driver enabled		9	15.5	mA
			$\overline{RE}$ at V_{CC}, D at V_{CC}, DE at 0 V, No load	Receiver disabled and driver disabled (standby)		1	5	µA
			$\overline{RE}$ at 0 V, D and DE at V_{CC}, No load	Receiver enabled and driver enabled		9	15.5	mA

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) For $T_A > 85°C$, V_{CC} is ±5%.

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7.6 Receiver Electrical Characteristics

Over recommended operating conditions unless otherwise noted

PARAMETER		TEST CONDITIONS		MIN	TYP[1]	MAX	UNIT
V_{IT+}	Positive-going input threshold voltage	I_O = –8 mA			–0.065	–0.01	V
$V_{IT–}$	Negative-going input threshold voltage	I_O = 8 mA		–0.2	–0.1		
V_{hys}	Hysteresis voltage (V_{IT+} – $V_{IT–}$)				35		mV
V_{IK}	Enable-input clamp voltage	I_I = –18 mA		–1.5			V
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –8 mA, see 図 8-8		2.4			V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_{OL} = 8 mA, see 図 8-8				0.4	V
I_{OZ}	High-impedance-state output current	V_O = 0 or V_{CC}, $\overline{RE}$ at V_{CC}		–1		1	μA
I_I	Bus input current	V_A or V_B = 12 V	HVD11, HVD12, Other inputs at 0 V		0.05	0.11	mA
		V_A or V_B = 12 V, V_{CC} = 0 V			0.06	0.13	
		V_A or V_B = –7 V		–0.1	–0.05		
		V_A or V_B = –7 V, V_{CC} = 0 V		–0.05	–0.04		
		V_A or V_B = 12 V	HVD10, Other inputs at 0 V		0.2	0.5	mA
		V_A or V_B = 12 V, V_{CC} = 0 V			0.25	0.5	
		V_A or V_B = –7 V		–0.4	–0.2		
		V_A or V_B = –7 V, V_{CC} = 0 V		–0.4	–0.15		
I_{IH}	High-level input current, $\overline{RE}$	V_{IH} = 2 V		–30		0	μA
I_{IL}	Low-level input current, $\overline{RE}$	V_{IL} = 0.8 V		–30		0	μA
C_{ID}	Differential input capacitance	V_{ID} = 0.4 sin(4E6πt) + 0.5 V, DE at 0 V			15		pF
I_{CC}	Supply current	$\overline{RE}$ at 0 V D and DE at 0 V No load	Receiver enabled and driver disabled		4	8	mA
		$\overline{RE}$ at V_{CC} D at V_{CC} DE at 0 V No load	Receiver disabled and driver disabled (standby)		1	5	μA
		$\overline{RE}$ at 0 V D and DE at V_{CC} No load	Receiver enabled and driver enabled		9	15.5	mA

(1) All typical values are at 25°C and with a 3.3-V supply.

7.7 Power Dissipation Characteristics

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
P_D	Device power dissipation	R_L= 60 Ω, C_L = 50 pF, DE at V_{CC}, $\overline{RE}$ at 0 V, Input to D is a 50% duty-cycle square wave at indicated signaling rate	HVD10 (32Mbps)		198	250	mW
			HVD11 (10Mbps)		141	176	
			HVD12 (500 kbps)		133	161	
T_A	Ambient air temperature[1]	High-K board, no airflow	D pkg	–40		116	°C
		No airflow[2]	P pkg	–40		123	
T_{JSD}	Thermal shutdown junction temperature[1]				165		°C

(1) See *セクション 12.3.1* section for an explanation of these parameters.
(2) JESD51−10, Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements.

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7.8 Driver Switching Characteristics

Over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	HVD10	R_L = 54 Ω, C_L = 50 pF See 図 8-4	5	8.5	16	ns
		HVD11		18	25	40	
		HVD12		135	200	300	
t_{PHL}	Propagation delay time, high-to-low-level output	HVD10		5	8.5	16	ns
		HVD11		18	25	40	
		HVD12		135	200	300	
t_r	Differential output signal rise time	HVD10		3	4.5	10	ns
		HVD11		10	20	30	
		HVD12		100	170	300	
t_f	Differential output signal fall time	HVD10		3	4.5	10	ns
		HVD11		10	20	30	
		HVD12		100	170	300	
$t_{sk(p)}$	Pulse skew ($\lvert t_{PHL} – t_{PLH}\rvert$)	HVD10				1.5	ns
		HVD11				2.5	
		HVD12				7	
$t_{sk(pp)}$ [2]	Part-to-part skew	HVD10				6	ns
		HVD11				11	
		HVD12				100	
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	HVD10	R_L = 110 Ω, $\overline{RE}$ at 0 V See 図 8-5			31	ns
		HVD11				55	
		HVD12				300	
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output	HVD10				25	ns
		HVD11				55	
		HVD12				300	
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	HVD10	R_L = 110 Ω, $\overline{RE}$ at 0 V See 図 8-6			26	ns
		HVD11				55	
		HVD12				300	
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output	HVD10				26	ns
		HVD11				75	
		HVD12				400	
t_{PZH}	Propagation delay time, standby-to-high-level output		R_L = 110 Ω, $\overline{RE}$ at 3 V See 図 8-5			6	µs
t_{PZL}	Propagation delay time, standby-to-low-level output		R_L = 110 Ω, $\overline{RE}$ at 3 V See 図 8-6			6	µs

(1) All typical values are at 25°C and with a 3.3-V supply.
(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

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7.9 Receiver Switching Characteristics

Over recommended operating conditions unless otherwise noted

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	HVD10	V_{ID} = –1.5 V to 1.5 V C_L = 15 pF See 図 8-9	12.5	20	25	ns
t_{PHL}	Propagation delay time, high-to-low-level output	HVD10		12.5	20	25	
t_{PLH}	Propagation delay time, low-to-high-level output	HVD11 HVD12		30	55	70	ns
t_{PHL}	Propagation delay time, high-to-low-level output	HVD11 HVD12		30	55	70	ns
$t_{sk(p)}$	Pulse skew ($\|t_{PHL} – t_{PLH}\|$)	HVD10				1.5	ns
		HVD11				4	
		HVD12				4	
$t_{sk(pp)}$ (2)	Part-to-part skew	HVD10				8	ns
		HVD11				15	
		HVD12				15	
t_r	Output signal rise time		C_L = 15 pF See 図 8-9	1	2	5	ns
t_f	Output signal fall time			1	2	5	
t_{PZH} (1)	Output enable time to high level		C_L = 15 pF, DE at 3 V See 図 8-10			15	ns
t_{PZL} (1)	Output enable time to low level					15	
t_{PHZ}	Output disable time from high level					20	
t_{PLZ}	Output disable time from low level					15	
t_{PZH} (2)	Propagation delay time, standby-to-high-level output		C_L = 15 pF, DE at 0 See 図 8-11			6	µs
t_{PZL} (2)	Propagation delay time, standby-to-low-level output					6	

(1) All typical values are at 25°C and with a 3.3-V supply

(2) $t_{sk(pp)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices when both devices operate with the same supply voltages, at the same temperature, and have identical packages and test circuits.

7.10 Dissipation Ratings

PACKAGE	T_A ≤ 25°C POWER RATING	DERATING FACTOR(1) ABOVE T_A = 25°C	T_A = 70°C POWER RATING	T_A = 85°C POWER RATING	T_A = 125°C POWER RATING
D(2)	597 mW	4.97 mW/°C	373 mW	298 mW	100 mW
D(3)	990 mW	8.26 mW/°C	620 mW	496 mW	165 mW
P	1290 mW	10.75 mW/°C	806 mW	645 mW	215 mW

(1) This is the inverse of the junction-to-ambient thermal resistance when board-mounted and with no air flow.

(2) Tested in accordance with the Low-K thermal metric definitions of EIA/JESD51-3.

(3) Tested in accordance with the High-K thermal metric definitions of EIA/JESD51-7.

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7.11 Typical Characteristics

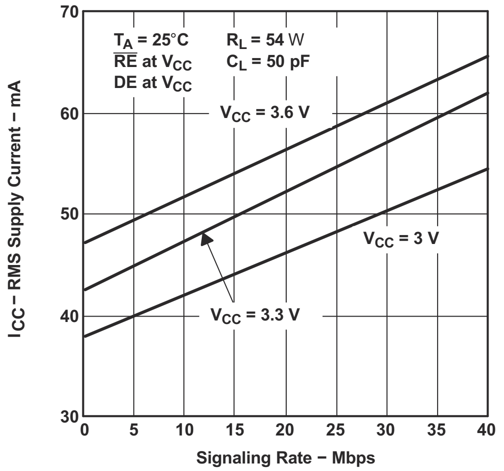

図 7-1. HVD10 RMS Supply Current vs Signaling Rate

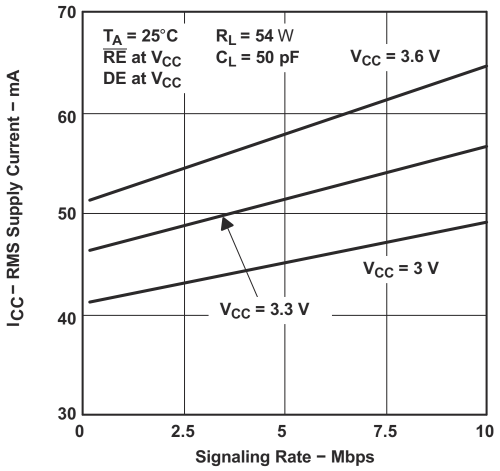

図 7-2. HVD11 RMS Supply Current vs Signaling Rate

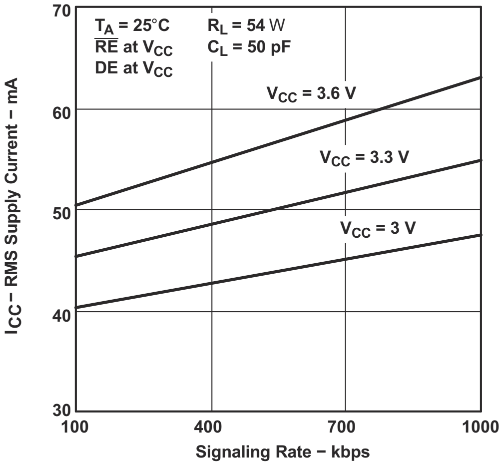

図 7-3. HVD12 RMS Supply Current vs Signaling Rate

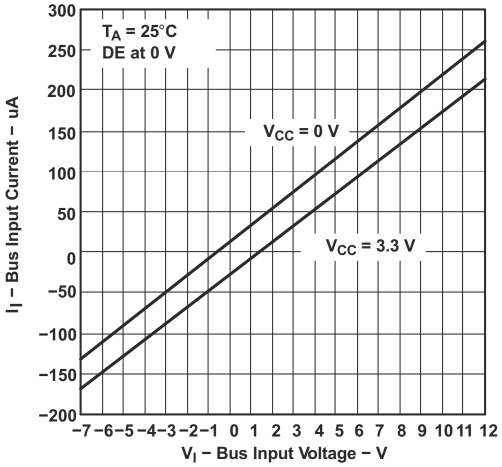

図 7-4. HVD10 Bus Input Current vs Bus Input Voltage

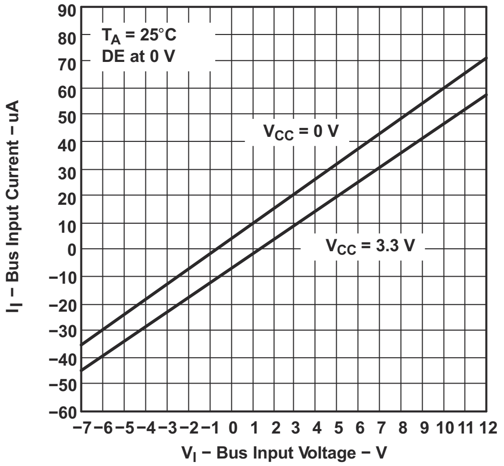

図 7-5. HVD11 or HVD12 Bus Input Current vs Bus Input Voltage

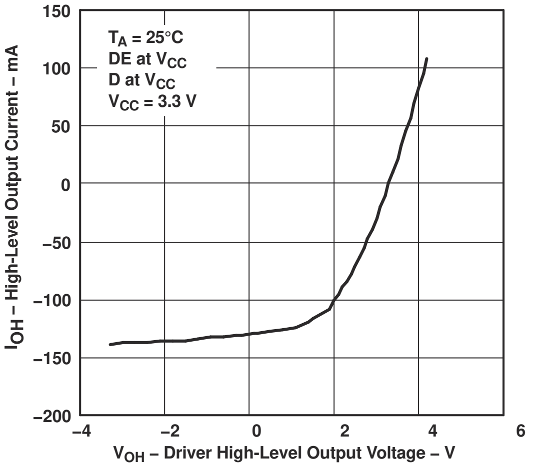

図 7-6. High-Level Output Current vs Driver High-Level Output Voltage

7.11 Typical Characteristics (continued)

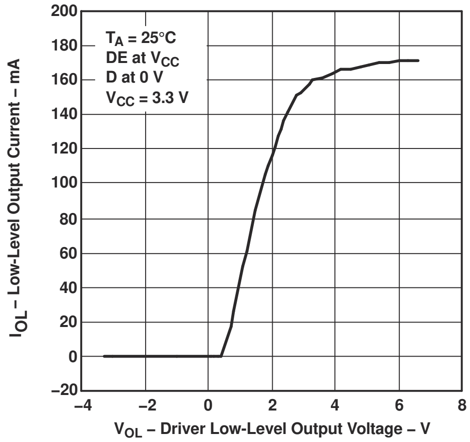

図 7-7. Low-Level Output Current vs Driver Low-Level Output Voltage

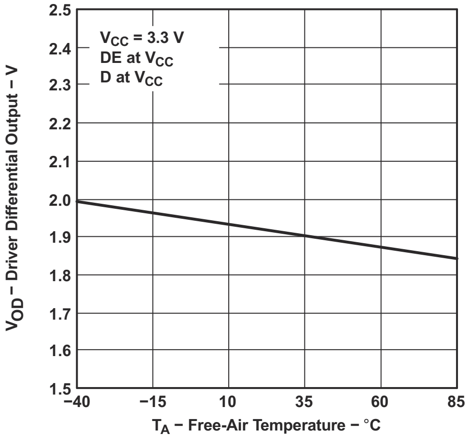

図 7-8. Driver Differential Output vs Free-Air Temperature

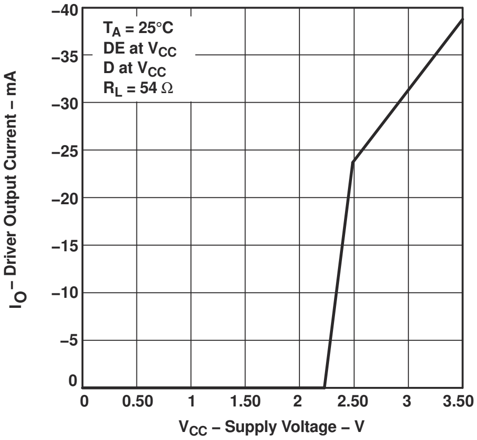

図 7-9. Driver Output Current vs Supply Voltage

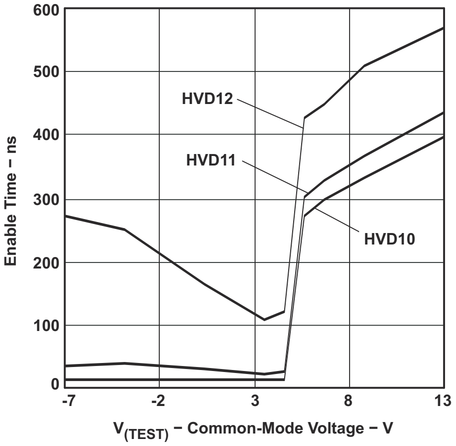

図 7-10. Enable Time vs Common-Mode Voltage

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8 Parameter Measurement Information

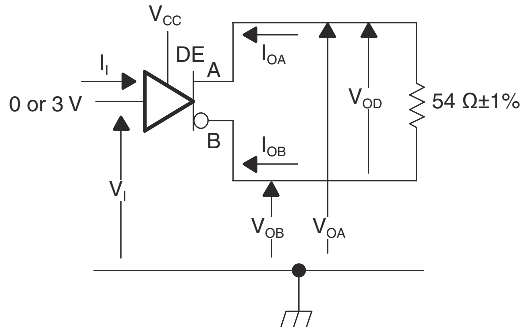

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図 8-1. Driver V_{OD} Test Circuit and Voltage and Current Definitions

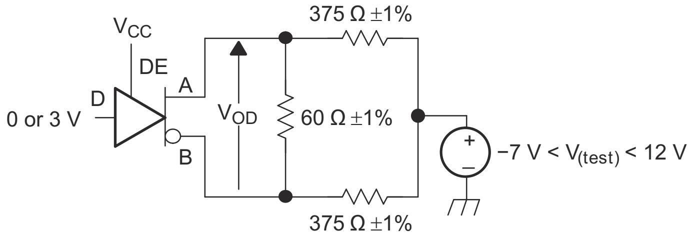

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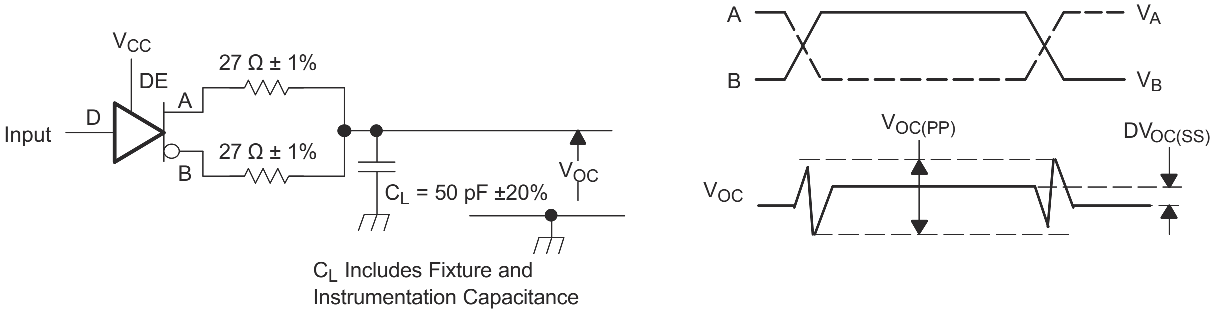
図 8-2. Driver V_{OD} With Common-Mode Loading Test Circuit



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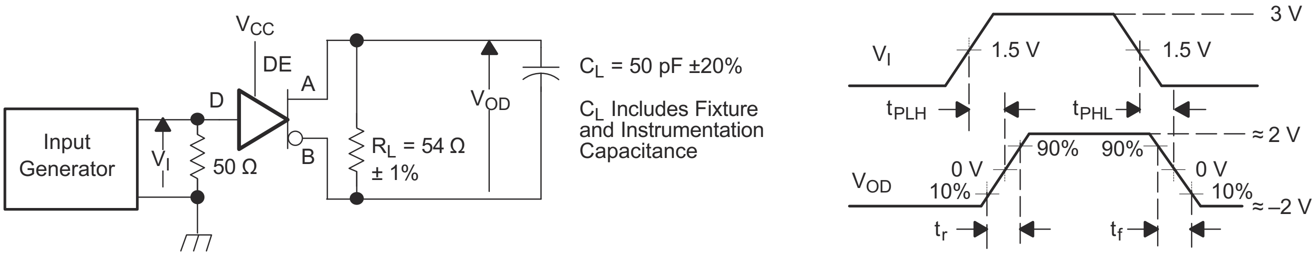
Input: PRR = 500 kHz, 50% Duty Cycle, t_r < 60 ns, t_f < 6 ns Z_O = 50 Ω

図 8-3. Test Circuit and Definitions for the Driver Common-Mode Output Voltage



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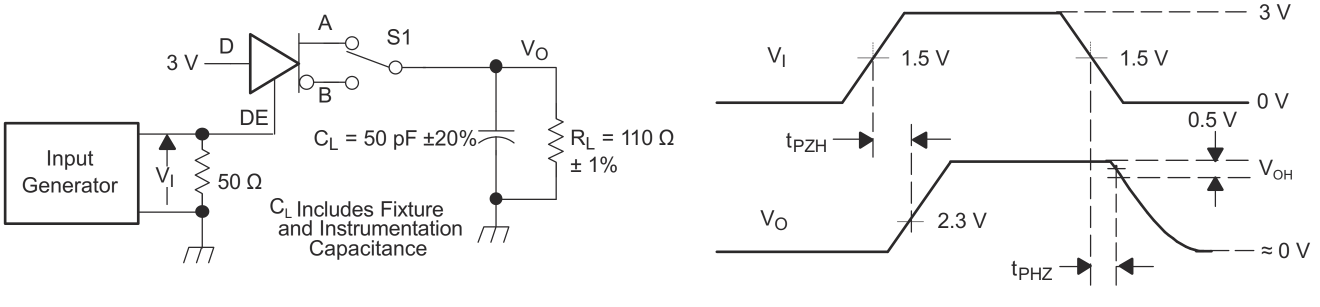
Generator: PRR = 500 kHz, 50% Duty Cycle, t_r < 60 ns, t_f < 6 ns Z_O = 50 Ω

図 8-4. Driver Switching Test Circuit and Voltage Waveforms



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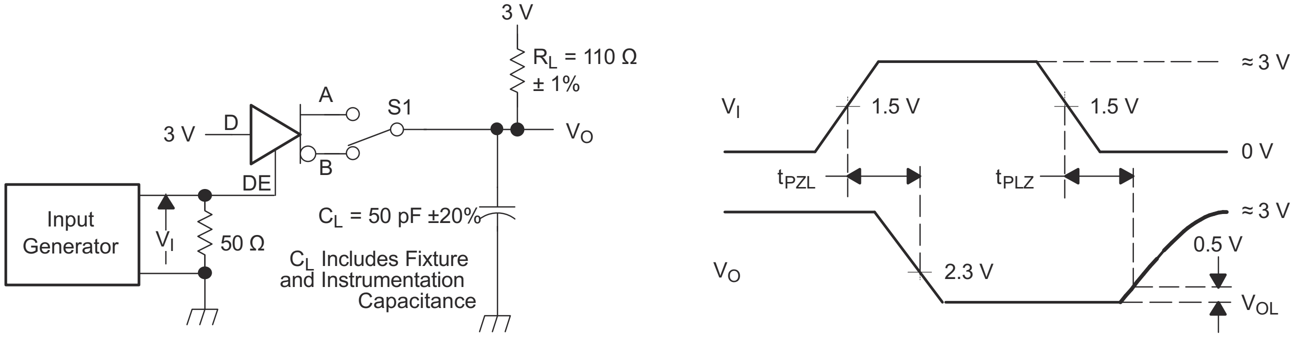
Generator: PRR = 500 kHz, 50% Duty Cycle, t_r < 60 ns, t_f < 6 ns Z_O = 50 Ω

図 8-5. Driver High-Level Enable and Disable Time Test Circuit and Voltage Waveforms



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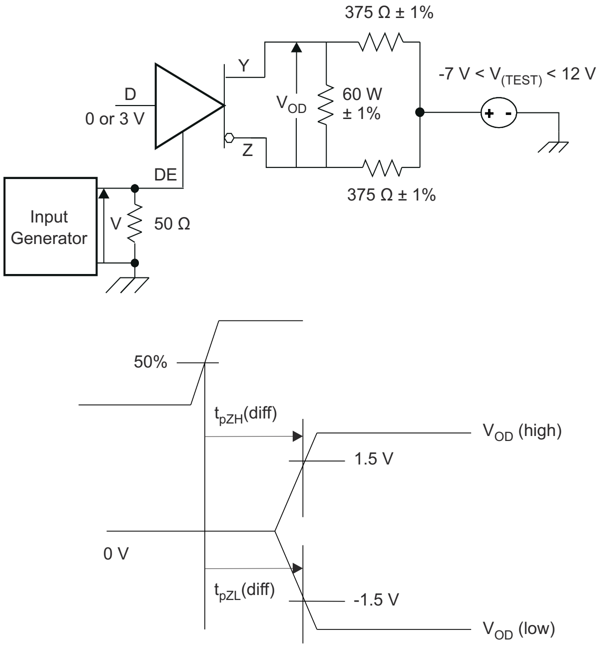
Generator: PRR = 500 kHz, 50% Duty Cycle, t_r < 60 ns, t_f < 6 ns Z_O = 50 Ω

図 8-6. Driver Low-Level Output Enable and Disable Time Test Circuit and Voltage Waveforms



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The time $t_{PZL(x)}$ is the measure from DE to $V_{OD}(x)$. V_{OD} is valid when it is greater than 1.5 V.

図 8-7. Driver Enable Time from DE to V_{OD}

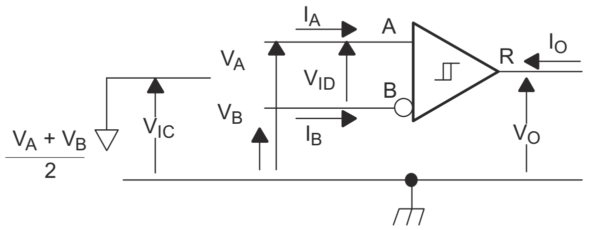

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図 8-8. Receiver Voltage and Current Definitions

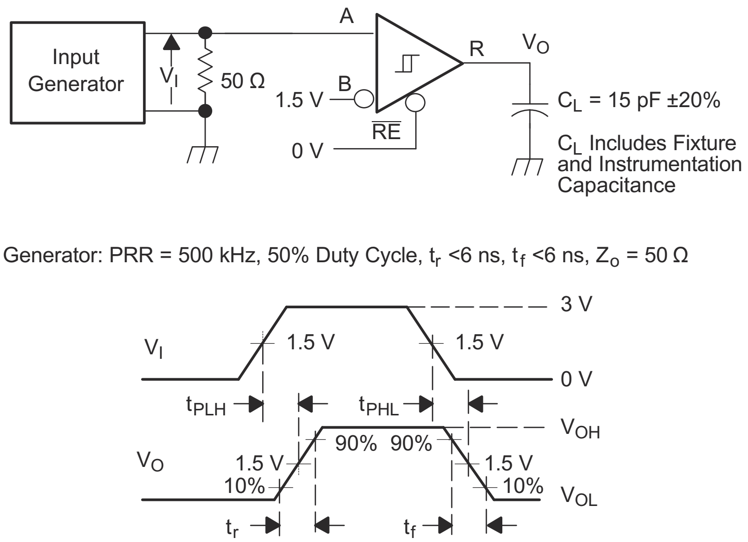

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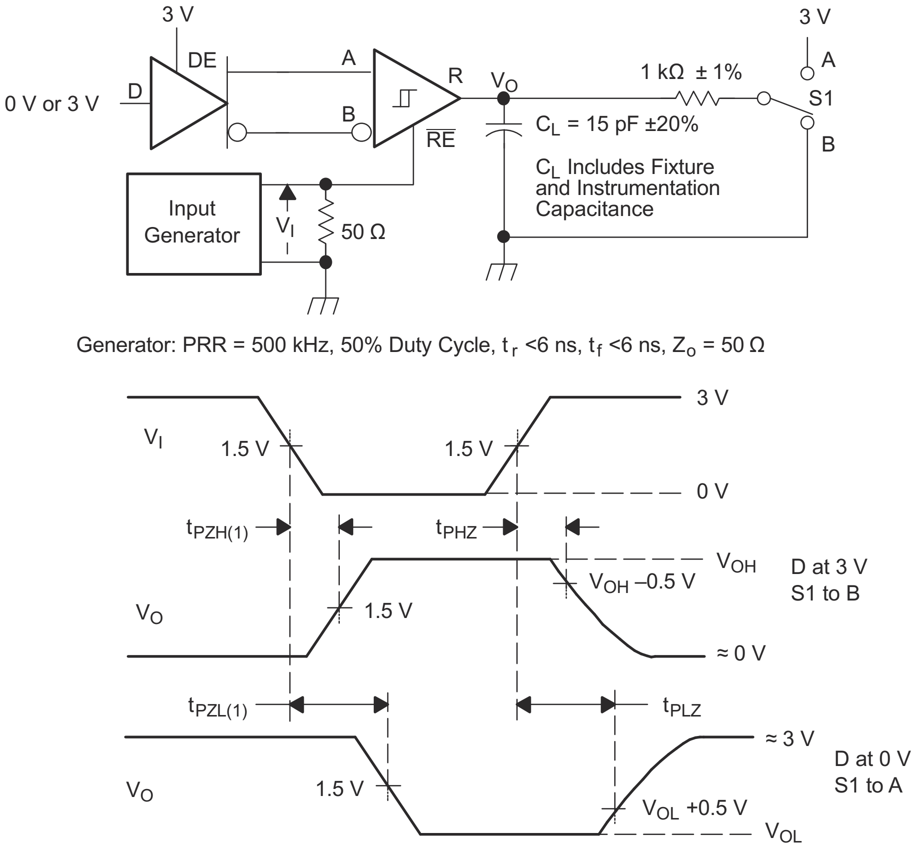
図 8-9. Receiver Switching Test Circuit and Voltage Waveforms



Generator: PRR = 500 kHz, 50% Duty Cycle, t_r <6 ns, t_f <6 ns, Z_o = 50 Ω

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図 8-10. Receiver Enable and Disable Time Test Circuit and Voltage Waveforms With Drivers Enabled

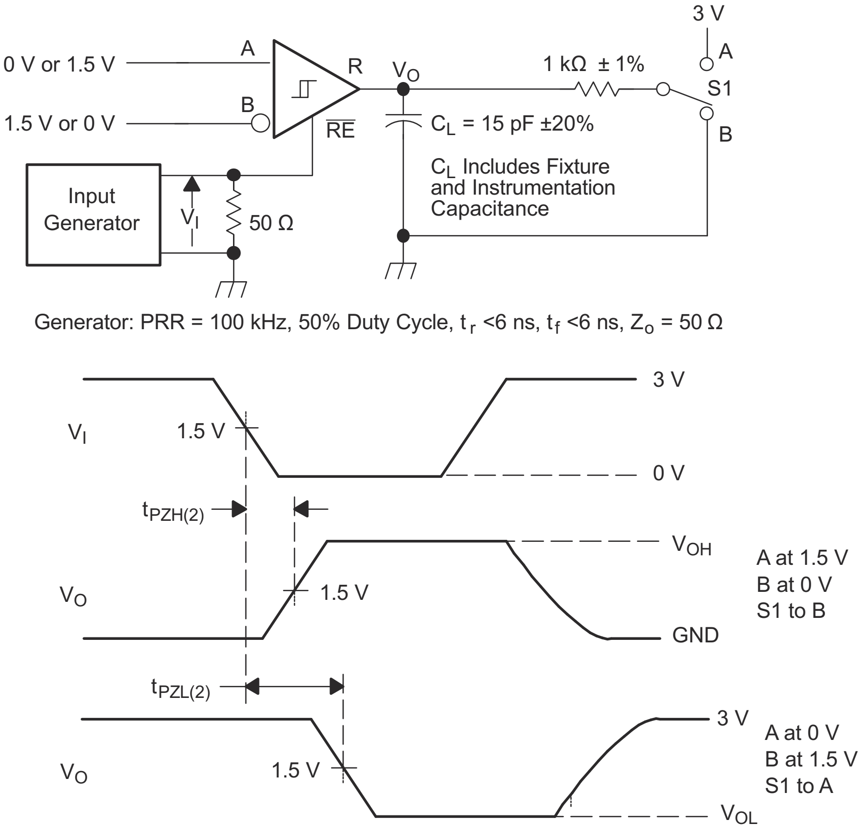

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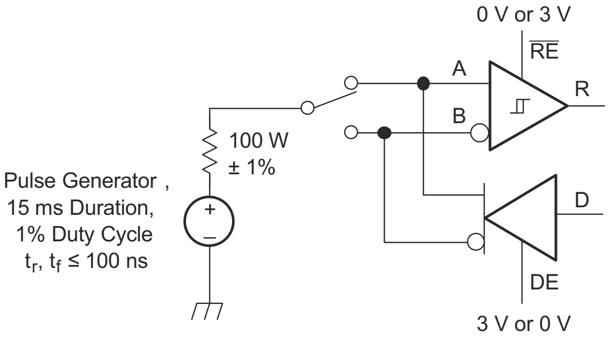
図 8-11. Receiver Enable Time From Standby (Driver Disabled)



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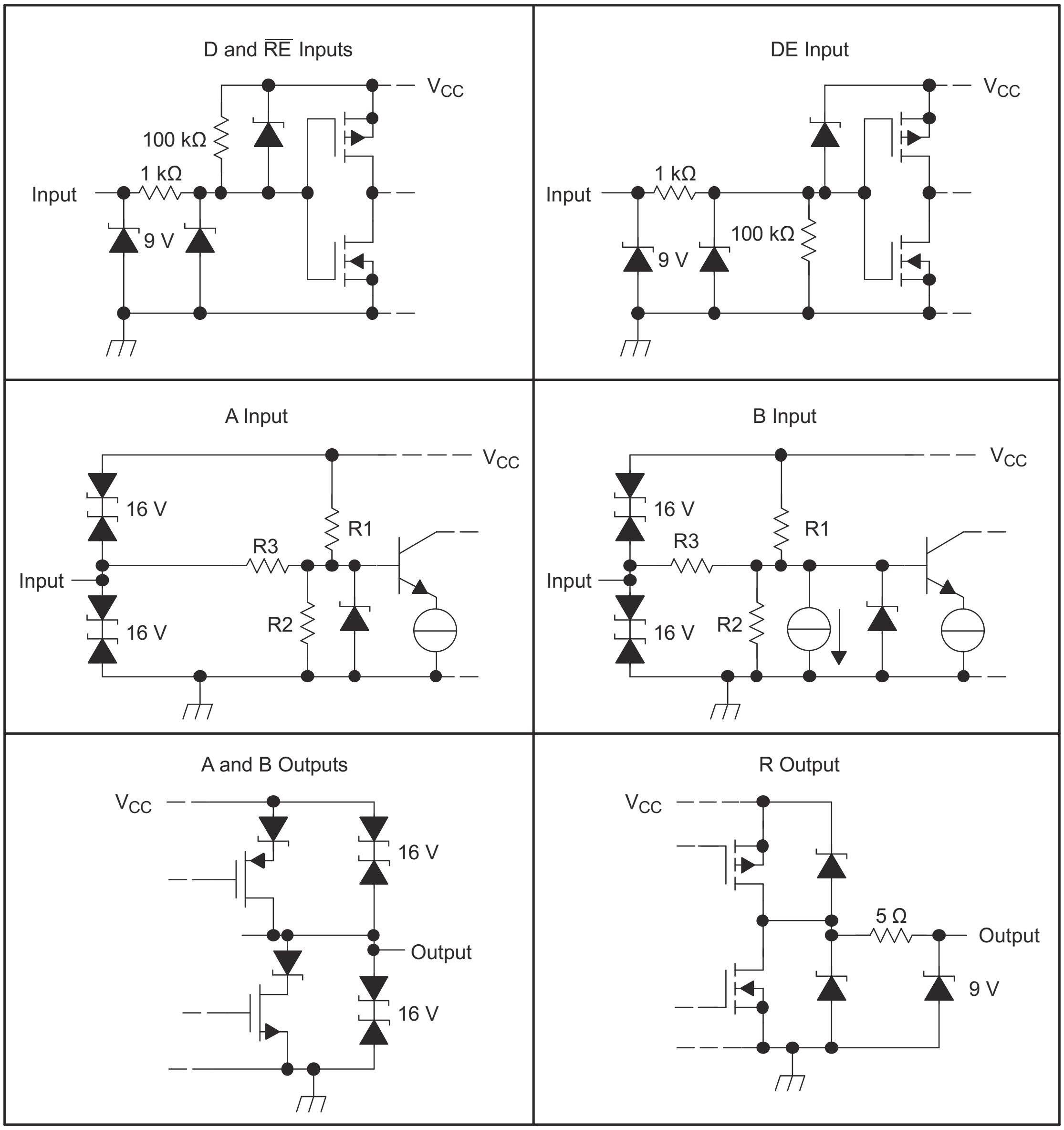
NOTE: This test is conducted to test survivability only. Data stability at the R output is not specified.

図 8-12. Test Circuit, Transient Over Voltage Test



	R1/R2	R3
SN65HVD10	9 kW	45 kW
SN65HVD11	36 kW	180 kW
SN65HVD12	36 kW	180 kW

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図 8-13. Equivalent Input and Output Schematic Diagrams

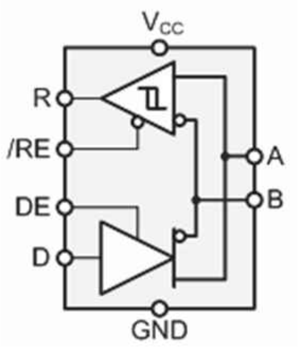
9 Detailed Description

9.1 Overview

The SN65HVD10, SN65HVD11, and SN65HVD12 are 3.3 V, half-duplex, and RS-485 transceivers that are available in 3 speed grades suitable for data transmission up to 32 Mbps, 10 Mbps, and 1 Mbps.

These devices have both active-high driver enables and active-low receiver enables. A standby current of less than
5 µA can be achieved by disabling both driver and receiver.

9.2 Functional Block Diagram



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9.3 Feature Description

Internal ESD protection circuits protect the transceiver bus terminals against ±16-kV Human Body Model (HBM) electrostatic discharges and ±4-kV electrical fast transients (EFT) according to IEC61000-4-4.

The SN65HVD1x half-duplex family provides internal biasing of the receiver input thresholds for open-circuit, bus-idle, or short-circuit fail-safe conditions, as well as a typical receiver hysteresis of 35 mV.

9.4 Device Functional Modes

When the driver enable pin, DE, is logic high, the differential outputs A and B follow the logic states at data input D. A logic high at D causes A to turn high and B to turn low. In this case, the differential output voltage defined as $V_{OD} = V_A - V_B$ is positive. When D is low, the output states reverse, B turns high, A becomes low, and V_{OD} is negative.

When DE is low, both outputs turn high-impedance. In this condition, the logic state at D is irrelevant. The DE pin has an internal pulldown resistor to ground; therefore, when left open, the driver is disabled (high-impedance) by default. The D pin has an internal pullup resistor to V_{CC}; therefore, when left open while the driver is enabled, output A turns high and B turns low.

表 9-1. Driver Functions(1)

INPUT	ENABLE	OUTPUTS		FUNCTION
D	DE	A	B	
H	H	H	L	Actively drive bus High
L	H	L	H	Actively drive bus Low
X	L	Z	Z	Driver disabled
X	OPEN	Z	Z	Driver disabled by default
OPEN	H	H	L	Actively drive bus High by default

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

When the receiver enable pin, $\overline{RE}$, is logic low, the receiver is enabled. When the differential input voltage defined as $V_{ID} = V_A - V_B$ is positive and higher than the positive input threshold, V_{IT+}, the receiver output, R, turns high. When V_{ID} is negative and lower than the negative input threshold, V_{IT-}, the receiver output, R, turns low. If V_{ID} is between V_{IT+} and V_{IT-}, the output is indeterminate.

When $\overline{RE}$ is logic high or left open, the receiver output is high-impedance and the magnitude and polarity of V_{ID} are irrelevant. Internal biasing of the receiver inputs causes the output to go fail-safe-high when the transceiver is disconnected from the bus (open-circuit), the bus lines are shorted (short-circuit), or when the bus is not actively driven (idle bus).

表 9-2. Receiver Functions(1)

DIFFERENTIAL INPUT $V_{ID} = V_A - V_B$	ENABLE $\overline{RE}$	OUTPUT R	FUNCTION
$V_{ID} > V_{IT+}$	L	H	Receive valid bus High
$V_{IT-} < V_{ID} < V_{IT+}$	L	?	Indeterminate bus state
$V_{ID} < V_{IT-}$	L	L	Receive valid bus Low
X	H	Z	Receiver disabled
X	OPEN	Z	Receiver disabled by default
Open-circuit bus	L	H	Fail-safe high output
Short-circuit bus	L	H	Fail-safe high output

(1) H = high level; L = low level; Z = high impedance; X = irrelevant; ? = indeterminate

9.4.1 Low-Power Standby Mode

When both the driver and receiver are disabled (DE low and $\overline{RE}$ high) the device is in standby mode. If the enable inputs are in this state for less than 60 ns, the device does not enter standby mode. This guards against inadvertently entering standby mode during driver or receiver enabling. Only when the enable inputs are held in this state for 300 ns or more, the device is assured to be in standby mode. In this low-power standby mode, most internal circuitry is powered down, and the supply current is typically less than 1 µA. When either the driver or the receiver is re-enabled, the internal circuitry becomes active.

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10 Application and Implementation

Note

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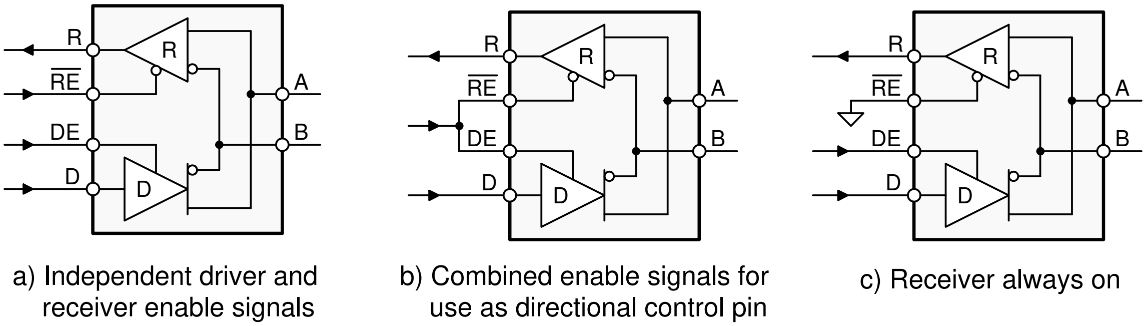
10.1 Application Information

The SN65HVD10, 'HVD11, and 'HVD12 are half-duplex RS-485 transceivers commonly used for asynchronous data transmissions. The driver and receiver enable pins allow the configuration of different operating modes.



a) Independent driver and receiver enable signals

b) Combined enable signals for use as directional control pin

c) Receiver always on

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図 10-1. Half-Duplex Transceiver Configurations

1. Using independent enable lines provides the most flexible control, as it allows the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows selective listening into the bus traffic, whether the driver is transmitting data or not.
2. Combining the enable signals simplify the interface to the controller, by forming a single direction-control signal. In this configuration, the transceiver operates as a driver when the direction-control line is high, and as a receiver when the direction-control line is low.
3. Only one line is required when connecting the receiver-enable input to ground and controlling only the driver-enable input. In this configuration, a node not only receives the data from the bus, but also the data it sends and can verify that the correct data have been transmitted.

10.2 Typical Application

An RS-485 bus consists of multiple transceivers connected in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor, R_T, whose value matches the characteristic impedance, Z_0, of the cable. This method, known as parallel termination, allows higher data rates over a longer cable length.

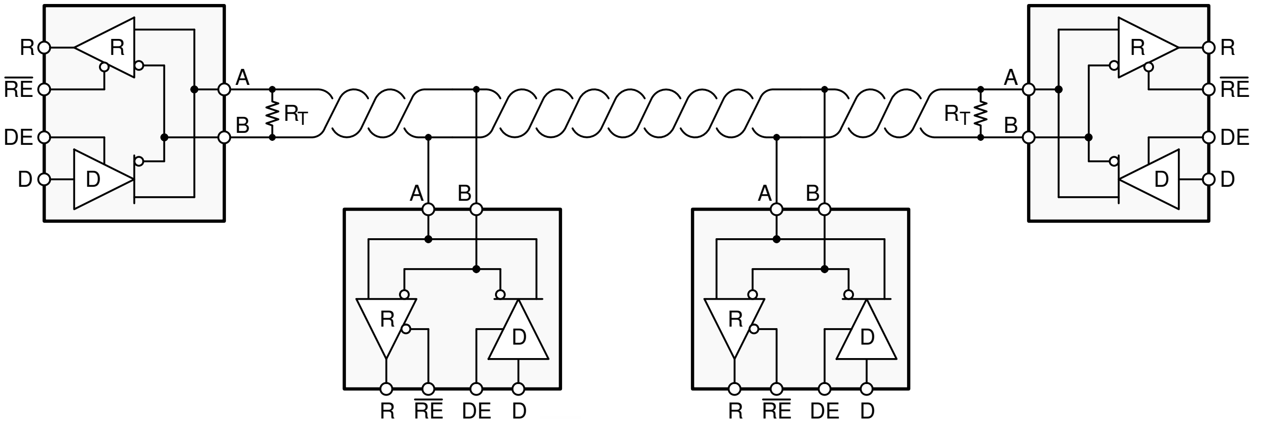

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図 10-2. Typical RS-485 Network With Half-Duplex Transceivers

10.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking, that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

10.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and bus length, meaning the higher the data rate, the shorter the cable length; and conversely, the lower the data rate, the longer the cable may be without introducing data errors. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing small signal jitter of up to 5 or 10%.

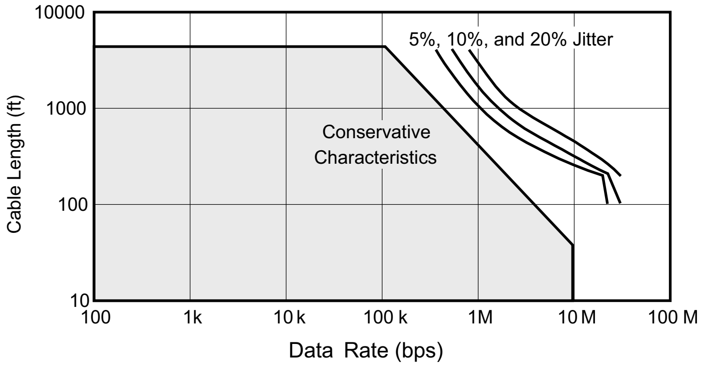

図 10-3. Cable Length vs Data Rate Characteristic

10.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a nonterminated piece of bus line, which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length or round-trip delay of a stub should be less than one-tenth of the rise time of the driver, therefore giving a maximum physical stub length as shown in 式 1.

$$L_{(STUB)} \leq 0.1 \times t_r \times v \times c \tag{1}$$

where

- t_r is the 10/90 rise time of the driver
- v is the signal velocity of the cable or trace as a factor of c
- c is the speed of light (3×10^8 m/s)

Per 式 1, 表 10-1 lists the maximum cable-stub lengths for the minimum-driver output rise-times of the SN65HVD1x full-duplex family of transceivers for a signal velocity of 78%.

表 10-1. Maximum Stub Length

DEVICE	MINIMUM DRIVER OUTPUT RISE TIME (ns)	MAXIMUM STUB LENGTH	
		(m)	(ft)
SN65HVD10	3	0.07	0.23
SN65HVD11	10	0.23	0.75
SN65HVD12	100	2.34	7.67

10.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. SN65HVD11 and HVD12 are both 1/8 UL transceivers, which means that up to 256 receivers can be connected to the bus. The SN65HVD10 is a 1/4 UL transceiver, and up to 64 receivers can be connected to the bus.

10.2.1.4 Receiver Fail-safe

The differential receivers of the SN65HVD1x family are fail-safe to invalid bus states caused by:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving.

In any of these cases, the differential receiver will output a fail-safe logic High state so that the output of the receiver is not indeterminate.

Receiver fail-safe is accomplished by offsetting the receiver thresholds, such that the input indeterminate range does not include zero volts differential. To comply with the RS-422 and RS-485 standards, the receiver output must output a High when the differential input V_{ID} is more positive than +200 mV, and must output a Low when V_{ID} is more negative than –200 mV. The receiver parameters which determine the fail-safe performance are $V_{IT(+)}$ and $V_{IT(-)}$. As shown in *セクション 7.6*, differential signals more negative than –200 mV will always cause a Low receiver output, and differential signals more positive than +200 mV will always cause a High receiver output.

When the differential input signal is close to zero, it is still above the maximum $V_{IT(+)}$ threshold of –10 mV, and the receiver output will be High.

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10.2.2 Detailed Design Procedure

To protect bus nodes against high-energy transients, the implementation of external transient protection devices is therefore necessary. 図 10-4 shows a protection circuit against 10-kV ESD (IEC 61000-4-2), 4-kV EFT (IEC 61000-4-4), and 1-kV surge (IEC 61000-4-5) transients.

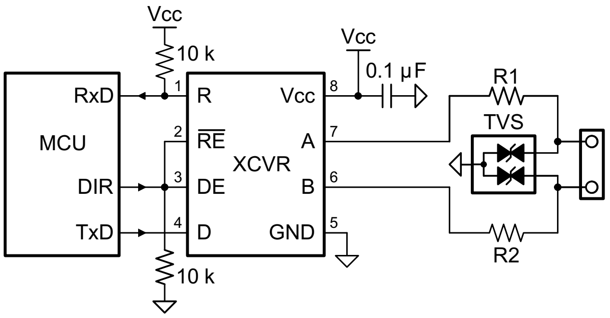

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図 10-4. Transient Protection Against ESD, EFT, and Surge Transients

表 10-2. Bill of Materials

DEVICE	FUNCTION	ORDER NUMBER	MANUFACTURER
XCVR	3.3-V, full-duplex RS-485 transceiver	SN65HVD1xD	TI
R1, R2	10-Ω, pulse-proof, thick-film resistor	CRCW0603010RJNEAHP	Vishay
TVS	Bidirectional 400-W transient suppressor	CDSOT23-SM712	Bourns

10.2.3 Application Curve

図 10-5 demonstrates operation of the SN65HVD12 at a signaling rate of 250 kbps. Two SN65HVD12 transceivers are used to transmit data through a 2,000 foot (600 m) segment of Commscope 5524 category 5e+ twisted pair cable. The bus is terminated at each end by a 100-Ω resistor, matching the cable characteristic impedance.

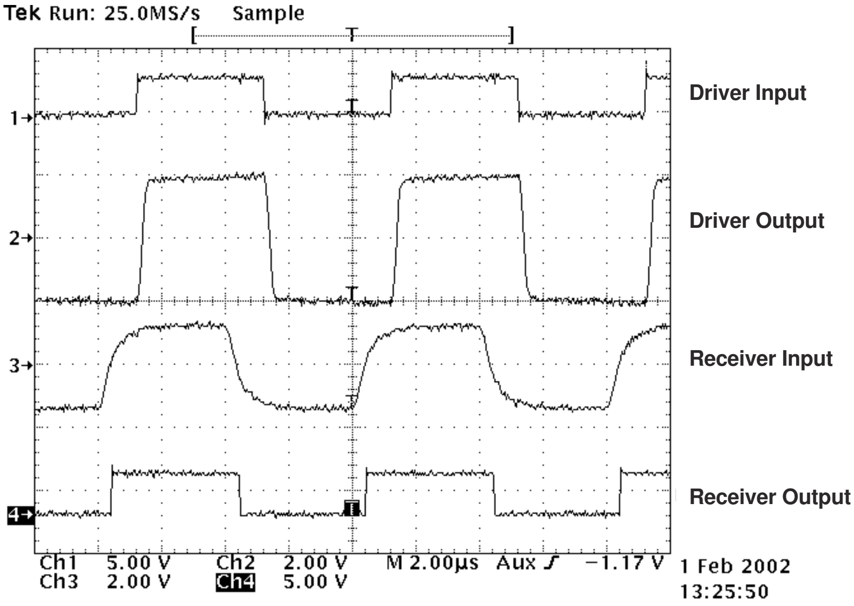

図 10-5. SN65HVD12 Input and Output Through 2000 Feet of Cable

11 Power Supply Recommendations

To assure reliable operation at all data rates and supply voltages, each supply must be buffered with a 100-nF ceramic capacitor located as close to the supply pins as possible. The TPS76333 linear voltage regulator is suitable for the 3.3-V supply.

12 Layout

12.1 Layout Guidelines

On-chip IEC-ESD protection is sufficient for laboratory and portable equipment, but never sufficient for EFT and surge transients occurring in industrial environments. Therefore, robust and reliable bus node design requires the use of external transient protection devices.

It is because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, that high-frequency layout techniques must be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from entering the board.
2. Use V_{CC} and ground planes to provide low-inductance. Note that high-frequency currents follow the path of least inductance and not the path of least impedance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF bypass capacitors as close as possible to the V_{CC} pins of transceiver, UART, and controller ICs on the board.
5. Use at least two vias for V_{CC} and ground connections of bypass capacitors and protection devices to minimize effective via-inductance.
6. Use 1-kΩ to 10-kΩ pull-up or pull-down resistors to enable lines to limit noise currents in these lines during transient events.
7. Insert pulse-proof series resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) which reduce the transients to a few hundred volts of clamping voltage, and transient blocking units (TBUs) that limit transient current to less than 1 mA.

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12.2 Layout Example

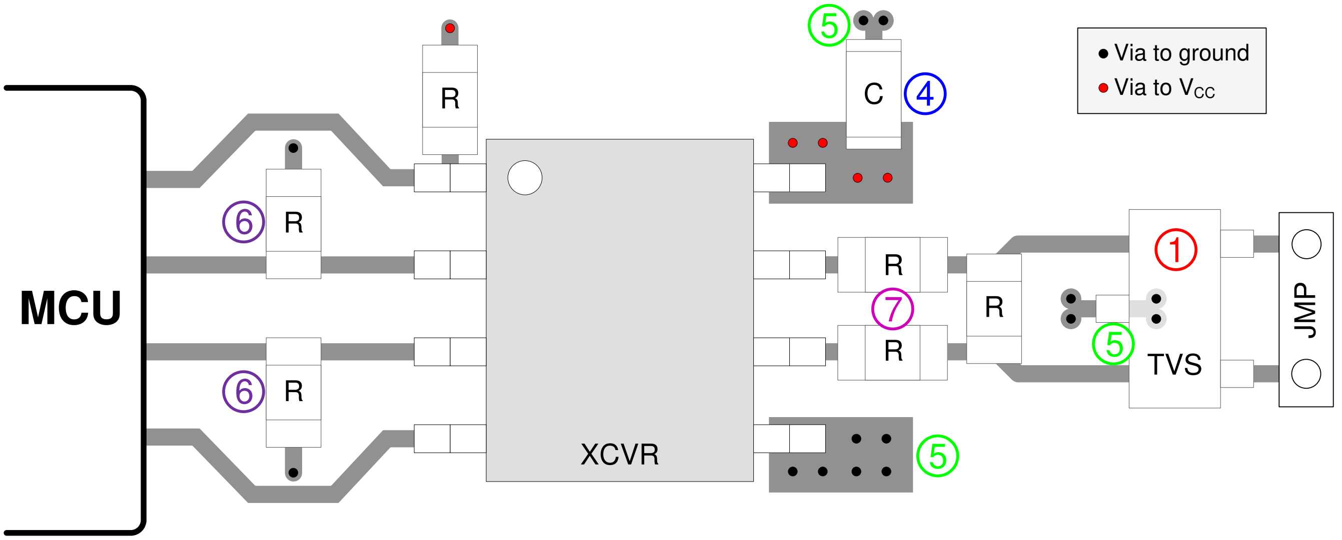

図 12-1. SN65HVD1x Layout Example

12.3 Thermal Considerations

12.3.1 Thermal Characteristics of IC Packages

$R_{\theta JA}$ (Junction-to-Ambient Thermal Resistance) is defined as the difference in junction temperature to ambient temperature divided by the operating power.

$R_{\theta JA}$ is not a constant and is a strong function of:

- the PCB design (50% variation)
- altitude (20% variation)
- device power (5% variation)

$R_{\theta JA}$ can be used to compare the thermal performance of packages when specific test conditions are defined and used. Standardized testing includes specification of PCB construction, test chamber volume, sensor locations, and the thermal characteristics of holding fixtures. $R_{\theta JA}$ is often misused when it is used to calculate junction temperatures for other installations.

TI uses two test PCBs as defined by JEDEC specifications. The low-k board gives average in-use condition thermal performance, and it consists of a single copper trace layer 25 mm long and 2-oz thick. The high-k board gives best case in-use condition, and it consists of two 1-oz buried power planes with a single copper trace layer 25 mm long and 2-oz thick. A 4% to 50% difference in $R_{\theta JA}$ can be measured between these two test cards.

$R_{\theta JC}$ (Junction-to-Case Thermal Resistance) is defined as the difference in junction temperature to case divided by the operating power. It is measured by putting the mounted package up against a copper block cold plate to force heat to flow from the die, through the mold compound into the copper block.

$R_{\theta JC}$ is a useful thermal characteristic when a heat sink is applied to package. It is not a useful characteristic to predict junction temperature, because it provides pessimistic numbers if the case temperature is measured in a nonstandard system and junction temperatures are backed out. It can be used with $R_{\theta JB}$ in 1-dimensional thermal simulation of a package system.

$R_{\theta JB}$ (Junction-to-Board Thermal Resistance) is defined as the difference in the junction temperature and the PCB temperature at the center of the package (closest to the die) when the PCB is clamped in a cold-plate structure. $R_{\theta JB}$ is only defined for the high-k test card.

$R_{\theta JB}$ provides an overall thermal resistance between the die and the PCB. It includes a bit of the PCB thermal resistance (especially for BGAs with thermal balls) and can be used for simple 1-dimensional network analysis of package system, see 図 12-2.

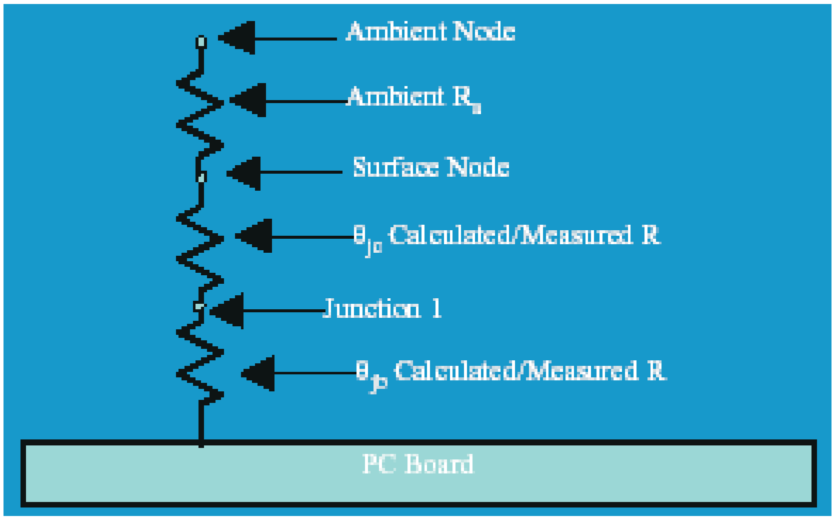

図 12-2. PCB Thermal Resistances

13 Device and Documentation Support

13.1 Device Support

13.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to order now.

表 13-1. Related Links

PARTS	PRODUCT FOLDER	ORDER NOW	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN65HVD10	Click here	Click here	Click here	Click here	Click here
SN65HVD11	Click here	Click here	Click here	Click here	Click here
SN65HVD12	Click here	Click here	Click here	Click here	Click here
SN75HVD10	Click here	Click here	Click here	Click here	Click here
SN75HVD11	Click here	Click here	Click here	Click here	Click here
SN75HVD12	Click here	Click here	Click here	Click here	Click here

13.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

13.4 サポート・リソース

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13.5 Trademarks

TI E2E™ is a trademark of Texas Instruments.
すべての商標は、それぞれの所有者に帰属します。

13.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

13.7 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65HVD10D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	VP10
SN65HVD10DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP10
SN65HVD10DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP10
SN65HVD10DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP10
SN65HVD10P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65HVD10
SN65HVD10P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65HVD10
SN65HVD10QD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	VP10Q
SN65HVD10QDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP10Q
SN65HVD10QDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP10Q
SN65HVD10QDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP10Q
SN65HVD10QDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP10Q
SN65HVD11D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	VP11
SN65HVD11DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP11
SN65HVD11DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP11
SN65HVD11DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP11
SN65HVD11P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65HVD11
SN65HVD11P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65HVD11
SN65HVD11QD	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 125	VP11Q
SN65HVD11QDR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP11Q
SN65HVD11QDR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP11Q
SN65HVD11QDRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP11Q
SN65HVD11QDRG4.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 125	VP11Q
SN65HVD12D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	VP12
SN65HVD12DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP12
SN65HVD12DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP12
SN65HVD12DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP12
SN65HVD12P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65HVD12
SN65HVD12P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-40 to 85	65HVD12
SN75HVD10D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	VN10

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN75HVD10DR	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	VN10
SN75HVD10P	Obsolete	Production	PDIP (P) | 8	-	-	Call TI	Call TI	0 to 70	75HVD10
SN75HVD11D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	VN11
SN75HVD12D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	VN12
SN75HVD12DR	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	VN12
SN75HVD12P	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	75HVD12
SN75HVD12P.A	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	75HVD12
SN75HVD12PE4	Active	Production	PDIP (P) | 8	50 | TUBE	Yes	NIPDAU	N/A for Pkg Type	0 to 70	75HVD12

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF SN65HVD10, SN65HVD11, SN65HVD12 :

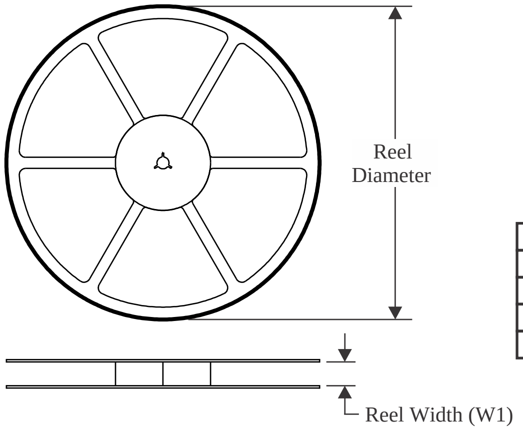
- Enhanced Product : SN65HVD10-EP, SN65HVD12-EP

NOTE: Qualified Version Definitions:

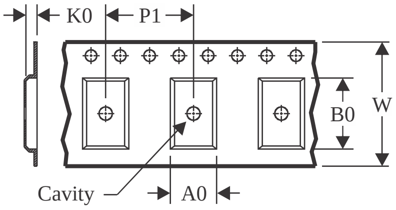
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

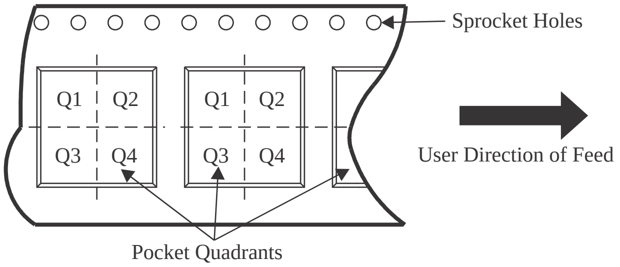


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

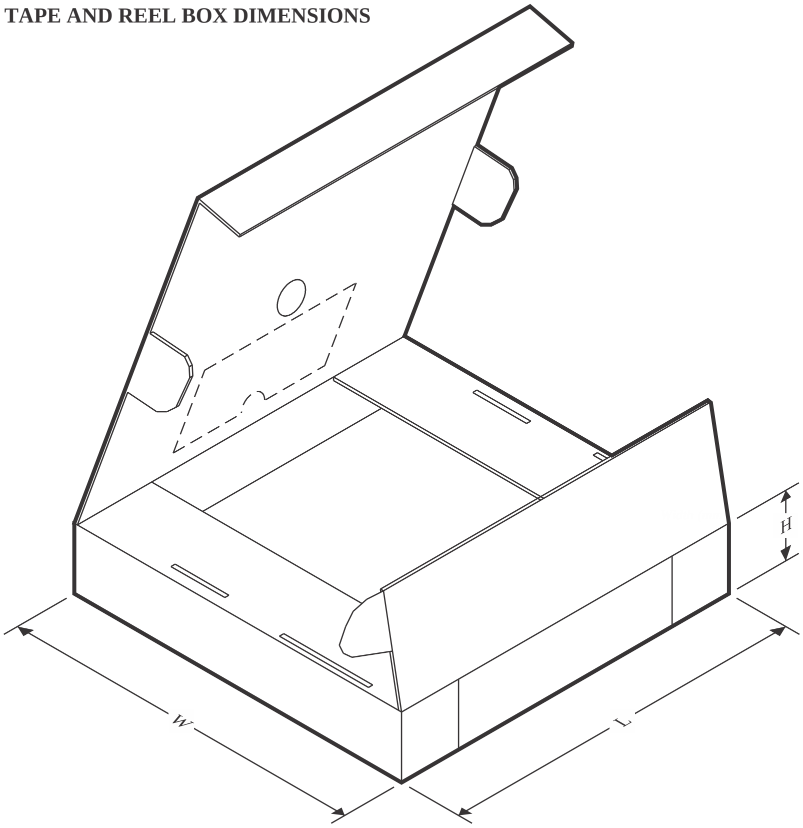
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD10DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD10DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD10QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD10QDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD11DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD11QDR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD11QDRG4	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
SN65HVD12DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

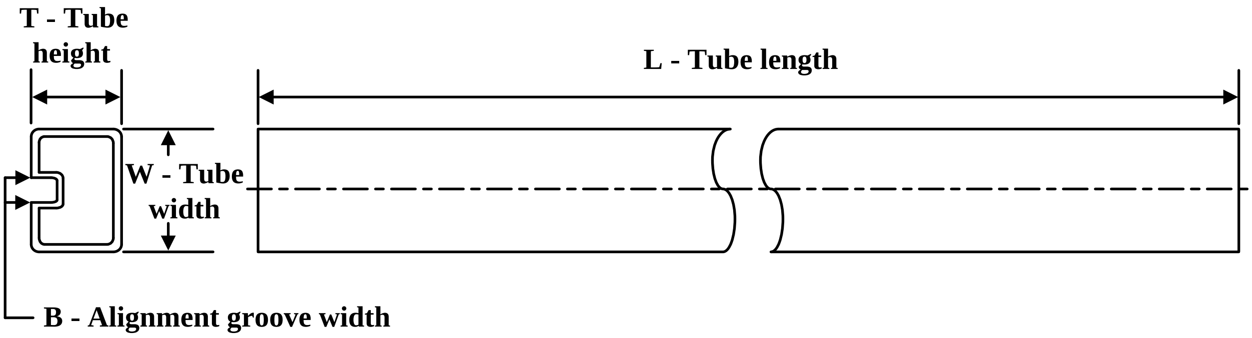
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

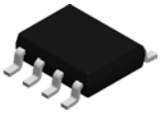
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD10DR	SOIC	D	8	2500	340.5	336.1	25.0
SN65HVD10DR	SOIC	D	8	2500	356.0	356.0	35.0
SN65HVD10QDR	SOIC	D	8	2500	356.0	356.0	35.0
SN65HVD10QDRG4	SOIC	D	8	2500	356.0	356.0	35.0
SN65HVD11DR	SOIC	D	8	2500	340.5	336.1	25.0
SN65HVD11QDR	SOIC	D	8	2500	356.0	356.0	35.0
SN65HVD11QDRG4	SOIC	D	8	2500	356.0	356.0	35.0
SN65HVD12DR	SOIC	D	8	2500	340.5	336.1	25.0

TUBE



*All dimensions are nominal

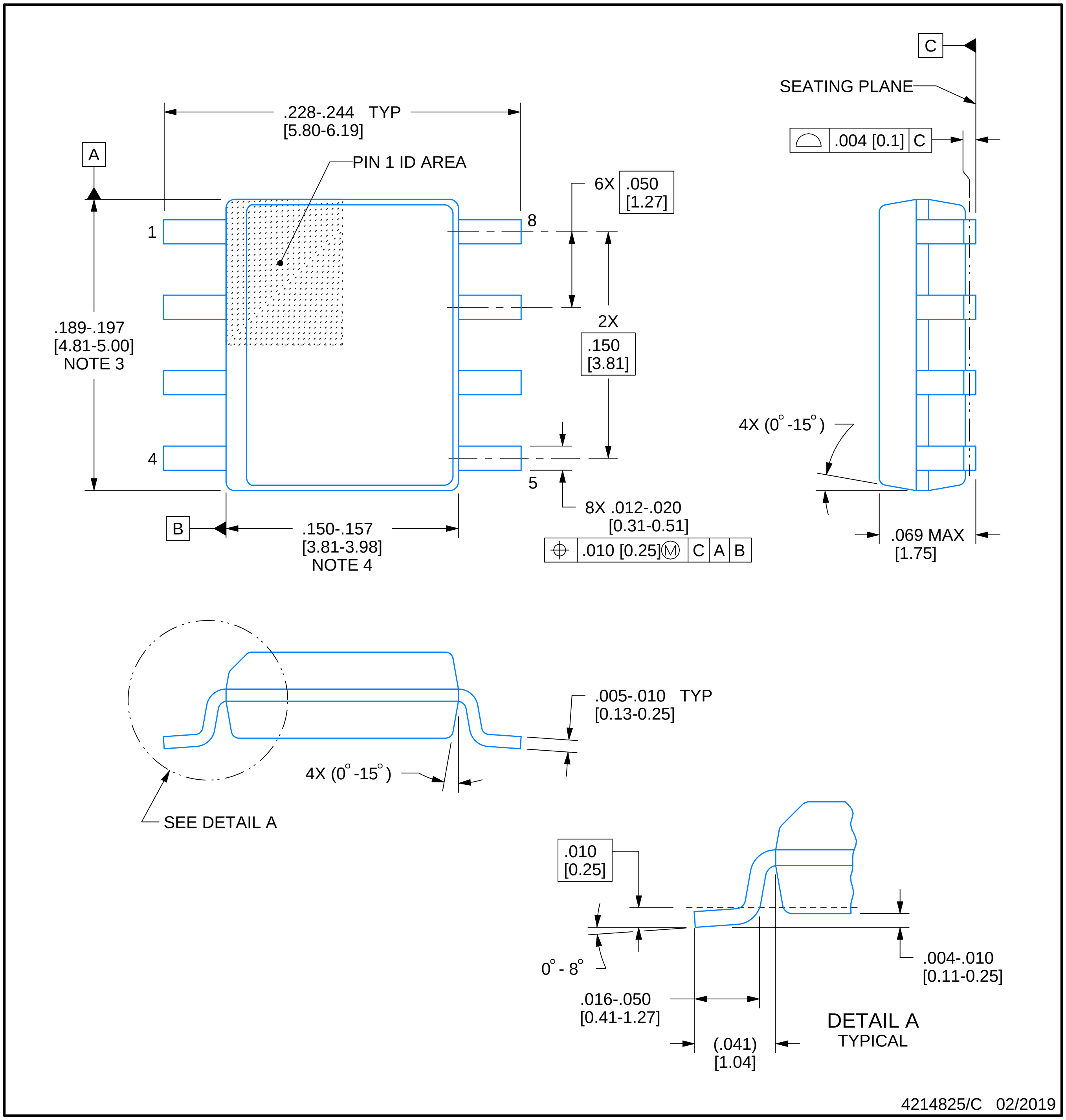
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
SN65HVD10P	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD10P.A	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD11P	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD11P.A	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD12P	P	PDIP	8	50	506	13.97	11230	4.32
SN65HVD12P.A	P	PDIP	8	50	506	13.97	11230	4.32
SN75HVD12P	P	PDIP	8	50	506	13.97	11230	4.32
SN75HVD12P.A	P	PDIP	8	50	506	13.97	11230	4.32
SN75HVD12PE4	P	PDIP	8	50	506	13.97	11230	4.32



PACKAGE OUTLINE

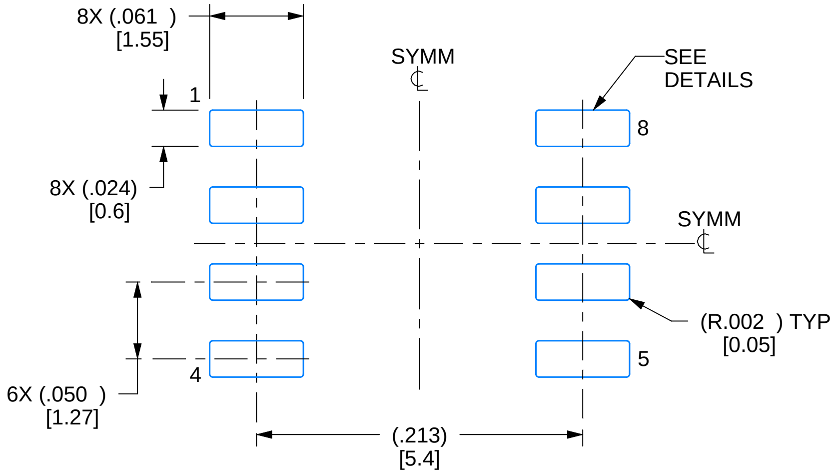
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

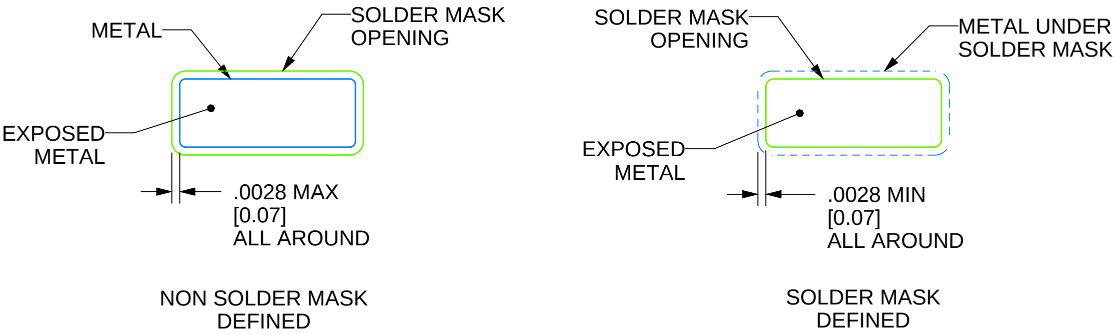


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

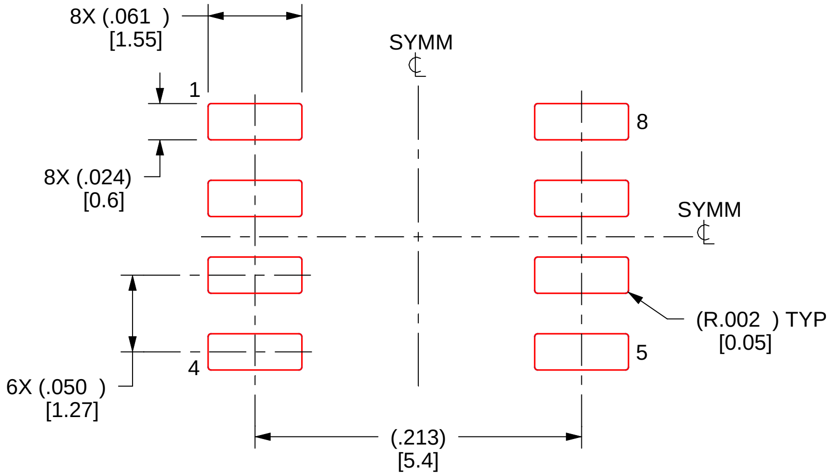


SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

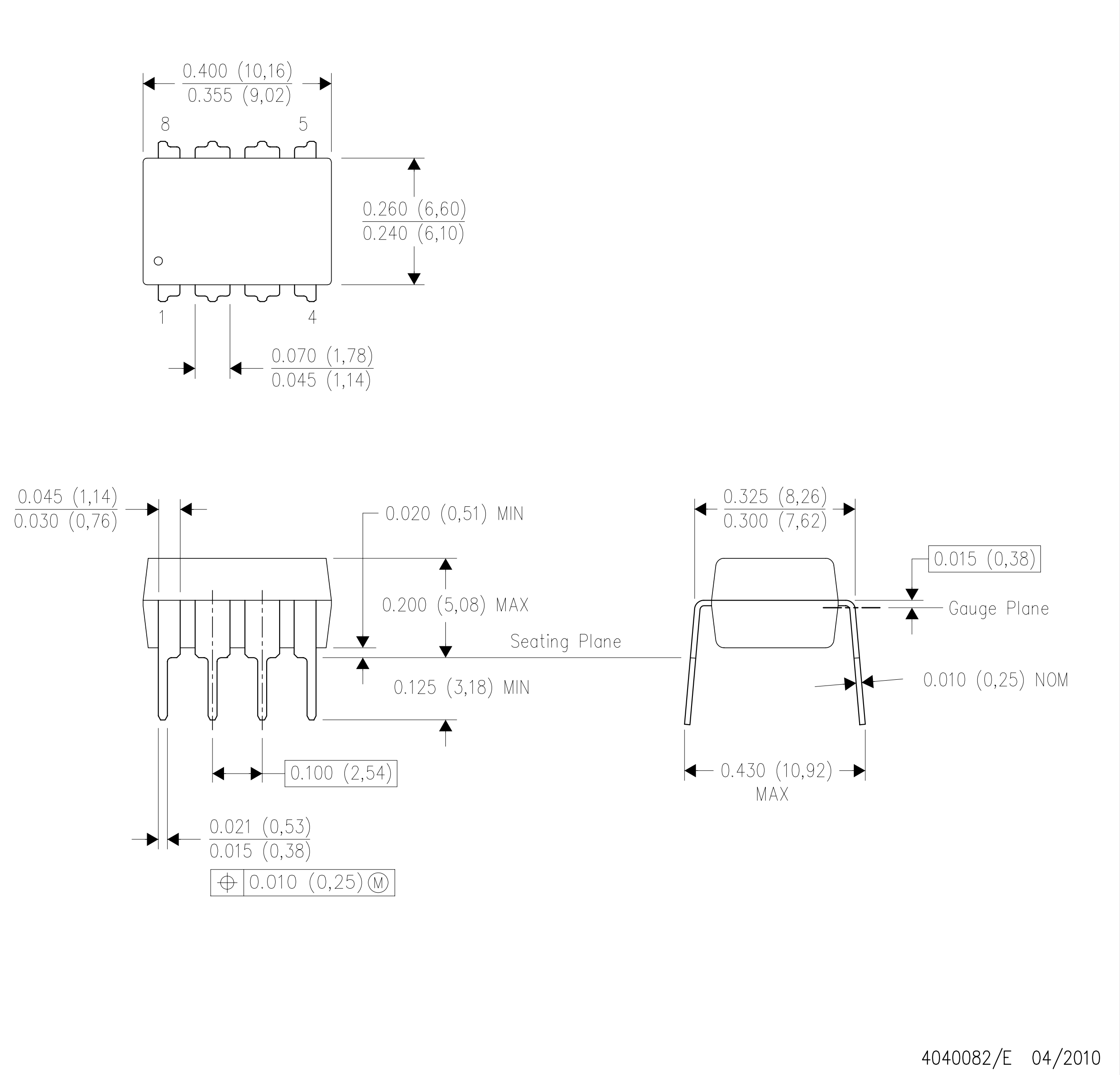


SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

P (R-PDIP-T8) PLASTIC DUAL-IN-LINE PACKAGE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS-001 variation BA.

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