TEXAS INSTRUMENTS
CD54HC165, CD74HC165, CD54HCT165, CD74HCT165
JAJSNE8D – FEBRUARY 1998 – REVISED NOVEMBER 2021

CDx4HC165/CDx4HCT165 ハイスピード CMOS ロジック、8 ビット、パラレル入力、シリアル出力、シフト・レジスタ

1 特長

- バッファ付き入力
- 非同期パラレル・ロード
- 相補出力
- ファンアウト (全温度範囲にわたって)
  - 標準出力:10 の LSTTL 負荷
  - バス・ドライバ出力:15 の LSTTL 負荷
- 広い動作温度範囲:-55℃～125℃
- 平衡な伝搬遅延と遷移時間
- LSTTL ロジック IC に比べて消費電力を大幅削減
- HC タイプ
  - 2V～6V で動作
  - 優れたノイズ耐性:N_{IL} = V_{CC} の 30%、N_{IH} = V_{CC} の 30% (V_{CC} = 5V の場合)
- HCT タイプ
  - 4.5V～5.5V で動作
  - LSTTL 入力ロジックと直接互換、V_{IL} = 0.8V (最大値)、V_{IH} = 2V (最小値)
  - CMOS 入力互換、V_{OL}、V_{OH} で I_I ≤ 1μA

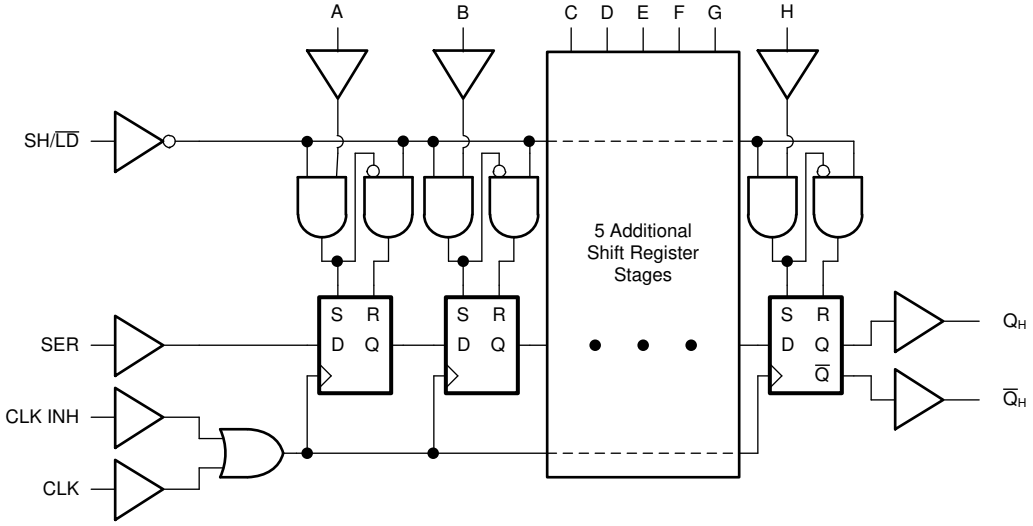
2 概要

'HC165 と 'HCT165 は、最終段から利用できる相補シリアル出力 (Q_H と $\overline{Q}_H$) を備えた 8 ビット・パラレルまたはシリアル入力シフト・レジスタです。パラレル・ロード (SH/$\overline{LD}$) 入力が LOW の場合、A～H 入力のパラレル・データは非同期的にレジスタにロードされます。SH/$\overline{LD}$ が HIGH の場合、データは順次に SER 入力からレジスタに入り、クロックの立ち上がり遷移ごとに 1 つづつ右の位置 (A→B→C など) にシフトされます。この機能を使うと、Q_H 出力を後続デバイスの SER 入力に接続することでパラレル入力シリアル出力コンバータを拡張できます。

製品情報

部品番号	パッケージ(1)	本体サイズ (公称)
CD54HC165F3A	CDIP (16)	24.38mm × 6.92mm
CD74HC165M	SOIC (16)	9.90mm × 3.90mm
CD74HC165E	PDIP (16)	19.31mm × 6.35mm
CD54HCT165F3A	CDIP (16)	24.38mm × 6.92mm
CD74HCT165M	SOIC (16)	9.90mm × 3.90mm
CD74HCT165E	PDIP (16)	19.31mm × 6.35mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。



機能ダイアグラム

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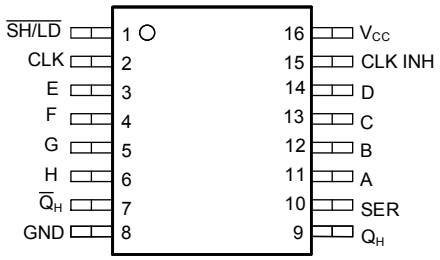
3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (October 2003) to Revision D (November 2021)	Page
• 最新のデータシート規格を反映するように、文書全体の表、図、相互参照の採番と書式設定を更新	1
• 現行の TI の命名規則に合わせてピン名を以下のように更新。$\overline{PL}$ を SH/$\overline{LD}$、CP を CLK、D4 を E、D5 を F、D6 を G、D7 を H、$\overline{Q}_7$ を $\overline{Q}_H$、Q_7 を Q_H、DS を SER、D0 を A、D1 を B、D2 を C、D3 を D、$\overline{CE}$ を CLK INH。	1

4 Pin Configuration and Functions



J, N, or D package
16-Pin CDIP, PDIP, SOIC
Top View

5 Specifications

5.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

			MIN	MAX	UNIT
V_{CC}	Supply voltage		–0.5	7	V
I_{IK}	Input diode current	For V_I < -0.5 V or V_I > V_{CC} + 0.5 V		±20	mA
I_{OK}	Output diode current	For V_O < -0.5 V or V_O > V_{CC} + 0.5 V		±20	mA
IO	Drain current per output	For V_O < -0.5 V V_O > V_{CC} + 0.5 V		±25	mA
I_O	Output source or sink current per output pin	For V_O > -0.5 V or V_O < V_{CC} + 0.5 V		±25	mA
	Continuous current through V_{CC} or GND			±50	mA
T_J	Junction temperature			150	°C
T_{stg}	Storage temperature		-65	150	°C
	Lead temperature (Soldering 10s) (SOIC- Lead tips only)			300	°C

(1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Reccomended Operating Conditions

			MIN	MAX	UNIT
V_{CC}	Supply voltage range	HC Types	2	6	V
		HCT Types	4.5	5.5	
V_I, V_O	Input or output voltage		0	V_{CC}	V
t_t	Input rise and fall time	2 V		1000	ns
		4.5 V		500	
		6 V		400	
T_A	Temperature range		–55	125	℃

5.3 Thermal Information

THERMAL METRIC		CD74HC165, CD74HCT165		UNIT
		D (SOIC)	N (PDIP)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(1)	73	67	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.

5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS(2)	V_{CC} (V)	25℃			-40℃ to 85℃		-55℃ to 125℃		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V_{IH}	High level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		V
			6	4.2			4.2		4.2		V
V_{IL}	Low level input voltage		2			0.5		0.5		0.5	V
			4.5			1.35		1.35		1.35	V
			6			1.8		1.8		1.8	V
V_{OH}	High level output voltage	I_{OH} = – 20 μA	2	1.9			1.9		1.9		V
		I_{OH} = – 20 μA	4.5	4.4			4.4		4.4		V
		I_{OH} = – 20 μA	6	5.9			5.9		5.9		V
	High level output voltage	I_{OH} = – 4 mA	4.5	3.98			3.84		3.7		V
		I_{OH} = – 5.2 mA	6	5.48			5.34		5.2		V
V_{OL}	Low level output voltage	I_{OL} = 20 μA	2			0.1		0.1		0.1	V
		I_{OL} = 20 μA	4.5			0.1		0.1		0.1	V
		I_{OL} = 20 μA	6			0.1		0.1		0.1	V
	Low level output voltage	I_{OL} = 4 mA	4.5			0.26		0.33		0.4	V
		I_{OL} = 5.2 mA	6			0.26		0.33		0.4	V
I_I	Input leakage current	V_I = V_{CC} or GND	6			±0.1		±1		±1	μA
I_{CC}	Supply current	V_I = V_{CC} or GND	6			8		80		160	μA
HCT TYPES											
V_{IH}	High level input voltage		4.5 to 5.5	2			2		2		V
V_{IL}	Low level input voltage		4.5 to 5.5			0.8		0.8		0.8	V
V_{OH}	High level output voltage	I_{OH} = – 20 μA	4.5	4.4			4.4		4.4		V
	High level output voltage	I_{OH} = – 4 mA	4.5	3.98			3.84		3.7		V
V_{OL}	Low level output voltage	I_{OL} = 20 μA	4.5			0.1		0.1		0.1	V
	Low level output voltage	I_{OL} = 4 mA	4.5			0.26		0.33		0.4	V
I_I	Input leakage current	V_I = V_{CC} or GND	5.5			±0.1		±1		±1	μA
I_{CC}	Supply current	V_I = V_{CC} or GND	5.5			8		80		160	μA
ΔI_{CC} (1)	Additional quiescent device current per input pin	SER, A to H inputs held at V_{CC} – 2.1	4.5 to 5.5		100	126		157.5		171.5	μA
		CLK and SH/$\overline{LD}$ inputs held at V_{CC} – 2.1	4.5 to 5.5		100	234		292.5		318.5	

(1) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.
(2) V_I = V_{IH} or V_{IL}.

5.5 Prerequisite for Switching Characteristics

PARAMETER		V_{CC} (V)	25℃		-40℃ to 85℃		-55℃ to 125℃		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_{WL}, t_{WH}	CLK Pulse Width	2	80		100		120		ns
		4.5	16		20		24		
		6	14		17		20		
t_{WL}	SH/$\overline{LD}$ Pulse Width	2	80		100		120		ns
		4.5	16		20		24		
		6	14		17		20		
t_{SU}	Set-up Time SER to CLK	2	80		100		120		ns
		4.5	16		20		24		
		6	14		17		20		
$t_{SU(L)}$	CLK INH to CLK	2	80		100		120		ns
		4.5	16		20		24		
		6	14		17		20		
t_{SU}	A-H to SH/$\overline{LD}$	2	80		100		120		ns
		4.5	16		20		24		
		6	14		17		20		
t_H	Hold Time SER to CLK or CLK INH	2	35		45		55		ns
		4.5	7		9		11		
		6	6		8		9		
t_H	CLK INH to CLK	2	0		0		0		ns
		4.5	0		0		0		
		6	0		0		0		
t_{REC}	Recovery Time SH/$\overline{LD}$ to CLK	2	100		125		150		ns
		4.5	20		25		30		
		6	17		21		26		
f_{MAX}	Maximum Clock Pulse Frequency	2	6		5		4		MHz
		4.5	30		24		20		
		6	35		28		24		
HCT TYPES									
t_{WL}, t_{WH}	CLK Pulse Width	4.5	18		23		27		ns
t_{WL}	SH/$\overline{LD}$ Pulse Width	4.5	20		25		30		ns
t_{SU}	Set-up Time SER to CLK	4.5	20		25		30		ns
$t_{SU(L)}$	CLK INH to CLK	4.5	20		25		30		ns
t_{SU}	A-H to SH/$\overline{LD}$	6	20		25		30		ns
t_H	Hold Time SER to CLK or CLK INH	4.5	7		9		11		ns
t_S, t_H	CLK INH to CLK	4.5	0		0		0		ns
t_{REC}	Recovery Time SH/$\overline{LD}$ to CLK	4.5	20		25		30		ns
f_{MAX}	Maximum Clock Pulse Frequency	4.5	27		22		18		MHz

5.6 Switching Characteristics

Input t_r, t_f = 6 ns. Unless otherwise specified, C_L = 50pF

PARAMETER		V_{CC}(V)	25℃		-40℃ to 85℃	-55℃ to 125℃	UNIT
			TYP	MAX	MAX	MAX	
HC TYPES							
t_{pd}	CLK or CLK INH to Q_H or $\overline{Q}_H$	2		165	205	250	ns
		4.5	13(3)	33	41	50	ns
		6		28	35	43	ns
	SH/$\overline{LD}$ to Q_H or $\overline{Q}_H$	2		175	220	265	ns
		4.5	14(3)	35	44	53	ns
		6		30	37	45	ns
	H to Q_H or $\overline{Q}_H$	2		150	190	225	ns
		4.5	12(3)	30	38	45	ns
		6		26	33	38	ns
t_t	Output Transition Times	2		75	95	110	ns
		4.5		15	19	22	ns
		6		13	16	19	ns
C_{IN}	Input Capacitance			10	10	10	pF
C_{PD}	Power Dissipation Capacitance(1) (2)	5	17				pF
HCT TYPES							
t_{pd}	CLK or CLK INH to Q_H or $\overline{Q}_H$	4.5	17(3)	40	50	60	ns
	SH/$\overline{LD}$ to Q_H or $\overline{Q}_H$	4.5	17(3)	40	50	60	ns
	H to Q_H or $\overline{Q}_H$	4.5	14(3)	35	44	53	ns
t_t	Output Transition Times	4.5		15	19	22	ns
C_{IN}	Input Capacitance			10	10	10	pF
C_{PD}	Power Dissipation Capacitance(1) (2)	5	24				pF

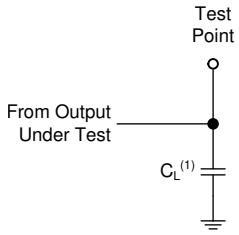
(1) C_{PD} is used to determine the dynamic power consumption, per package.
(2) $P_D = V_{CC}{}^2 f_i + \Sigma (C_L V_{CC}{}^2 + f_O)$ where f_i = Input Frequency, f_O = Output Frequency, C_L = Output Load Capacitance, V_{CC} = Supply Voltage.
(3) C_L = 15 pF and V_{CC} = 5 V.

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, Z_O = 50 Ω, t_t < 6 ns.

For clock inputs, f_{max} is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



(1) C_L includes probe and test-fixture capacitance.

図 6-1. Load Circuit for Push-Pull Outputs

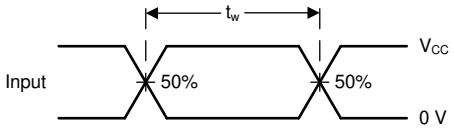


図 6-2. Voltage Waveforms, Standard CMOS Inputs Pulse Duration

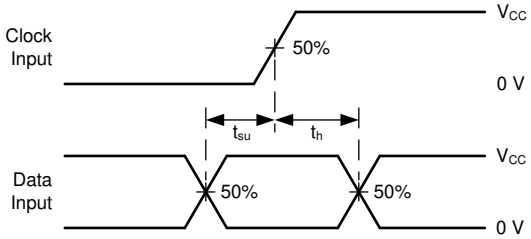
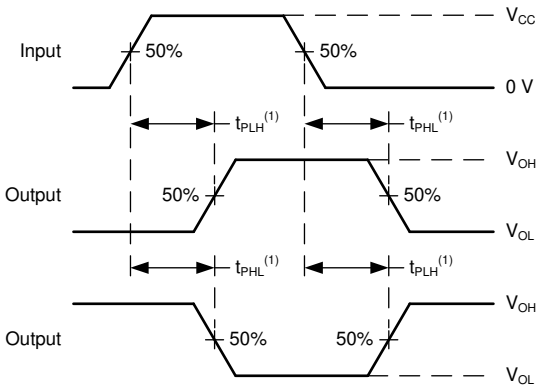
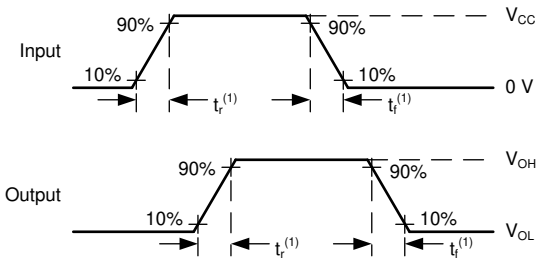


図 6-3. Voltage Waveforms, Standard CMOS Inputs Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

図 6-4. Voltage Waveforms, Standard CMOS Inputs Setup Propagation Delays



(1) The greater between t_r and t_f is the same as t_t.

図 6-5. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Input Devices

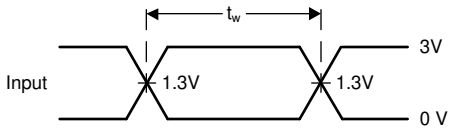


図 6-6. Voltage Waveforms, TTL-Compatible CMOS Inputs Pulse Duration

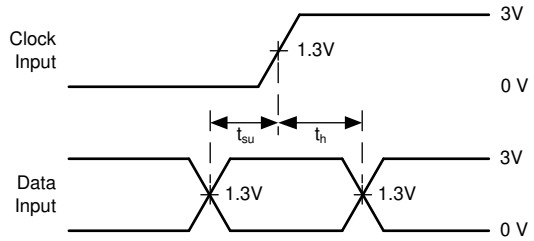
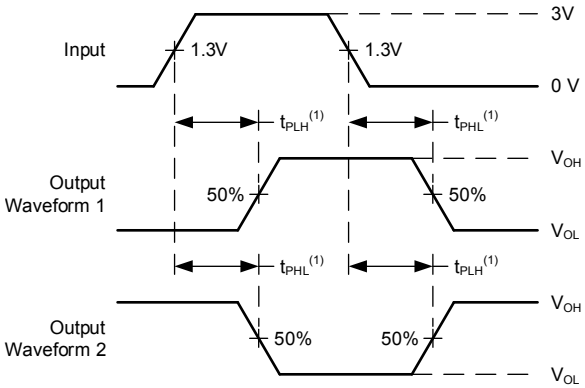


図 6-7. Voltage Waveforms, TTL-Compatible CMOS Inputs Setup and Hold Times



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd}.

図 6-8. Voltage Waveforms, TTL-Compatible CMOS Inputs Propagation Delays

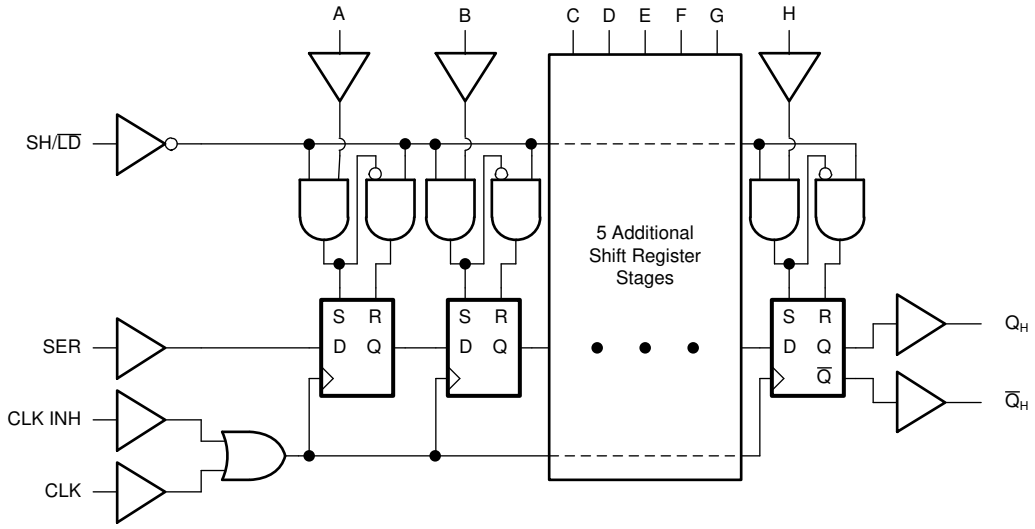
7 Detailed Description

7.1 Overview

The ’HC165 and ’HCT165 are 8-bit parallel or serial-in shift registers with complementary serial outputs (Q_H and $\overline{Q}_H$) available from the last stage. When the parallel load (SH/$\overline{LD}$) input is LOW, parallel data from the A to H inputs are loaded into the register asynchronously. When the SH/$\overline{LD}$ is HIGH, data enters the register serially at the SER input and shifts one place to the right (A→B→C, etc.) with each positive-going clock transition. This feature allows parallel-to-serial converter expansion by connecting the Q_H output to the SER input of the succeeding device.

For predictable operation the LOW-to-HIGH transition of CLK INH should only take place while CLK is HIGH. Also, CLK and CLK INH should be LOW before the LOW-to-HIGH transition of SH/$\overline{LD}$ to prevent shifting the data when SH/$\overline{LD}$ goes HIGH.

7.2 Functional Block Diagram



7.3 Device Functional Modes

表 7-1. Truth Table(1)

OPERATING MODE	INPUTS					QnREGISTER		OUTPUTS	
	SH$\overline{LD}$	CLK INH	CLK	SER	A - H	Q_A	Q_B - Q_G	Q_H	$\overline{Q}_H$
Parallel Load	L	X	X	X	L	L	L-L	L	H
	L	X	X	X	H	H	H-H	H	L
Serial Shift	H	L	↑	l	X	L	q_A - q_F	q_G	$\overline{q}_G$
	H	L	↑	h	X	H	q_A - q_F	q_G	$\overline{q}_G$
Hold (Do Nothing)	H	H	X	X	X	q_A	q_B - q_G	q_H	$\overline{q}_H$

(1) H = High voltage level.
h = High voltage level one set-up time prior to the low-to-high clock transition.
l = Low voltage level one set-up time prior to the low-to-high clock transition.
L = Low voltage level.
X = Don’t care.
↑ = Transition from low to high level.
q_n = Lower case letters indicate the state of the reference output clock transition.

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1-µF capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1-µF and 1-µF capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC}, whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 サポート・リソース

TI E2E™ サポート・フォーラムは、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計で必要な支援を迅速に得ることができます。

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10.3 Trademarks

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10.4 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

TI Glossary	This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
5962-8685501EA	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8685501EA CD54HCT165F3A
CD54HC165F3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	8409501EA CD54HC165F3A
CD54HCT165F3A	Active	Production	CDIP (J) | 16	25 | TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	5962-8685501EA CD54HCT165F3A
CD74HC165E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC165E
CD74HC165M	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC165M
CD74HC165M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU | SN | NIPDAU	Level-1-260C-UNLIM	-55 to 125	(CD4051BM, HC165M)
CD74HC165MT	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HC165M
CD74HCT165E	Active	Production	PDIP (N) | 16	25 | TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT165E
CD74HCT165M	Obsolete	Production	SOIC (D) | 16	-	-	Call TI	Call TI	-55 to 125	HCT165M
CD74HCT165M96	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU | SN	Level-1-260C-UNLIM	-55 to 125	HCT165M
CD74HCT165M96G4	Active	Production	SOIC (D) | 16	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT165M

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

OTHER QUALIFIED VERSIONS OF CD54HC165, CD54HCT165, CD74HC165, CD74HCT165 :

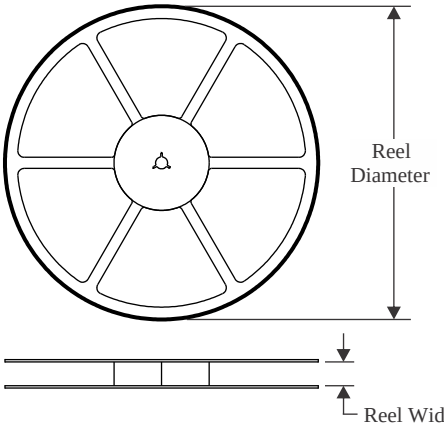
- Catalog : CD74HC165, CD74HCT165
- Military : CD54HC165, CD54HCT165

NOTE: Qualified Version Definitions:

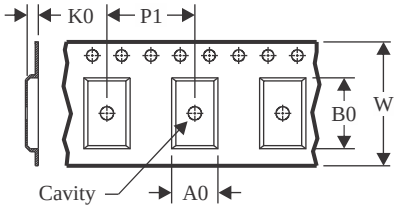
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

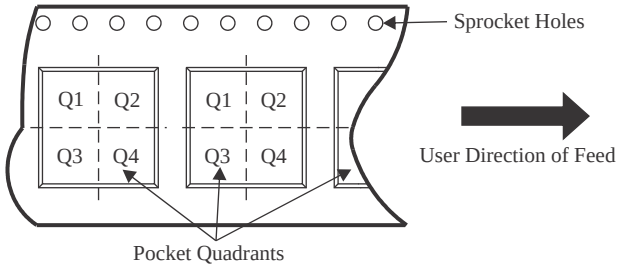


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

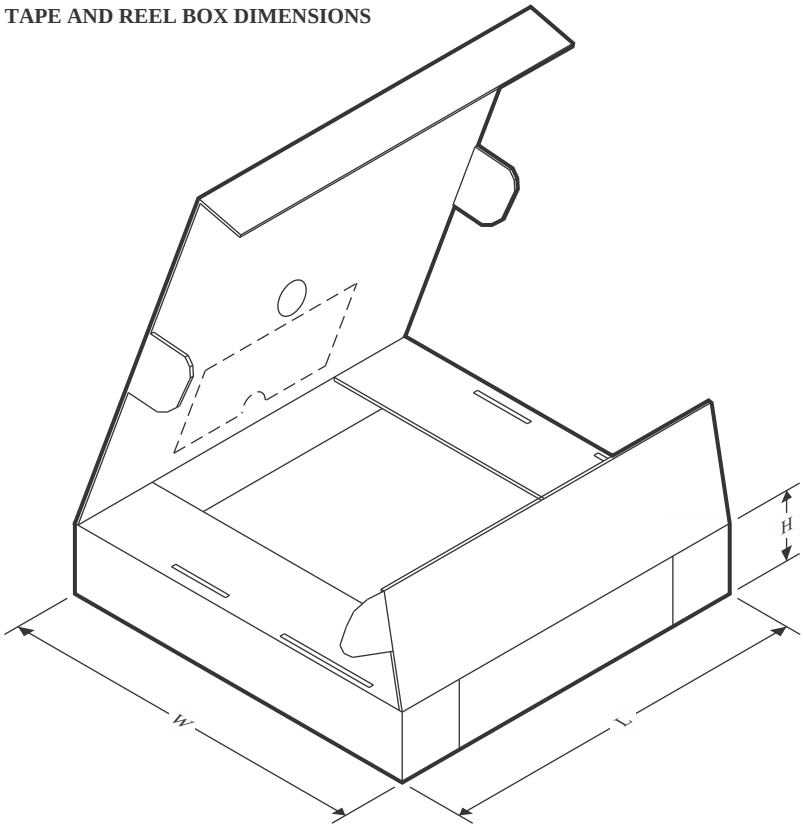
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC165M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HC165M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT165M96	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
CD74HCT165M96G4	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1

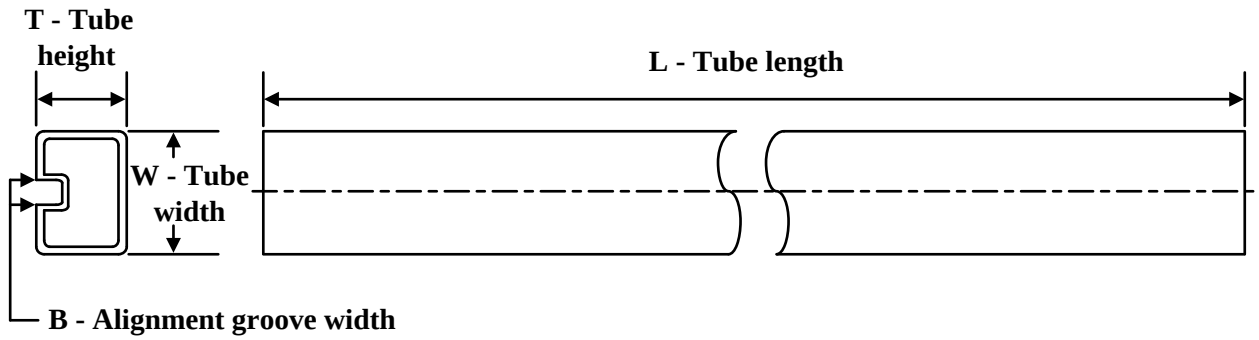
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC165M96	SOIC	D	16	2500	356.0	356.0	35.0
CD74HC165M96	SOIC	D	16	2500	356.0	356.0	35.0
CD74HCT165M96	SOIC	D	16	2500	356.0	356.0	35.0
CD74HCT165M96G4	SOIC	D	16	2500	353.0	353.0	32.0

TUBE



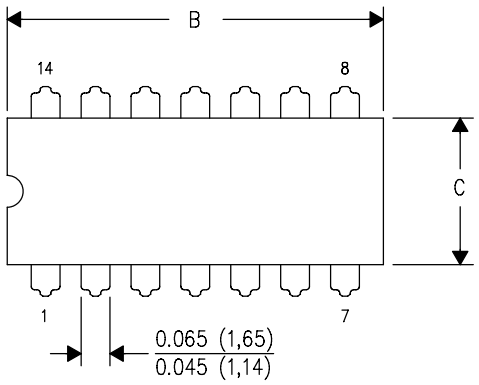
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (µm)	B (mm)
CD74HC165E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HC165E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT165E	N	PDIP	16	25	506	13.97	11230	4.32
CD74HCT165E	N	PDIP	16	25	506	13.97	11230	4.32

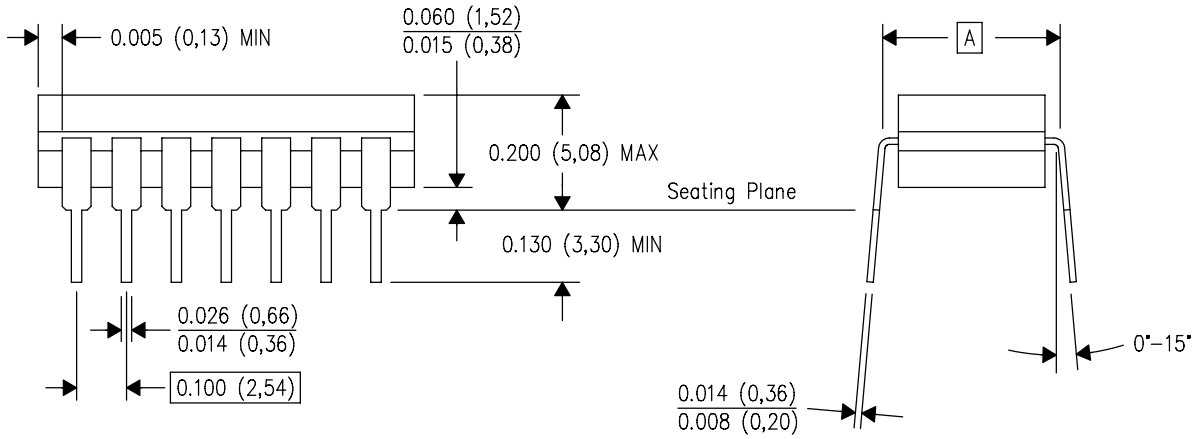
J (R–GDIP–T**)

14 LEADS SHOWN

CERAMIC DUAL IN–LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



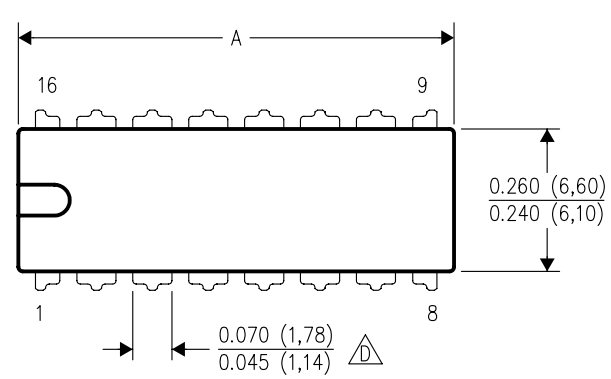
4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

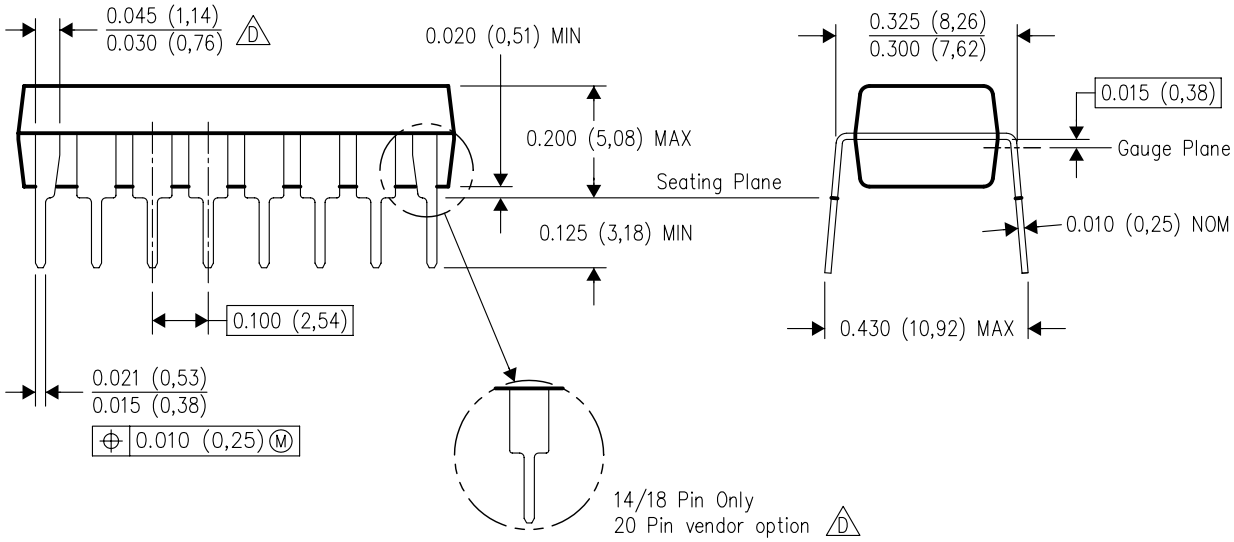
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



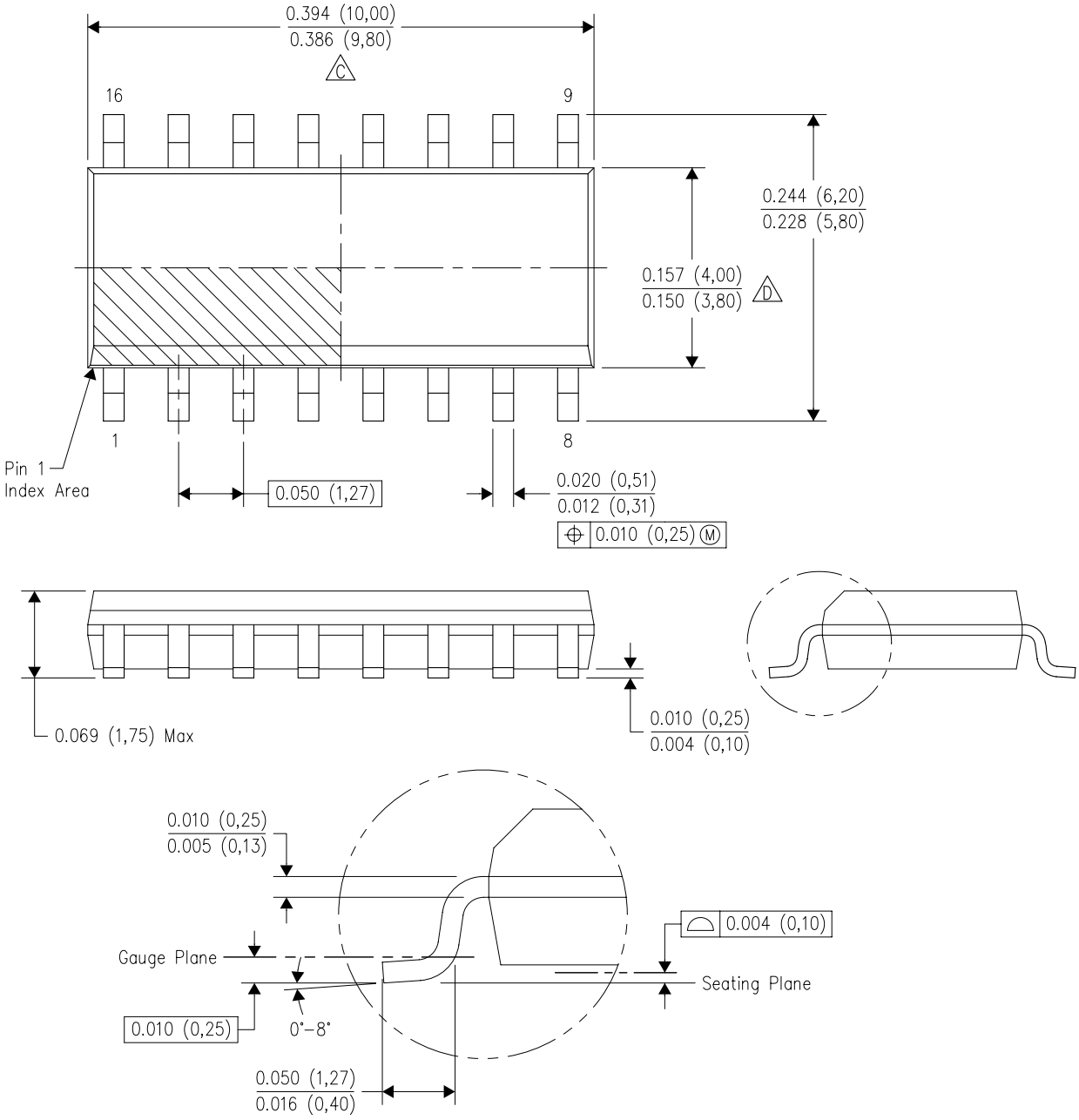
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

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