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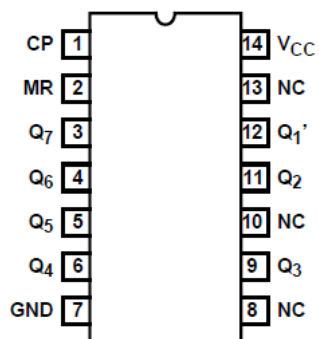
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3 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision C (October 2003) to Revision D (March 2022)	Page
• 最新のデータシート規格を反映するように、文書全体の採番、書式設定、表、図、相互参照を更新.....	1

4 Pin Configuration and Functions



J, N, D or PW Package
14-Pin CDIP, PDIP, SOIC, or TSSOP
Top View

5 Specifications

5.1 Absolute Maximum Ratings⁽¹⁾

			MIN	MAX	UNIT
V _{CC}	Supply voltage		– 0.5	7	V
I _{IK}	Input diode current	For V _I < –0.5 V or V _I > V _{CC} + 0.5 V		±20	mA
I _{OK}	Output diode current	For V _O < –0.5 V or V _O > V _{CC} + 0.5 V		±20	mA
I _O	Output source or sink current per output pin	For V _O > –0.5 V or V _O < V _{CC} + 0.5 V		±25	mA
	Continuous current through V _{CC} or GND			±50	mA
T _J	Junction temperature			150	°C
T _{stg}	Storage temperature range		– 65	150	°C
	Lead temperature (soldering 10s) (SOIC - lead tips only)			300	°C

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

5.2 Recommended Operating Conditions

			MIN	MAX	UNIT
V _{CC}	Supply voltage range	HC Types	2	6	V
		HCT Types	4.5	5.5	V
V _I , V _O	DC input or output voltage		0	V _{CC}	V
t _t	Input rise and fall time	2 V		1000	ns
		4.5 V		500	
		6 V		400	
T _A	Temperature range		– 55	125	°C

5.3 Thermal Information

THERMAL METRIC		D (SOIC)	N (PDIP)	PW (TSSOP)	UNIT
		14 PINS	14 PINS	14 PINS	
R _{θJA}	Junction-to-ambient thermal resistance ⁽¹⁾	86	80	113	°C/W

- (1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics](#) application report.

5.4 Electrical Characteristics

PARAMETER		TEST CONDITIONS ⁽²⁾	V _{CC} (V)	25°C			–40°C to 85°C		–55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
V _{IH}	High level input voltage		2	1.5			1.5		1.5		V
			4.5	3.15			3.15		3.15		
			6	4.2			4.2		4.2		
V _{IL}	Low level input voltage		2	0.5			0.5		0.5		V
			4.5	1.35			1.35		1.35		
			6	1.8			1.8		1.8		
V _{OH}	High level output voltage CMOS loads	I _{OH} = – 20 µA	2	1.9			1.9		1.9		V
		I _{OH} = – 20 µA	4.5	4.4			4.4		4.4		
		I _{OH} = – 20 µA	6	5.9			5.9		5.9		
	High level output voltage TTL loads	I _{OH} = – 4 mA	4.5	3.98			3.84		3.7		
		I _{OH} = – 5.2 mA	6	5.48			5.34		5.2		
V _{OL}	Low level output voltage CMOS loads	I _{OL} = 20 µA	2	0.1			0.1		0.1		V
		I _{OL} = 20 µA	4.5	0.1			0.1		0.1		
		I _{OL} = 20 µA	6	0.1			0.1		0.1		
	Low level output voltage TTL loads	I _{OL} = 4 mA	4.5	0.26			0.33		0.4		
		I _{OL} = 5.2 mA	6	0.26			0.33		0.4		
I _I	Input leakage current	V _{CC} or GND	6	±0.1			±1		±1		µA
I _{CC}	Quiescent device current	V _{CC} or GND	6	8			80		160		µA
HCT TYPES											
V _{IH}	High level input voltage		4.5 to 5.5	2			2		2		V
V _{IL}	Low level input voltage		4.5 to 5.5	0.8			0.8		0.8		V
V _{OH}	High level output voltage CMOS loads	I _{OH} = – 20 µA	4.5	4.4			4.4		4.4		V
	High level output voltage TTL loads	I _{OH} = – 4 mA	4.5	3.98			3.84		3.7		
V _{OL}	Low level output voltage	I _{OL} = 20 µA	4.5	0.1			0.1		0.1		V
	Low level output voltage	I _{OL} = 4 mA	4.5	0.26			0.33		0.4		
I _I	Input leakage current	V _{CC} and GND	5.5	±0.1			±1		±1		µA
I _{CC}	Supply current	V _{CC} or GND	5.5	8			80		160		µA
ΔI _{CC} (1)	Additional supply current per input pin	CP, MR inputs held at V _{CC} - 2.1	4.5 to 5.5	100 180			225		245		µA

(1) For dual-supply systems theoretical worst case (V_I = 2.4 V, V_{CC} = 5.5 V) specification is 1.8 mA.

(2) V_I = V_{IH} or V_{IL}, unless otherwise noted.

5.5 Prerequisite for Switching Specifications

PARAMETER		V _{CC} (V)	25°C		-40°C to 85°C		-55°C to 125°C		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
HC TYPES									
f _{MAX}	Maximum input pulse frequency	2	6	5	4	MHz			
		4.5	30	24	20	MHz			
		6	35	29	24	MHz			
t _W	Input pulse width	2	80	100	120	ns			
		4.5	16	20	24	ns			
		6	14	17	20	ns			
t _{REM}	Reset removal time	2	50	65	75	ns			
		4.5	10	13	15	ns			
		6	9	11	13	ns			
t _W	Reset pulse width	2	80	100	120	ns			
		4.5	16	20	24	ns			
		6	14	17	20	ns			
HCT TYPES									
f _{MAX}	Maximum input pulse frequency	4.5	25	20	16	MHz			
t _W	Input pulse width	4.5	20	25	30	ns			
t _{REC}	Reset recovery time	4.5	10	13	15	ns			
t _W	Reset pulse width	4.5	20	25	30	ns			

5.6 Switching Characteristics

$t_r, t_f = 6$ ns. See (Parameter Measurement Information)

PARAMETER		TEST CONDITIONS	V _{CC} (V)	25°C			-40°C to 85°C		-55°C to 125°C		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
HC TYPES											
t _{PLH} , t _{PHL}	Propagation delay time CP to Q1' output	C _L = 50 pF	2	140			175		210		ns
			4.5	28			35		42		ns
		C _L = 15 pF	5	11							ns
		C _L = 50 pF	6	24			30		36		ns
t _{PLH} , t _{PHL}	Propagation delay time, Q _n to Q _n + 1	C _L = 50 pF	2	75			95		110		ns
			4.5	15			19		22		ns
		C _L = 15 pF	5	6							ns
		C _L = 50 pF	6	13			13		19		ns
t _{PLH} , t _{PHL}	Propagation delay time, MR to Q _n	C _L = 50 pF	2	170			215		255		ns
			4.5	34			43		51		ns
			5	14							ns
			6	29			27		43		ns
t _{TLH} , t _{THL}	Output transition time	C _L = 50 pF	2	75			95		110		ns
			4.5	15			19		22		ns
			6	13			16		19		ns
C _{IN}	Input capacitance	C _L = 50 pF	10			10		10		pF	
C _{PD}	Power dissipation capacitance ^{(1) (2)}	C _L = 15 pF	5	30							pF
HCT TYPES											
t _{PLH} , t _{PHL}	Propagation delay time CP to Q1' output	C _L = 50 pF	4.5	40			50		60		ns
											ns
		C _L = 15 pF	5	17							ns
											ns
t _{PLH} , t _{PHL}	Propagation delay time, Q _n to Q _n + 1	C _L = 50 pF	4.5	15			19		22		ns
		C _L = 15 pF	5	6							ns
t _{PLH} , t _{PHL}	Propagation delay time, MR to Q _n	C _L = 50 pF	4.5	40			50		60		
		C _L = 15 pF	5	17							
t _{TLH} , t _{THL}	Output transition time	C _L = 50 pF	4.5	15			19		22		ns
C _{IN}	Input capacitance	C _L = 15 pF	10			10		10		pF	
C _{PD}	Power dissipation capacitance ^{(1) (2)}	C _L = 15 pF	5	30							pF

(1) C_{PD} is used to determine the dynamic power consumption, per buffer.

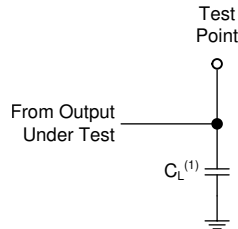
(2) $P_D = V_{CC}^2 f_i + \sum (C_L V_{CC}^2 f_i / M)$ where: $M = 2^1, 2^2, 2^3, 2^4, 2^5, 2^6, 2^7$ f_i = input frequency, C_L = output load capacitance, V_{CC} = supply voltage.

6 Parameter Measurement Information

Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1 \text{ MHz}$, $Z_O = 50 \Omega$, $t_t < 6 \text{ ns}$.

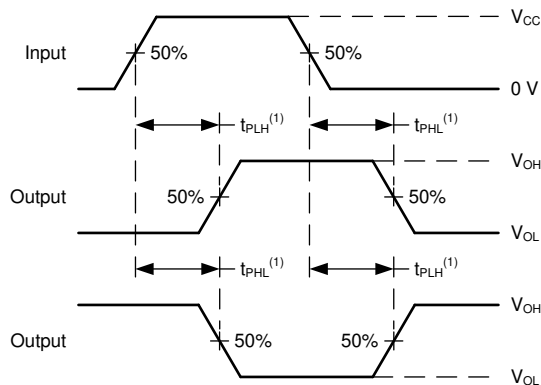
For clock inputs, $f_{\max}$ is measured when the input duty cycle is 50%.

The outputs are measured one at a time with one input transition per measurement.



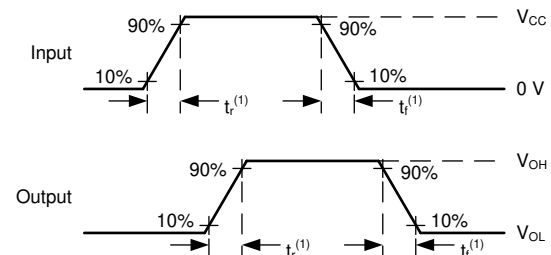
(1) C_L includes probe and test-fixture capacitance.

FIG 6-1. Load Circuit for Push-Pull Outputs



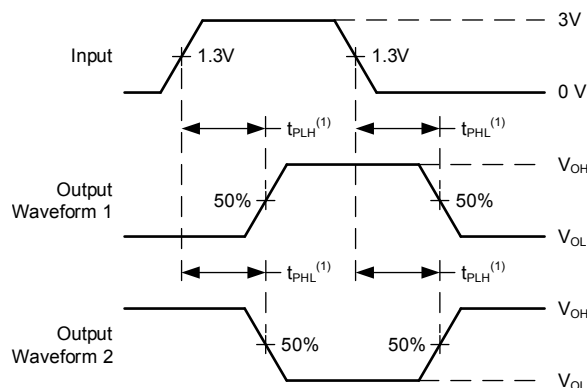
(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

FIG 6-2. Voltage Waveforms, Propagation Delays for Standard CMOS Inputs



(1) The greater between t_r and t_f is the same as t_t .

FIG 6-3. Voltage Waveforms, Input and Output Transition Times for Standard CMOS Inputs



(1) The greater between t_{PLH} and t_{PHL} is the same as t_{pd} .

FIG 6-4. Voltage Waveforms, Propagation Delays for TTL-Compatible Inputs

8 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in the *Recommended Operating Conditions*. Each V_{CC} terminal should have a good bypass capacitor to prevent power disturbance. A 0.1- μ F capacitor is recommended for this device. It is acceptable to parallel multiple bypass caps to reject different frequencies of noise. The 0.1- μ F and 1- μ F capacitors are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

9 Layout

9.1 Layout Guidelines

When using multiple-input and multiple-channel logic devices inputs must not ever be left floating. In many cases, functions or parts of functions of digital logic devices are unused; for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such unused input pins must not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. All unused inputs of digital logic devices must be connected to a logic high or logic low voltage, as defined by the input voltage specifications, to prevent them from floating. The logic level that must be applied to any particular unused input depends on the function of the device. Generally, the inputs are tied to GND or V_{CC} , whichever makes more sense for the logic function or is more convenient.

10 Device and Documentation Support

TI offers an extensive line of development tools. Tools and software to evaluate the performance of the device, generate code, and develop solutions are listed below.

10.1 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Subscribe to updates* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

10.2 サポート・リソース

[TI E2E™ サポート・フォーラム](#)は、エンジニアが検証済みの回答と設計に関するヒントをエキスパートから迅速かつ直接得ることができる場所です。既存の回答を検索したり、独自の質問をしたりすることで、設計に必要な支援を迅速に得ることができます。

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10.3 Trademarks

TI E2E™ is a trademark of Texas Instruments.

すべての商標は、それぞれの所有者に帰属します。

10.4 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

10.5 Glossary

[TI Glossary](#)

This glossary lists and explains terms, acronyms, and definitions.

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package Pins	Package qty Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
CD54HC4024F	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC4024F
CD54HC4024F.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HC4024F
CD54HCT4024F3A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT4024F3A
CD54HCT4024F3A.A	Active	Production	CDIP (J) 14	25 TUBE	No	SNPB	N/A for Pkg Type	-55 to 125	CD54HCT4024F3A
CD74HC4024E	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4024E
CD74HC4024E.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HC4024E
CD74HC4024M	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-55 to 125	HC4024M
CD74HC4024M96	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU SN NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4024M
CD74HC4024M96.A	Active	Production	SOIC (D) 14	2500 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HC4024M
CD74HC4024MT	Obsolete	Production	SOIC (D) 14	-	-	Call TI	Call TI	-55 to 125	HC4024M
CD74HC4024PW	Obsolete	Production	TSSOP (PW) 14	-	-	Call TI	Call TI	-55 to 125	HJ4024
CD74HC4024PWR	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU SN NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4024
CD74HC4024PWR.A	Active	Production	TSSOP (PW) 14	2000 LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HJ4024
CD74HCT4024E	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4024E
CD74HCT4024E.A	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4024E
CD74HCT4024EE4	Active	Production	PDIP (N) 14	25 TUBE	Yes	NIPDAU	N/A for Pkg Type	-55 to 125	CD74HCT4024E
CD74HCT4024M	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4024M
CD74HCT4024M.A	Active	Production	SOIC (D) 14	50 TUBE	Yes	NIPDAU	Level-1-260C-UNLIM	-55 to 125	HCT4024M

⁽¹⁾ **Status:** For more details on status, see our [product life cycle](#).

⁽²⁾ **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

⁽³⁾ **RoHS values:** Yes, No, RoHS Exempt. See the [TI RoHS Statement](#) for additional information and value definition.

⁽⁴⁾ **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

⁽⁵⁾ **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

⁽⁶⁾ **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF CD54HC4024, CD54HCT4024, CD74HC4024, CD74HCT4024 :

- Catalog : [CD74HC4024](#), [CD74HCT4024](#)
- Military : [CD54HC4024](#), [CD54HCT4024](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

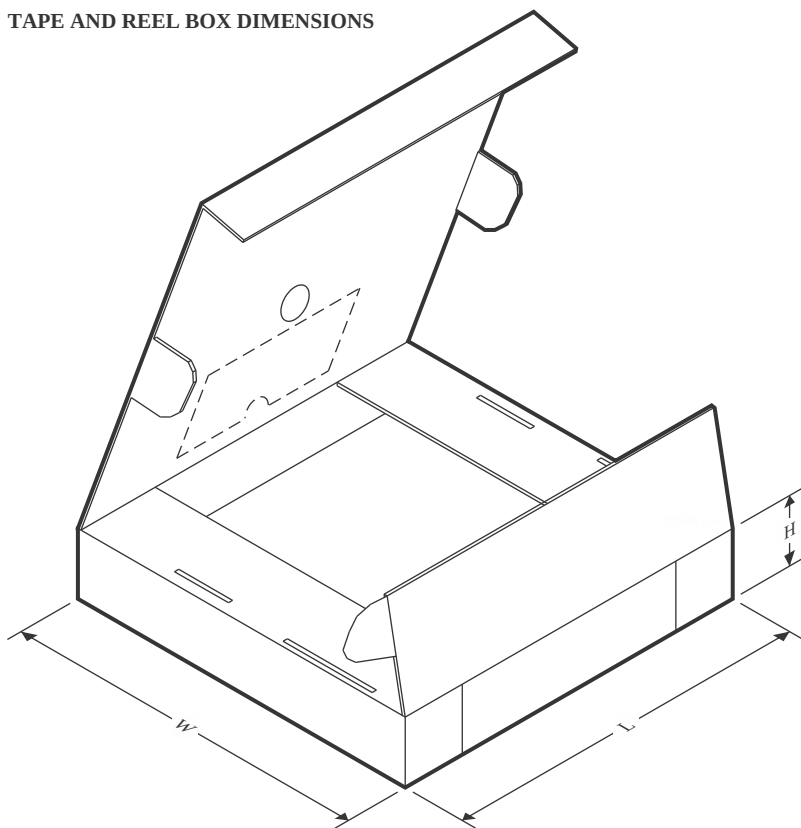
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CD74HC4024M96	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
CD74HC4024PWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1
CD74HC4024PWR	TSSOP	PW	14	2000	330.0	12.4	6.85	5.45	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

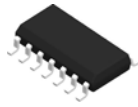
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CD74HC4024M96	SOIC	D	14	2500	356.0	356.0	35.0
CD74HC4024PWR	TSSOP	PW	14	2000	356.0	356.0	35.0
CD74HC4024PWR	TSSOP	PW	14	2000	366.0	364.0	50.0

TUBE

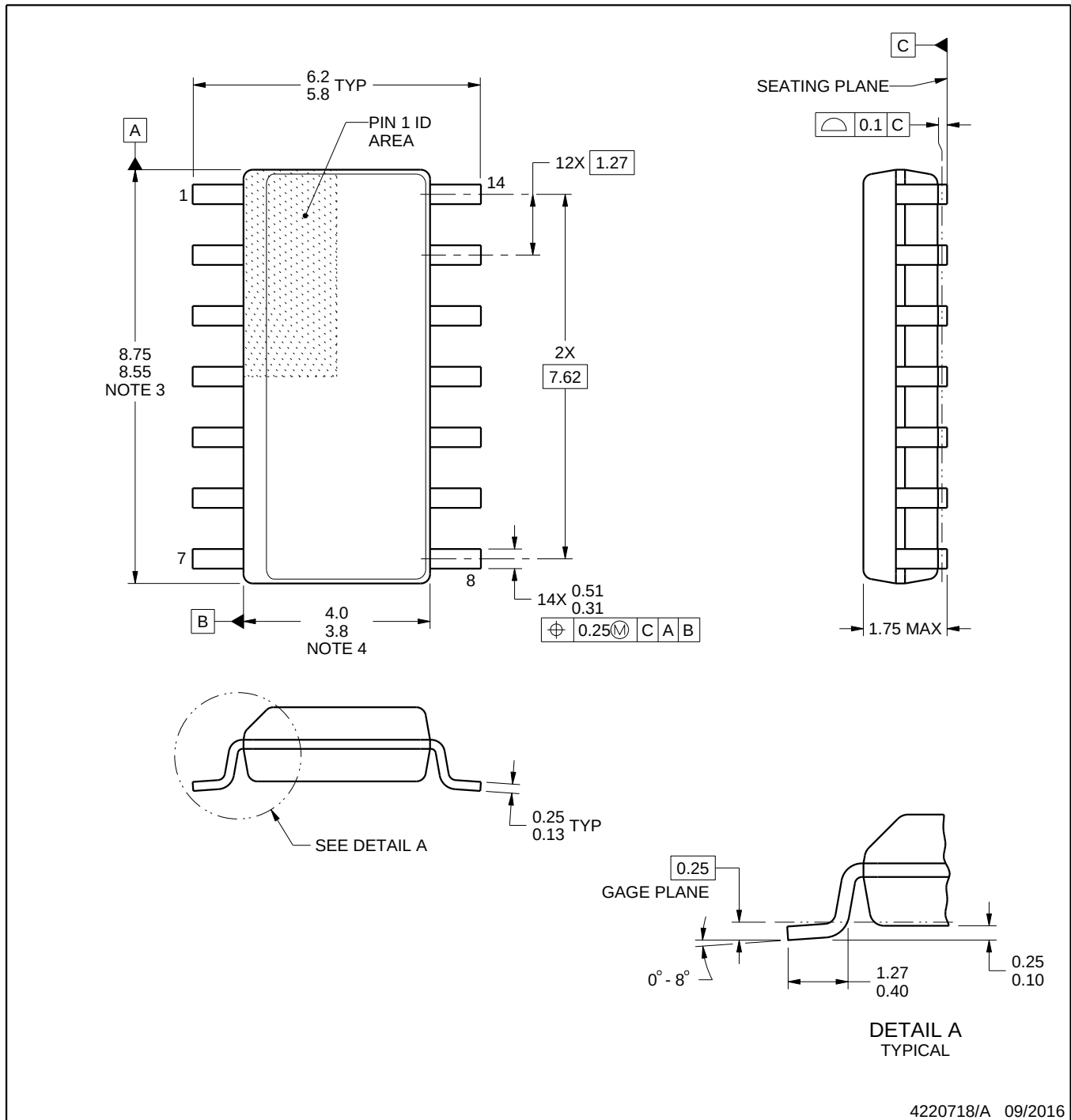


*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
CD74HC4024E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC4024E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC4024E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HC4024E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT4024E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT4024E	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT4024E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT4024E.A	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT4024EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT4024EE4	N	PDIP	14	25	506	13.97	11230	4.32
CD74HCT4024M	D	SOIC	14	50	506.6	8	3940	4.32
CD74HCT4024M.A	D	SOIC	14	50	506.6	8	3940	4.32

D0014A**PACKAGE OUTLINE****SOIC - 1.75 mm max height**

SMALL OUTLINE INTEGRATED CIRCUIT

**NOTES:**

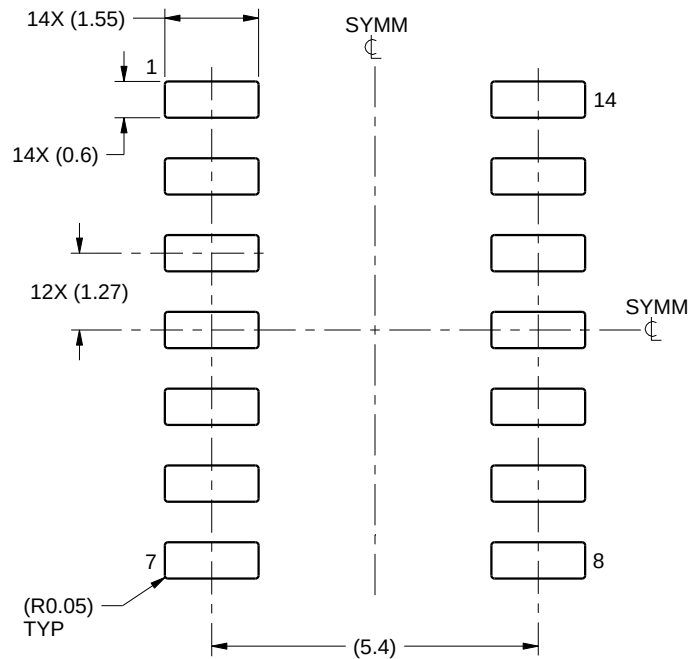
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm, per side.
5. Reference JEDEC registration MS-012, variation AB.

EXAMPLE BOARD LAYOUT

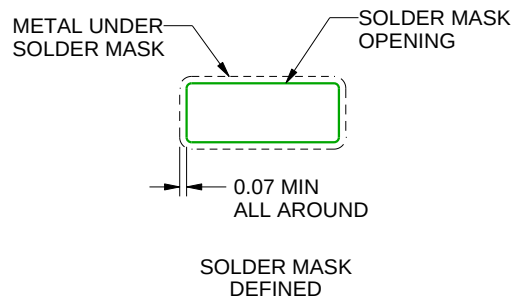
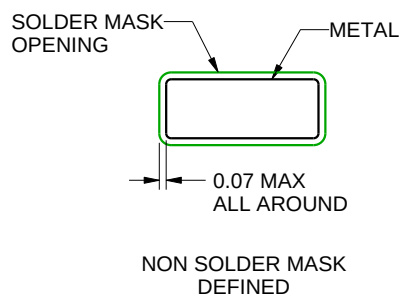
D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
SCALE:8X



SOLDER MASK DETAILS

4220718/A 09/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

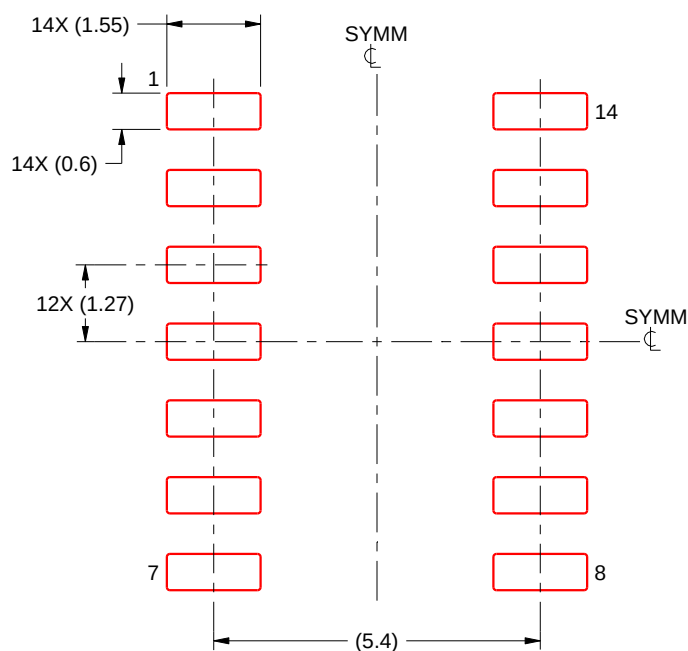
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0014A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:8X

4220718/A 09/2016

NOTES: (continued)

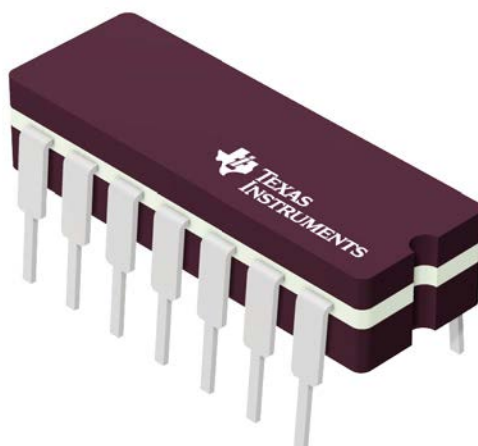
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

J 14

GENERIC PACKAGE VIEW

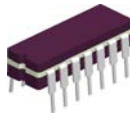
CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE

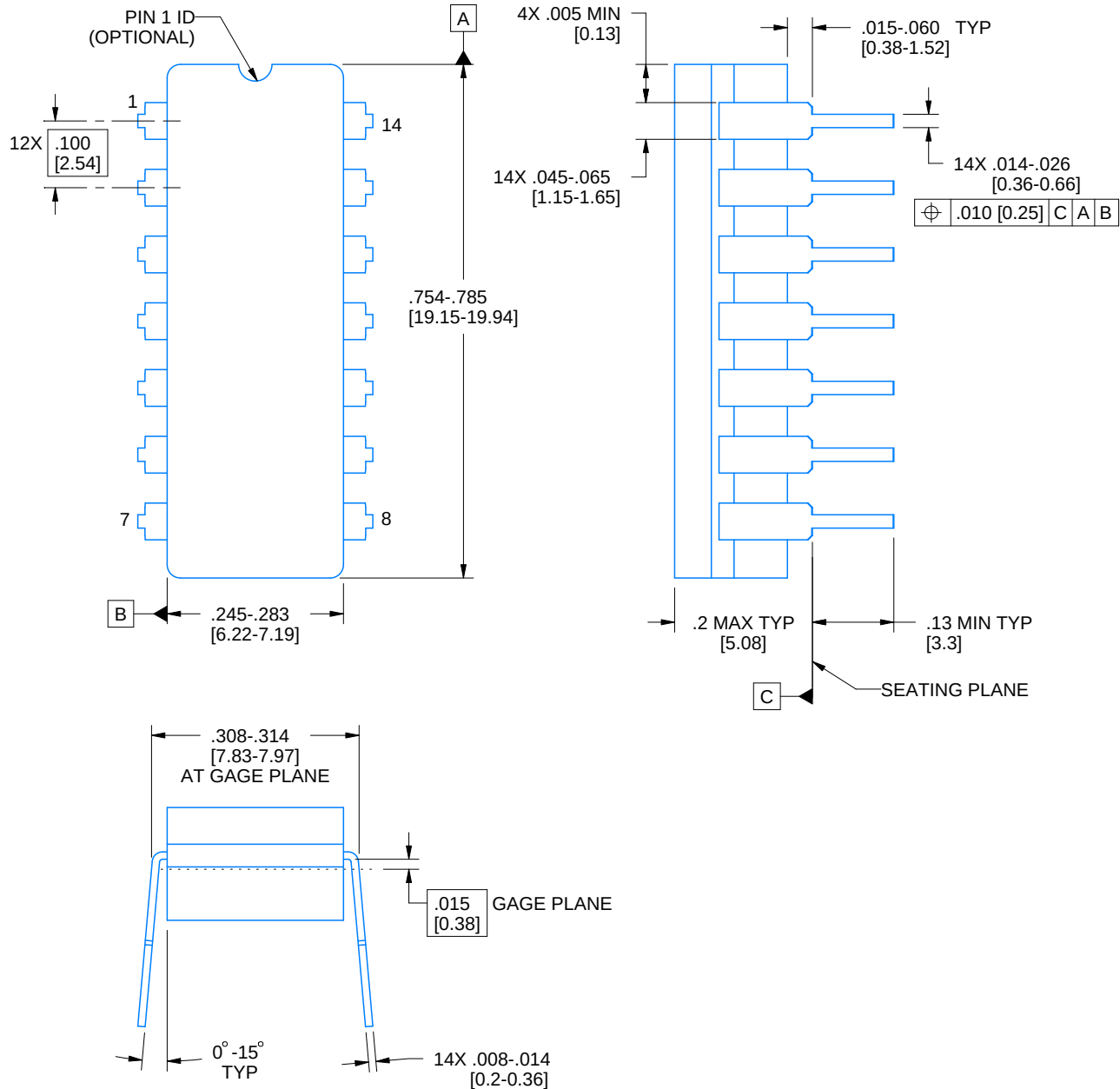


Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4040083-5/G

J0014A**PACKAGE OUTLINE****CDIP - 5.08 mm max height**

CERAMIC DUAL IN LINE PACKAGE



4214771/A 05/2017

NOTES:

1. All controlling linear dimensions are in inches. Dimensions in brackets are in millimeters. Any dimension in brackets or parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This package is hermetically sealed with a ceramic lid using glass frit.
4. Index point is provided on cap for terminal identification only and on press ceramic glass frit seal only.
5. Falls within MIL-STD-1835 and GDIP1-T14.



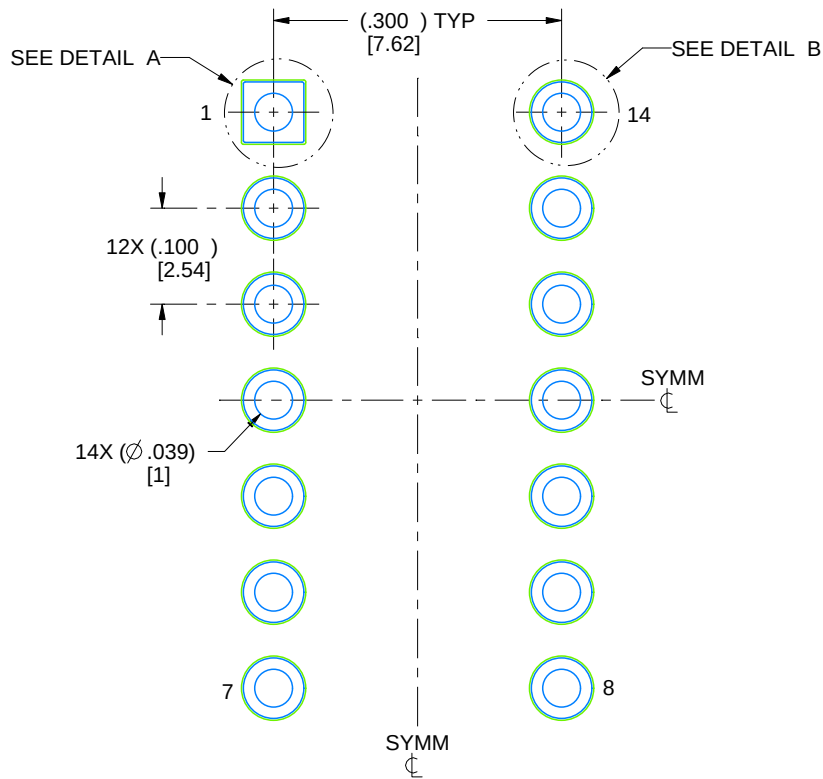
**TEXAS
INSTRUMENTS**
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EXAMPLE BOARD LAYOUT

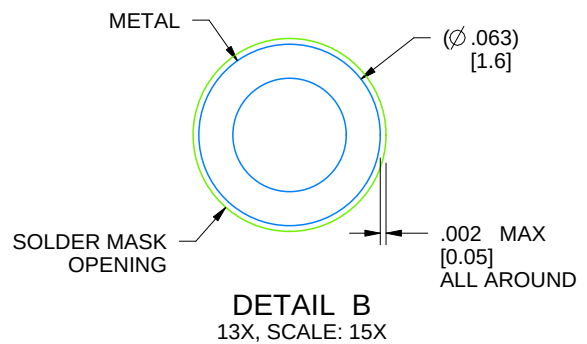
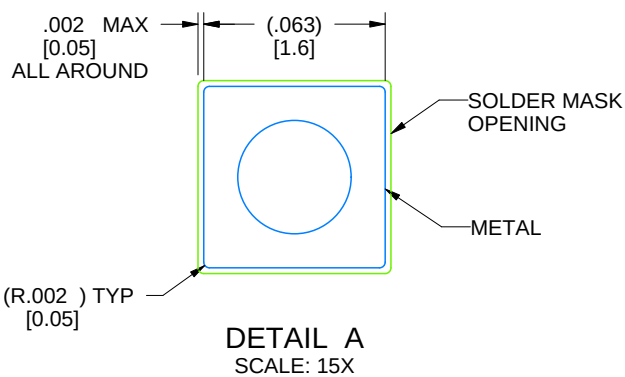
J0014A

CDIP - 5.08 mm max height

CERAMIC DUAL IN LINE PACKAGE



LAND PATTERN EXAMPLE
NON-SOLDER MASK DEFINED
SCALE: 5X

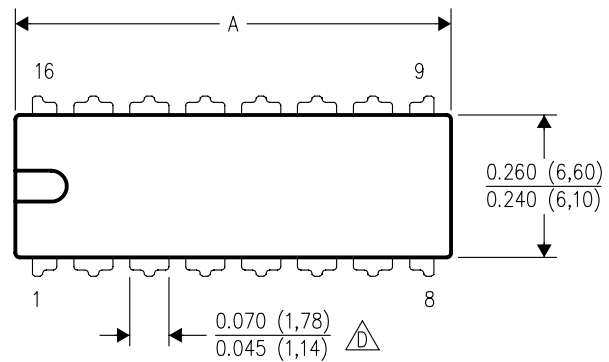


4214771/A 05/2017

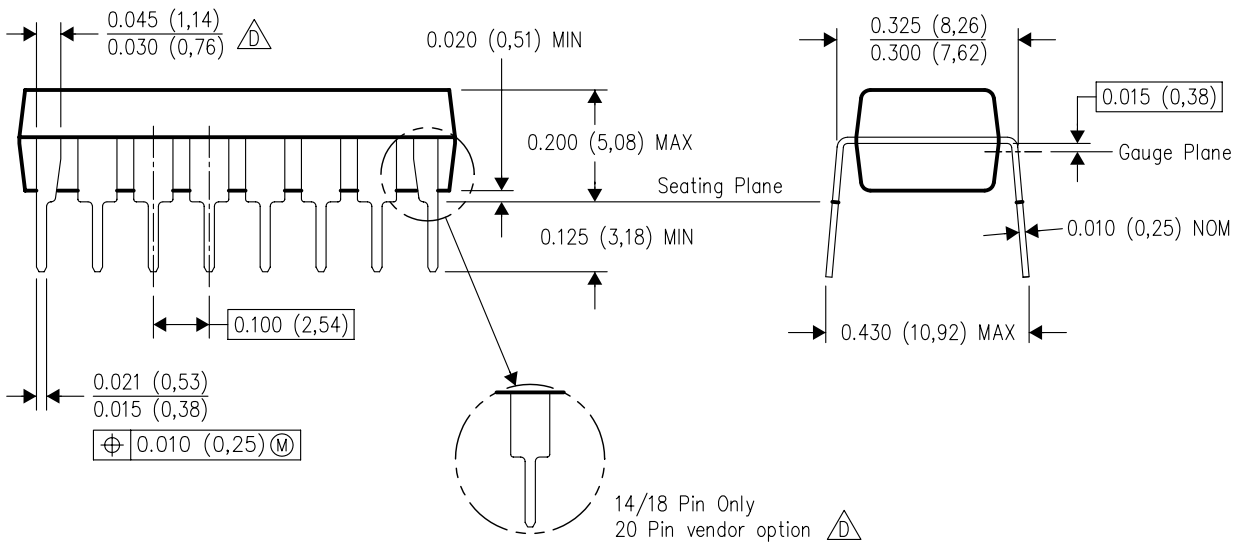
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



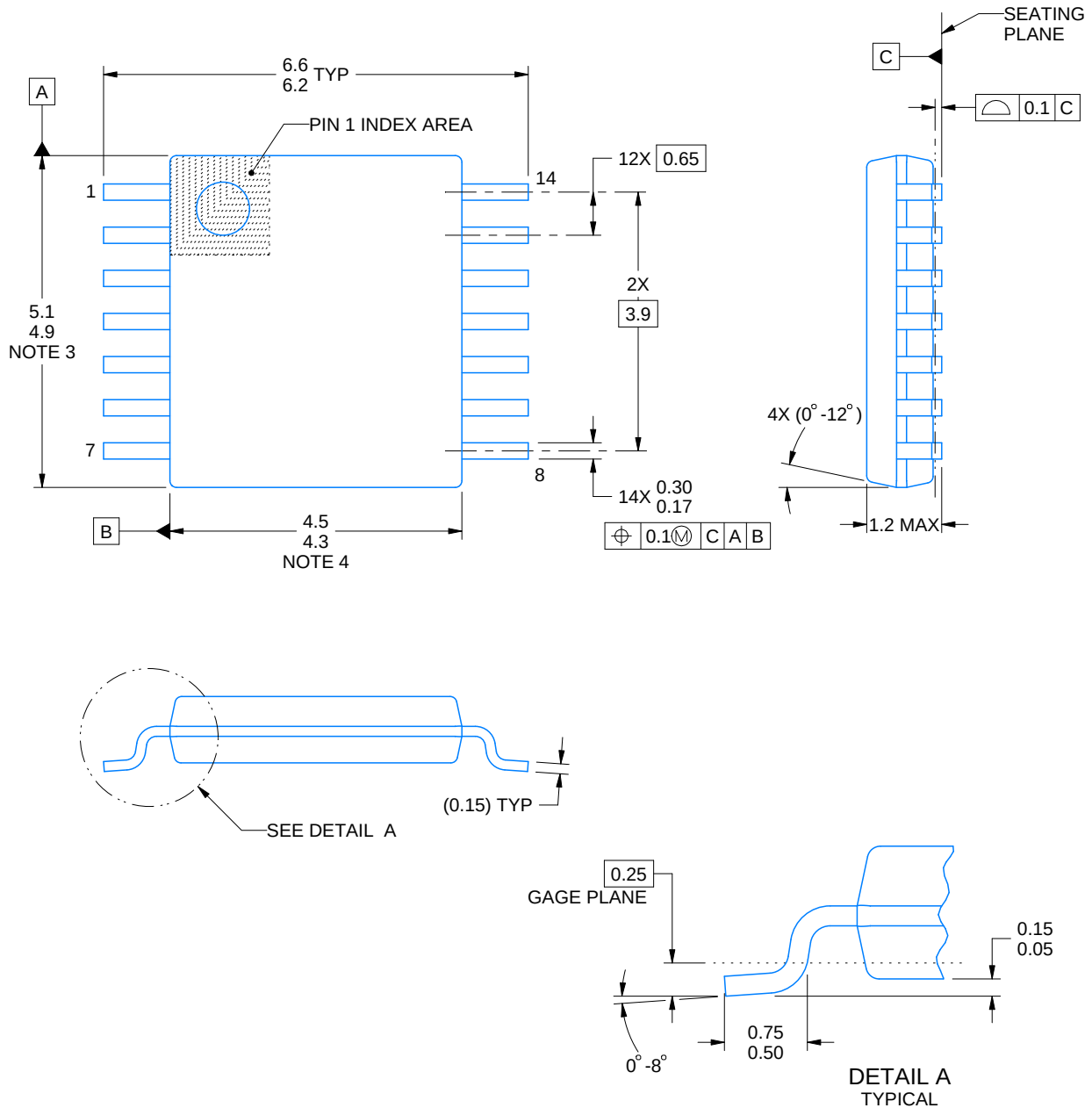
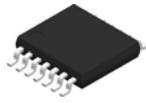
PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.



4220202/B 12/2023

NOTES:

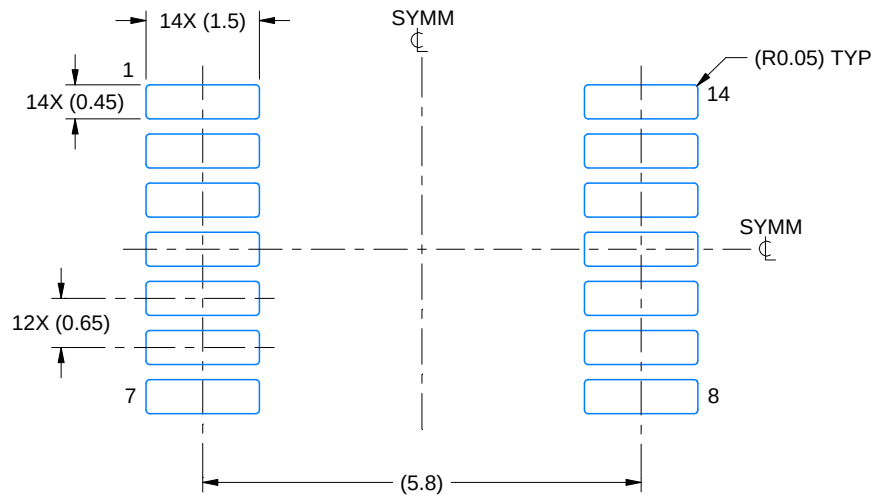
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

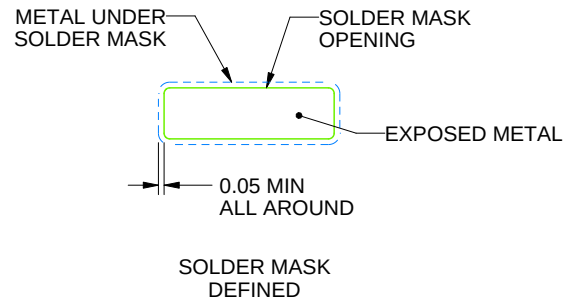
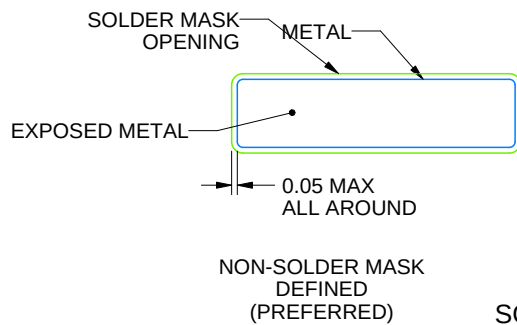
PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



SOLDER MASK DETAILS

4220202/B 12/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

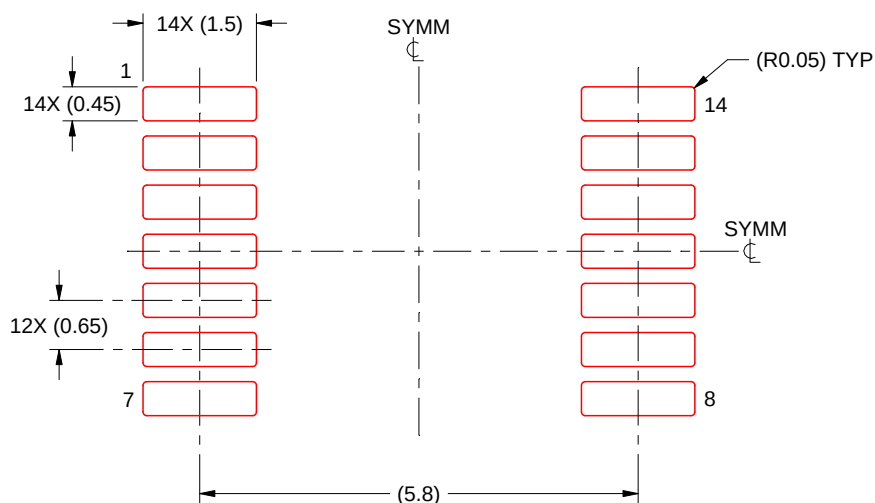
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

PW0014A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220202/B 12/2023

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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