SNx5HVD1176 PROFIBUS® RS-485 トランシーバ

1 特長

- PROFIBUS® ネットワーク向けに最適化
  - 最大 40Mbps の信号速度
  - 2.1 V を超える差動出力 (54Ω 負荷時)
  - 10pF の低バス容量 (最大値)
- TIA/EIA-485-A の要件に準拠
- ±10kV HBM を超える ESD の保護
- バスの開放、短絡、またはアイドル時のフェイル・セーフを備えるレシーバ
- バス上のトランシーバ数は最大 160 個
- 出力遷移時およびドライバのイネーブル / ディスエーブル切り替え時の低いスキュー
- 最大 50 MHz までの同相信号除去
- 回路短絡時の電流制限
- ホット・スワップに対応
- サーマル・シャットダウン保護機能

2 アプリケーション

- プロセス・オートメーション
  - 化学物質の製造
  - 醸造と蒸留
  - 製紙
- ファクトリ・オートメーション
  - 自動車の製造
  - ローリング、プレス、スタンプ機械
  - ネットワーク接続センサ
- 一般的な RS-485 ネットワーク
  - モータおよびモーション制御
  - HVAC およびビルディング・オートメーション・ネットワーク
  - ネットワーク接続セキュリティ・ステーション

3 概要

SNx5HVD1176 デバイスは、PROFIBUS (EN 50170) アプリケーションでの使用に最適化された特性を持つ、半二重差動トランシーバです。ドライバ出力の差動電圧は、PROFIBUS の要件 (54Ω の負荷で 2.1V) を上回ります。テクノロジーの成長を、最大 40Mbps の信号速度という高いデータ転送速度で支えます。小さなバス容量により、信号の歪みが抑制されます。

SN65HVD1176 および SN75HVD1176 デバイスは、ツイストペア・ネットワークを介した差動データ転送のための ANSI 標準 TIA/EIA-485-A (RS-485) の要件を満たすか、それを上回る性能を備えています。ドライバ出力とレシーバ入力は互いに接続されており、単位負荷が 1/5 となる半二重バス・ポートを形成しているので、1 つのバスで最大 160 のノードを使用できます。バス・ラインが短絡している場合、開放されている場合、またはドライバがアクティブでない場合、レシーバの出力はロジック High に維持されます。電源電圧が 2.5V を下回ると、ドライバ出力は高インピーダンスになり、電源サイクル中またはバスへのライブ挿入中のバスの外乱を防止します。短絡フォルト状況では、内部電流制限により出力電流が一定値に制限されるので、これにより、トランシーバのバス・ピンを保護します。サーマル・シャットダウン回路は、負荷および駆動の状況に障害がある場合に発生する、過剰な消費電力による損傷からデバイスを保護します。

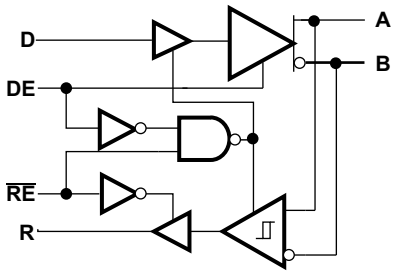
SN75HVD1176 デバイスは 0℃～70℃の温度範囲で、SN65HVD1176 デバイスは -40℃～85℃の範囲での動作が規定されています。

このデバイスの絶縁型バージョンについては、デジタル・アイソレータ内蔵の ISO1176 デバイス (SLLS897) を参照してください。

パッケージ情報

部品番号	パッケージ(1)	本体サイズ (公称)
SN65HVD1176 SN75HVD1176	SOIC (8)	4.90mm × 3.91mm

(1) 利用可能なパッケージについては、このデータシートの末尾にある注文情報を参照してください。



論理図 (正論理)

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- Changed the *Thermal Information* table ... 5
- Changed the *Typical Characteristics* graphs ... 10

Changes from Revision G (June 2015) to Revision H (September 2015) — **Page**

- Changed V_{ID} ≥ 0.02 V To: V_{ID} ≥ –0.02 V in 表 7-2 ... 17

Changes from Revision F (June 2013) to Revision G (June 2015) — **Page**

- 「ピン構成および機能」セクション、「ESD 定格」表、「消費電力」表、「機能説明」セクション、「デバイスの機能モード」、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加 ... 1
- Added storage temperature to the *Absolute Maximum Ratings* table ... 4
- Added Psi JT and Psi JB values to the *Thermal Information* table ... 5
- Deleted redundant $I_{O(OFF)}$ and I_{OZ} lines from the *Electrical Characteristics* table ... 6
- Deleted redundant C_{OD} line from the *Electrical Characteristics* table ... 6

Changes from Revision E (August 2008) to Revision F (June 2013) — **Page**

- ピン配置とロジック図で、RE を $\overline{RE}$ に変更 ... 1

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5 Pin Configuration and Functions

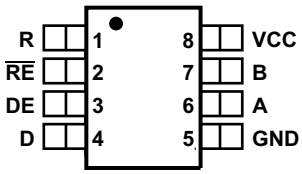

図 5-1. D Package 8-Pin SOIC Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
A	6	Bus input/output	Driver output/receiver input (complementary to B)
B	7	Bus input/output	Driver output/receiver input (complementary to A)
D	4	Digital input	Driver data input
DE	3	Digital input	Driver enable high
GND	5	Reference potential	Local device ground
R	1	Digital output	Receive data output
$\overline{RE}$	2	Digital input	Receiver enable low
VCC	8	Supply	3-V to 5.5-V supply

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6 Specifications

6.1 Absolute Maximum Ratings

over operating junction temperature range unless otherwise noted(1)

		MIN	MAX	UNIT
V_{CC}	Supply voltage(2)	–0.5	7	V
	Voltage at any bus I/O terminal	–9	14	V
	Voltage input, transient pulse, A and B, (through 100 Ω, see 図 7-15)	–40	40	V
	Voltage input at any D, DE or $\overline{RE}$ terminal	–0.5	7	V
I_O	Receiver output current	–10	10	mA
T_J	Junction temperature		150	°C
T_{stg}	Storage temperature	–40	130	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. All voltage values are with respect to the network ground terminal unless otherwise noted.
(2) All voltage values, except differential I/O bus voltages, are with respect to network ground terminal.

6.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	All pins	±4000	V
			Bus terminals and GND	±10000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

			MIN	NOM	MAX	UNIT
V_{CC}	Supply voltage		4.75	5	5.25	V
	Voltage at either bus I/O terminal	A, B	–7		12	V
V_{IH}	High-level input voltage	D, DE, $\overline{RE}$	2		V_{CC}	V
V_{IL}	Low-level input voltage		0		0.8	V
V_{IL}	Differential input voltage	A with respect to B	–12		12	V
I_O	Output current	Driver	–70		70	mA
		Receiver	–8		8	mA
T_J	Junction temperature (1)	SN65HVD1176	–40		130	°C
		SN75HVD1176	0		130	°C
R_L	Differential load resistance		54			Ω
$1/t_{U1}$	Signaling rate				40	Mbps

(1) See the セクション 6.7 table for more information on maintenance of this requirement.

6.4 Thermal Information

THERMAL METRIC(1)		SN75HVD1176	SN65HVD1176	UNIT
		D (SOIC)	D (SOIC)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance(2)	104.7	116.7	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	45.8	56.3	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	45.9	63.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.7	8.8	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.2	62.2	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.
(2) The intent of $R_{\theta JA}$ specification is solely for a thermal performance comparison of one package to another in a standardized environment. This methodology is not meant to and will not predict the performance of a package in an application-specific environment.

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6.5 Electrical Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
DRIVER							
V_O	Open-circuit output voltage	A or B	No load	0		V_{CC}	V
$\|V_{OD(SS)}\|$	Steady-state differential output voltage magnitude	R_L = 54 Ω	See 図 7-1	2.1	2.9		V
		With common-mode loading, (V_{TEST} from –7 V to 12 V) See 図 7-2		2.1	2.7		V
$\Delta\|V_{OD(SS)}\|$	Change in steady-state differential output voltage between logic states	See 図 7-1 and 図 7-6		–0.2	0	0.2	V
$V_{OC(SS)}$	Steady-state common-mode output voltage	See 図 7-5		2	2.5	3	V
$\Delta V_{OC(SS)}$	Change in steady-state common-mode output voltage	See 図 7-5		–0.2	0	0.2	V
$V_{OC(PP)}$	Peak-to-peak common-mode output voltage	See 図 7-5			0.5		V
$V_{OD(RING)}$	Differential output voltage over and under shoot	R_L = 54 Ω, C_L = 50 pF See 図 7-6				10%	$V_{OD(PP)}$
I_I	Input current	D, DE		–50		50	µA
$I_{OS(P)}$	Peak short-circuit output current	DE at V_{CC}, See 図 7-8	V_{OS} = –7 V to 12 V	–250		250	mA
$I_{OS(SS)}$	Steady-state short-circuit output current	DE at V_{CC}, See 図 7-8	V_{OS} > 4 V, Output driving low	60	90	135	mA
			VOS < 1 V, Output driving high	–135	–90	–60	mA
RECEIVER							
$V_{IT(+)}$	Positive-going differential input voltage threshold	See 図 7-9	V_O = 2.4 V, I_O = –8 mA		–80	–20	mV
$V_{IT(–)}$	Negative-going differential input voltage threshold		V_O = 0.4 V, I_O = 8 mA	–200	–120		mV
V_{HYS}	Hysteresis voltage (V_{IT+} – V_{IT-})				40		mV
V_{OH}	High-level output voltage	V_{ID} = 200 mV, I_{OH} = –8 mA, See 図 7-9		4	4.6		V
V_{OL}	Low-level output voltage	V_{ID} = –200 mV, I_{OL} = 8 mA, See 図 7-9			0.2	0.4	V
I_A, I_B	Bus pin input current	V_I = –7 V to 12 V, Other input = 0 V	V_{CC} = 4.75 V to 5.25 V	–160		200	µA
$I_{A(OFF)}$ $I_{B(OFF)}$			V_{CC} = 0 V	–160		200	
I_I	Receiver enable input current	$\overline{RE}$		–50		50	µA
I_{OZ}	High-impedance - state output current	$\overline{RE}$ = V_{CC}		–1		1	µA
R_I	Input resistance			60			kΩ
C_{ID}	Differential input capacitance	Test input signal is a 1.5-MHz sine wave with amplitude 1 V_{PP}, capacitance measured across A and B			7	10	pF
C_{MR}	Common mode rejection	See 図 7-11			4		V

(1) All typical values are at V_{CC} = 5 V and 25°C.

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6.6 Supply Current

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{CC}	Supply Current(1)	Driver and receiver, $\overline{RE}$ at 0 V, DE at V_{CC}, All other inputs open, no load		4	6	mA
		Driver only, $\overline{RE}$ at V_{CC}, DE at V_{CC}, All other inputs open, no load		3.8	6	mA
		Receiver only, $\overline{RE}$ at 0 V, DE at 0 V, All other inputs open, no load		3.6	6	mA
		Standby only, $\overline{RE}$ at V_{CC}, DE at 0 V, All other inputs open		0.2	5	µA

(1) Over recommended operating conditions

6.7 Power Dissipation

over recommended operating conditions (unless otherwise noted)

PARAMETER			TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
P_D	Device power dissipation		R_L = 54 Ω, C_L = 50 pF, 0 V to 3 V, 15 MHz, 50% duty cycle square wave input, driver and receiver enabled		277	318	mW
T_A	Ambient air temperature	SN65HVD1176	Low-K board, no air flow, P_D = 318 mW	–40		64	°C
			High-K board, no air flow, P_D = 318 mW	–40		89	°C
		SN75HVD1176	Low-K board, no air flow, P_D = 318 mW	0			°C
			High-K board, no air flow, P_D = 318 mW	0			°C
T_{SD}	Thermal shut down junction temperature				150		°C

(1) All typical values are with V_{CC} = 5 V and T_A = 25°C.

6.8 Switching Characteristics

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS		MIN	TYP(1)	MAX	UNIT
DRIVER							
t_{PLH}	Propagation delay time low-level-to-high-level output	R_L = 54 Ω, C_L = 50 pF, See 図 7-3		4	7	10	ns
t_{PHL}	Propagation delay time high-level-to-low-level output			4	7	10	ns
$t_{sk(p)}$	Pulse skew | $t_{PLH} - t_{PHL}$ |				0	2	ns
t_r	Differential output rise time			2	3	7.5	ns
t_f	Differential output fall time			2	3	7.5	ns
$t_{t(MLH)}$, $t_{t(MHL)}$	Output transition skew	See 図 7-4			0.2	1	ns
$t_{p(AZH)}$, $t_{p(BZH)}$ $t_{p(AZL)}$, $t_{p(BZL)}$	Propagation delay time, high-impedance-to-active output	R_L = 110 Ω, C_L = 50 pF See 図 7-7	$\overline{RE}$ at 0 V		10	20	ns
$t_{p(AHZ)}$, $t_{p(BHZ)}$ $t_{p(ALZ)}$, $t_{p(BLZ)}$	Propagation delay time, active-to- high-impedance output				10	20	ns
$\lvert t_{p(AZL)} - t_{p(BZH)} \rvert$ $\lvert t_{p(AZH)} - t_{p(BZL)} \rvert$	Enable skew time				0.55	1.5	ns
$\lvert t_{p(ALZ)} - t_{p(BHZ)} \rvert$ $\lvert t_{p(AHZ)} - t_{p(BLZ)} \rvert$	Disable skew time					2.5	ns
$t_{p(AZH)}$, $t_{p(BZH)}$ $t_{p(AZL)}$, $t_{p(BZL)}$	Propagation delay time, high-impedance-to-active output (from sleep mode)	R_L = 110 Ω, C_L = 50 pF See 図 7-7	$\overline{RE}$ at 5 V		1	4	µs
$t_{p(AHZ)}$, $t_{p(BHZ)}$ $t_{p(ALZ)}$, $t_{p(BLZ)}$	Propagation delay time, active-output-to high-impedance (to sleep mode)				30	50	ns

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6.8 Switching Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP[1]	MAX	UNIT
$t_{(CFB)}$	Time from application of short-circuit to current foldback	See 図 7-8		0.5		µs
$t_{(TSD)}$	Time from application of short-circuit to thermal shutdown	T_A = 25°C, See 図 7-8	100			µs

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6.8 Switching Characteristics (continued)

over recommended operating conditions (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP(1)	MAX	UNIT
RECEIVER						
t_{PLH}	Propagation delay time, low-to-high level output	See 図 7-10		20	25	ns
t_{PHL}	Propagation delay time, high-to-low level output			20	25	ns
$t_{sk(p)}$	Pulse skew | $t_{PLH} - t_{PHL}$ |			1	2	ns
t_r	Receiver output voltage rise time			2	4	ns
t_f	Receiver output voltage fall time			2	4	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output	DE at V_{CC}, See 図 7-13			20	ns
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output				20	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output	DE at V_{CC}, See 図 7-14			20	ns
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output				20	ns
t_{PZH}	Propagation delay time, high-impedance-to-high-level output (standby to active)	DE at 0 V, See 図 7-12		1	4	µs
t_{PHZ}	Propagation delay time, high-level-to-high-impedance output (active to standby)			13	20	ns
t_{PZL}	Propagation delay time, high-impedance-to-low-level output (standby to active)	DE at 0 V, See 図 7-12		2	4	µs
t_{PLZ}	Propagation delay time, low-level-to-high-impedance output (active to standby)			13	20	ns

(1) All typical values are at V_{CC} = 5 V and 25°C.

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6.9 Typical Characteristics

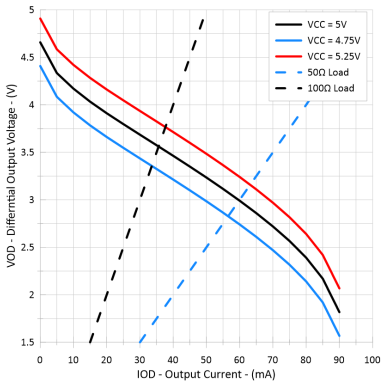

図 6-1. Differential Output Voltage vs Load Current

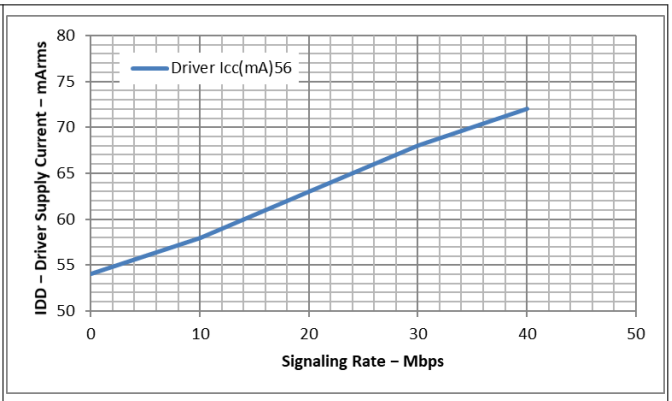

図 6-2. Driver Supply Current vs Signaling Rate

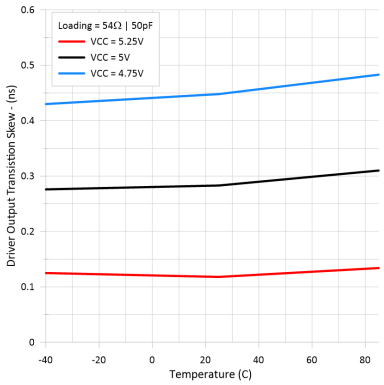

図 6-3. Driver Output Transition Skew vs Free-Air Temperature

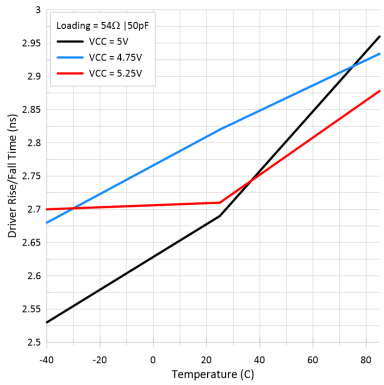

図 6-4. Driver Rise, Fall Time vs Free-Air Temperature

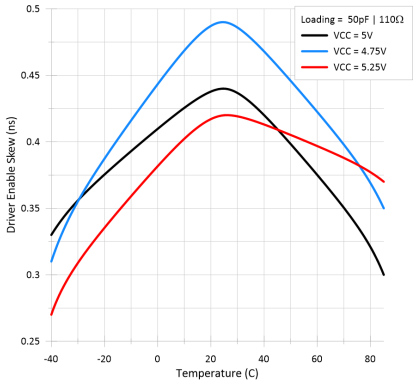

図 6-5. Driver Enable Skew vs Free-Air Temperature

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Parameter Measurement Information

注

Test load capacitance includes probe and jig capacitance (unless otherwise specified).

Signal generator characteristics: rise and fall time < 6 ns, pulse rate 100 kHz, 50% duty cycle, Z_o = 50 Ω (unless otherwise specified).

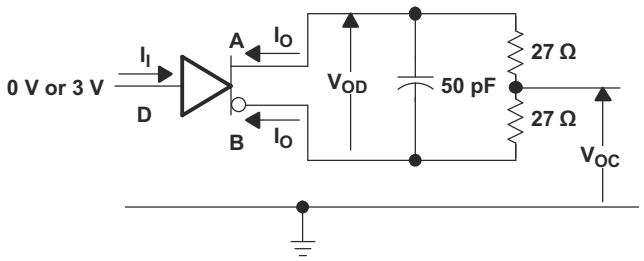

図 7-1. Driver Test Circuit, V_{OD} and V_{OC} Without Common-Mode Loading

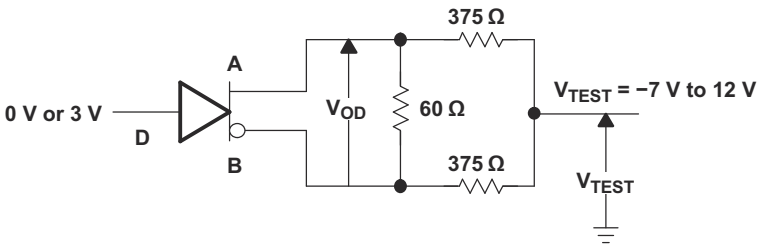

図 7-2. Driver Test Circuit, V_{OD} With Common-Mode Loading

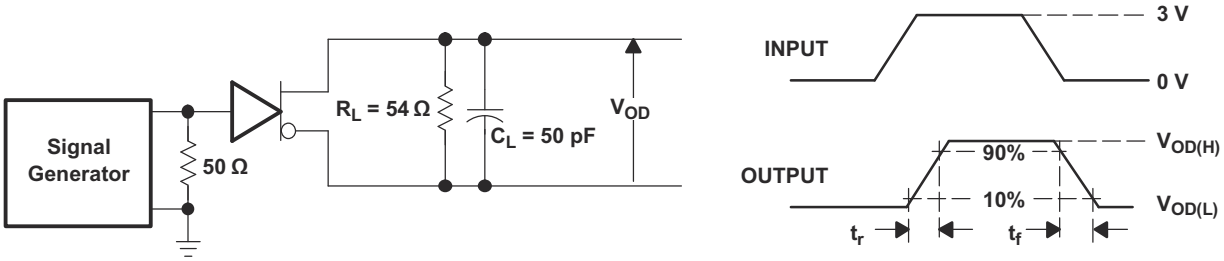

図 7-3. Driver Switching Test Circuit and Rise/Fall Time Measurement

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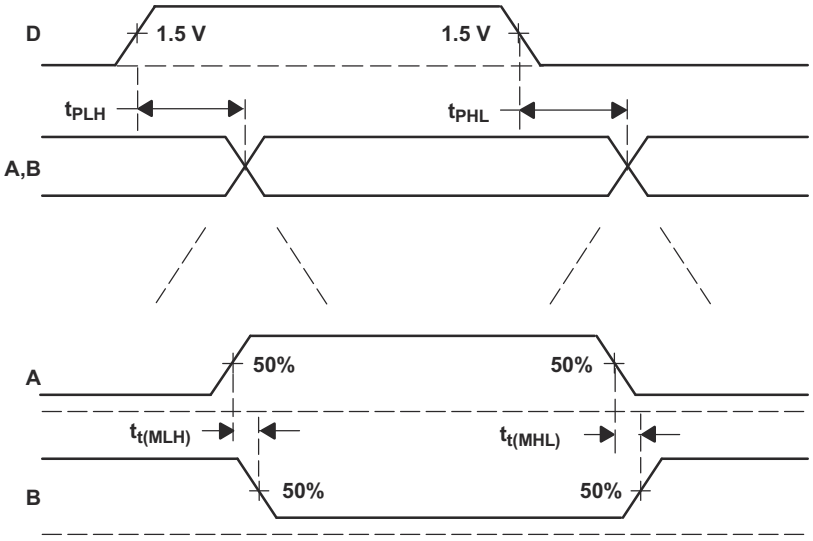


図 7-4. Driver Switching Waveforms for Propagation Delay and Output Midpoint Time Measurements

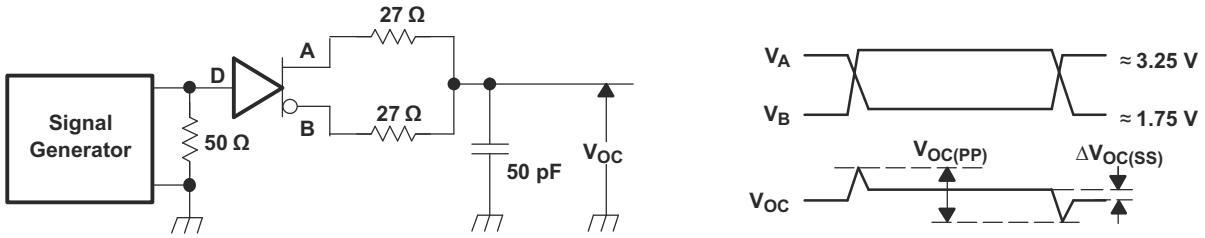
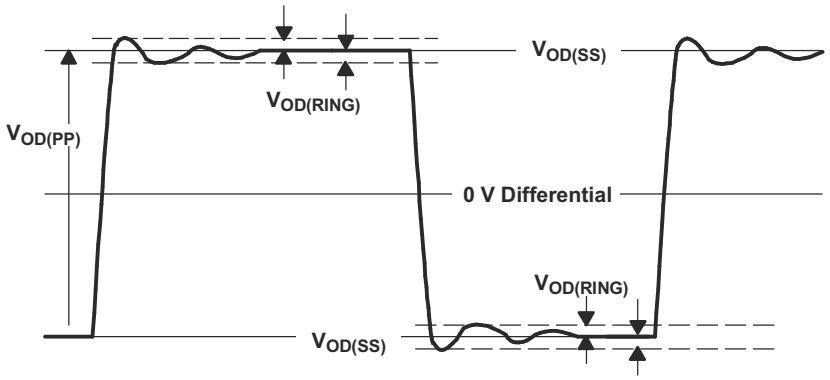


図 7-5. Driver V_{OC} Test Circuit and Waveforms



A. $V_{OD(RING)}$ is measured at four points on the output waveform, corresponding to overshoot and undershoot from the $V_{OD(H)}$ and $V_{OD(L)}$ steady state values.

図 7-6. $V_{OD(RING)}$ Waveform and Definitions

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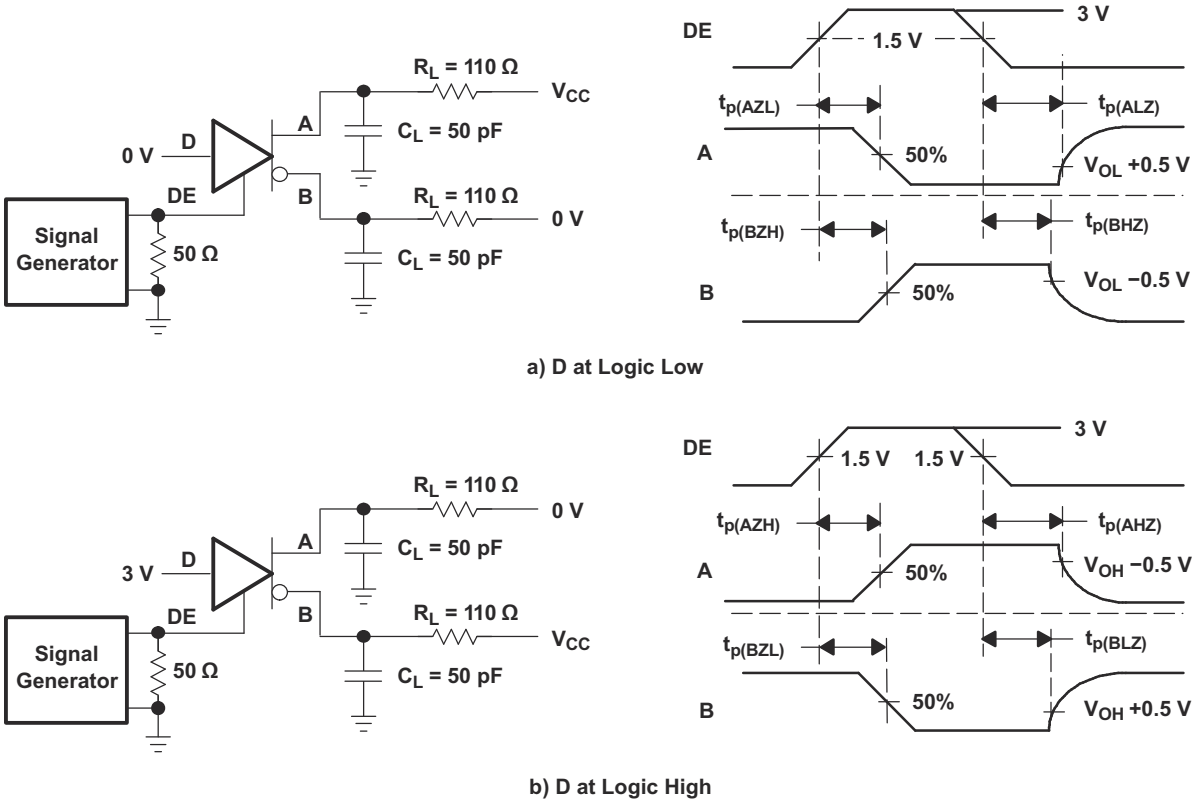

図 7-7. Driver Enable/Disable Test

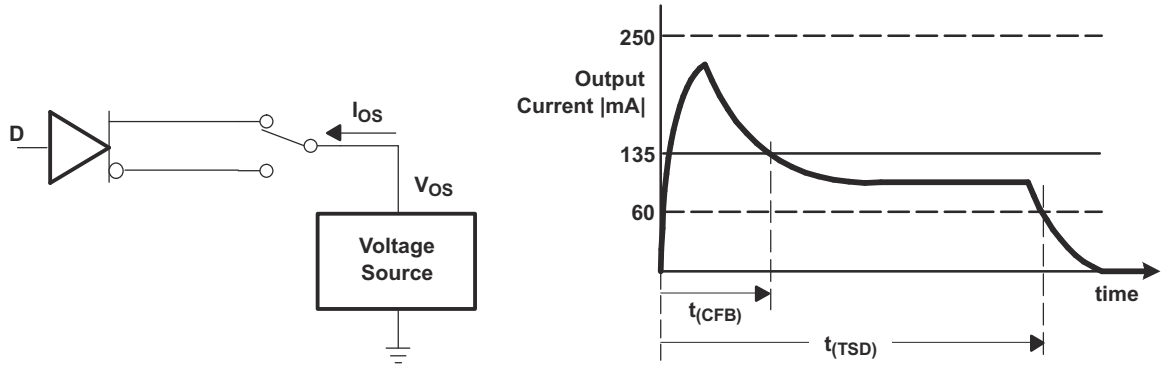

図 7-8. Driver Short-Circuit Test Circuit and Waveforms (Short Circuit applied at Time t = 0)

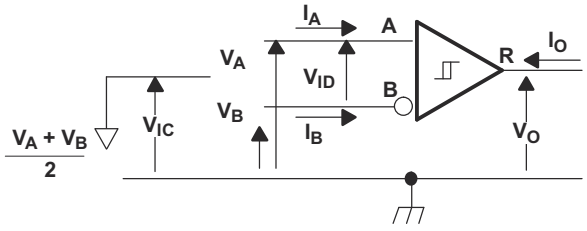

図 7-9. Receiver DC Parameter Definitions

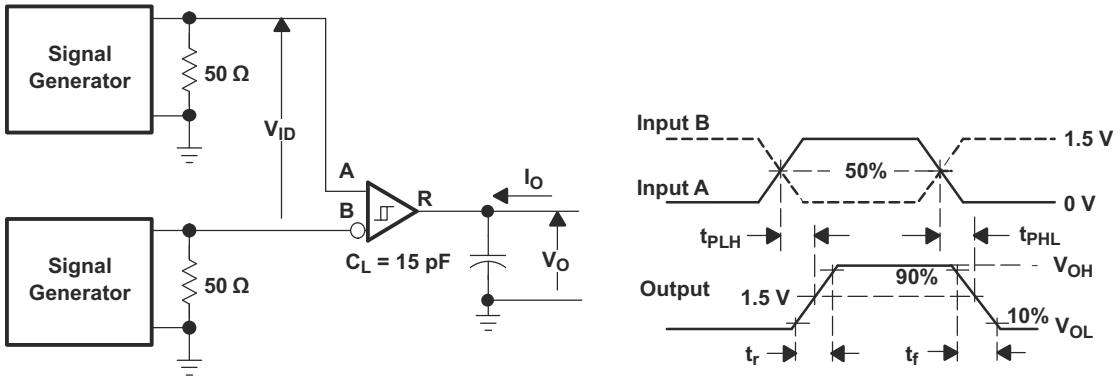

図 7-10. Receiver Switching Test Circuit and Waveforms

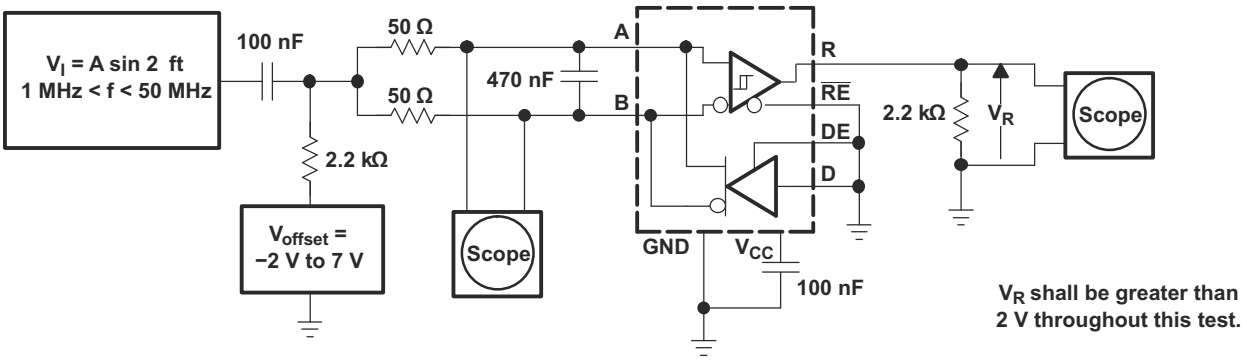

図 7-11. Receiver Common-Mode Rejection Test Circuit

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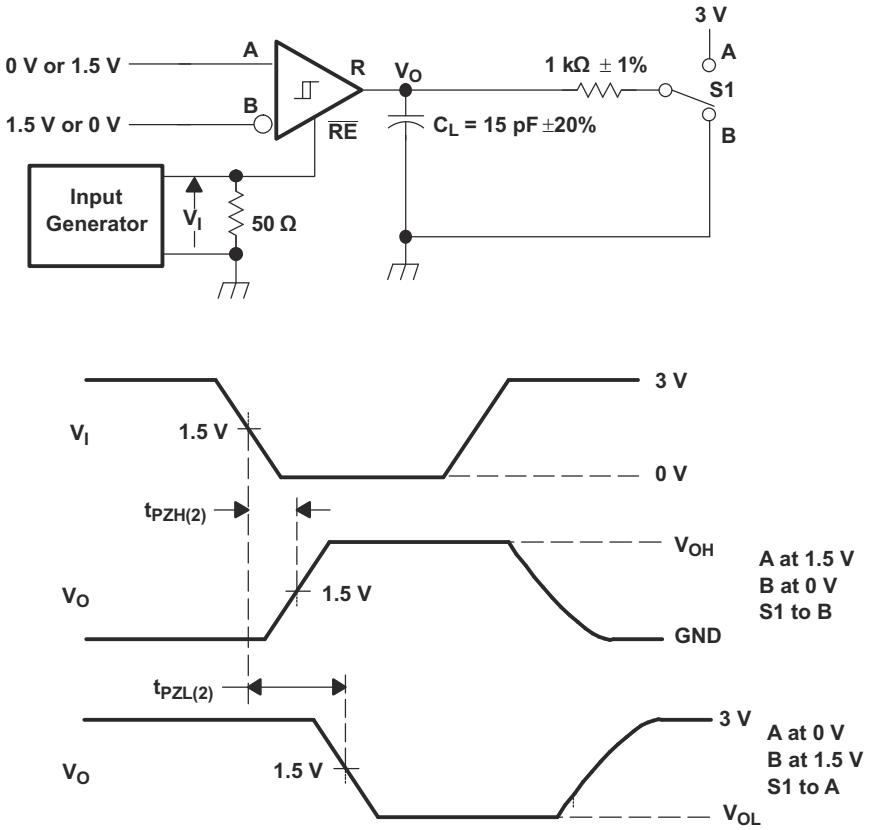

図 7-12. Receiver Enable Time From Standby (Driver Disabled)

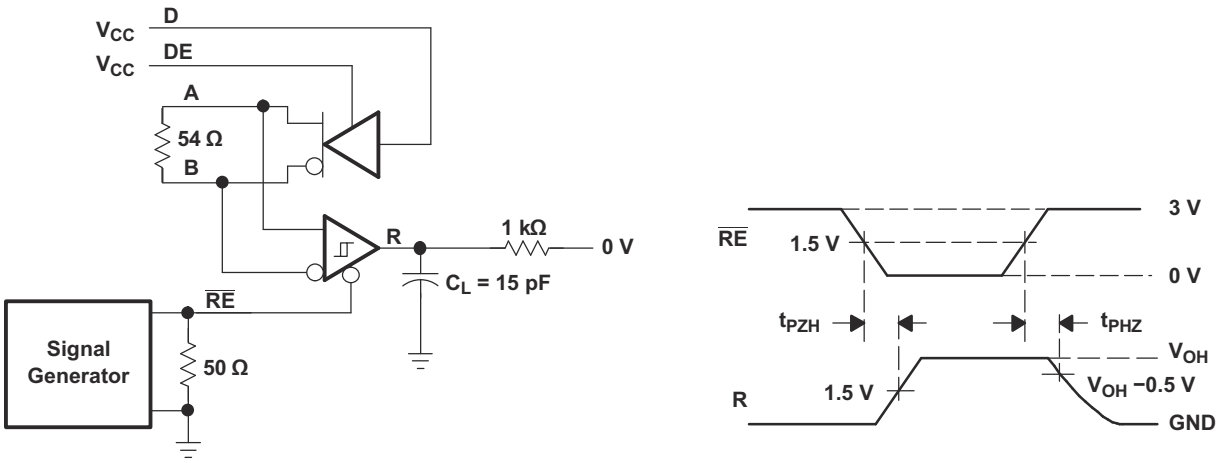

図 7-13. Receiver Enable Test Circuit and Waveforms, Data Output High (Driver Active)

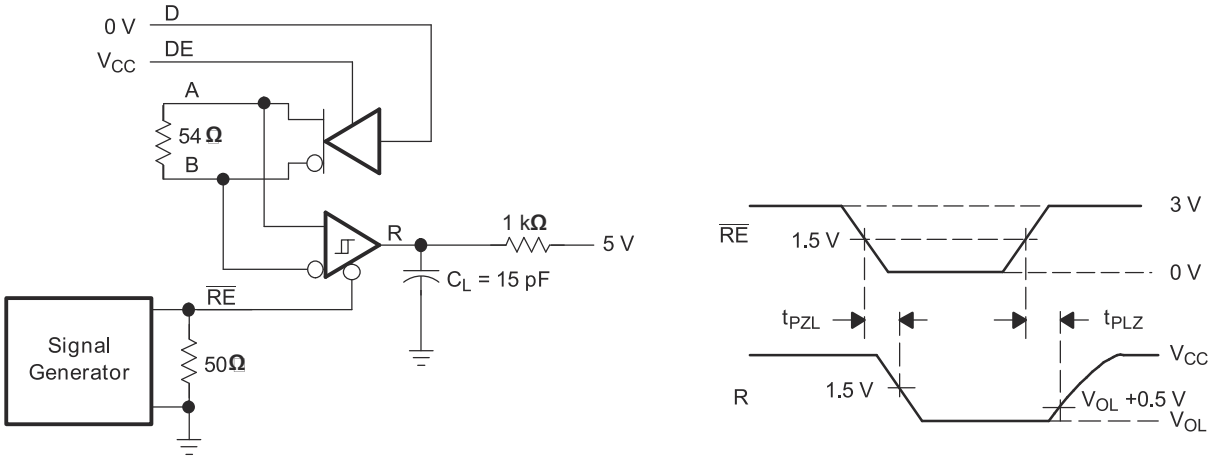

図 7-14. Receiver Enable Test Circuit and Waveforms, Data Output Low (Driver Active)

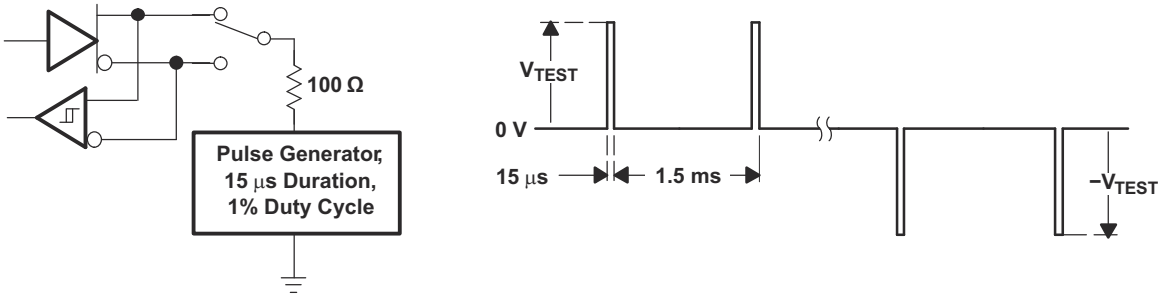

図 7-15. Test Circuit and Waveforms, Transient Overvoltage Test

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7 Detailed Description

7.1 Overview

The SNx5HVD1176 device is a 5-V, half-duplex, RS-485 transceiver optimized for use in PROFIBUS (EN50170) applications and suitable for data transmission up to 40 Mbps.

The driver output differential voltage exceeds the PROFIBUS requirement of 2.1 V with a 54-Ω load, and the low transceiver output capacitance of 10 pF supports the PROFIBUS requirements for maximum bus capacitance across various data rates.

This device has an active-high driver enable and an active-low receiver enable. A standby current of less than 5 µA can be achieved by disabling both driver and receiver.

7.2 Functional Block Diagram

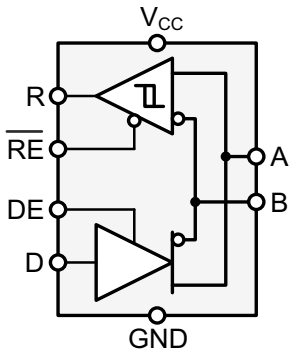

図 7-1. Logic Diagram (Positive Logic)

7.3 Feature Description

Internal ESD protection circuits protect the transceiver bus terminals against ±10-kV Human Body Model (HBM) electrostatic discharges and all other pins up to ±4 kV.

The SN65HVD1176 device provides internal biasing of the receiver input thresholds for open-circuit, bus-idle, or short-circuit failsafe conditions, and a typical receiver hysteresis of 40 mV.

7.4 Device Functional Modes

表 7-1. Driver Function Table(1)

INPUT	ENABLE	OUTPUTS	
D	DE	A	B
H	H	H	L
L	H	L	H
X	L	Z	Z
X	OPEN	Z	Z
OPEN	H	H	L

(1) H = high level, L = low level, X = don't care, Z = high impedance (off)

表 7-2. Receiver Function Table(1)

DIFFRENTIAL INPUT $V_{ID} = (V_A – V_B)$	ENABLE $\overline{RE}$	OUTPUT R
$V_{ID} \geq –0.02$ V	L	H
$–0.2 V < V_{ID} < –0.02$ V	L	?
$V_{ID} \leq –0.2$ V	L	L
X	H	Z

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表 7-2. Receiver Function Table(1) (continued)

DIFFRENTIAL INPUT $V_{ID} = (V_A – V_B)$	ENABLE $\overline{RE}$	OUTPUT R
X	OPEN	Z
Open Circuit	L	H
Short Circuit	L	H
Idle (terminated) bus	L	H

(1) H = high level, L = low level, X = don't care,
Z = high impedance (off), ? = indeterminate

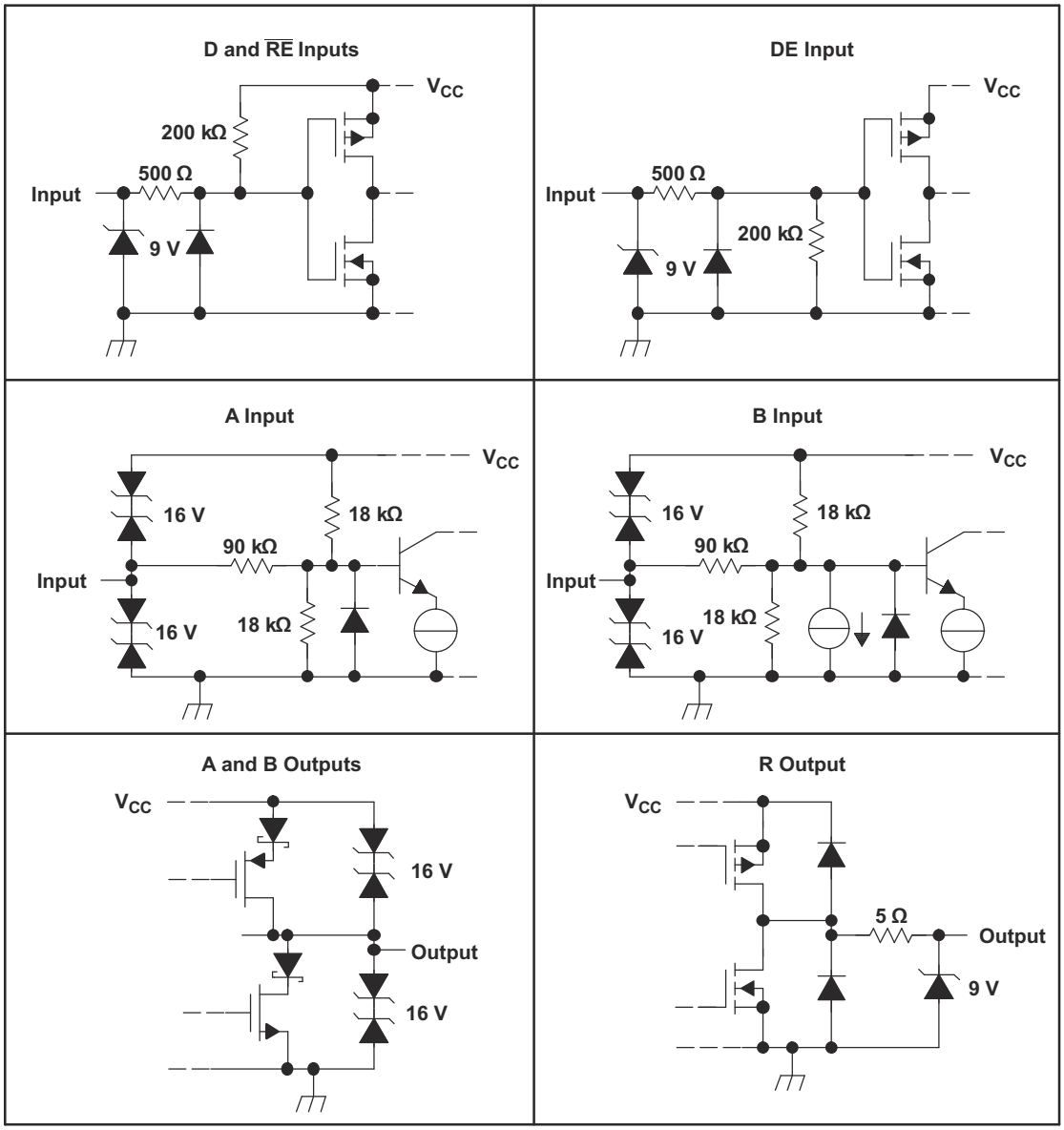

図 7-2. Equivalent Input and Output Schematic Diagrams

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8 Application and Implementation

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8.1 Application Information

The SN65HVD1176 device is a half-duplex RS-485 transceiver commonly used for asynchronous data transmissions. The driver- and receiver-enable pins allow for the configuration of different operating modes.

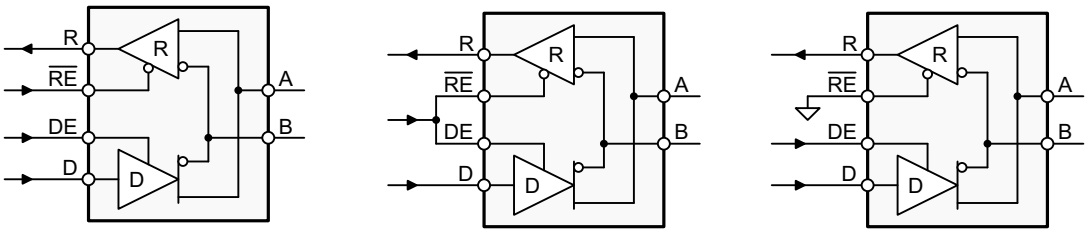

図 8-1. Half-Duplex Transceiver Configurations

Using independent enable lines provides the most flexible control because it allows the driver and the receiver to be turned on and off individually. While this configuration requires two control lines, it allows for selective listening into the bus traffic, whether the driver is transmitting data or not.

Combining the enable signals simplifies the interface to the controller by forming a single direction-control signal. In this configuration, the transceiver operates as a driver when the direction-control line is high and as a receiver when the direction-control line is low.

Additionally, only one line is required when connecting the receiver-enable input to ground and controlling only the driver-enable input. In this configuration, a node receives the data from the bus and the data it sends; the node can also verify that the correct data has been transmitted.

8.2 Typical Application

An RS-485 bus consists of multiple transceivers connecting in parallel to a bus cable. To eliminate line reflections, each cable end is terminated with a termination resistor R_T) whose value matches the characteristic impedance (Z_0) of the cable. This method, known as parallel termination, allows for higher data rates over longer cable length.

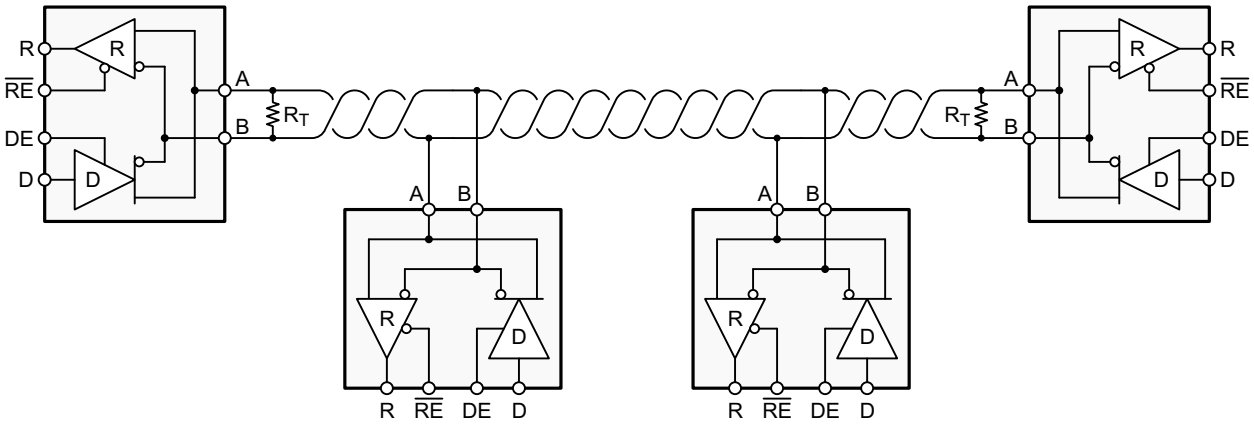

図 8-2. Typical RS-485 Network With Half-Duplex Transceivers

The PROFIBUS standard extends RS-485 by specifying the value of the termination resistor, the characteristic impedance of the bus cable, and the value of fail-safe termination at both ends of the bus.

PROFIBUS requires that 220-Ω termination resistors be placed at both ends of the bus, the bus cable impedance be between 135 Ω and 165 Ω, and that 390-Ω fail-safe resistors be placed on both the A and B lines at both ends of the bus.

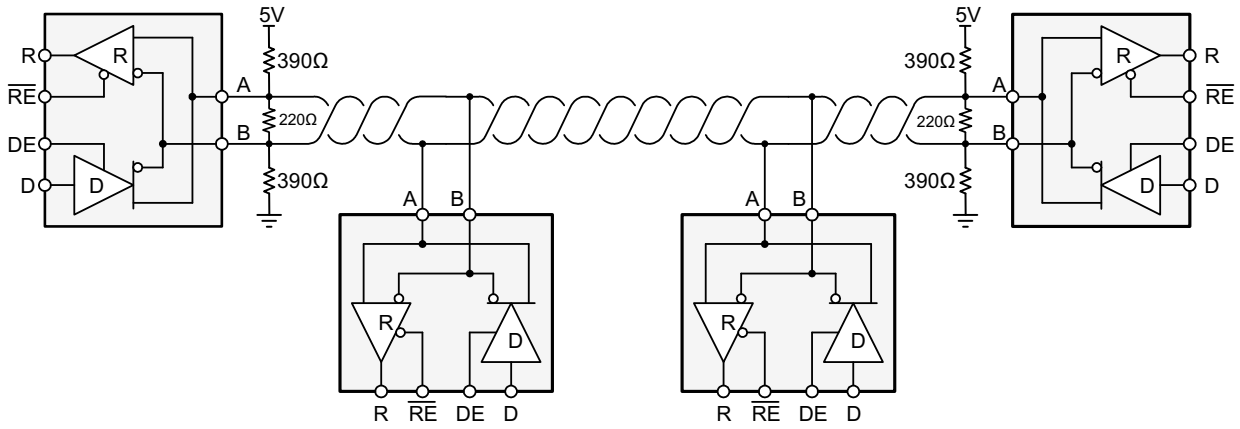

図 8-3. Typical PROFIBUS network

8.2.1 Design Requirements

RS-485 is a robust electrical standard suitable for long-distance networking that may be used in a wide range of applications with varying requirements, such as distance, data rate, and number of nodes.

8.2.1.1 Data Rate and Bus Length

There is an inverse relationship between data rate and bus length, that is, the higher the data rate, the shorter the cable length. Conversely, the lower the data rate, the longer the cable may be without introducing data errors. While most RS-485 systems use data rates between 10 kbps and 100 kbps, some applications require data rates up to 250 kbps at distances of 4000 feet and longer. Longer distances are possible by allowing for small signal jitter of up to 5 or 10%.

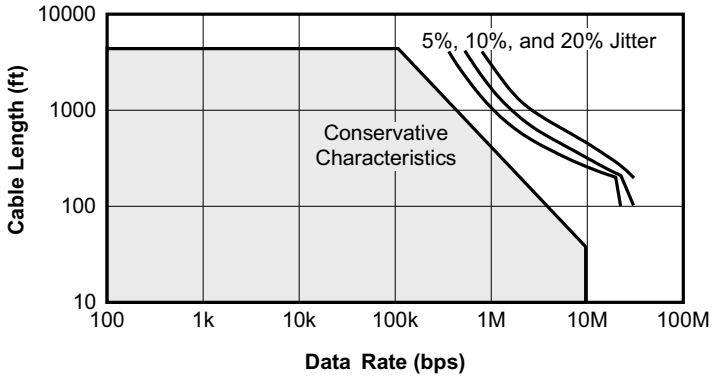

図 8-4. Cable Length vs Data Rate Characteristic

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8.2.1.2 Stub Length

When connecting a node to the bus, the distance between the transceiver inputs and the cable trunk, known as the stub, should be as short as possible. Stubs present a nonterminated piece of bus line which can introduce reflections as the length of the stub increases. As a general guideline, the electrical length, or round-trip delay, of a stub should be less than one-tenth of the rise time of the driver, thus giving a maximum physical stub length as shown in 式 1.

$$L_{stub} \leq 0.1 \times t_r \times v \times c \quad (1)$$

where:

t_r is the 10/90 rise time of the driver
c is the speed of light (3×10^8 m/s)
v is the signal velocity of the cable or trace as a factor of c

Per 式 1, the maximum recommended stub length for the minimum driver output rise time of the SN65HVD1176 device for a signal velocity of 78% is 0.05 meters (0.16 feet).

8.2.1.3 Bus Loading

The RS-485 standard specifies that a compliant driver must be able to driver 32 unit loads (UL), where 1 unit load represents a load impedance of approximately 12 kΩ. Because the SN65HVD1176 device is a 1/5 UL transceiver, it is possible to connect up to 160 receivers to the bus.

8.2.1.4 Receiver Failsafe

The differential receiver of the SN65HVD1176 device is *failsafe* to invalid bus states caused by the following:

- Open bus conditions, such as a disconnected connector
- Shorted bus conditions, such as cable damage shorting the twisted-pair together
- Idle bus conditions that occur when no driver on the bus is actively driving

In any of these cases, the differential receiver will output a failsafe logic-high state so that the output of the receiver is not indeterminate.

Receiver failsafe is accomplished by offsetting the receiver thresholds such that the input-indeterminate range does not include zero volts differential.

To comply with the RS-422 and RS-485 standards, the receiver output must output a high when the differential input VID is more positive than +200 mV, and must output a low when V_{ID} is more negative than –200 mV. The receiver parameters that determine the fail-safe performance are $V_{IT(+)}$ and $V_{IT(–)}$.

As shown in セクション 6.5, differential signals more negative than –200 mV will always cause a low receiver output, and differential signals more positive than –20 mV will always cause a high receiver output. Thus, when the differential input signal is close to zero, it is still above the maximum $V_{IT(+)}$ threshold of –20 mV, and the receiver output will be high.

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8.2.2 Detailed Design Procedure

To protect bus nodes against high-energy transients, the implementation of external transient protection devices is necessary.

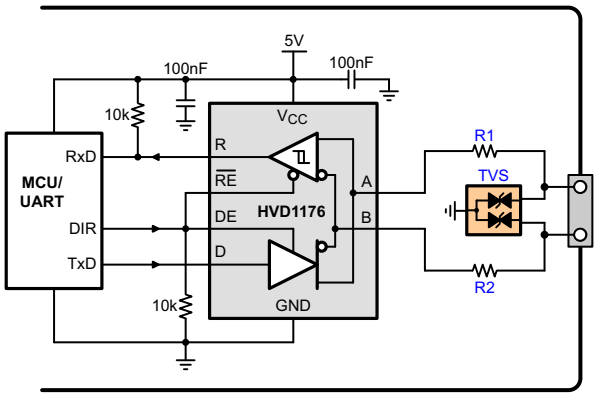

図 8-5. Transient Protection Against ESD, EFT, and Surge Transients

図 8-5 shows a protection circuit against 10-kV ESD (IEC 61000-4-2), 4-kV EFT (IEC 61000-4-4), and 1-kV surge (IEC 61000-4-5) transients. 表 8-1 lists the associated Bill of Materials.

表 8-1. Bill of Materials

Device	Function	Order Number	Manufacturer
XCVR	5-V, 40-Mbps ProfiBus Transceiver	SN65HVD1176	TI
R1, R2	10-Ω, Pulse-Proof Thick-Film Resistor	CRCW0603010RJNEAHP	Vishay
TVS	Bidirectional 400-W Transient Suppressor	CDSOT23-SM712	Bourns

8.2.3 Application Curve

図 8-6 demonstrates operation of the SN65HVD1179 at a signaling rate of 40 Mbps.

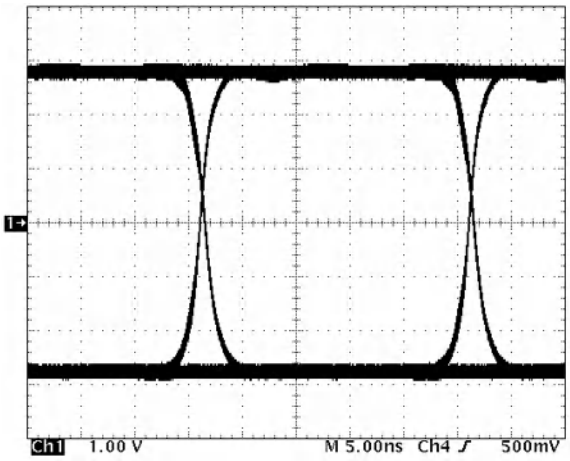

図 8-6. Differential Output of SN65HVD1176 Operation at 40 Mbps

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9 Power Supply Recommendations

To ensure reliable operation at all data rates and supply voltages, each supply must be buffered with a 100-nF ceramic capacitor located as close to the supply pins as possible. The TPS76350 device is a linear voltage regulator suitable for the 5-V supply.

10 Layout

10.1 Layout Guidelines

On-chip IEC-ESD protection is sufficient for laboratory and portable equipment but insufficient for EFT and surge transients occurring in industrial environments. Therefore, robust and reliable bus-node design requires the use of external transient protection devices.

Because ESD and EFT transients have a wide frequency bandwidth from approximately 3 MHz to 3 GHz, high frequency layout techniques must be applied during PCB design.

1. Place the protection circuitry close to the bus connector to prevent noise transients from entering the board.
2. Use VCC and ground planes to provide low-inductance.
3. Design the protection components into the direction of the signal path. Do not force the transient currents to divert from the signal path to reach the protection device.
4. Apply 100-nF to 220-nF bypass capacitors as close as possible to the VCC pins of the transceiver, the UART, or the controller ICs on the board.
5. Use at least two vias for VCC and ground connections of bypass capacitors and protection devices to minimize effective via inductance.
6. Use 1-kΩ to 10-kΩ pullup and pulldown resistors for enable lines to limit noise currents in these lines during transient events.
7. Insert series pulse-proof resistors into the A and B bus lines if the TVS clamping voltage is higher than the specified maximum voltage of the transceiver bus terminals. These resistors limit the residual clamping current into the transceiver and prevent it from latching up.
8. While pure TVS protection is sufficient for surge transients up to 1 kV, higher transients require metal-oxide varistors (MOVs) that reduce the transients to a few hundred volts of clamping voltage and transient blocking units (TBUs) that limit transient current to less than 1 mA.

10.2 Layout Example

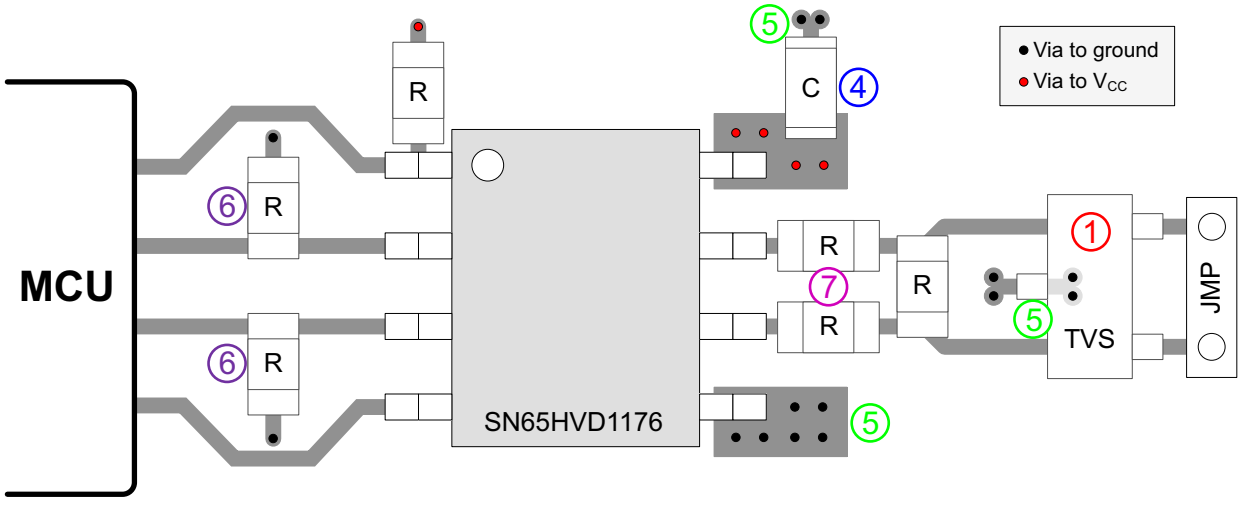

図 10-1. SNx5HVD08 Layout Example

11 Device and Documentation Support

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11.2 Documentation Support

For related documentation see the following: *ISO1176 ISOLATED RS-485 PROFIBUS TRANSCEIVER* (SLLS897)

11.3 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

表 11-1. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN65HVD1176	Click here	Click here	Click here	Click here	Click here
SN75HVD1176	Click here	Click here	Click here	Click here	Click here

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11.7 用語集

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable part number	Status (1)	Material type (2)	Package | Pins	Package qty | Carrier	RoHS (3)	Lead finish/ Ball material (4)	MSL rating/ Peak reflow (5)	Op temp (°C)	Part marking (6)
SN65HVD1176D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	-40 to 85	VP1176
SN65HVD1176DR	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP1176
SN65HVD1176DR.A	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP1176
SN65HVD1176DRG4	Active	Production	SOIC (D) | 8	2500 | LARGE T&R	Yes	NIPDAU	Level-1-260C-UNLIM	-40 to 85	VP1176
SN75HVD1176D	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	VN1176
SN75HVD1176DR	Obsolete	Production	SOIC (D) | 8	-	-	Call TI	Call TI	0 to 70	VN1176

(1) **Status:** For more details on status, see our product life cycle.

(2) **Material type:** When designated, preproduction parts are prototypes/experimental devices, and are not yet approved or released for full production. Testing and final process, including without limitation quality assurance, reliability performance testing, and/or process qualification, may not yet be complete, and this item is subject to further changes or possible discontinuation. If available for ordering, purchases will be subject to an additional waiver at checkout, and are intended for early internal evaluation purposes only. These items are sold without warranties of any kind.

(3) **RoHS values:** Yes, No, RoHS Exempt. See the TI RoHS Statement for additional information and value definition.

(4) **Lead finish/Ball material:** Parts may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

(5) **MSL rating/Peak reflow:** The moisture sensitivity level ratings and peak solder (reflow) temperatures. In the event that a part has multiple moisture sensitivity ratings, only the lowest level per JEDEC standards is shown. Refer to the shipping label for the actual reflow temperature that will be used to mount the part to the printed circuit board.

(6) **Part marking:** There may be an additional marking, which relates to the logo, the lot trace code information, or the environmental category of the part.

Multiple part markings will be inside parentheses. Only one part marking contained in parentheses and separated by a "~" will appear on a part. If a line is indented then it is a continuation of the previous line and the two combined represent the entire part marking for that device.

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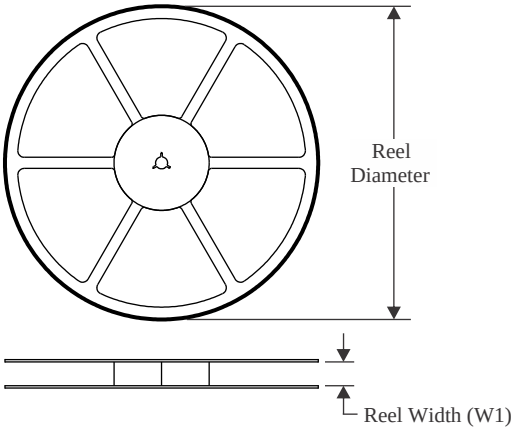
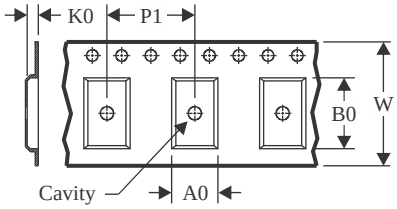
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

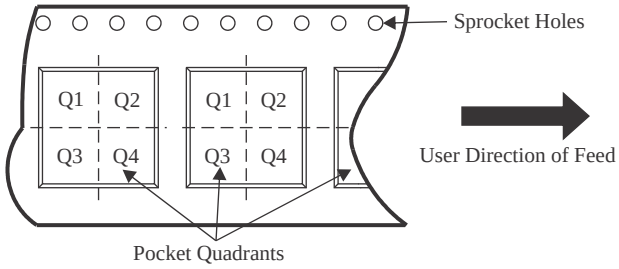


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

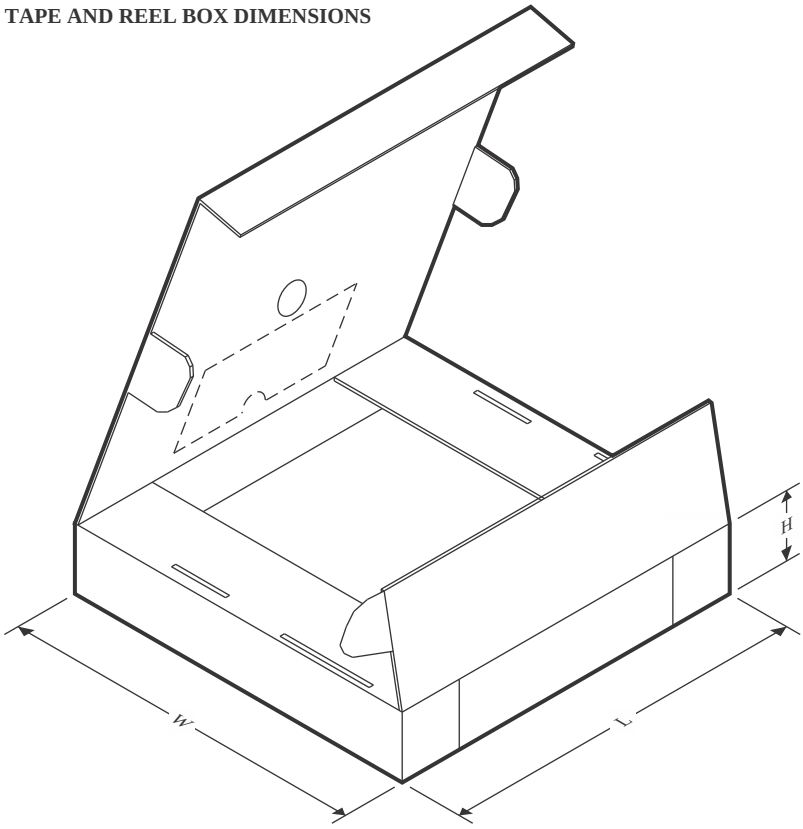
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

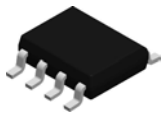
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN65HVD1176DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN65HVD1176DR	SOIC	D	8	2500	353.0	353.0	32.0

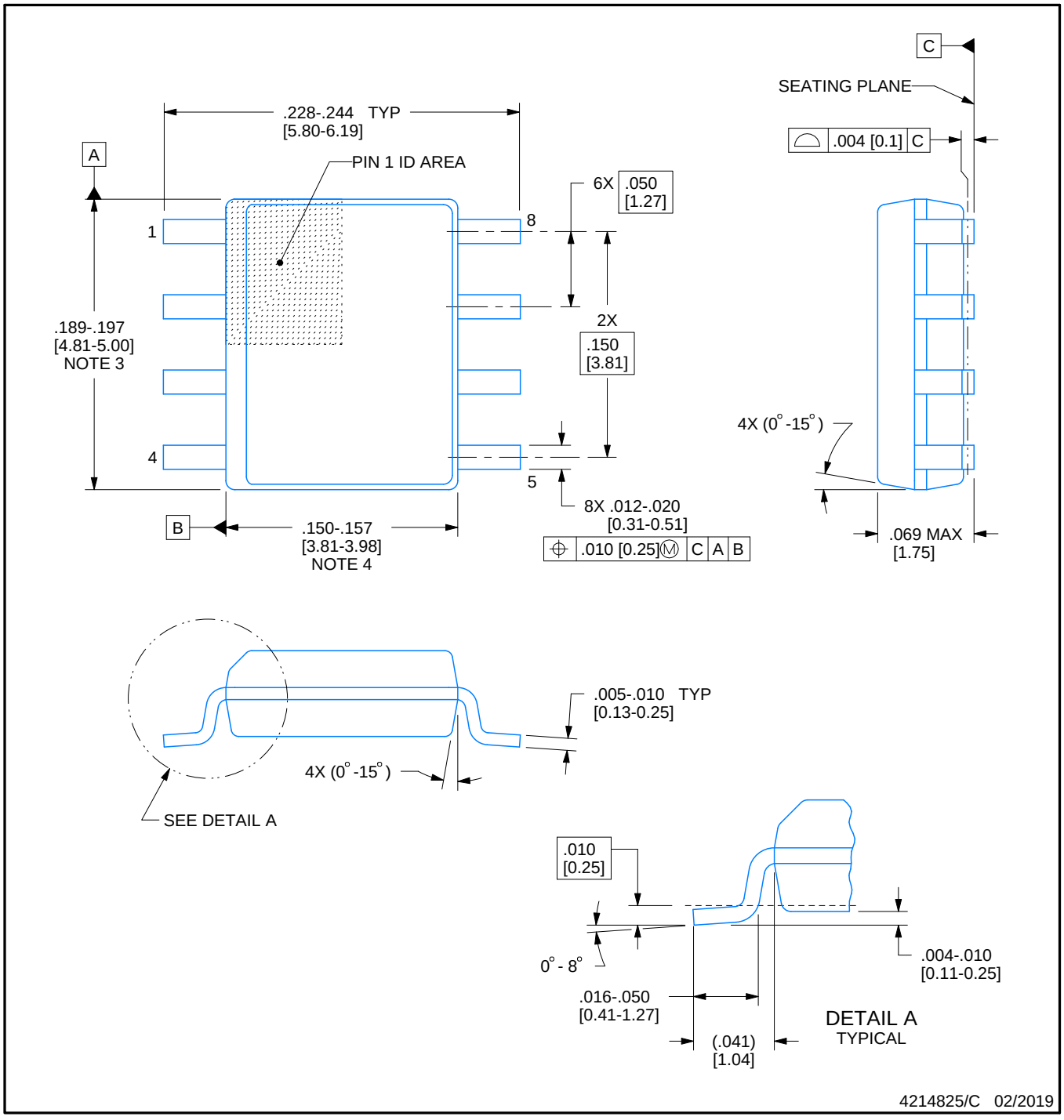


PACKAGE OUTLINE

D0008A

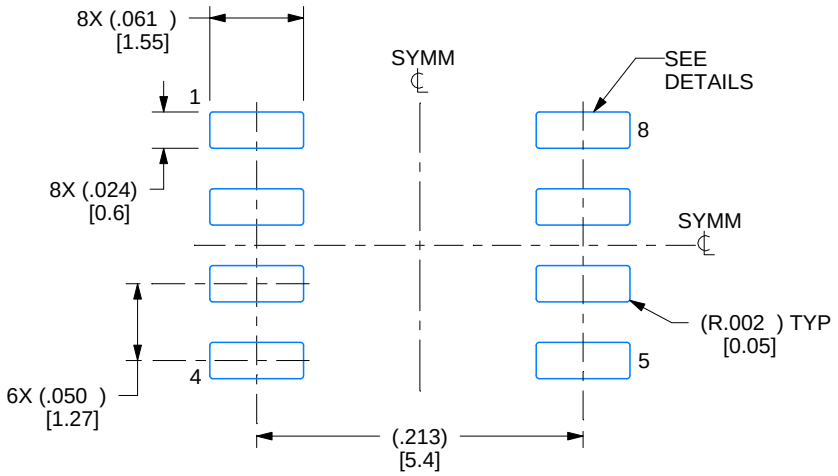
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

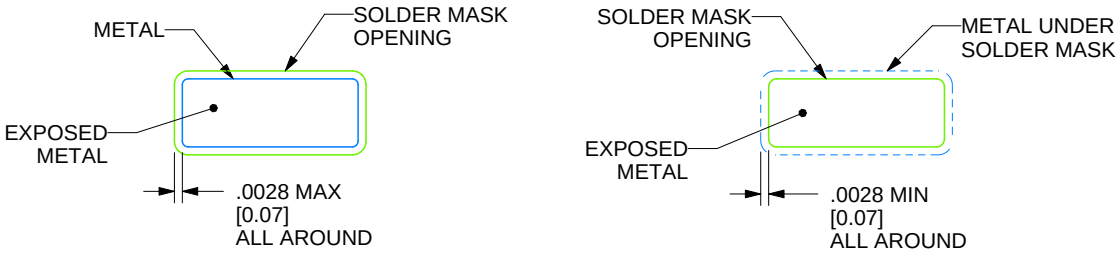


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

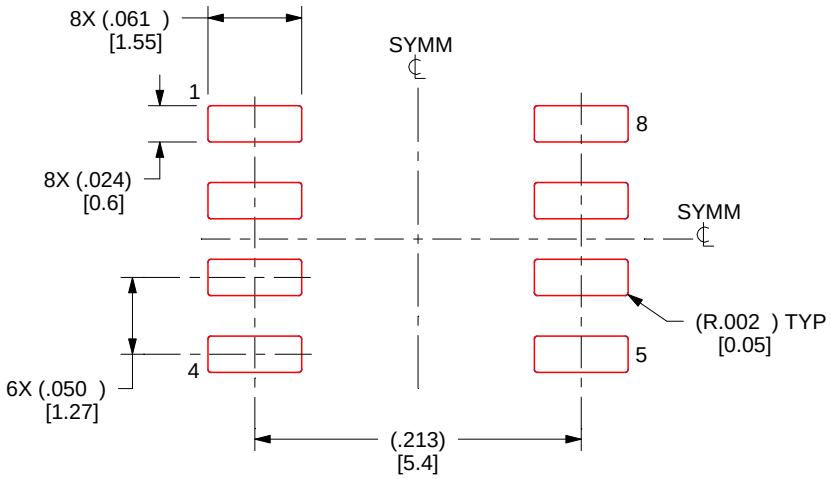
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

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NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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