Selecting output caps for buck converters based on Z_{out} and load slew rates

By Brian Cheng, *Member Group Technical Staff, Systems, Applications and Marketing Manager* **Bob Neidorff,** *TI Fellow, DC-DC Converter IC Design*

Introduction

With a growing demand for mobile devices, servers, storage and telecommunication equipment, and cloud-computing infrastructures, there is a need for more computing power, greater efficiency and higher power densities. Microprocessors inside the equipment determine the power requirements and buck converters for powering these microprocessors are key to improving load-transient performance.

Figure 1 shows the load-transient profiles for an Intel processor under different operating conditions. The variable load frequencies and fast load slew rates normally require high-frequency decoupling capacitors for a multiphase buck converter, as shown in Figure 2. In the traditional design approach, the required total output capacitance can be roughly estimated based on the overshoot requirements.^[1] However, different types of capacitors have different equivalent series resistance (ESR), cost and size, so there are many possible implementations that give the same capacitance, but have different performance. To date, there are no clear design guidelines to explain how to select the combinations of different types of output capacitors based on the load-transient profiles. This article explains how the loadtransient performance unique to fast load slew rates can be impacted with different output-capacitor choices and how to arrive at an optimal solution.

Figure 1. Dynamic operation modes for an Intel processor generating different loads to multiphase buck converters







Power

Frequency analysis of a load profile with different load slew rates

Adopting a trapezoidal load profile will emulate the load currents from a microprocessor during operations, as shown in Figure 3. By applying Fourier transformations to the trapezoidal load waveform, the load profile can be represented as Equation 1, with Figure 3b illustrating its spectrum. As shown in Figure 3b, in addition to the fundamental load frequency, there are many harmonic components caused by different load frequencies, duty ratios and slew rates. These harmonics may cause additional voltage deviations during load transients based on the output impedance at high-frequencies.

Figure 4a shows two load profiles with the same load frequency (10 kHz) and duty ratios (50%), but with different slew rates (450 A/µs and 22.5 A/µs). Based on Equation 1, Figure 4b shows the spectrums of the two load profiles. These curves show that the high-frequency harmonic components are well attenuated, with the slower load slew rate due to a second pole at a lower frequency.



Figure 3. Trapezoidal load profile and spectrum



Figure 4. 10-kHz load transients with a 225-A step at fast and slow slew rates



There are several types of capacitors, such as an OS-CON, polymer aluminum or ceramic, each with different characteristics.^[2] Figure 5 shows the impedance curves of different capacitor types and ratings. Note that different capacitors can provide different impedances over frequency, so it is important to understand the output-impedance requirements of a buck converter to select the corresponding capacitor types and ratings.

For example, if the plot for impedance versus frequency shows an impedance that's too high between 100 kHz and 500 kHz, then the most effective way to lower that impedance is with a capacitor that has a resonant frequency of 500 kHz, such as the 220-µF ceramic capacitor shown in Figure 5. On the other hand, if cost concerns make an OC-CON capacitor preferable, there are two options to reduce the impedance: 1) Use parallel multiple OS-CON capacitors to lower the overall equivalent series resistance, or 2) add ceramic capacitors with a lower resonant frequency, such as a 220-µF ceramic capacitor with a 500-kHz resonant frequency.

Table 1 illustrates the critical design parameters and requirements of a multiphase buck converter powering a microprocessor.

Table 1. Design requirements and parameters

Design Requirements			
Input voltage (V)	12 V ±10%		
Output voltage (V)	0.885 V		
Maximum load current (A)	450 A		
Maximum load step (A) and slew rate (A/ μs)	225 A at 500 A/µs		
Undershoot/overshoot requirements (mV)	±22.5 mV		
Design Parameters			
Selected phase numbers	12		
Selected inductance (nH)	150 nH		
Selected switching frequency (kHz)	400 kHz		
Estimated minimum output capacitance based on charge balance calculations	24,000 µ F		



Figure 6 shows a simplified power delivery network (PDN) comprised of different types of output capacitors and the printed circuit board parasitic.

Table 2 shows two design examples of C_{out} selections having a similar total capacitance but different open-loop output impedances.

Table 2. Design examples of C_{out} selections

Design Example No. 1			
ltem	Туре	Quantity	Effective Capacitance (µF)
C ₀₁	470- μ F/6-m Ω SP capacitor	24	11,160
C ₀₂	220-µF ceramic capacitor	48	10,080
C ₀₃	100-µF ceramic capacitor	36	2,916
Total o	apacitance (μF)		24,156
Design Example No. 2			
ltem	Туре	Quantity	Effective Capacitance (µF)
C ₀₁	560- μ F/9-m Ω OS-CON capacitor	20	11,200
C ₀₂	560- μ F/9-m Ω OS-CON capacitor	21	11,760
C ₀₃	22-µF ceramic capacitor	68	1,224
Total c	apacitance (µF)		24,184

Figure 7 shows the closed-loop output impedance of both design examples with compensations. The lowfrequency (<100 kHz) and very-high-frequency (>2 MHz) closed-loop output impedances are similar for both design



examples. However, the mid- to high-frequency (between 100 kHz to 1 MHz) output impedances are quite different, which will lead to different load-transient performance, even when the load frequency is low; recall the harmonic components of the load profile shown in Figure 4. Equation 2 estimates the output-voltage deviations due to load transients as:

$$\Delta V_{out}(f) = I_{load}(f) \times Z_{out}(f)$$
⁽²⁾

Therefore, the load profile shown in Figure 4 and the closed-loop output impedance shown in Figure 7 will determine the output-voltage deviations at different load frequencies.



Figure 6. Simplified PDN of a multiphase

Analog Design Journal

Figure 8 shows the load-transient performance of two design examples with 10-kHz repetitive load transients, 225-A load steps and two load slew rates (450 A/us and 22.5 A/us). The loadtransient performance is worse with design example No. 2 even though the total capacitances are almost the same for both cases. This is because of the harmonic components of the load profile in the mid frequency ranges (100 kHz to 1 MHz), as was explained for Figure 4b. The loadtransient performance of the two design examples are almost identical when reducing the load slew rate as shown in Figure 8b. This is not surprising given the attenuated harmonic components of the load profile shown in Figure 4b.

Conclusion

There are clear relationships between the frequency spectrum of the load-transient profile, the load-transient performance and the output impedance. For powering different microprocessors, the loadtransient profile (load steps, frequency ranges, duty ratios and slew rates) as well as the load-transient requirements (undershoot and overshoot) can differ. It is important to know how to select output capacitors based on analysis of the loadtransient profile and output impedance. This relationship is critical to fulfill the undershoot/overshoot specifications, especially for the advanced processors with very-fast load slew rates.

References

- Jason Arrigo, "Input and output capacitor selection," Texas Instruments Application Report (SLTA055), February 2006.
- Michael Score, "Ceramic or electrolytic output capacitors in DC/DC converters – Why not both?," Texas Instruments Analog Applications Journal (SLYT639), 3Q 2015.





TI Worldwide Technical Support

TI Support

Thank you for your business. Find the answer to your support need or get in touch with our support center at

www.ti.com/support

- China: http://www.ti.com.cn/guidedsupport/cn/docs/supporthome.tsp
- Japan: http://www.tij.co.jp/guidedsupport/jp/docs/supporthome.tsp

Technical support forums

Search through millions of technical questions and answers at TI's E2E™ Community (engineer-to-engineer) at

e2e.ti.com China: http://www.deyisupport.com/ Japan: http://e2e.ti.com/group/jp/

TI Training

From technology fundamentals to advanced implementation, we offer on-demand and live training to help bring your next-generation designs to life. Get started now at

training.ti.com

- China: http://www.ti.com.cn/general/cn/docs/gencontent.tsp?contentId=71968
- Japan: https://training.ti.com/jp

Important Notice: The products and services of Texas Instruments Incorporated and its subsidiaries described herein are sold subject to TI's standard terms and conditions of sale. Customers are advised to obtain the most current and complete information about TI products and services before placing orders. TI assumes no liability for applications assistance, customer's applications or product designs, software performance, or infringement of patents. The publication of information regarding any other company's products or services does not constitute TI's approval, warranty or endorsement thereof.

A011617

E2E is a trademark of Texas Instruments. All other trademarks are the property of their respective owners.

© 2019 Texas Instruments Incorporated. All rights reserved.



SLYT766

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265 Copyright © 2019, Texas Instruments Incorporated