TPS22975 5.7V、6A、16mΩオン抵抗負荷スイッチ

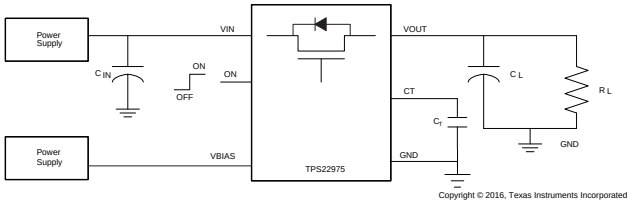
1 特長

- シングル・チャネル負荷スイッチを内蔵
- 入力電圧範囲: 0.6V～V_{BIAS}
- V_{BIAS}電圧範囲: 2.5V～5.7V
- オン抵抗(R_{ON})
  - VIN = 0.6V～5.7V、V_{BIAS} = 5.7Vで R_{ON} = 16mΩ (標準値)
- 最大連続スイッチ電流: 6A
- 低い静止電流
  - V_{IN} = V_{BIAS} = 5Vにおいて37µA (標準値)
- 制御入力スレッショルドが低いため、1.2V、1.8V、2.5V、3.3Vロジックを使用可能
- 立ち上がり時間を構成可能
- サーマル・シャットダウン
- クイック出力放電(QOD) (オプション)
- サーマル・パッドを搭載したSON 8ピン・パッケージ
- JESD 22に従ってESD性能をテスト済み
  - HBM 2000V、CDM 1000V

2 アプリケーション

- Ultrabook™
- ノートPCおよびネットブック
- タブレットPC
- コンシューマ・エレクトロニクス
- セットトップ・ボックス、住居用ゲートウェイ
- テレコム・システム
- ソリッド・ステート・ドライブ(SSD)

概略回路図



3 概要

TPS22975製品ファミリは、TPS22975とTPS22975Nの2つのデバイスで構成されます。いずれのデバイスもシングル・チャネルの負荷スイッチで、立ち上がり時間を構成して突入電流を最小化できます。このデバイスにはNチャネルMOSFETが搭載され、0.6V～ 5.7Vの入力電圧範囲で動作し、最大で6Aの連続電流をサポートできます。スイッチはオン/オフ入力(ON)により制御され、低電圧の制御信号と直接接続が可能です。TPS22975には、スイッチがオフになったときにクイック出力放電を行うため、230Ωのオンチップ負荷抵抗をオプションで搭載できます。

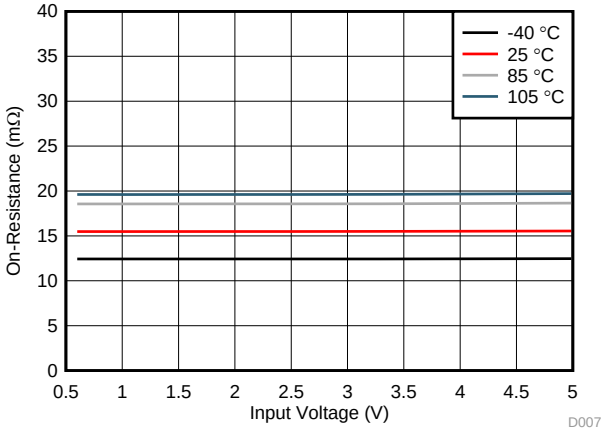
TPS22975は小型で省スペースの2mm×2mm 8ピンのSONパッケージ(DSG)で供給され、大きな消費電力に対応できるようサーマル・パッドが搭載されています。このデバイスは、自由通気で-40℃～+105℃の温度範囲で動作するよう規定されています。

製品情報(1)

型番	パッケージ	本体サイズ(公称)
TPS22975 TPS22975N	WSON (8)	2.00mm×2.00mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

オン抵抗と入力電圧との関係



V_{BIAS} = 5V、I_{VOUT} = –200mA

目次

4 改訂履歴

Revision A (June 2016) から **Revision B** に変更 **Page**

- Updated V_{IH} in *Recommended Operating Conditions* ... 4

2016年5月発行のものから更新 **Page**

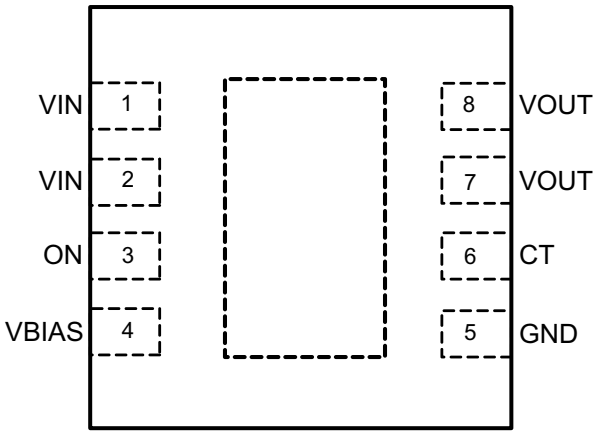
- デバイスのステータスを*製品プレビュー*から*量産データ*へ変更 ... 1

5 Device Comparison Table

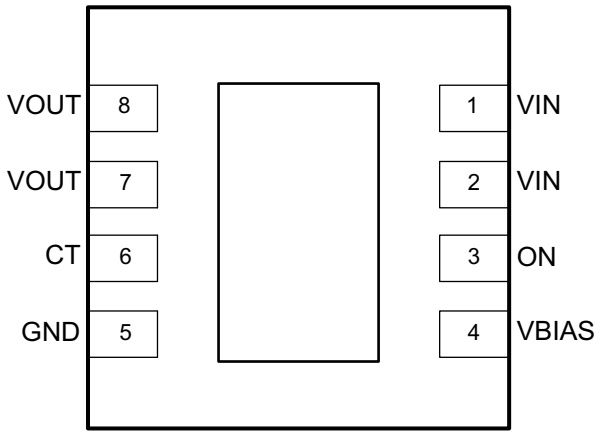
DEVICE	R_{ON} AT V_{IN} = V_{BIAS} = 5 V (TYPICAL)	QUICK-OUTPUT DISCHARGE	MAXIMUM OUTPUT CURRENT	ENABLE
TPS22975	16 mΩ	Yes	6 A	Active high
TPS22975N	16 mΩ	No	6 A	Active high

6 Pin Configuration and Functions

DSG Package
8-Pin (WSON)
Top View



DSG Package
8-Pin (WSON)
Bottom View



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	VIN	I	Switch input. Input bypass capacitor recommended for minimizing V_{IN} dip. Must be connected to Pin 1 and Pin 2. See the *Application and Implementation* section for more information
2			
3	ON	I	Active high switch control input. Do not leave floating
4	VBIAS	I	Bias voltage. Power supply to the device. Recommended voltage range for this pin is 2.5 V to 5.7 V. See the *Application and Implementation* section for more information
5	GND	—	Device ground
6	CT	O	Switch slew rate control. Can be left floating. See the *Adjustable Rise Time* section under *Feature Description* for more information
7	VOUT	O	Switch output
8			
—	Thermal Pad	—	Thermal pad (exposed center pad) to alleviate thermal stress. Tie to GND. See the *Layout Example* section for layout guidelines

7 Specifications

7.1 Absolute Maximum Ratings

Over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{IN}	Input voltage	–0.3	6	V
V_{OUT}	Output voltage	–0.3	6	V
V_{BIAS}	Bias voltage	–0.3	6	V
V_{ON}	On voltage	–0.3	6	V
I_{MAX}	Maximum continuous switch current		6	A
I_{PLS}	Maximum pulsed switch current, pulse < 300 µs, 2% duty cycle		8	A
T_J	Maximum junction temperature		125	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1000	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

7.3 Recommended Operating Conditions

			MIN	MAX	UNIT
V_{IN}	Input voltage		0.6	V_{BIAS}	V
V_{BIAS}	Bias voltage		2.5	5.7	V
V_{ON}	ON voltage		0	5.7	V
V_{OUT}	Output voltage			V_{IN}	V
V_{IH}	High-level input voltage, ON	V_{BIAS} = 2.5 V to 5 V, T_A< 85°C	1.05	5.7	V
		V_{BIAS} = 2.5 V to 5 V, T_A< 105°C	1.1	5.7	
		V_{BIAS} = 5 V to 5.7 V, T_A< 105°C	1.2	5.7	
V_{IL}	Low-level input voltage, ON	V_{BIAS} = 2.5 V to 5.7 V	0	0.5	V
C_{IN}	Input capacitor		1(1)		µF
T_A	Operating free-air temperature(1)(2)		–40	105	°C

(1) See the *Application Information* section.
(2) In applications where high power dissipation and-or poor package thermal resistance is present, the maximum ambient temperature may have to be derated and device lifetime may be affected. Maximum ambient temperature ($T_{A(max)}$) is dependent on the maximum operating junction temperature ($T_{J(max)}$), the maximum power dissipation of the device in the application ($P_{D(max)}$), and the junction-to-ambient thermal resistance of the part-package in the application (θ_{JA}), and can be approximated by the following equation: $T_{A\ (max)} = T_{J(max)} – (\theta_{JA} \times P_{D(max)})$.

7.4 Thermal Information

THERMAL METRIC(1)		TPS22975 DSG (WSON) 8 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	74.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	81	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	44.7	°C/W
ψ_{JT}	Junction-to-top characterization parameter	3.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	45.1	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	16.4	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

7.5 Electrical Characteristics—V_{BIAS} = 5 V

Unless otherwise noted, the specifications in the following table applies where V_{BIAS} = 5 V. Typical values are for T_A = 25 °C.

PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{Q, VBIAS}$	V_{BIAS} quiescent current	I_{OUT} = 0 A, V_{IN} = V_{ON} = 5 V		–40°C to +105°C		37	45	µA
$I_{SD, VBIAS}$	V_{BIAS} shutdown current	V_{ON} = V_{OUT} = 0 V		–40°C to +105°C			2.3	µA
$I_{SD, VIN}$	V_{IN} off-state supply current	V_{ON} = V_{OUT} = 0 V	V_{IN} = 5 V	–40°C to +85°C		0.005	5	µA
				–40°C to +105°C			10	
			V_{IN} = 3.3 V	–40°C to +85°C		0.002	1.5	
				–40°C to +105°C			3.5	
			V_{IN} = 1.8 V	–40°C to +85°C		0.002	1	
				–40°C to +105°C			2	
			V_{IN} = 0.6 V	–40°C to +85°C		0.001	0.5	
				–40°C to +105°C			1	
I_{ON}	On-pin input leakage current	V_{ON} = 5.5 V		–40°C to +105°C			0.1	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	On-resistance	I_{OUT} = –200 mA	V_{IN} = 5 V	25°C		16	19	mΩ
				–40°C to +85°C			23	
				–40°C to +105°C			25	
			V_{IN} = 3.3 V	25°C		16	19	
				–40°C to +85°C			23	
				–40°C to +105°C			25	
			V_{IN} = 1.8 V	25°C		16	19	
				–40°C to +85°C			23	
				–40°C to +105°C			25	
			V_{IN} = 1.5 V	25°C		16	19	
				–40°C to +85°C			23	
				–40°C to +105°C			25	
			V_{IN} = 1.05 V	25°C		16	19	
				–40°C to +85°C			23	
				–40°C to +105°C			25	
			V_{IN} = 0.6 V	25°C		16	19	
				–40°C to +85°C			23	
				–40°C to +105°C			25	
$V_{ON, HYS}$	On-pin hysteresis	V_{IN} = 5 V		25°C		120		mV
R_{PD} (1)	Output pulldown resistance	V_{IN} = 5 V, V_{ON} = 0 V		–40°C to +105°C		230	300	Ω
T_{SD}	Thermal shutdown	Junction temperature rising				160		°C
$T_{SD, HYS}$	Thermal shutdown hysteresis	Junction temperature falling				20		°C

(1) TPS22975 only

7.6 Electrical Characteristics—V_{BIAS} = 2.5 V

Unless otherwise noted, the specifications in the following table applies where V_{BIAS} = 2.5 V. Typical values are for T_A = 25 °C.

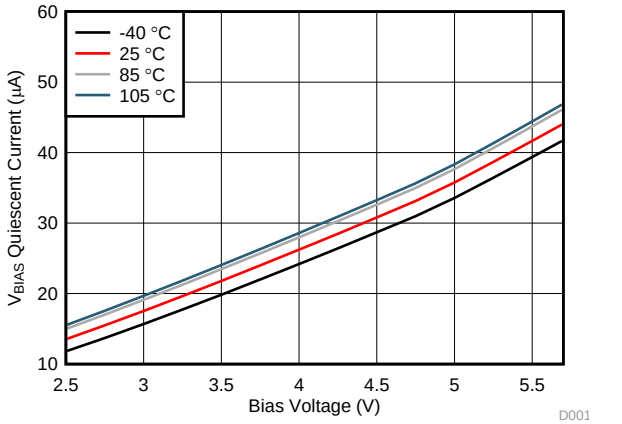
PARAMETER		TEST CONDITIONS		T_A	MIN	TYP	MAX	UNIT
POWER SUPPLIES AND CURRENTS								
$I_{Q, VBIAS}$	V_{BIAS} quiescent current	I_{OUT} = 0 mA, V_{IN} = V_{ON} = 2.5 V		–40°C to +105°C		14	20	µA
$I_{SD, VBIAS}$	V_{BIAS} shutdown current	V_{ON} = V_{OUT} = 0 V		–40°C to +105°C			1	µA
$I_{SD, VIN}$	V_{IN} off-state supply current	V_{ON} = V_{OUT} = 0 V	V_{IN} = 2.5 V	–40°C to +85°C		0.005	1.3	µA
				–40°C to +105°C			2.6	
			V_{IN} = 1.8 V	–40°C to +85°C		0.002	1	
				–40°C to +105°C			2	
			V_{IN} = 1.05 V	–40°C to +85°C		0.002	0.8	
				–40°C to +105°C			1.5	
			V_{IN} = 0.6 V	–40°C to +85°C		0.001	0.5	
				–40°C to +105°C			1	
I_{ON}	On-pin input leakage current	V_{ON} = 5.5 V		–40°C to +105°C			0.1	µA
RESISTANCE CHARACTERISTICS								
R_{ON}	On-resistance	I_{OUT} = –200 mA	V_{IN} = 2.5 V	25°C		20	26	mΩ
				–40°C to +85°C			32	
				–40°C to +105°C			34	
			V_{IN} = 1.8 V	25°C		18	23	
				–40°C to +85°C			29	
				–40°C to +105°C			31	
			V_{IN} = 1.5 V	25°C		18	22	
				–40°C to +85°C			28	
				–40°C to +105°C			30	
			V_{IN} = 1.2 V	25°C		17	22	
				–40°C to +85°C			27	
				–40°C to +105°C			29	
			V_{IN} = 0.6 V	25°C		17	21	
				–40°C to +85°C			26	
				–40°C to +105°C			27	
$V_{ON, HYS}$	On-pin hysteresis	V_{IN} = 2.5 V		25°C		85		mV
R_{PD} (1)	Output pulldown resistance	V_{IN} = 2.5 V, V_{ON} = 0 V		–40°C to +105°C		230	330	Ω
T_{SD}	Thermal shutdown	Junction temperature rising				160		°C
$T_{SD, HYS}$	Thermal shutdown hysteresis	Junction temperature falling				20		°C

(1) TPS22975 only

7.7 Switching Characteristics

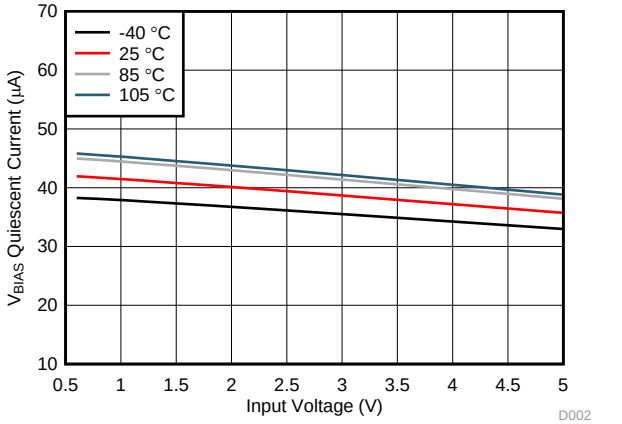
PARAMETER		TEST CONDITION	MIN	TYP	MAX	UNIT
V_{IN} = V_{BIAS} = 5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		1450		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		2		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		1750		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		2		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		600		
V_{IN} = 0.6 V, V_{BIAS} = 5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		620		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		2		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		280		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		2		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		485		
V_{IN} = V_{BIAS} = 2.5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		2180		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		2		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		2150		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		2		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		1120		
V_{IN} = 0.6 V, V_{BIAS} = 2.5 V, T_A = 25ºC (unless otherwise noted)						
t_{ON}	Turnon time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		1315		µs
t_{OFF}	Turnoff time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		3		
t_R	V_{OUT} rise time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		650		
t_F	V_{OUT} fall time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		2		
t_D	ON delay time	R_L = 10 Ω, C_L = 0.1 µF, C_{IN} = 1 µF, C_T = 1000 pF, V_{ON} = 5 V		975		

7.8 Typical DC Characteristics



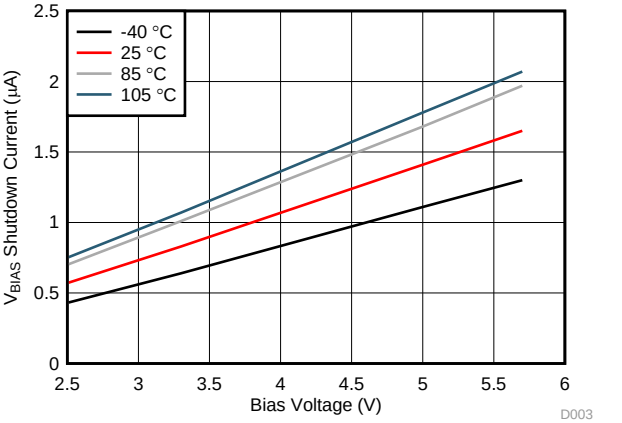
$V_{IN} = V_{BIAS}$ $V_{ON} = 5$ V $V_{OUT} = 0$ V

Figure 1. V_{BIAS} Quiescent Current vs Bias Voltage



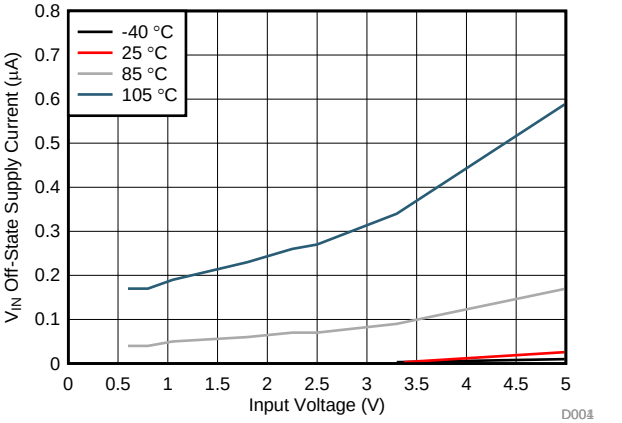
$V_{BIAS} = 5$ V $V_{ON} = 5$ V $V_{OUT} = 0$ V

Figure 2. V_{BIAS} Quiescent Current vs Input Voltage



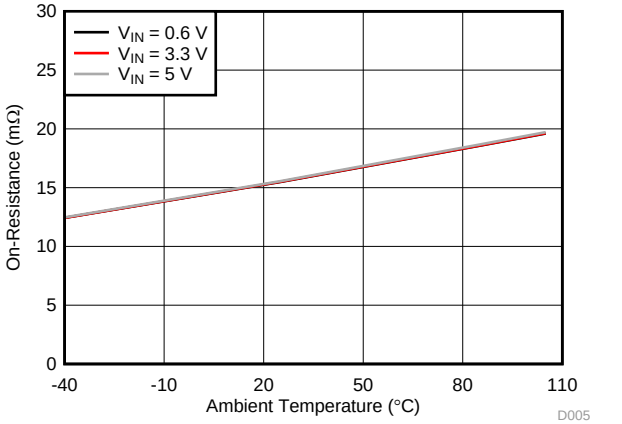
$V_{IN} = V_{BIAS}$ $V_{ON} = 0$ V $V_{OUT} = 0$ V

Figure 3. V_{BIAS} Shutdown Current vs Bias Voltage



$V_{BIAS} = 5$ V $V_{ON} = 0$ V $V_{OUT} = 0$ V

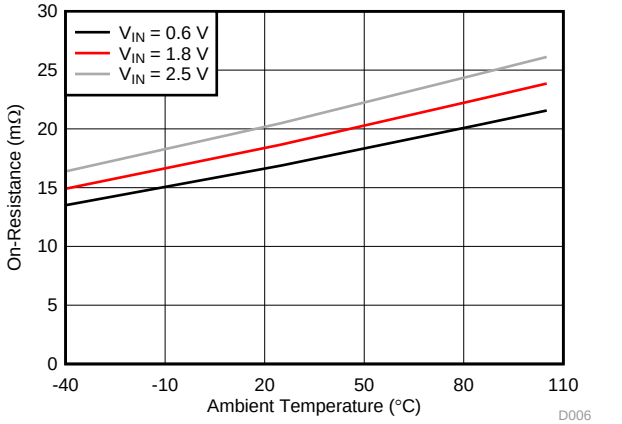
Figure 4. V_{IN} Off-State Supply Current vs Input Voltage



$V_{BIAS} = 5$ V $I_{OUT} = -200$ mA $V_{ON} = 5$ V

Note: All three R_{ON} curves have the same values; therefore, only one line is visible.

Figure 5. On-Resistance vs Ambient Temperature



$V_{BIAS} = 2.5$ V $I_{OUT} = -200$ mA $V_{ON} = 5$ V

Figure 6. On-Resistance vs Ambient Temperature

Typical DC Characteristics (continued)

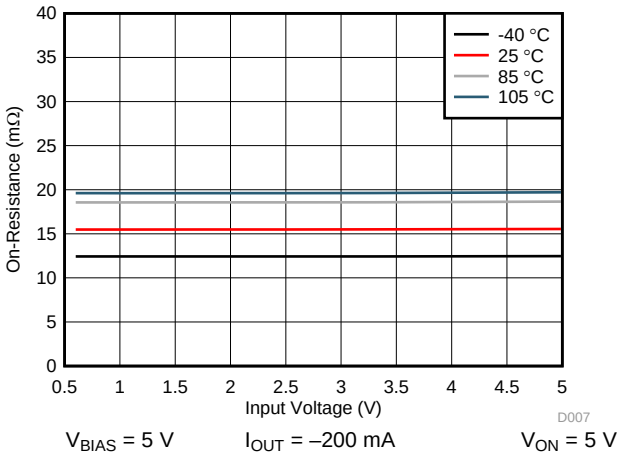


Figure 7. On-Resistance vs Input Voltage

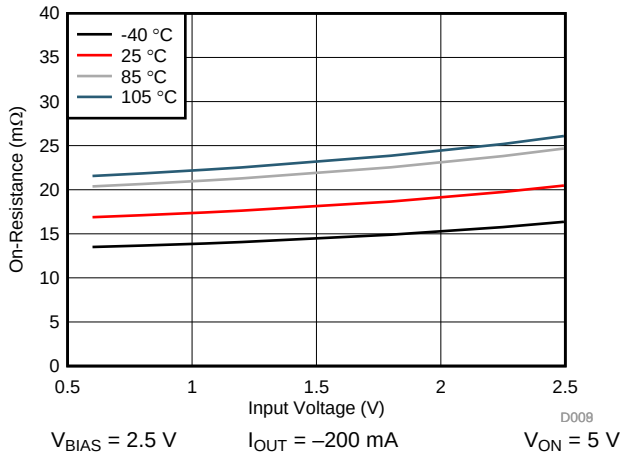


Figure 8. On-Resistance vs Input Voltage

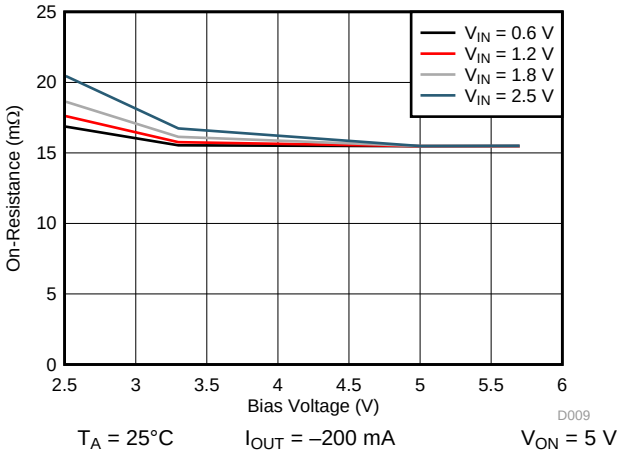


Figure 9. On-Resistance vs Bias Voltage

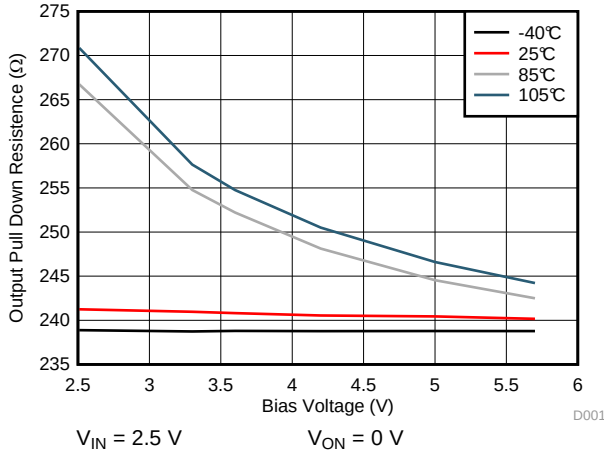
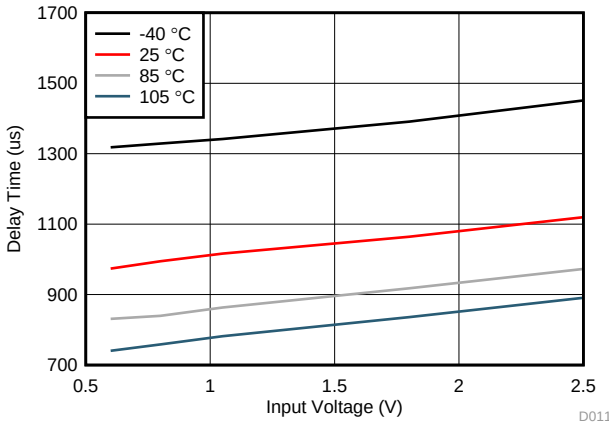


Figure 10. Output Pull Down Resistance vs Bias Voltage

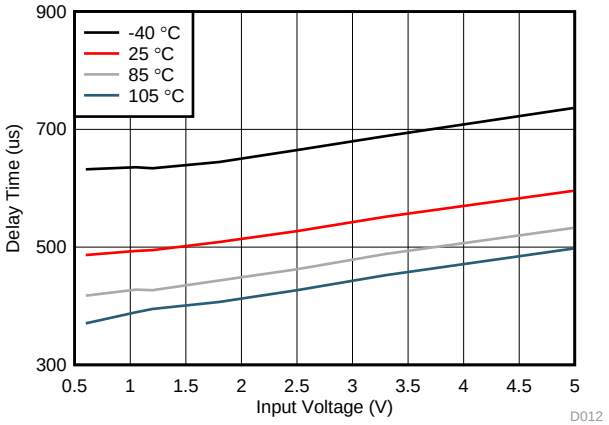
7.9 Typical AC Characteristics

T_A = 25°C, C_T = 1000 pF, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω



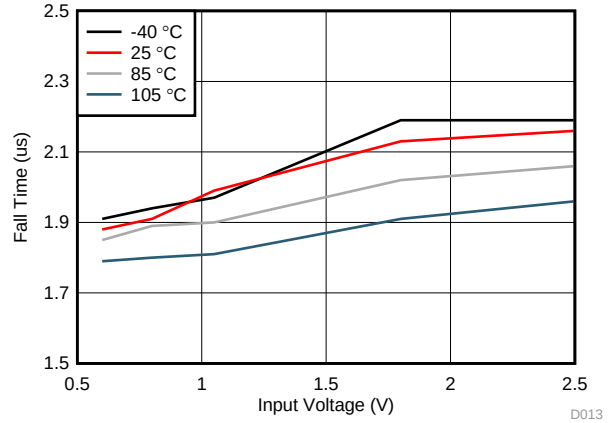
V_{BIAS} = 2.5 V

Figure 11. Delay Time vs Input Voltage



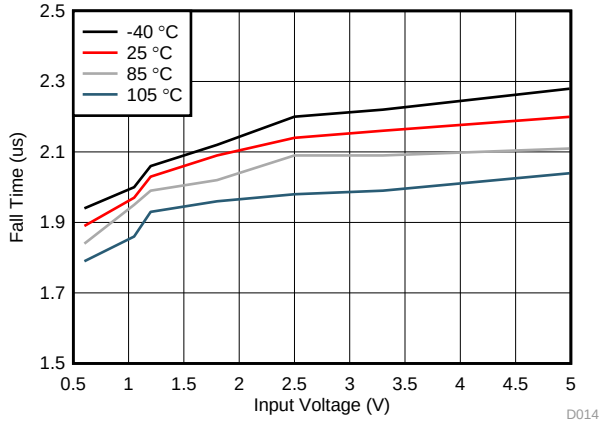
V_{BIAS} = 5 V

Figure 12. Delay Time vs Input Voltage



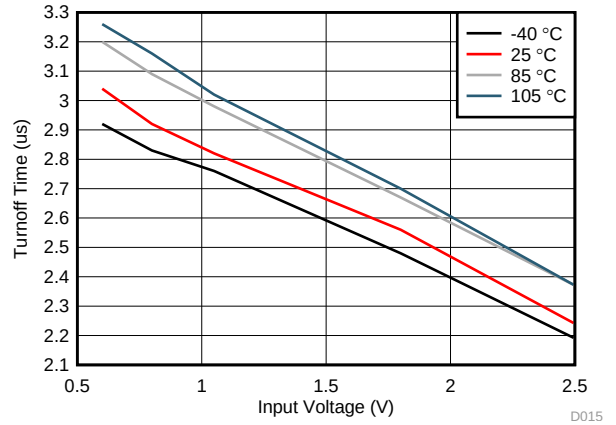
V_{BIAS} = 2.5 V

Figure 13. Fall Time vs Input Voltage



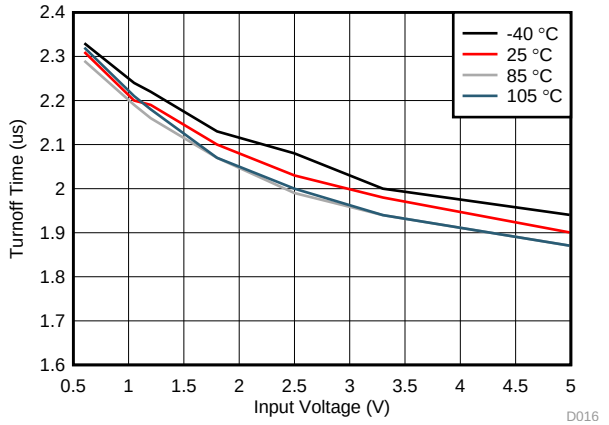
V_{BIAS} = 5 V

Figure 14. Fall Time vs Input Voltage



V_{BIAS} = 2.5 V

Figure 15. Turnoff Time vs Input Voltage

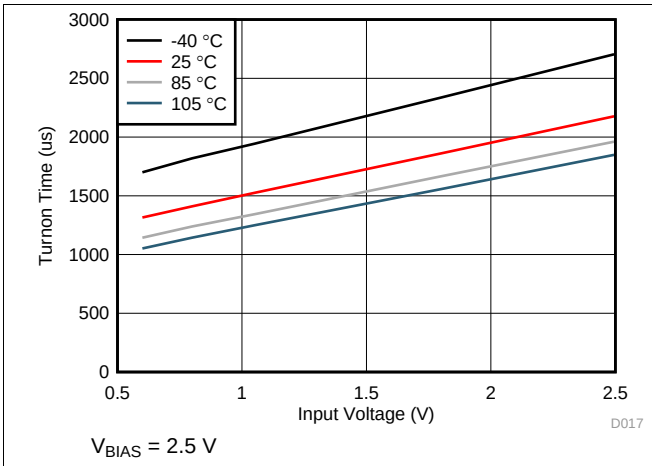


V_{BIAS} = 5 V

Figure 16. Turnoff Time vs Input Voltage

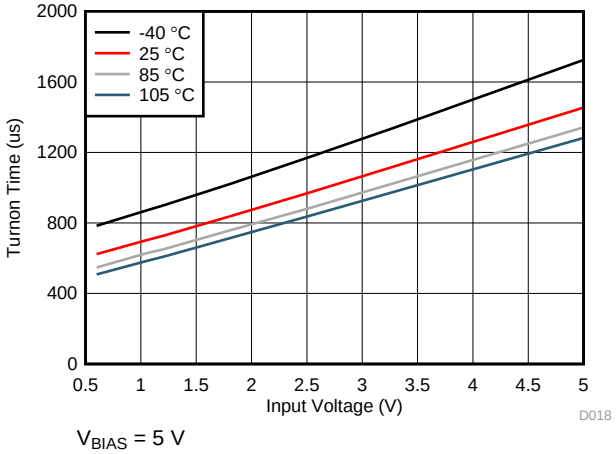
Typical AC Characteristics (continued)

T_A = 25°C, C_T = 1000 pF, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω



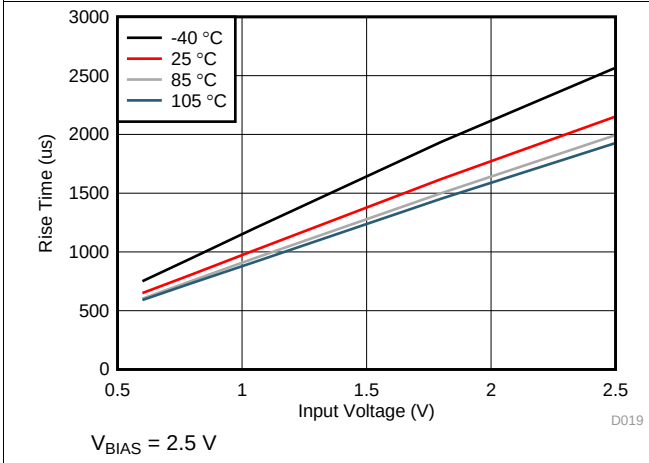
V_{BIAS} = 2.5 V

Figure 17. Turnon Time vs Input Voltage



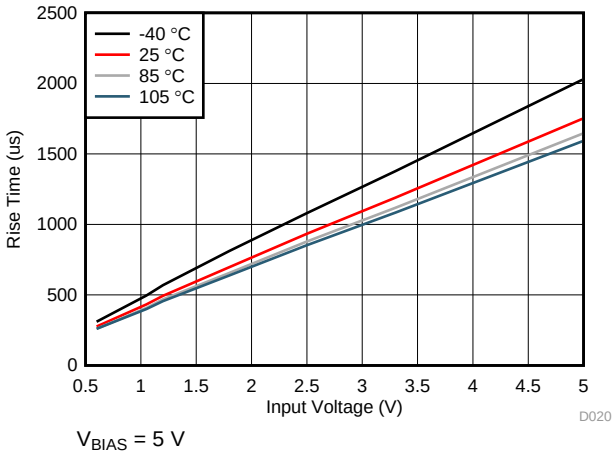
V_{BIAS} = 5 V

Figure 18. Turnon Time vs Input Voltage



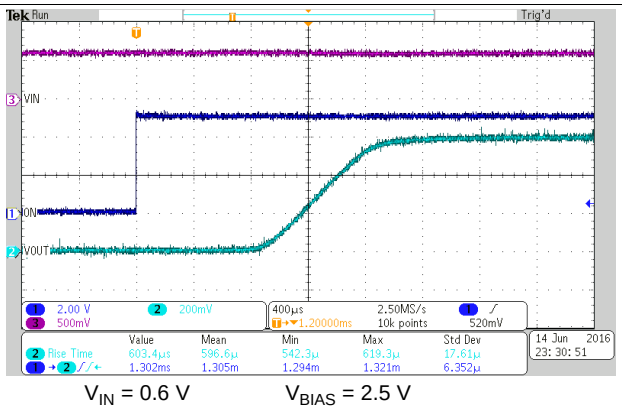
V_{BIAS} = 2.5 V

Figure 19. Rise Time vs Input Voltage



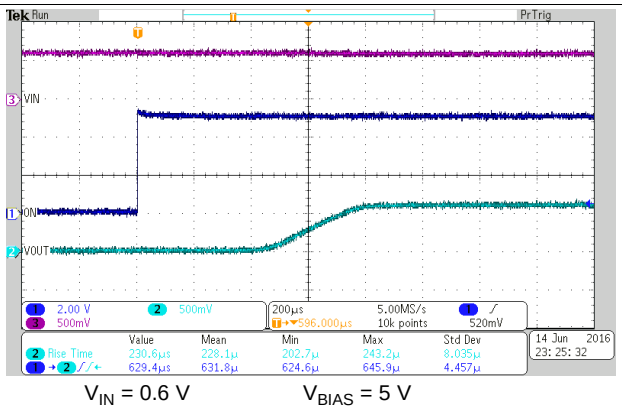
V_{BIAS} = 5 V

Figure 20. Rise Time vs Input Voltage



V_{IN} = 0.6 V V_{BIAS} = 2.5 V

Figure 21. Turnon Response Time

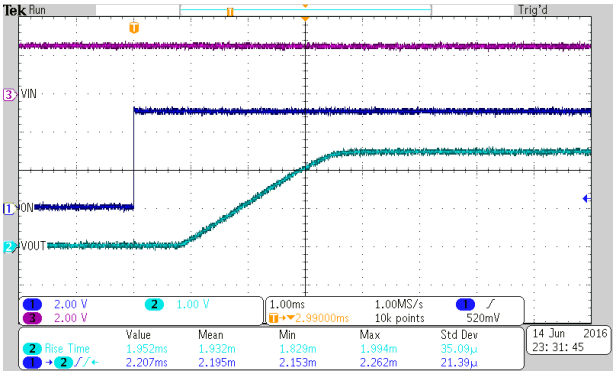


V_{IN} = 0.6 V V_{BIAS} = 5 V

Figure 22. Turnon Response Time

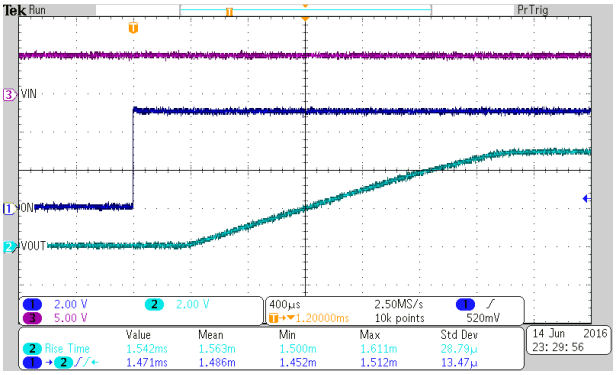
Typical AC Characteristics (continued)

T_A = 25°C, C_T = 1000 pF, C_{IN} = 1 µF, C_L = 0.1 µF, R_L = 10 Ω



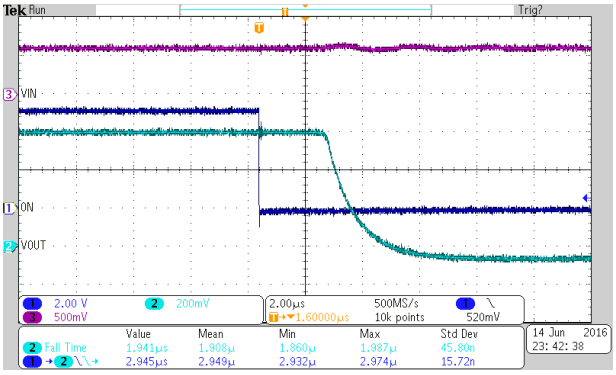
V_{IN} = 2.5 V V_{BIAS} = 2.5 V

Figure 23. Turnon Response Time



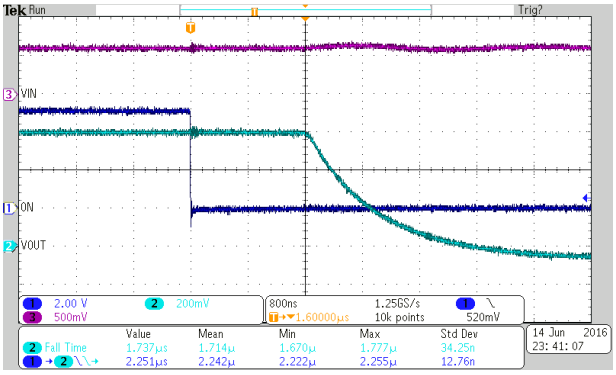
V_{IN} = 5 V V_{BIAS} = 5 V

Figure 24. Turnon Response Time



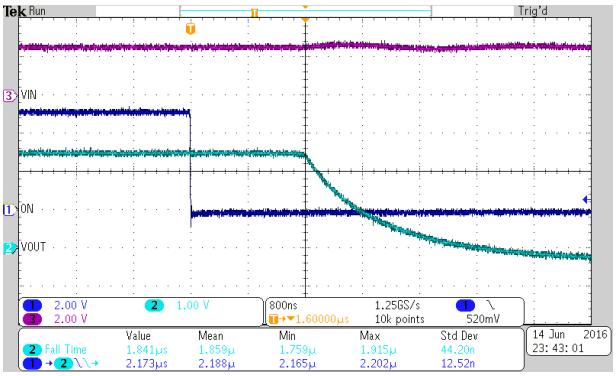
V_{IN} = 0.6 V V_{BIAS} = 2.5 V

Figure 25. Turnoff Response Time



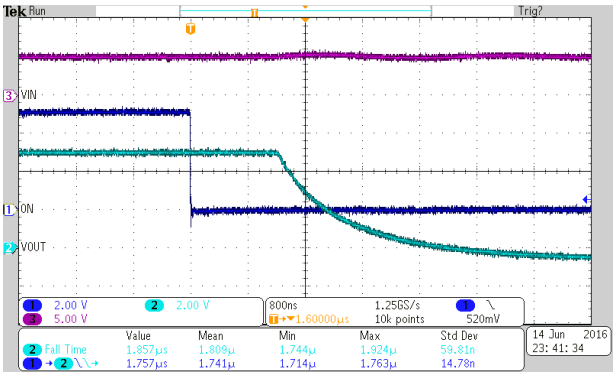
V_{IN} = 0.6 V V_{BIAS} = 5 V

Figure 26. Turnoff Response Time



V_{IN} = 2.5 V V_{BIAS} = 2.5 V

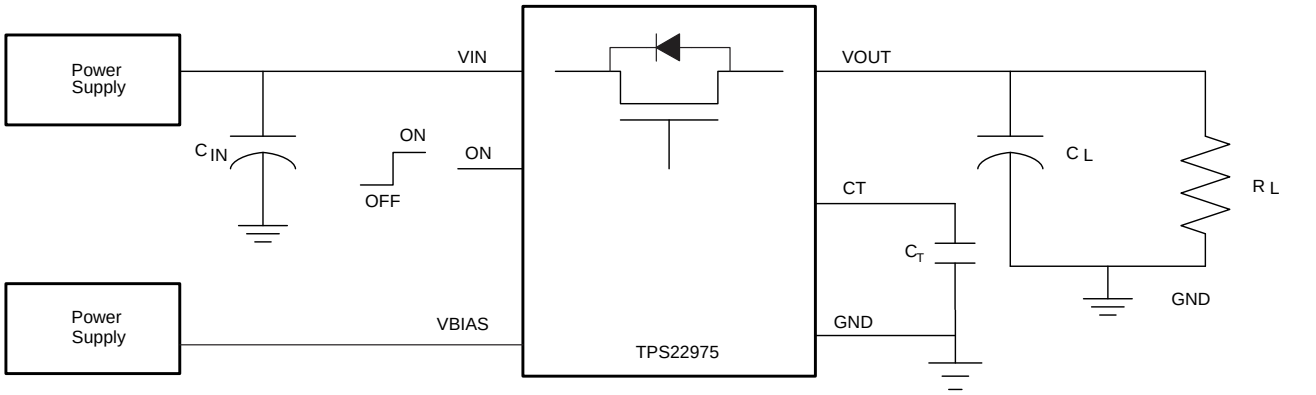
Figure 27. Turnoff Response Time



V_{IN} = 5 V V_{BIAS} = 5 V

Figure 28. Turnoff Response Time

8 Parameter Measurement Information



A. Rise and fall times of the control signal are 100 ns.

B. Turnoff times and fall times are dependent on the time constant at the load. For the TPS22975, the internal pull-down resistance R_{PD} is enabled when the switch is disabled. The time constant is (R_{PD} || R_L) × C_L.

Figure 29. Test Circuit

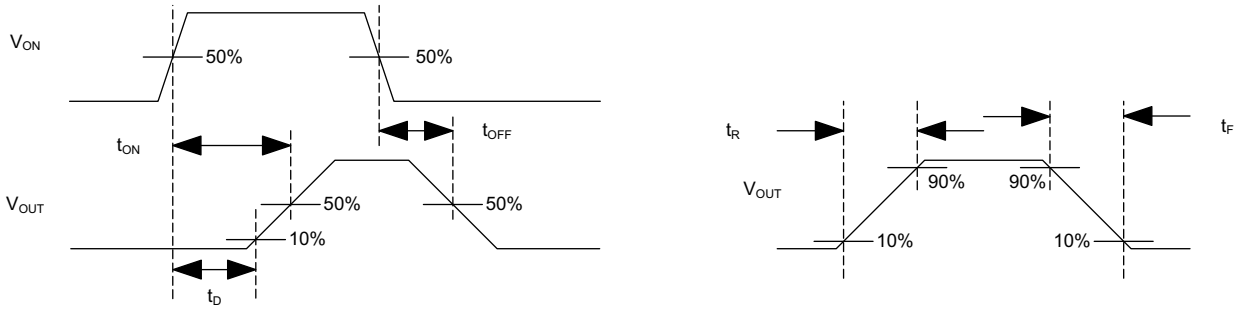


Figure 30. t_{ON} and t_{OFF} Waveforms

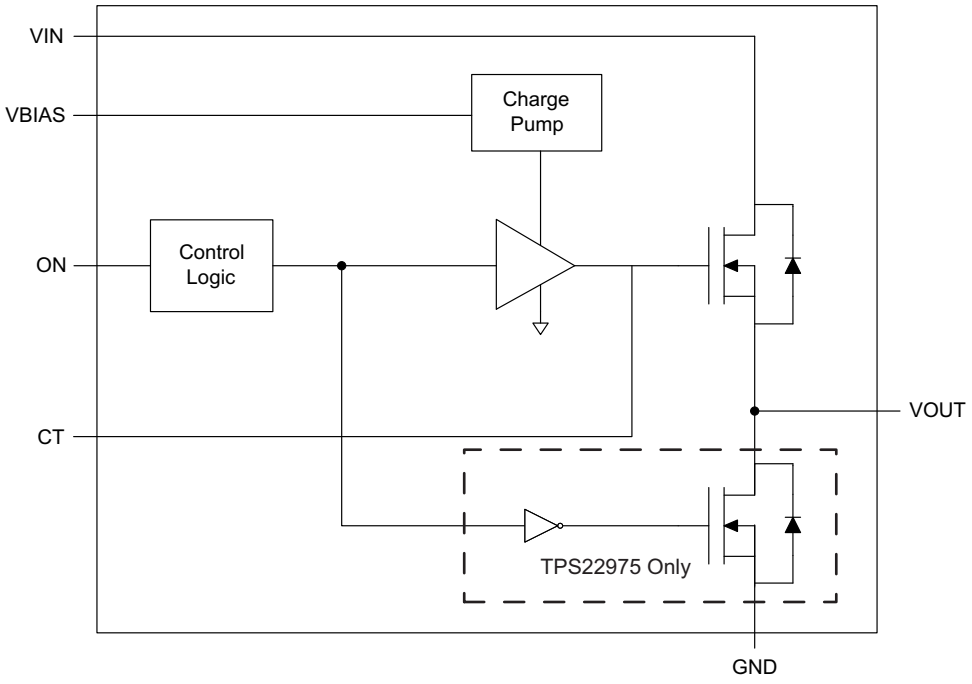
9 Detailed Description

9.1 Overview

The TPS22975 device is a single-channel, 6-A load switch in an 8-pin SON package. To reduce the voltage drop in high current rails, the device implements an N-channel MOSFET. The device has a configurable slew rate for applications that require a specific rise-time.

The device prevents downstream circuits from pulling high standby current from the supply by limiting the leakage current of the device when it is disabled. The integrated control logic, driver, power supply, and output discharge FET eliminates the need for any external components, which reduces solution size and bill of materials (BOM) count.

9.2 Functional Block Diagram



9.3 Feature Description

9.3.1 Adjustable Rise Time

A capacitor to GND on the CT pin sets the slew rate. The voltage on the CT pin can be as high as 15 V; therefore, the minimum voltage rating for the CT capacitor must be 30 V for optimal performance. An approximate formula for the relationship between C_T and slew rate when V_{BIAS} is set to 5 V is shown in Equation 1. This equation accounts for 10% to 90% measurement on V_{OUT} and does not apply for C_T < 100 pF. Use Table 1 to determine rise times for when C_T = 0 pF.

$$SR = 0.43 \times C_T + 26 \quad (1)$$

where

- SR is the slew rate (in µs/V)
- C_T is the capacitance value on the CT pin (in pF)
- The units for the constant 26 are µs/V. The units for the constant 0.43 are µs/(V × pF).

Rise time can be calculated by multiplying the input voltage by the slew rate. Table 1 contains rise time values measured on a typical device. Rise times shown in Table 1 are only valid for the power-up sequence where V_{IN} and V_{BIAS} are already in steady state condition before the ON pin is asserted high.

Table 1. Rise Time t_R vs CT Capacitor

C_T (pF)	RISE TIME (µs) 10% - 90%, C_L = 0.1 µF, C_{IN} = 1 µF, R_L = 10 Ω, V_{BIAS} = 5 V(1)						
	VIN = 5 V	VIN = 3.3 V	VIN = 1.8 V	VIN = 1.5 V	VIN = 1.2 V	VIN = 1.05 V	VIN = 0.6 V
0	140	105	75	65	60	55	40
220	520	360	215	185	160	140	95
470	970	660	385	330	275	240	155
1000	1750	1190	700	595	495	435	275
2200	3875	2615	1520	1290	1070	940	595
4700	7580	5110	2950	2510	2075	1830	1150
10000	16980	11485	6650	5635	4685	4110	2595

(1) Typical Values at 25°C with a 25-V X7R 10% Ceramic Capacitor on CT

9.3.2 Quick-Output Discharge (QOD) (Optional)

The TPS22975 includes an optional QOD feature. When the switch is disabled, an internal discharge resistance is connected between VOUT and GND to remove the remaining charge from the output. This resistance has a typical value of 230 Ω and prevents the output from floating while the switch is disabled. For best results, it is recommended that the device gets disabled before V_{BIAS} falls below the minimum recommended voltage.

9.3.3 Thermal Shutdown

Thermal shutdown protects the part from internally or externally generated excessive temperatures. When the device temperature triggers T_{SD} (typical 160°C), the switch is turned off. The switch automatically turns on again if the temperature of the die drops 20 degrees below the T_{SD} threshold.

9.4 Device Functional Modes

The Table 2 lists the VOUT pin states as determined by the ON pin.

Table 2. VOUT Connection

ON	TPS22975	TPS22975N
L	GND	Open
H	VIN	VIN

10 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

10.1 Application Information

10.1.1 ON and OFF Control

The ON pin controls the state of the switch. ON is active high and has a 1.2-V ON-pin enable threshold, making it capable of interfacing with low-voltage signals. The ON pin is compatible with standard GPIO logic thresholds. It can be used with any microcontroller with 1.2 V or higher GPIO voltage. This pin cannot be left floating and must be driven either high or low for proper functionality.

10.1.2 Input Capacitor (C_{IN}) (Optional)

To limit the voltage drop on the input supply caused by transient inrush currents when the switch turns on into a discharged load capacitor or short-circuit, a capacitor needs to be placed between VIN and GND. A 1-µF ceramic capacitor, C_{IN}, placed close to the pins, is usually sufficient. Higher values of C_{IN} can be used to further reduce the voltage drop during high current applications. When switching heavy loads, it is recommended to have an input capacitor about 10 times higher than the output capacitor (C_L) to avoid excessive voltage drop.

10.1.3 Output Capacitor (C_L) (Optional)

Because of the integrated body diode in the NMOS switch, a C_{IN} greater than C_L is highly recommended. A C_L greater than C_{IN} can cause V_{OUT} to exceed V_{IN} when the system supply is removed. This could result in current flow through the body diode from V_{OUT} to V_{IN}. A C_{IN} to C_L ratio of 10 to 1 is recommended for minimizing V_{IN} dip caused by inrush currents during startup; however, a 10 to 1 ratio for capacitance is not required for proper functionality of the device. A ratio smaller than 10 to 1 (such as 1 to 1) could cause slightly more V_{IN} dip upon turn-on because of inrush currents. This can be mitigated by increasing the capacitance on the CT pin for a longer rise time (see the *Adjustable Rise Time* section).

10.2 Typical Application

For optimal R_{ON} performance, it is recommended to have $V_{IN} \leq V_{BIAS}$. The device is functional if $V_{IN} > V_{BIAS}$ but it exhibits R_{ON} greater than what is listed in the *Electrical Characteristics—V_{BIAS} = 5 V* and Electrical Characteristics—V_{BIAS} = 2.5 V tables.

Figure 31 demonstrates how the TPS22975 can be used to power downstream modules.

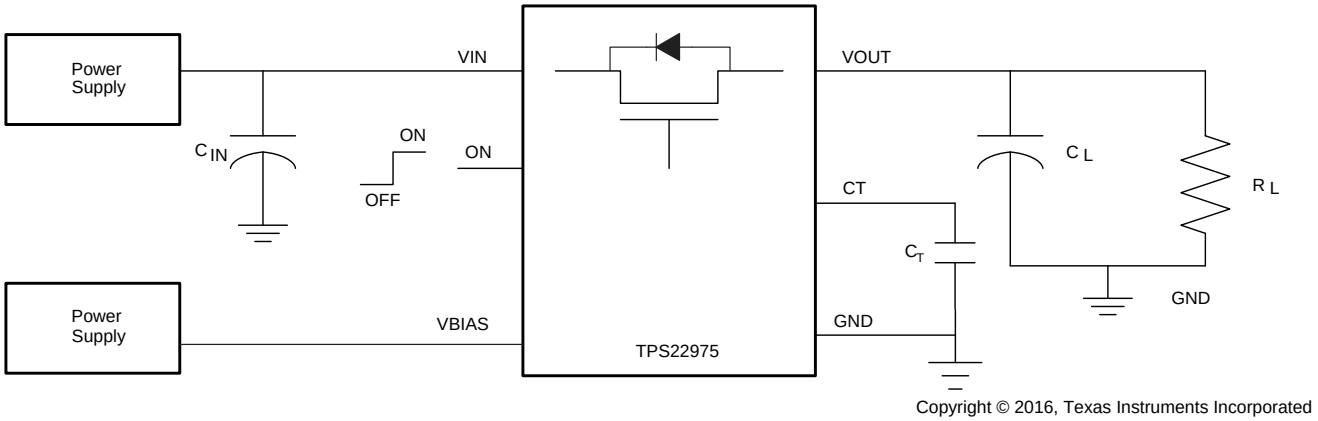


Figure 31. Powering a Downstream Module

Typical Application (continued)

10.2.1 Design Requirements

DESIGN PARAMETER	EXAMPLE VALUE
V_{IN}	3.3 V
V_{BIAS}	5 V
C_L	22 µF
Maximum Acceptable Inrush Current	400 mA

10.2.2 Detailed Design Procedure

10.2.2.1 Inrush Current

When the switch is enabled, the output capacitors must be charged up from 0 V to the set value (3.3 V in this example). This charge arrives in the form of inrush current. Inrush current can be calculated using Equation 2.

$$\text{Inrush Current} = C_L \times dV_{OUT}/dt \quad (2)$$

Where:

- C_L is the output capacitance
- dV_{OUT} is the change in V_{OUT} during the ramp up of the output voltage when device is enabled.
- dt is the rise time in V_{OUT} during the ramp up of the output voltage when the device is enabled.

The TPS22975 offers adjustable rise time for VOUT. This feature allows the user to control the inrush current during turnon. The appropriate rise time can be calculated using the design requirements and the inrush current equation as shown in Equation 3.

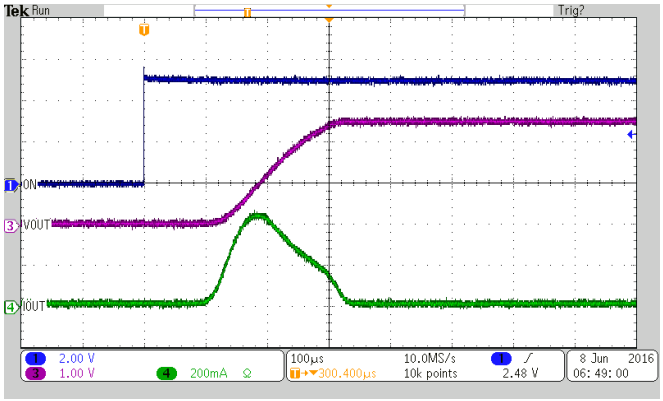
$$400\ \text{mA} = 22\ \mu\text{F} \times 3.3\ \text{V}/dt \quad (3)$$

The value of dt is given by Equation 4.

$$dt = 181.5\ \mu\text{s} \quad (4)$$

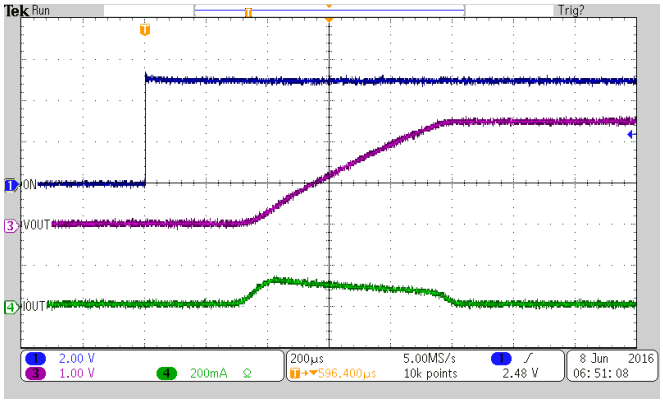
To ensure an inrush current of less than 400 mA, choose a CT value that yields a rise time of more than 181.5 µs. See the oscilloscope captures in the *Application Curves* section for an example of how the CT capacitor can be used to reduce inrush current.

10.2.3 Application Curves



V_{BIAS} = 5 V V_{IN} = 3.3 V C_L = 22 µF

Figure 32. Inrush Current with CT = 0 pF



V_{BIAS} = 5 V V_{IN} = 3.3 V C_L = 22 µF

Figure 33. Inrush Current with CT = 220 pF

11 Power Supply Recommendations

The supply to the device must be well regulated and placed as close to the device terminal as possible with the recommended 1-μF bypass capacitor. If the supply is located more than a few inches from the device terminals, additional bulk capacitance may be required in addition to the ceramic bypass capacitors. If additional bulk capacitance is required, an electrolytic, tantalum or ceramic capacitor of 1 μF may be sufficient.

The TPS22975 operates regardless of power sequencing order. The order in which voltages are applied to V_{IN}, V_{BIAS}, and ON does not damage the device as long as the voltages do not exceed the absolute maximum operating conditions. If voltage is applied to ON before V_{IN}, the slew rate of V_{OUT} can not be controlled.

12 Layout

12.1 Layout Guidelines

For best performance, all traces must be as short as possible. To be most effective, the input and output capacitors must be placed close to the device to minimize the effects that parasitic trace inductances may have on normal operation. Using wide traces for VIN, VOUT, and GND helps minimize the parasitic electrical effects along with minimizing the case to ambient thermal impedance. The CT trace must be as short as possible to reduce parasitic capacitance.

12.2 Layout Example

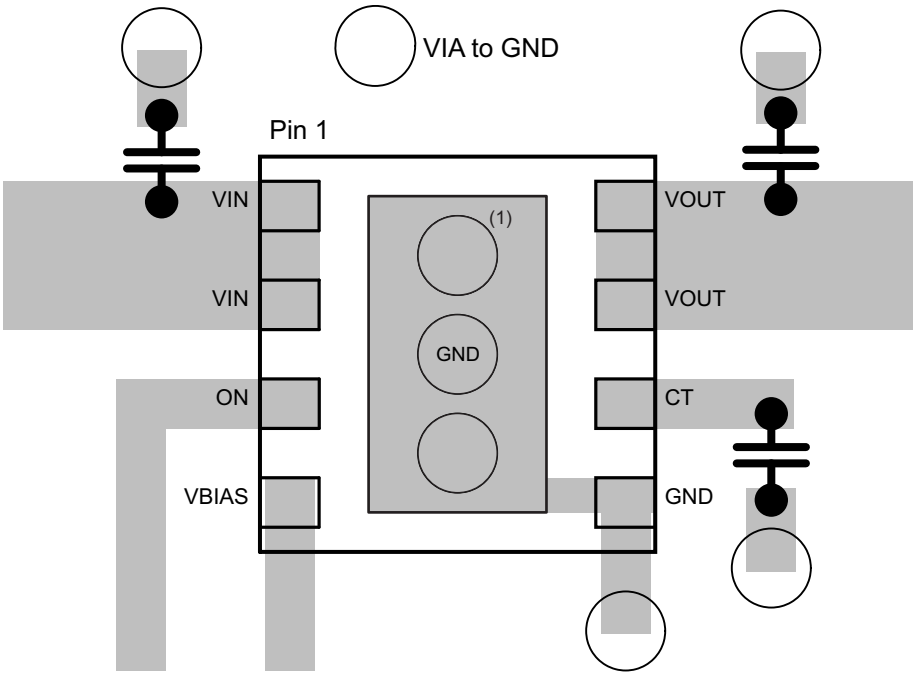


Figure 34. Layout Recommendation

12.3 Thermal Considerations

The maximum IC junction temperature must be restricted to 125°C under normal operating conditions. To calculate the maximum allowable dissipation, $P_{D(max)}$, for a given ambient temperature, use Equation 5 as a guideline.

$$P_{D(max)} = \frac{T_{J(max)} - T_A}{\theta_{JA}} \quad (5)$$

where

- $P_{D(max)}$ is the maximum allowable power dissipation
- $T_{J(max)}$ is the maximum allowable junction temperature (125°C for the TPS22975)
- T_A is the ambient temperature of the device
- Θ_{JA} is the junction to air thermal impedance. See the *Thermal Information* section. This parameter is highly dependent upon board layout.

In Figure 34, notice that the thermal vias are located under the exposed thermal pad of the device. This allows for thermal diffusion away from the device.

13 デバイスおよびドキュメントのサポート

13.1 デバイス・サポート

13.1.1 開発サポート

TPS22975 PSpiceトランジェント・モデルについては、SLVMBO6を参照してください。

13.2 関連資料

関連資料については、以下を参照してください。

- 『負荷スイッチのオン抵抗の基礎』、SLVA771
- 『TPS22975 負荷スイッチ評価モジュール ユーザー・ガイド』、SLVUAR3

13.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の隅にある「通知を受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

13.4 コミュニティ・リソース

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

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設計サポート ***TIの設計サポート*** **役に立つE2Eフォーラムや、設計サポート・ ツールをすばやく見つけることができます。技術サポート用の連絡先情報も参照できます。**

13.5 商標

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13.6 静電気放電に関する注意事項

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

13.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

14 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPS22975DSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	13XH	Samples
TPS22975DSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	13XH	Samples
TPS22975NDSGR	ACTIVE	WSON	DSG	8	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	14YH	Samples
TPS22975NDSGT	ACTIVE	WSON	DSG	8	250	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 105	14YH	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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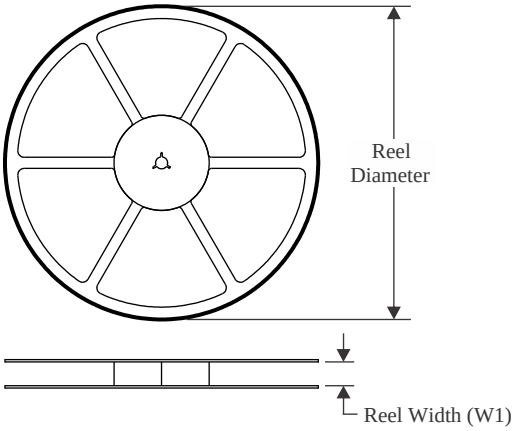
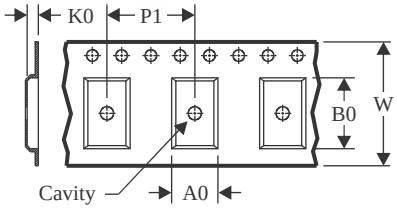
TAPE AND REEL INFORMATION

REEL DIMENSIONS

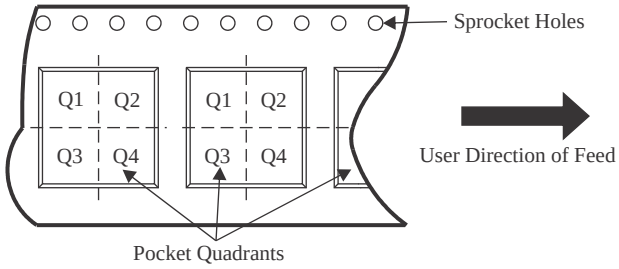


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

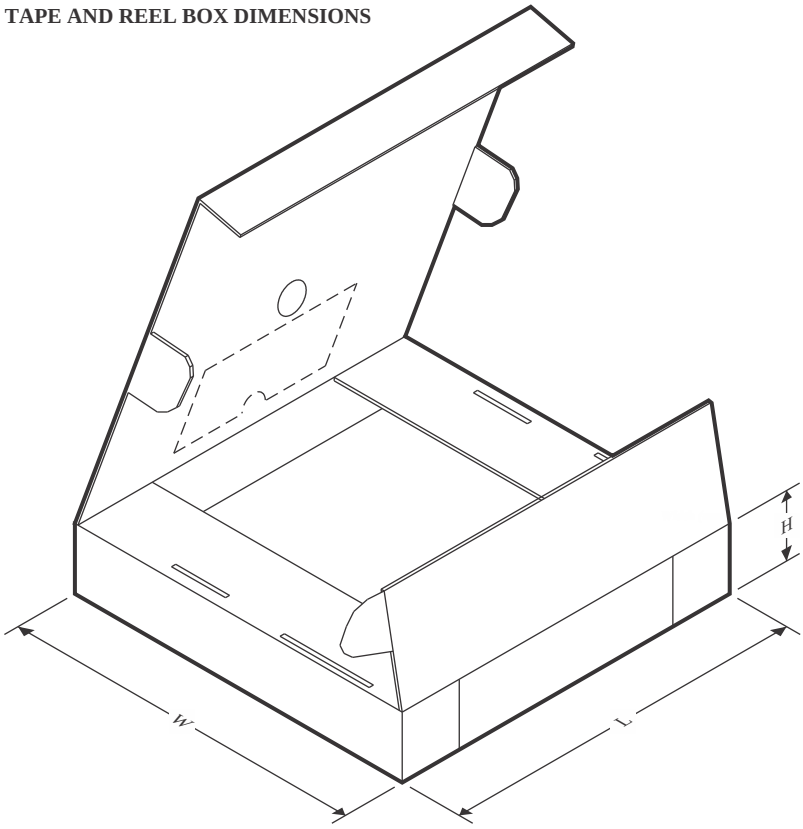
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPS22975DSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22975DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22975DSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22975NDSGR	WSON	DSG	8	3000	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22975NDSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2
TPS22975NDSGT	WSON	DSG	8	250	180.0	8.4	2.3	2.3	1.15	4.0	8.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPS22975DSGR	WSON	DSG	8	3000	182.0	182.0	20.0
TPS22975DSGT	WSON	DSG	8	250	182.0	182.0	20.0
TPS22975DSGT	WSON	DSG	8	250	210.0	185.0	35.0
TPS22975NDSGR	WSON	DSG	8	3000	182.0	182.0	20.0
TPS22975NDSGT	WSON	DSG	8	250	182.0	182.0	20.0
TPS22975NDSGT	WSON	DSG	8	250	210.0	185.0	35.0

GENERIC PACKAGE VIEW

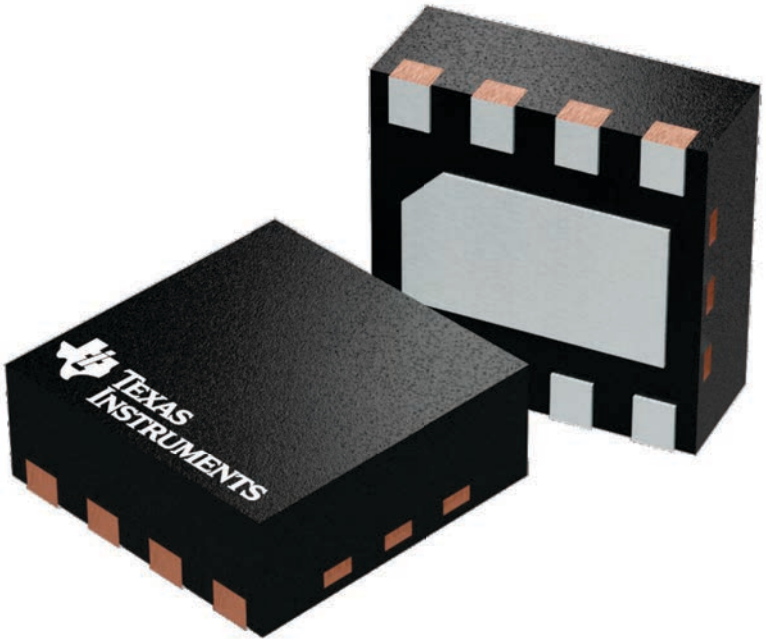
DSG 8

WSON - 0.8 mm max height

2 x 2, 0.5 mm pitch

PLASTIC SMALL OUTLINE - NO LEAD

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



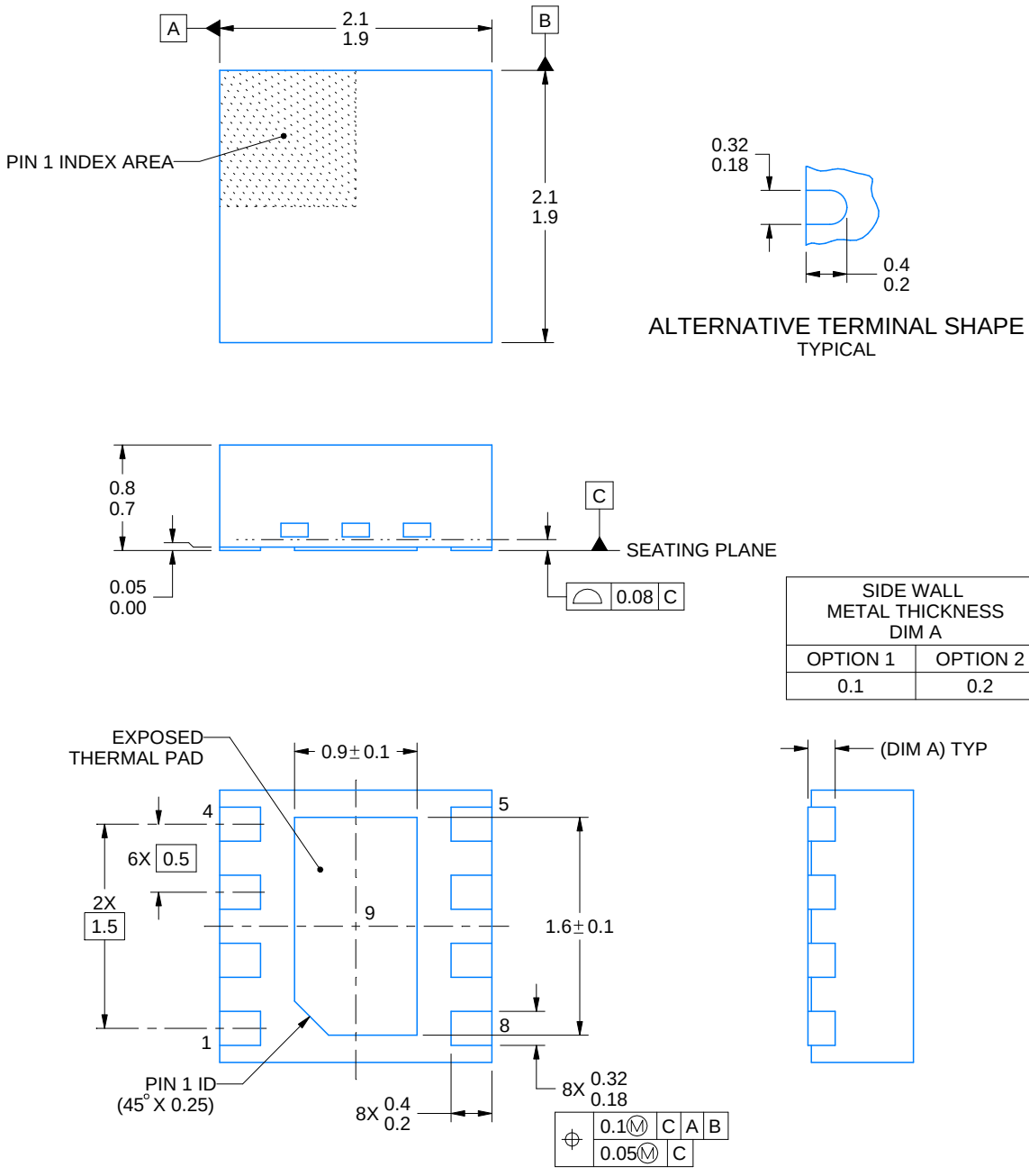
4224783/A

PACKAGE OUTLINE

DSG0008A

WSON - 0.8 mm max height

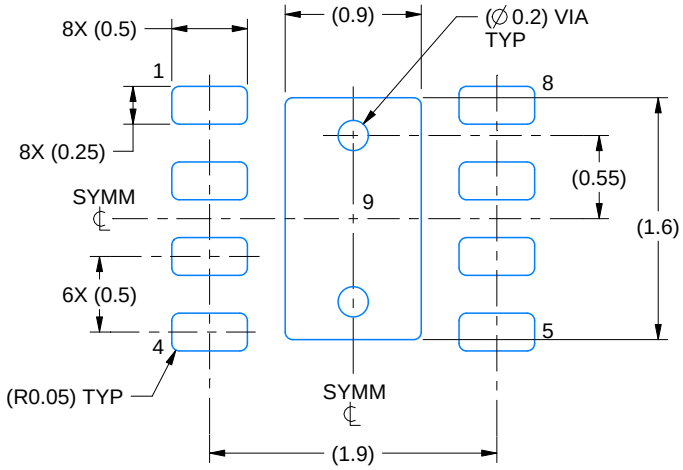
PLASTIC SMALL OUTLINE - NO LEAD



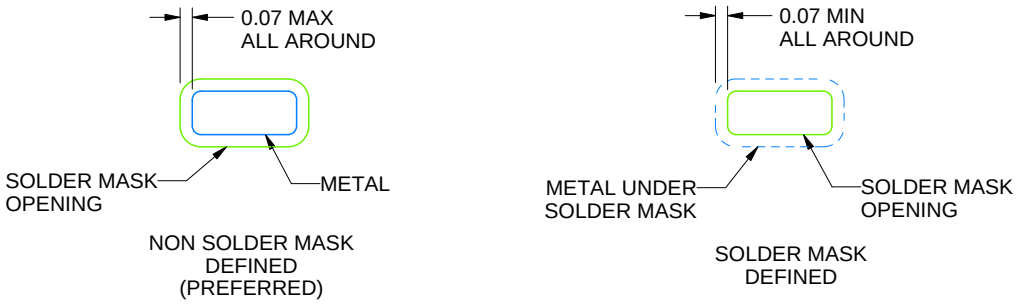
4218900/E 08/2022

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:20X

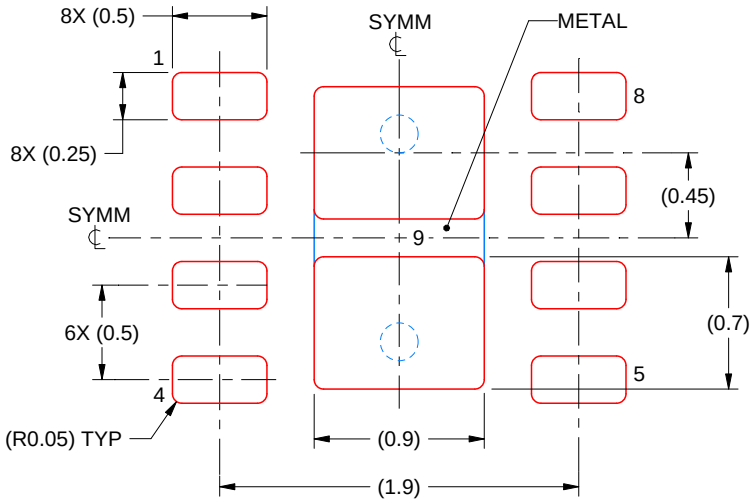


SOLDER MASK DETAILS

4218900/E 08/2022

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 9:
87% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:25X

4218900/E 08/2022

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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