

AMC1035 $\pm 1V$ のバイポーラ入力と2.5Vの基準出力を持つデルタ-シグマ変調器

1 特長

- 電圧および温度の検出に最適化されたデルタ-シグマ変調器
 - $\pm 1V$ の入力電圧範囲
 - 高い差動入力抵抗: $1.6G\Omega$ (標準値)
 - 内蔵の $2.5V$ 、 $\pm 5mA$ 基準電圧によるレシオメトリック測定
- 非常に優れた DC 性能
 - オフセット誤差: $\pm 0.5mV$ (最大値)
 - オフセット・ドリフト係数: $\pm 6\mu V/^{\circ}C$ (最大値)
 - ゲイン誤差: $\pm 0.25\%$ (最大値)
 - ゲイン・ドリフト係数: $\pm 45ppm/^{\circ}C$ (最大値)
 - レシオメトリック・ゲイン・ドリフト係数: $\pm 15ppm/^{\circ}C$ (最大値)
- マンチェスター・エンコードまたはコード化なしのビットストリーム出力を選択可能
- 拡張産業用温度範囲にわたって完全に動作を規定: $-40^{\circ}C \sim +125^{\circ}C$

2 アプリケーション

- 産業用途での AC 電圧および温度センシング
 - モータ・ドライブ
 - 光電池インバータ
 - 無停電電源
 - 産業用輸送システム

3 概要

AMC1035は高精度のデルタ-シグマ($\Delta\Sigma$)変調器で、単一の $3.0V \sim 5.5V$ 電源で動作し、外部から供給される $9MHz \sim 21MHz$ の範囲のクロック信号を使用します。マンチェスター・モードでは、規定のクロック範囲は $9MHz \sim 11MHz$ です。デバイスの差動 $\pm 1V$ 入力構造は、産業用アプリケーションで一般的な、ノイズの多い環境に向けて最適化されています。

AMC1035のビットストリーム出力をマンチェスター符号化すると、受信側デバイスのセットアップおよびホールド時間の要件に制約が発生することを防止し、回路レイアウトの労力を削減できます。デジタル・フィルタ

(TMS320F28004x、TMS320F2807x、TMS320F2837x マイクロコントローラ・ファミリに内蔵されているものなど)を使用して出力ビットストリームを間引くと、 $82kSPS$ のデータ速度、 $87dB$ のダイナミック・レンジで、 16 ビットの分解能が得られます。

AMC1035の内部基準ソースはレシオメトリックな回路アーキテクチャをサポートしているため、電源電圧の変動や温度ドリフトが測定精度に及ぼす悪影響を最小限に抑えられます。

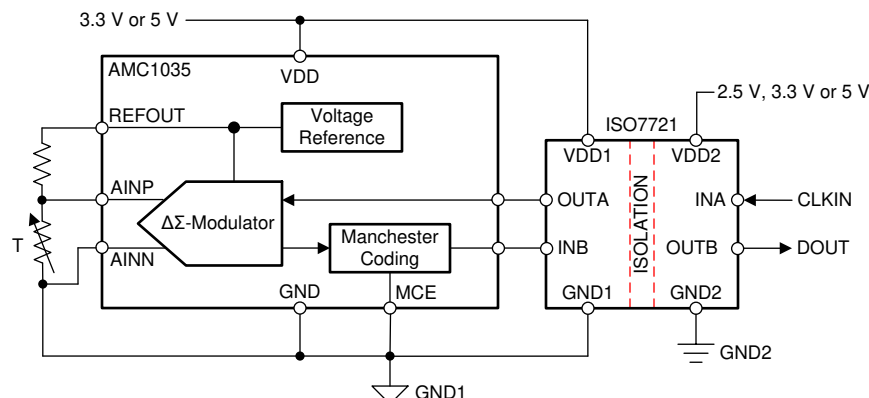
また、AMC1035はデジタル・アイソレータと絶縁電源を使用して、AC電源ライン電圧センシングにも使用できます。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ (公称)
AMC1035	SOIC (8)	4.9mm×3.9mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

アプリケーションの例



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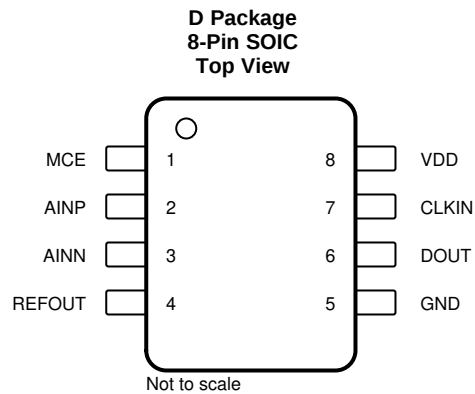
4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (November 2018) から Revision B に変更	Page
Deleted PSRR specification for $T_A > 85^\circ\text{C}$ from <i>Reference Output</i> section of <i>Electrical Characteristics</i> table	6
変更 SINAD equation.....	22

2018年8月発行のものから更新	Page
ドキュメントのステータスを「事前情報」から「量産データ」に変更	1

5 Pin Configuration and Functions



Pin Functions

PIN		I/O	DESCRIPTION
NO.	NAME		
1	MCE	I	Manchester coding enabled, active high, with internal pulldown resistor (typical value: 200 k Ω). The polarity of this signal must not be changed when the clock signal is applied.
2	AINP	I	Noninverting analog input.
3	AINN	I	Inverting analog input.
4	REFOUT	O	Reference output: 2.5 V nominal, maximum ± 5 -mA sink and source capability.
5	GND	—	Ground reference.
6	DOUT	O	Modulator bitstream data output, updated with the rising edge of the clock signal present on CLKIN. This pin is a Manchester coded output if MCE is pulled high. Use the rising edge of the clock to latch the modulator bitstream at the input of the digital filter device.
7	CLKIN	I	Modulator clock input: 9 MHz to 21 MHz with an internal pulldown resistor (typical value: 200 k Ω). The clock signal must be applied continuously for proper device operation; see the Clock Input section for additional details.
8	VDD	—	Power supply, 3.0 V to 5.5 V. See the Power Supply Recommendations section for decoupling recommendations.

6 Specifications

6.1 Absolute Maximum Ratings

see ⁽¹⁾

	MIN	MAX	UNIT
Supply voltage, VDD to GND	−0.3	7	V
Analog input voltage at AINP, AINN	GND − 5	VDD + 0.5	V
Analog output voltage at REFOUT	GND − 0.5	VDD + 0.5	V
Digital input voltage at CLKIN or MCE	GND − 0.5	VDD + 0.5	V
Digital output voltage at DOUT	GND − 0.5	VDD + 0.5	V
Input current to any pin except supply pins	−10	10	mA
Junction temperature, T _J		150	°C
Storage temperature, T _{stg}	−65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
POWER SUPPLY						
VDD	Supply voltage	VDD to GND	3.0	3.3	5.5	V
ANALOG INPUT						
V _{Clipping}	Differential input voltage before clipping output	V _{IN} = V _{AINP} − V _{AINN}	±1.25			V
V _{FSR}	Specified linear differential full-scale voltage	V _{IN} = V _{AINP} − V _{AINN}	−1		1	V
	Absolute common-mode input voltage ⁽¹⁾	(V _{AINP} + V _{AINN}) / 2 to GND	−2		VDD	V
V _{CM}	Operating common-mode input voltage ⁽²⁾	(V _{AINP} + V _{AINN}) / 2 to GND, 3.0 V ≤ VDD < 4 V, V _{AINP} = V _{AINN}	−1.4		VDD − 1.4	V
		(V _{AINP} + V _{AINN}) / 2 to GND, 3.0 V ≤ VDD < 4.5 V, V _{AINP} − V _{AINN} = 1.25 V	−0.8		VDD − 2.4	
		(V _{AINP} + V _{AINN}) / 2 to GND, 4 V ≤ VDD ≤ 5.5 V, V _{AINP} = V _{AINN}	−1.4		2.7	
		(V _{AINP} + V _{AINN}) / 2 to GND, 4.5 V ≤ VDD ≤ 5.5 V, V _{AINP} − V _{AINN} = 1.25 V	−0.8		2.1	
DIGITAL INPUT						
	Input voltage	V _{MCE} or V _{CLKIN} to GND	GND		VDD	V
TEMPERATURE RANGE						
T _A	Operating ambient temperature		−40	25	125	°C

- (1) Steady-state voltage supported by the device in case of a system failure. See specified common-mode input voltage V_{CM} for normal operation. Observe analog input voltage range as specified in the [Absolute Maximum Ratings](#) table.
(2) See the [Analog Input](#) section for more details.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		AMC1035	UNIT
		D (SOIC)	
		8 PINS	
R _{θJA}	Junction-to-ambient thermal resistance	120	°C/W
R _{θJC(top)}	Junction-to-case (top) thermal resistance	52	°C/W
R _{θJB}	Junction-to-board thermal resistance	61	°C/W
ψ _{JT}	Junction-to-top characterization parameter	10	°C/W
ψ _{JB}	Junction-to-board characterization parameter	60	°C/W
R _{θJC(bot)}	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC Package Thermal Metrics](#) application report.

6.5 Electrical Characteristics

minimum and maximum specifications apply from T_A = –40°C to +125°C, VDD = 3.0 V to 5.5 V, AINP = –1 V to 1 V, AINN = GND, and sinc³ filter with OSR = 256 (unless otherwise noted); typical specifications are at T_A = 25°C, CLKIN = 20 MHz, and VDD = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
ANALOG INPUTS						
V _{CMUV} ⁽¹⁾	Negative common-mode undervoltage detection level ⁽²⁾	(V _{AINP} + V _{AINN}) / 2, V _{AINP} = V _{AINN}	–1.45			V
		(V _{AINP} + V _{AINN}) / 2, V _{AINP} – V _{AINN} = 1.25 V	–0.85			
V _{CMOV} ⁽¹⁾	Positive common-mode overvoltage detection level ⁽²⁾	3.0 V ≤ VDD < 4 V, V _{AINP} = V _{AINN}	VDD – 1.35			V
		3.0 V ≤ VDD < 4.5 V, V _{AINP} – V _{AINN} = 1.25 V	VDD – 2.35			
		4 V ≤ VDD ≤ 5.5 V, V _{AINP} = V _{AINN}	2.75			
		4.5 V ≤ VDD ≤ 5.5 V, V _{AINP} – V _{AINN} = 1.25 V	2.15			
R _{IN}	Single-ended input resistance	AINN = GND	0.1	0.4		GΩ
R _{IND}	Differential input resistance		0.16	1.6		GΩ
C _{IN}	Single-ended input capacitance	AINN = GND		2		pF
C _{IND}	Differential input capacitance			2		pF
I _{IB}	Input bias current	AINP = AINN = GND, (I _{AINP} + I _{AINN}) / 2	–10	±3	10	nA
TC _{I_{IB}}	Input bias current thermal drift	AINP = AINN = GND, (I _{AINP} + I _{AINN}) / 2		±5		pA/°C
I _{IO}	Input offset current	I _{IO} = I _{AINP} – I _{AINN}	–5	±1	5	nA
CMRR	Common-mode rejection ratio	AINP = AINN, f _{IN} = 0 Hz, V _{CM min} ≤ V _{IN} ≤ V _{CM max}	–104			dB
		AINP = AINN, f _{IN} from 0.1 Hz to 50 kHz, –0.5 V ≤ V _{IN} ≤ 0.5 V	–88			
DC ACCURACY						
	Resolution ⁽³⁾		16			Bits
INL	Integral nonlinearity ⁽⁴⁾	Resolution: 16 bits	–12	±2	12	LSB
E _O	Offset error	Initial, at T _A = 25°C, AINP = AINN = GND	–0.5	±0.03	0.5	mV
TCE _O	Offset error thermal drift ⁽⁵⁾		–6	±0.1	6	μV/°C
E _G	Gain error	Initial, at T _A = 25°C	–0.25%	±0.02%	0.25%	
		Initial, at T _A = 25°C, ratiometric mode	–0.3%	±0.02%	0.3%	
TCE _G	Gain error thermal drift ⁽⁶⁾		–45	±20	45	ppm/°C
		Ratiometric mode	–15	±4	15	
PSRR	Power-supply rejection ratio	AINP = AINN = GND, at dc	–90			dB
		AINP = AINN = GND, 10 kHz, 100-mV ripple	–84			

(1) See the [Analog Input](#) section for more details.

(2) The common-mode overvoltage detection level has a typical hysteresis of 35 mV.

(3) The filter output is truncated to 16 bits. 16 bits of no missing codes is specified by design.

(4) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as number of LSBs or as a percent of the specified linear full-scale range FSR.

(5) Offset error drift is calculated using the box method, as described by the following equation:

$$TCE_O = \frac{value_{MAX} - value_{MIN}}{TempRange}$$

(6) Gain error drift is calculated using the box method, as described by the following equation:

$$TCE_G(ppm) = \left(\frac{value_{MAX} - value_{MIN}}{value \times TempRange} \right) \times 10^6$$

Electrical Characteristics (continued)

minimum and maximum specifications apply from $T_A = -40^{\circ}\text{C}$ to $+125^{\circ}\text{C}$, $V_{DD} = 3.0\text{ V}$ to 5.5 V , $A_{INP} = -1\text{ V}$ to 1 V , $A_{INN} = \text{GND}$, and sinc³ filter with $\text{OSR} = 256$ (unless otherwise noted); typical specifications are at $T_A = 25^{\circ}\text{C}$, $\text{CLKIN} = 20\text{ MHz}$, and $V_{DD} = 3.3\text{ V}$

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
AC ACCURACY						
SNR	Signal-to-noise ratio	f _{IN} = 1 kHz	81	87		dB
SINAD	Signal-to-noise + distortion	f _{IN} = 1 kHz	77	83		dB
THD	Total harmonic distortion	f _{IN} = 1 kHz		–87	–78	dB
SFDR	Spurious-free dynamic range	f _{IN} = 1 kHz	78	87		dB
REFERENCE OUTPUT						
V _{REFOUT}	Reference output voltage	Initial, at T _A = 25°C, no load	2.495	2.5	2.505	V
TCV _{REFOUT}	Reference output voltage drift		–50	±20	50	ppm/°C
I _{REFOUT}	Reference output current	C _{LOAD} < 1 nF ⁽⁷⁾	–5		5	mA
	Load regulation	Load to GND or VDD		0.15	0.35	mV/mA
I _{SC}	Short-circuit current	REFOUT to GND		23		mA
		REFOUT to VDD		–21		
PSRR	Power-supply rejection ratio		–200	±30	200	μV/V
DIGITAL INPUTS (CMOS Logic With Schmitt-Trigger)						
I _{IN}	Input current	GND ≤ V _{IN} ≤ VDD			35	μA
C _{IN}	Input capacitance			3		pF
V _{IH}	High-level input voltage		0.7 × VDD		VDD + 0.3	V
V _{IL}	Low-level input voltage		–0.3		0.3 × VDD	V
DIGITAL OUTPUT: CMOS						
C _{LOAD}	Output load capacitance	f _{CLKIN} = 21 MHz		15	30	pF
V _{OH}	High-level output voltage	I _{OH} = –20 μA	VDD – 0.1			V
		I _{OH} = –4 mA	VDD – 0.4			
V _{OL}	Low-level output voltage	I _{OL} = 20 μA			0.1	V
		I _{OL} = 4 mA			0.4	
POWER SUPPLY						
I _{VDD}	High-side supply current	3.0 V ≤ VDD ≤ 3.6 V, I _{REFOUT} = 0 mA, MCE = 0, C _{LOAD} = 15 pF		5.2	6.8	mA
		3.0 V ≤ VDD ≤ 3.6 V, I _{REFOUT} = 0 mA, MCE = 1, C _{LOAD} = 15 pF ⁽⁸⁾		4.6	6.1	
		4.5 V ≤ VDD ≤ 5.5 V, I _{REFOUT} = 0 mA, MCE = 0, C _{LOAD} = 15 pF		6.4	8.3	
		4.5 V ≤ VDD ≤ 5.5 V, I _{REFOUT} = 0 mA, MCE = 1, C _{LOAD} = 15 pF ⁽⁸⁾		5.4	7.2	

(7) Capacitive load with a value $\geq 1\text{ nF}$ requires series resistor to be connected to the REFOUT pin. See the [Reference Output](#) section for more details.

(8) Typical value is specified at $f_{CLKIN} = 10\text{ MHz}$, maximum value is specified at $f_{CLKIN} = 11\text{ MHz}$.

6.6 Switching Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
f_{CLKIN}	CLKIN clock frequency	MCE = 0	9	20	21	MHz
		MCE = 1	9	10	11	
Duty _{Cycle}	CLKIN clock duty cycle ⁽¹⁾		40%	50%	60%	
t_{H1}	DOUT hold time after rising edge of CLKIN	MCE = 0, $C_{\text{LOAD}} = 15 \text{ pF}$	6			ns
t_{H2}	DOUT hold time after rising edge of CLKIN	MCE = 1, $C_{\text{LOAD}} = 15 \text{ pF}$	6		23	ns
t_{H3}	DOUT hold time after falling edge of CLKIN	MCE = 1, $C_{\text{LOAD}} = 15 \text{ pF}$	10		26	ns
t_{D1}	Rising edge of CLKIN to DOUT valid delay	MCE = 0, $C_{\text{LOAD}} = 15 \text{ pF}$			25	ns
t_{D2}	Rising edge of CLKIN to DOUT valid delay	MCE = 1, $C_{\text{LOAD}} = 15 \text{ pF}$	11		27	ns
t_{D3}	Falling edge of CLKIN to DOUT valid delay	MCE = 1, $C_{\text{LOAD}} = 15 \text{ pF}$	15		30	ns
t_r	DOUT rise time	10% to 90%, $3.0 \text{ V} \leq \text{VDD} \leq 3.6 \text{ V}$, $C_{\text{LOAD}} = 15 \text{ pF}$		2.5	5	ns
		10% to 90%, $4.5 \text{ V} \leq \text{VDD} \leq 5.5 \text{ V}$, $C_{\text{LOAD}} = 15 \text{ pF}$		1.5	3.5	
t_f	DOUT fall time	90% to 10%, $3.0 \text{ V} \leq \text{VDD} \leq 3.6 \text{ V}$, $C_{\text{LOAD}} = 15 \text{ pF}$		2.5	5.8	ns
		90% to 10%, $4.5 \text{ V} \leq \text{VDD} \leq 5.5 \text{ V}$, $C_{\text{LOAD}} = 15 \text{ pF}$		1.8	4.4	
t_{ASTART}	Analog startup time	VDD step to 3.0 V, 0.1% settling, CLKIN applied		0.25		ms

(1) The duty cycle of DOUT equals the clock duty cycle of the applied CLKIN signal.

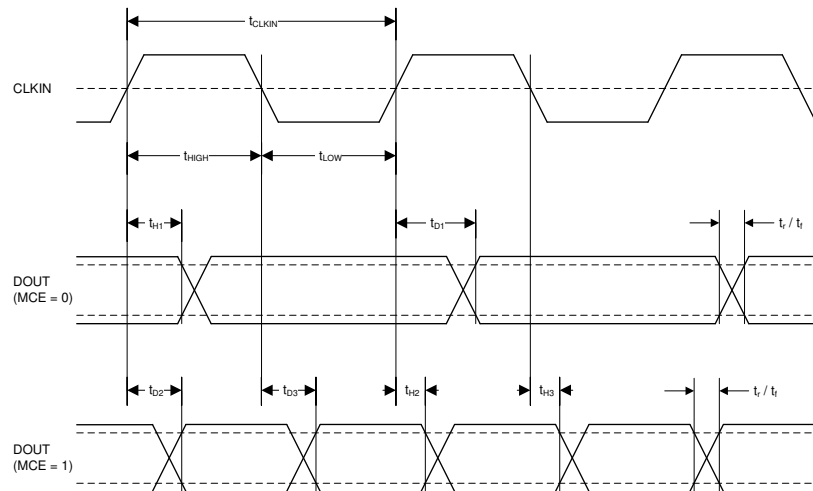


图 1. Digital Interface Timing

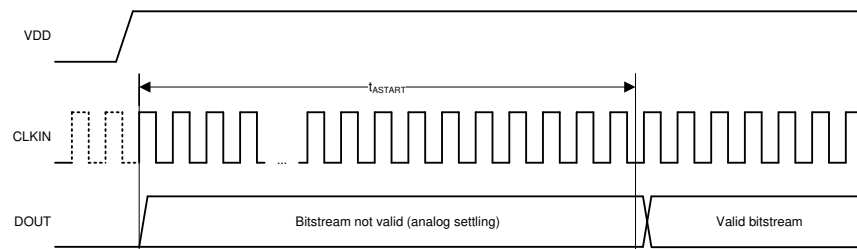


图 2. Device Startup Timing

6.7 Typical Characteristics

at $V_{DD} = 3.3\text{ V}$, $A_{INP} = -1\text{ V}$ to 1 V , $A_{INN} = \text{GND}$, $f_{CLKIN} = 20\text{ MHz}$, $MCE = 0$, and sinc³ filter with $OSR = 256$ (unless otherwise noted)

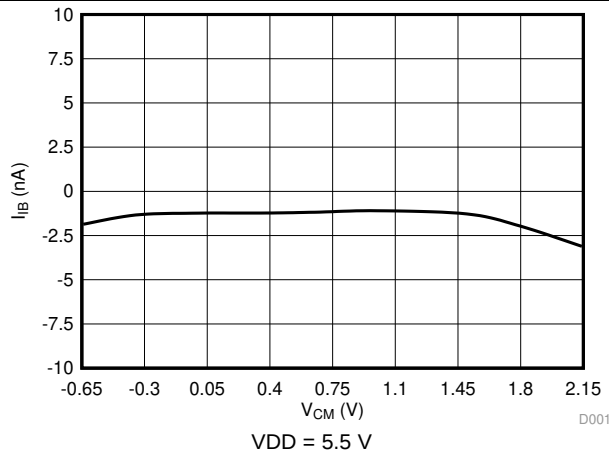


图 3. Input Bias Current vs Common-Mode Input Voltage

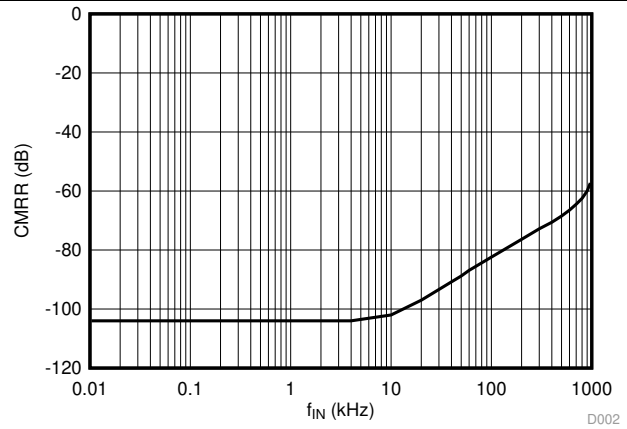


图 4. Common-Mode Rejection Ratio vs Input Signal Frequency

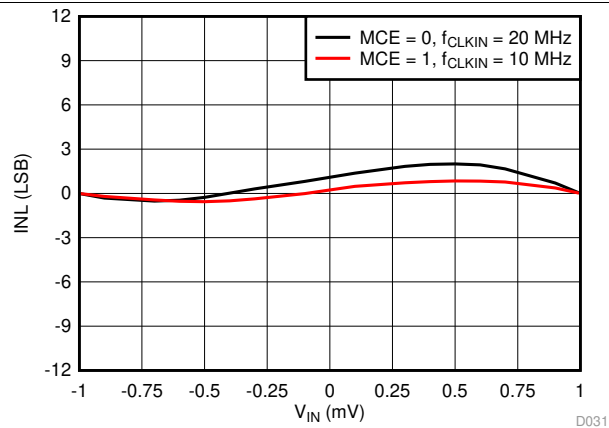


图 5. Integral Nonlinearity vs Input Voltage

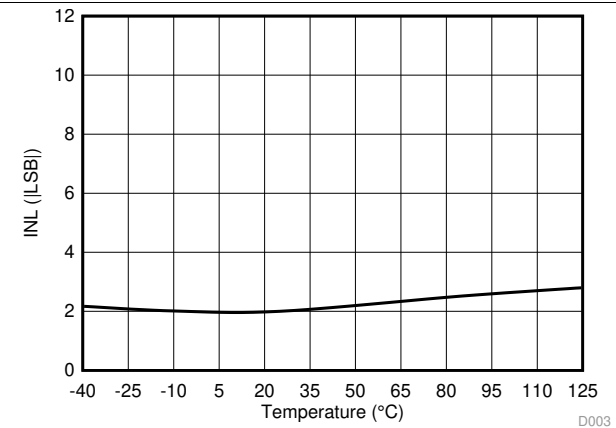


图 6. Integral Nonlinearity vs Temperature

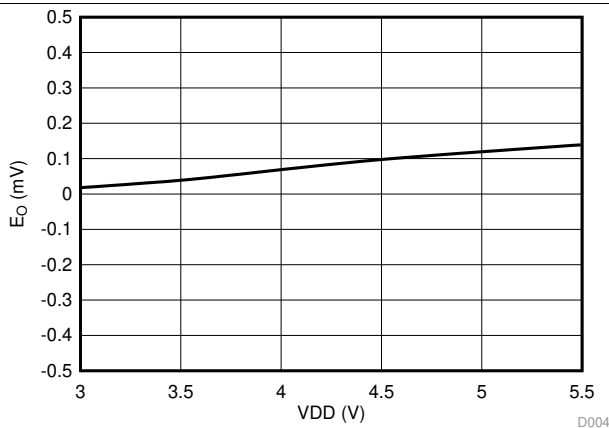


图 7. Offset Error vs Supply Voltage

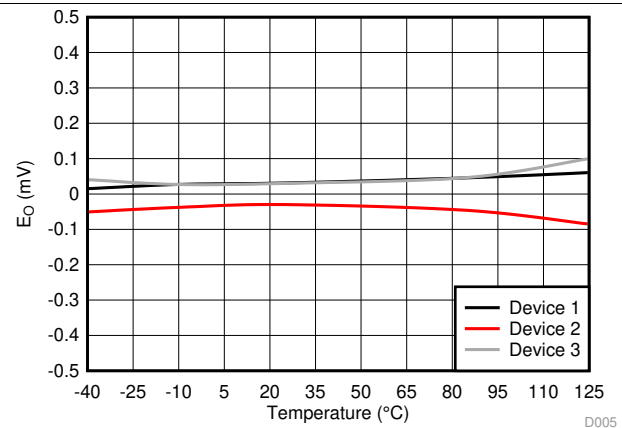


图 8. Offset Error vs Temperature

Typical Characteristics (continued)

at $V_{DD} = 3.3\text{ V}$, $A_{INP} = -1\text{ V}$ to 1 V , $A_{INN} = \text{GND}$, $f_{CLKIN} = 20\text{ MHz}$, $MCE = 0$, and sinc³ filter with $OSR = 256$ (unless otherwise noted)

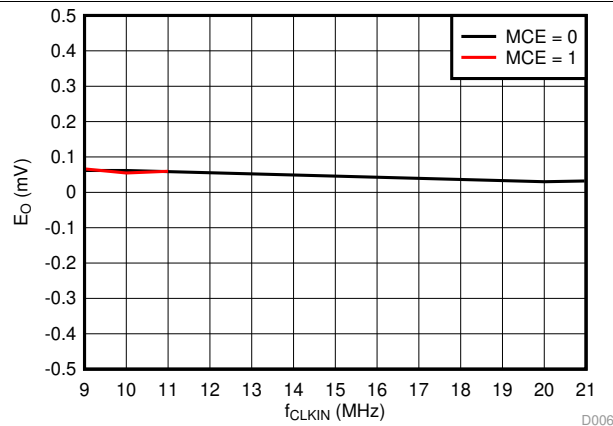


Figure 9. Offset Error vs Clock Frequency

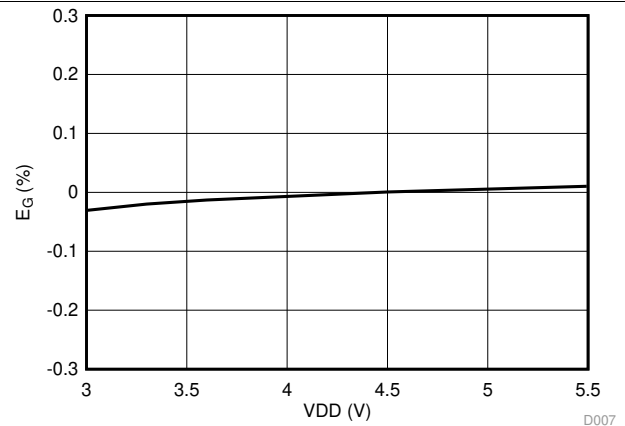


Figure 10. Gain Error vs Supply Voltage

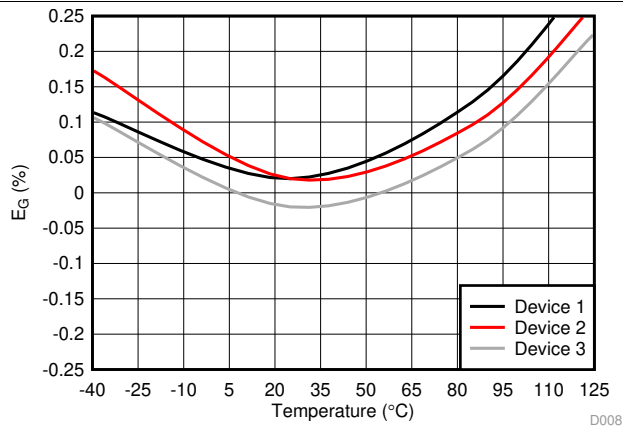


Figure 11. Gain Error vs Temperature

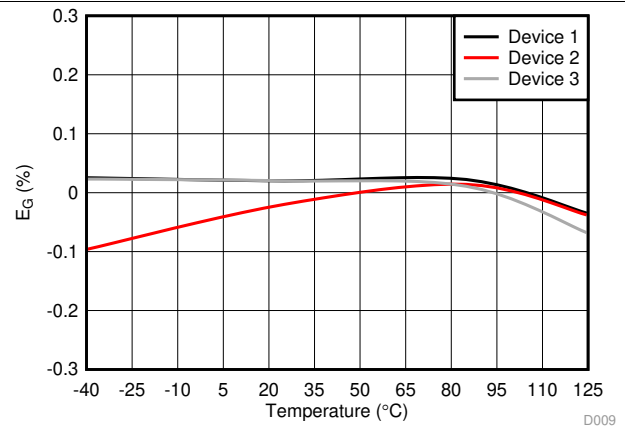


Figure 12. Ratiometric Gain Error vs Temperature

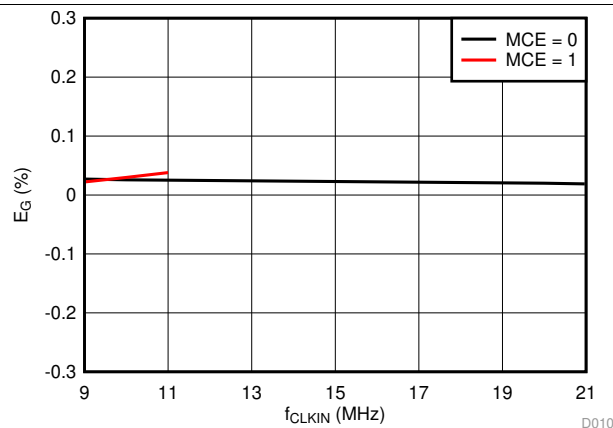


Figure 13. Gain Error vs Clock Frequency

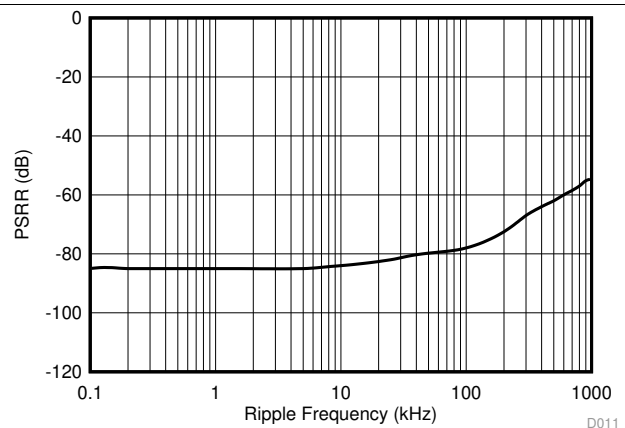


Figure 14. Power-Supply Rejection Ratio vs Ripple Frequency

Typical Characteristics (continued)

at $V_{DD} = 3.3\text{ V}$, $A_{INP} = -1\text{ V}$ to 1 V , $A_{INN} = \text{GND}$, $f_{CLKIN} = 20\text{ MHz}$, $MCE = 0$, and sinc³ filter with $OSR = 256$ (unless otherwise noted)

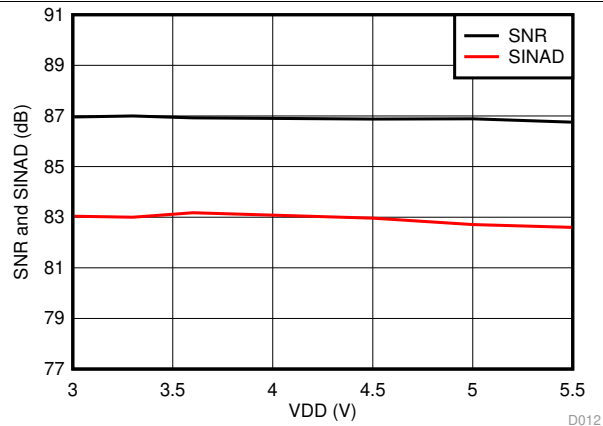


Figure 15. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Supply Voltage

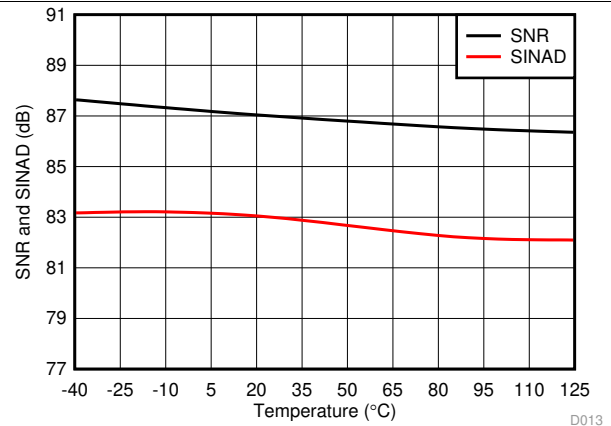


Figure 16. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Temperature

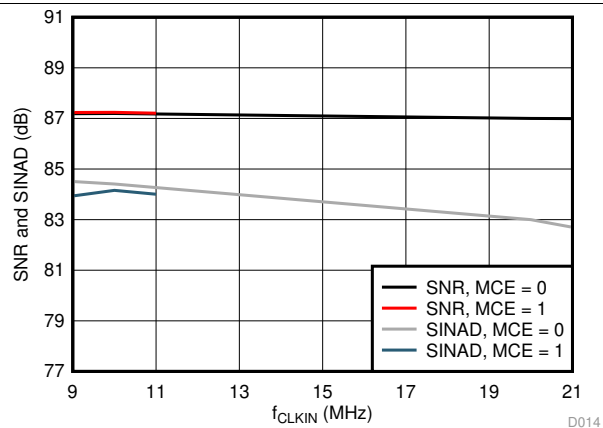


Figure 17. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Clock Frequency

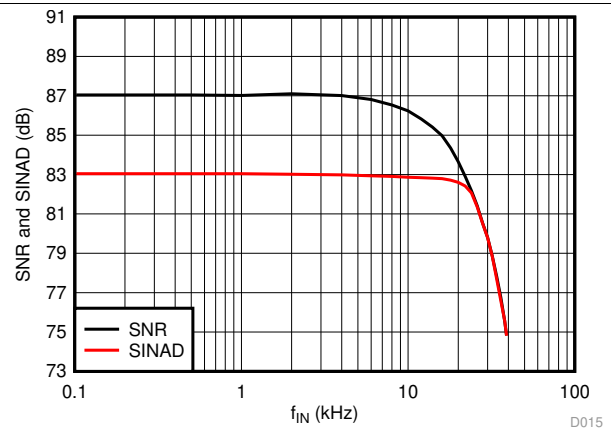


Figure 18. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Input Signal Frequency

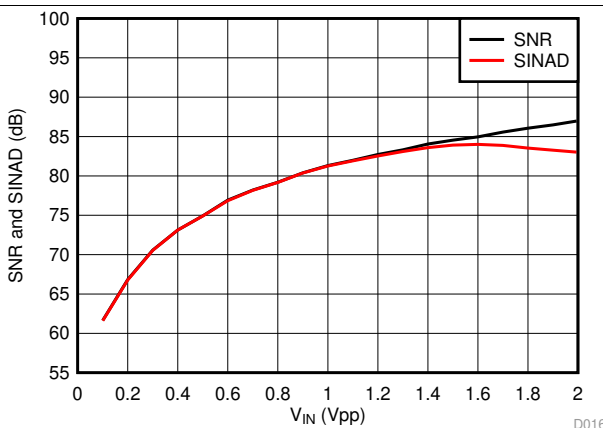


Figure 19. Signal-to-Noise Ratio and Signal-to-Noise + Distortion vs Input Signal Amplitude

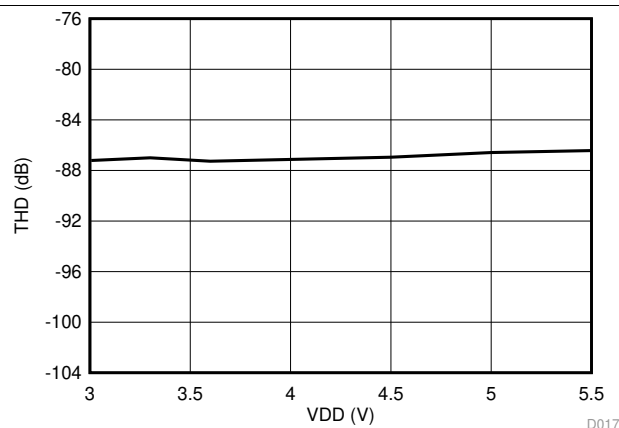


Figure 20. Total Harmonic Distortion vs Supply Voltage

Typical Characteristics (continued)

at $V_{DD} = 3.3\text{ V}$, $A_{INP} = -1\text{ V}$ to 1 V , $A_{INN} = \text{GND}$, $f_{CLKIN} = 20\text{ MHz}$, $MCE = 0$, and sinc³ filter with $OSR = 256$ (unless otherwise noted)

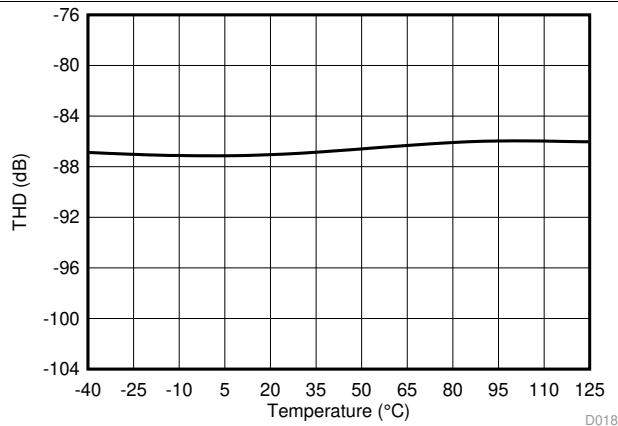


Figure 21. Total Harmonic Distortion vs Temperature

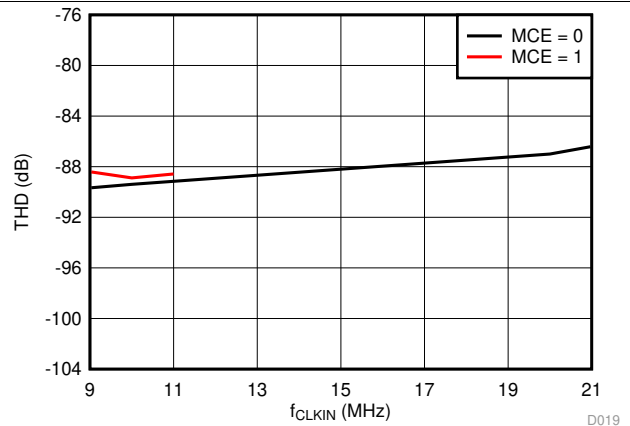


Figure 22. Total Harmonic Distortion vs Clock Frequency

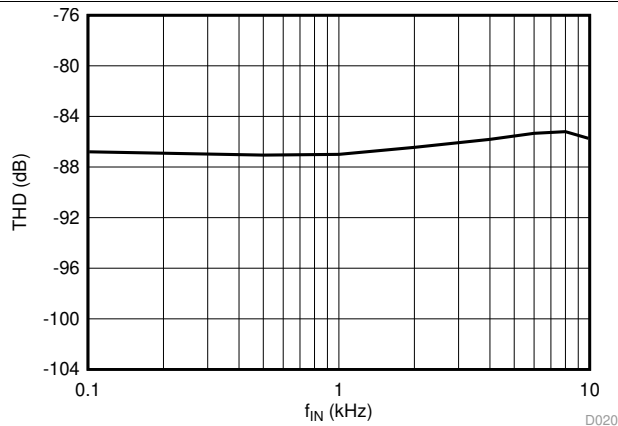


Figure 23. Total Harmonic Distortion vs Input Signal Frequency

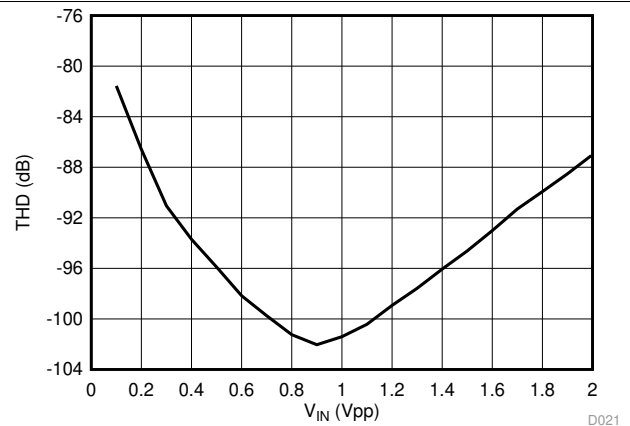


Figure 24. Total Harmonic Distortion vs Input Signal Amplitude

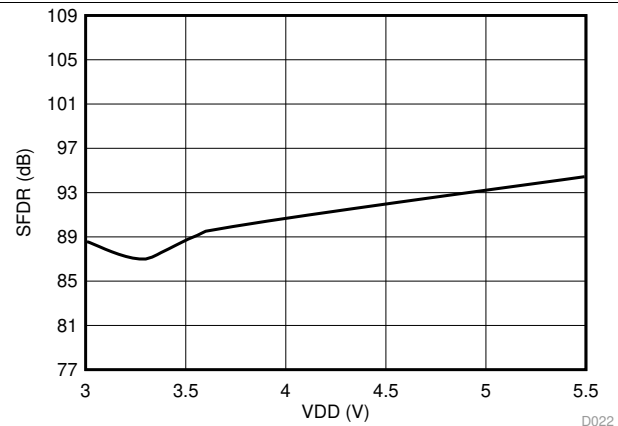


Figure 25. Spurious-Free Dynamic Range vs Supply Voltage

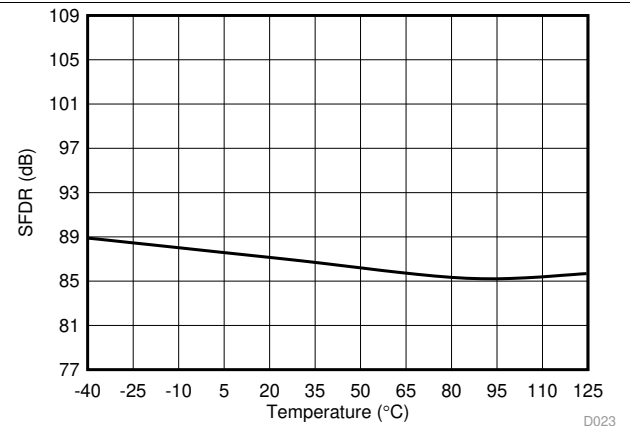


Figure 26. Spurious-Free Dynamic Range vs Temperature

Typical Characteristics (continued)

at $V_{DD} = 3.3\text{ V}$, $A_{INP} = -1\text{ V}$ to 1 V , $A_{INN} = \text{GND}$, $f_{CLKIN} = 20\text{ MHz}$, $MCE = 0$, and sinc^3 filter with $\text{OSR} = 256$ (unless otherwise noted)

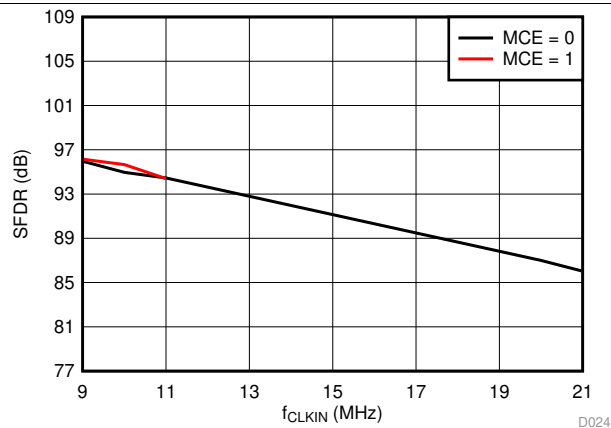


Figure 27. Spurious-Free Dynamic Range vs Clock Frequency

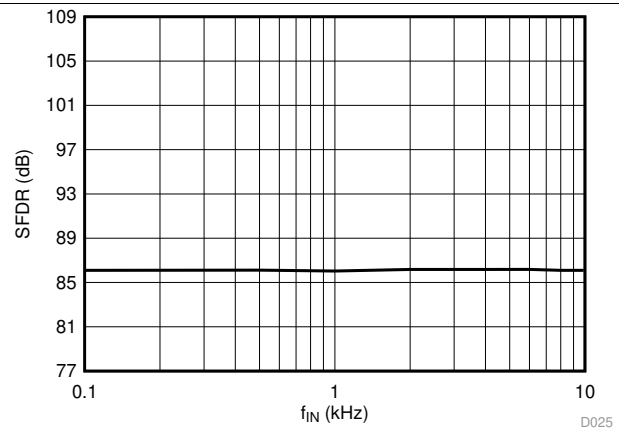


Figure 28. Spurious-Free Dynamic Range vs Input Signal Frequency

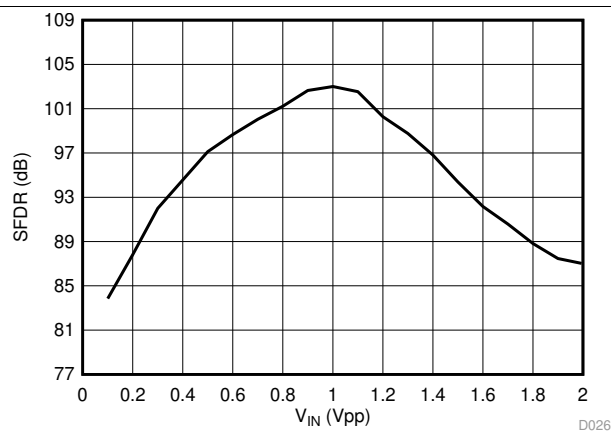


Figure 29. Spurious-Free Dynamic Range vs Input Signal Amplitude

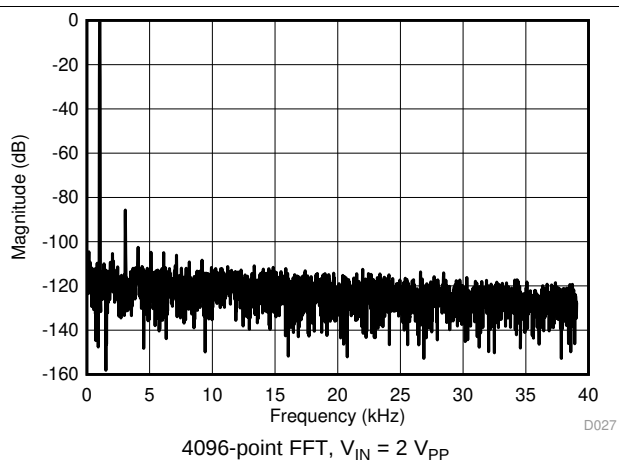


Figure 30. Frequency Spectrum With 1-kHz Input Signal

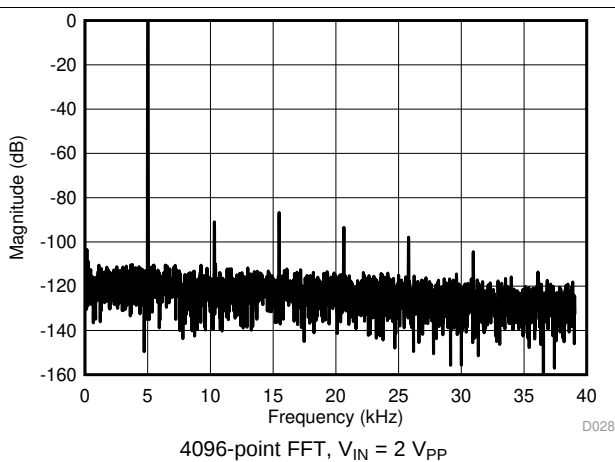


Figure 31. Frequency Spectrum With 5-kHz Input Signal

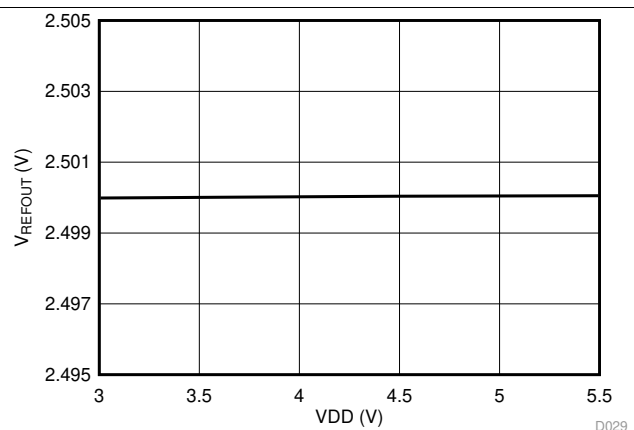


Figure 32. Reference Output Voltage vs Supply Voltage

Typical Characteristics (continued)

at $V_{DD} = 3.3\text{ V}$, $A_{INP} = -1\text{ V}$ to 1 V , $A_{INN} = \text{GND}$, $f_{CLKIN} = 20\text{ MHz}$, $MCE = 0$, and sinc³ filter with $OSR = 256$ (unless otherwise noted)

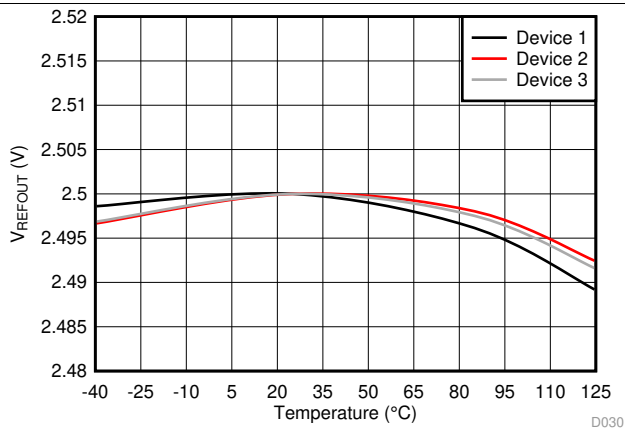


Figure 33. Reference Output Voltage vs Temperature

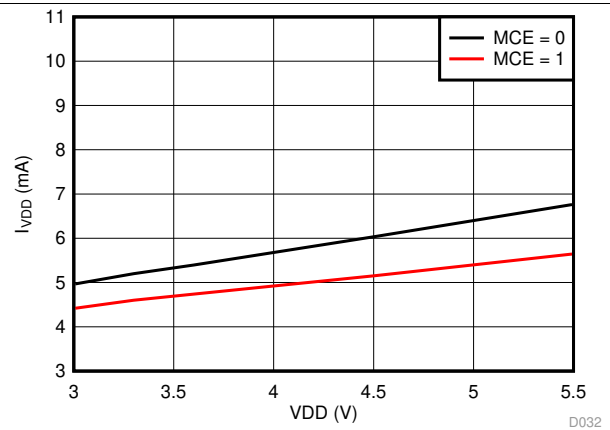


Figure 34. Supply Current vs Supply Voltage

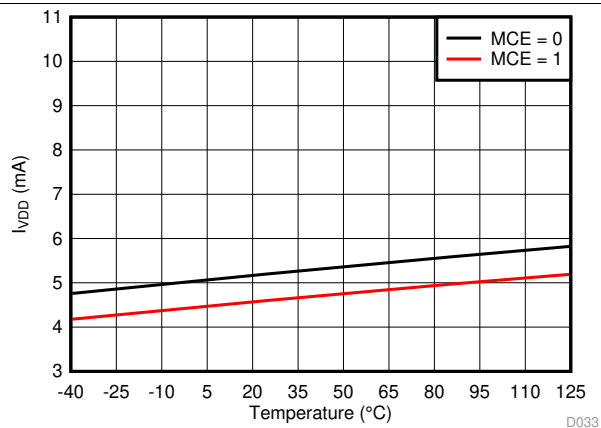


Figure 35. Supply Current vs Temperature

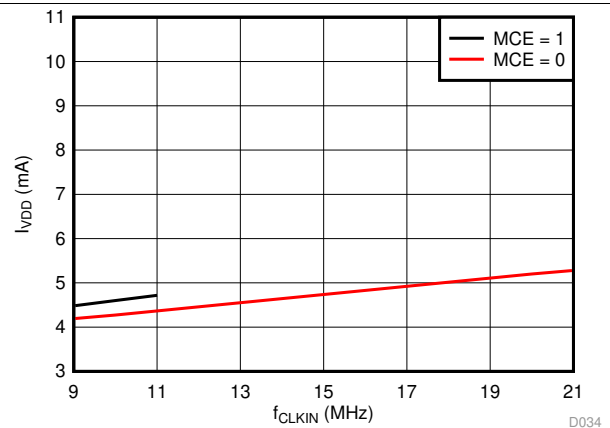


Figure 36. Supply Current vs Clock Frequency

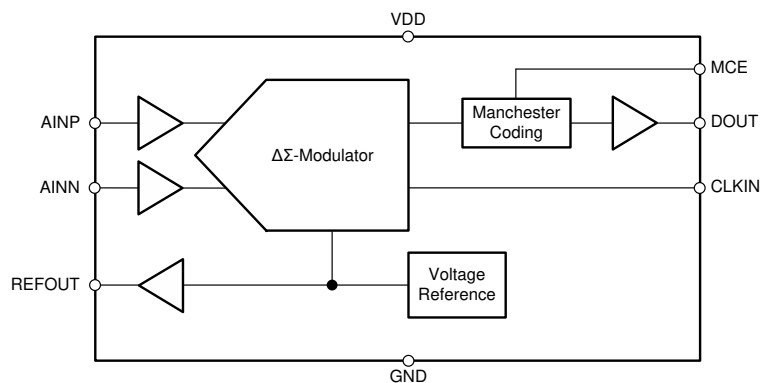
7 Detailed Description

7.1 Overview

The differential analog input (comprised of input signals AINP and AINN) of the AMC1035 is a chopper-stabilized buffer, followed by the switched-capacitor input of a second-order, delta-sigma ($\Delta\Sigma$) modulator stage that digitizes the input signal into a 1-bit output stream. The data output DOUT of the converter provides a stream of digital ones and zeros that is synchronous to the externally-provided clock source at the CLKIN pin with a frequency in the range of 9 MHz to 21 MHz. The time average of this serial bitstream output is proportional to the analog input voltage.

The [Functional Block Diagram](#) section shows a detailed block diagram of the AMC1035. The 1.6-G Ω differential input resistance of the analog input stage supports low gain-error signal sensing in high-voltage applications using resistive dividers. The external clock input simplifies the synchronization of multiple measurement channels on the system level. The extended frequency range of up to 21 MHz supports higher performance levels compared to the other solutions available on the market.

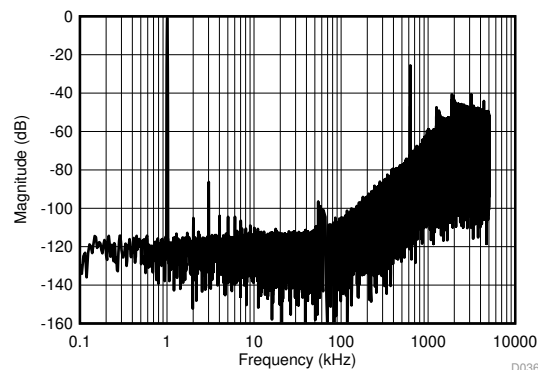
7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Analog Input

The AMC1035 incorporates front-end circuitry that contains a buffered sampling stage, followed by a $\Delta\Sigma$ modulator. To support a bipolar input range, the device uses a charge pump that allows single-supply operation to simplify the overall system design and minimize the circuit cost. For reduced offset and offset drift, the input buffer is chopper-stabilized with the switching frequency set at $f_{CLKIN} / 32$. [Figure 37](#) shows the spur created by the switching frequency.



sinc^3 filter, $\text{OSR} = 2$, $f_{CLKIN} = 20 \text{ MHz}$, $f_{IN} = 1 \text{ kHz}$

Figure 37. Quantization Noise Shaping

Feature Description (continued)

The linearity and noise performance of the device are ensured only when the differential analog input voltage remains within the specified linear full-scale range (FSR), that is ± 1 V, and within the specified input common-mode range.

Figure 38 shows the specified common-mode input voltage that applies for the full-scale input voltage range as specified in this document along with the corresponding common-mode undervoltage and overvoltage threshold levels.

If smaller input signals are used, the operational common-mode input voltage range widens. Figure 39 shows the common-mode input voltage that applies with no differential input signal; that is, when the voltage applied on AINP is equal to the voltage applied on AINN. The common-mode input voltage range scales with the actual differential input voltage between this range and the range in Figure 38.

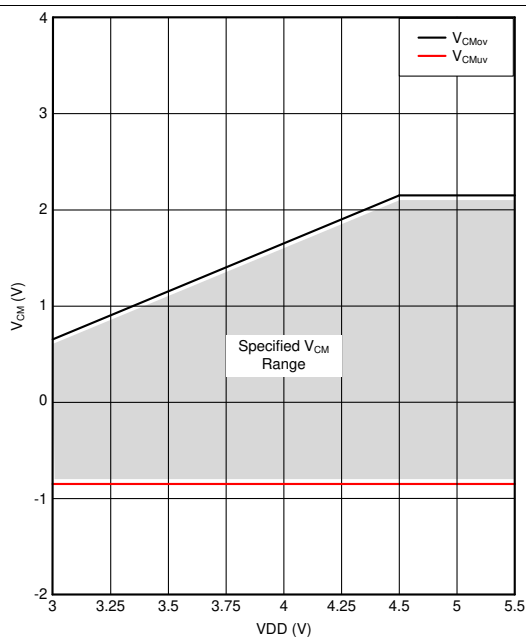


Figure 38. Common-Mode Input Voltage Range With a Full-Scale Differential Input Signal of ± 1.25 V

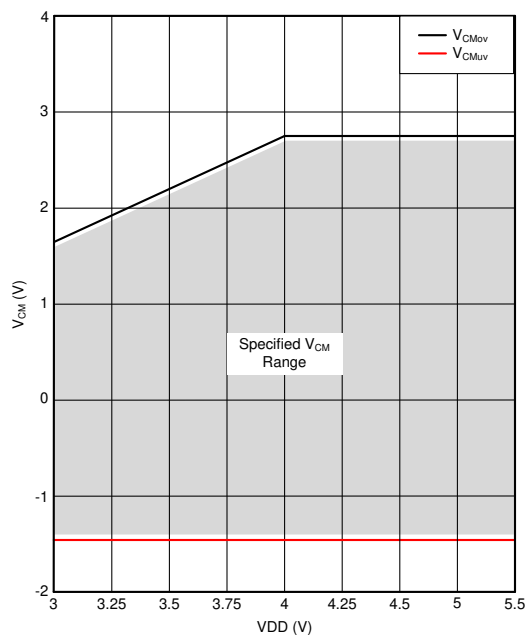


Figure 39. Common-Mode Input Voltage Range With a Zero Differential Input Signal

Feature Description (continued)

7.3.2 Modulator

The modulator implemented in the AMC1035 (such as the one conceptualized in [Figure 40](#)) is a second-order, switched-capacitor, feed-forward $\Delta\Sigma$ modulator. The analog input voltage V_{IN} and the output V_5 of the 1-bit digital-to-analog converter (DAC) are subtracted, providing an analog voltage V_1 at the input of the first integrator stage. The output of the first integrator feeds the input of the second integrator stage, resulting in output voltage V_3 that is summed with the input signal V_{IN} and the output of the first integrator V_2 . Depending on the polarity of the resulting voltage V_4 , the output of the comparator is changed. In this case, the 1-bit DAC responds on the next clock pulse by changing the associated analog output voltage V_5 , causing the integrators to progress in the opposite direction and forcing the value of the integrator output to track the average value of the input.

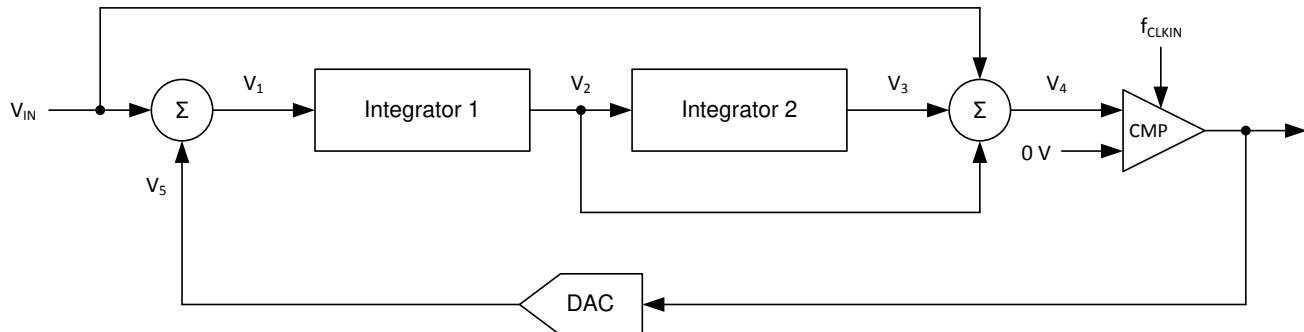


Figure 40. Block Diagram of a Second-Order Modulator

As depicted in [Figure 37](#), the modulator shifts the quantization noise to high frequencies. Therefore, use a low-pass digital filter at the output of the device to increase the overall performance. This filter is also used to convert from the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). TI's microcontroller families [TMS320F28004x](#), [TMS320F2807x](#), and [TMS320F2837x](#) offer a suitable programmable, hardwired filter structure termed a *sigma-delta filter module* (SDFM) optimized for usage with the AMC1035. Also, SD24_B converters on the [MSP430F677x](#) microcontrollers offer a path to directly access the integrated sinc-filters for a simple system-level solution for multichannel, isolated current sensing. An additional option is to use a suitable application-specific device, such as the [AMC1210](#) (a four-channel digital sinc filter). Alternatively, a field-programmable gate array (FPGA) can be used to implement the filter.

7.3.3 Reference Output

The AMC1035 offers a voltage reference output that can source or sink current to significantly reduce the gain error thermal drift in ratiometric applications as specified in the [Electrical Characteristics](#) table. The [IGBT Temperature Sensing](#) section provides an example of a ratiometric use case for the AMC1035.

The reference output can drive capacitive loads less than 1 nF. Use a series resistor to avoid oscillations and degradation of performance for capacitive loads ≥ 1 nF. [Table 1](#) lists the recommended series resistor values for given capacitor value examples. Interpolate for capacitive loads with a value between the given examples.

Table 1. Series Resistor Value for Capacitive Loads ≥ 1 nF on REFOUT Pin

CAPACITIVE LOAD ON REFOUT PIN	1 nF	3.3 nF	10 nF	33 nF	100 nF	330 nF	1 μ F	3.3 μ F	10 μ F
Recommended series resistor	33 Ω	56 Ω	47 Ω	33 Ω	15 Ω	10 Ω	5.6 Ω	3.3 Ω	1.8 Ω

7.3.4 Clock Input

The AMC1035 system clock is provided externally at the CLKIN pin. The clock signal must be applied continuously for proper device operation.

To support the bipolar input voltage range with a single supply, the AMC1035 includes a charge pump. This charge pump stops operating if the clock signal is below the specified frequency range or if the signal is paused or missing. Additionally, the input bias current increases beyond the specified range and significantly reduces the input resistance of the device. When the clock signal is paused or missing, the modulator stops the analog signal conversion and the digital output signal remains frozen in the last logic state. When the clock signal is applied again after a pause, the internal analog circuitry biasing must settle for proper device performance. In this case, consider the t_{ASTART} specification in the [Switching Characteristics](#) table.

7.3.5 Digital Output

A differential input signal of 0 V ideally produces a stream of ones and zeros that are high 50% of the time. A differential input of 1 V produces a stream of ones and zeros that are high 90% of the time. With 16 bits of resolution, that percentage ideally corresponds to code 58982 (an unsigned code). A differential input of –1 V produces a stream of ones and zeros that are high 10% of the time and ideally results in code 6553 with 16-bit resolution. These input voltages are also the specified linear range of the AMC1035 with performance as specified in this document. If the input voltage value exceeds this range, the output of the modulator shows nonlinear behavior when the quantization noise increases. The output of the modulator clips with a stream of only zeros with an input less than or equal to –1.25 V or with a stream of only ones with an input greater than or equal to 1.25 V. In this case, however, the AMC1035 generates a single 1 (if the input is at negative full-scale) or 0 every 128 clock cycles to indicate proper device function (see the [Fail-Safe Output](#) section for more details). [Figure 41](#) shows the input voltage versus the output modulator signal.

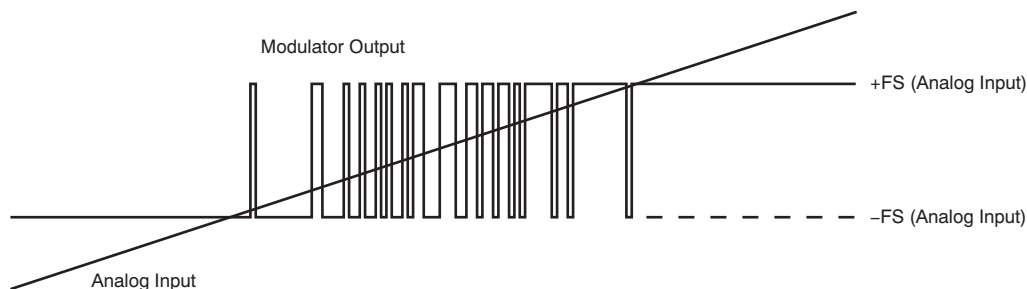


Figure 41. Analog Input versus the AMC1035 Modulator Output

[Equation 1](#) calculates the density of ones in the output bitstream for any input voltage value (with the exception of a full-scale input signal, as described in the [Output Behavior in Case of a Full-Scale Input](#) section):

$$\frac{V_{\text{IN}} + V_{\text{Clipping}}}{2 \times V_{\text{Clipping}}} \quad (1)$$

The modulator bitstream on the DOUT pin changes with the rising edge of the clock signal applied on the CLKIN pin. Use the rising edge of the clock to latch the modulator bitstream at the input of the digital filter device.

7.3.6 Manchester Coding Feature

The AMC1035 offers the IEEE 802.3-compliant Manchester coding feature that generates at least one transition per bit to support clock signal recovery from the bitstream. The Manchester coding combines the clock and data information using exclusive-OR (XOR) logical operation that results in a bitstream free of DC components. [Figure 42](#) shows the resulting bitstream from this coding. The duty cycle of the Manchester encoded bitstream depends on the duty cycle of the input clock CLKIN. To enable Manchester coding on the AMC1035, pull the input pin MCE high. The DOUT signal is inverted if the MCE status changes when CLKIN is high.

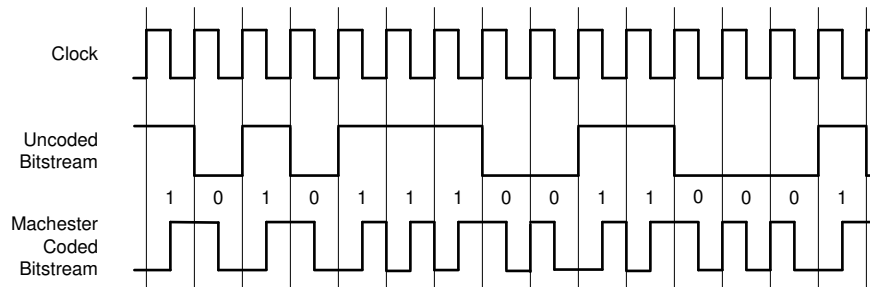


Figure 42. Manchester Coded Output of the AMC1035

7.4 Device Functional Modes

The AMC1035 is operational when the power supply VDD and clock signal CLKIN are applied, as specified in [Table 39](#) and the [Switching Characteristics](#) table.

7.4.1 Output Behavior in Case of a Full-Scale Input

If a full-scale input signal is applied to the AMC1035 (that is, $|V_{IN}| \geq |V_{Clipping}|$), the device generates a single one or zero every 128 bits at DOUT, as shown in [Figure 43](#), depending on the actual polarity of the signal being sensed. This feature is also supported with Manchester-coded output and allows full-scale and invalid input signals to be identified as described in the [Fail-Safe Output](#) section and can be used for advanced system-level diagnostics.

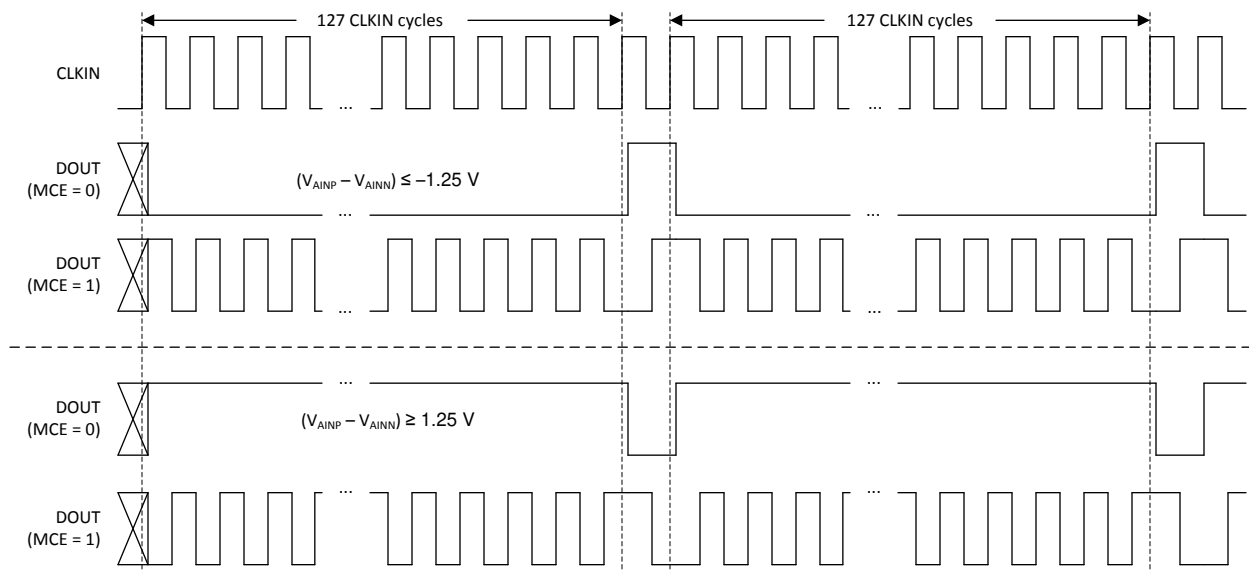


Figure 43. Overrange Output of the AMC1035

Device Functional Modes (continued)

7.4.2 Fail-Safe Output

Figure 44 shows that if the common-mode voltage of the input reaches or exceeds the specified common-mode undervoltage, V_{CMUV} , or overvoltage detection level, V_{CMOV} as defined in the [Electrical Characteristics](#) table, the DOUT of the AMC1035 is held at steady-state high.

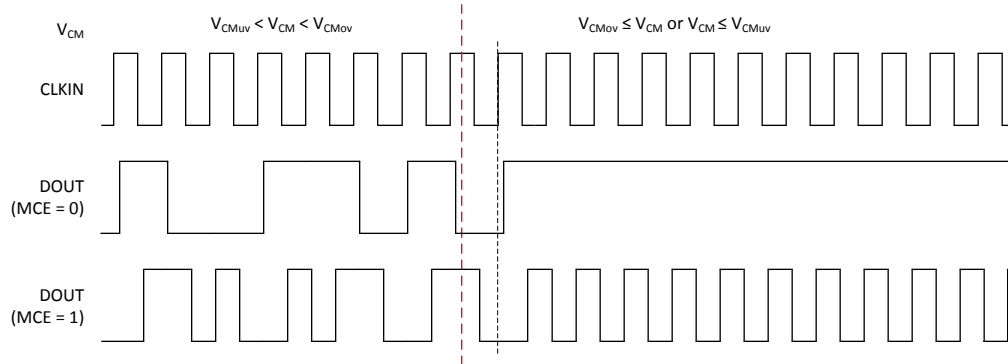


Figure 44. Fail-Safe Output of the AMC1035

8 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

8.1.1 Digital Filter Usage

The modulator generates a bitstream that is processed by a digital filter to obtain a digital word similar to a conversion result of a conventional analog-to-digital converter (ADC). Figure 2 shows a sinc^3 -type filter, which is a very simple filter, built with minimal effort and hardware:

$$H(z) = \left(\frac{1 - z^{-\text{OSR}}}{1 - z^{-1}} \right)^3 \quad (2)$$

This filter provides the best output performance at the lowest hardware size (count of digital gates) for a second-order modulator. All the characterization in this document is also done with a sinc^3 filter with an oversampling ratio (OSR) of 256 and an output word width of 16 bits.

An example code for implementing a sinc^3 filter in an FPGA is discussed in the [Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications](#) application note, available for download at www.ti.com.

8.2 Typical Applications

8.2.1 Voltage Sensing

$\Delta\Sigma$ modulators are widely used in frequency inverter designs because of their high AC and DC performance. Frequency inverters are critical parts of industrial motor drives, photovoltaic inverters (string and central inverters), uninterruptible power supplies (UPS), and other industrial applications.

Figure 45 shows a simplified schematic of a motor drive application with the AMC1035 used for the DC-link and output phase voltage sensing. In this example, all resistive dividers reference to the negative DC-link voltage that is also used as a ground reference point for the microcontroller. An additional fifth AMC1035 can be used for temperature sensing of the insulated-gate bipolar transistor (IGBT) module; see the [IGBT Temperature Sensing](#) section for more details.

Current feedback is performed with shunt resistors (R_{SHUNT}) and TI's [AMC1306M25](#) isolated modulators. Depending on the system design, either all three or only two motor phase currents are sensed.

Depending on the overall digital processing power requirements and with a total of eight $\Delta\Sigma$ modulator bitstreams to be processed by the MCU, a derivative from either the low-cost single-core [TMS320F2807x](#) or the dual-core [TMS320F2837x](#) families can be used in this application.

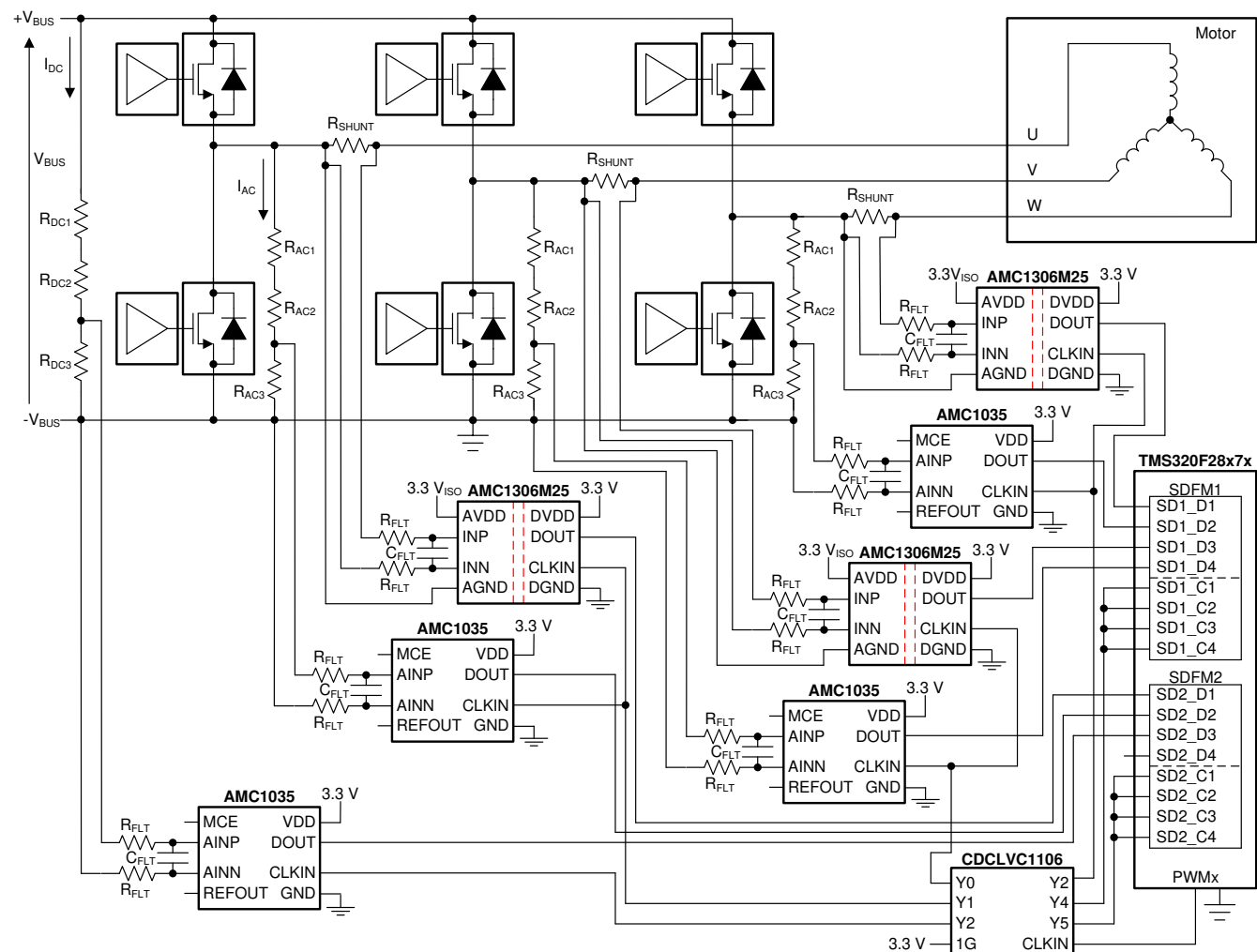


Figure 45. The AMC1035 in a Frequency Inverter Application

Typical Applications (continued)

8.2.1.1 Design Requirements

表 2 lists the parameters for this typical application.

表 2. Design Requirements

PARAMETER	VALUE
Supply voltage	3.3 V
Voltage drop across the sensing resistor R_{DC1} for a linear response	1 V (maximum)
Voltage drop across the sensing resistors R_{ACx} for a linear response	± 1 V (maximum)
Current through the sensing resistors R_{ACx}	± 100 μ V (maximum)

8.2.1.2 Detailed Design Procedure

Use Ohm's Law to calculate the minimum total resistance of the resistive dividers to limit the cross current to the desired values:

- For the voltage sensing on the DC bus: $R_{DC1} + R_{DC2} + R_{DC3} = V_{BUS} / I_{DC}$
- For the voltage sensing on the output phases U, V, and W: $R_{AC1} + R_{AC2} + R_{AC3} = V_{PHASE(max)} / I_{AC}$

Consider the following two restrictions to choose the proper value of the resistors R_{DC3} and R_{AC3} :

- The voltage drop caused by the nominal voltage range of the system must not exceed the recommended input voltage range of the AMC1035: $V_{XC3} \leq V_{FSR}$
- The voltage drop caused by the maximum allowed system overvoltage must not exceed the input voltage that causes a clipping output: $V_{XC3} \leq V_{Clipping}$

Use similar approach for calculation of the shunt resistor values R_{SHUNT} and see the [AMC1306M25 data sheet](#) for further details.

表 3 lists examples of nominal E96-series (1% accuracy) resistor values for systems using 600 V and 800 V on the DC bus.

表 3. Resistor Value Examples for DC Bus Sensing

PARAMETER	600-V DC BUS	800-V DC Bus
Resistive divider resistor R_{DC1}	3.01 M Ω	4.22 M Ω
Resistive divider resistor R_{DC2}	3.01 M Ω	4.22 M Ω
Sense resistor R_{DC3}	10 k Ω	10.5 k Ω
Resulting current through resistive divider I_{DC}	99.5 μ A	94.7 μ A
Resulting voltage drop on sense resistor V_{RDC3}	0.995 V	0.994 V

表 4 lists examples of nominal E96-series (1% accuracy) resistor values for systems using 230 V and 690 V on the output phases.

表 4. Resistor Value Examples for Output Phase Voltage Sensing

PARAMETER	± 400 -V _{AC} PHASE	± 690 -V _{AC} PHASE
Resistive divider resistor R_{AC1}	2.0 M Ω	3.48 M Ω
Resistive divider resistor R_{AC2}	2.0 M Ω	3.48 M Ω
Sense resistor R_{AC3}	10.0 k Ω	10.0 k Ω
Resulting current through resistive divider I_{AC}	99.8 μ A	99.0 μ A
Resulting voltage drop on sense resistor V_{RAC3}	± 0.998 V	± 0.990 V

Use a power supply with a nominal voltage of 3.3 V to directly connect all modulators to the microcontroller.

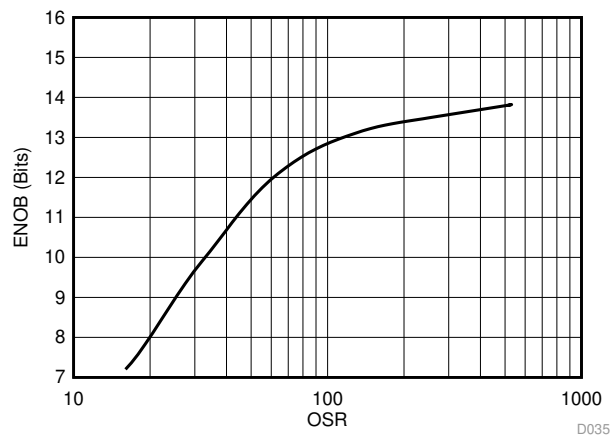
For modulator output bitstream filtering, a device from TI's [TMS320F2807x](#) family of low-cost microcontrollers (MCUs) or [TMS320F2837x](#) family of dual-core MCUs is recommended. These MCU families support up to eight channels of dedicated hardwired filter structures called sigma-delta filter modules (SDFMs) that significantly simplify system level design by offering two filtering paths per channel: one providing high accuracy results for the control loop and one that offers a fast response path for overcurrent detection. Use one of the pulse-width modulation (PWM) sources inside the MCU to generate the clock for the modulators and for easy synchronization of all feedback signals and the switching control of the gate drivers.

[Figure 45](#) uses a clock buffer to distribute the clock reference signal generated on one of the PWM outputs of the MCU (called PWMx in [Figure 45](#)) to all modulators used in the circuit and as a reference for the digital filters in the MCU. In this example, TI's [CDCLVC1106](#) is used for this purpose. Each CDCLVC1106 output can drive a load of 8 pF that is sufficient to drive up to two modulator and up to four SDFM clock inputs.

8.2.1.3 Application Curve

The effective number of bits (ENOB) is often used to compare the performance of ADCs and $\Delta\Sigma$ modulators. [Figure 46](#) shows the ENOB of the AMC1035 with different oversampling ratios on a sinc3 filter. This number is calculated from the SINAD by using [Equation 3](#) in this document.

$$\text{SINAD} = 1.76 \text{ dB} + 6.02 \text{ dB} \times \text{ENOB} \quad (3)$$



Sinc3 filter

Figure 46. Measured Effective Number of Bits vs Oversampling Ratio

8.2.2 IGBT Temperature Sensing

The high input impedance of the AMC1035 is optimized for usage in voltage-sensing applications. Additionally, the internal voltage reference supports temperature sensing using a positive temperature coefficient (PTC) or a negative temperature coefficient (NTC) sensor often integrated in the IGBT module.

The same reference is internally used by the modulator, resulting in a ratiometric system solution that minimizes the overall temperature drift of the sensing path. [Figure 47](#) shows a simplified schematic of the AMC1035 used for temperature sensing of the IGBT module.

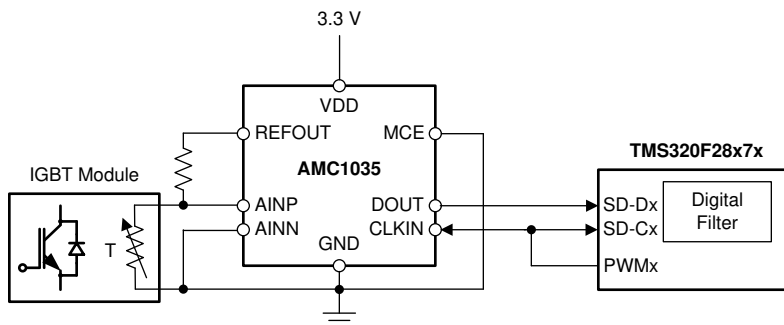


Figure 47. Using the AMC1035 for Temperature Sensing

8.2.3 What to Do and What Not to Do

Do not leave the analog inputs of the AMC1035 unconnected (floating) when the device is powered up. If either modulator input is left floating, the input bias current may drive this input beyond the specified common-mode input voltage range. If both inputs are beyond that range, the gain of the front-end diminishes. In both cases, the modulator outputs a fail-safe bitstream as described in the [Fail-Safe Output](#) section.

9 Power Supply Recommendations

For decoupling of the power supply, a 0.1- μ F capacitor is recommended to be placed as close to the VDD pin of the AMC1035 as possible, as shown in [Figure 48](#), followed by an additional capacitor in the range of 1 μ F to 10 μ F.

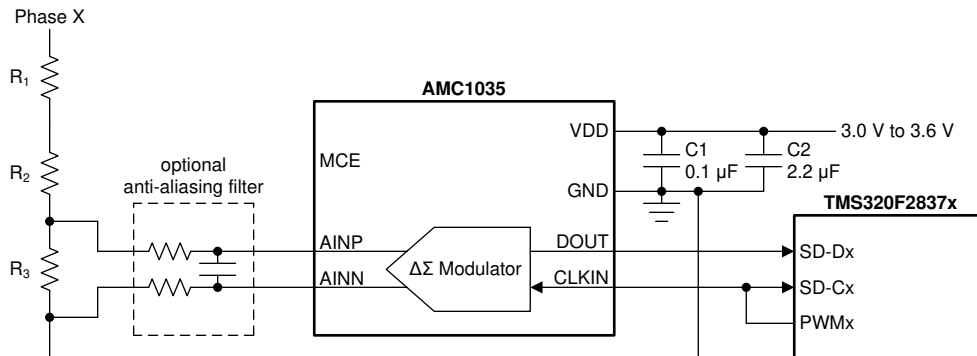


Figure 48. Decoupling the AMC1035

Safety considerations or high common-mode voltage levels may require the AMC1035 to be galvanically isolated from other parts of the system. [Figure 49](#) shows an example of a circuit that uses the [ISO7721](#) to isolate the signal path and the SN6501 and a transformer to generate the required isolated power.

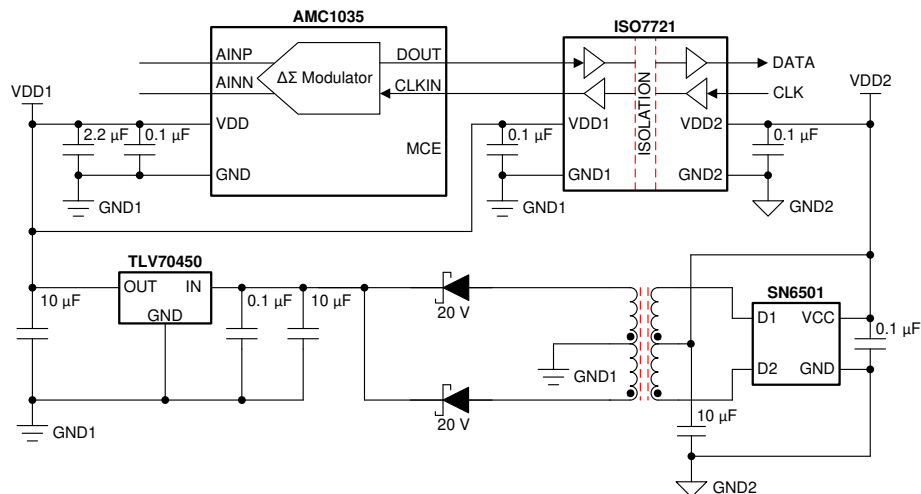


Figure 49. Galvanic Isolation of the AMC1035

[Figure 50](#) shows an alternative solution that uses the [ISOW7821](#) to isolate the signal path and provide the isolated power supply for the AMC1035.

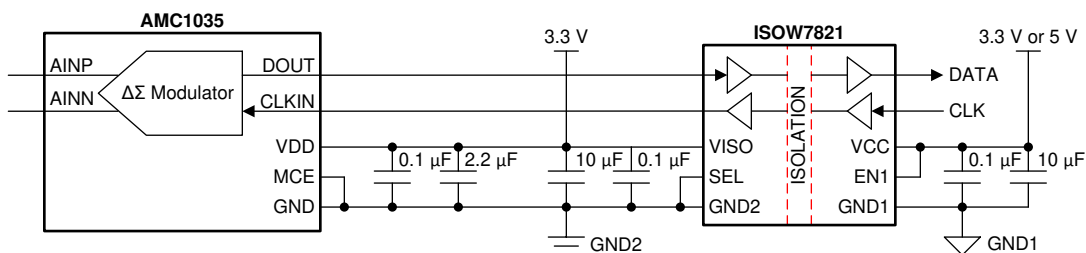


Figure 50. Galvanic Isolation of the AMC1035 for PCB Space-Constrained Applications

10 Layout

10.1 Layout Guidelines

Figure 51 shows two layout recommendations for designs based on 1206-SMD or 0603-SMD size decoupling capacitors placed as close as possible to the AMC1035. For best performance, place the AMC1035 as close as possible to the source of the analog signal to be converted and keep the layout of the AINP and AINN traces symmetrical.

10.2 Layout Example

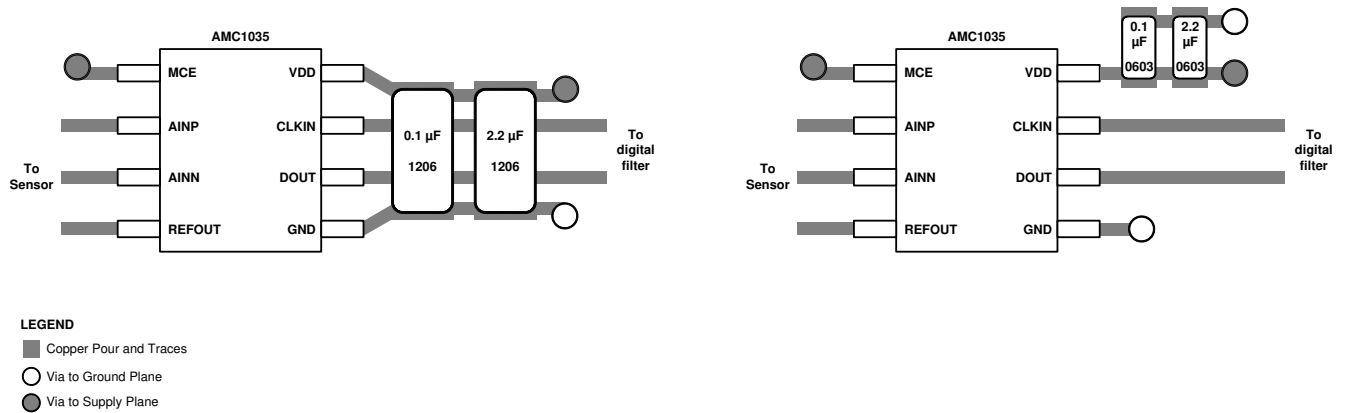


Figure 51. Recommended Layout of the AMC1035

11 デバイスおよびドキュメントのサポート

11.1 ドキュメントのサポート

11.1.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、『[TMS320F28004x Piccolo™ マイクロコントローラ](#)』データシート
- テキサス・インスツルメンツ、『[TMS320F2807x Piccolo™ マイクロコントローラ](#)』データシート
- テキサス・インスツルメンツ、『[TMS320F2837xD デュアル・コア Delfino™ マイクロコントローラ](#)』データシート
- テキサス・インスツルメンツ、『[ISO772x 高速、堅牢な EMC 強化型 2 チャンネル・デジタル・アイソレータ](#)』データシート
- テキサス・インスツルメンツ、『[MSP430F677x、MSP430F676x、MSP430F674x 多相メータリング SoC](#)』データシート
- テキサス・インスツルメンツ、『[AMC1210 2 次デルタ-シグマ変調器用のクワッド・デジタル・フィルタ](#)』データシート
- テキサス・インスツルメンツ、『[ADS1202 と FPGA デジタル・フィルタとの組み合わせによるモータ制御アプリケーションでの電流測定](#)』アプリケーション・レポート
- テキサス・インスツルメンツ、『[AMC1306x 高 CMTI、小型、高精度の強化絶縁デルタ-シグマ変調器](#)』データシート
- テキサス・インスツルメンツ、『[CDCLVC11xx 3.3V および 2.5V LVCMOS 高性能クロック・バッファ・ファミリ](#)』データシート
- テキサス・インスツルメンツ、『[LM117、LM317-N 広い温度範囲に対応した 3 ピン可変レギュレータ](#)』データシート
- テキサス・インスツルメンツ、『[SN6502 絶縁電源用の低ノイズ、350mA、410kHz の変圧器ドライバ](#)』データシート
- テキサス・インスツルメンツ、『[ISOW7821 高性能、5000V_{RMS} 強化デュアル・チャンネル・デジタル・アイソレータ、高効率低放射の DC/DC コンバータ内蔵](#)』データシート

11.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.com のデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.3 コミュニティ・リソース

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.6 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC1035D	ACTIVE	SOIC	D	8	75	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MC1035	Samples
AMC1035DR	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	MC1035	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1035DR	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1035DR	SOIC	D	8	2500	340.5	338.1	20.6

TUBE



*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
AMC1035D	D	SOIC	8	75	507	8	3940	4.32



PACKAGE OUTLINE

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.

7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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