TEXAS INSTRUMENTS

DRV8904-Q1, DRV8906-Q1, DRV8908-Q1
DRV8910-Q1, DRV8912-Q1

JAJSGV8B – SEPTEMBER 2019 – REVISED DECEMBER 2019

DRV89xx-Q1 高度な診断機能を備えた車載マルチ・チャネル・ハーフブリッジ・ドライバ

1 特長

- **車載アプリケーション用に AEC-Q100 認定済み**
- **4、6、8、10、12 のハーフブリッジ出力**
- **4.5V～32V の動作電圧**
  - 絶対最大定格電圧 40V
- **各出力について 1A の RMS 電流**
  - 並列出力の最大電流 6A
- **低消費電力スリープ・モード** (1.5µA)
- **3.3V と 5 V のロジック入力をサポート**
- **SPI による構成と診断**
  - 5MHz、16 ビットの SPI 通信
  - デイジー・チェーン機能
- **SPI を使用して PWM ジェネレータをプログラム可能**
  - 独立したハーフブリッジ PWM 動作
  - ハイサイド、ローサイド、H ブリッジ負荷駆動用に構成可能
  - 8 ビットのデューティ・サイクル分解能をサポート
- **SPI を使用してチャネルごとに詳細に診断できる内蔵保護機能**
  - nFAULT ピン出力
  - VM 低電圧誤動作防止 (UVLO)
  - VM 過電圧保護 (OVP)
  - ロジック電源パワーオン・リセット (POR)
  - 過電流保護 (OCP)
  - 拡張開放負荷検出 (OLD)
  - サーマル警告およびシャットダウン (OTW/OTSD)

2 アプリケーション

- HVAC フラップ DC モーター
- サイド・ミラーの調整と折り畳み
- LED アプリケーション
- 各種ブラシ付き DC モーターおよびソレノイド

3 概要

DRV89xx-Q1 は、4～12 のハーフブリッジを備えた統合マルチチャネル・ハーフブリッジ・ドライバのピン互換ファミリです。このデバイス・ファミリはオン抵抗 ($R_{DS(ON)}$) が小さいため、大電流動作時の熱性能が優れています。

これらのデバイスは、ブラシ付き DC (BDC) モーターまたはステッピング・モーターを独立、連続、並列モードで駆動できます。ハーフブリッジは完全に制御可能であり、順方向、逆方向、惰性、ブレーキのモーター動作を実現できます。

これらのデバイスは、デイジー・チェーン接続可能な標準の 16 ビット、5MHz のシリアル・ペリフェラル・インターフェイス (SPI) を備えており、完全な構成と詳細な診断が可能です。デバイスによって 4 つまたは 8 つのプログラム可能な PWM ジェネレータを内蔵しているため、モーター動作または LED 調光制御中に電流を制限できます。

フォルト発生時にシステムに警告する nFAULT ピンをはじめ、多くの保護および診断機能を内蔵しています。公称負荷電流が小さい時に開放負荷条件を検出するための低電流の開放負荷検出 (OLD) モードと、オフライン OLD のためのパッシブ OLD モードを備えています。また、短絡、低電圧、過熱状態に対して完全に保護されています。

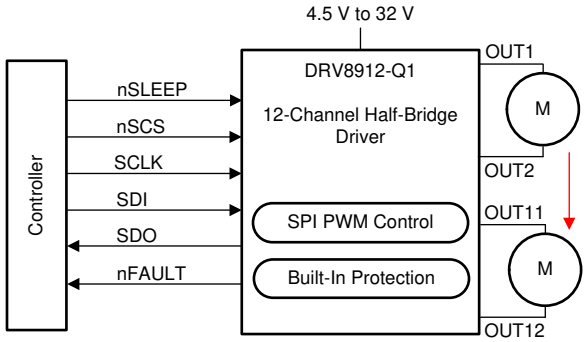
弊社のポートフォリオ全体については、ti.com のブラシ付きモーター・ドライバをご覧ください。

製品情報(1)

型番	パッケージ	本体サイズ (公称)
DRV8912-Q1	HTSSOP (24)	7.80mm×4.40mm
DRV8910-Q1		
DRV8908-Q1		
DRV8906-Q1		
DRV8904-Q1		

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

(2) **概略回路図**



英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Revision A (December 2019) から Revision B に変更 **Page**

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2019年9月発行のものから更新 **Page**

- デバイスのステータスを「量産データ」に 変更 ... 1

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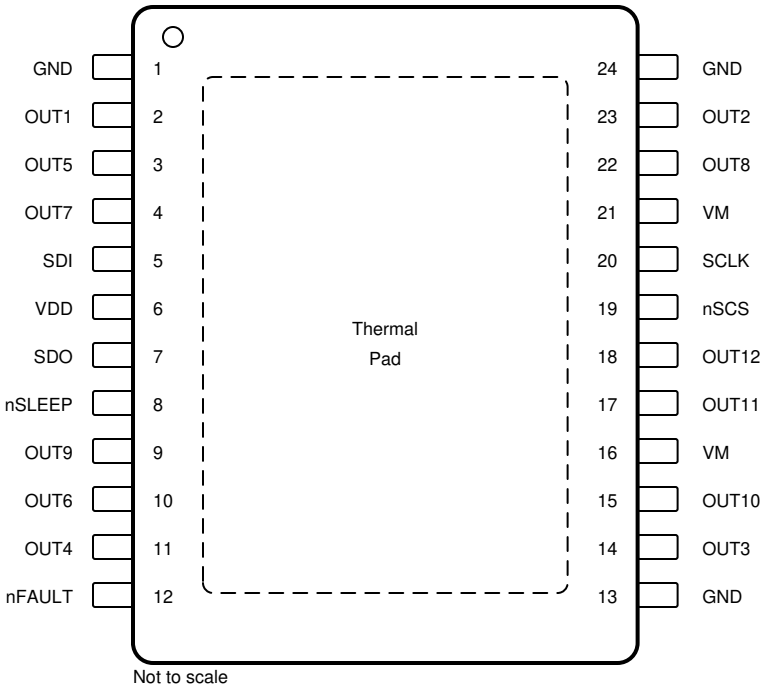
5 Device Comparison Table

DEVICE	NUMBER OF HALF-BRIDGES	NUMBER OF PWM GENERATORS	OPEN-LOAD DETECTION SCHEMES	LINK TO REGISTER MAP
DRV8912-Q1	12	4	Active OLD, Low-Current Active OLD, Negative-Current Active OLD	表 17
DRV8910-Q1	10	4		表 18
DRV8908-Q1	8	8	Passive OLD, Active OLD, Low-Current Active OLD, Negative-Current Active OLD	表 50
DRV8906-Q1	6	8		表 51
DRV8904-Q1	4	8		表 52

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6 Pin Configuration and Functions

DRV8912-Q1 PWP Package
24-Pin HTSSOP Package With Exposed Thermal Pad
Top View



Not to scale

Pin Functions—DRV8912-Q1

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	13	PWR	Device power ground. Connect the GND pin to the system ground.
GND	24	PWR	Device power ground. Connect the GND pin to the system ground.
GND	1	PWR	Device power ground. Connect the GND pin to the system ground.
nFAULT	12	OD	Fault indicator output. This pin is pulled logic low during a fault condition and requires an external pull-up resistor.
nSCS	19	I	Serial chip select. A logic low on this pin enables serial interface communication. Internal pull-up.
nSLEEP	8	I	Driver enable pin. When this pin is logic low the device goes to a low-power sleep mode. Internal pull-down.
OUT1	2	O	Half-bridge 1 output
OUT2	23	O	Half-bridge 2 output
OUT3	14	O	Half-bridge 3 output
OUT4	11	O	Half-bridge 4 output
OUT5	3	O	Half-bridge 5 output
OUT6	10	O	Half-bridge 6 output
OUT7	4	O	Half-bridge 7 output
OUT8	22	O	Half-bridge 8 output
OUT9	9	O	Half-bridge 9 output
OUT10	15	O	Half-bridge 10 output
OUT11	17	O	Half-bridge 11 output
OUT12	18	O	Half-bridge 12 output

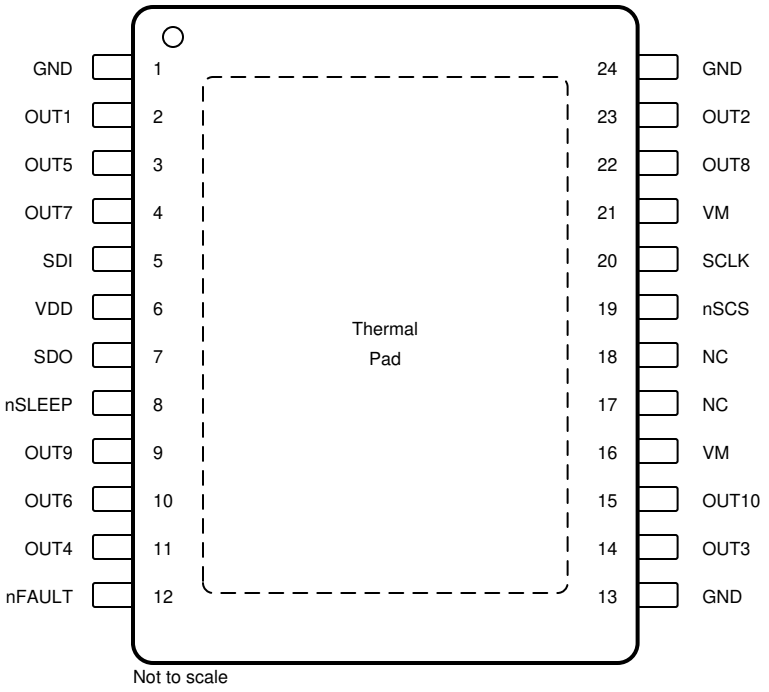
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Pin Functions—DRV8912-Q1 (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
SCLK	20	I	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin. Internal pull-down.
SDI	5	I	Serial data input. Data is captured on the falling edge of the SCLK pin. Internal pull-down.
SDO	7	PP	Serial data output. Data is shifted out on the rising edge of the SCLK pin.
VDD	6	PWR	Logic power supply input. Connect a X5R or X7R, 0.1-μF, VDD-rated ceramic capacitor and greater than or equal to 1-μF bulk capacitance between the VDD and GND pins.
VM	16	PWR	Main power supply input. Connect all VM pins together to the motor supply voltage. Connect a X5R or X7R, 0.1-μF, VM-rated ceramic capacitor and greater than or equal to 10-μF bulk capacitance between the VM and GND pins.
VM	21	PWR	Main power supply input. Connect all VM pins together to the motor supply voltage. Connect a X5R or X7R, 0.1-μF, VM-rated ceramic capacitor and greater than or equal to 10-μF bulk capacitance between the VM and GND pins.

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DRV8910-Q1 PWP Package
24-Pin HTSSOP Package With Exposed Thermal Pad
Top View



Not to scale

Pin Functions—DRV8910-Q1

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	13	PWR	Device power ground. Connect the GND pin to the system ground.
GND	24	PWR	Device power ground. Connect the GND pin to the system ground.
GND	1	PWR	Device power ground. Connect the GND pin to the system ground.
NC	17	—	Not connected
NC	18	—	Not connected
nFAULT	12	OD	Fault indicator output. This pin is pulled logic low during a fault condition and requires an external pull-up resistor.
nSCS	19	I	Serial chip select. A logic low on this pin enables serial interface communication. Internal pull-up.
nSLEEP	8	I	Driver enable pin. When this pin is logic low the device goes to a low-power sleep mode. Internal pull-down.
OUT1	2	O	Half-bridge 1 output
OUT2	23	O	Half-bridge 2 output
OUT3	14	O	Half-bridge 3 output
OUT4	11	O	Half-bridge 4 output
OUT5	3	O	Half-bridge 5 output
OUT6	10	O	Half-bridge 6 output
OUT7	4	O	Half-bridge 7 output
OUT8	22	O	Half-bridge 8 output
OUT9	9	O	Half-bridge 9 output
OUT10	15	O	Half-bridge 10 output
SCLK	20	I	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin. Internal pull-down.
SDI	5	I	Serial data input. Data is captured on the falling edge of the SCLK pin. Internal pull-down.

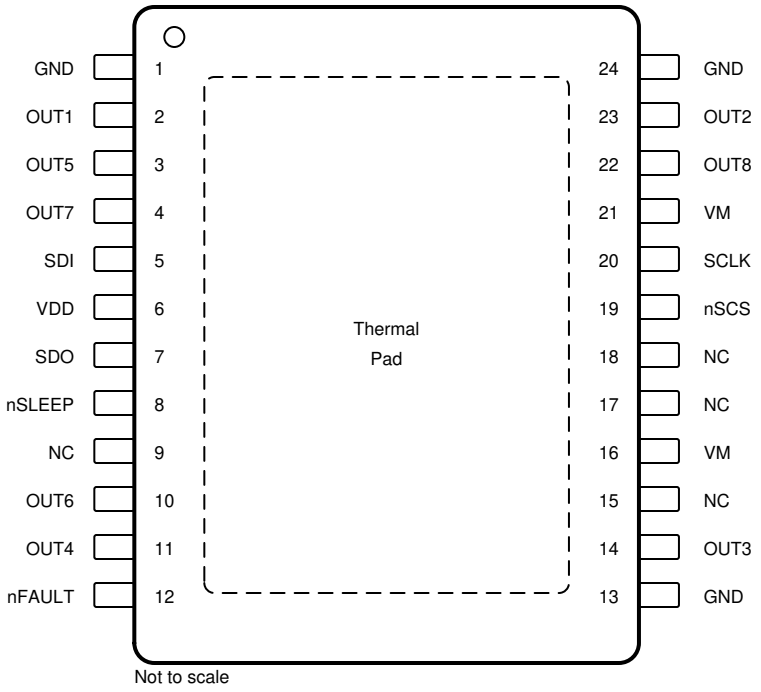
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Pin Functions—DRV8910-Q1 (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
SDO	7	PP	Serial data output. Data is shifted out on the rising edge of the SCLK pin.
VDD	6	PWR	Logic power supply input. Connect a X5R or X7R, 0.1-μF, VDD-rated ceramic capacitor and greater than or equal to 1-μF bulk capacitance between the VDD and GND pins.
VM	16	PWR	Main power supply input. Connect all VM pins together to the motor supply voltage. Connect a X5R or X7R, 0.1-μF, VM-rated ceramic capacitor and greater than or equal to 10-μF bulk capacitance between the VM and GND pins.
VM	21	PWR	Main power supply input. Connect all VM pins together to the motor supply voltage. Connect a X5R or X7R, 0.1-μF, VM-rated ceramic capacitor and greater than or equal to 10-μF bulk capacitance between the VM and GND pins.

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DRV8908-Q1 PWP Package
24-Pin HTSSOP Package With Exposed Thermal Pad
Top View



Not to scale

Pin Functions—DRV8908-Q1

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	13	PWR	Device power ground. Connect the GND pin to the system ground.
GND	24	PWR	Device power ground. Connect the GND pin to the system ground.
GND	1	PWR	Device power ground. Connect the GND pin to the system ground.
NC	9	—	Not connected
NC	15	—	Not connected
NC	17	—	Not connected
NC	18	—	Not connected
nFAULT	12	OD	Fault indicator output. This pin is pulled logic low during a fault condition and requires an external pull-up resistor.
nSCS	19	I	Serial chip select. A logic low on this pin enables serial interface communication. Internal pull-up.
nSLEEP	8	I	Driver enable pin. When this pin is logic low the device goes to a low-power sleep mode. Internal pull-down.
OUT1	2	O	Half-bridge 1 output
OUT2	23	O	Half-bridge 2 output
OUT3	14	O	Half-bridge 3 output
OUT4	11	O	Half-bridge 4 output
OUT5	3	O	Half-bridge 5 output
OUT6	10	O	Half-bridge 6 output
OUT7	4	O	Half-bridge 7 output
OUT8	22	O	Half-bridge 8 output
SCLK	20	I	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin. Internal pull-down.
SDI	5	I	Serial data input. Data is captured on the falling edge of the SCLK pin. Internal pull-down.

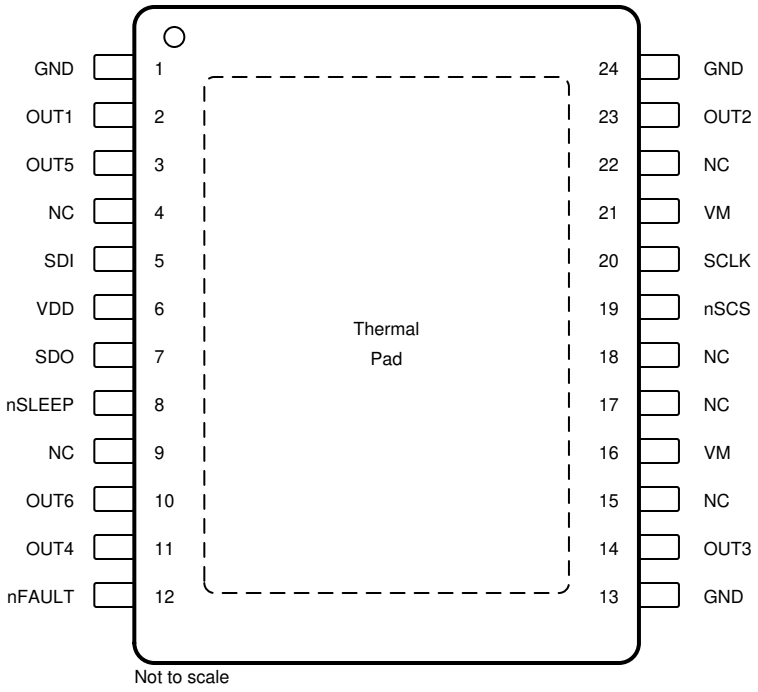
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Pin Functions—DRV8908-Q1 (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
SDO	7	PP	Serial data output. Data is shifted out on the rising edge of the SCLK pin.
VDD	6	PWR	Logic power supply input. Connect a X5R or X7R, 0.1-μF, VDD-rated ceramic capacitor and greater than or equal to 1-μF bulk capacitance between the VDD and GND pins.
VM	16	PWR	Main power supply input. Connect all VM pins together to the motor supply voltage. Connect a X5R or X7R, 0.1-μF, VM-rated ceramic capacitor and greater than or equal to 10-μF bulk capacitance between the VM and GND pins.
VM	21	PWR	Main power supply input. Connect all VM pins together to the motor supply voltage. Connect a X5R or X7R, 0.1-μF, VM-rated ceramic capacitor and greater than or equal to 10-μF bulk capacitance between the VM and GND pins.

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DRV8906-Q1 PWP Package
24-Pin HTSSOP Package With Exposed Thermal Pad
Top View



Not to scale

Pin Functions—DRV8906-Q1

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	13	PWR	Device power ground. Connect the GND pin to the system ground.
GND	24	PWR	Device power ground. Connect the GND pin to the system ground.
GND	1	PWR	Device power ground. Connect the GND pin to the system ground.
NC	4	—	Not connected
NC	9	—	Not connected
NC	15	—	Not connected
NC	17	—	Not connected
NC	18	—	Not connected
NC	22	—	Not connected
nFAULT	12	OD	Fault indicator output. This pin is pulled logic low during a fault condition and requires an external pull-up resistor.
nSCS	19	I	Serial chip select. A logic low on this pin enables serial interface communication. Internal pull-up.
nSLEEP	8	I	Driver enable pin. When this pin is logic low the device goes to a low-power sleep mode. Internal pull-down.
OUT1	2	O	Half-bridge 1 output
OUT2	23	O	Half-bridge 2 output
OUT3	14	O	Half-bridge 3 output
OUT4	11	O	Half-bridge 4 output
OUT5	3	O	Half-bridge 5 output
OUT6	10	O	Half-bridge 6 output
SCLK	20	I	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin. Internal pull-down.
SDI	5	I	Serial data input. Data is captured on the falling edge of the SCLK pin. Internal pull-down.

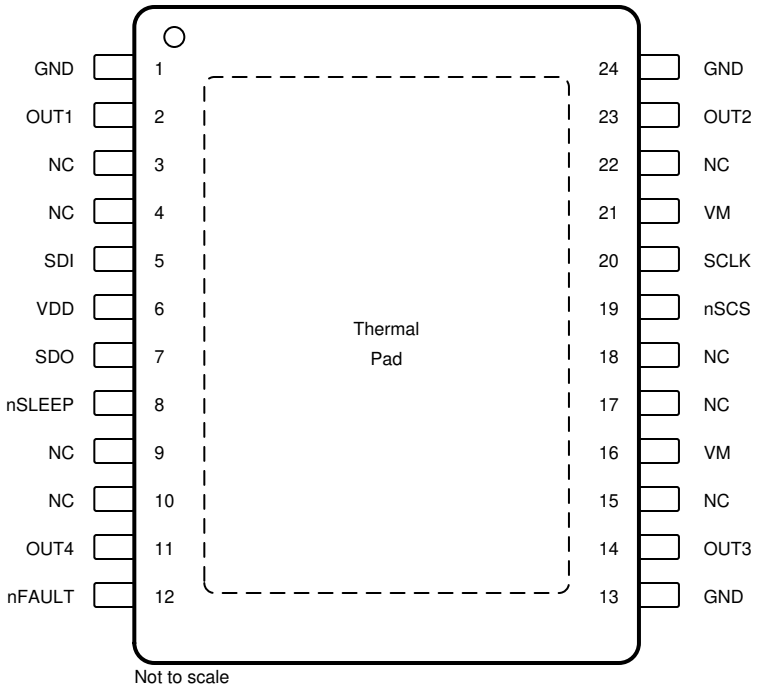
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Pin Functions—DRV8906-Q1 (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
SDO	7	PP	Serial data output. Data is shifted out on the rising edge of the SCLK pin.
VDD	6	PWR	Logic power supply input. Connect a X5R or X7R, 0.1-μF, VDD-rated ceramic capacitor and greater than or equal to 1-μF bulk capacitance between the VDD and GND pins.
VM	16	PWR	Main power supply input. Connect all VM pins together to the motor supply voltage. Connect a X5R or X7R, 0.1-μF, VM-rated ceramic capacitor and greater than or equal to 10-μF bulk capacitance between the VM and GND pins.
VM	21	PWR	Main power supply input. Connect all VM pins together to the motor supply voltage. Connect a X5R or X7R, 0.1-μF, VM-rated ceramic capacitor and greater than or equal to 10-μF bulk capacitance between the VM and GND pins.

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DRV8904-Q1 PWP Package
24-Pin HTSSOP Package With Exposed Thermal Pad
Top View



Pin Functions—DRV8904-Q1

PIN		TYPE	DESCRIPTION
NAME	NO.		
GND	13	PWR	Device power ground. Connect the GND pin to the system ground.
GND	24	PWR	Device power ground. Connect the GND pin to the system ground.
GND	1	PWR	Device power ground. Connect the GND pin to the system ground.
NC	3	—	Not connected
NC	4	—	Not connected
NC	9	—	Not connected
NC	10	—	Not connected
NC	15	—	Not connected
NC	17	—	Not connected
NC	18	—	Not connected
NC	22	—	Not connected
nFAULT	12	OD	Fault indicator output. This pin is pulled logic low during a fault condition and requires an external pull-up resistor.
nSCS	19	I	Serial chip select. A logic low on this pin enables serial interface communication. Internal pull-up.
nSLEEP	8	I	Driver enable pin. When this pin is logic low the device goes to a low-power sleep mode. Internal pull-down.
OUT1	2	O	Half-bridge 1 output
OUT2	23	O	Half-bridge 2 output
OUT3	14	O	Half-bridge 3 output
OUT4	11	O	Half-bridge 4 output
SCLK	20	I	Serial clock input. Serial data is shifted out and captured on the corresponding rising and falling edge on this pin. Internal pull-down.
SDI	5	I	Serial data input. Data is captured on the falling edge of the SCLK pin. Internal pull-down.

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Pin Functions—DRV8904-Q1 (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
SDO	7	PP	Serial data output. Data is shifted out on the rising edge of the SCLK pin.
VDD	6	PWR	Logic power supply input. Connect a X5R or X7R, 0.1-μF, VDD-rated ceramic capacitor and greater than or equal to 1-μF bulk capacitance between the VDD and GND pins.
VM	16	PWR	Main power supply input. Connect all VM pins together to the motor supply voltage. Connect a X5R or X7R, 0.1-μF, VM-rated ceramic capacitor and greater than or equal to 10-μF bulk capacitance between the VM and GND pins.
VM	21	PWR	Main power supply input. Connect all VM pins together to the motor supply voltage. Connect a X5R or X7R, 0.1-μF, VM-rated ceramic capacitor and greater than or equal to 10-μF bulk capacitance between the VM and GND pins.

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7 Specifications

7.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Power supply pin voltage (VM)	4.5	40	V
Logic supply pin voltage (VDD)	–0.3	5.75	V
Output pin voltage (OUTx)	–0.7	VM + 0.7	V
Logic pin input voltage (nSCS, nSLEEP, SCLK, SDI)	–0.3	VDD + 0.3	V
Logic pin output voltage (nFAULT, SDO)	–0.3	VDD + 0.3	V
Continuous supply current (VM pins combined)	0	6	A
Peak output current drive (OUTx)	Internally Limited	Internally Limited	A
Continous sink current (GND pins combined)	0	6	A
Junction temperature, T_J	–40	150	°C
Storage temperature, T_{stg}	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

7.2 ESD Ratings

				VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per AEC Q100-002(1)	OUTx and VM pins	±4000	V
			Other pins	±2000	
		Charged device model (CDM), per AEC Q100-011	Corner pins (1, 12, 13, and 24)	±750	
			Other pins	±500	

(1) AEC Q100-002 indicates that HBM stressing shall be in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

7.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
V_{VM}	Power supply voltage (VM)	4.5		32	V
V_{DD}	Logic supply voltage (VDD)	3		5.5	V
V_{IN}	Logic input voltage (nSCS, nSLEEP, SCLK, SDI)	0		5.5	V
V_{OD}	Open drain pullup voltage (nFAULT)	0		5.5	V
I_{OD}	Open drain output current (nFAULT)	0		5	mA
V_{OP}	Push-pull pullup voltage (SDO)	0		5.5	V
I_{OP}	Push-pull output current (SDO)	0		5	mA
T_A	Operating ambient temperature	–40		125	°C
T_J	Operating junction temperature	–40		150	°C

7.4 Thermal Information

THERMAL METRIC(1)		DRV8912-Q1 DRV8910-Q1	DRV8908-Q1 DRV8906-Q1 DRV8904-Q1	UNIT
		PWP (HTSSOP)	PWP (HTSSOP)	
		24 PINS	24 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	30.2	31.2	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	23.7	25.4	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	10.1	11.2	°C/W

(1) For more information about traditional and new thermal metrics, see Semiconductor and IC Package Thermal Metrics application report.

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Thermal Information (continued)

THERMAL METRIC(1)		DRV8912-Q1 DRV8910-Q1	DRV8908-Q1 DRV8906-Q1 DRV8904-Q1	UNIT
		PWP (HTSSOP)	PWP (HTSSOP)	
		24 PINS	24 PINS	
Ψ_{JT}	Junction-to-top characterization parameter	0.3	0.4	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	10.0	11.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	2.5	3.1	°C/W

7.5 Electrical Characteristics

at T_J = –40°C to +150°C, V_{VM} = 4.5 to 32 V (Main Supply), V_{VDD} = 3 to 5.5 V (Logic Supply) (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 13.5 V, V_{VDD} = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
POWER SUPPLIES (VDD, VM)						
I_{VMQ}	VM sleep mode current	V_{VM} = 13.5 V, nSLEEP = 0, T_A = 25 °C		0.35	1	µA
		V_{VM} = 13.5 V, nSLEEP = 0, T_A = 125 °C			2	µA
I_{VDDQ}	VDD sleep mode current	V_{VM} = 13.5 V, V_{VDD} = 3.3 V, nSLEEP = 0, T_A = 25 °C		0.01	0.3	µA
		V_{VM} = 13.5 V, V_{VDD} = 3.3 V, nSLEEP = 0, T_A = 125 °C			2	µA
I_{VMS}	VM standby mode current	V_{VM} = 13.5 V, nSLEEP = 1, Driver = 'OFF', T_A = 25 °C		0.2	0.5	mA
		V_{VM} = 13.5 V, nSLEEP = 1, Driver = 'OFF', T_A = 125 °C			0.5	mA
I_{VDDS}	VDD standby mode current	V_{VM} = 13.5 V, V_{VDD} = 3.3 V, nSLEEP = 1, SPI = 'OFF', T_A = 25 °C		0.6	1	mA
		V_{VM} = 13.5 V, V_{VDD} = 3.3 V, nSLEEP = 1, SPI = 'OFF', T_A = 125 °C			1	mA
I_{VM}	VM operating mode current	V_{VM} = 13.5 V, nSLEEP = 1, All High-Side FETs = 'ON', T_A = 25 °C		2.6	5	mA
		V_{VM} = 13.5 V, nSLEEP = 1, All High-Side FETs = 'ON', T_A = 125 °C			5	mA
I_{VDD}	VDD operating mode current	V_{VM} = 13.5 V, V_{VDD} = 3.3 V, nSLEEP = 1, All High-Side FETs = 'ON', SPI = 'ON' (5 MHz), T_A = 25 °C		2.8	5	mA
		V_{VM} = 13.5 V, V_{VDD} = 3.3 V, nSLEEP = 1, All High-Side FETs = 'ON', SPI = 'ON' (5 MHz), T_A = 125 °C			5	mA
t_{WAKE}	Wake-up time	nSLEEP high to SPI ready			200	µs
t_{SLEEP}	Turnoff time	nSLEEP low to device sleep			20	µs
LOGIC-LEVEL INPUTS (nSLEEP, SCLK, SDI)						
V_{IL}	Input logic low voltage		0		0.3*VDD	V
V_{IH}	Input logic high voltage		0.7*VDD		VDD	V
V_{HYS}	Input logic hysteresis		200			mV
I_{IL}	Input logic low current	V_{IN} = 0 V	–1		1	µA
I_{IH}	Input logic high current	V_{IN} = V_{VDD}		34	75	µA
C_{ID}	Input capacitance				15	pF
LOGIC-LEVEL INPUTS (nSCS)						
V_{IL}	Input logic low voltage		0		0.3*VDD	V
V_{IH}	Input logic high voltage		0.7*VDD		VDD	V
V_{HYS}	Input logic hysteresis		200			mV
I_{IL}	Input logic low current	V_{IN} = 0 V		34	75	µA

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Electrical Characteristics (continued)

at T_J = –40°C to +150°C, V_{VM} = 4.5 to 32 V (Main Supply), V_{VDD} = 3 to 5.5 V (Logic Supply) (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 13.5 V, V_{VDD} = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{IH}	Input logic high current	V_{IN} = V_{VDD}	–1		1	µA
C_{ID}	Input capacitance				15	pF
OPEN-DRAIN OUTPUTS (nFAULT)						
V_{OL}	Output logic low voltage	I_{OD} = 5 mA	0		0.4	V
I_{OH}	Output logic high current	V_{OD} = 5 V	–1		1	µA
C_{OD}	Output capacitance				15	pF
PUSH-PULL OUTPUTS (SDO)						
V_{OL}	Output logic low voltage	I_{OP} = 5 mA	0		0.4	V
V_{OH}	Output logic high voltage	I_{OP} = 5 mA	VDD–0.6		VDD	V
I_{OL}	Output logic low current	V_{OP} = 0 V	–1		1	µA
I_{OH}	Output logic high current	V_{OP} = V_{VDD}	–1		1	µA
C_{OD}	Output capacitance				30	pF
DRIVER OUTPUTS (OUTx)						
$R_{DS(ON)}$	High-side MOSFET on resistance	V_{VM} = 13.5 V, I_{OUT} = 0.5 A, T_A = 25°C		0.75	1.1	Ω
		V_{VM} = 13.5 V, I_{OUT} = 0.5 A, T_A = 125°C			1.5	Ω
	Low-side MOSFET on resistance	V_{VM} = 13.5 V, I_{OUT} = 0.5 A, T_A = 25°C		0.75	1.1	Ω
		V_{VM} = 13.5 V, I_{OUT} = 0.5 A, T_A = 125°C			1.5	Ω
SR	Output rise and fall time (high-side and low-side)	V_{VM} = 13.5 V, 10-90%, R_{LOAD} = 27 Ω, HBx_SR = 0b		0.6		V/µs
		V_{VM} = 13.5 V, 10-90%, R_{LOAD} = 27 Ω, HBx_SR = 1b		2.5		V/µs
t_{DEAD}	Output dead time (high to low / low to high)	V_{VM} = 13.5 V, SR = 0, HS/LS driver OFF to LS/HS driver ON	8	20	32	µs
		V_{VM} = 13.5 V, SR = 1, HS/LS driver OFF to LS/HS driver ON	2	5	15	µs
t_{PD}	Propagation delay (high-side / low-side ON/OFF)	High-side ON (SPI last transition) to OUTx transition, SR = 0	5	12	25	µs
		High-side ON (SPI last transition) to OUTx transition, SR = 1	3	5	10	µs
I_{LEAK}	Leakage current low-side	V_{OUTx} = 13.5 V, nSLEEP = 1, SR = 0b		6	10	µA
		V_{OUTx} = 13.5 V, nSLEEP = 1, SR = 1b		20	35	µA
		V_{OUTx} = 13.5 V, nSLEEP = 0		4	15	µA
	Leakage current high-side	V_{OUTx} = 0 V, nSLEEP = 1			2	µA
		V_{OUTx} = 0 V, nSLEEP = 0			2	µA
PWM MODE						
f_{PWM}	PWM switching frequency	PWM_CHx_FREQ = 00b		80		Hz
		PWM_CHx_FREQ = 01b		100		Hz
		PWM_CHx_FREQ = 10b		200		Hz
		PWM_CHx_FREQ = 11b		2000		Hz
PROTECTION CIRCUITS						
V_{UVLO}	Supply undervoltage lockout (UVLO)	Supply rising	4.0		4.5	V
		Supply falling	3.8		4.3	V
V_{UVLO_HYS}	Supply undervoltage lockout hysteresis	Rising to falling theshold		200		mV
t_{UVLO}	Supply undervoltage deglitch time			10		µs

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Electrical Characteristics (continued)

at T_J = –40°C to +150°C, V_{VM} = 4.5 to 32 V (Main Supply), V_{VDD} = 3 to 5.5 V (Logic Supply) (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 13.5 V, V_{VDD} = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{OVP}	Supply overvoltage protection (OVP)	Supply rising, EXT_OVP = 0b	21		25	V
		Supply falling, EXT_OVP = 0b	20		24	V
		Supply rising, EXT_OVP = 1b	32.7		35	V
		Supply falling, EXT_OVP = 1b	32		34.3	V
V_{OVP_HYS}	Supply overvoltage protection hysteresis	Rising to falling theshold, EXT_OVP = 0b		1		V
		Rising to falling theshold, EXT_OVP = 1b		0.7		V
t_{OVP}	Supply overvoltage deglitch time			10		µs
V_{POR}	Logic undervoltage (POR)	Supply rising	2.45		3	V
		Supply falling	2.4		2.95	V
V_{POR_HYS}	Logic undervoltage hysteresis	Rising to falling theshold		75		mV
I_{OCP}	Overcurrent protection trip point(1)(2)		1.3	1.8	2.3	A
t_{OCP}	Overcurrent protection deglitch time	OCP_DEG = 000b		10		µs
		OCP_DEG = 001b		5		µs
		OCP_DEG = 010b		2.5		µs
		OCP_DEG = 011b		1		µs
		OCP_DEG = 100b		60		µs
		OCP_DEG = 101b		40		µs
		OCP_DEG = 110b		30		µs
		OCP_DEG = 111b		20		µs
I_{OLD}	Open load detection current	Current flowing from VM to OUTx (High-Side = ON) or OUTx to GND (Low-Side = ON)	2	9	18	mA
I_{OLD_NEG}	Negative open load detection current	Current flowing from OUTx to VM (High-Side = ON) or GND to OUTx (Low-Side = ON)	2	15	30	mA
I_{OLD_LOW}	Open load detection current in low current OLD mode	Current flowing from VM to OUTx (High-Side = ON) or OUTx to GND (Low-Side = ON)	0.2	0.8	2	mA
I_{OL_GND}	Passive OLD current	DRV8908/6/4, FETs in Hi-Z state, current from OUTx to GND during OLD trip		100		µA
V_{OL_GND}	Passive OLD voltage threshold	DRV8908/6/4, FETs in Hi-Z state, voltage at OUTx during OLD trip for GND-connected load		3.1		V
I_{OL_VM}	Passive OLD current	DRV8908/6/4, FETs in Hi-Z state, current from VM to OUTx for OLD trip, HBX_VM_POLD = 0b		100		µA
V_{OL_VM}	Passive OLD voltage threshold	DRV8908/6/4, FETs in Hi-Z state, voltage at OUTx during OLD trip for VM-connected load, HBX_VM_POLD = 0b		1.1		V
I_{OL_VM}	Passive OLD current	DRV8908/6/4, FETs in Hi-Z state, current from VM to OUTx for OLD trip, HBX_VM_POLD = 1b		480		µA
V_{OL_VM}	Passive OLD voltage threshold	DRV8908/6/4, FETs in Hi-Z state, voltage at OUTx during OLD trip for VM connceted load, HBX_VM_POLD = 1b		1.6		V

(1) For 20-V < V_{VM} < 28-V, the OCP deglicth time must be limited to 10-µs (Default Deglitch Value, OCP_DEG = 000b).
(2) For V_{VM} > 28 V, the OCP deglicth time must be limited to 1-µs (Lowest Deglitch Value, OCP_DEG = 011b).

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Electrical Characteristics (continued)

at T_J = –40°C to +150°C, V_{VM} = 4.5 to 32 V (Main Supply), V_{VDD} = 3 to 5.5 V (Logic Supply) (unless otherwise noted). Typical limits apply for T_A = 25°C, V_{VM} = 13.5 V, V_{VDD} = 3.3 V

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
R_{OL}	Passive OLD detect resistance threshold	DRV8908/6/4, FETs in Hi-Z state, Full bridge connection	5		100	kΩ
R_{OL}	Passive OLD detect resistance threshold	DRV8908/6/4, FETs in Hi-Z State, Load connected to GND	5		100	kΩ
R_{OL}	Passive OLD detect resistance threshold	DRV8908/6/4, FETs in Hi-Z State, Load connected to VM, HBX_VM_POLD = 0b	5		400	kΩ
R_{OL}	Passive OLD detect resistance threshold	DRV8908/6/4, FETs in Hi-Z State, Load connected to VM, HBX_VM_POLD = 1b	5		100	kΩ
t_{OLD}	Open load deglitch time	Active OLD (Continuous Mode)	2	3	4	ms
t_{OLD}	Open load deglitch time	Active OLD (PWM Mode)	150	200	300	µs
T_{OTW}	Thermal warning temperature	Die temperature (T_j)	120	140	170	°C
T_{OTW_HYS}	Thermal warning hysteresis	Die temperature (T_j)		20		°C
T_{OTSD}	Thermal shutdown temperature	Die temperature (T_j)	150	175	200	°C
T_{OTSD_HYS}	Thermal shutdown hysteresis	Die temperature (T_j)		20		°C

7.6 Timing Requirements

PARAMETER		TEST CONDITIONS	MIN	NOM	MAX	UNIT
SPI (nSCS, SCLK, SDI, SDO)						
t_{READY}	SPI ready after after enable	VM > UVLO, ENABLE = 3.3 V			1	ms
t_{CLK}	SCLK minimum period		200			ns
t_{CLKH}	SCLK minimum high time		100			ns
t_{CLKL}	SCLK minimum low time		100			ns
t_{SU_SDI}	SDI input data setup time		40			ns
t_{HD_SDI}	SDI input data hold time		60			ns
t_{DLY_SDO}	SDO output data delay time	SCLK high to SDO valid			60	ns
t_{SU_nSCS}	nSCS input setup time		100			ns
t_{HD_nSCS}	nSCS input hold time		100			ns
t_{HI_nSCS}	nSCS minimum high time before active low		600			ns
t_{DIS_nSCS}	nSCS disable delay time	nSCS high to SDO high impedance		30		ns
t_{SC_SPI}	Successive SPI write gaps			2.5		µs

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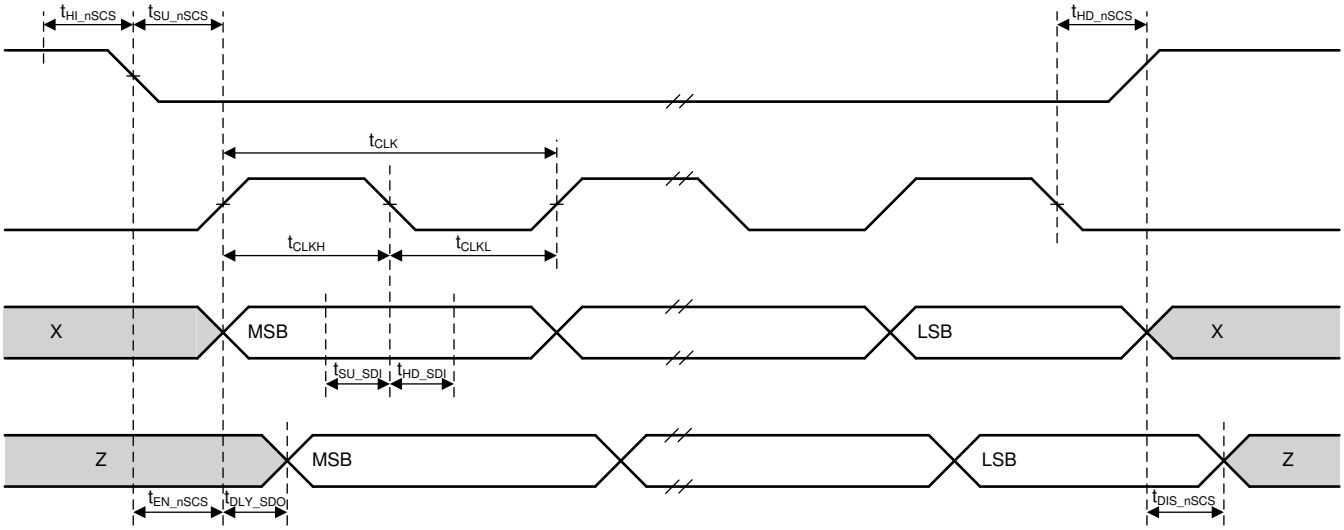


図 1. SPI Timing

7.7 Typical Characteristics

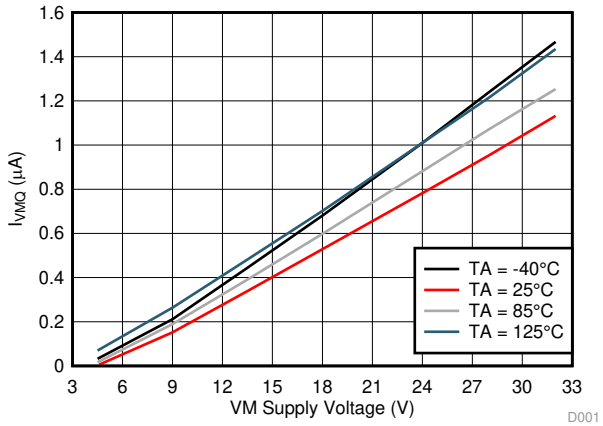


図 2. VM Sleep Mode Current (I_{VMQ}) vs Supply Voltage (V_{VM})

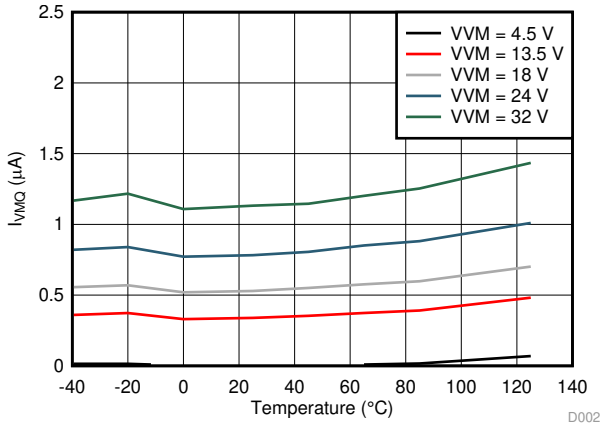


図 3. VM Sleep Mode Current (I_{VMQ}) vs Ambient Temperature (T_A)

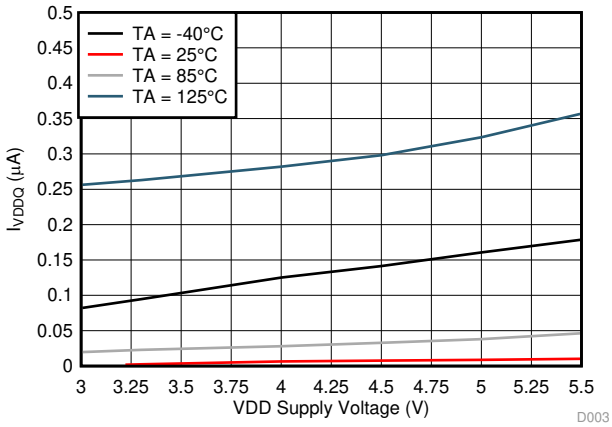


図 4. VDD Sleep Mode Current (I_{VDDQ}) vs Supply Voltage (V_{VDD})

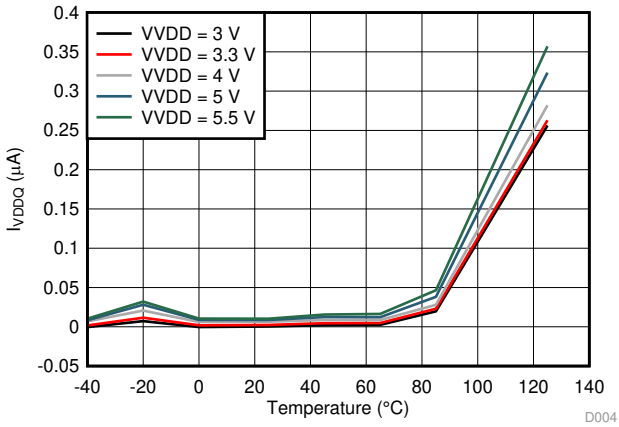


図 5. VDD Sleep Mode Current (I_{VDDQ}) vs Ambient Temperature (T_A)

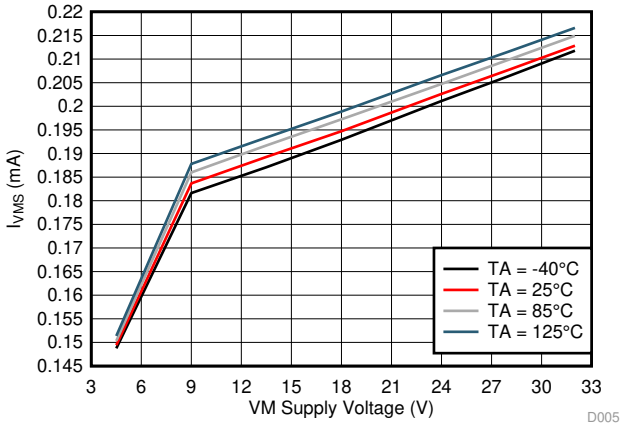


図 6. VM Standby Mode Current (I_{VMS}) vs Supply Voltage (V_{VM})

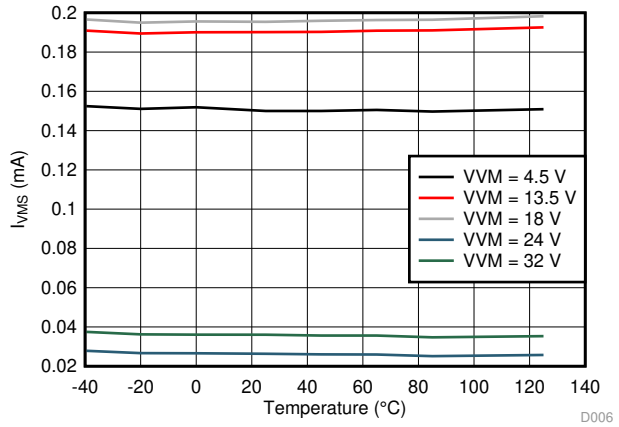


図 7. VM Standby Mode Current (I_{VMS}) vs Ambient Temperature (T_A)

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Typical Characteristics (continued)

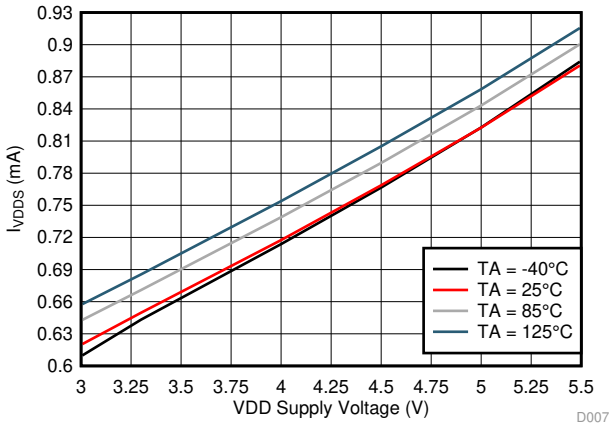


図 8. VDD Standby Mode Current (I_{VDDS}) vs Supply Voltage (V_{VDD})

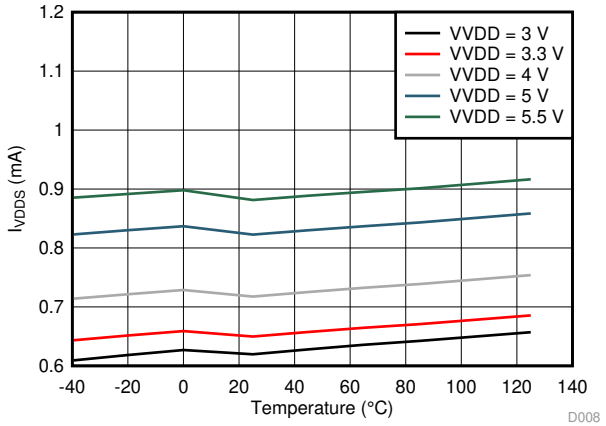


図 9. VDD Standby Mode Current (I_{VDDS}) vs Ambient Temperature (T_A)

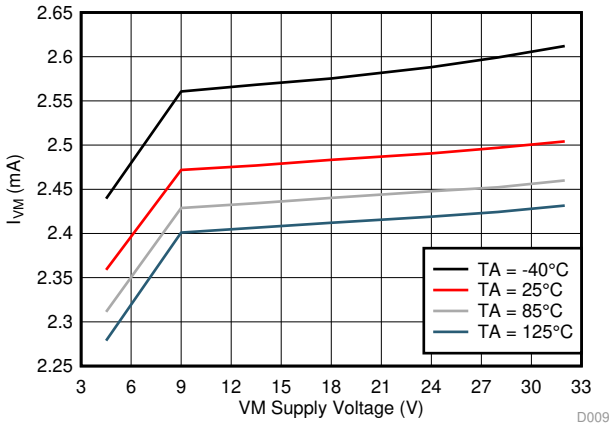


図 10. VM Operating Mode Current (I_{VM}) vs Supply Voltage (V_{VM})

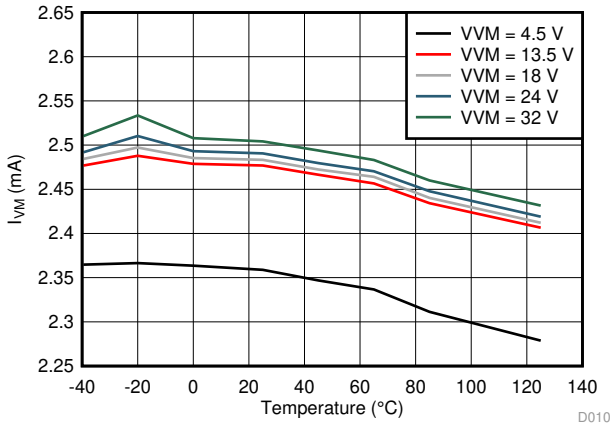


図 11. VM Operating Mode Current (I_{VM}) vs Ambient Temperature (T_A)

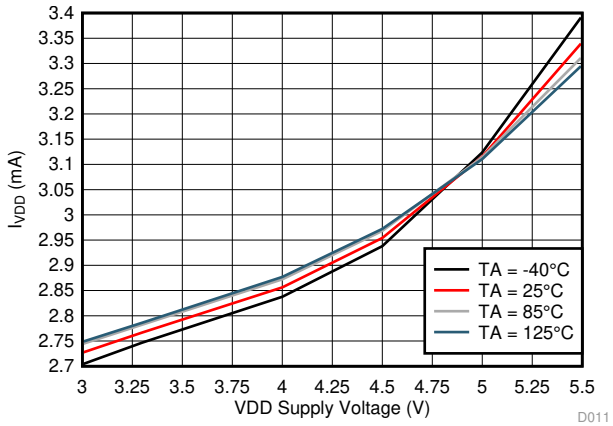


図 12. VDD Operating Mode Current (I_{VDD}) vs Supply Voltage (V_{VDD})

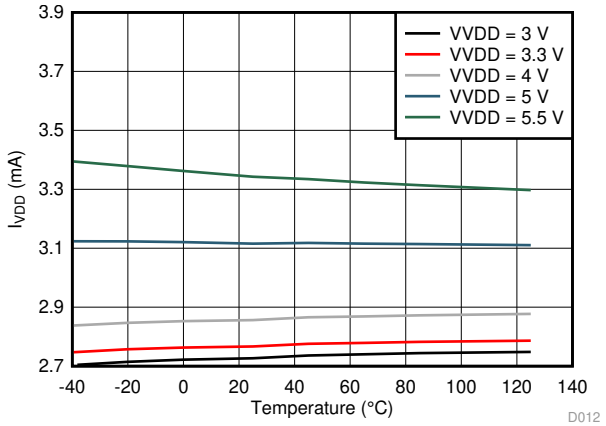


図 13. VDD Operating Mode Current (I_{VDD}) vs Ambient Temperature (T_A)

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Typical Characteristics (continued)

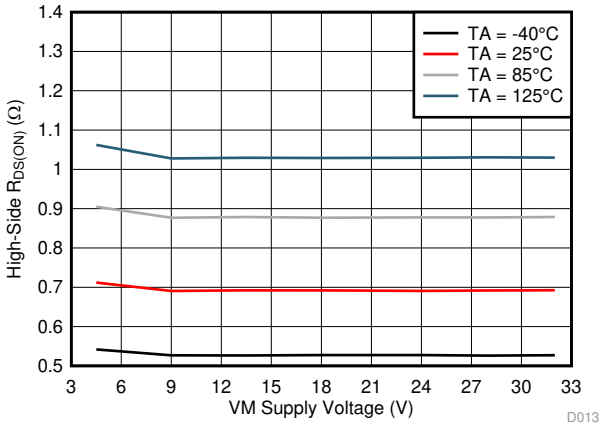


図 14. Figure 7. High Side On-State Resistance ($R_{DS(ON)}$) vs Supply Voltage (V_{VM})

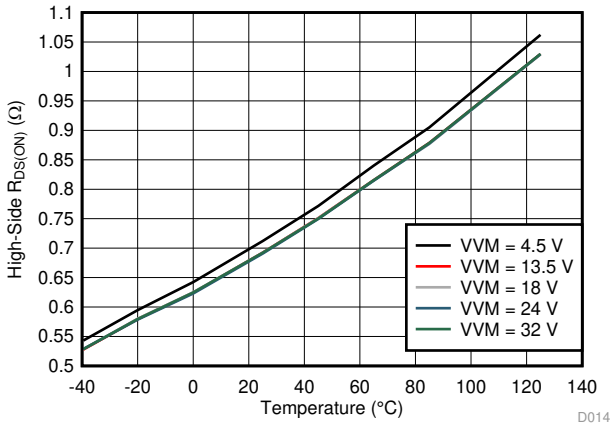


図 15. High Side On-State Resistance ($R_{DS(ON)}$) vs Ambient Temperature (T_A)

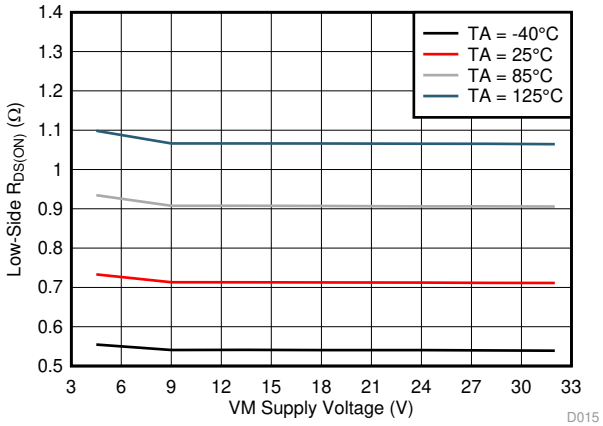


図 16. Low-Side On-State Resistance ($R_{DS(ON)}$) vs Supply Voltage (V_{VM})

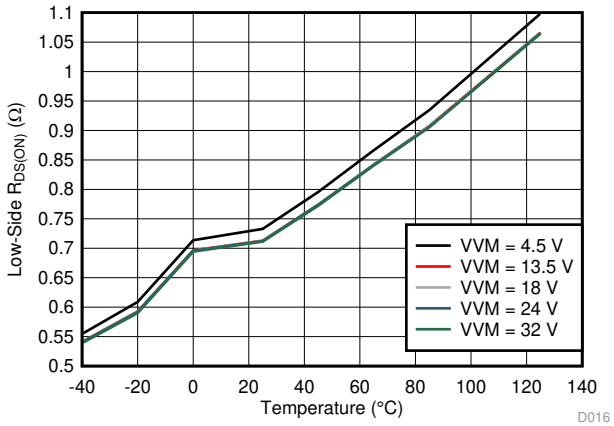


図 17. Low-Side On-State Resistance ($R_{DS(ON)}$) vs Ambient Temperature (T_A)

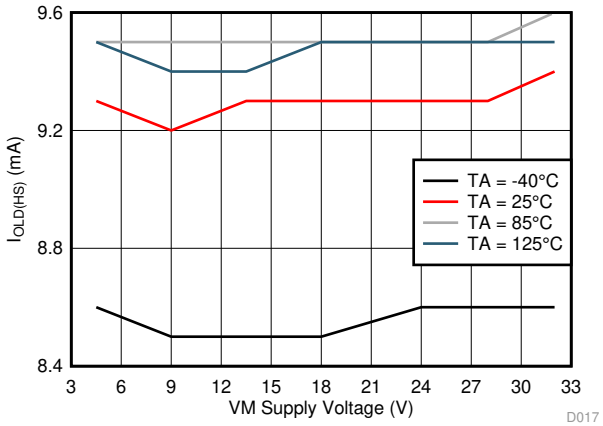


図 18. High-Side Open-Load Detection Current (I_{OLD}) vs Supply Voltage (V_{VM})

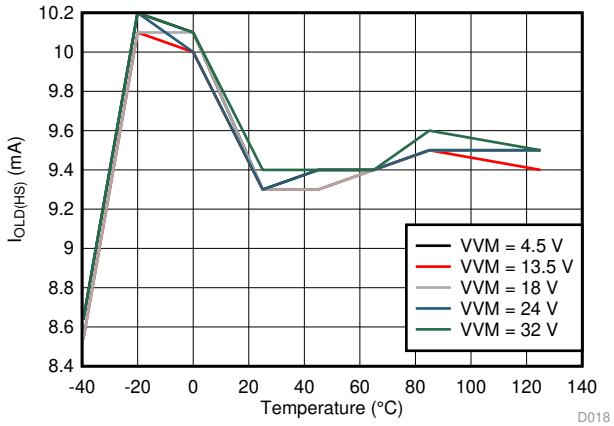


図 19. High-Side Open-load Detection Current (I_{OLD}) vs Ambient Temperature (T_A)

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Typical Characteristics (continued)

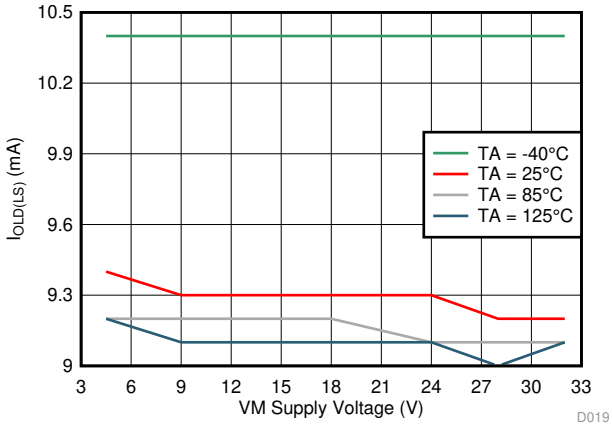


図 20. Low-Side Open-Load Detection Current (I_{OLD}) vs Supply Voltage (V_{VM})

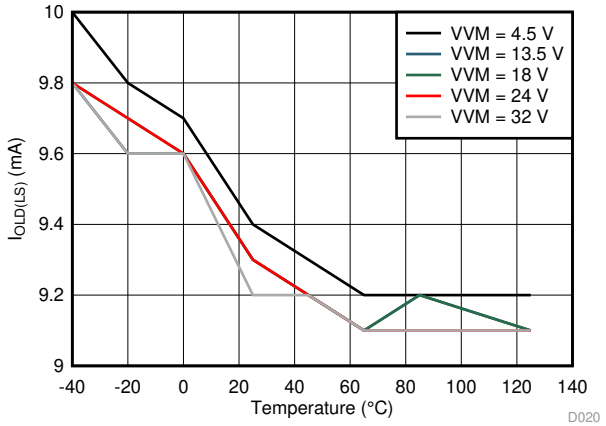


図 21. Low-Side Open-load Detection Current (I_{OLD}) vs Ambient Temperature (T_A)

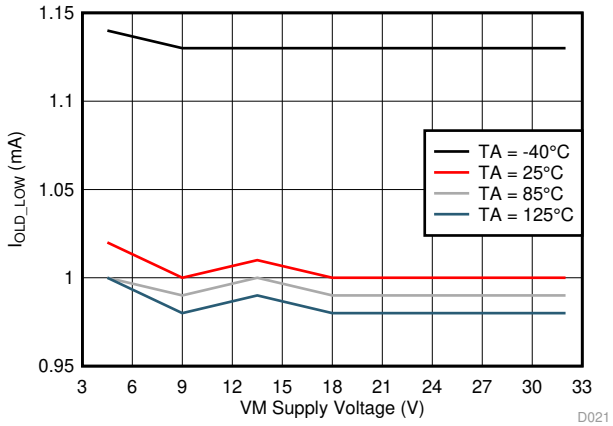


図 22. Low open-load detection current (I_{OLD_LOW}) vs supply voltage (V_{VM})

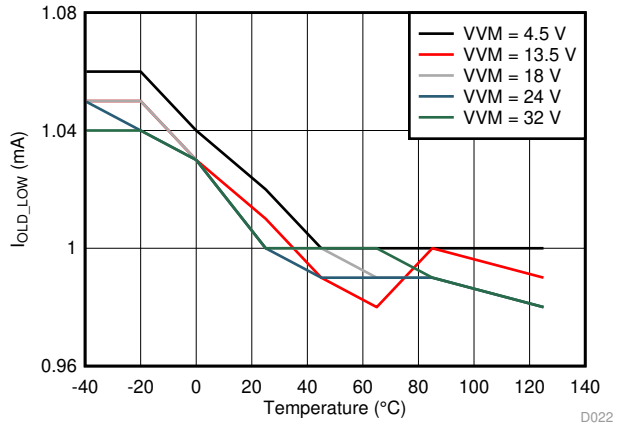


図 23. Low open-load detection current (I_{OLD_LOW}) vs ambient temperature (T_A)

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8 Detailed Description

8.1 Overview

The DRV89xx-Q1 family are 4.5-V to 32-V integrated multi half-bridge drivers which supports a maximum voltage of 40-V for load-dump scenario. The half-bridges are designed to support 1-A per half-bridge and 6-A from the VM/GND pins. The DRV89xx family offers drivers from 4 to 12 half-bridge outputs.

A standard 16-bit, 5-MHz serial peripheral interface (SPI) provides a simple method for configuring the various device settings and reading fault diagnostic information through an external controller. The device is also equipped with a daisy-chain functionality which allows connecting multiple devices using a single nSCS line and saving on multiple resources.

This device has 4 internal PWM generators (DRV8912-Q1 and DRV8910-Q1) or 8 internal PWM generators (DRV8908-Q1, DRV8906-Q1 and DRV8904-Q1) which can be mapped to any of the half-bridge through SPI registers. The PWM frequency (4 options) and duty (8-bit resolution) for each channel can be selected using the SPI registers. This PWM mode is useful for implementing the current control of motor or dimming control of LEDs.

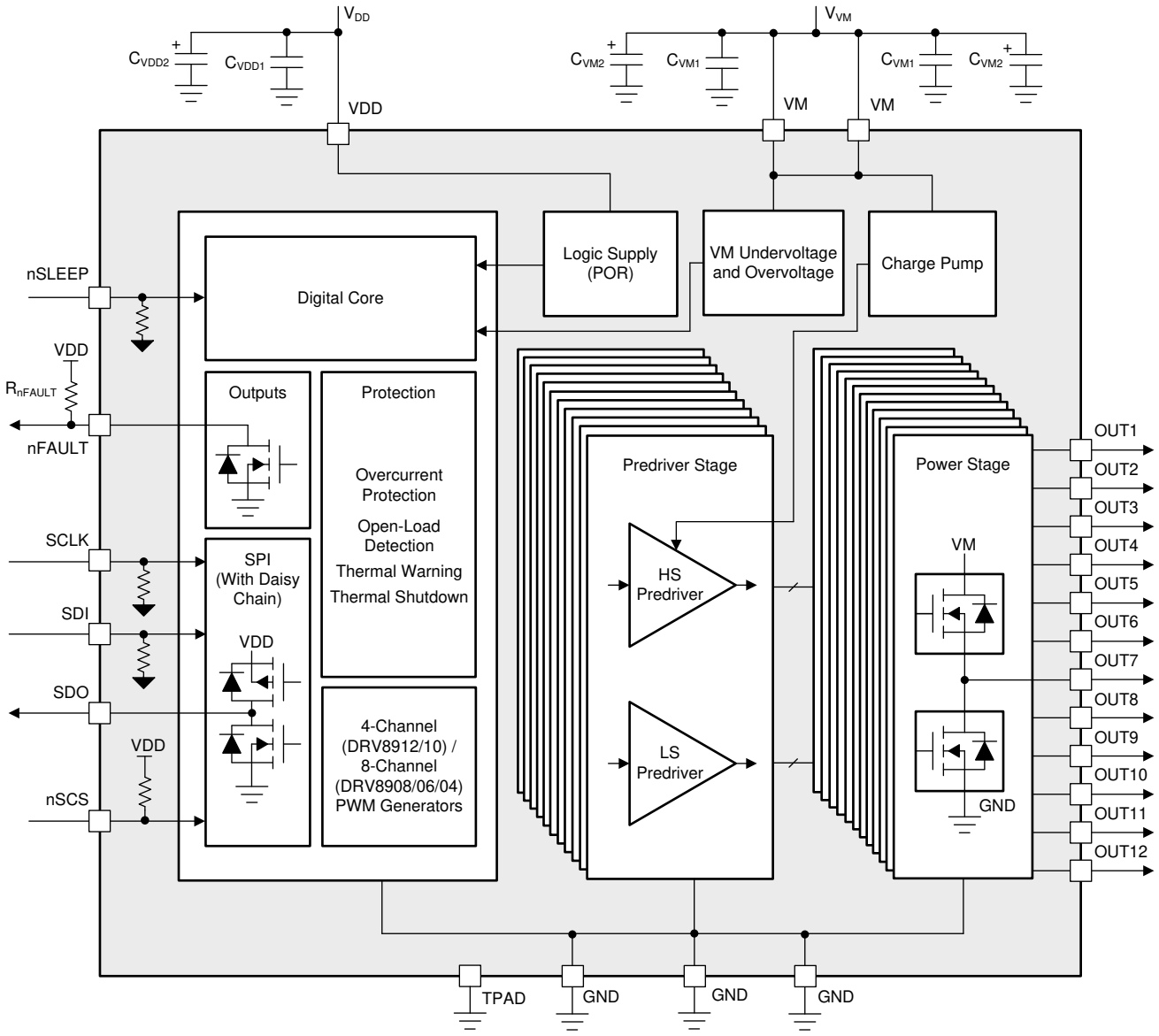
The device also has numerous integrated protection features which protects the device in case of any abnormal scenario. The over-current protection (OCP) ensures the device protection in any short scenarios like the phase short, phase to ground short and phase to supply short conditions. Undervoltage lockout (UVLO) and overvoltage protection (OVP) ensures the driver operation in fluctuating voltages to support the crank-start and load-dump scenario in automotive applications. In addition to this, the open-load detection (OLD) feature ensure the proper load connection. All devices support active OLD, low-current OLD, and negative-current OLD. Passive OLD is only supported on DRV8908-Q1, DRV8906-Q1 and DRV8904-Q1 devices. Device faults are indicated on the nFAULT pin, and detailed information is available in the device SPI registers.

The device integrates a spread spectrum clocking feature for both the internal digital oscillator and internal charge pump. This feature combined with programmable output slew-rate control minimizes the radiated emissions from the device.

The device is available in a 24-pin HTSSOP package with a thermal pad.

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8.2 Functional Block Diagram



8.3 Feature Description

表 1 lists the recommended values of the external components for the driver.

表 1. DRV89xx-Q1 Driver External Components

COMPONENTS	PIN 1	PIN 2	RECOMMENDED
C_{VM1}	VM	GND	X5R or X7R, 0.1-µF, VM-rated capacitor
C_{VM2}	VM	GND	≥ 10 µF, VM-rated capacitor
C_{VDD1}	VDD	GND	X5R or X7R, 0.1-µF, 6.3-V capacitor
C_{VDD2}	VDD	GND	≥ 1 µF, 6.3-V capacitor
R_{nFAULT}	VDD	nFAULT	Pullup resistor

8.3.1 Half Bridge Drivers

8.3.1.1 Control Modes

The half-bridge drivers can be programmed to drive loads (motor, solenoids, LEDs) continuously (without PWM) or in chopping mode (with PWM) and in parallel operation for driving high current.

8.3.1.1.1 *Continuous Mode (Without PWM)*

The half-bridges are configured to operate in the continuous mode without using any PWM switching by default. Any high-side or low-side switch is switched on by individually setting the high-side enable bits (HBX_HS_EN) and low-side enable bits (HBX_LS_EN) in operation control registers (OP_CTRL_1, OP_CTRL_2 and OP_CTRL_3).

注

If the high-side enable bit (HBX_HS_EN) and low-side enable bit (HBX_LS_EN) of a particular half-bridge is set high (shoot-through configuration), then the particular half-bridge driver will remain in Hi-Z state until he shoot-through condition is cleared.

The high-side and low-side enable bits of a particular half-bridge are configured to drive the motor in forward mode, reverse mode, brake mode and coast mode as shown in 表 2.

表 2. Motor Operation in Continuous Mode (Motor Connected between HB1 and HB2)

nSLEEP	HALF-BRIDGE-1	HALF-BRIDGE-2	OUT1	OUT2	BRIDGE OPERATION (DC MOTOR)
0	HB1_HS_EN = Don't Care HB1_LS_EN = Don't Care	HB2_HS_EN = Don't Care HB2_LS_EN = Don't Care	Z	Z	Sleep Mode
1	HB1_HS_EN = 0 HB1_LS_EN = 0	HB2_HS_EN = 0 HB2_LS_EN = 0	Z	Z	Motor Coast
1	HB1_HS_EN = 1 HB1_LS_EN = 0	HB2_HS_EN = 0 HB2_LS_EN = 1	H	L	Forward Direction
1	HB1_HS_EN = 0 HB1_LS_EN = 1	HB2_HS_EN = 1 HB2_LS_EN = 0	L	H	Reverse Direction
1	HB1_HS_EN = 0 HB1_LS_EN =1	HB2_HS_EN = 0 HB2_LS_EN = 1	L	L	Motor Brake (Low-Side)
1	HB1_HS_EN =1 HB1_LS_EN = 0	HB2_HS_EN = 1 HB2_LS_EN = 0	H	H	Motor Brake (High-Side)
1	HB1_HS_EN = 1 HB1_LS_EN = 1	HB2_HS_EN = 1 HB2_LS_EN = 1	Z	Z	Motor Coast

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図 24 shows the bridge configuration for motor operation in forward direction with high-side FET of OUT1 and low-side FET of OUT2 in conducting state with current flowing from OUT1 to OUT2. Similarly, the motor operation in reverse direction is achieved by switching ON the high-side FET of OUT2 and low-side FET of OUT1 such that current flows from OUT2 to OUT1 as shown in 図 25.

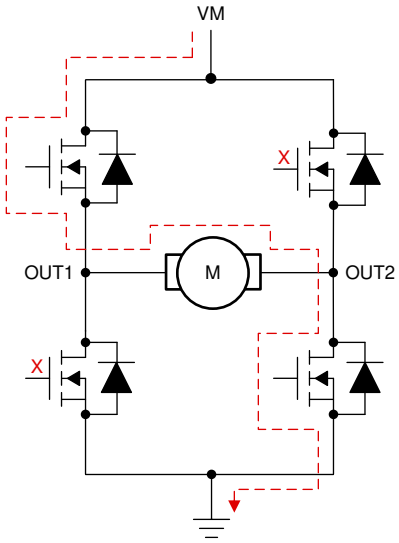


図 24. Continuous Mode (Forward Direction)

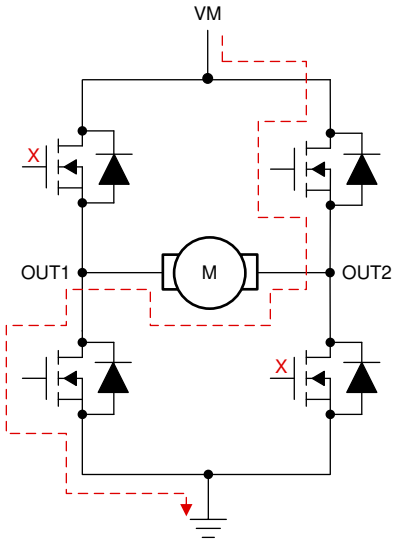


図 25. Continuous Mode (Reverse Direction)

図 26 and 図 27 shows the bridge operation in coast mode with motor initially running in forward and reverse direction respectively. As shown in these figures, due to the energy stored in motor's inductance, the current will continue to flow in motor and take the path flow through the body diodes of FETs.

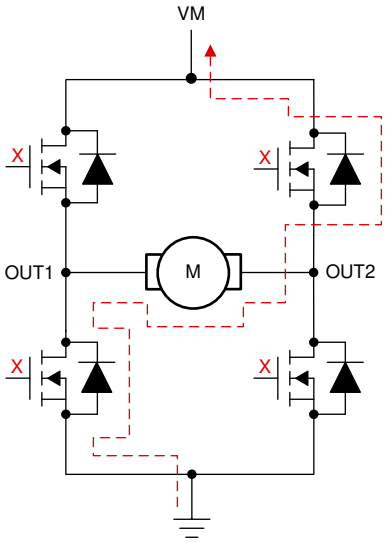


図 26. Continuous Mode (Coast - From Forward Direction)

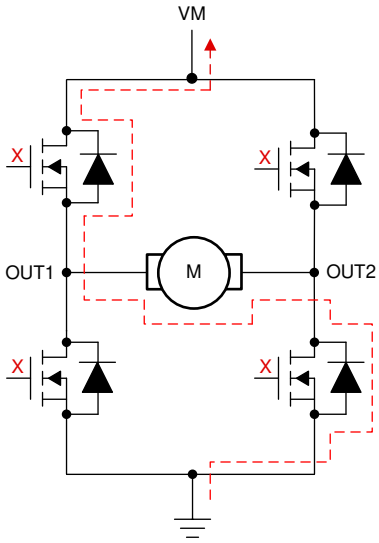


図 27. Continuous Mode (Coast- From Reverse Direction)

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図 28 shows the low-side braking of the motor when both low-side FET's of the driver are turned ON. In this case, the motor is considered to be operating in forward direction (current flow from OUT1 to OUT2) and then braking is applied. similarly, for the high-side braking, both high-side FET's of the driver are turned ON as shown in 図 29.

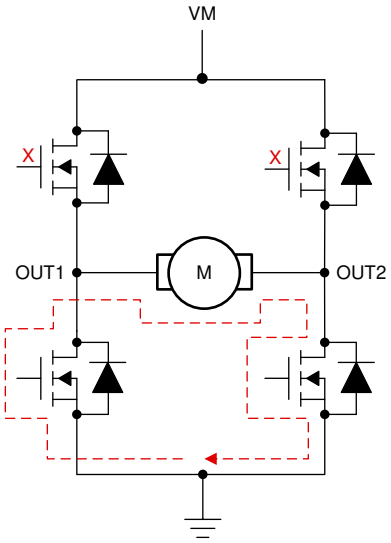


図 28. Continuous Mode (Brake - Low-Side)

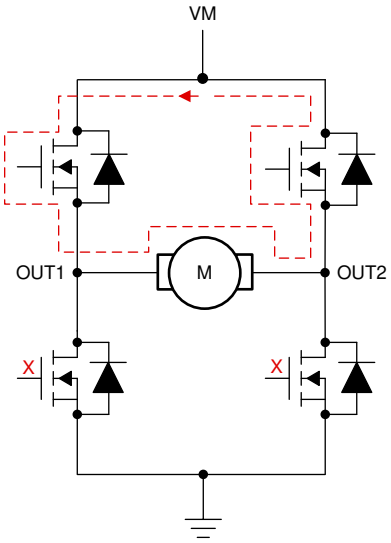


図 29. Continuous Mode (Brake - High-Side)

8.3.1.1.2 *Chopping Mode (With PWM)*

The half-bridges can be configured in the chopping mode by enabling the PWM switching on any particular half-bridge or both half-bridges. Each half-bridge can be mapped to any of the 4 PWM channels for which frequency and duty can be controlled independently. User has the flexibility to select the PWM frequency of channels out of 4 settings of 80-Hz, 100-Hz, 200-Hz and 2-kHz. Moreover, duty (8-bit resolution) of the 4 PWM generators can be adjusted independently.

The PWM chopping mode operation is done in five steps as follows and explained in detail below.

1. PWM Configuration
2. Free-Wheeling Mode (Synchronous Rectification) Disable / Enable
3. PWM Channels Mapping
4. PWM Channels Configuration (PWM Frequency and PWM Duty)
5. Half-Bridge Enable

8.3.1.1.2.1 PWM Configuration

The operation of selected half-bridge to operate in continuous mode or chopping mode (PWM mode) is selected using the PWM control register (PWM_CTRL_1 and PWM_CTRL_2). The HBX_PWM bit in PWM control register is set to enable the PWM switching in half-bridge.

注

The default mode of any half-bridge is continuous mode. If the corresponding HBx_PWM bit in PMW_CTRL_X register is not set, then the particular half-bridge will operate in continuous mode.

8.3.1.1.2.2 Free-Wheeling Mode (Synchronous Rectification) Disable / Enable

The synchronous rectification of the half-bridge operating in PWM can be enabled by setting the HBX_FW bit in free-wheeling control registers (FW_CTRL_1 and FW_CTRL_2). 図 30 shows the operation of the driver when the synchronous rectification mode is disabled. As shown in this figure, during the PWM off time, the high-side diode of the OUT2 conducts to close the current path required for motor.

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When synchronous rectification mode is enabled, if either of the low-side or high-side of the half-bridge operates in the PWM switching, then the other switch of the same half-bridge operates in complementary fashion. 図 31 shows such example of the synchronous rectification, where the high-side FET of OUT2 half-bridge is turned ON when the low-side FET of same half-bridge is turned off in a PWM cycle.

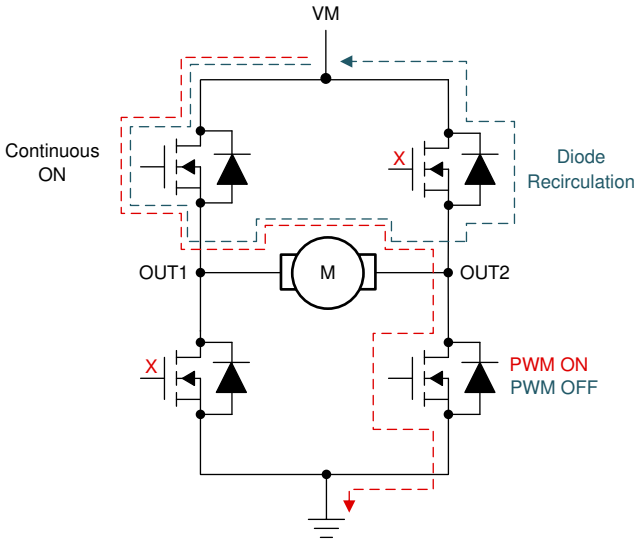


図 30. PWM Mode (Synchronous Rectification = OFF)

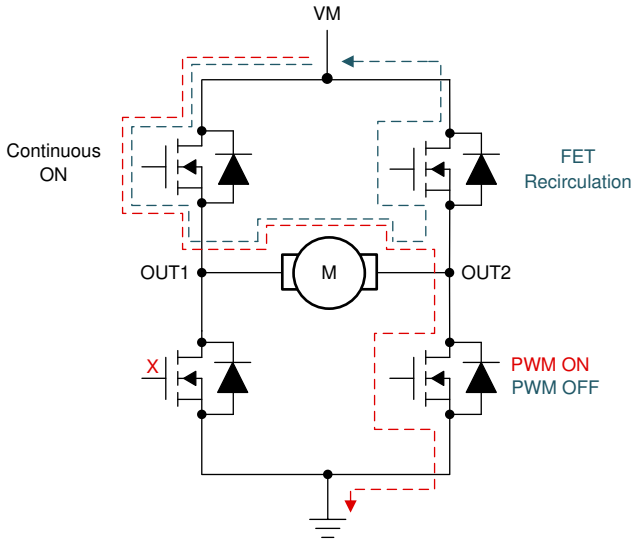


図 31. PWM Mode (Synchronous Rectification = ON)

注

The default mode of any half-bridge is asynchronous rectification mode. If the corresponding bit in FW_CTRL_X regsiter is not set, then the particular half-bridge will operate in asynchronous rectification mode.

8.3.1.1.2.3 PWM Channels Mapping

DRV89XX-Q1 devices includes 4/8 PWM generators which can be mapped to any of the OUTX half bridge outputs using the PWM map control registers. The HBx_PWM_MAP bits in the PWM_MAP_CTRL_X registers are used to map any of the 4 channels in DRV8912-Q1/DRV8910-Q1 or 8 channels in DRV8908-Q1/DRV8906-Q1/DRV8904-Q1 to the OUTX outputs as shown in 表 3.

表 3. PWM Mapping of DRV8912-Q1/DRV8910-Q1

HBX_PWM MAP BITS	PWM CHANNEL
HBX_PWM_MAP = 00b	Channel 1 Selected for OUTX
HBX_PWM_MAP = 01b	Channel 2 Selected for OUTX
HBX_PWM_MAP = 10b	Channel 3 Selected for OUTX
HBX_PWM_MAP = 11b	Channel 4 Selected for OUTX

注

Any half-bridge is mapped to PWM channel 1 by default.

8.3.1.1.2.4 PWM Channels Configuration (PWM Frequency and PWM Duty)

The frequency and duty of each PWM generator can be controlled independently. The PWM_CHx_FREQ bits of PWM frequency control register (PWM_FREQ_CTRL) is used to select the frequency of PWM generator as shown in 表 4. The PWM duty of each channel is controlled by the PWM duty control register (PWM_DUTY_CTRL_X).

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表 4. PWM Frequency

HBX_PWM MAP BITS	PWM CHANNEL
PWM_CHx_FREQ = 00b	80 Hz
PWM_CHx_FREQ = 01b	100 Hz
PWM_CHx_FREQ = 10b	200 Hz
PWM_CHx_FREQ = 11b	2000 Hz

8.3.1.1.2.5 Half-Bridge Enable

The four steps of PWM mode enable, free-wheeling mode configuration, PWM channel mapping and PWM channels configuration ensure the proper configuration of PWM mode. Once the half-bridge is configured for the PWM generation, the half-bridge is enabled by enabling either of the high-side or low-side switch by individually setting the high-side enable bits (HBX_HS_EN) or low-side enable bits (HBX_LS_EN) in operation control registers (OP_CTRL_1, OP_CTRL_2 and OP_CTRL_3).

注

The PWM is applicable to either of the high-side or low-side switch depending upon the HBX_HS_EN and HBX_LS_EN bits in OP_CTRL_X registers. In synchronous rectification mode, the opposite side switch will conduct in PWM off time.

8.3.1.1.3 Parallel Mode (Continuous Operation)

Parallel mode in DRV89XX-Q1 device is implemented to support higher current loads which cannot be supported by a single channel. This mode can also be used for reducing the effective on-state resistance ($R_{DS(ON)}$) for achieving a better thermal performance of the device.

The configuration of various mode is very similar to the single half-bridge operation as explained in *Continuous Mode (Without PWM)* section. Considering six half-bridges for the parallel operation (OUT1, OUT2, OUT3 as group - 'X' and OUT4, OUT5, OUT6 as group 'Y'), various modes can be summarized in 表 5.

表 5. Motor Operation in Parallel Mode (Continuous Operation) (with Motor Connected between OUT1/2/3 and OUT4/5/6)

nSLEEP	HALF-BRIDGE-1 HALF-BRIDGE-2 HALF-BRIDGE-3 (X)	HALF-BRIDGE-4 HALF-BRIDGE-5 HALF-BRIDGE-6 (Y)	OUT1 OUT2 OUT3	OUT4 OUT5 OUT6	BRIDGE OPERATION (DC MOTOR)
0	HBX_HS_EN = Don't Care HBX_LS_EN = Don't Care	HBY_HS_EN = Don't Care HBY_LS_EN = Don't Care	Z	Z	Sleep Mode
1	HBX_HS_EN = 0 HBX_LS_EN = 0	HBY_HS_EN = 0 HBY_LS_EN = 0	Z	Z	Motor Coast
1	HBX_HS_EN = 1 HBX_LS_EN = 0	HBY_HS_EN = 0 HBY_LS_EN = 1	H	L	Forward Direction
1	HBX_HS_EN = 0 HBX_LS_EN = 1	HBY_HS_EN = 1 HBY_LS_EN = 0	L	H	Reverse Direction
1	HBX_HS_EN = 0 HBX_LS_EN =1	HBY_HS_EN = 0 HBY_LS_EN = 1	L	L	Motor Brake (Low-Side)
1	HBX_HS_EN =1 HBX_LS_EN = 0	HBY_HS_EN = 1 HBY_LS_EN = 0	H	H	Motor Brake (High-Side)
1	HBX_HS_EN = 1 HBX_LS_EN = 1	HBY_HS_EN = 1 HBY_LS_EN = 1	Z	Z	Motor Coast

注

For parallel mode operation, the device operation under safe operating area (SOA) is recommended for supply voltage, V_{VM} ≤ 20-V, HBX_SR = HBY_SR = 1b, t_{OCP} ≤ 10-µs and PL_MODE_EN = 01b.

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図 32 shows three half-bridges (OUT1, OUT2 and OUT3) operating as a parallel high-side switch and other three half-bridges (OUT4, OUT5 and OUT6) are operating as a parallel low-side switch for achieving a forward motor operation. Similarly the reverse direction of motor is achieved by operation of OUT1, OUT2 and OUT3 as a parallel low-side switch and other three half-bridges (OUT4, OUT5 and OUT6) as parallel high-side switch as shown in 図 33.

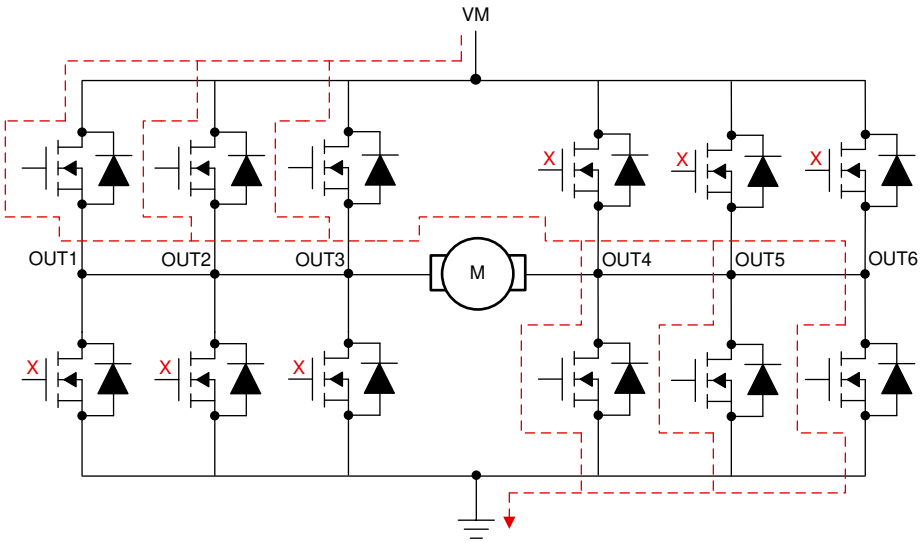


図 32. Parallel Mode (Forward Direction)

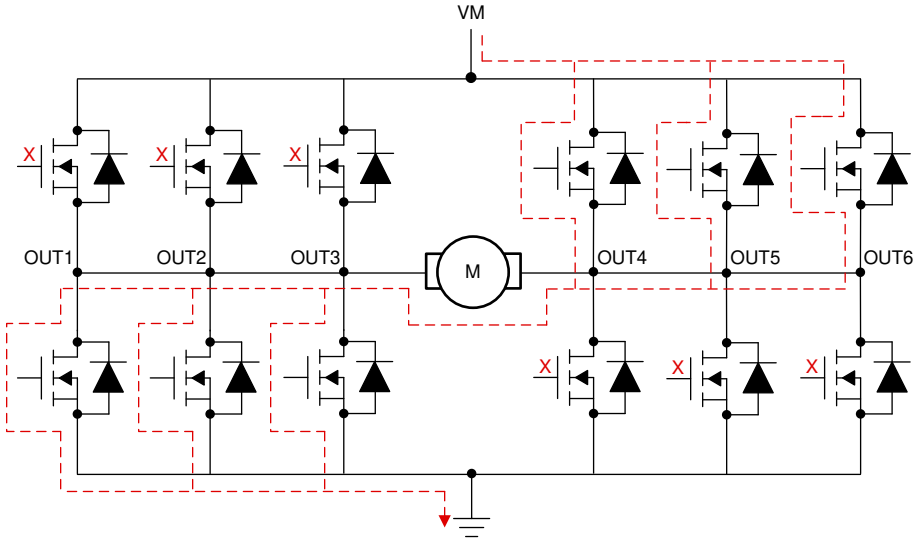


図 33. Parallel Mode (Reverse Direction)

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図 34 and 図 35 shows the bridge operation in coast mode with motor initially running in forward and reverse direction respectively. As shown in these figures, the body diodes of the FETs conducts to continue the current flow path due to energy stored in motor's inductance.

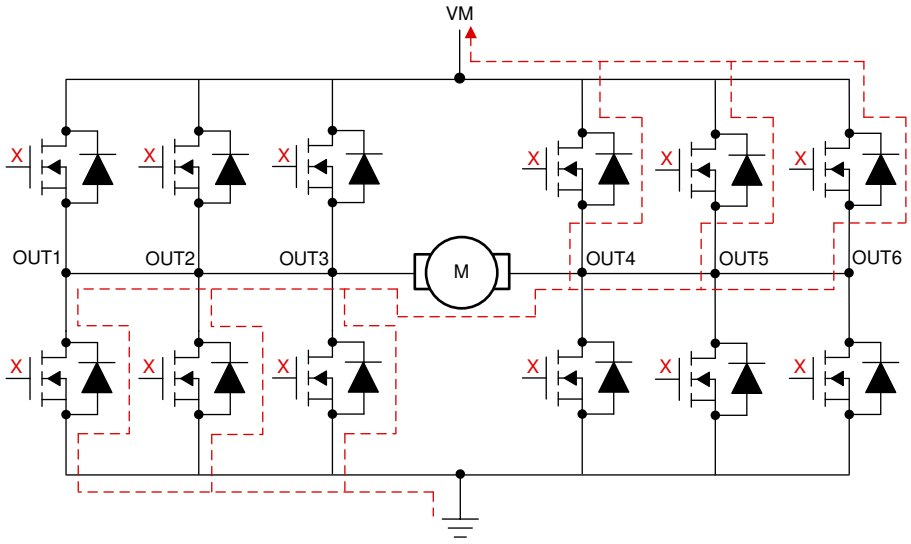


図 34. Parallel Mode (Coast from Forward Direction)

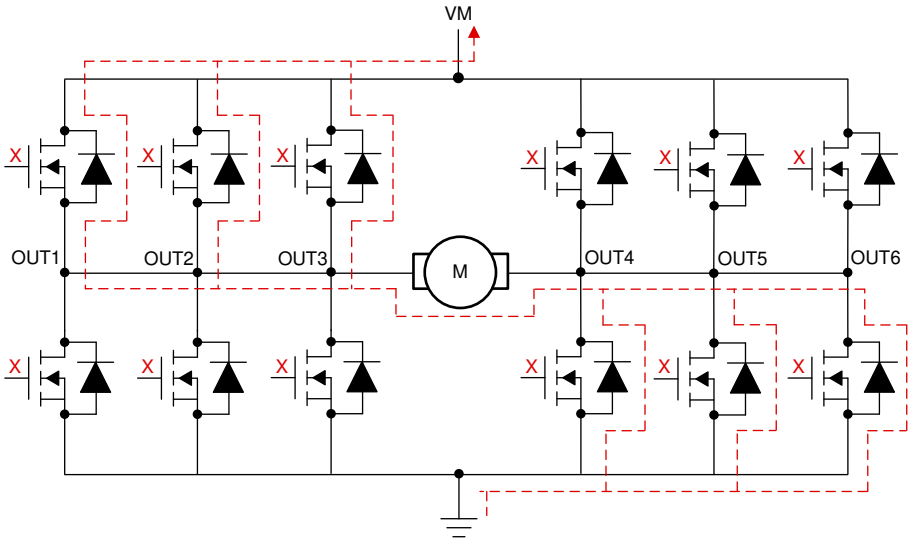


図 35. Parallel Mode (Coast from Reverse Direction)

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The low-side braking of the motor during all the low-side FET's of the driver turning ON is shown in 図 36. In this case, the motor is considered to be operating in forward direction (current flow from OUT1/2/3 to OUT4/5/6) and then braking is applied. similarly, for the high-side braking, all high-side FET's of the driver are turned ON as shown in 図 37.

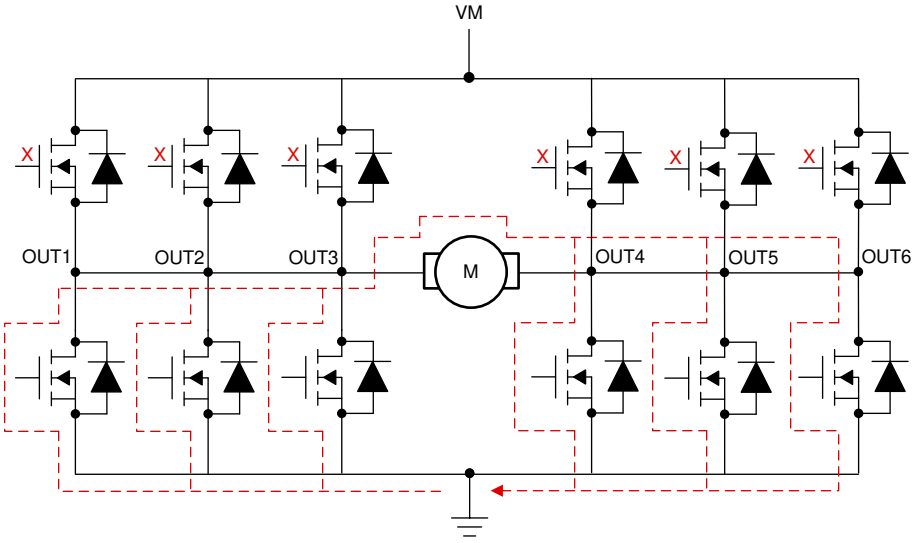


図 36. Parallel Mode (Brake - Low-Side)

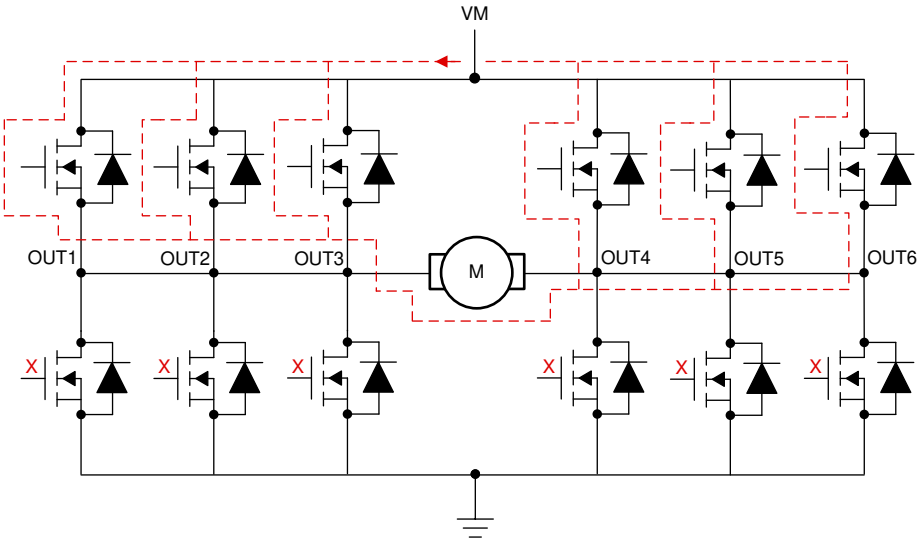


図 37. Parallel Mode (Brake - High-Side)

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8.3.1.1.4 Parallel Mode (PWM Operation)

The half-bridges connected in parallel mode can be configured in the chopping mode by enabling the PWM switching on any particular group of high-side or low-side half-bridges or both group of half-bridges. For PWM operation in parallel mode, all half-bridges is to be mapped to a single PWM channel selected from any of the 4 PWM channels to avoid any delay in the PWM durations which can lead to undesired OCP condition. The user has the flexibility to select the PWM frequency of channels out of 4 settings of 80-Hz, 100-Hz, 200-Hz and 2-kHz and the duty adjustment which supports 8-bit resolution. Following steps enable the PWM operation with driver connected for parallel mode and are explained below.

1. PWM Configuration
2. Free-Wheeling Mode (Synchronous Rectification) Disable / Enable
3. PWM Channels Mapping
4. PWM Channels Configuration (PWM Frequency and PWM Duty)
5. PWM Generators Disable
6. Half-Bridge Enable
7. PWM Generators Enable

8.3.1.1.4.1 PWM Configuration

The PWM control register (PWM_CTRL_1 and PWM_CTRL_2) are used to select the operation of particular half-bridges in the PWM mode. Considering a case for the motor movement in forward direction as shown in 図 34, with low-side FETs of OUT4, OUT5 and OUT6 operating in PWM mode. The HBX_PWM bit in PWM control register is set to enable the PWM switching in selected half-bridges as shown below:

- HB4_PWM = 1b
- HB5_PWM = 1b
- HB6_PWM = 1b

8.3.1.1.4.2 Free-Wheeling Mode (Synchronous Rectification) Disable / Enable

The synchronous rectification of the half bridges operating in PWM mode (OUT4, OUT5 and OUT6) are enabled by setting the corresponding HBX_FW bits in free-wheeling control register (FW_CTRL_1 and FW_CTRL_2). By default, the synchronous rectification mode is disabled.

- HB4_FW = 1b
- HB5_FW = 1b
- HB6_FW = 1b

図 38 shows the parallel operation of half-bridges in PWM mode with synchronous rectification disabled. As shown in this figure, during the PWM off time, the high-side diode of the OUT4, OUT5 and OUT6 conducts to close the current path required for motor.

When synchronous rectification mode is enabled, the high-side FETs of OUT4, OUT5 and OUT6 starts conducting during the PWM OFF time to close the motor current path as shown in 図 39.

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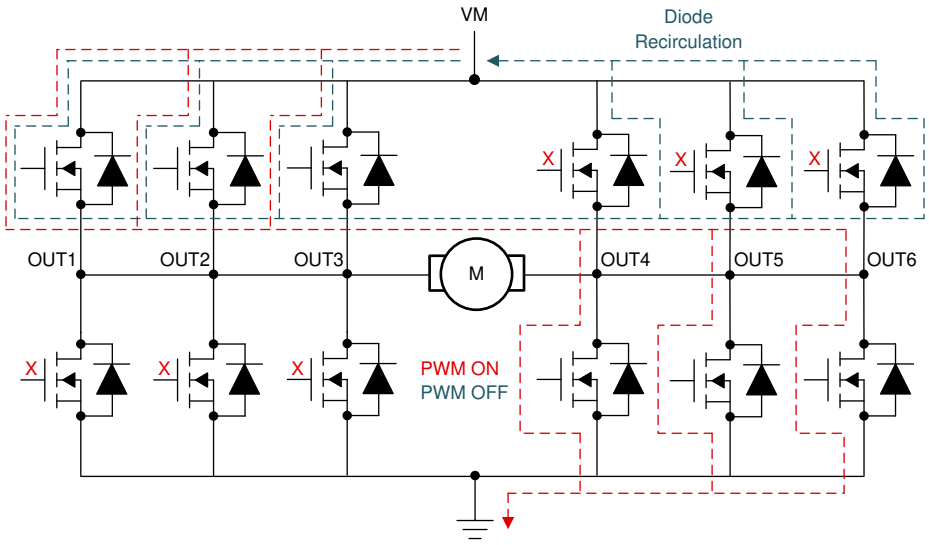


図 38. Parallel Mode (PWM with Synchronous Rectification = OFF)

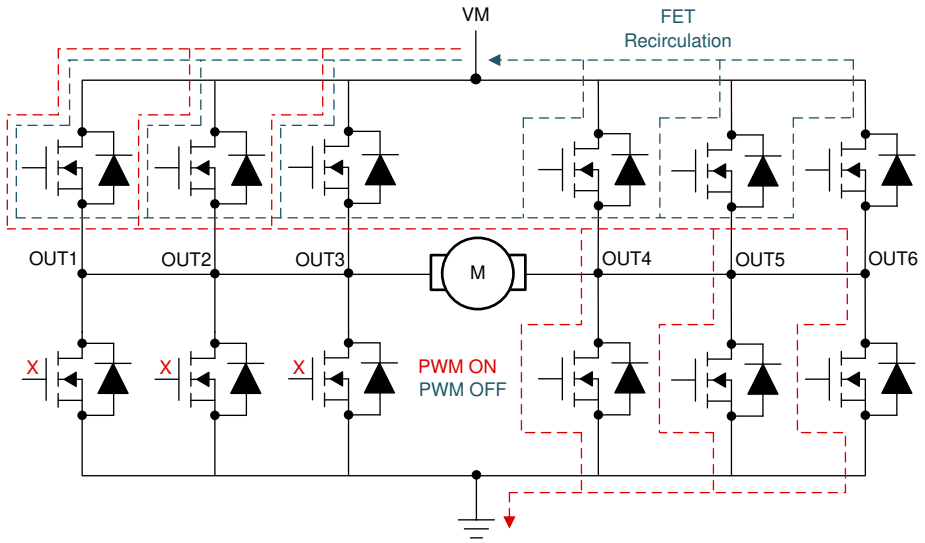


図 39. Parallel Mode (PWM with Synchronous Rectification = ON)

8.3.1.1.4.3 PWM Channels Mapping

The low-side FET's of half-bridges OUT4, OUT5 and OUT6 are mapped to any of the PWM generator by using the HBX_PWM_MAP bits in PWM mapping control registers. For parallel operation, all the half-bridges operating in PWM mode is mapped to a single PWM generator. Considering that PWM generator-4 is used for the mapping of half-bridges, following bits of the PWM_MAP_CTRL_X registers are affected:

- HB4_PWM_MAP = 11b
- HB5_PWM_MAP = 11b
- HB6_PWM_MAP = 11b

注

If the PWM of any channel is enabled, then it is mapped to PWM generator-1 by default.

8.3.1.1.4.4 PWM Channels Configuration (PWM Frequency and PWM Duty)

The PWM_CHx_FREQ bits of PWM frequency control registers (PWM_FREQ_CTRL_X) is used to select the frequency of PWM generator. Moreover, the PWM duty of each channel is controlled by the PWM duty control register (PWM_DUTY_CTRL_X). Considering a frequency of 2-kHz is selected for the PWM operation (for PWM Generator-4), following frequency control and duty control registers are effected:

- PWM_CH4_FREQ = 11b
- PWM_CH4_FREQ = '8-bit duty'

8.3.1.1.4.5 PWM Generators Disable

The PWM generators are disabled to ensure that all the half-bridges are turned-on at same time to avoid false OCP conditions for supporting higher current operation. The false OCP condition can arise due to the minimum time required for the SPI delay to switch on various half-bridges available in different registers. This can cause higher current (OCP condition) in one of the paralleled half-bridge while other half-bridge turning ON is delayed to the SPI register write delay and the propagation delay. Therefore, this sequence includes disabling the PWM generators initially, then enabling half-bridges and followed by enabling the PWM generators to avoid such issue. The PWM generator-4 is disabled by using the following command in the PWM_CTRL_X registers:

- PWM_CH4_DIS = 1b

注

All PWM generators are enabled by default (Default value of PWM_CTRL_X registers is 00h).

8.3.1.1.4.6 Half-Bridge Enable

Once the PWM generators are disabled, the high-side and low-side FETs in half-bridges to be paralleled are enabled. High-side switches (connected in parallel) operating in continuous mode are enabled using the following bits in the OP_CTRL_X registers:

- HB1_HS_EN = 1b
- HB2_HS_EN = 1b
- HB3_HS_EN = 1b

Moreover, the low-side switches (connected in parallel) operating in PWM mode are enabled using the following bits in the OP_CTRL_X:

- HB4_LS_EN = 1b
- HB5_LS_EN = 1b
- HB6_LS_EN = 1b

8.3.1.1.4.7 PWM Generators Enable

After the half-bridges are enabled, the PWM generators are also enabled for tuning-on the respective FETs operating in PWM mode. For this case, the low-side FETs of OUT4, OUT5 and OUT6 are turned ON for PWM operation connected to PWM generator-4. The PWM generator is enabled by the bits in the PWM_CTRL_X registers as shown:

- PWM_CH4_DIS = 0b

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8.3.1.2 Half-Bridge Drive Architecture

8.3.1.2.1 Slew Rate

An adjustable gate-drive current control to the MOSFETs of half-bridges is implemented to achieve the slew rate control. The MOSFET VDS slew rates are a critical factor for optimizing radiated emissions, energy and duration of diode recovery spikes and switching voltage transients related to parasitics. These slew rates are predominantly determined by the rate of gate charge to internal MOSFETs as shown in 図 40.

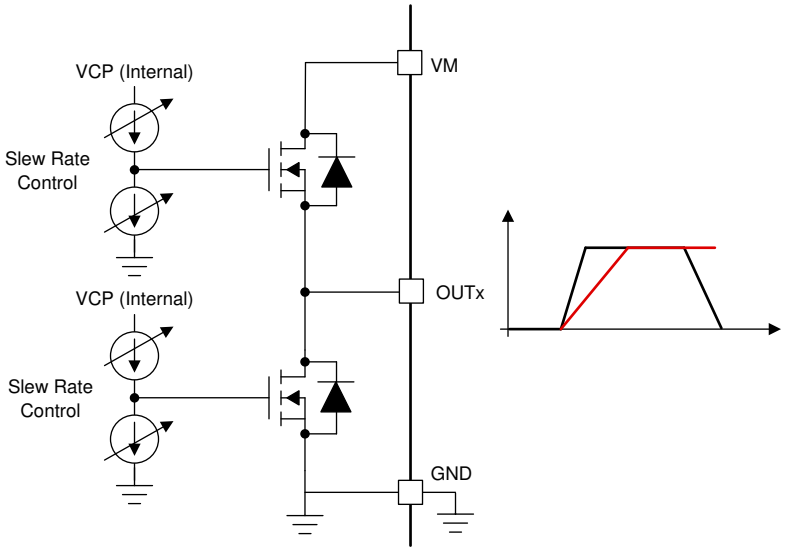


図 40. Slew Rate Circuit Implementation

The slew rate of each half-bridge can be adjusted by HBX_SR bits in Slew Rate control register (SR_CTRL_1 and SR_CTRL_2). Each half-bridge can be selected to a slew rate of 0.6-V/µs or 2.5-V/µs. The slew rate is calculated by the rise-time and fall-time of the voltage on OUTx pin as shown in 図 41. The slew rate (SR) is calculate as shown in

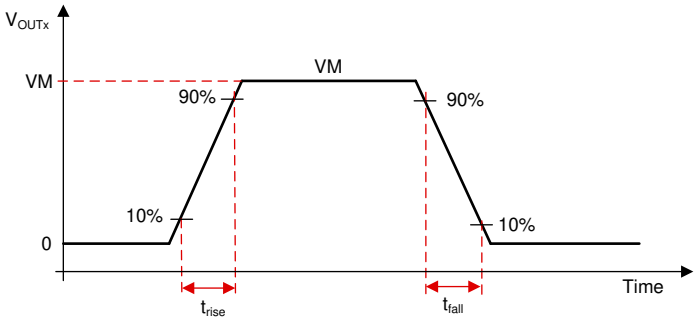


図 41. Slew Rate Timings

8.3.1.2.2 Cross Conduction (Dead Time)

The device is fully protected for any cross conduction of MOSFETs. In half-bridge configuration, the operation of high-side and low-side MOSFETs are ensured to avoid any shoot through currents by inserting a dead time (t_{dead}). This is implemented by sensing the gate-source voltage (V_{GS}) of the high-side and low-side MOSFETs and ensured that V_{GS} of high-side MOSFET has reached below turn-off levels before switching on the low-side MOSFET of same half-bridge as shown in 図 42 and 図 43.

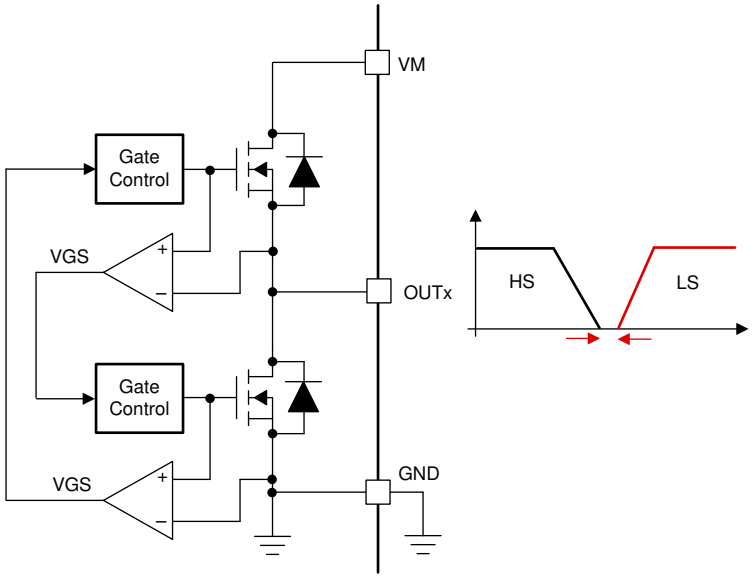


図 42. Cross Conduction Protection

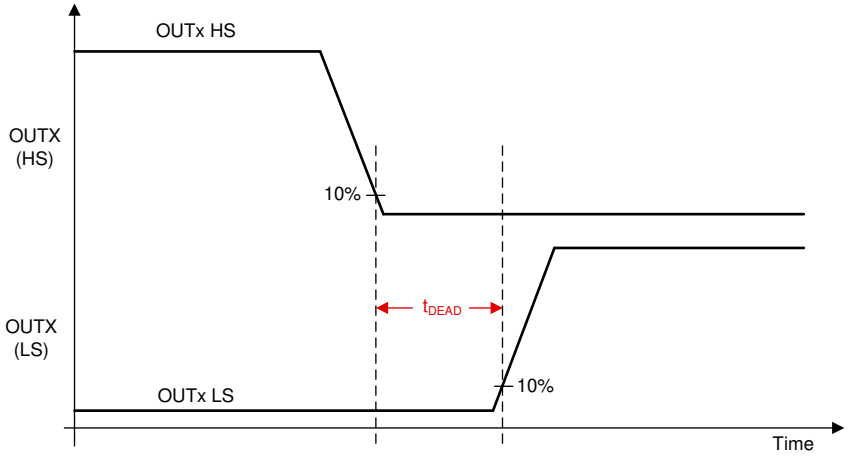


図 43. Dead Time

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8.3.1.2.3 Propagation Delay

Propagation delay refers to the delay time from SPI valid condition to OUTx going high (10% level) as shown in 図 44. The propagation constitutes of three major parameters.

1. Digital delay for SPI command decode.
2. Analog delay for driver switch-on and gate current charging delay.
3. Slew rate delay for OUTx node to reach 10% of the final settling value.

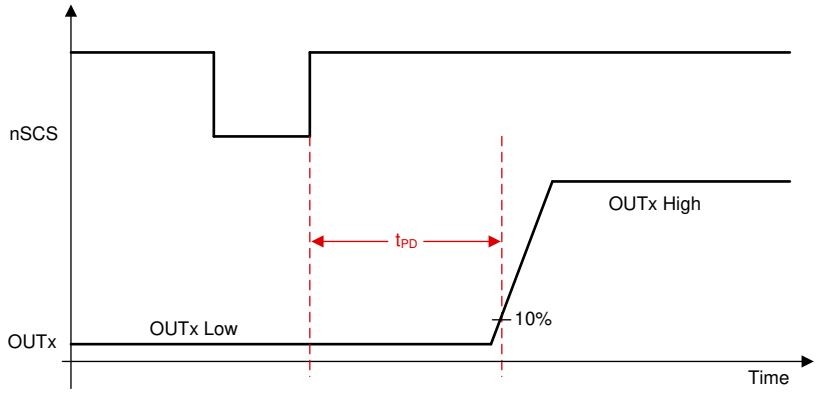


図 44. Propagation Delay

8.3.2 Pin Diagrams

This section presents the I/O structure of all digital input and output pins.

8.3.2.1 Logic Level Input Pin (nSLEEP, SCLK and SDI)

図 45 shows the input structure for the logic levels pins, nSLEEP, SCLK and SDI. The input can be with a voltage or external resistor. It is recommended to put SCLK and SDI pin low in device sleep mode to reduce leakage current through internal pull-down resistors.

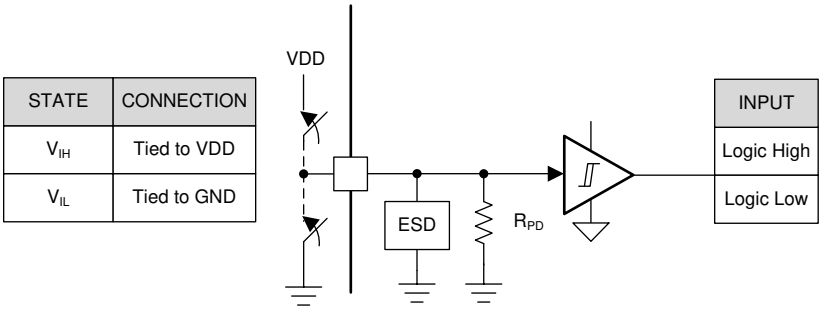


図 45. Logic Level Input Pin Structure (nSLEEP, SCLK and SDI)

8.3.2.2 Logic Level Input Pin (nSCS)

図 46 shows the input structure for the logic levels pin, nSCS. The input can be with a voltage or external resistor.

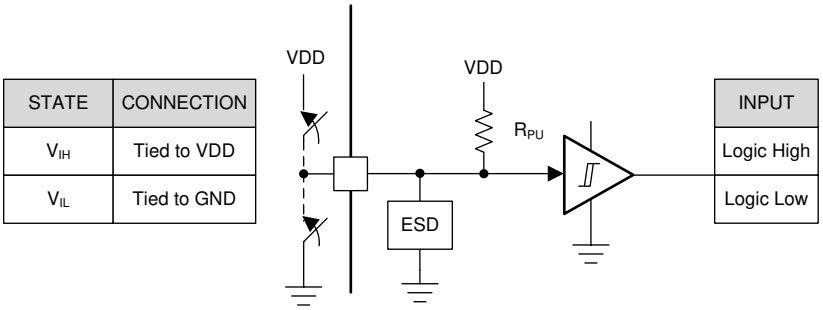


図 46. Logic Level Input Pin Structure (nSCS)

8.3.2.3 Open Drain Output Pin (nFAULT)

図 47 shows the structure of the open-drain output pin, nFAULT. The open-drain output requires an external pullup resistor to function properly.

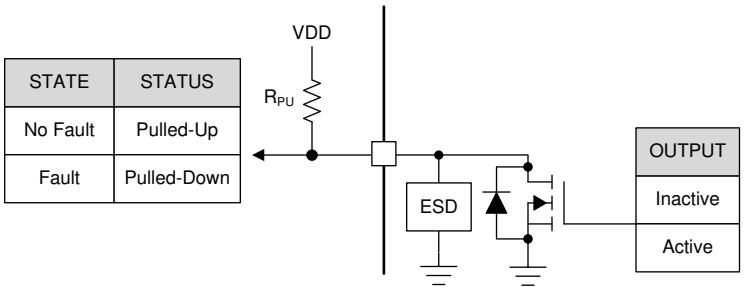


図 47. Open Drain Output Pin Structure (nFAULT)

8.3.2.4 Push Pull Output Pin (SDO)

図 48 shows the structure of push-pull pin, SDO.

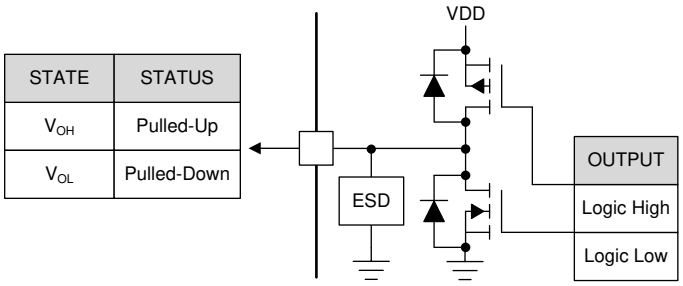


図 48. Push Pull Output Pin (SDO) Structure

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8.3.3 Protection Circuits

The DRV89xx-Q1 device is fully protected against undervoltage, overcurrent, and over-temperature events.

8.3.3.1 VM Supply Undervoltage Lockout (UVLO)

If at any time the input supply voltage on the VM pin falls below the V_{UVLO} threshold, all of the half-bridges are disabled, the charge pump is disabled, and the nFAULT pin is driven low as shown in 図 49. The UVLO bit is also latched high in the IC status (IC_STAT) register. Normal operation resumes (driver operation and the nFAULT pin is released) when the VM undervoltage condition is removed. The UVLO bit remains set until cleared through the CLR_FLT bit.

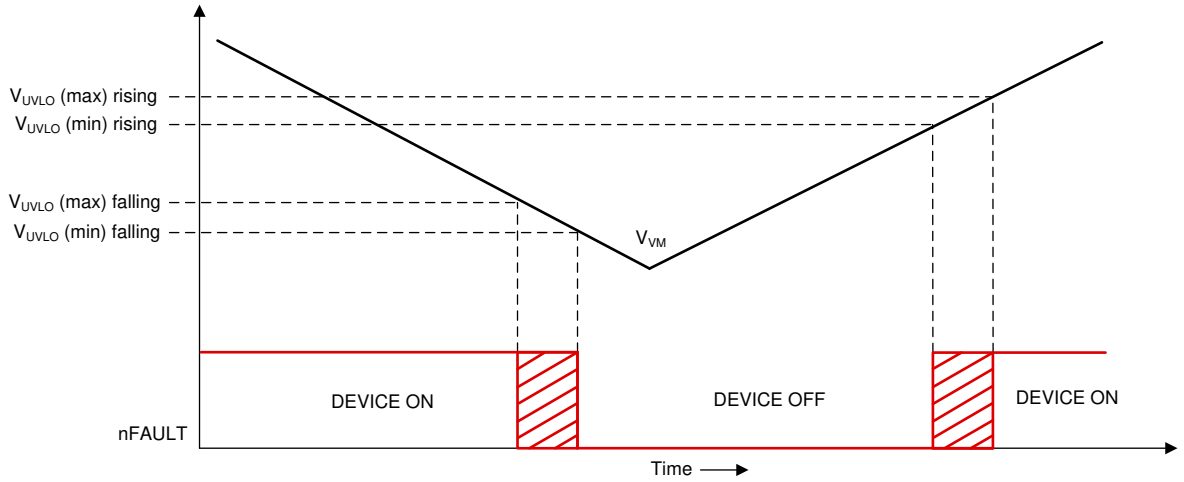


図 49. VM UVLO Operation

8.3.3.2 VM Supply Overvoltage Protection (OVP)

If at any time the input supply voltage on the VM pin rises above the V_{OVP} threshold, all of the half-bridges are disabled, the charge pump is disabled, and the nFAULT pin is driven low as shown in 図 50. The OVP bit is also latched high in the IC status (IC_STAT) register. Normal operation resumes (driver operation and the nFAULT pin is released) when the VM overvoltage condition is removed. The OVP bit remains set until cleared through the CLR_FLT bit.

An extended overvoltage operation is also supported in this device for higher over-voltage range up to 32-V. This operation is enabled by setting the EXT_OVP bit in the configuration (CONFIG_CTRL) register.

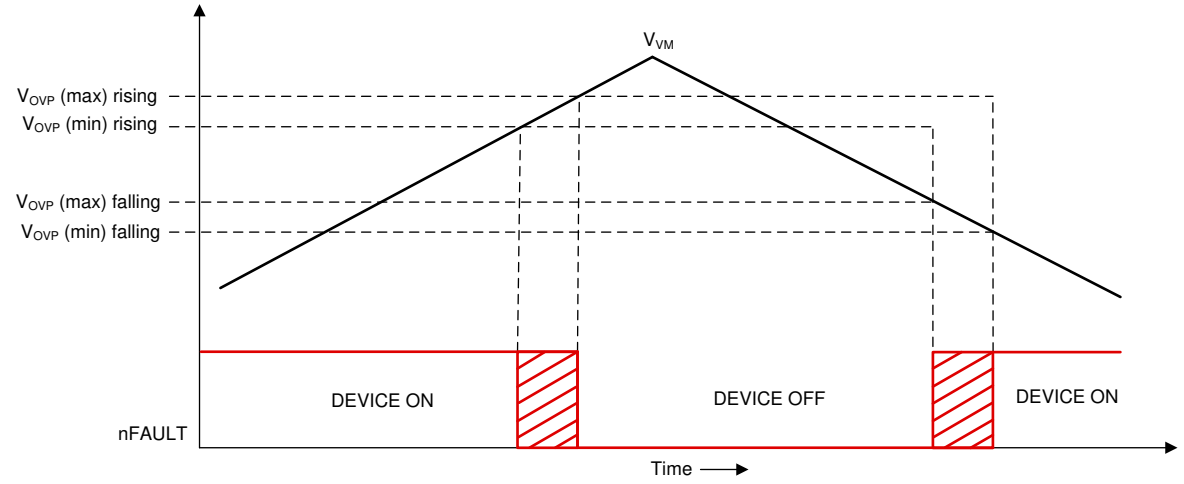


図 50. Over Voltage Protection

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8.3.3.3 Logic Supply Power on Reset (POR)

If at any time the input logic supply voltage on the VDD pin falls below the V_{POR} threshold or the nSLEEP pin is toggled (high to low), all of the half-bridges are disabled and the charge pump is disabled, as shown in 図 51. Normal operation resumes (driver operation) when the VDD undervoltage condition is removed or the nSLEEP pin is latched high. The NPOR bit is reset and latched low in the IC status (IC_STAT) register once the device presumes VDD. The NPOR bit remains in reset condition until cleared through the CLR_FLT bit.

If the device has successfully waked up, then the NPOR bit is automatically latched high once the CLR_FLT command is issued.

注

NPOR is not reported to nFAULT pin.

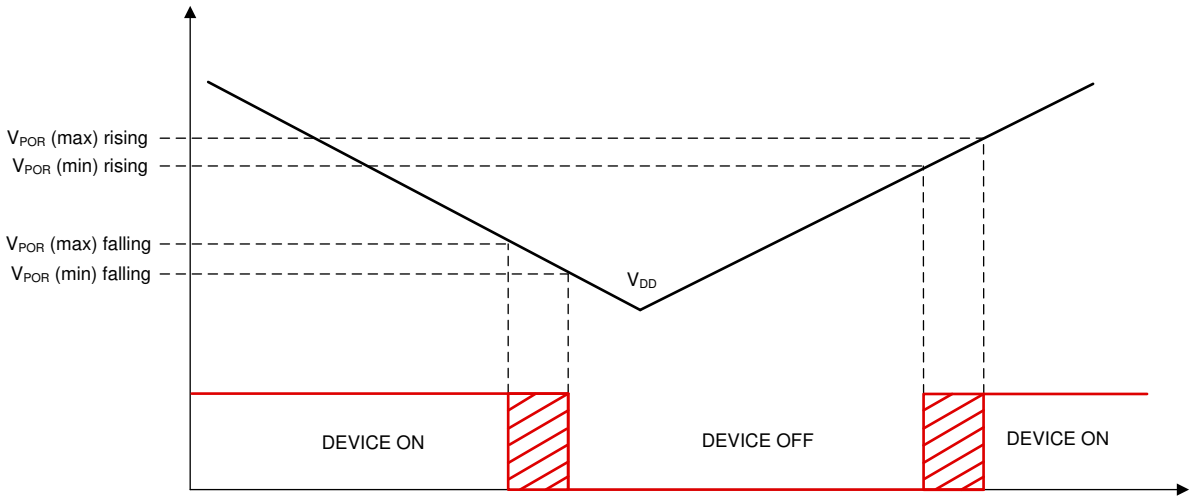


図 51. VDD UVLO Operation

8.3.3.4 Overcurrent Protection (OCP)

A current-limit circuit on each MOSFET limits the current through the MOSFET by removing the gate drive signal. If this current limit stay active for longer than the t_{OCP} deglitch time, the high-side and the low-side FETs in the corresponding half bridge are disabled and the nFAULT pin is driven low. The OCP bit in the IC status (IC_STAT) register and corresponding bit in overcurrent protection status register (OCP_STAT_X) register is latched high. The charge pump remains active during this condition. The OCP bit in the IC status (IC_STAT) register and corresponding bits (HBX_HS_OCP / HBX_LS_OCP) in overcurrent protection status register (OCP_STAT_X) register remains set until cleared through the CLR_FLT bit.

User also has the programmability of disabling the OCP fault on the nFAULT pin by setting the OCP_REP bit in the CONFIG_CTRL register.

The device also provides two slew-rate options for the device turn-off during an OCP event which can be programmed via the PL_MODE_EN bits in OLD_CTRL_2 register. The default option (PL_MODE_EN = 00b) is the faster slew rate option (typical around 1µs) which can be used for the single bridge operation. The slower option (PL_MODE_EN = 01b) provides a slower slew rate (half-bridge slew rate, HBX_SR) which can be used for the higher current applications in device parallel mode operation.

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表 6. Overcurrent Protection

Drive Current	BRIDGE CONFIGURATION	REGISTER SETTINGS	BRIDGE STATE	nFAULT PIN		BITS AFFECTED	RECOVERY
				OCP_REP = 0	OCP_REP = 1		
$I_{LOAD} < I_{OCP}$	OUT1 High-Side ON	HB1_HS_EN = 1	ENABLED	HIGH	HIGH	N/A	N/A
	OUT2 Low-Side ON	HB1_LS_EN = 1	ENABLED	HIGH	HIGH		
$I_{LOAD} < I_{OCP}$	Full Bridge (OUT1/2) Forward Direction	HB1_HS_EN = 1 HB2_LS_EN = 1	ENABLED	HIGH	HIGH		
	Full Bridge (OUT1/2) Reverse Direction	HB1_LS_EN = 1 HB2_HS_EN = 1	ENABLED	HIGH	HIGH		
I_{SHORT} or I_{LOAD} > I_{OCP}	OUT1 High-Side ON OUT1 Short to GND	HB1_HS_EN = 1	Hi-Z	LOW	HIGH	OCP = 1 (IC_STAT) HB1_HS_OCP = 1	OCP Condition Removed CLR_FLT = 1
	OUT1 Low-Side ON OUT1 Short to VM	HB1_LS_EN = 1	Hi-Z	LOW	HIGH	OCP = 1 (IC_STAT) HB1_LS_OCP = 1	
I_{SHORT} or I_{LOAD} > I_{OCP}	Full Bridge (OUT1/2) Forward Direction OUT1 / OUT2 Short	HB1_HS_EN = 1 HB2_LS_EN = 1	Hi-Z	LOW	HIGH	OCP = 1 (IC_STAT) HB1_HS_OCP = 1 or HB2_LS_OCP = 1 (1)	
	Full Bridge (OUT1/2) Reverse Direction OUT1 / OUT2 Short	HB1_LS_EN = 1 HB2_HS_EN = 1	Hi-Z	LOW	HIGH	OCP = 1 (IC_STAT) HB1_LS_OCP = 1 or HB2_HS_OCP = 1 (2)	

(1) Either of the HB1_HS_OCP or HB2_LS_OCP will set depending upon which half-bridge OCP trigger first.
(2) Either of the HB1_LS_OCP or HB2_HS_OCP will set depending upon which half-bridge OCP trigger first.

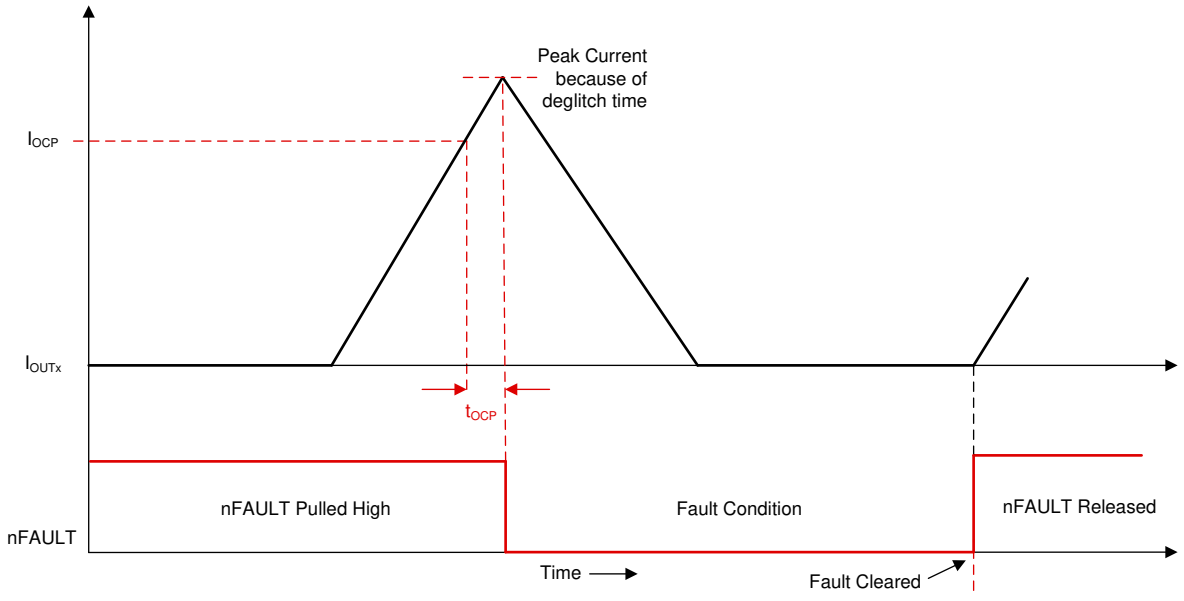


図 52. Over Current Protection

8.3.3.5 Open-load detection (OLD)

The DRV89XX-Q1 devices implement multiple open-load detection schemes to allow the controller to determine if a load is connected to the OUTX terminals. The OLD schemes available in DRV89XX-Q1 are listed below. 表 7 summarizes the use-cases for each OLD scheme.

- Active OLD
- Low-Current Active OLD
- Negative-Current Active OLD
- Passive OLD (only available in DRV8908-Q1, DRV8906-Q1 and DRV8904-Q1)

表 7. Summary of OLD features

	PASSIVE OLD	ACTIVE OLD	LOW-CURRENT ACTIVE OLD	NEGATIVE-CURRENT ACTIVE OLD
Part numbers	DRV8908/06/04-Q1	DRV8912/10/08/06/04-Q1		
When is it used	Detects open-load condition prior to enabling the outputs	Detects the open-load condition while driving a load	Detects the open-load condition while driving a load with small operating current	Detects the open-load condition during current re-circulation (on high-side or low-side) when synchronous rectification is enabled for both half-bridge and full-bridge configurations
State of OUTx for valid OLD	Hi-Z (outputs disabled)	H/L	L	H/L
OLD Trigger Condition	$V_{OLx_HS(+)} > V_{OLx_HS}$ or $V_{OLx_LS(-)} < V_{OLx_LS}$	$I_{OUTX} < I_{OLD}$	$I_{OUTX} < I_{OLD_LOW}$	$I_{OUTX} > I_{OLD_NEG}$
Tradeoffs	Passive OLD sequence is not enabled if any other fault other than OCP/OLD is present.	A false flag can occur during current re-circulation if synchronous rectification is ON. Enabling Negative-current OLD will solve this. A false flag can also occur if the operating current for the load is small (below I_{OLD} threshold). See Low-current OLD for solution.	Only applicable for the current flowing in the low-side FETs. The I_{OCP} for the low-side FET is also reduced by 11 times. The $R_{DS(ON)}$ of the low-side FET will increase by 11 times, hence the thermal performance has to be monitored.	Only functional during current re-circulation, however it works in conjunction with active OLD. This feature is not needed if synchronous rectification is disabled.
Can be used with other OLD schemes	No	Negative-current OLD and low-current OLD	Active OLD and negative-current OLD	Active OLD and low-current OLD

8.3.3.5.1 Active OLD

Active OLD can identify an open-load condition on the OUTX pins while driving a load. As shown in 図 53, the DRV89xx identifies an open-load fault condition when the current through the MOSFET (I_{OUTX}) is lower than the open-load current threshold (I_{OLD}) for longer than the open-load deglitch time (t_{OLD}). At that point the device takes the following actions.

- OLD bit in the IC status (IC_STAT) register sets to 1
- HBX_HS_OLD or HBX_LS_OLD bit in the open-load status register (OLD_STAT_X) sets to 1 (depending if the fault is on the high-side MOSFET or low-side MOSFET, respectively).
- nFAULT pin is drives low to indicate a fault to the controller.

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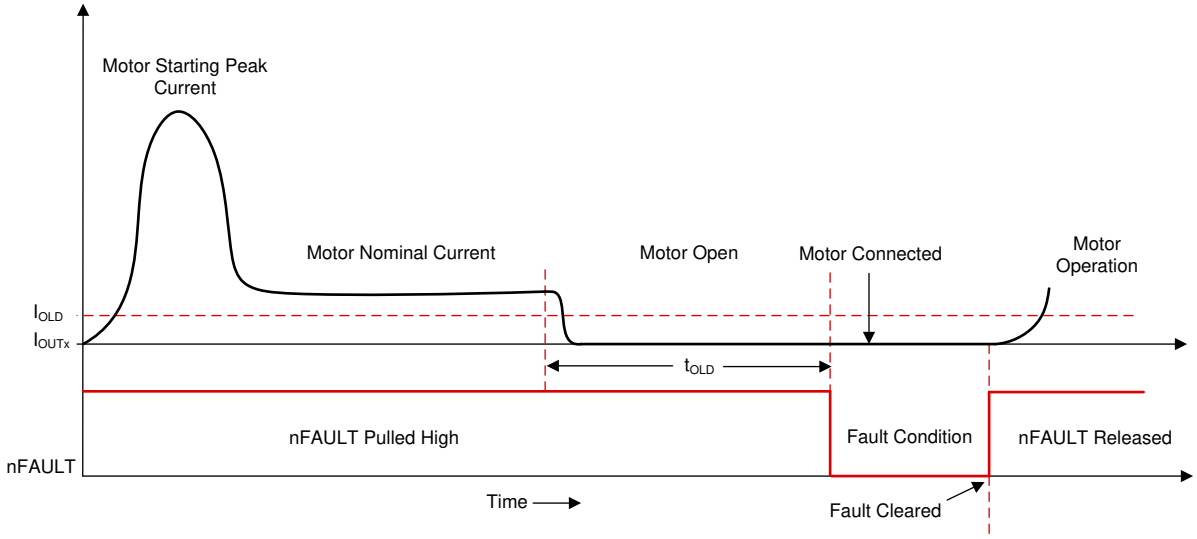


図 53. Active open-load detection

Normal operation resumes (driver operation resumes, the nFAULT pin goes high, OLD bit is reset to 0) when the open-load condition is removed (the user reconnects the load to the OUTX connection) and the controller writes the CLR_FLT bit to 1.

注

After the open-load fault condition is removed, the nFAULT pin will be driven high and the fault status are removed when,

- CLR_FLT command is issued after deglitch time (t_{OLD}) while OUTX is set high.
- CLR_FLT command is issued after OUTX is set to Hi-Z.
- CLR_FLT command is issued after HBX_OLD_DIS bit is set.

By default, OLD on the DRV89xx-Q1 devices is enabled. The OLD control registers (OLD_CTRL_1 and OLD_CTRL_2) allow the user to disable OLD on the OUTX pins with the HBX_OLD_DIS bits. The OLD_OP bit in the OLD_CTRL_2 register determines the response of the device to an active OLD fault. If OLD_OP = 0, the OUTX pins go to the Hi-Z state to stop driving the outputs. If OLD_OP = 1, the OUTX pins stay in their previous state and do not react to the OLD fault unless the user takes action. Similarly, the OLD_REP bit determines if the OLD fault will report on the nFAULT pin or only in the IC_STAT register. 表 8 summarizes the open-load detection feature and conditions.

注

By default the OLD feature is enabled, the outputs disable (go Hi-Z) when the OLD flags, and the nFAULT pin will report the OLD.

表 8. OLD Configuration

LOAD / OPEN	REGISTER SETTINGS	OLD_OP	OLD_REP	OUT1	OUT2	nFAULT	BITS EFFECTED	RECOVERY
Half-Bridge Load Connected	HB1_HS_EN = 1	X	X	H	X	HIGH	N/A	N/A
	HB1_LS_EN = 1	X	X	L	X	HIGH		
Full-Bridge Load Connected	HB1_HS_EN = 1 HB2_LS_EN = 1	X	X	H	L	HIGH		
	HB1_LS_EN = 1 HB2_HS_EN = 1	X	X	L	H	HIGH		

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表 8. OLD Configuration (continued)

LOAD / OPEN	REGISTER SETTINGS	OLD_OP	OLD_REP	OUT1	OUT2	nFAULT	BITS EFFECTED	RECOVERY
Half-Bridge Open	HB1_HS_EN = 1	0	0	Hi-Z	X	LOW	OLD = 1 (IC_STAT) HB1_HS_OLD = 1	OLD Condition Removed CLR_FLT = 1
		0	1	Hi-Z	X	HIGH		
		1	0	H	X	LOW		
		1	1	H	X	HIGH		
	HB1_LS_EN = 1	0	0	Hi-Z	X	LOW	OLD = 1 (IC_STAT) HB1_LS_OLD = 1	
		0	1	Hi-Z	X	HIGH		
		1	0	L	X	LOW		
		1	1	L	X	HIGH		
Full-Bridge Open	HB1_HS_EN = 1 HB2_LS_EN = 1	0	0	Hi-Z	Hi-Z	LOW	OLD = 1 (IC_STAT) HB1_HS_OLD = 1 or HB2_LS_OLD = 1 (1)	
		0	1	Hi-Z	Hi-Z	HIGH		
		1	0	H	L	LOW		
		1	1	H	L	HIGH		
	HB1_LS_EN = 1 HB2_HS_EN = 1	0	0	Hi-Z	Hi-Z	LOW	OLD = 1 (IC_STAT) HB1_LS_OLD = 1 or HB2_HS_OLD = 1 (2)	
		0	1	Hi-Z	Hi-Z	HIGH		
		1	0	L	H	LOW		
		1	1	L	H	HIGH		

(1) Either of the HB1_HS_OLD or HB2_LS_OLD will set depending upon which half-bridge OLD triggers first.
(2) Either of the HB1_LS_OLD or HB2_HS_OLD will set depending upon which half-bridge OLD triggers first.

8.3.3.5.1.1 Negative-current OLD

The DRV89XX-Q1 device also includes a negative-current OLD mode. The negative current can flow either through the body diode of high-side FET or the FET itself depending on whether or not the channel is configured for synchronous rectification. 図 54 shows the current re-circulation through the body diode of the high-side FET when the synchronous rectification mode is OFF (i.e. HB2_FW = 0). In this case, the active OLD will not falsely report an open-load condition since the OLD circuit only enables when the FET is ON. Negative-current OLD will also work during re-circulation through the low-side FETs.

図 55 shows the negative current re-circulation through the high-side FET when synchronous rectification is ON (i.e. HB2_FW = 1). In this scenario, for default operation (OLD_NEG_EN = 0), the device can show a false open-load fault since the FET current is lower than the positive OLD threshold. However, when negative-current OLD mode is enabled, the device will only flag an open-load fault if $I_{OUTX} < I_{OLD_NEG}$. This mode is enabled by setting the OLD_NEG_EN bit in OLD_CTRL3 register.

図 56 shows the waveforms of false open-load detection when the negative-current OLD setting is disabled (OLD_NEG_EN = 0). As shown in this figure, the high-side FET of the OUT1 channel is always switched ON and the low-side and high-side FET of the OUT2 channel are operating in complimentary way (i.e. synchronous rectification mode is enabled). In synchronous rectification, the current flows in negative direction from OUT2 to VM (i.e. FET Source to Drain) during the high-side FET conduction. Initially, for the first PWM cycle, the OLD mode is disabled to show the currents in different FETs during the motor operation. When OLD is enabled in second PWM cycle, then the device registers a false open-load detect during the high-side FET conduction as shown in 図 56. The nFAULT pin is pulled low and both high-side and low-side FET of OUT2 channels are disabled. The body diode of the high side FET (OUT2) conducts to complete the motor current path.

This false detection of open load is eliminated by enabling the negative-current OLD setting (OLD_NEG_EN = 1). As shown in 図 57, the negative OLD current setting (I_{OLD_NEG}) is enabled for the high-side FET of OUT2 channel. This setting allows the negative current path (from source to drain) in high-side FET. The nFAULT pin is latched high and OUT2 channel is not disabled when OLD is enabled in second PWM cycle.

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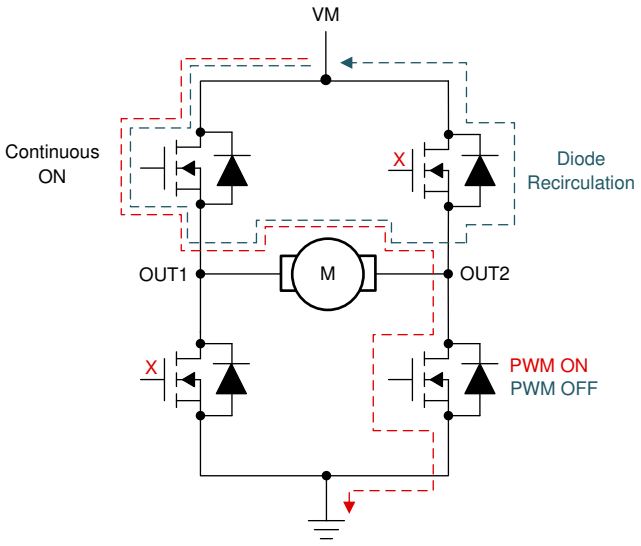


図 54. Negative Current Flow in OUT2 by Body Diode of High-Side FET

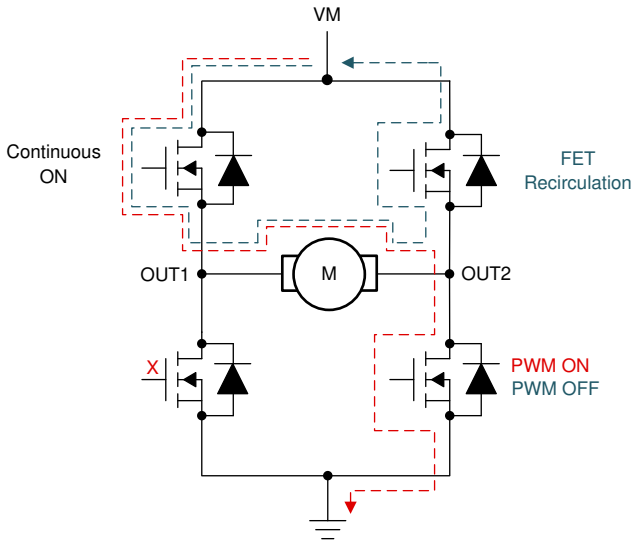


図 55. Negative Current Flow in High-Side FET of OUT2 Channel

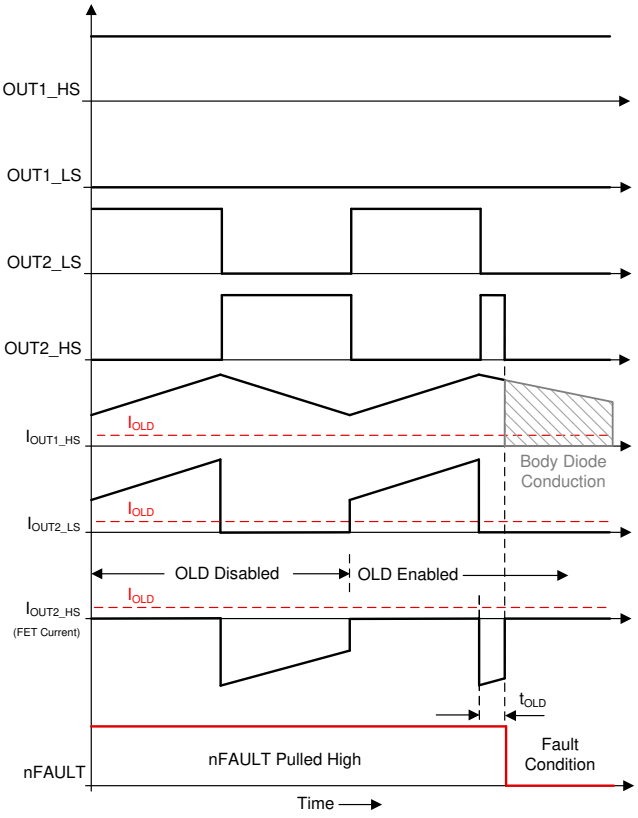


図 56. Waveforms Showing False OLD With Negative-Current OLD Disabled

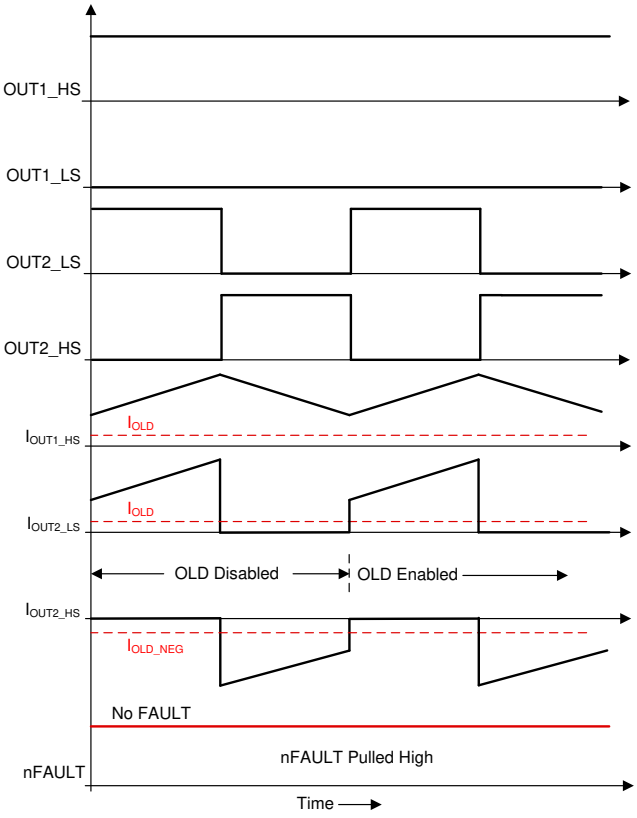


図 57. Waveforms Showing Operation with Negative-Current OLD Enabled

8.3.3.5.2 Low-current OLD

Low-current open-load detection is another type of active open-load detection in the DRV89XX-Q1 devices. In low-current open-load detection, the current detection threshold is around 10x lower than the active open-load detection scheme. This feature gives the user flexibility to detect a valid open-load condition when driving loads that require low current.

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As shown in 図 58, if the low-side MOSFET is in operating condition (switched-ON) and the current flowing in the particular MOSFET is lower than the low-current active open-load current threshold (I_{OLD_LOW}) for at least open-load detection deglitch time (t_{OLD}), then an open-load condition is detected. The OLD bit in the IC status (IC_STAT) register is set, the HBX_LS_OLD bit in the open-load status register (OLD_STAT_X) is set and nFAULT pin is driven low during an open-load detect. Normal operation resumes (driver operation and the nFAULT pin is released) when the open-load condition is removed and CLR_FLT command is issued. The OLD bit remains set until cleared through the CLR_FLT bit.

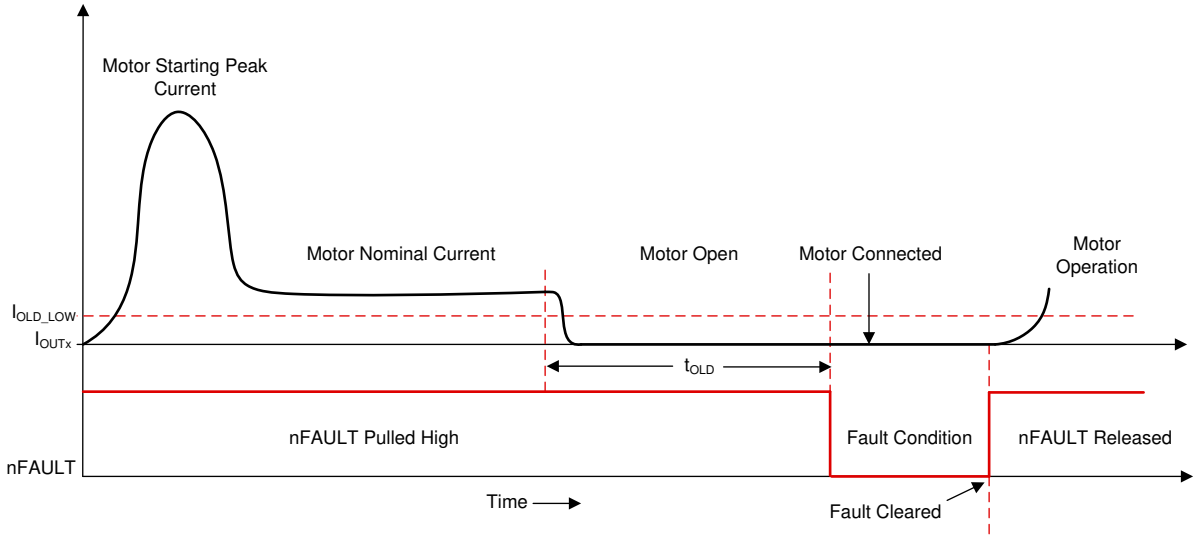


図 58. Low-Current OLD

注

The low-current OLD has following limitations

- This feature is only applicable for the current flowing in low-side FET.
- Once this mode is enabled the corresponding over-current threshold for the low-side FET is also reduced by 11 times (~120 mA min.).
- The $R_{DS(on)}$ of the low side FET will increase by 11 times (~7.5 Ω typical), hence the thermal performance has to be monitored. However, for the lower current the thermal dissipation is limited.

図 59 shows the flowchart for implementing the low-current active OLD in continuous mode of operation. Following are the steps to configure and detect the low-current active OLD in the DRV89XX-Q1 device.

1. Enable OLD by setting the OLD_OP bit in OLD_CTRL_2 register. This setting will ensure that the OUTX outputs continue to operate when and OLD fault occurs.
2. Enable the full-bridge operation by setting the individual HBX_HS_EN/HBX_LS_EN bits in operation control (OP_CTRL_1, OP_CTRL_2 and OP_CTRL_3) registers.
3. Check for the nFAULT pin status and the OLD fault in the IC_STAT register.
4. If the nFAULT pin is low and the OLD fault is high, then check for the individual HBX_HS_OLD/HBX_LS_OLD bits in OLD status (OLD_STAT_1, OLD_STAT_2 and OLD_STAT_3) registers.
5. Disable OLD using the HBX_OLD_DIS bits for the OUTX pins acting as high-side drivers.
6. Enable the low-current OLD mode for the half-bridge which low-side is operating by using the HBX_LOLD_EN bit in OLD control (OLD_CTRL_3 and OLD_CTRL_4) registers. This will also disable the high-side OLD for the particular half-bridge.
7. Wait for the open-load deglitch time (t_{OLD}).
8. Issue the clear fault command (CLR_FLT) to release the nFAULT pin and clear the OLD bits if low-current OLD is not detected.

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9. If the OLD bit is high and the nFAULT pin is not released (low), then low-current OLD fault is detected.

注

The low-current OLD is applicable only for low-side FETs. The user has to enable the low-current OLD mode for the corresponding low-side FET.

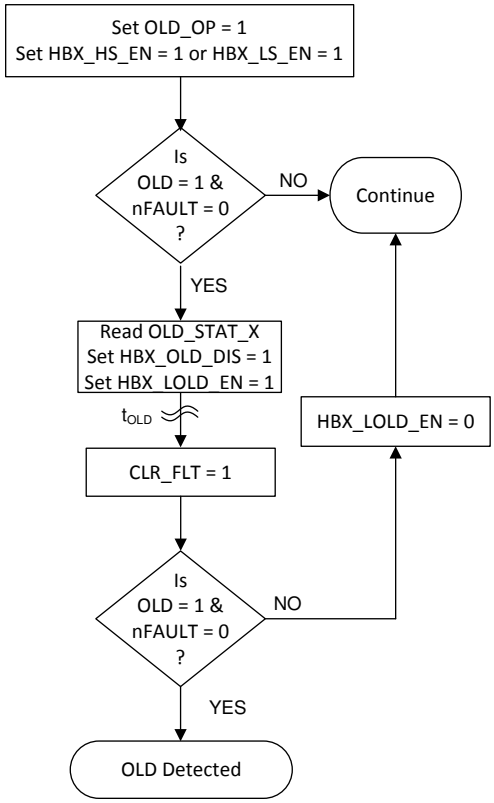


図 59. Flowchart for Enabling Low-Current OLD (Continuous Mode)

8.3.3.5.3 Passive OLD

In passive OLD, the detection of open load is carried before the driver is turned on. The state of all FETs remains in Hi-Z state, while a minimal amount of current flows through motor for short amount of time to test the motor connection. The diagnostic current is very small to avoid causing the motor rotation.

図 60 shows the circuit implementation of the passive OLD. As shown in this figure, a constant current source pulls the OUT1 pin to the AVDD (internal) fixed voltage which allows current flow from OUT1 to OUT2 terminal. The current drawn is completely dependent on the motor resistance between OUT1 and OUT2 and limited by the internal current sourcing (I_{OL_PU}) and sinking (I_{OL_PD}) capability of the passive OLD circuitry. Depending on this current and the comparator threshold voltage (V_{OL_HS} and V_{OL_LS}), the comparator output OL1_HS and OL2_LS are either set or reset which determines the open-load status. When an open load is detected, the OLD bit in the IC status (IC_STAT) register is set, the HBX_LS_OLD bit in the open-load status register (OLD_STAT_X) is set and nFAULT pin is driven low. The OLD bit remains set until cleared through the CLR_FLT bit. This implementation is applicable for any half-bridges.

注

Passive OLD sequence is not disabled by the HBX_OLD_DIS bits.

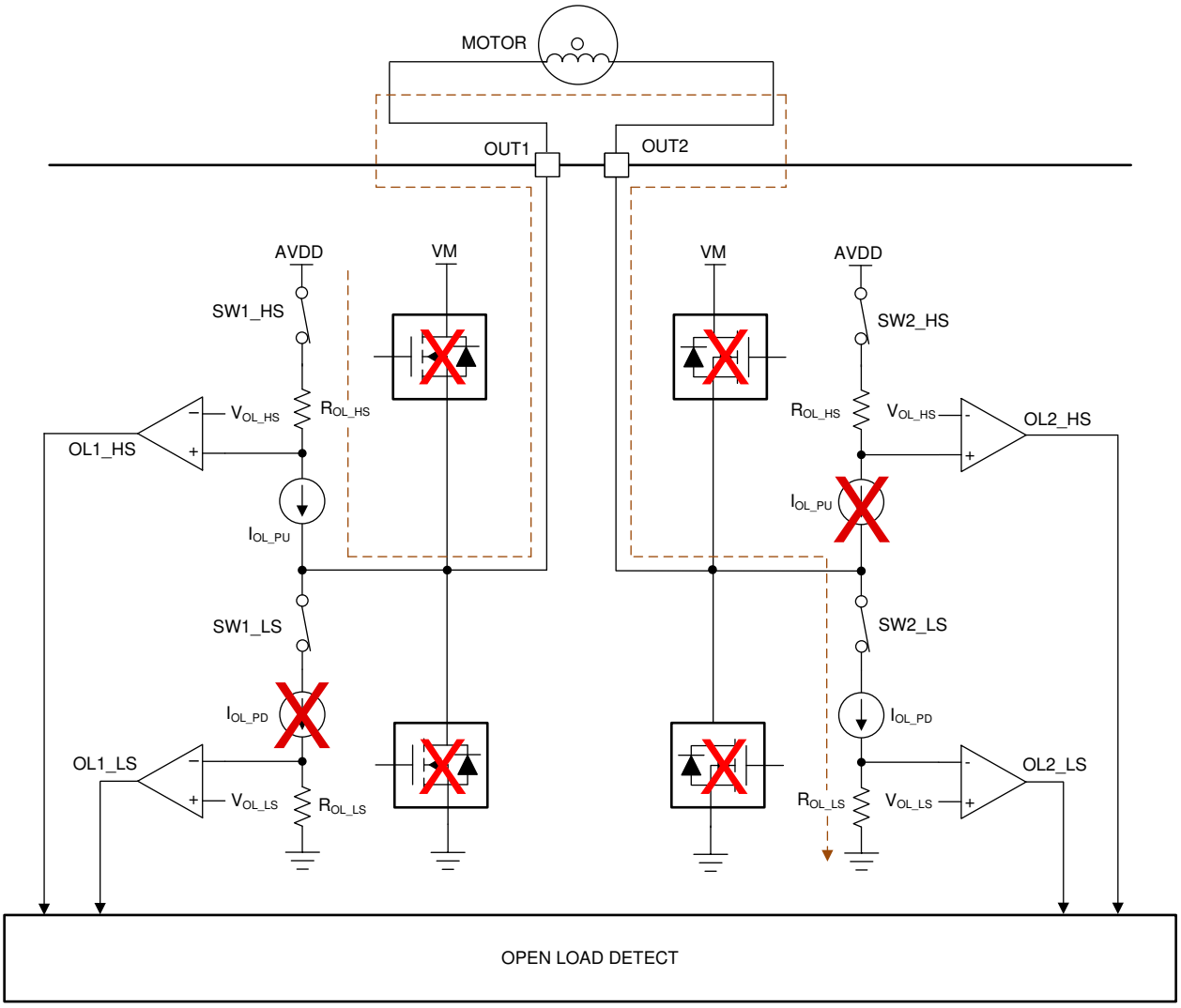


図 60. Passive OLD Circuit

Following are the steps to configure and detect the passive OLD in the DRV89XX-Q1 device.

1. Enable the passive OLD mode for the individual half-bridges which is to be diagnosed using the Half-bridge passive OLD enable bits (HBX_POLD_EN) in OLD_CTRL_5 register.
2. Configure the half-bridge operation control bits (HBX_HS_EN/HBX_LS_EN) in operation control register (OP_CTRL_X) to determine the high-side and low-side OLD check. Note that these bits are now used for the passive OLD configuration. If anytime, the HBX_POLD_EN is reset then the bridge starts operating.
3. Enable the passive OLD using the Passive OLD Enable bit (POLD_EN) in CONFIG_CTRL register. Setting the POLD_EN bit enables the passive OLD detection circuit on all OUTx pin for which the corresponding HBX_HS_EN or HBX_LS_EN are set to 1.
4. Wait for the passive OLD time as determined by the user.
5. After the completion of passive OLD time, disable the passive OLD enable bit (POLD_EN).
6. Monitor the nFAULT pin / OLD bit in Status register (IC_STAT) and the HBX_HS_OLD/HBX_LS_OLD bit in the OLD status registers (OLD_STAT_X) for any open-load detection.
7. Restart the sequence for other half-bridges / full-bridges.

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During normal driving, HBX_HS_EN and HBX_LS_EN bits control the state of OUTX. However, when POLD_EN and HBX_POLD_EN are 1, the OUTX channel is disabled, and HBX_HS_EN and HBX_LS_EN control SWX_HS and SWX_LS used for passive OLD (see schematic representation in 図 60). 表 9 shows the truth table for this operation.

表 9. Truth Table for Passive OLD

HBX_POLD_EN	HBX_HS_EN	HBX_LS_EN	OUTX	SWX_HS	SWX_LS	OPEN LOAD SEQUENCE
0	X	X	Follows HBX_HS_EN and HBX_LS_EN	Open	Open	Passive OLD for the channel is disabled and HBX_HS_EN/HBX_LS_EN set output OUTx state
1	0	0	Z	Open	Open	Off state - no passive OLD
1	0	1	Z	Open	Closed	Valid passive OLD for VM-connected load
1	1	0	Z	Closed	Open	Valid passive OLD for GND-connected load
1	1	1	Z	Open	Open	Invalid state

注

The OLD_REP bit works in a similar way as for the active OLD. The OLD_OP bit is not applicable for passive OLD operation since the outputs are already disabled.

注

Passive OLD sequence is not enabled if any other fault (other than OCP/OLD) is present.

表 10 shows an example for configuring passive OLD for various loads. The HBX_VM_POLD bits can be enabled for any loads that connect directly to VM. In cases where VM is low, the passive OLD current may need to be larger so passive OLD does not falsely indicate an open load. Setting HBX_VM_POLD = 1 chooses a smaller R_{OL} so more current flows and the device can properly detect an open load.

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表 10. Passive OLD Configurations

CONNECTION	HB1_VM_POLD	HB2_VM_POLD	HB1_HS_EN	HB1_LS_EN	HB2_HS_EN	HB2_LS_EN	OPEN-LOAD DETECTION
Full Bridge Operation (Motor Connected Between OUT1 and OUT2)	0	0	1	0	0	1	Detection based on resistance threshold (Forward Connection)
	0	0	0	1	1	0	Detection based on resistance threshold (Reverse Connection)
	0	0	1	0	1	0	Invalid case (both high-side OLD circuitry operating)
	0	0	0	1	0	1	Invalid case (both low-side OLD circuitry operating)
Half Bridge Operation (Load Connected Between OUT1/2 and VM)	1	X	0	1	0	0	Detection only for OUT1 channel based on resistance threshold
	X	1	0	0	0	1	Detection only for OUT2 channel based on resistance threshold
	1	1	0	1	0	1	Detection for both outputs based on resistance threshold
	X	X	1	0	0	0	Invalid case (OUT1 high-side OLD circuitry is operating for VM connected load)
	X	X	0	0	1	0	Invalid case (OUT2 high-side OLD circuitry is operating for VM connected load)
	X	X	1	0	1	0	Invalid case (both high-side OLD circuitry is operating for VM connected load)
Half Bridge Operation (Load Connected Between OUT1/2 and GND)	0	0	1	0	0	0	Detection only for OUT1 channel based on resistance threshold
	0	0	0	0	1	0	Detection only for OUT2 channel based on resistance threshold
	0	0	1	0	1	0	Detection for both outputs based on resistance threshold
	0	0	0	1	0	0	Invalid case (OUT1 low-side OLD circuitry is operating for GND connected load)
	0	0	0	0	0	1	Invalid case (OUT2 low-side OLD circuitry is operating for GND connected load)
	0	0	0	1	0	1	Invalid case (both low-side OLD circuitry is operating for GND connected load)

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8.3.3.6 Thermal Warning (OTW)

If the die temperature exceeds the trip point of the thermal warning (T_{OTW}), the OTW bit is set in the IC status (IC_STAT) register. The reporting of OTW on the nFAULT pin can be enabled by setting the over-temperature warning reporting (OTW_REP) bit in the configuration control (CONFIG_CTRL) register. The device performs no additional action and continues to function. In this case, the nFAULT pin releases when the die temperature decreases below the hysteresis point of the thermal warning (T_{OTW_HYS}). The OTW bit remains set until cleared through the CLR_FLT bit and the die temperature is lower than thermal warning trip (T_{OTW}).

注

Over Temperature warning is not reported on nFAULT pin by default.

8.3.3.7 Thermal Shutdown (OTSD)

If the die temperature exceeds the trip point of the thermal shutdown limit (T_{OTSD}), all half-bridge drivers are disabled, the charge pump is shut down, and the nFAULT pin is driven low. In addition, the OTSD bit is latched high in IC status (IC_STAT) register. Normal operation resumes (driver operation and the nFAULT pin is released) when the overtemperature shutdown condition is removed and die temperature decreases below the hysteresis point of the thermal warning (T_{OTSD_HYS}). The OTSD bit remains latched high indicating that a thermal event occurred until a clear fault command is issued through the CLR_FLT bit. This protection feature cannot be disabled.

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8.4 Device Functional Modes

8.4.1 Sleep Mode (nSLEEP = 0)

The nSLEEP pin manages the state of the DRV89xx-Q1 device. When the nSLEEP pin is low, the device enters a low-power sleep mode. In sleep mode, all half-bridge drivers are disabled, the internal charge pump is disabled, the internal regulators are disabled, and the SPI bus is disabled. The t_{SLEEP} time must elapse after a falling edge on the nSLEEP pin before the device enters sleep mode. The device comes out of sleep mode automatically if the nSLEEP pin is pulled high. The t_{WAKE} time must elapse before the device is ready for inputs.

8.4.2 Operating Mode (nSLEEP = 1)

When the nSLEEP pin is high and $V_{VM} > V_{UVLO}$, the device enters operating mode. The t_{WAKE} time must elapse before the device is ready for inputs. In this mode the half bridge drivers, charge pump, internal regulators, and SPI bus are active. 表 11 summarizes the different operating modes of DRV89XX-Q1 device.

表 11. Functional Modes

MODE	CONDITION	HALF-BRIDGES	INTERNAL CIRCUITS
Operating	4.5-V < V_{VM} < 20-V (EXT_OVP = 0b) 4.5-V < V_{VM} < 32-V (EXT_OVP = 1b) nSLEEP Pin = High	Operating	Operating
Sleep	4.5-V < V_{VM} < 32-V nSLEEP Pin = Low	Disabled	Disabled
Fault	Any Fault Condition Met	Depends on Fault	Depends on Fault

8.4.3 Fault Mode

The DRV89XX-Q1 is protected against various faults as summarized in 表 12.

表 12. Fault Action and Response

FAULT	CONDITION	CONFIGURATION	REPORT	HALF-BRIDGE	LOGIC	RECOVERY
VM Undervoltage (UVLO)	$V_{VM} < V_{UVLO}$ (Max. 4.5-V)	—	nFAULT Pin IC_STAT Register	Hi-Z	Active	Automatic: $V_{VM} > V_{UVLO}$
VDD Undervoltage (UVLO)	$V_{VDD} < V_{POR}$ (Max 3-V)	—	IC_STAT Register	Hi-Z	Reset	Automatic: $V_{VDD} > V_{POR}$
VM Overvoltage (OVP)	$V_{VM} > V_{OVP}$ (Min. 20-V)	EXT_OVP = 0	nFAULT Pin IC_STAT Register	Hi-Z	Active	Automatic: $V_{VM} < V_{OVP}$
	$V_{VM} > V_{OVP}$ (Min. 32-V)	EXT_OVP = 1				
Over Current Protection (OCP)	$I_{OUT} > I_{OCP}$ (Min. 1.3-A)	OCP_REP = 0	IC_STAT Register	Hi-Z	Active	CLR_FLT = 1 & $I_{OUT} < I_{OCP}$
		OCP_REP = 1	nFAULT Pin IC_STAT Register	Hi-Z	Active	
Open-Load Detect (OLD)	$I_{OUT} < I_{OLD}$ (Max. 15-mA)	OLD_OP = 0 OLD_REP = 0	nFAULT Pin IC_STAT Register	Hi-Z	Active	CLR_FLT = 1 & $I_{MOTOR} > I_{OLD}$
		OLD_OP = 0 OLD_REP = 1	IC_STAT Register	Hi-Z	Active	
		OLD_OP = 1 OLD_REP = 0	nFAULT Pin IC_STAT Register	Operating	Active	
		OLD_OP = 1 OLD_REP = 1	IC_STAT Register	Operating	Active	
	$R_{LOAD} > R_{OLD}$ (Max. 100-kΩ)	OLD_REP = 0	nFAULT Pin IC_STAT Register	N/A	Active	CLR_FLT = 1 & OLD Sequenced & $R_{LOAD} < R_{OLD}$
		OLD_REP = 1	IC_STAT Register	N/A	Active	
Over-Temperature Warning (OTW)	$T_J > T_{OTW}$ (Min. 120°C)	OTW_REP = 0	IC_STAT Register	Operating	Active	No Action
		OTW_REP = 1	nFAULT Pin IC_STAT Register	Operating	Active	Automatic: $T_J < T_{OTW} - T_{OTW_HYS}$

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表 12. Fault Action and Response (continued)

FAULT	CONDITION	CONFIGURATION	REPORT	HALF-BRIDGE	LOGIC	RECOVERY
Over-Temperature Shutdown (OTSD)	$T_J > T_{OTSD}$ (Min. 150°C)	—	nFAULT Pin IC_STAT Register	Hi-Z	Active	Automatic: $T_J < T_{OTSD} – T_{OTSD_HYS}$

8.5 Programming

8.5.1 SPI

SPI bus is used to set device configurations, operating parameters, and read out diagnostic information on the DRV89xx-Q1 device. The SPI operates in slave mode and connects to a master controller. The SPI input data (SDI) word consists of a 16 bit word, with an 8 bit command and 8 bits of data. The SPI output data (SDO) word consists of 8 bit register data and the first 8 bits make up the Status Register with Fault Status indication. The data sequence between the MCU and the SPI slave driver is shown in 図 61.

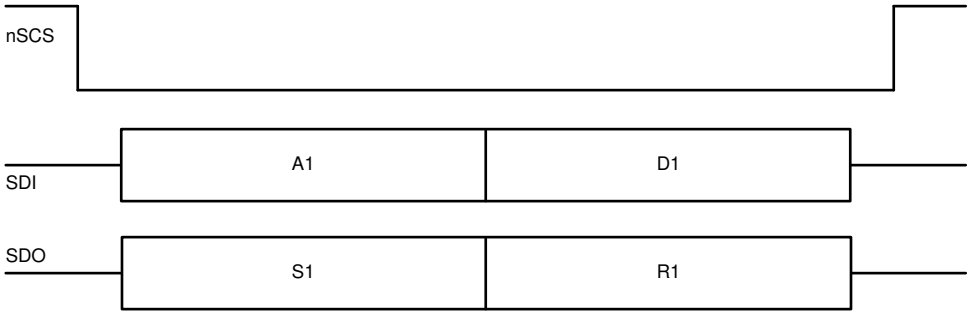


図 61. SPI Data Frame

A valid frame must meet the following conditions:

- The SCLK pin should be low when the nSCS pin transitions from high to low and from low to high.
- The nSCS pin should be pulled high for at least 400 ns between words.
- When the nSCS pin is pulled high, any signals at the SCLK and SDI pins are ignored and the SDO pin is placed in the Hi-Z state.
- Data is captured on the falling edge of SCLK and data is propagated on the rising edge of SCLK.
- The most significant bit (MSB) is shifted in and out first.
- A full 16 SCLK cycles must occur for transaction to be valid.
- If the data word sent to the SDI pin is less than or more than 16 bits, a frame error occurs and the data word is ignored.
- For a write command, the existing data in the register being written to is shifted out on the SDO pin following the 8 bit command data.

8.5.2 SPI Format

The SDI input data word is 16 bits long and consists of the following format:

- 1 read or write bit, W (bit B14)
- 6 address bits, A (bits B13 through B8)
- 8 data bits, D (bits B7 through B0)

The SDO output data word is 16 bits long and the first 8 bits makes up the IC status register. The report word is the content of the register being accessed.

For a write command (W0 = 0), the response word on the SDO pin is the data currently in the register being written to.

For a read command (W0 = 1), the response word is the data currently in the register being read.

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Programming (continued)

表 13. SDI Input Data Word Format

		R/W	Address						Data							
Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data	0	W0	A5	A4	A3	A2	A1	A0	D7	D6	D5	D4	D3	D2	D1	D0

表 14. SDO Output Data Word Format

	IC Status								Report							
Bit	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Data	1	1	OT	OLD	OCP	UVLO	OVP	NPOR	D7	D6	D5	D4	D3	D2	D1	D0

8.5.3 SPI Interface for Multiple Slaves

Multiple DRV89XX-Q1 devices can be connected to the master controller with and without the daisy chain. For connecting a 'n' number of DRV89XX-Q1 to a master controller without using a daisy chain, 'n' number of I/O resources from master controller has to be utilized for nSCS pins as shown 図 62. Whereas, if the daisy chain configuration is used, then a single nSCS line can be used for connecting multiple DRV89XX-Q1 devices as shown in 図 63.

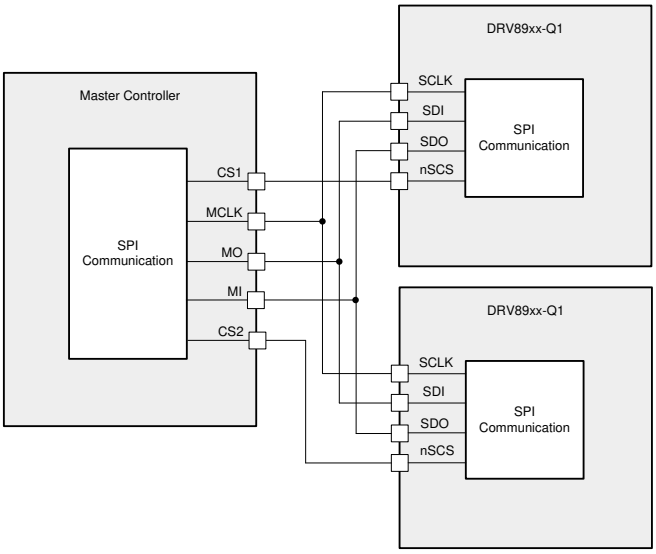


図 62. SPI Operation Without Daisy Chain

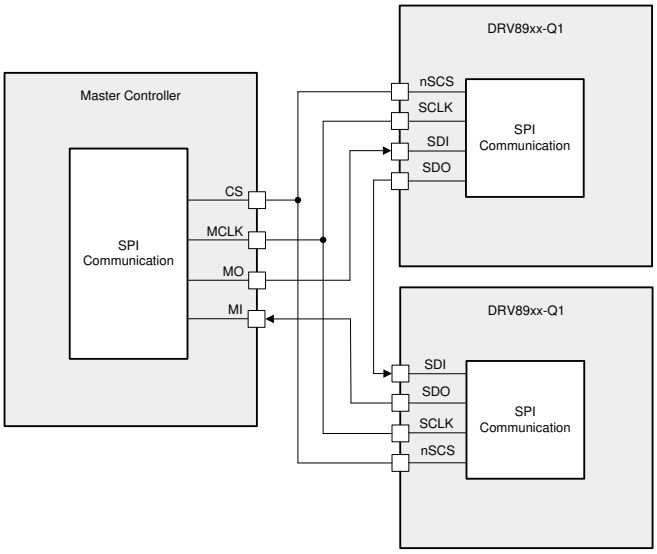


図 63. SPI Operation With Daisy Chain

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8.5.3.1 SPI Interface for Multiple Slaves in Daisy Chain

The DRV89XX-Q1 device can be connected in a daisy chain configuration to save GPIO ports when multiple devices are communicating to the same MCU. 図 64 shows the topology when 3 devices are connected in series with waveforms.

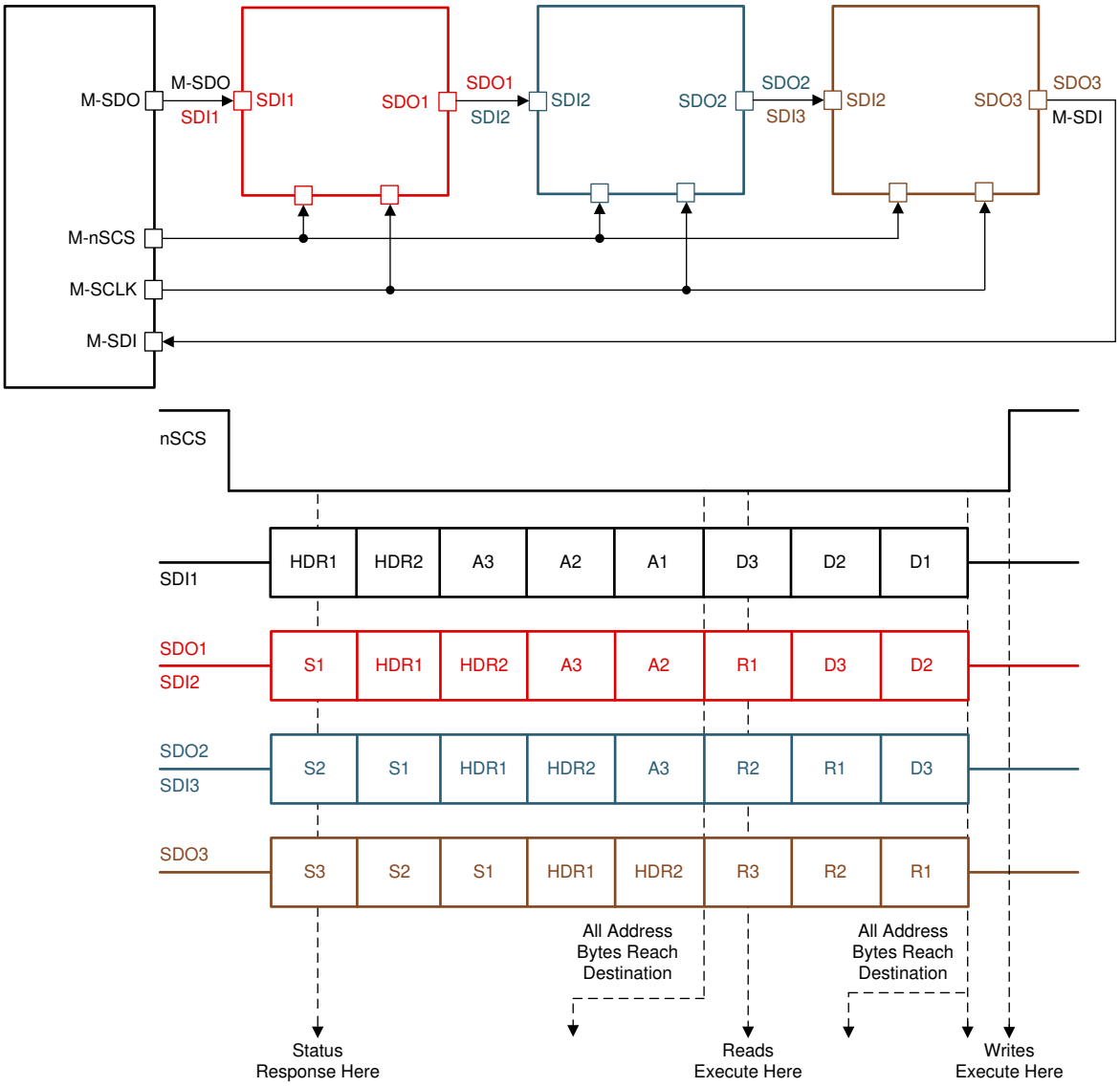


図 64. Daisy Chain SPI Operation

The first device in the chain shown above receives data from the master controller in the following format. See SDI1 in 図 64

- 2 bytes of Header
- 3 bytes of Address
- 3 bytes of Data

After the data has been transmitted through the chain, the master controller receives it in the following format. See SDO3 in 図 64

- 3 bytes of Status
- 2 bytes of Header (should be identical to the information controller sent)
- 3 bytes of Report

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The Header bytes contain information of the number of devices connected in the chain, and a global clear fault command that will clear the fault registers of all the devices on the rising edge of the chip select (nSCS) signal. N5 through N0 are 6 bits dedicated to show the number of devices in the chain as shown in 図 65. Up to 63 devices can be connected in series per daisy chain connection.

The 5 LSBs of the HDR2 register are don't care bits that can be used by the MCU to determine integrity of the daisy chain connection. Header bytes must start with 1 and 0 for the two MSBs.

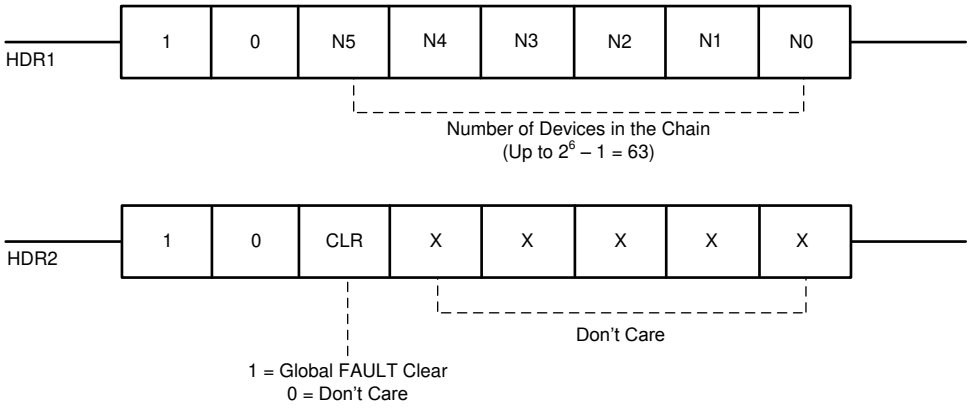


図 65. Header Bits

The Status byte provides information about the fault status register for each device in the daisy chain as shown in 図 66. That way the master controller does not have to initiate a read command to read the fault status from any particular device. This saves the controller additional read commands and makes the system more efficient to determine fault conditions flagged in a device.

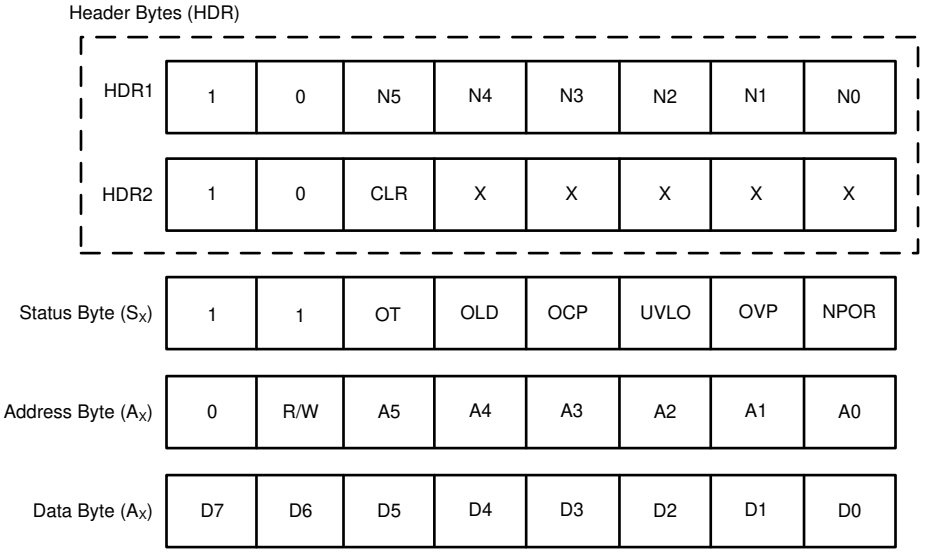


図 66. Daisy Chain Read Registers

When data passes through a device, it determines the position of itself in the chain by counting the number of Status bytes it receives following by the first Header byte. For example, in this 3 device configuration, device 2 in the chain will receive two Status bytes before receiving HDR1 byte, followed by HDR2 byte.

From the two Status bytes it knows that its position is second in the chain, and from HDR2 byte it knows how many devices are connected in the chain. That way it only loads the relevant address and data byte in its buffer and bypasses the other bits. This protocol allows for faster communication without adding latency to the system for up to 63 devices in the chain.

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The address and data bytes remain the same with respect to a single device connection. The Report bytes (R1 through R3), as shown in the figure above, is the content of the register being accessed.

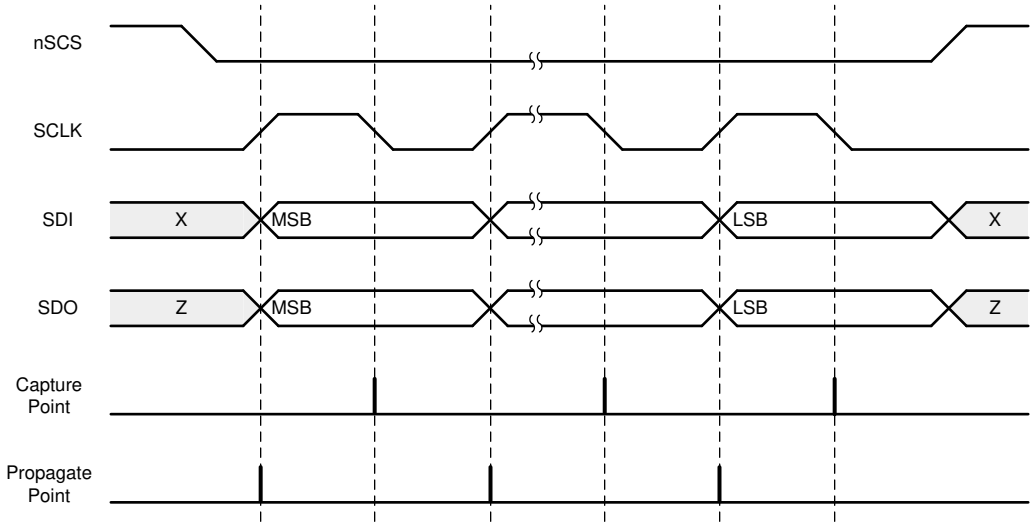


図 67. SPI Slave Timing Diagram

8.6 Register Map

This section contains the register maps and bit descriptions for all of the DRV89xx-Q1 devices. DRV8912-Q1 and DRV8910-Q1 Register Maps contains the register maps and register descriptions for DRV8912-Q1 and DRV8910-Q1 devices. DRV8908-Q1, DRV8906-Q1 and DRV8904-Q1 Register Maps contains the register maps and register descriptions for DRV8908-Q1, DRV8906-Q1, and DRV8904-Q1 devices. 表 15 summarizes the differences among the part numbers in the DRV89xx-Q1 family.

表 15. Summary of DRV89xx-Q1 Device Family

DEVICE	NUMBER OF HALF-BRIDGES	NUMBER OF PWM GENERATORS	OPEN-LOAD DETECTION SCHEMES	LINK TO REGISTER MAP
DRV8912-Q1	12	4	Active OLD, Low-Current Active OLD, Negative-Current Active OLD	表 17
DRV8910-Q1	10	4		表 18
DRV8908-Q1	8	8	Passive OLD, Active OLD, Low-Current Active OLD, Negative-Current Active OLD	表 50
DRV8906-Q1	6	8		表 51
DRV8904-Q1	4	8		表 52

Complex bit access types are encoded to fit into small table cells. 表 16 shows the codes that are used for access types in this section.

表 16. Control Registers Access Type Codes

Access Type	Code	Description
Read Type		
R	R	Read
Write Type		
W	W	Write
Reset or Default Value		
-n		Value after reset or the default value

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8.6.1 DRV8912-Q1 and DRV8910-Q1 Register Maps

表 17. DRV8912-Q1 Register Map

Name	7	6	5	4	3	2	1	0	Type	Address
IC_STAT	Reserved	OTSD	OTW	OLD	OCP	UVLO	OVP	NPOR	R	00h
OCP_STAT_1	HB4_HS_OCP	HB4_LS_OCP	HB3_HS_OCP	HB3_LS_OCP	HB2_HS_OCP	HB2_LS_OCP	HB1_HS_OCP	HB1_LS_OCP	R	01h
OCP_STAT_2	HB8_HS_OCP	HB8_LS_OCP	HB7_HS_OCP	HB7_LS_OCP	HB6_HS_OCP	HB6_LS_OCP	HB5_HS_OCP	HB5_LS_OCP	R	02h
OCP_STAT_3	HB12_HS_OCP	HB12_LS_OCP	HB11_HS_OCP	HB11_LS_OCP	HB10_HS_OCP	HB10_LS_OCP	HB9_HS_OCP	HB9_LS_OCP	R	03h
OLD_STAT_1	HB4_HS_OLD	HB4_LS_OLD	HB3_HS_OLD	HB3_LS_OLD	HB2_HS_OLD	HB2_LS_OLD	HB1_HS_OLD	HB1_LS_OLD	R	04h
OLD_STAT_2	HB8_HS_OLD	HB8_LS_OLD	HB7_HS_OLD	HB7_LS_OLD	HB6_HS_OLD	HB6_LS_OLD	HB5_HS_OLD	HB5_LS_OLD	R	05h
OLD_STAT_3	HB12_HS_OLD	HB12_LS_OLD	HB11_HS_OLD	HB11_LS_OLD	HB10_HS_OLD	HB10_LS_OLD	HB9_HS_OLD	HB9_LS_OLD	R	06h
CONFIG_CTRL	Reserved	IC_ID			OCP_REP	OTW_REP	EXT_OVP	CLR_FLT	RW	07h
OP_CTRL_1	HB4_HS_EN	HB4_LS_EN	HB3_HS_EN	HB3_LS_EN	HB2_HS_EN	HB2_LS_EN	HB1_HS_EN	HB1_LS_EN	RW	08h
OP_CTRL_2	HB8_HS_EN	HB8_LS_EN	HB7_HS_EN	HB7_LS_EN	HB6_HS_EN	HB6_LS_EN	HB5_HS_EN	HB5_LS_EN	RW	09h
OP_CTRL_3	HB12_HS_EN	HB12_LS_EN	HB11_HS_EN	HB11_LS_EN	HB10_HS_EN	HB10_LS_EN	HB9_HS_EN	HB9_LS_EN	RW	0Ah
PWM_CTRL_1	HB8_PWM	HB7_PWM	HB6_PWM	HB5_PWM	HB4_PWM	HB3_PWM	HB2_PWM	HB1_PWM	RW	0Bh
PWM_CTRL_2	PWM_CH4_DIS	PWM_CH3_DIS	PWM_CH2_DIS	PWM_CH1_DIS	HB12_PWM	HB11_PWM	HB10_PWM	HB9_PWM	RW	0Ch
FW_CTRL_1	HB8_FW	HB7_FW	HB6_FW	HB5_FW	HB4_FW	HB3_FW	HB2_FW	HB1_FW	RW	0Dh
FW_CTRL_2	Reserved				HB12_FW	HB11_FW	HB10_FW	HB9_FW	RW	0Eh
PWM_MAP_CTRL_1	HB4_PWM_MAP		HB3_PWM_MAP		HB2_PWM_MAP		HB1_PWM_MAP		RW	0Fh
PWM_MAP_CTRL_2(1)	HB8_PWM_MAP		HB7_PWM_MAP		HB6_PWM_MAP		HB5_PWM_MAP		RW	10h(1)
PWM_MAP_CTRL_3	HB12_PWM_MAP		HB11_PWM_MAP		HB10_PWM_MAP		HB9_PWM_MAP		RW	11h
PWM_FREQ_CTRL	PWM_CH4_FREQ		PWM_CH3_FREQ		PWM_CH2_FREQ		PWM_CH1_FREQ		RW	12h
PWM_DUTY_CTRL_1	PWM_DUTY_CH1								RW	13h
PWM_DUTY_CTRL_2	PWM_DUTY_CH2								RW	14h
PWM_DUTY_CTRL_3	PWM_DUTY_CH3								RW	15h
PWM_DUTY_CTRL_4	PWM_DUTY_CH4								RW	16h
SR_CTRL_1	HB8_SR	HB7_SR	HB6_SR	HB5_SR	HB4_SR	HB3_SR	HB2_SR	HB1_SR	RW	17h
SR_CTRL_2	Reserved				HB12_SR	HB11_SR	HB10_SR	HB9_SR	RW	18h
OLD_CTRL_1	HB8_OLD_DIS	HB7_OLD_DIS	HB6_OLD_DIS	HB5_OLD_DIS	HB4_OLD_DIS	HB3_OLD_DIS	HB2_OLD_DIS	HB1_OLD_DIS	RW	19h
OLD_CTRL_2	OLD_REP	OLD_OP	PL_MODE_EN		HB12_OLD_DIS	HB11_OLD_DIS	HB10_OLD_DIS	HB9_OLD_DIS	RW	1Ah
OLD_CTRL_3	OCP_DEG			OLD_NEG_EN	HB12_LOLD_EN	HB11_LOLD_EN	HB10_LOLD_EN	HB9_LOLD_EN	RW	1Bh
OLD_CTRL_4	HB8_LOLD_EN	HB7_LOLD_EN	HB6_LOLD_EN	HB5_LOLD_EN	HB4_LOLD_EN	HB3_LOLD_EN	HB2_LOLD_EN	HB1_LOLD_EN	RW	24h

(1) After this register address, the functions are similar between DRV8912-Q1 and DRV8910-Q1. However, DRV8908-Q1, DRV8906-Q1, and DRV8904-Q1 have different functions for these addresses.

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表 18. DRV8910-Q1 Register Map

Name	7	6	5	4	3	2	1	0	Type	Address
IC_STAT	Reserved	OTSD	OTW	OLD	OCP	UVLO	OVP	NPOR	R	00h
OCP_STAT_1	HB4_HS_OCP	HB4_LS_OCP	HB3_HS_OCP	HB3_LS_OCP	HB2_HS_OCP	HB2_LS_OCP	HB1_HS_OCP	HB1_LS_OCP	R	01h
OCP_STAT_2	HB8_HS_OCP	HB8_LS_OCP	HB7_HS_OCP	HB7_LS_OCP	HB6_HS_OCP	HB6_LS_OCP	HB5_HS_OCP	HB5_LS_OCP	R	02h
OCP_STAT_3	Reserved				HB10_HS_OCP	HB10_LS_OCP	HB9_HS_OCP	HB9_LS_OCP	R	03h
OLD_STAT_1	HB4_HS_OLD	HB4_LS_OLD	HB3_HS_OLD	HB3_LS_OLD	HB2_HS_OLD	HB2_LS_OLD	HB1_HS_OLD	HB1_LS_OLD	R	04h
OLD_STAT_2	HB8_HS_OLD	HB8_LS_OLD	HB7_HS_OLD	HB7_LS_OLD	HB6_HS_OLD	HB6_LS_OLD	HB5_HS_OLD	HB5_LS_OLD	R	05h
OLD_STAT_3	Reserved				HB10_HS_OLD	HB10_LS_OLD	HB9_HS_OLD	HB9_LS_OLD	R	06h
CONFIG_CTRL	Reserved	IC_ID			OCP_REP	OTW_REP	EXT_OVP	CLR_FLT	RW	07h
OP_CTRL_1	HB4_HS_EN	HB4_LS_EN	HB3_HS_EN	HB3_LS_EN	HB2_HS_EN	HB2_LS_EN	HB1_HS_EN	HB1_LS_EN	RW	08h
OP_CTRL_2	HB8_HS_EN	HB8_LS_EN	HB7_HS_EN	HB7_LS_EN	HB6_HS_EN	HB6_LS_EN	HB5_HS_EN	HB5_LS_EN	RW	09h
OP_CTRL_3	Reserved				HB10_HS_EN	HB10_LS_EN	HB9_HS_EN	HB9_LS_EN	RW	0Ah
PWM_CTRL_1	HB8_PWM	HB7_PWM	HB6_PWM	HB5_PWM	HB4_PWM	HB3_PWM	HB2_PWM	HB1_PWM	RW	0Bh
PWM_CTRL_2	PWM_CH4_DIS	PWM_CH3_DIS	PWM_CH2_DIS	PWM_CH1_DIS	Reserved		HB10_PWM	HB9_PWM	RW	0Ch
FW_CTRL_1	HB8_FW	HB7_FW	HB6_FW	HB5_FW	HB4_FW	HB3_FW	HB2_FW	HB1_FW	RW	0Dh
FW_CTRL_2	Reserved						HB10_FW	HB9_FW	RW	0Eh
PWM_MAP_CTRL_1	HB4_PWM_MAP		HB3_PWM_MAP		HB2_PWM_MAP		HB1_PWM_MAP		RW	0Fh
PWM_MAP_CTRL_2 (1)	HB8_PWM_MAP		HB7_PWM_MAP		HB6_PWM_MAP		HB5_PWM_MAP		RW	10h (1)
PWM_MAP_CTRL_3	Reserved				HB10_PWM_MAP		HB9_PWM_MAP		RW	11h
PWM_FREQ_CTRL	PWM_CH4_FREQ		PWM_CH3_FREQ		PWM_CH2_FREQ		PWM_CH1_FREQ		RW	12h
PWM_DUTY_CTRL_1	PWM_DUTY_CH1								RW	13h
PWM_DUTY_CTRL_2	PWM_DUTY_CH2								RW	14h
PWM_DUTY_CTRL_3	PWM_DUTY_CH3								RW	15h
PWM_DUTY_CTRL_4	PWM_DUTY_CH4								RW	16h
SR_CTRL_1	HB8_SR	HB7_SR	HB6_SR	HB5_SR	HB4_SR	HB3_SR	HB2_SR	HB1_SR	RW	17h
SR_CTRL_2	Reserved						HB10_SR	HB9_SR	RW	18h
OLD_CTRL_1	HB8_OLD_DIS	HB7_OLD_DIS	HB6_OLD_DIS	HB5_OLD_DIS	HB4_OLD_DIS	HB3_OLD_DIS	HB2_OLD_DIS	HB1_OLD_DIS	RW	19h
OLD_CTRL_2	OLD_REP	OLD_OP	PL_MODE_EN		Reserved		HB10_OLD_DIS	HB9_OLD_DIS	RW	1Ah
OLD_CTRL_3	OCP_DEG			OLD_NEG_EN	Reserved		HB10_LOLD_EN	HB9_LOLD_EN	RW	1Bh
OLD_CTRL_4	HB8_LOLD_EN	HB7_LOLD_EN	HB6_LOLD_EN	HB5_LOLD_EN	HB4_LOLD_EN	HB3_LOLD_EN	HB2_LOLD_EN	HB1_LOLD_EN	RW	24h

(1) After this register address, the register functions are similar between DRV8912-Q1 and DRV8910-Q1. However, DRV8908-Q1, DRV8906-Q1, and DRV8904-Q1 have different functions for these addresses.

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8.6.1.1 Status Registers

The status registers are used to report warning and fault conditions. The status registers are read-only registers.

表 19 lists the memory-mapped registers for the status registers. All register offset addresses not listed in 表 19 should be considered as reserved locations and the register contents should not be modified.

表 19. Status Registers Summary Table

Address	Register Name	Section
0x00	IC Status	Go
0x01	Overcurrent Protection (OCP) Status 1	Go
0x02	Overcurrent Protection (OCP) Status 2	Go
0x03	Overcurrent Protection (OCP) Status 3	Go
0x04	Open-Load Detect (OLD) Status 1	Go
0x05	Open-Load Detect (OLD) Status 2	Go
0x06	Open-Load Detect (OLD) Status 3	Go

8.6.1.1.1 IC Status (IC_STAT) Register (Address = 0x00) [reset = 0x00]

The IC status (IC_STAT) register is shown in 図 68 and described in 表 20.

Register access type: Read only

図 68. IC Status Register

7	6	5	4	3	2	1	0
Reserved	OTSD	OTW	OLD	OCP	UVLO	OVP	NPOR
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 20. IC Status Register Field Descriptions

Bit	Field	Type	Default	Description
7	Reserved	R	0b	Reserved
6	OTSD	R	0b	**0b = No overtemperature shutdown is detected** 1b = Overcurrent condition is detected
5	OTW	R	0b	**0b = No overtemperature warning is detected** 1b = Overcurrent condition is detected
4	OLD	R	0b	**0b = No open-load condition is detected** 1b = Open-load condition is detected
3	OCP	R	0b	**0b = No overcurrent condition is detected** 1b = Overcurrent condition is detected
2	UVLO	R	0b	**0b = No undervoltage lock-out condition is detected** 1b = Under-voltage lock-out condition condition is detected
1	OVP	R	0b	**0b = No overvoltage condition is detected** 1b = Overvoltage condition is detected
0	NPOR	R	0b	**0b = Power-on-reset condition is detected** 1b = No power-on-reset condition is detected

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8.6.1.1.2 *Overcurrent Protection (OCP) Status 1 (OCP_STAT_1) Register (Address = 0x01) [reset = 0x00]*

The overcurrent protection (OCP) status 1 register is shown in 図 69 and described in 表 21.

Register access type: Read only

図 69. Overcurrent Protection (OCP) Status 1 Register

7	6	5	4	3	2	1	0
HB4_HS_OCP	HB4_LS_OCP	HB3_HS_OCP	HB3_LS_OCP	HB2_HS_OCP	HB2_LS_OCP	HB1_HS_OCP	HB1_LS_OCP
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 21. Overcurrent Protection (OCP) Status 1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	HB4_HS_OCP	R	0b	**0b = No overcurrent detected on high-side switch of half-bridge 4** 1b = Overcurrent detected on high-side switch of half-bridge 4
6	HB4_LS_OCP	R	0b	**0b = No overcurrent detected on low-side switch of half-bridge 4** 1b = Overcurrent detected on low-side switch of half-bridge 4
5	HB3_HS_OCP	R	0b	**0b = No overcurrent detected on high-side switch of half-bridge 3** 1b = Overcurrent detected on high-side switch of half-bridge 3
4	HB3_LS_OCP	R	0b	**0b = No overcurrent detected on low-side switch of half-bridge 3** 1b = Overcurrent detected on low-side switch of half-bridge 3
3	HB2_HS_OCP	R	0b	**0b = No overcurrent detected on high-side switch of half-bridge 2** 1b = Overcurrent detected on high-side switch of half-bridge 2
2	HB2_LS_OCP	R	0b	**0b = No overcurrent detected on low-side switch of half-bridge 2** 1b = Overcurrent detected on low-side switch of half-bridge 2
1	HB1_HS_OCP	R	0b	**0b = No overcurrent detected on high-side switch of half-bridge 1** 1b = Overcurrent detected on high-side switch of half-bridge 1
0	HB1_LS_OCP	R	0b	**0b = No overcurrent detected on low-side switch of half-bridge 1** 1b = Overcurrent detected on low-side switch of half-bridge 1

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8.6.1.1.3 *Overcurrent Protection (OCP) Status 2 (OCP_STAT_2) Register (Address = 0x02) [reset = 0x00]*

The overcurrent protection (OCP) status 2 register is shown in 図 70 and described in .

Register access type: Read only

図 70. Overcurrent Protection (OCP) Status 2 Register

7	6	5	4	3	2	1	0
HB8_HS_OCP	HB8_LS_OCP	HB7_HS_OCP	HB7_LS_OCP	HB6_HS_OCP	HB6_LS_OCP	HB5_HS_OCP	HB5_LS_OCP
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 22. Overcurrent Protection (OCP) Status 2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	HB8_HS_OCP	R	0b	**0b = No overcurrent detected on high-side switch of half-bridge 8** 1b = Overcurrent detected on high-side switch of half-bridge 8
6	HB8_LS_OCP	R	0b	**0b = No overcurrent detected on low-side switch of half-bridge 8** 1b = Overcurrent detected on low-side switch of half-bridge 8
5	HB7_HS_OCP	R	0b	**0b = No overcurrent detected on high-side switch of half-bridge 7** 1b = Overcurrent detected on high-side switch of half-bridge 7
4	HB7_LS_OCP	R	0b	**0b = No overcurrent detected on low-side switch of half-bridge 7** 1b = Overcurrent detected on low-side switch of half-bridge 7
3	HB6_HS_OCP	R	0b	**0b = No overcurrent detected on high-side switch of half-bridge 6** 1b = Overcurrent detected on high-side switch of half-bridge 6
2	HB6_LS_OCP	R	0b	**0b = No overcurrent detected on low-side switch of half-bridge 6** 1b = Overcurrent detected on low-side switch of half-bridge 6
1	HB5_HS_OCP	R	0b	**0b = No overcurrent detected on high-side switch of half-bridge 5** 1b = Overcurrent detected on high-side switch of half-bridge 5
0	HB5_LS_OCP	R	0b	**0b = No overcurrent detected on low-side switch of half-bridge 5** 1b = Overcurrent detected on low-side switch of half-bridge 5

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8.6.1.1.4 *Overcurrent Protection (OCP) Status 3 (OCP_STAT_3) Register (Address = 0x03) [reset = 0x00]*

The overcurrent protection (OCP) status 3 register is shown in 図 71 and described in 表 23.

Register access type: Read only

図 71. Overcurrent Protection (OCP) Status 3 Register

7	6	5	4	3	2	1	0
HB12_HS_OCP	HB12_LS_OCP	HB11_HS_OCP	HB11_LS_OCP	HB10_HS_OCP	HB10_LS_OCP	HB9_HS_OCP	HB9_LS_OCP
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 23. Overcurrent Protection (OCP) Status 3 Register Field Descriptions

Bit	Field	Type	Default	Description
7	HB12_HS_OCP	R	0b	**0b = No overcurrent detected on high-side switch of half-bridge 12** 1b = Overcurrent detected on high-side switch of half-bridge 12
6	HB12_LS_OCP	R	0b	**0b = No overcurrent detected on low-side switch of half-bridge 12** 1b = Overcurrent detected on low-side switch of half-bridge 12
5	HB11_HS_OCP	R	0b	**0b = No overcurrent detected on high-side switch of half-bridge 11** 1b = Overcurrent detected on high-side switch of half-bridge 11
4	HB11_LS_OCP	R	0b	**0b = No overcurrent detected on low-side switch of half-bridge 11** 1b = Overcurrent detected on low-side switch of half-bridge 11
3	HB10_HS_OCP	R	0b	**0b = No overcurrent detected on high-side switch of half-bridge 10** 1b = Overcurrent detected on high-side switch of half-bridge 10
2	HB10_LS_OCP	R	0b	**0b = No overcurrent detected on low-side switch of half-bridge 10** 1b = Overcurrent detected on low-side switch of half-bridge 10
1	HB9_HS_OCP	R	0b	**0b = No overcurrent detected on high-side switch of half-bridge 9** 1b = Overcurrent detected on high-side switch of half-bridge 9
0	HB9_LS_OCP	R	0b	**0b = No overcurrent detected on low-side switch of half-bridge 9** 1b = Overcurrent detected on low-side switch of half-bridge 9

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8.6.1.1.5 *Open-Load Detect (OLD) Status 1 (OLD_STAT_1) Register (Address = 0x04) [reset = 0x00]*

The open-load detect (OLD) status 1 register is shown in 図 72 and described in 表 24.

Register access type: Read only

図 72. Open-Load Detect (OLD) Status 1 Register

7	6	5	4	3	2	1	0
HB4_HS_OLD	HB4_LS_OLD	HB3_HS_OLD	HB3_LS_OLD	HB2_HS_OLD	HB2_LS_OLD	HB1_HS_OLD	HB1_LS_OLD
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 24. Open-Load Detect (OLD) Status 1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	HB4_HS_OLD	R	0b	**0b = No open load detected on high-side switch of half-bridge 4** 1b = Open load detected on high-side switch of half-bridge 4
6	HB4_LS_OLD	R	0b	**0b = No open load detected on low-side switch of half-bridge 4** 1b = Open load detected on low-side switch of half-bridge 4
5	HB3_HS_OLD	R	0b	**0b = No open load detected on high-side switch of half-bridge 3** 1b = Open load detected on high-side switch of half-bridge 3
4	HB3_LS_OLD	R	0b	**0b = No open load detected on low-side switch of half-bridge 3** 1b = Open load detected on low-side switch of half-bridge 3
3	HB2_HS_OLD	R	0b	**0b = No open load detected on high-side switch of half-bridge 2** 1b = Open load detected on high-side switch of half-bridge 2
2	HB2_LS_OLD	R	0b	**0b = No open load detected on low-side switch of half-bridge 2** 1b = Open load detected on low-side switch of half-bridge 2
1	HB1_HS_OLD	R	0b	**0b = No open load detected on high-side switch of half-bridge 1** 1b = Open load detected on high-side switch of half-bridge 1
0	HB1_LS_OLD	R	0b	**0b = No open load detected on low-side switch of half-bridge 1** 1b = Open load detected on low-side switch of half-bridge 1

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8.6.1.1.6 *Open-Load Detect (OLD) Status 2 (OLD_STAT_2) Register (Address = 0x05) [reset = 0x00]*

The open-load detect (OLD) status 2 register is shown in 図 73 and described in 表 25.

Register access type: Read only

図 73. Open-Load Detect (OLD) Status 2 Register

7	6	5	4	3	2	1	0
HB8_HS_OLD	HB8_LS_OLD	HB7_HS_OLD	HB7_LS_OLD	HB6_HS_OLD	HB6_LS_OLD	HB5_HS_OLD	HB5_LS_OLD
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 25. Open-Load Detect (OLD) Status 2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	HB8_HS_OLD	R	0b	**0b = No open load detected on high-side switch of half-bridge 8** 1b = Open load detected on high-side switch of half-bridge 8
6	HB8_LS_OLD	R	0b	**0b = No open load detected on low-side switch of half-bridge 8** 1b = Open load detected on low-side switch of half-bridge 8
5	HB7_HS_OLD	R	0b	**0b = No open load detected on high-side switch of half-bridge 7** 1b = Open load detected on high-side switch of half-bridge 7
4	HB7_LS_OLD	R	0b	**0b = No open load detected on low-side switch of half-bridge 7** 1b = Open load detected on low-side switch of half-bridge 7
3	HB6_HS_OLD	R	0b	**0b = No open load detected on high-side switch of half-bridge 6** 1b = Open load detected on high-side switch of half-bridge 6
2	HB6_LS_OLD	R	0b	**0b = No open load detected on low-side switch of half-bridge 6** 1b = Open load detected on low-side switch of half-bridge 6
1	HB5_HS_OLD	R	0b	**0b = No open load detected on high-side switch of half-bridge 5** 1b = Open load detected on high-side switch of half-bridge 5
0	HB5_LS_OLD	R	0b	**0b = No open load detected on low-side switch of half-bridge 5** 1b = Open load detected on low-side switch of half-bridge 5

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8.6.1.1.7 *Open-Load Detect (OLD) Status 3 (OLD_STAT_3) Register (Address = 0x06) [reset = 0x00]*

The open-load detect (OLD) status 3 register is shown in 図 74 and described in 表 26.

Register access type: Read only

図 74. Open-Load Detect (OLD) Status 3 Register

7	6	5	4	3	2	1	0
HB12_HS_OLD	HB12_LS_OLD	HB11_HS_OLD	HB11_LS_OLD	HB10_HS_OLD	HB10_LS_OLD	HB9_HS_OLD	HB9_LS_OLD
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 26. Open-Load Detect (OLD) Status 3 Register Field Descriptions

Bit	Field	Type	Default	Description
7	HB12_HS_OLD	R	0b	**0b = No open load detected on high-side switch of half-bridge 12** 1b = Open load detected on high-side switch of half-bridge 12
6	HB12_LS_OLD	R	0b	**0b = No open load detected on low-side switch of half-bridge 12** 1b = Open load detected on low-side switch of half-bridge 12
5	HB11_HS_OLD	R	0b	**0b = No open load detected on high-side switch of half-bridge 11** 1b = Open load detected on high-side switch of half-bridge 11
4	HB11_LS_OLD	R	0b	**0b = No open load detected on low-side switch of half-bridge 11** 1b = Open load detected on low-side switch of half-bridge 11
3	HB10_HS_OLD	R	0b	**0b = No open load detected on high-side switch of half-bridge 10** 1b = Open load detected on high-side switch of half-bridge 10
2	HB10_LS_OLD	R	0b	**0b = No open load detected on low-side switch of half-bridge 10** 1b = Open load detected on low-side switch of half-bridge 10
1	HB9_HS_OLD	R	0b	**0b = No open load detected on high-side switch of half-bridge 9** 1b = Open load detected on high-side switch of half-bridge 9
0	HB9_LS_OLD	R	0b	**0b = No open load detected on low-side switch of half-bridge 9** 1b = Open load detected on low-side switch of half-bridge 9

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8.6.1.2 Control Registers

The control registers are used to configure the device. The control registers are read and write capable.

表 27 lists the memory-mapped registers for the control registers. All register offset addresses not listed in 表 27 should be considered as reserved locations and the register contents should not be modified.

表 27. Control Registers Summary Table

Address	Register Name	Section
0x07	Configuration Register	Go
0x08	Operation Control 1 Register	Go
0x09	Operation Control 2 Register	Go
0x0A	Operation Control 3 Register	Go
0x0B	PWM Control 1 Register	Go
0x0C	PWM Control 2 Register	Go
0x0D	Free-Wheeling Control 1 Register	Go
0x0E	Free-Wheeling Control 2 Register	Go
0x0F	PWM Map Control 1 Register	Go
0x10	PWM Map Control 2 Register	Go
0x11	PWM Map Control 3 Register	Go
0x12	PWM Frequency Control Register	Go
0x13	PWM Duty Control Channel 1 Register	Go
0x14	PWM Duty Control Channel 2 Register	Go
0x15	PWM Duty Control Channel 3 Register	Go
0x16	PWM Duty Control Channel 4 Register	Go
0x17	Slew Rate Control 1 Register	Go
0x18	Slew Rate Control 2 Register	Go
0x19	Open-Load Detect Control 1 Register	Go
0x1A	Open-Load Detect Control 2 Register	Go
0x1B	Open-Load Detect Control 3 Register	Go
0x24	Open-Load Detect Control 4 Register	Go

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8.6.1.2.1 *Configuration (CONFIG_CTRL) Register (Address = 0x07) [reset = 0x00]*

The configuration register is shown in 図 75 and described in 表 28.

Register access type: Read/Write

図 75. Configuration Register

7	6	5	4	3	2	1	0
Reserved		IC_ID		OCP_REP	OTW_REP	EXT_OVP	CLR_FLT
R/W-0b	R-Xb	R-Xb	R-Xb	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 28. Configuration Register Field Descriptions

Bit	Field	Type	Default	Description
7	Reserved	R/W	0b	Reserved
6-4	IC_ID	R	XXXb	000b = Device connected is DRV8912-Q1 (12 Channel Device) 001b = Device connected is DRV8910-Q1 (10 Channel Device) 010b = Device connected is DRV8908-Q1 (8 Channel Device) 011b = Device connected is DRV8906-Q1 (6 Channel Device) 100b = Device connected is DRV8904-Q1 (4 Channel Device) 101b = Reserved 110b = Reserved 111b = Reserved
3	OCP_REP	R/W	0b	**0b = Overcurrent condition is reported in nFAULT pin** 1b = Overcurrent condition warning is not reported on the nFAULT pin
2	OTW_REP	R/W	0b	**0b = Overtemperature warning is not reported in nFAULT pin** 1b = Overtemperature warning is reported on the nFAULT pin
1	EXT_OVP	R/W	0b	**0b = Overvoltage protection threshold is at 21 V** 1b = Overvoltage protection threshold is at 33 V
0	CLR_FLT	R/W	0b	**0b = Faults not cleared** 1b = Clear all faults

注

CLR_FLT bit is an auto-clear bit and will always read '0'.

8.6.1.2.2 *Operation Control 1 (OP_CTRL_1) Register (Address = 0x08) [reset = 0x00]*

The operation control 1 register is shown in 図 76 and described in 表 29.

Register access type: Read/Write

図 76. Operation Control 1 Register

7	6	5	4	3	2	1	0
HB4_HS_EN	HB4_LS_EN	HB3_HS_EN	HB3_LS_EN	HB2_HS_EN	HB2_LS_EN	HB1_HS_EN	HB1_LS_EN
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 29. Operation Control 1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	HB4_HS_EN	R/W	0b	**0b = Half-bridge 4 high-side switch is disabled** 1b = Half-bridge 4 high-side switch is enabled
6	HB4_LS_EN	R/W	0b	**0b = Half-bridge 4 low-side switch is disabled** 1b = Half-bridge 4 low-side switch is enabled
5	HB3_HS_EN	R/W	0b	**0b = Half-bridge 3 high-side switch is disabled** 1b = Half-bridge 3 high-side switch is enabled
4	HB3_LS_EN	R/W	0b	**0b = Half-bridge 3 low-side switch is disabled** 1b = Half-bridge 3 low-side switch is enabled
3	HB2_HS_EN	R/W	0b	**0b = Half-bridge 2 high-side switch is disabled** 1b = Half-bridge 2 high-side switch is enabled
2	HB2_LS_EN	R/W	0b	**0b = Half-bridge 2 low-side switch is disabled** 1b = Half-bridge 2 low-side switch is enabled
1	HB1_HS_EN	R/W	0b	**0b = Half-bridge 1 high-side switch is disabled** 1b = Half-bridge 1 high-side switch is enabled
0	HB1_LS_EN	R/W	0b	**0b = Half-bridge 1 low-side switch is disabled** 1b = Half-bridge 1 low-side switch is enabled

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8.6.1.2.3 *Operation Control 2 (OP_CTRL_2) Register (Address = 0x09) [reset = 0x00]*

The operation control 2 register is shown in 図 77 and described in 表 30.

Register access type: Read/Write

図 77. Operation Control 2 Register

7	6	5	4	3	2	1	0
HB8_HS_EN	HB8_LS_EN	HB7_HS_EN	HB7_LS_EN	HB6_HS_EN	HB6_LS_EN	HB5_HS_EN	HB5_LS_EN
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 30. Operation Control 2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	HB8_HS_EN	R/W	0b	**0b = Half-bridge 8 high-side switch is disabled** 1b = Half-bridge 8 high-side switch is enabled
6	HB8_LS_EN	R/W	0b	**0b = Half-bridge 8 low-side switch is disabled** 1b = Half-bridge 8 low-side switch is enabled
5	HB7_HS_EN	R/W	0b	**0b = Half-bridge 7 high-side switch is disabled** 1b = Half-bridge 7 high-side switch is enabled
4	HB7_LS_EN	R/W	0b	**0b = Half-bridge 7 low-side switch is disabled** 1b = Half-bridge 7 low-side switch is enabled
3	HB6_HS_EN	R/W	0b	**0b = Half-bridge 6 high-side switch is disabled** 1b = Half-bridge 6 high-side switch is enabled
2	HB6_LS_EN	R/W	0b	**0b = Half-bridge 6 low-side switch is disabled** 1b = Half-bridge 6 low-side switch is enabled
1	HB5_HS_EN	R/W	0b	**0b = Half-bridge 5 high-side switch is disabled** 1b = Half-bridge 5 high-side switch is enabled
0	HB5_LS_EN	R/W	0b	**0b = Half-bridge 5 low-side switch is disabled** 1b = Half-bridge 5 low-side switch is enabled

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8.6.1.2.4 *Operation Control 3 (OP_CTRL_3) Register (Address = 0x0A) [reset = 0x00]*

The operation control 3 register is shown in 図 78 and described in 表 31.

Register access type: Read/Write

図 78. Operation Control 3 Register

7	6	5	4	3	2	1	0
HB12_HS_EN	HB12_LS_EN	HB11_HS_EN	HB11_LS_EN	HB10_HS_EN	HB10_LS_EN	HB9_HS_EN	HB9_LS_EN
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 31. Operation Control 3 Register Field Descriptions

Bit	Field	Type	Default	Description
7	HB12_HS_EN	R/W	0b	**0b = Half-bridge 12 high-side switch is disabled** 1b = Half-bridge 12 high-side switch is enabled
6	HB12_LS_EN	R/W	0b	**0b = Half-bridge 12 low-side switch is disabled** 1b = Half-bridge 12 low-side switch is enabled
5	HB11_HS_EN	R/W	0b	**0b = Half-bridge 11 high-side switch is disabled** 1b = Half-bridge 11 high-side switch is enabled
4	HB11_LS_EN	R/W	0b	**0b = Half-bridge 11 low-side switch is disabled** 1b = Half-bridge 11 low-side switch is enabled
3	HB10_HS_EN	R/W	0b	**0b = Half-bridge 10 high-side switch is disabled** 1b = Half-bridge 10 high-side switch is enabled
2	HB10_LS_EN	R/W	0b	**0b = Half-bridge 10 low-side switch is disabled** 1b = Half-bridge 10 low-side switch is enabled
1	HB9_HS_EN	R/W	0b	**0b = Half-bridge 9 high-side switch is disabled** 1b = Half-bridge 9 high-side switch is enabled
0	HB9_LS_EN	R/W	0b	**0b = Half-bridge 9 low-side switch is disabled** 1b = Half-bridge 9 low-side switch is enabled

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8.6.1.2.5 *PWM Control 1 (PWM_CTRL_1) Register (Address = 0x0B) [reset = 0x00]*

The PWM control 1 register is shown in 図 79 and described in 表 32.

Register access type: Read/Write

図 79. PWM Control 1 Register

7	6	5	4	3	2	1	0
HB8_PWM	HB7_PWM	HB6_PWM	HB5_PWM	HB4_PWM	HB3_PWM	HB2_PWM	HB1_PWM
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 32. PWM Control 1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	HB8_PWM	R/W	0b	**0b = Half-bridge 8 is operating in continuous mode** 1b = Half-bridge 8 is operating in PWM mode
6	HB7_PWM	R/W	0b	**0b = Half-bridge 7 is operating in continuous mode** 1b = Half-bridge 7is operating in PWM mode
5	HB6_PWM	R/W	0b	**0b = Half-bridge 6 is operating in continuous mode** 1b = Half-bridge 6 is operating in PWM mode
4	HB5_PWM	R/W	0b	**0b = Half-bridge 5 is operating in continuous mode** 1b = Half-bridge 5 is operating in PWM mode
3	HB4_PWM	R/W	0b	**0b = Half-bridge 4 is operating in continuous mode** 1b = Half-bridge 4 is operating in PWM mode
2	HB3_PWM	R/W	0b	**0b = Half-bridge 3 is operating in continuous mode** 1b = Half-bridge 3 is operating in PWM mode
1	HB2_PWM	R/W	0b	**0b = Half-bridge 2 is operating in continuous mode** 1b = Half-bridge 2 is operating in PWM mode
0	HB1_PWM	R/W	0b	**0b = Half-bridge 1 is operating in continuous mode** 1b = Half-bridge 1 is operating in PWM mode

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8.6.1.2.6 *PWM Control 2 (PWM_CTRL_2) Register (Address = 0x0C) [reset = 0x00]*

The PWM control 2 register is shown in 図 80 and described in 表 33.

Register access type: Read/Write

図 80. PWM Control 2 Register

7	6	5	4	3	2	1	0
PWM_CH4_DIS	PWM_CH3_DIS	PWM_CH2_DIS	PWM_CH1_DIS	HB12_PWM	HB11_PWM	HB10_PWM	HB9_PWM
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 33. PWM Control 2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	PWM_CH4_DIS	R/W	0b	**0b = PWM Generator-4 is enabled** 1b = PWM Generator-4 is disabled
6	PWM_CH3_DIS	R/W	0b	**0b = PWM Generator-3 is enabled** 1b = PWM Generator-3 is disabled
5	PWM_CH2_DIS	R/W	0b	**0b = PWM Generator-2 is enabled** 1b = PWM Generator-2 is disabled
4	PWM_CH1_DIS	R/W	0b	**0b = PWM Generator-1 is enabled** 1b = PWM Generator-1 is disabled
3	HB12_PWM	R/W	0b	**0b = Half-bridge 12 is operating in continuous mode** 1b = Half-bridge 12 is operating in PWM mode
2	HB11_PWM	R/W	0b	**0b = Half-bridge 11 is operating in continuous mode** 1b = Half-bridge 11 is operating in PWM mode
1	HB10_PWM	R/W	0b	**0b = Half-bridge 10 is operating in continuous mode** 1b = Half-bridge 10 is operating in PWM mode
0	HB9_PWM	R/W	0b	**0b = Half-bridge 9 is operating in continuous mode** 1b = Half-bridge 9 is operating in PWM mode

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8.6.1.2.7 *Free-Wheeling Control 1 (FW_CTRL_1) Register (Address = 0x0D) [reset = 0x00]*

The free-wheeling control 1 register is shown in 図 81 and described in 表 34.

Register access type: Read/Write

図 81. Free-Wheeling Control 1 Register

7	6	5	4	3	2	1	0
HB8_FW	HB7_FW	HB6_FW	HB5_FW	HB4_FW	HB3_FW	HB2_FW	HB1_FW
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 34. Free-Wheeling Control 1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	HB8_FW	R/W	0b	**0b = Passive free-wheeling on half-bridge 8 is enabled** 1b = Active free-wheeling on half-bridge 8 is enabled
6	HB7_FW	R/W	0b	**0b = Passive free-wheeling on half-bridge 7 is enabled** 1b = Active free-wheeling on half-bridge 7 is enabled
5	HB6_FW	R/W	0b	**0b = Passive free-wheeling on half-bridge 6 is enabled** 1b = Active free-wheeling on half-bridge 6 is enabled
4	HB5_FW	R/W	0b	**0b = Passive free-wheeling on half-bridge 5 is enabled** 1b = Active free-wheeling on half-bridge 5 is enabled
3	HB4_FW	R/W	0b	**0b = Passive free-wheeling on half-bridge 4 is enabled** 1b = Active free-wheeling on half-bridge 4 is enabled
2	HB3_FW	R/W	0b	**0b = Passive free-wheeling on half-bridge 3 is enabled** 1b = Active free-wheeling on half-bridge 3 is enabled
1	HB2_FW	R/W	0b	**0b = Passive free-wheeling on half-bridge 2 is enabled** 1b = Active free-wheeling on half-bridge 2 is enabled
0	HB1_FW	R/W	0b	**0b = Passive free-wheeling on half-bridge 1 is enabled** 1b = Active free-wheeling on half-bridge 1 is enabled

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8.6.1.2.8 *Free-Wheeling Control 2 (FW_CTRL_2) Register (Address = 0x0E) [reset = 0x00]*

The free-wheeling control 2 register is shown in 図 82 and described in 表 35.

Register access type: Read/Write

図 82. Free-Wheeling Control 2 Register

7	6	5	4	3	2	1	0
Reserved				HB12_FW	HB11_FW	HB10_FW	HB9_FW
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 35. Free-Wheeling Control 2 Register Field Descriptions

Bit	Field	Type	Default	Description
7-4	Reserved	R/W	0000b	Reserved
3	HB12_FW	R/W	0b	**0b = Passive free-wheeling on half-bridge 12 is enabled** 1b = Active free-wheeling on half-bridge 12 is enabled
2	HB11_FW	R/W	0b	**0b = Passive free-wheeling on half-bridge 11 is enabled** 1b = Active free-wheeling on half-bridge 11 is enabled
1	HB10_FW	R/W	0b	**0b = Passive free-wheeling on half-bridge 10 is enabled** 1b = Active free-wheeling on half-bridge 10 is enabled
0	HB9_FW	R/W	0b	**0b = Passive free-wheeling on half-bridge 9 is enabled** 1b = Active free-wheeling on half-bridge 9 is enabled

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8.6.1.2.9 *PWM Map Control 1 (PWM_MAP_CTRL_1) Register (Address = 0x0F) [reset = 0x00]*

The PWM Map Control 1 register is shown in 図 83 and described in 表 36.

Register access type: Read/Write

図 83. PWM Map Control 1 Register

7	6	5	4	3	2	1	0
HB4_PWM_MAP		HB3_PWM_MAP		HB2_PWM_MAP		HB1_PWM_MAP	
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 36. PWM Map Control 1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	HB4_PWM_MAP	R/W	00b	**00b = HB4 mapped to PWM channel 1** 01b = HB4 mapped to PWM channel 2 10b = HB4 mapped to PWM channel 3 11b = HB4 mapped to PWM channel 4
5-4	HB3_PWM_MAP	R/W	00b	**00b = HB3 mapped to PWM channel 1** 01b = HB3 mapped to PWM channel 2 10b = HB3 mapped to PWM channel 3 11b = HB3 mapped to PWM channel 4
3-2	HB2_PWM_MAP	R/W	00b	**00b = HB2 mapped to PWM channel 1** 01b = HB2 mapped to PWM channel 2 10b = HB2 mapped to PWM channel 3 11b = HB2 mapped to PWM channel 4
1-0	HB1_PWM_MAP	R/W	00b	**00b = HB1 mapped to PWM channel 1** 01b = HB1 mapped to PWM channel 2 10b = HB1 mapped to PWM channel 3 11b = HB1 mapped to PWM channel 4

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8.6.1.2.10 *PWM Map Control 2 (PWM_MAP_CTRL_2) Register (Address = 0x10) [reset = 0x00]*

The PWM Map Control 2 register is shown in 図 84 and described in 表 37.

Register access type: Read/Write

図 84. PWM Map Control 2 Register

7	6	5	4	3	2	1	0
HB8_PWM_MAP		HB7_PWM_MAP		HB6_PWM_MAP		HB5_PWM_MAP	
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 37. PWM Map Control 2 Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	HB8_PWM_MAP	R/W	00b	**00b = HB8 mapped to PWM channel 1** 01b = HB8 mapped to PWM channel 2 10b = HB8 mapped to PWM channel 3 11b = HB8 mapped to PWM channel 4
5-4	HB7_PWM_MAP	R/W	00b	**00b = HB7 mapped to PWM channel 1** 01b = HB7 mapped to PWM channel 2 10b = HB7 mapped to PWM channel 3 11b = HB7 mapped to PWM channel 4
3-2	HB6_PWM_MAP	R/W	00b	**00b = HB6 mapped to PWM channel 1** 01b = HB6 mapped to PWM channel 2 10b = HB6 mapped to PWM channel 3 11b = HB6 mapped to PWM channel 4
1-0	HB5_PWM_MAP	R/W	00b	**00b = HB5 mapped to PWM channel 1** 01b = HB5 mapped to PWM channel 2 10b = HB5 mapped to PWM channel 3 11b = HB5 mapped to PWM channel 4

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8.6.1.2.11 *PWM Map Control 3 (PWM_MAP_CTRL_3) Register (Address = 0x11) [reset = 0x00]*

The PWM Map Control 3 register is shown in 図 85 and described in 表 38.

Register access type: Read/Write

図 85. PWM Map Control 3 Register

7	6	5	4	3	2	1	0
HB12_PWM_MAP		HB11_PWM_MAP		HB10_PWM_MAP		HB9_PWM_MAP	
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 38. PWM Map Control 3 Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	HB12_PWM_MAP	R/W	00b	**00b = HB12 mapped to PWM channel 1** 01b = HB12 mapped to PWM channel 2 10b = HB12 mapped to PWM channel 3 11b = HB12 mapped to PWM channel 4
5-4	HB11_PWM_MAP	R/W	00b	**00b = HB11 mapped to PWM channel 1** 01b = HB11 mapped to PWM channel 2 10b = HB11 mapped to PWM channel 3 11b = HB11 mapped to PWM channel 4
3-2	HB10_PWM_MAP	R/W	00b	**00b = HB10 mapped to PWM channel 1** 01b = HB10 mapped to PWM channel 2 10b = HB10 mapped to PWM channel 3 11b = HB10 mapped to PWM channel 4
1-0	HB9_PWM_MAP	R/W	00b	**00b = HB9 mapped to PWM channel 1** 01b = HB9 mapped to PWM channel 2 10b = HB9 mapped to PWM channel 3 11b = HB9 mapped to PWM channel 4

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8.6.1.2.12 *PWM Frequency Control (PWM_FREQ_CTRL) Register (Address = 0x12) [reset = 0x00]*

The PWM Frequency Control register is shown in 図 86 and described in 表 39.

Register access type: Read/Write

図 86. PWM Frequency Control Register

7	6	5	4	3	2	1	0
PWM_CH4_FREQ		PWM_CH3_FREQ		PWM_CH2_FREQ		PWM_CH1_FREQ	
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 39. PWM Frequency Control Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	PWM_CH4_FREQ	R/W	00b	**00b = PWM frequency is 80 Hz** 01b = PWM frequency is 100 Hz 10b = PWM frequency is 200 Hz 11b = PWM frequency is 2000 Hz
5-4	PWM_CH3_FREQ	R/W	00b	**00b = PWM frequency is 80 Hz** 01b = PWM frequency is 100 Hz 10b = PWM frequency is 200 Hz 11b = PWM frequency is 2000 Hz
3-2	PWM_CH2_FREQ	R/W	00b	**00b = PWM frequency is 80 Hz** 01b = PWM frequency is 100 Hz 10b = PWM frequency is 200 Hz 11b = PWM frequency is 2000 Hz
1-0	PWM_CH1_FREQ	R/W	00b	**00b = PWM frequency is 80 Hz** 01b = PWM frequency is 100 Hz 10b = PWM frequency is 200 Hz 11b = PWM frequency is 2000 Hz

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8.6.1.2.13 *PWM Duty Control Channel 1 (PWM_DUTY_CH1) Register (Address = 0x13) [reset = 0x00]*

The channel 1 PWM duty cycle control register is shown in 図 87 and described in 表 40.

Register access type: Read/Write

図 87. PWM Duty Control Channel 1 Register

7	6	5	4	3	2	1	0
PWM_DUTY_CH1							
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 40. PWM Duty Control Channel 1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PWM_DUTY_CH1	R/W	00000000b	**00000000b = 0 % PWM Duty** 11111111b = 100 % PWM Duty Calculate duty as decimal (xxxxxxxxb) × 1/255

8.6.1.2.14 *PWM Duty Control Channel 2 (PWM_DUTY_CH2) Register (Address = 0x14) [reset = 0x00]*

The channel 2 PWM duty cycle control register is shown in 図 88 and described in 表 41.

Register access type: Read/Write

図 88. PWM Duty Control Channel 2 Register

7	6	5	4	3	2	1	0
PWM_DUTY_CH2							
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 41. PWM Duty Control Channel 2 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PWM_DUTY_CH2	R/W	00000000b	**00000000b = 0 % PWM Duty** 11111111b = 100 % PWM Duty Calculate duty as decimal (xxxxxxxxb) × 1/255

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8.6.1.2.15 *PWM Duty Control Channel 3 (PWM_DUTY_CH3) Register (Address = 0x15) [reset = 0x00]*

The channel 3 PWM duty cycle control register is shown in 図 89 and described in 表 42.

Register access type: Read/Write

図 89. PWM Duty Control Channel 3 Register

7	6	5	4	3	2	1	0
PWM_DUTY_CH3							
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 42. PWM Duty Control Channel 3 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PWM_DUTY_CH3	R/W	00000000b	**00000000b = 0 % PWM Duty** 11111111b = 100 % PWM Duty Calculate duty as decimal (xxxxxxxxb) × 1/255

8.6.1.2.16 *PWM Duty Control Channel 4 (PWM_DUTY_CH4) Register (Address = 0x16) [reset = 0x00]*

The channel 4 PWM duty cycle control register is shown in 図 90 and described in 表 43.

Register access type: Read/Write

図 90. PWM Duty Control Channel 4 Register

7	6	5	4	3	2	1	0
PWM_DUTY_CH4							
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 43. PWM Duty Control Channel 4 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PWM_DUTY_CH4	R/W	00000000b	**00000000b = 0 % PWM Duty** 11111111b = 100 % PWM Duty Calculate duty as decimal (xxxxxxxxb) × 1/255

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8.6.1.2.17 *Slew Rate Control 1 (SR_CTRL_1) Register (Address = 0x17) [reset = 0x00]*

The slew rate control 1 register is shown in 図 91 and described in 表 44.

Register access type: Read/Write

図 91. Slew Rate Control 1 Register

7	6	5	4	3	2	1	0
HB8_SR	HB7_SR	HB6_SR	HB5_SR	HB4_SR	HB3_SR	HB2_SR	HB1_SR
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 44. Slew Rate Control 1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	HB8_SR	R/W	0b	**0b = 0.6 V/µs** 1b = 2.5 V/µs
6	HB7_SR	R/W	0b	**0b = 0.6 V/µs** 1b = 2.5 V/µs
5	HB6_SR	R/W	0b	**0b = 0.6 V/µs** 1b = 2.5 V/µs
4	HB5_SR	R/W	0b	**0b = 0.6 V/µs** 1b = 2.5 V/µs
3	HB4_SR	R/W	0b	**0b = 0.6 V/µs** 1b = 2.5 V/µs
2	HB3_SR	R/W	0b	**0b = 0.6 V/µs** 1b = 2.5 V/µs
1	HB2_SR	R/W	0b	**0b = 0.6 V/µs** 1b = 2.5 V/µs
0	HB1_SR	R/W	0b	**0b = 0.6 V/µs** 1b = 2.5 V/µs

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8.6.1.2.18 *Slew Rate Control 2 (SR_CTRL_2) Register (Address = 0x18) [reset = 0x00]*

The slew rate control 2 register is shown in 図 92 and described in 表 45.

Register access type: Read/Write

図 92. Slew Rate Control 2 Register

7	6	5	4	3	2	1	0
Reserved				HB12_SR	HB11_SR	HB10_SR	HB9_SR
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 45. Slew Rate Control 2 Register Field Descriptions

Bit	Field	Type	Default	Description
7-4	Reserved	R/W	0000b	Reserved
3	HB12_SR	R/W	0b	**0b = 0.6 V/µs** 1b = 2.5 V/µs
2	HB11_SR	R/W	0b	**0b = 0.6 V/µs** 1b = 2.5 V/µs
1	HB10_SR	R/W	0b	**0b = 0.6 V/µs** 1b = 2.5 V/µs
0	HB9_SR	R/W	0b	**0b = 0.6 V/µs** 1b = 2.5 V/µs

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8.6.1.2.19 *Open-Load Detect (OLD) Control 1 (OLD_CTRL_1) Register (Address = 0x19) [reset = 0x00]*

The open-load detect (OLD) control (OLD_CTRL_1) register-1 is shown in 図 93 and described in 表 46.

Register access type: Read/Write

図 93. Open-Load Detect (OLD) Control (OLD_CTRL_1) Register

7	6	5	4	3	2	1	0
HB8_OLD_DIS	HB7_OLD_DIS	HB6_OLD_DIS	HB5_OLD_DIS	HB4_OLD_DIS	HB3_OLD_DIS	HB2_OLD_DIS	HB1_OLD_DIS
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 46. Open-Load Detect (OLD) Control (OLD_CTRL_1) Register Field Descriptions

Bit	Field	Type	Default	Description
7	HB8_OLD_DIS	R/W	0b	**0b = Open-load detection on half-bridge 8 is enabled** 1b = Open-load on half-bridge 8 is disabled
6	HB7_OLD_DIS	R/W	0b	**0b = Open-load detection on half-bridge 7 is enabled** 1b = Open-load on half-bridge 7 is disabled
5	HB6_OLD_DIS	R/W	0b	**0b = Open-load detection on half-bridge 6 is enabled** 1b = Open-load on half-bridge 6 is disabled
4	HB5_OLD_DIS	R/W	0b	**0b = Open-load detection on half-bridge 5 is enabled** 1b = Open-load on half-bridge 5 is disabled
3	HB4_OLD_DIS	R/W	0b	**0b = Open-load detection on half-bridge 4 is enabled** 1b = Open-load on half-bridge 4 is disabled
2	HB3_OLD_DIS	R/W	0b	**0b = Open-load detection on half-bridge 3 is enabled** 1b = Open-load on half-bridge 3 is disabled
1	HB2_OLD_DIS	R/W	0b	**0b = Open-load detection on half-bridge 2 is enabled** 1b = Open-load on half-bridge 2 is disabled
0	HB1_OLD_DIS	R/W	0b	**0b = Open-load detection on half-bridge 1 is enabled** 1b = Open-load on half-bridge 1 is disabled

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8.6.1.2.20 *Open-Load Detect (OLD) Control 2 (OLD_CTRL_2) Register (Address = 0x1A) [reset = 0x00]*

The open-load detect (OLD) control (OLD_CTRL_2) register-2 is shown in 図 94 and described in 表 47.

Register access type: Read/Write

図 94. Open-Load Detect (OLD) Control (OLD_CTRL_2) Register

7	6	5	4	3	2	1	0
OLD_REP	OLD_OP	PL_MODE_EN		HB12_OLD_DIS	HB11_OLD_DIS	HB10_OLD_DIS	HB9_OLD_DIS
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 47. Open-Load Detect (OLD) Control (OLD_CTRL_2) Register Field Descriptions

Bit	Field	Type	Default	Description
7	OLD_REP	R/W	0b	**0b = Report on nFAULT pin during OLD condition** 1b = No report on nFAULT pin during OLD condition
6	OLD_OP	R/W	0b	**0b = Half bridges are not active after OLD condition detect** 1b = Half bridges are active after OLD condition detect
5-4	PL_MODE_EN	W	00b	**00b = Parallel mode OCP fast turn-off slew is enabled** 01b = Parallel mode OCP slow turn-off slew is enabled 10b = Invalid Setting 11b = Invalid Setting
3	HB12_OLD_DIS	R/W	0b	**0b = Open-load detection on half-bridge 12 is enabled** 1b = Open-load on half-bridge 12 is disabled
2	HB11_OLD_DIS	R/W	0b	**0b = Open-load detection on half-bridge 11 is enabled** 1b = Open-load on half-bridge 11 is disabled
1	HB10_OLD_DIS	R/W	0b	**0b = Open-load detection on half-bridge 10 is enabled** 1b = Open-load on half-bridge 10 is disabled
0	HB9_OLD_DIS	R/W	0b	**0b = Open-load detection on half-bridge 9 is enabled** 1b = Open-load on half-bridge 9 is disabled

注

For DRV8912 and DRV8910, the PL_MODE_EN is write only bits and always read "00b".

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8.6.1.2.21 Open-Load Detect (OLD) Control 3 (OLD_CTRL_3) Register (Address = 0x1B) [reset = 0x00]

The open-load detect (OLD) control (OLD_CTRL_3) register-3 is shown in 図 95 and described in 表 48. This register also contains the bits to set the OCP deglitch time (OCP_DEG).

Register access type: Read/Write

図 95. Open-Load Detect (OLD) Control (OLD_CTRL_3) Register

7	6	5	4	3	2	1	0
	OCP_DEG		OLD_NEG_EN	HB12_LOLD_EN	HB11_LOLD_EN	HB10_LOLD_EN	HB9_LOLD_EN
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 48. Open-Load Detect (OLD) Control (OLD_CTRL_3) Register Field Descriptions

Bit	Field	Type	Default	Description
7-5	OCP_DEG	R/W	000b	**000b = OCP deglitch time is 10 µs** 001b = OCP deglitch time is 5 µs 010b = OCP deglitch time is 2.5µs 011b = OCP deglitch time is 1 µs 100b = OCP deglitch time is 60 µs 101b = OCP deglitch time is 40 µs 110b = OCP deglitch time is 30 µs 111b = OCP deglitch time is 20 µs
4	OLD_NEG_EN	R/W	0b	**0b = Negative-current OLD mode is disabled** 1b = Negative-current OLD mode is enabled
3	HB12_LOLD_EN	R/W	0b	**0b = Low-current OLD on half-bridge 12 is disabled** 1b = Low-current OLD on half-bridge 12 is enabled
2	HB11_LOLD_EN	R/W	0b	**0b = Low-current OLD on half-bridge 11 is disabled** 1b = Low-current OLD on half-bridge 12 is enabled
1	HB10_LOLD_EN	R/W	0b	**0b = Low-current OLD on half-bridge 10 is disabled** 1b = Low-current OLD on half-bridge 12 is enabled
0	HB9_LOLD_EN	R/W	0b	**0b = Low-current OLD on half-bridge 9 is disabled** 1b = Low-current OLD on half-bridge 9 is enabled

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8.6.1.2.22 Open-Load Detect (OLD) Control 4 (OLD_CTRL_4) Register (Address = 0x24) [reset = 0x00]

The open-load detect (OLD) control (OLD_CTRL_4) register-4 is shown in 図 96 and described in 表 49.

Register access type: Read/Write

図 96. Open-Load Detect (OLD) Control (OLD_CTRL_4) Register

7	6	5	4	3	2	1	0
HB8_LCOLD_EN	HB7_LOLD_EN	HB6_LOLD_EN	HB5_LOLD_EN	HB4_LOLD_EN	HB3_LOLD_EN	HB2_LOLD_EN	HB1_LOLD_EN
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 49. Open-Load Detect (OLD) Control (OLD_CTRL_4) Register Field Descriptions

Bit	Field	Type	Default	Description
7	HB8_LOLD_EN	R/W	0b	**0b = Low-current OLD on half-bridge 8 is disabled** 1b = Low-current OLD on half-bridge 8 is enabled
6	HB7_LOLD_EN	R/W	0b	**0b = Low-current OLD on half-bridge 7 is disabled** 1b = Low-current OLD on half-bridge 7 is enabled
5	HB6_LOLD_EN	R/W	0b	**0b = Low-current OLD on half-bridge 6 is disabled** 1b = Low-current OLD on half-bridge 6 is enabled
4	HB5_LOLD_EN	R/W	0b	**0b = Low-current OLD on half-bridge 5 is disabled** 1b = Low-current OLD on half-bridge 5 is enabled
3	HB4_LOLD_EN	R/W	0b	**0b = Low-current OLD on half-bridge 4 is disabled** 1b = Low-current OLD on half-bridge 4 is enabled
2	HB3_LOLD_EN	R/W	0b	**0b = Low-current OLD on half-bridge 3 is disabled** 1b = Low-current OLD on half-bridge 3 is enabled
1	HB2_LOLD_EN	R/W	0b	**0b = Low-current OLD on half-bridge 2 is disabled** 1b = Low-current OLD on half-bridge 2 is enabled
0	HB1_LOLD_EN	R/W	0b	**0b = Low-current OLD on half-bridge 1 is disabled** 1b = Low-current OLD on half-bridge 1 is enabled

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8.6.2 DRV8908-Q1, DRV8906-Q1 and DRV8904-Q1 Register Maps

表 50. DRV8908-Q1 Register Map

Name	7	6	5	4	3	2	1	0	Type	Address
IC_STAT	Reserved	OTSD	OTW	OLD	OCP	UVLO	OVP	NPOR	R	00h
OCP_STAT_1	HB4_HS_OCP	HB4_LS_OCP	HB3_HS_OCP	HB3_LS_OCP	HB2_HS_OCP	HB2_LS_OCP	HB1_HS_OCP	HB1_LS_OCP	R	01h
OCP_STAT_2	HB8_HS_OCP	HB8_LS_OCP	HB7_HS_OCP	HB7_LS_OCP	HB6_HS_OCP	HB6_LS_OCP	HB5_HS_OCP	HB5_LS_OCP	R	02h
OCP_STAT_3	Reserved								R	03h
OLD_STAT_1	HB4_HS_OLD	HB4_LS_OLD	HB3_HS_OLD	HB3_LS_OLD	HB2_HS_OLD	HB2_LS_OLD	HB1_HS_OLD	HB1_LS_OLD	R	04h
OLD_STAT_2	HB8_HS_OLD	HB8_LS_OLD	HB7_HS_OLD	HB7_LS_OLD	HB6_HS_OLD	HB6_LS_OLD	HB5_HS_OLD	HB5_LS_OLD	R	05h
OLD_STAT_3	Reserved								R	06h
CONFIG_CTRL	POLD_EN	IC_ID			OCP_REP	OTW_REP	EXT_OVP	CLR_FLT	RW	07h
OP_CTRL_1	HB4_HS_EN	HB4_LS_EN	HB3_HS_EN	HB3_LS_EN	HB2_HS_EN	HB2_LS_EN	HB1_HS_EN	HB1_LS_EN	RW	08h
OP_CTRL_2	HB8_HS_EN	HB8_LS_EN	HB7_HS_EN	HB7_LS_EN	HB6_HS_EN	HB6_LS_EN	HB5_HS_EN	HB5_LS_EN	RW	09h
OP_CTRL_3	Reserved								RW	0Ah
PWM_CTRL_1	HB8_PWM	HB7_PWM	HB6_PWM	HB5_PWM	HB4_PWM	HB3_PWM	HB2_PWM	HB1_PWM	RW	0Bh
PWM_CTRL_2	PWM_CH8_DIS	PWM_CH7_DIS	PWM_CH6_DIS	PWM_CH5_DIS	PWM_CH4_DIS	PWM_CH3_DIS	PWM_CH2_DIS	PWM_CH1_DIS	RW	0Ch
FW_CTRL_1	HB8_FW	HB7_FW	HB6_FW	HB5_FW	HB4_FW	HB3_FW	HB2_FW	HB1_FW	RW	0Dh
FW_CTRL_2	Reserved								RW	0Eh
PWM_MAP_CTRL_1	Reserved		HB2_PWM_MAP			HB1_PWM_MAP			RW	0Fh
PWM_MAP_CTRL_2(1)	Reserved		HB4_PWM_MAP			HB3_PWM_MAP			RW	10h(1)
PWM_MAP_CTRL_3	Reserved		HB6_PWM_MAP			HB5_PWM_MAP			RW	11h
PWM_MAP_CTRL_4	Reserved		HB8_PWM_MAP			HB7_PWM_MAP			RW	12h
PWM_FREQ_CTRL _1	PWM_CH4_FREQ		PWM_CH3_FREQ		PWM_CH2_FREQ		PWM_CH1_FREQ		RW	13h
PWM_FREQ_CTRL _2	PWM_CH8_FREQ		PWM_CH7_FREQ		PWM_CH6_FREQ		PWM_CH5_FREQ		RW	14h
PWM_DUTY_CTRL_1	PWM_DUTY_CH1								RW	15h
PWM_DUTY_CTRL_2	PWM_DUTY_CH2								RW	16h
PWM_DUTY_CTRL_3	PWM_DUTY_CH3								RW	17h
PWM_DUTY_CTRL_4	PWM_DUTY_CH4								RW	18h
PWM_DUTY_CTRL_5	PWM_DUTY_CH5								RW	19h
PWM_DUTY_CTRL_6	PWM_DUTY_CH6								RW	1Ah
PWM_DUTY_CTRL_7	PWM_DUTY_CH7								RW	1Bh
PWM_DUTY_CTRL_8	PWM_DUTY_CH8								RW	1Ch
SR_CTRL_1	HB8_SR	HB7_SR	HB6_SR	HB5_SR	HB4_SR	HB3_SR	HB2_SR	HB1_SR	RW	1Dh

(1) After this register address, the register functions are similar among DRV8908-Q1, DRV8906-Q1, and DRV8904-Q1. However, DRV8912-Q1 and DRV8910-Q1 have different functions for these addresses.

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表 50. DRV8908-Q1 Register Map (continued)

Name	7	6	5	4	3	2	1	0	Type	Address
SR_CTRL_2	Reserved								RW	1Eh
OLD_CTRL_1	HB8_OLD_DIS	HB7_OLD_DIS	HB6_OLD_DIS	HB5_OLD_DIS	HB4_OLD_DIS	HB3_OLD_DIS	HB2_OLD_DIS	HB1_OLD_DIS	RW	1Fh
OLD_CTRL_2	OLD_REP	OLD_OP	PL_MODE_EN		Reserved				RW	20h
OLD_CTRL_3	OCP_DEG			OLD_NEG_EN	Reserved				RW	21h
OLD_CTRL_4	HB8_LOLD_EN	HB7_LOLD_EN	HB6_LOLD_EN	HB5_LOLD_EN	HB4_LOLD_EN	HB3_LOLD_EN	HB2_LOLD_EN	HB1_LOLD_EN	RW	22h
OLD_CTRL_5	HB8_POLD_EN	HB7_POLD_EN	HB6_POLD_EN	HB5_POLD_EN	HB4_POLD_EN	HB3_POLD_EN	HB2_POLD_EN	HB1_POLD_EN	RW	23h
OLD_CTRL_6	HB8_VM_POLD	HB7_VM_POLD	HB6_VM_POLD	HB5_VM_POLD	HB4_VM_POLD	HB3_VM_POLD	HB2_VM_POLD	HB1_VM_POLD	RW	24h

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表 51. DRV8906-Q1 Register Map

Name	7	6	5	4	3	2	1	0	Type	Address
IC_STAT	Reserved	OTSD	OTW	OLD	OCP	UVLO	OVP	NPOR	R	00h
OCP_STAT_1	HB4_HS_OCP	HB4_LS_OCP	HB3_HS_OCP	HB3_LS_OCP	HB2_HS_OCP	HB2_LS_OCP	HB1_HS_OCP	HB1_LS_OCP	R	01h
OCP_STAT_2	Reserved				HB6_HS_OCP	HB6_LS_OCP	HB5_HS_OCP	HB5_LS_OCP	R	02h
OCP_STAT_3	Reserved								R	03h
OLD_STAT_1	HB4_HS_OLD	HB4_LS_OLD	HB3_HS_OLD	HB3_LS_OLD	HB2_HS_OLD	HB2_LS_OLD	HB1_HS_OLD	HB1_LS_OLD	R	04h
OLD_STAT_2	Reserved				HB6_HS_OLD	HB6_LS_OLD	HB5_HS_OLD	HB5_LS_OLD	R	05h
OLD_STAT_3	Reserved								R	06h
CONFIG_CTRL	POLD_EN	IC_ID			OCP_REP	OTW_REP	EXT_OVP	CLR_FLT	RW	07h
OP_CTRL_1	HB4_HS_EN	HB4_LS_EN	HB3_HS_EN	HB3_LS_EN	HB2_HS_EN	HB2_LS_EN	HB1_HS_EN	HB1_LS_EN	RW	08h
OP_CTRL_2	Reserved				HB6_HS_EN	HB6_LS_EN	HB5_HS_EN	HB5_LS_EN	RW	09h
OP_CTRL_3	Reserved								RW	0Ah
PWM_CTRL_1	Reserved		HB6_PWM	HB5_PWM	HB4_PWM	HB3_PWM	HB2_PWM	HB1_PWM	RW	0Bh
PWM_CTRL_2	Reserved		PWM_CH6_DIS	PWM_CH5_DIS	PWM_CH4_DIS	PWM_CH3_DIS	PWM_CH2_DIS	PWM_CH1_DIS	RW	0Ch
FW_CTRL_1	Reserved		HB6_FW	HB5_FW	HB4_FW	HB3_FW	HB2_FW	HB1_FW	RW	0Dh
FW_CTRL_2	Reserved								RW	0Eh
PWM_MAP_CTRL_1	Reserved		HB2_PWM_MAP			HB1_PWM_MAP			RW	0Fh
PWM_MAP_CTRL_2(1)	Reserved		HB4_PWM_MAP			HB3_PWM_MAP			RW	10h(1)
PWM_MAP_CTRL_3	Reserved		HB6_PWM_MAP			HB5_PWM_MAP			RW	11h
PWM_MAP_CTRL_4	Reserved								RW	12h
PWM_FREQ_CTRL _1	PWM_CH4_FREQ		PWM_CH3_FREQ		PWM_CH2_FREQ		PWM_CH1_FREQ		RW	13h
PWM_FREQ_CTRL _2	Reserved				PWM_CH6_FREQ		PWM_CH5_FREQ		RW	14h
PWM_DUTY_CTRL_1	PWM_DUTY_CH1								RW	15h
PWM_DUTY_CTRL_2	PWM_DUTY_CH2								RW	16h
PWM_DUTY_CTRL_3	PWM_DUTY_CH3								RW	17h
PWM_DUTY_CTRL_4	PWM_DUTY_CH4								RW	18h
PWM_DUTY_CTRL_5	PWM_DUTY_CH5								RW	19h
PWM_DUTY_CTRL_6	PWM_DUTY_CH6								RW	1Ah
PWM_DUTY_CTRL_7	Reserved								RW	1Bh
PWM_DUTY_CTRL_8	Reserved								RW	1Ch
SR_CTRL_1	Reserved		HB6_SR	HB5_SR	HB4_SR	HB3_SR	HB2_SR	HB1_SR	RW	1Dh
SR_CTRL_2	Reserved								RW	1Eh
OLD_CTRL_1	Reserved		HB6_OLD_DIS	HB5_OLD_DIS	HB4_OLD_DIS	HB3_OLD_DIS	HB2_OLD_DIS	HB1_OLD_DIS	RW	1Fh

(1) After this register address, the register functions are similar among DRV8908-Q1, DRV8906-Q1, and DRV8904-Q1. However, DRV8912-Q1 and DRV8910-Q1 have different functions for these addresses.

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表 51. DRV8906-Q1 Register Map (continued)

Name	7	6	5	4	3	2	1	0	Type	Address
OLD_CTRL_2	OLD_REP	OLD_OP	PL_MODE_EN		Reserved				RW	20h
OLD_CTRL_3	OCP_DEG			OLD_NEG_EN	Reserved				RW	21h
OLD_CTRL_4	Reserved		HB6_LOLD_EN	HB5_LOLD_EN	HB4_LOLD_EN	HB3_LOLD_EN	HB2_LOLD_EN	HB1_LOLD_EN	RW	22h
OLD_CTRL_5	Reserved		HB6_POLD_EN	HB5_POLD_EN	HB4_POLD_EN	HB3_POLD_EN	HB2_POLD_EN	HB1_POLD_EN	RW	23h
OLD_CTRL_6	Reserved		HB6_VM_POLD	HB5_VM_POLD	HB4_VM_POLD	HB3_VM_POLD	HB2_VM_POLD	HB1_VM_POLD	RW	24h

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表 52. DRV8904-Q1 Register Map

Name	7	6	5	4	3	2	1	0	Type	Address
IC_STAT	Reserved	OTSD	OTW	OLD	OCP	UVLO	OVP	NPOR	R	00h
OCP_STAT_1	HB4_HS_OCP	HB4_LS_OCP	HB3_HS_OCP	HB3_LS_OCP	HB2_HS_OCP	HB2_LS_OCP	HB1_HS_OCP	HB1_LS_OCP	R	01h
OCP_STAT_2	Reserved								R	02h
OCP_STAT_3	Reserved								R	03h
OLD_STAT_1	HB4_HS_OLD	HB4_LS_OLD	HB3_HS_OLD	HB3_LS_OLD	HB2_HS_OLD	HB2_LS_OLD	HB1_HS_OLD	HB1_LS_OLD	R	04h
OLD_STAT_2	Reserved								R	05h
OLD_STAT_3	Reserved								R	06h
CONFIG_CTRL	POLD_EN	IC_ID			OCP_REP	OTW_REP	EXT_OVP	CLR_FLT	RW	07h
OP_CTRL_1	HB4_HS_EN	HB4_LS_EN	HB3_HS_EN	HB3_LS_EN	HB2_HS_EN	HB2_LS_EN	HB1_HS_EN	HB1_LS_EN	RW	08h
OP_CTRL_2	Reserved								RW	09h
OP_CTRL_3	Reserved								RW	0Ah
PWM_CTRL_1	Reserved				HB4_PWM	HB3_PWM	HB2_PWM	HB1_PWM	RW	0Bh
PWM_CTRL_2	Reserved				PWM_CH4_DIS	PWM_CH3_DIS	PWM_CH2_DIS	PWM_CH1_DIS	RW	0Ch
FW_CTRL_1	Reserved				HB4_FW	HB3_FW	HB2_FW	HB1_FW	RW	0Dh
FW_CTRL_2	Reserved								RW	0Eh
PWM_MAP_CTRL_1	Reserved		HB2_PWM_MAP			HB1_PWM_MAP			RW	0Fh
PWM_MAP_CTRL_2(1)	Reserved		HB4_PWM_MAP			HB3_PWM_MAP			RW	10h(1)
PWM_MAP_CTRL_3	Reserved								RW	11h
PWM_MAP_CTRL_4	Reserved								RW	12h
PWM_FREQ_CTRL _1	PWM_CH4_FREQ		PWM_CH3_FREQ		PWM_CH2_FREQ		PWM_CH1_FREQ		RW	13h
PWM_FREQ_CTRL _2	Reserved								RW	14h
PWM_DUTY_CTRL_1	PWM_DUTY_CH1								RW	15h
PWM_DUTY_CTRL_2	PWM_DUTY_CH2								RW	16h
PWM_DUTY_CTRL_3	PWM_DUTY_CH3								RW	17h
PWM_DUTY_CTRL_4	PWM_DUTY_CH4								RW	18h
PWM_DUTY_CTRL_5	Reserved								RW	19h
PWM_DUTY_CTRL_6	Reserved								RW	1Ah
PWM_DUTY_CTRL_7	Reserved								RW	1Bh
PWM_DUTY_CTRL_8	Reserved								RW	1Ch
SR_CTRL_1	Reserved				HB4_SR	HB3_SR	HB2_SR	HB1_SR	RW	1Dh
SR_CTRL_2	Reserved								RW	1Eh
OLD_CTRL_1	Reserved				HB4_OLD_DIS	HB3_OLD_DIS	HB2_OLD_DIS	HB1_OLD_DIS	RW	1Fh

(1) After this register address, the register functions are similar among DRV8908-Q1, DRV8906-Q1, and DRV8904-Q1. However, DRV8912-Q1 and DRV8910-Q1 have different functions for these addresses.

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表 52. DRV8904-Q1 Register Map (continued)

Name	7	6	5	4	3	2	1	0	Type	Address
OLD_CTRL_2	OLD_REP	OLD_OP	PL_MODE_EN		Reserved				RW	20h
OLD_CTRL_3	OCP_DEG			OLD_NEG_EN	Reserved				RW	21h
OLD_CTRL_4	Reserved				HB4_LOLD_EN	HB3_LOLD_EN	HB2_LOLD_EN	HB1_LOLD_EN	RW	22h
OLD_CTRL_5	Reserved				HB4_POLD_EN	HB3_POLD_EN	HB2_POLD_EN	HB1_POLD_EN	RW	23h
OLD_CTRL_6	Reserved				HB4_VM_POLD	HB3_VM_POLD	HB2_VM_POLD	HB1_VM_POLD	RW	24h

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8.6.2.1 Status Registers

The status registers are used to report warning and fault conditions. The status registers are read-only registers.

表 53 lists the memory-mapped registers for the status registers. All register offset addresses not listed in 表 53 should be considered as reserved locations and the register contents should not be modified.

表 53. Status Registers Summary Table

Address	Register Name	Section
0x00	IC Status	Go
0x01	Overcurrent Protection (OCP) Status 1	Go
0x02	Overcurrent Protection (OCP) Status 2	Go
0x03	Overcurrent Protection (OCP) Status 3	Go
0x04	Open-Load Detect (OLD) Status 1	Go
0x05	Open-Load Detect (OLD) Status 2	Go
0x06	Open-Load Detect (OLD) Status 3	Go

8.6.2.1.1 IC Status (IC_STAT) Register (Address = 0x00) [reset = 0x00]

The IC status (IC_STAT) register is shown in 図 97 and described in 表 54.

Register access type: Read only

図 97. IC Status Register

7	6	5	4	3	2	1	0
Reserved	OTSD	OTW	OLD	OCP	UVLO	OVP	NPOR
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 54. IC Status Register Field Descriptions

Bit	Field	Type	Default	Description
7	Reserved	R	0b	Reserved
6	OTSD	R	0b	**0b = No overtemperature shutdown is detected** 1b = Overcurrent condition is detected
5	OTW	R	0b	**0b = No overtemperature warning is detected** 1b = Overcurrent condition is detected
4	OLD	R	0b	**0b = No open-load condition is detected** 1b = Open-load condition is detected
3	OCP	R	0b	**0b = No overcurrent condition is detected** 1b = Overcurrent condition is detected
2	UVLO	R	0b	**0b = No undervoltage lock-out condition is detected** 1b = Under-voltage lock-out condition condition is detected
1	OVP	R	0b	**0b = No overvoltage condition is detected** 1b = Overvoltage condition is detected
0	NPOR	R	0b	**0b = Power-on-reset condition is detected** 1b = No power-on-reset condition is detected

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8.6.2.1.2 *Overcurrent Protection (OCP) Status 1 (OCP_STAT_1) Register (Address = 0x01) [reset = 0x00]*

The overcurrent protection (OCP) status 1 register is shown in 図 98 and described in 表 55.

Register access type: Read only

図 98. Overcurrent Protection (OCP) Status 1 Register

7	6	5	4	3	2	1	0
HB4_HS_OCP	HB4_LS_OCP	HB3_HS_OCP	HB3_LS_OCP	HB2_HS_OCP	HB2_LS_OCP	HB1_HS_OCP	HB1_LS_OCP
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 55. Overcurrent Protection (OCP) Status 1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	HB4_HS_OCP	R	0b	**0b = No overcurrent detected on high-side switch of half-bridge 4** 1b = Overcurrent detected on high-side switch of half-bridge 4
6	HB4_LS_OCP	R	0b	**0b = No overcurrent detected on low-side switch of half-bridge 4** 1b = Overcurrent detected on low-side switch of half-bridge 4
5	HB3_HS_OCP	R	0b	**0b = No overcurrent detected on high-side switch of half-bridge 3** 1b = Overcurrent detected on high-side switch of half-bridge 3
4	HB3_LS_OCP	R	0b	**0b = No overcurrent detected on low-side switch of half-bridge 3** 1b = Overcurrent detected on low-side switch of half-bridge 3
3	HB2_HS_OCP	R	0b	**0b = No overcurrent detected on high-side switch of half-bridge 2** 1b = Overcurrent detected on high-side switch of half-bridge 2
2	HB2_LS_OCP	R	0b	**0b = No overcurrent detected on low-side switch of half-bridge 2** 1b = Overcurrent detected on low-side switch of half-bridge 2
1	HB1_HS_OCP	R	0b	**0b = No overcurrent detected on high-side switch of half-bridge 1** 1b = Overcurrent detected on high-side switch of half-bridge 1
0	HB1_LS_OCP	R	0b	**0b = No overcurrent detected on low-side switch of half-bridge 1** 1b = Overcurrent detected on low-side switch of half-bridge 1

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8.6.2.1.3 *Overcurrent Protection (OCP) Status 2 (OCP_STAT_2) Register (Address = 0x02) [reset = 0x00]*

The overcurrent protection (OCP) status 2 register is shown in 図 99 and described in 表 56.

Register access type: Read only

図 99. Overcurrent Protection (OCP) Status 2 Register

7	6	5	4	3	2	1	0
HB8_HS_OCP	HB8_LS_OCP	HB7_HS_OCP	HB7_LS_OCP	HB6_HS_OCP	HB6_LS_OCP	HB5_HS_OCP	HB5_LS_OCP
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 56. Overcurrent Protection (OCP) Status 2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	HB8_HS_OCP	R	0b	**0b = No overcurrent detected on high-side switch of half-bridge 8** 1b = Overcurrent detected on high-side switch of half-bridge 8
6	HB8_LS_OCP	R	0b	**0b = No overcurrent detected on low-side switch of half-bridge 8** 1b = Overcurrent detected on low-side switch of half-bridge 8
5	HB7_HS_OCP	R	0b	**0b = No overcurrent detected on high-side switch of half-bridge 7** 1b = Overcurrent detected on high-side switch of half-bridge 7
4	HB7_LS_OCP	R	0b	**0b = No overcurrent detected on low-side switch of half-bridge 7** 1b = Overcurrent detected on low-side switch of half-bridge 7
3	HB6_HS_OCP	R	0b	**0b = No overcurrent detected on high-side switch of half-bridge 6** 1b = Overcurrent detected on high-side switch of half-bridge 6
2	HB6_LS_OCP	R	0b	**0b = No overcurrent detected on low-side switch of half-bridge 6** 1b = Overcurrent detected on low-side switch of half-bridge 6
1	HB5_HS_OCP	R	0b	**0b = No overcurrent detected on high-side switch of half-bridge 5** 1b = Overcurrent detected on high-side switch of half-bridge 5
0	HB5_LS_OCP	R	0b	**0b = No overcurrent detected on low-side switch of half-bridge 5** 1b = Overcurrent detected on low-side switch of half-bridge 5

8.6.2.1.4 *Overcurrent Protection (OCP) Status 3 (OCP_STAT_3) Register (Address = 0x03) [reset = 0x00]*

The overcurrent protection (OCP) status 3 register is shown in 図 100 and described in 図 100.

Register access type: Read only

図 100. Overcurrent Protection (OCP) Status 3 Register

7	6	5	4	3	2	1	0
Reserved							
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 57. Overcurrent Protection (OCP) Status 3 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	Reserved	R	0b	Reserved.

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8.6.2.1.5 *Open-Load Detect (OLD) Status 1 (OLD_STAT_1) Register (Address = 0x04) [reset = 0x00]*

The open-load detect (OLD) status 1 register is shown in 図 101 and described in 表 58.

Register access type: Read only

図 101. Open-Load Detect (OLD) Status 1 Register

7	6	5	4	3	2	1	0
HB4_HS_OLD	HB4_LS_OLD	HB3_HS_OLD	HB3_LS_OLD	HB2_HS_OLD	HB2_LS_OLD	HB1_HS_OLD	HB1_LS_OLD
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 58. Open-Load Detect (OLD) Status 1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	HB4_HS_OLD	R	0b	**0b = No open load detected on high-side switch of half-bridge 4** 1b = Open load detected on high-side switch of half-bridge 4
6	HB4_LS_OLD	R	0b	**0b = No open load detected on low-side switch of half-bridge 4** 1b = Open load detected on low-side switch of half-bridge 4
5	HB3_HS_OLD	R	0b	**0b = No open load detected on high-side switch of half-bridge 3** 1b = Open load detected on high-side switch of half-bridge 3
4	HB3_LS_OLD	R	0b	**0b = No open load detected on low-side switch of half-bridge 3** 1b = Open load detected on low-side switch of half-bridge 3
3	HB2_HS_OLD	R	0b	**0b = No open load detected on high-side switch of half-bridge 2** 1b = Open load detected on high-side switch of half-bridge 2
2	HB2_LS_OLD	R	0b	**0b = No open load detected on low-side switch of half-bridge 2** 1b = Open load detected on low-side switch of half-bridge 2
1	HB1_HS_OLD	R	0b	**0b = No open load detected on high-side switch of half-bridge 1** 1b = Open load detected on high-side switch of half-bridge 1
0	HB1_LS_OLD	R	0b	**0b = No open load detected on low-side switch of half-bridge 1** 1b = Open load detected on low-side switch of half-bridge 1

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8.6.2.1.6 *Open-Load Detect (OLD) Status 2 (OLD_STAT_2) Register (Address = 0x05) [reset = 0x00]*

The open-load detect (OLD) status 2 register is shown in 図 102 and described in 表 59.

Register access type: Read only

図 102. Open-Load Detect (OLD) Status 2 Register

7	6	5	4	3	2	1	0
HB8_HS_OLD	HB8_LS_OLD	HB7_HS_OLD	HB7_LS_OLD	HB6_HS_OLD	HB6_LS_OLD	HB5_HS_OLD	HB5_LS_OLD
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 59. Open-Load Detect (OLD) Status 2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	HB8_HS_OLD	R	0b	**0b = No open load detected on high-side switch of half-bridge 8** 1b = Open load detected on high-side switch of half-bridge 8
6	HB8_LS_OLD	R	0b	**0b = No open load detected on low-side switch of half-bridge 8** 1b = Open load detected on low-side switch of half-bridge 8
5	HB7_HS_OLD	R	0b	**0b = No open load detected on high-side switch of half-bridge 7** 1b = Open load detected on high-side switch of half-bridge 7
4	HB7_LS_OLD	R	0b	**0b = No open load detected on low-side switch of half-bridge 7** 1b = Open load detected on low-side switch of half-bridge 7
3	HB6_HS_OLD	R	0b	**0b = No open load detected on high-side switch of half-bridge 6** 1b = Open load detected on high-side switch of half-bridge 6
2	HB6_LS_OLD	R	0b	**0b = No open load detected on low-side switch of half-bridge 6** 1b = Open load detected on low-side switch of half-bridge 6
1	HB5_HS_OLD	R	0b	**0b = No open load detected on high-side switch of half-bridge 5** 1b = Open load detected on high-side switch of half-bridge 5
0	HB5_LS_OLD	R	0b	**0b = No open load detected on low-side switch of half-bridge 5** 1b = Open load detected on low-side switch of half-bridge 5

8.6.2.1.7 *Open-Load Detect (OLD) Status 3 (OLD_STAT_3) Register (Address = 0x06) [reset = 0x00]*

The open-load detect (OLD) status 3 register is shown in 図 103 and described in 表 60.

Register access type: Read only

図 103. Open-Load Detect (OLD) Status 3 Register

7	6	5	4	3	2	1	0
Reserved							
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 60. Open-Load Detect (OLD) Status 3 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	Reserved	R	0b	Reserved.

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8.6.2.2 Control Registers

The control registers are used to configure the device. The control registers are read and write capable.

表 61 lists the memory-mapped registers for the control registers. All register offset addresses not listed in 表 61 should be considered as reserved locations and the register contents should not be modified.

表 61. Control Registers Summary Table

Address	Register Name	Section
0x07	Configuration Register	Go
0x08	Operation Control 1 Register	Go
0x09	Operation Control 2 Register	Go
0x0A	Operation Control 3 Register	Go
0x0B	PWM Control 1 Register	Go
0x0C	PWM Control 2 Register	Go
0x0D	Free-Wheeling Control 1 Register	Go
0x0E	Free-Wheeling Control 2 Register	Go
0x0F	PWM Map Control 1 Register	Go
0x10	PWM Map Control 2 Register	Go
0x11	PWM Map Control 3 Register	Go
0x12	PWM Map Control 4 Register	Go
0x13	PWM Frequency Control 1 Register	Go
0x14	PWM Frequency Control 2 Register	Go
0x15	PWM Duty Control Channel 1 Register	Go
0x16	PWM Duty Control Channel 2 Register	Go
0x17	PWM Duty Control Channel 3 Register	Go
0x18	PWM Duty Control Channel 4 Register	Go
0x19	PWM Duty Control Channel 5 Register	Go
0x1A	PWM Duty Control Channel 6 Register	Go
0x1B	PWM Duty Control Channel 7 Register	Go
0x1C	PWM Duty Control Channel 8 Register	Go
0x1D	Slew Rate Control 1 Register	Go
0x1E	Slew Rate Control 2 Register	Go
0x1F	Open-Load Detect (OLD) Control 1 Register	Go
0x20	Open-Load Detect (OLD) Control 2 Register	Go
0x21	Open-Load Detect (OLD) Control 3 Register	Go
0x22	Open-Load Detect (OLD) Control 4 Register	Go
0x23	Open-Load Detect (OLD) Control 5 Register	Go
0x24	Open-Load Detect (OLD) Control 6 Register	Go

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8.6.2.2.1 *Configuration (CONFIG_CTRL) Register (Address = 0x07) [reset = 0x00]*

The configuration register is shown in 図 104 and described in 表 62.

Register access type: Read/Write

図 104. Configuration Register

7	6	5	4	3	2	1	0
POLD_EN		IC_ID		OCP_REP	OTW_REP	EXT_OVP	CLR_FLT
R/W-0b	R-Xb	R-Xb	R-Xb	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 62. Configuration Register Field Descriptions

Bit	Field	Type	Default	Description
7	POLD_EN	R/W	0b	**0b = Passive OLD is disabled** 1b = Passive OLD is enabled
6-4	IC_ID	R	XXXb	000b = Device connected is DRV8912-Q1 (12 Channel Device) 001b = Device connected is DRV8910-Q1 (10 Channel Device) 010b = Device connected is DRV8908-Q1 (8 Channel Device) 011b = Device connected is DRV8906-Q1 (6 Channel Device) 100b = Device connected is DRV8904-Q1 (4 Channel Device) 101b = Reserved 110b = Reserved 111b = Reserved
3	OCP_REP	R/W	0b	**0b = Overcurrent condition is reported in nFAULT pin** 1b = Overcurrent condition warning is not reported on the nFAULT pin
2	OTW_REP	R/W	0b	**0b = Overtemperature warning is not reported in nFAULT pin** 1b = Overtemperature warning is reported on the nFAULT pin
1	EXT_OVP	R/W	0b	**0b = Overvoltage protection threshold is at 21 V** 1b = Overvoltage protection threshold is at 33 V
0	CLR_FLT	R/W	0b	**0b = Faults not cleared** 1b = Clear all faults

注

CLR_FLT bit is an auto-clear bit and will always read '0'.

8.6.2.2.2 *Operation Control 1 (OP_CTRL_1) Register (Address = 0x08) [reset = 0x00]*

The operation control 1 register is shown in 図 105 and described in 表 63.

Register access type: Read/Write

図 105. Operation Control 1 Register

7	6	5	4	3	2	1	0
HB4_HS_EN	HB4_LS_EN	HB3_HS_EN	HB3_LS_EN	HB2_HS_EN	HB2_LS_EN	HB1_HS_EN	HB1_LS_EN
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 63. Operation Control 1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	HB4_HS_EN	R/W	0b	**0b = Half-bridge 4 high-side switch is disabled** 1b = Half-bridge 4 high-side switch is enabled
6	HB4_LS_EN	R/W	0b	**0b = Half-bridge 4 low-side switch is disabled** 1b = Half-bridge 4 low-side switch is enabled
5	HB3_HS_EN	R/W	0b	**0b = Half-bridge 3 high-side switch is disabled** 1b = Half-bridge 3 high-side switch is enabled
4	HB3_LS_EN	R/W	0b	**0b = Half-bridge 3 low-side switch is disabled** 1b = Half-bridge 3 low-side switch is enabled
3	HB2_HS_EN	R/W	0b	**0b = Half-bridge 2 high-side switch is disabled** 1b = Half-bridge 2 high-side switch is enabled
2	HB2_LS_EN	R/W	0b	**0b = Half-bridge 2 low-side switch is disabled** 1b = Half-bridge 2 low-side switch is enabled
1	HB1_HS_EN	R/W	0b	**0b = Half-bridge 1 high-side switch is disabled** 1b = Half-bridge 1 high-side switch is enabled
0	HB1_LS_EN	R/W	0b	**0b = Half-bridge 1 low-side switch is disabled** 1b = Half-bridge 1 low-side switch is enabled

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8.6.2.2.3 *Operation Control 2 (OP_CTRL_2) Register (Address = 0x09) [reset = 0x00]*

The operation control 2 register is shown in 図 106 and described in 表 64.

Register access type: Read/Write

図 106. Operation Control 2 Register

7	6	5	4	3	2	1	0
HB8_HS_EN	HB8_LS_EN	HB7_HS_EN	HB7_LS_EN	HB6_HS_EN	HB6_LS_EN	HB5_HS_EN	HB5_LS_EN
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 64. Operation Control 2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	HB8_HS_EN	R/W	0b	**0b = Half-bridge 8 high-side switch is disabled** 1b = Half-bridge 8 high-side switch is enabled
6	HB8_LS_EN	R/W	0b	**0b = Half-bridge 8 low-side switch is disabled** 1b = Half-bridge 8 low-side switch is enabled
5	HB7_HS_EN	R/W	0b	**0b = Half-bridge 7 high-side switch is disabled** 1b = Half-bridge 7 high-side switch is enabled
4	HB7_LS_EN	R/W	0b	**0b = Half-bridge 7 low-side switch is disabled** 1b = Half-bridge 7 low-side switch is enabled
3	HB6_HS_EN	R/W	0b	**0b = Half-bridge 6 high-side switch is disabled** 1b = Half-bridge 6 high-side switch is enabled
2	HB6_LS_EN	R/W	0b	**0b = Half-bridge 6 low-side switch is disabled** 1b = Half-bridge 6 low-side switch is enabled
1	HB5_HS_EN	R/W	0b	**0b = Half-bridge 5 high-side switch is disabled** 1b = Half-bridge 5 high-side switch is enabled
0	HB5_LS_EN	R/W	0b	**0b = Half-bridge 5 low-side switch is disabled** 1b = Half-bridge 5 low-side switch is enabled

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8.6.2.2.4 *Operation Control 3 (OP_CTRL_3) Register (Address = 0x0A) [reset = 0x00]*

The operation control 3 register is shown in 図 107 and described in 表 65.

Register access type: Read

図 107. Operation Control 3 Register

7	6	5	4	3	2	1	0
Reserved							
R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b	R-0b

表 65. Operation Control 3 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	Reserved	R	0b	Reserved.

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8.6.2.2.5 *PWM Control 1 (PWM_CTRL_1) Register (Address = 0x0B) [reset = 0x00]*

The PWM control 1 register is shown in 図 108 and described in 表 66.

Register access type: Read/Write

図 108. PWM Control 1 Register

7	6	5	4	3	2	1	0
HB8_PWM	HB7_PWM	HB6_PWM	HB5_PWM	HB4_PWM	HB3_PWM	HB2_PWM	HB1_PWM
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 66. PWM Control 1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	HB8_PWM	R/W	0b	**0b = Half-bridge 8 is operating in continuous mode** 1b = Half-bridge 8 is operating in PWM mode
6	HB7_PWM	R/W	0b	**0b = Half-bridge 7 is operating in continuous mode** 1b = Half-bridge 7is operating in PWM mode
5	HB6_PWM	R/W	0b	**0b = Half-bridge 6 is operating in continuous mode** 1b = Half-bridge 6 is operating in PWM mode
4	HB5_PWM	R/W	0b	**0b = Half-bridge 5 is operating in continuous mode** 1b = Half-bridge 5 is operating in PWM mode
3	HB4_PWM	R/W	0b	**0b = Half-bridge 4 is operating in continuous mode** 1b = Half-bridge 4 is operating in PWM mode
2	HB3_PWM	R/W	0b	**0b = Half-bridge 3 is operating in continuous mode** 1b = Half-bridge 3 is operating in PWM mode
1	HB2_PWM	R/W	0b	**0b = Half-bridge 2 is operating in continuous mode** 1b = Half-bridge 2 is operating in PWM mode
0	HB1_PWM	R/W	0b	**0b = Half-bridge 1 is operating in continuous mode** 1b = Half-bridge 1 is operating in PWM mode

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8.6.2.2.6 *PWM Control 2 (PWM_CTRL_2) Register (Address = 0x0C) [reset = 0x00]*

The PWM control 2 register is shown in 図 109 and described in 表 67.

Register access type: Read/Write

図 109. PWM Control 2 Register

7	6	5	4	3	2	1	0
PWM_CH8_DIS	PWM_CH7_DIS	PWM_CH6_DIS	PWM_CH5_DIS	PWM_CH4_DIS	PWM_CH3_DIS	PWM_CH2_DIS	PWM_CH1_DIS
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 67. PWM Control 2 Register Field Descriptions

Bit	Field	Type	Default	Description
7	PWM_CH8_DIS	R/W	0b	**0b = PWM Generator-8 is enabled** 1b = PWM Generator-8 is disabled
6	PWM_CH7_DIS	R/W	0b	**0b = PWM Generator-7 is enabled** 1b = PWM Generator-7 is disabled
5	PWM_CH6_DIS	R/W	0b	**0b = PWM Generator-6 is enabled** 1b = PWM Generator-6 is disabled
4	PWM_CH5_DIS	R/W	0b	**0b = PWM Generator-5 is enabled** 1b = PWM Generator-5 is disabled
3	PWM_CH4_DIS	R/W	0b	**0b = PWM Generator-4 is enabled** 1b = PWM Generator-4 is disabled
2	PWM_CH3_DIS	R/W	0b	**0b = PWM Generator-3 is enabled** 1b = PWM Generator-3 is disabled
1	PWM_CH2_DIS	R/W	0b	**0b = PWM Generator-2 is enabled** 1b = PWM Generator-2 is disabled
0	PWM_CH1_DIS	R/W	0b	**0b = PWM Generator-1 is enabled** 1b = PWM Generator-1 is disabled

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8.6.2.2.7 *Free-Wheeling Control 1 (FW_CTRL_1) Register (Address = 0x0D) [reset = 0x00]*

The free-wheeling control 1 register is shown in 図 110 and described in 表 68.

Register access type: Read/Write

図 110. Free-Wheeling Control 1 Register

7	6	5	4	3	2	1	0
HB8_FW	HB7_FW	HB6_FW	HB5_FW	HB4_FW	HB3_FW	HB2_FW	HB1_FW
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 68. Free-Wheeling Control 1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	HB8_FW	R/W	0b	**0b = Passive free-wheeling on half-bridge 8 is enabled** 1b = Active free-wheeling on half-bridge 8 is enabled
6	HB7_FW	R/W	0b	**0b = Passive free-wheeling on half-bridge 7 is enabled** 1b = Active free-wheeling on half-bridge 7 is enabled
5	HB6_FW	R/W	0b	**0b = Passive free-wheeling on half-bridge 6 is enabled** 1b = Active free-wheeling on half-bridge 6 is enabled
4	HB5_FW	R/W	0b	**0b = Passive free-wheeling on half-bridge 5 is enabled** 1b = Active free-wheeling on half-bridge 5 is enabled
3	HB4_FW	R/W	0b	**0b = Passive free-wheeling on half-bridge 4 is enabled** 1b = Active free-wheeling on half-bridge 4 is enabled
2	HB3_FW	R/W	0b	**0b = Passive free-wheeling on half-bridge 3 is enabled** 1b = Active free-wheeling on half-bridge 3 is enabled
1	HB2_FW	R/W	0b	**0b = Passive free-wheeling on half-bridge 2 is enabled** 1b = Active free-wheeling on half-bridge 2 is enabled
0	HB1_FW	R/W	0b	**0b = Passive free-wheeling on half-bridge 1 is enabled** 1b = Active free-wheeling on half-bridge 1 is enabled

8.6.2.2.8 *Free-Wheeling Control 2 (FW_CTRL_2) Register (Address = 0x0E) [reset = 0x00]*

The free-wheeling control 2 register is shown in 図 111 and described in 表 69.

Register access type: Read/Write

図 111. Free-Wheeling Control 2 Register

7	6	5	4	3	2	1	0
Reserved							
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 69. Free-Wheeling Control 2 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	Reserved	R/W	0000b	Reserved.

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8.6.2.2.9 *PWM Map Control 1 (PWM_MAP_CTRL_1) Register (Address = 0x0F) [reset = 0x00]*

The PWM Map Control 1 register is shown in 図 112 and described in 表 70.

Register access type: Read/Write

図 112. PWM Map Control 1 Register

7	6	5	4	3	2	1	0
Reserved			HB2_PWM_MAP			HB1_PWM_MAP	
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 70. PWM Map Control 1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	Reserved	R	00b	Reserved
3-2	HB2_PWM_MAP	R/W	000b	**00b = HB2 mapped to PWM channel 1** 001b = HB2 mapped to PWM channel 2 010b = HB2 mapped to PWM channel 3 011b = HB2 mapped to PWM channel 4 100b = HB2 mapped to PWM channel 5 101b = HB2 mapped to PWM channel 6 110b = HB mapped to PWM channel 7 111b = HB2 mapped to PWM channel 8
1-0	HB1_PWM_MAP	R/W	000b	**00b = HB1 mapped to PWM channel 1** 001b = HB1 mapped to PWM channel 2 010b = HB1 mapped to PWM channel 3 011b = HB1 mapped to PWM channel 4 100b = HB1 mapped to PWM channel 5 101b = HB1 mapped to PWM channel 6 110b = HB1 mapped to PWM channel 7 111b = HB1 mapped to PWM channel 8

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8.6.2.2.10 *PWM Map Control 2 (PWM_MAP_CTRL_2) Register (Address = 0x10) [reset = 0x00]*

The PWM frequency map control 2 register is shown in 図 113 and described in 表 71.

Register access type: Read/Write

図 113. PWM Map Control 2 Register

7	6	5	4	3	2	1	0
Reserved			HB4_PWM_MAP			HB3_PWM_MAP	
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 71. PWM Map Control 2 Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	Reserved	R	00b	Reserved
3-2	HB4_PWM_MAP	R/W	000b	**00b = HB4 mapped to PWM channel 1** 001b = HB4 mapped to PWM channel 2 010b = HB4 mapped to PWM channel 3 011b = HB4 mapped to PWM channel 4 100b = HB4 mapped to PWM channel 5 101b = HB4 mapped to PWM channel 6 110b = HB4 mapped to PWM channel 7 111b = HB4 mapped to PWM channel 8
1-0	HB3_PWM_MAP	R/W	000b	**00b = HB3 mapped to PWM channel 1** 001b = HB3 mapped to PWM channel 2 010b = HB3 mapped to PWM channel 3 011b = HB3 mapped to PWM channel 4 100b = HB3 mapped to PWM channel 5 101b = HB3 mapped to PWM channel 6 110b = HB3 mapped to PWM channel 7 111b = HB3 mapped to PWM channel 8

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8.6.2.2.11 *PWM Map Control 3 (PWM_MAP_CTRL_3) Register (Address = 0x11) [reset = 0x00]*

The PWM frequency map control 3 register is shown in 図 114 and described in 表 72.

Register access type: Read/Write

図 114. PWM Map Control 3 Register

7	6	5	4	3	2	1	0
Reserved			HB6_PWM_MAP			HB5_PWM_MAP	
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 72. PWM Map Control 3 Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	Reserved	R	00b	Reserved
3-2	HB6_PWM_MAP	R/W	000b	**00b = HB6 mapped to PWM channel 1** 01b = HB6 mapped to PWM channel 2 10b = HB6 mapped to PWM channel 3 11b = HB6 mapped to PWM channel 4 01b = HB6 mapped to PWM channel 5 10b = HB6 mapped to PWM channel 6 11b = HB6 mapped to PWM channel 7 01b = HB6 mapped to PWM channel 8
1-0	HB5_PWM_MAP	R/W	000b	**00b = HB5 mapped to PWM channel 1** 01b = HB5 mapped to PWM channel 2 10b = HB5 mapped to PWM channel 3 11b = HB5 mapped to PWM channel 4 01b = HB5 mapped to PWM channel 5 10b = HB5 mapped to PWM channel 6 11b = HB5 mapped to PWM channel 7 01b = HB5 mapped to PWM channel 8

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8.6.2.2.12 *PWM Map Control 4 (PWM_MAP_CTRL_4) Register (Address = 0x12) [reset = 0x00]*

The PWM frequency map control 4 register is shown in 図 115 and described in 表 73.

Register access type: Read/Write

図 115. PWM Map Control 4 Register

7	6	5	4	3	2	1	0
Reserved			HB8_PWM_MAP			HB7_PWM_MAP	
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 73. PWM Map Control 4 Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	Reserved	R	00b	Reserved
3-2	HB8_PWM_MAP	R/W	000b	**00b = HB8 mapped to PWM channel 1** 01b = HB8 mapped to PWM channel 2 10b = HB8 mapped to PWM channel 3 11b = HB8 mapped to PWM channel 4 01b = HB8 mapped to PWM channel 5 10b = HB8 mapped to PWM channel 6 11b = HB8 mapped to PWM channel 7 01b = HB8 mapped to PWM channel 8
1-0	HB7_PWM_MAP	R/W	000b	**00b = HB7 mapped to PWM channel 1** 01b = HB7 mapped to PWM channel 2 10b = HB7 mapped to PWM channel 3 11b = HB7 mapped to PWM channel 4 01b = HB7 mapped to PWM channel 5 10b = HB7 mapped to PWM channel 6 11b = HB7 mapped to PWM channel 7 01b = HB7 mapped to PWM channel 8

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8.6.2.2.13 *PWM Frequency Control 1 (PWM_FREQ_CTRL_1) Register (Address = 0x13 [reset = 0x00]*

The PWM frequency control register 1 is shown in 図 116 and described in 表 74.

Register access type: Read/Write

図 116. PWM Frequency Control 1 Register

7	6	5	4	3	2	1	0
PWM_CH4_FREQ		PWM_CH3_FREQ		PWM_CH2_FREQ		PWM_CH1_FREQ	
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 74. PWM Frequency Control 1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	PWM_CH4_FREQ	R/W	00b	**00b = PWM frequency is 80 Hz** 01b = PWM frequency is 100 Hz 10b = PWM frequency is 200 Hz 11b = PWM frequency is 2000 Hz
5-4	PWM_CH3_FREQ	R/W	00b	**00b = PWM frequency is 80 Hz** 01b = PWM frequency is 100 Hz 10b = PWM frequency is 200 Hz 11b = PWM frequency is 2000 Hz
3-2	PWM_CH2_FREQ	R/W	00b	**00b = PWM frequency is 80 Hz** 01b = PWM frequency is 100 Hz 10b = PWM frequency is 200 Hz 11b = PWM frequency is 2000 Hz
1-0	PWM_CH1_FREQ	R/W	00b	**00b = PWM frequency is 80 Hz** 01b = PWM frequency is 100 Hz 10b = PWM frequency is 200 Hz 11b = PWM frequency is 2000 Hz

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8.6.2.2.14 *PWM Frequency Control 2 (PWM_FREQ_CTRL_2) Register (Address = 0x14 [reset = 0x00]*

The PWM frequency control register 2 is shown in 図 117 and described in 表 75.

Register access type: Read/Write

図 117. PWM Frequency Control 2 Register

7	6	5	4	3	2	1	0
PWM_CH8_FREQ		PWM_CH7_FREQ		PWM_CH6_FREQ		PWM_CH5_FREQ	
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 75. PWM Frequency Control 2 Register Field Descriptions

Bit	Field	Type	Default	Description
7-6	PWM_CH8_FREQ	R/W	00b	**00b = PWM frequency is 80 Hz** 01b = PWM frequency is 100 Hz 10b = PWM frequency is 200 Hz 11b = PWM frequency is 2000 Hz
5-4	PWM_CH7_FREQ	R/W	00b	**00b = PWM frequency is 80 Hz** 01b = PWM frequency is 100 Hz 10b = PWM frequency is 200 Hz 11b = PWM frequency is 2000 Hz
3-2	PWM_CH6_FREQ	R/W	00b	**00b = PWM frequency is 80 Hz** 01b = PWM frequency is 100 Hz 10b = PWM frequency is 200 Hz 11b = PWM frequency is 2000 Hz
1-0	PWM_CH5_FREQ	R/W	00b	**00b = PWM frequency is 80 Hz** 01b = PWM frequency is 100 Hz 10b = PWM frequency is 200 Hz 11b = PWM frequency is 2000 Hz

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8.6.2.2.15 *PWM Duty Control Channel 1 (PWM_DUTY_CH1) Register (Address = 0x15) [reset = 0x00]*

The channel 1 PWM duty cycle control register is shown in 図 118 and described in 表 76.

Register access type: Read/Write

図 118. PWM Duty Control Channel 1 Register

7	6	5	4	3	2	1	0
PWM_DUTY_CH1							
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 76. PWM Duty Control Channel 1 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PWM_DUTY_CH1	R/W	00000000b	**00000000b = 0 % PWM Duty** 11111111b = 100 % PWM Duty Calculate duty as decimal (xxxxxxxxb) × 1/255

8.6.2.2.16 *PWM Duty Control Channel 2 (PWM_DUTY_CH2) Register (Address = 0x16) [reset = 0x00]*

The channel 2 PWM duty cycle control register is shown in 図 119 and described in 表 77.

Register access type: Read/Write

図 119. PWM Duty Control Channel 2 Register

7	6	5	4	3	2	1	0
PWM_DUTY_CH2							
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 77. PWM Duty Control Channel 2 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PWM_DUTY_CH2	R/W	00000000b	**00000000b = 0 % PWM Duty** 11111111b = 100 % PWM Duty Calculate duty as decimal (xxxxxxxxb) × 1/255

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8.6.2.2.17 *PWM Duty Control Channel 3 (PWM_DUTY_CH3) Register (Address = 0x17) [reset = 0x00]*

The channel 3 PWM duty cycle control register is shown in 図 120 and described in 表 78.

Register access type: Read/Write

図 120. PWM Duty Control Channel 3 Register

7	6	5	4	3	2	1	0
PWM_DUTY_CH3							
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 78. PWM Duty Control Channel 3 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PWM_DUTY_CH3	R/W	00000000b	**00000000b = 0 % PWM Duty** 11111111b = 100 % PWM Duty Calculate duty as decimal (xxxxxxxxb) × 1/255

8.6.2.2.18 *PWM Duty Control Channel 4 (PWM_DUTY_CH4) Register (Address = 0x18) [reset = 0x00]*

The channel 4 PWM duty cycle control register is shown in 図 121 and described in 表 79.

Register access type: Read/Write

図 121. PWM Duty Control Channel 4 Register

7	6	5	4	3	2	1	0
PWM_DUTY_CH4							
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 79. PWM Duty Control Channel 4 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PWM_DUTY_CH4	R/W	00000000b	**00000000b = 0 % PWM Duty** 11111111b = 100 % PWM Duty Calculate duty as decimal (xxxxxxxxb) × 1/255

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8.6.2.2.19 *PWM Duty Control Channel 5 (PWM_DUTY_CH5) Register (Address = 0x19) [reset = 0x00]*

The channel 5 PWM duty cycle control register is shown in 図 122 and described in 表 80.

Register access type: Read/Write

図 122. PWM Duty Control Channel 5 Register

7	6	5	4	3	2	1	0
PWM_DUTY_CH5							
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 80. PWM Duty Control Channel 5 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PWM_DUTY_CH5	R/W	00000000b	**00000000b = 0 % PWM Duty** 11111111b = 100 % PWM Duty Calculate duty as decimal (xxxxxxxxb) × 1/255

8.6.2.2.20 *PWM Duty Control Channel 6 (PWM_DUTY_CH6) Register (Address = 0x1A) [reset = 0x00]*

The channel 6 PWM duty cycle control register is shown in 図 123 and described in 表 81.

Register access type: Read/Write

図 123. PWM Duty Control Channel 6 Register

7	6	5	4	3	2	1	0
PWM_DUTY_CH6							
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 81. PWM Duty Control Channel 6 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PWM_DUTY_CH6	R/W	00000000b	**00000000b = 0 % PWM Duty** 11111111b = 100 % PWM Duty Calculate duty as decimal (xxxxxxxxb) × 1/255

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8.6.2.2.21 *PWM Duty Control Channel 7 (PWM_DUTY_CH7) Register (Address = 0x1B) [reset = 0x00]*

The channel 7 PWM duty cycle control register is shown in 図 124 and described in 表 82.

Register access type: Read/Write

図 124. PWM Duty Control Channel 7 Register

7	6	5	4	3	2	1	0
PWM_DUTY_CH7							
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 82. PWM Duty Control Channel 7 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PWM_DUTY_CH7	R/W	00000000b	**00000000b = 0 % PWM Duty** 11111111b = 100 % PWM Duty Calculate duty as decimal (xxxxxxxxb) × 1/255

8.6.2.2.22 *PWM Duty Control Channel 8 (PWM_DUTY_CH8) Register (Address = 0x1C) [reset = 0x00]*

The channel 8 PWM duty cycle control register is shown in 図 125 and described in 表 83.

Register access type: Read/Write

図 125. PWM Duty Control Channel 8 Register

7	6	5	4	3	2	1	0
PWM_DUTY_CH4							
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 83. PWM Duty Control Channel 8 Register Field Descriptions

Bit	Field	Type	Default	Description
7-0	PWM_DUTY_CH8	R/W	00000000b	**00000000b = 0 % PWM Duty** 11111111b = 100 % PWM Duty Calculate duty as decimal (xxxxxxxxb) × 1/255

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8.6.2.2.23 *Slew Rate Control 1 (SR_CTRL_1) Register (Address = 0x1D [reset = 0x00]*

The slew rate control 1 register is shown in 図 91 and described in 表 44.

Register access type: Read/Write

図 126. Slew Rate Control 1 Register

7	6	5	4	3	2	1	0
HB8_SR	HB7_SR	HB6_SR	HB5_SR	HB4_SR	HB3_SR	HB2_SR	HB1_SR
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 84. Slew Rate Control 1 Register Field Descriptions

Bit	Field	Type	Default	Description
7	HB8_SR	R/W	0b	**0b = 0.6 V/µs** 1b = 2.5 V/µs
6	HB7_SR	R/W	0b	**0b = 0.6 V/µs** 1b = 2.5 V/µs
5	HB6_SR	R/W	0b	**0b = 0.6 V/µs** 1b = 2.5 V/µs
4	HB5_SR	R/W	0b	**0b = 0.6 V/µs** 1b = 2.5 V/µs
3	HB4_SR	R/W	0b	**0b = 0.6 V/µs** 1b = 2.5 V/µs
2	HB3_SR	R/W	0b	**0b = 0.6 V/µs** 1b = 2.5 V/µs
1	HB2_SR	R/W	0b	**0b = 0.6 V/µs** 1b = 2.5 V/µs
0	HB1_SR	R/W	0b	**0b = 0.6 V/µs** 1b = 2.5 V/µs

8.6.2.2.24 *Slew Rate Control 2 (SR_CTRL_2) Register (Address = 0x1E) [reset = 0x00]*

The slew rate control 2 register is shown in 図 92 and described in 表 45.

Register access type: Read/Write

図 127. Slew Rate Control 2 Register

7	6	5	4				
Reserved							
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 85. Slew Rate Control 2 Register Field Descriptions

Bit	Field	Type	Default	Description
7-4	Reserved	R/W	0000b	Reserved

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8.6.2.2.25 *Open-Load Detect (OLD) Control 1 (OLD_CTRL_1) Register (Address = 0x1F) [reset = 0x00]*

The open-load detect (OLD) control (OLD_CTRL_1) register-1 is shown in 図 128 and described in 表 86.

Register access type: Read/Write

図 128. Open-Load Detect (OLD) Control (OLD_CTRL_1) Register

7	6	5	4	3	2	1	0
HB8_OLD_DIS	HB7_OLD_DIS	HB6_OLD_DIS	HB5_OLD_DIS	HB4_OLD_DIS	HB3_OLD_DIS	HB2_OLD_DIS	HB1_OLD_DIS
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 86. Open-Load Detect (OLD) Control (OLD_CTRL_1) Register Field Descriptions

Bit	Field	Type	Default	Description
7	HB8_OLD_DIS	R/W	0b	**0b = Open-load detection on half-bridge 8 is enabled** 1b = Open-load on half-bridge 8 is disabled
6	HB7_OLD_DIS	R/W	0b	**0b = Open-load detection on half-bridge 7 is enabled** 1b = Open-load on half-bridge 7 is disabled
5	HB6_OLD_DIS	R/W	0b	**0b = Open-load detection on half-bridge 6 is enabled** 1b = Open-load on half-bridge 6 is disabled
4	HB5_OLD_DIS	R/W	0b	**0b = Open-load detection on half-bridge 5 is enabled** 1b = Open-load on half-bridge 5 is disabled
3	HB4_OLD_DIS	R/W	0b	**0b = Open-load detection on half-bridge 4 is enabled** 1b = Open-load on half-bridge 4 is disabled
2	HB3_OLD_DIS	R/W	0b	**0b = Open-load detection on half-bridge 3 is enabled** 1b = Open-load on half-bridge 3 is disabled
1	HB2_OLD_DIS	R/W	0b	**0b = Open-load detection on half-bridge 2 is enabled** 1b = Open-load on half-bridge 2 is disabled
0	HB1_OLD_DIS	R/W	0b	**0b = Open-load detection on half-bridge 1 is enabled** 1b = Open-load on half-bridge 1 is disabled

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8.6.2.2.26 *Open-Load Detect (OLD) Control 2 (OLD_CTRL_2) Register (Address = 0x20) [reset = 0x00]*

The open-load detect (OLD) control (OLD_CTRL_2) register-2 is shown in 図 94 and described in 表 47.

Register access type: Read/Write

図 129. Open-Load Detect (OLD) Control (OLD_CTRL_2) Register

7	6	5	4	3	2	1	0
OLD_REP	OLD_OP	PL_MODE_EN		Reserved			
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 87. Open-Load Detect (OLD) Control (OLD_CTRL_2) Register Field Descriptions

Bit	Field	Type	Default	Description
7	OLD_REP	R/W	0b	**0b = Report on nFAULT pin during OLD condition** 1b = No report on nFAULT pin during OLD condition
6	OLD_OP	R/W	0b	**0b = Half bridges are not active after OLD condition detect** 1b = Half bridges are active after OLD condition detect
5-4	PL_MODE_EN	R/W	00b	**00b = Parallel mode OCP fast turn-off slew is enabled** 01b = Parallel mode OCP slow turn-off slew is enabled 10b = Invalid Setting 11b = Invalid Setting
3-0	Reserved	R	0b	Reserved

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8.6.2.2.27 Open-Load Detect (OLD) Control 3 (OLD_CTRL_3) Register (Address = 0x21) [reset = 0x00]

The open-load detect (OLD) control (OLD_CTRL_3) register-3 is shown in 図 95 and described in 表 48. This register also contains the bits to set the OCP deglitch time (OCP_DEG).

Register access type: Read/Write

図 130. Open-Load Detect (OLD) Control (OLD_CTRL_3) Register

7	6	5	4	3	2	1	0
OCP_DEG			OLD_NEG_EN	Reserved			
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 88. Open-Load Detect (OLD) Control (OLD_CTRL_3) Register Field Descriptions

Bit	Field	Type	Default	Description
7-5	OCP_DEG	R/W	000b	**000b = OCP deglitch time is 10 µs** 001b = OCP deglitch time is 5 µs 010b = OCP deglitch time is 2.5µs 011b = OCP deglitch time is 1 µs 100b = OCP deglitch time is 60 µs 101b = OCP deglitch time is 40 µs 110b = OCP deglitch time is 30 µs 111b = OCP deglitch time is 20 µs
4	OLD_NEG_EN	R/W	0b	**0b = Negative-current OLD mode is disabled** 1b = Negative-current OLD mode is enabled
3-0	Reserved	R/W	0b	Reserved

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8.6.2.2.28 Open Load Detect (OLD) Control 4 (OLD_CTRL_4) Register (Address = 0x22) [reset = 0x00]

The open load detect (OLD) control (OLD_CTRL_4) register-4 is shown in 図 131 and described in 表 89.

Register access type: Read/Write

図 131. Open Load Detect (OLD) Control (OLD_CTRL_4) Register

7	6	5	4	3	2	1	0
HB8_LCOLD_EN	HB7_LOLD_EN	HB6_LOLD_EN	HB5_LOLD_EN	HB4_LOLD_EN	HB3_LOLD_EN	HB2_LOLD_EN	HB1_LOLD_EN
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 89. Open Load Detect (OLD) Control (OLD_CTRL_4) Register Field Descriptions

Bit	Field	Type	Default	Description
7	HB8_LOLD_EN	R/W	0b	**0b = Low-current OLD on half-bridge 8 is disabled** 1b = Low-current OLD on half-bridge 8 is enabled
6	HB7_LOLD_EN	R/W	0b	**0b = Low-current OLD on half-bridge 7 is disabled** 1b = Low-current OLD on half-bridge 7 is enabled
5	HB6_LOLD_EN	R/W	0b	**0b = Low-current OLD on half-bridge 6 is disabled** 1b = Low-current OLD on half-bridge 6 is enabled
4	HB5_LOLD_EN	R/W	0b	**0b = Low-current OLD on half-bridge 5 is disabled** 1b = Low-current OLD on half-bridge 5 is enabled
3	HB4_LOLD_EN	R/W	0b	**0b = Low-current OLD on half-bridge 4 is disabled** 1b = Low-current OLD on half-bridge 4 is enabled
2	HB3_LOLD_EN	R/W	0b	**0b = Low-current OLD on half-bridge 3 is disabled** 1b = Low-current OLD on half-bridge 3 is enabled
1	HB2_LOLD_EN	R/W	0b	**0b = Low-current OLD on half-bridge 2 is disabled** 1b = Low-current OLD on half-bridge 2 is enabled
0	HB1_LOLD_EN	R/W	0b	**0b = Low-current OLD on half-bridge 1 is disabled** 1b = Low-current OLD on half-bridge 1 is enabled

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8.6.2.2.29 Open Load Detect (OLD) Control 5 (OLD_CTRL_5) Register (Address = 0x23) [reset = 0x00]

The open load detect (OLD) (OLD_CTRL_5) register-5 is shown in 図 132 and described in 表 90.

図 132. Open Load Detect (OLD) Control (OLD_CTRL_5) Register

7	6	5	4	3	2	1	0
HB8_POLD_EN	HB7_POLD_EN	HB6_POLD_EN	HB5_POLD_EN	HB4_POLD_EN	HB3_POLD_EN	HB2_POLD_EN	HB1_POLD_EN
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 90. Open Load Detect (OLD) Control (OLD_CTRL_5) Register Field Descriptions

Bit	Field	Type	Default	Description
7	HB8_POLD_EN	R/W	0b	**0b = Passive OLD operation of half-bridge 8 is disabled** 1b = Passive OLD operation of half-bridge 8 is enabled
6	HB7_POLD_EN	R/W	0b	**0b = Passive OLD operation of half-bridge 7 is disabled** 1b = Passive OLD operation of half-bridge 7 is enabled
5	HB6_POLD_EN	R/W	0b	**0b = Passive OLD operation of half-bridge 6 is disabled** 1b = Passive OLD operation of half-bridge 6 is enabled
4	HB5_POLD_EN	R/W	0b	**0b = Passive OLD operation of half-bridge 5 is disabled** 1b = Passive OLD operation of half-bridge 5 is enabled
3	HB4_POLD_EN	R/W	0b	**0b = Passive OLD operation of half-bridge 4 is disabled** 1b = Passive OLD operation of half-bridge 4 is enabled
2	HB3_POLD_EN	R/W	0b	**0b = Passive OLD operation of half-bridge 3 is disabled** 1b = Passive OLD operation of half-bridge 3 is enabled
1	HB2_POLD_EN	R/W	0b	**0b = Passive OLD operation of half-bridge 2 is disabled** 1b = Passive OLD operation of half-bridge 2 is enabled
0	HB1_POLD_EN	R/W	0b	**0b = Passive OLD operation of half-bridge 1 is disabled** 1b = Passive OLD operation of half-bridge 1 is enabled

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8.6.2.2.30 Open Load Detect (OLD) Control 6 (OLD_CTRL_6) Register (Address = 0x24) [reset = 0x00]

The open load detect (OLD) (OLD_CTRL_6) register-6 register is shown in 図 133 and described in 表 91.

図 133. Open Load Detect (OLD) Control (OLD_CTRL_6) Register

7	6	5	4	3	2	1	0
HB8_VM_POLD	HB7_VM_POLD	HB6_VM_POLD	HB5_VM_POLD	HB4_VM_POLD	HB3_VM_POLD	HB2_VM_POLD	HB1_VM_POLD
R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b	R/W-0b

表 91. Open Load Detect (OLD) Control (OLD_CTRL_6) Register Field Descriptions

Bit	Field	Type	Default	Description
7	HB8_VM_POLD	R/W	0b	**0b = Passive OLD operation for VM connected load of half-bridge 8 is disabled** 1b = Passive OLD operation for VM connected load of half-bridge 8 is enabled
6	HB7_VM_POLD	R/W	0b	**0b = Passive OLD operation for VM connected load of half-bridge 7 is disabled** 1b = Passive OLD operation for VM connected load of half-bridge 7 is enabled
5	HB6_VM_POLD	R/W	0b	**0b = Passive OLD operation for VM connected load of half-bridge 6 is disabled** 1b = Passive OLD operation for VM connected load of half-bridge 6 is enabled
4	HB5_VM_POLD	R/W	0b	**0b = Passive OLD operation for VM connected load of half-bridge 5 is disabled** 1b = Passive OLD operation for VM connected load of half-bridge 5 is enabled
3	HB4_VM_POLD	R/W	0b	**0b = Passive OLD operation for VM connected load of half-bridge 4 is disabled** 1b = Passive OLD operation for VM connected load of half-bridge 4 is enabled
2	HB3_VM_POLD	R/W	0b	**0b = Passive OLD operation for VM connected load of half-bridge 3 is disabled** 1b = Passive OLD operation for VM connected load of half-bridge 3 is enabled
1	HB2__VM_POLD	R/W	0b	**0b = Passive OLD operation for VM connected load of half-bridge 2 is disabled** 1b = Passive OLD operation for VM connected load of half-bridge 2 is enabled
0	HB1_VM_POLD	R/W	0b	**0b = Passive OLD operation for VM connected load of half-bridge 1 is disabled** 1b = Passive OLD operation for VM connected load of half-bridge 1 is enabled

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9 Application and Implementation

注

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The DRV89xx-Q1 device is primarily used in control of multiple brushed DC motors in HVAC applications. The design procedures in the Typical Application section highlight how to use and configure the DRV89xx-Q1 device.

The DRV89xx-Q1 device can alternatively be used in automotive side-mirrors targeting the mirror-fold (by paralleling the half-bridges to meet the high current requirement), mirror x-y direction control and side indicator LED's as presented in Alternative Application section.

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9.2 Typical Application

9.2.1 Primary Application

The DRV89xx-Q1 is primarily used for the control of multiple brushed DC motors which can be connected in independent-type, sequential-type or the parallel-type motor connection as shown in 図 134.

An automotive battery powers the device to power supply pin (VM). A 3.3-V regulated power supply is generated for the supplying power to the digital core (VDD) of the device. A micro-controller is connected to the DRV89XX-Q1 device with the SPI interface (4-lines) for control, configuration and diagnostics. The device operating or sleep state is controlled by the nSLEEP pin and nFAULT pins is used as an additional hardware diagnostics.

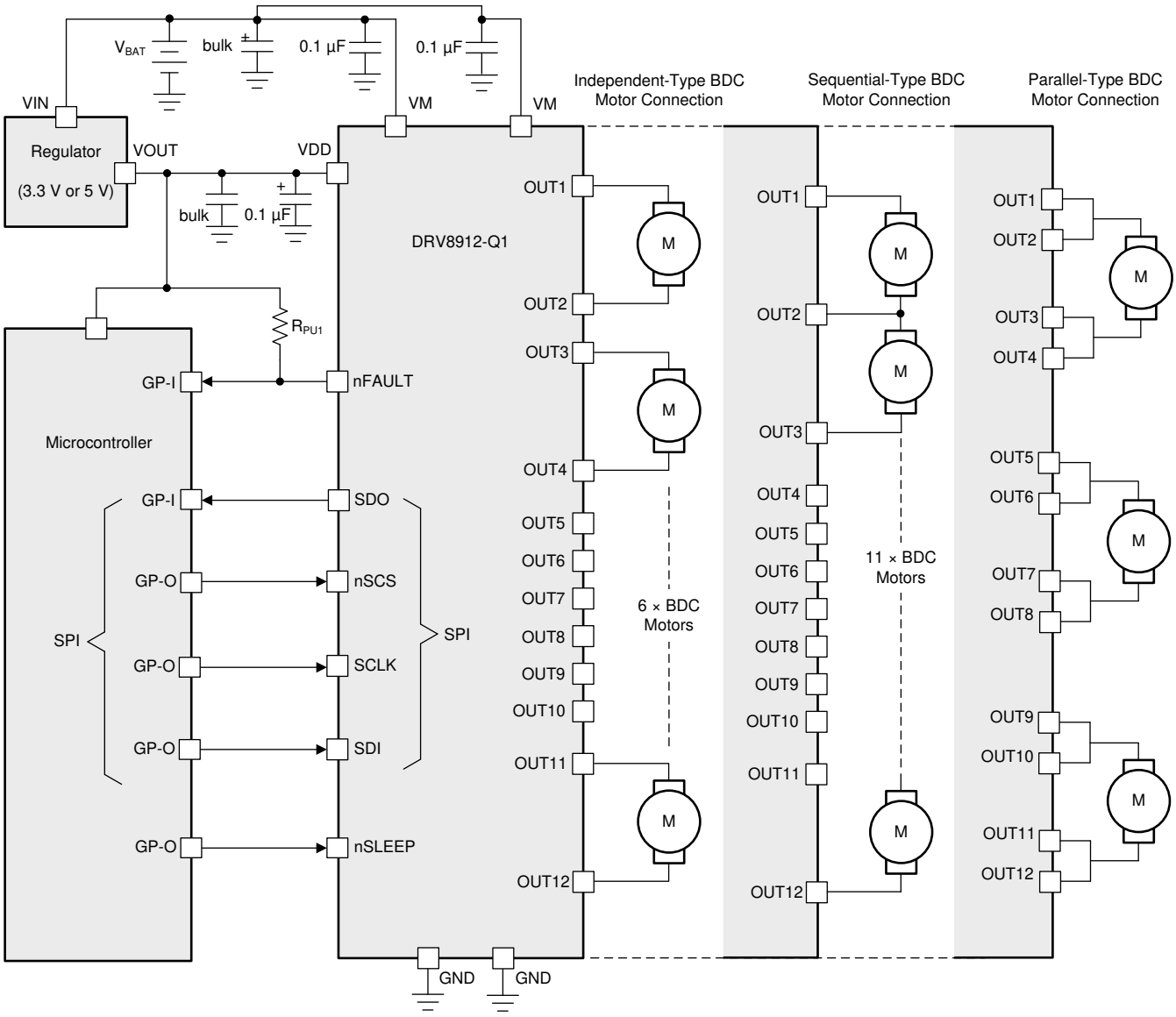


図 134. Primary Application Schematic (Automotive HVAC Application)

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Typical Application (continued)

9.2.1.1 Design Requirements

表 92 lists example input parameters for the system design.

表 92. Design Parameters

DESIGN PARAMETERS	REFERENCE	EXAMPLE VALUE
Supply voltage	V_{VM}	13.5-V
Supply digital voltage	V_{VDD}	3.3-V
Number of motor connected	N	6 motors
Number of motor operating in normal operation	N_F	4 motors
Number of motor operating in stall condition	N_S	2 motors
Motor RMS current	I_{RMS}	200-mA
Motor peak current	I_{PEAK}	800-mA
Motor resistance	R_{MOTOR}	16.9-Ω
Motor inductance	L_{MOTOR}	10-mH
PWM Frequency	f_{PWM}	2-kHz (Internal)
Rise and fall time for continuous mode (SR = 0)	t_{RISE_CONT}, t_{FALL_CONT}	22.5-µs
Rise and fall time for PWM mode (SR = 1)	t_{RISE_PWM}, t_{FALL_PWM}	5.4-µs

9.2.1.2 Detailed Design Procedure

The design procedure includes the selection of motor current rating the power dissipation to meet the desired thermal performance.

9.2.1.2.1 Motor Current Rating

Motor specification selection is the most importance criteria for the design. Each half-bridge (OUTx) of the DRV89XX-Q1 device is designed to handle RMS current of 1-A and the peak current is limited by the minimum over-current (OCP) limit of 1.3-A. Therefore, a motor with peak starting current higher than 1.3-A is expected to hit OCP limit. For higher peak current motors (starting current higher than 1.3-A), following methods can be implemented:

1. **Current Chopping:** During starting, if supply voltage is connected directly to the motor, then due to low back-emf (when speed is zero or low), a huge peak current is demanded by the motor. This peak current is only limited by the motor's winding resistance (R_{MOTOR}). This peak current of motor can be limited by starting the motor with low-duty PWM switching operation and then gradually increasing (duty-ramping) the duty with speed to 100% PWM operation (equivalent to motor operating in continuous mode). This duty-ramping provides enough time to ramp motor speed and build sufficient back-emf which limits the peak current. The DRV89XX-Q1 device implements a 2-kHz PWM switching operation which is suitable for the HVAC damper motors.
2. **OCP Deglitch Time Adjustments:** This method is applicable if the motor inertia is low and the motor can quickly pick up the speed. For this method, the motor starting current should settle to lower than minimum over-current limit (I_{OCP}) before OCP deglitch time (t_{OCP}) is over. The device provides multiple (8 settings) OCP deglitch time settings with a default deglitch time of 10-µs and can be increased to a maximum value of 60-µs.

注

For multiple motor connection, it has to be ensured that the total device current should be lower than the maximum current-carrying capability of the power-supply (VM/GND) pins i.e. 6-A (maximum).

9.2.1.2.2 Power Dissipation

A detailed explanation of the power dissipation of the device is presented in Power Dissipation section.

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9.2.2 Alternative Application

The DRV89xx-Q1 can alternatively be used for the mirrors targeting the mirror-fold, mirror x-y direction control and side indicator LED's as shown in 図 135.

The half-bridges are connected in parallel to support the higher current requirement of the mirror fold application. Whereas, single half-bridges can be used for driving the low-current motors used for the mirror X and Y positioning. Moreover, the LED's used in side indicators, puddle lamp is lower current which can be easily driven by single half-bridges.

The driver is powered by the automotive battery with a 3.3-V regulated power supply generated for the supplying power to the digital pin (VDD). A micro-controller is connected to the DRV89XX-Q1 device with the SPI interface (4-lines) for control, configuration and diagnostics. The device operating or sleep state is controlled by the nSLEEP pin and nFAULT pins is used as an additional hardware diagnostics.

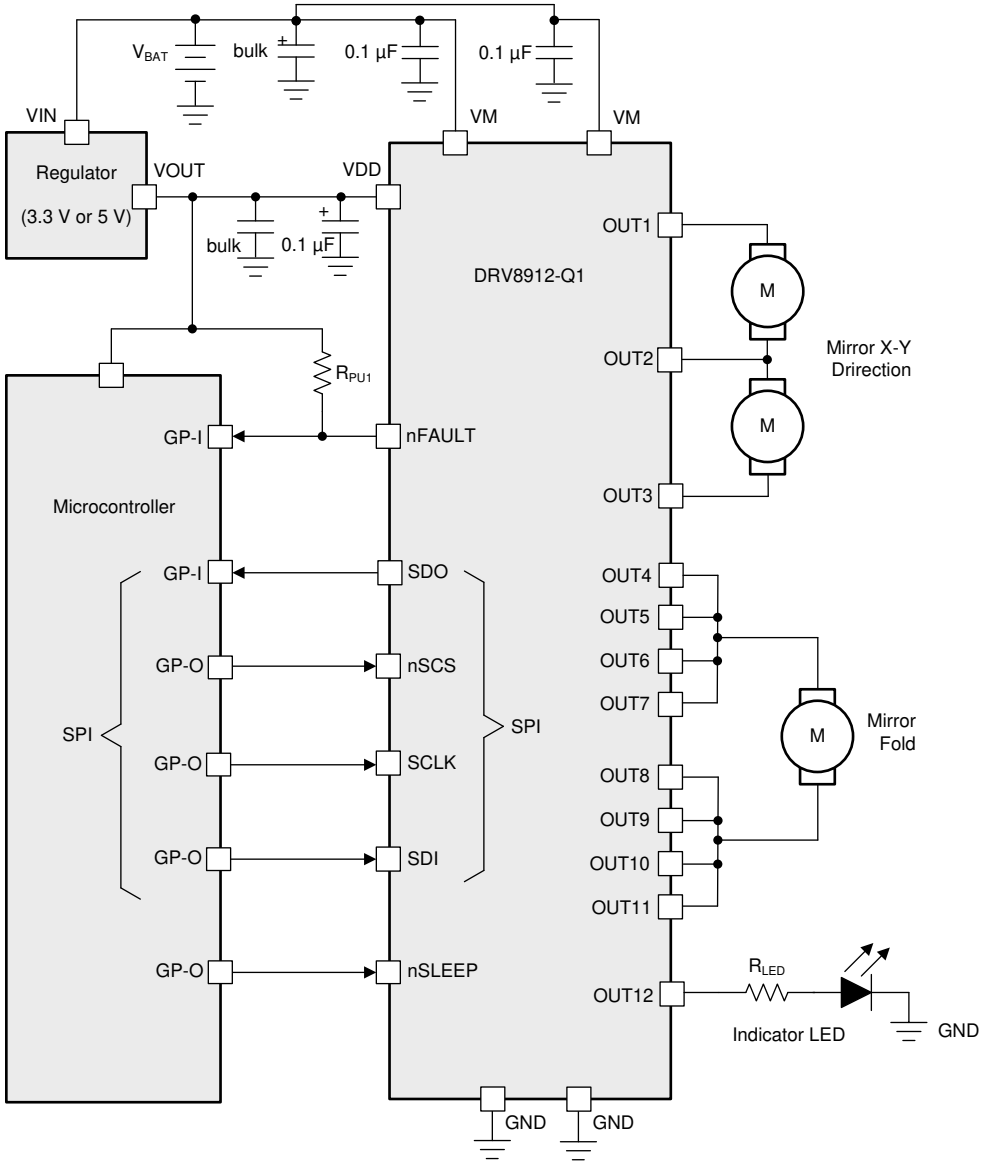


図 135. Alternative Application Schematic (Automotive Side-Mirror Application)

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9.2.2.1 Design Requirements

表 93 lists example input parameters for the system design.

表 93. Design Parameters

DESIGN PARAMETERS	REFERENCE	EXAMPLE VALUE
Supply voltage	V_{VM}	13.5-V
Supply digital voltage	V_{VDD}	3.3-V
Motor RMS current (Mirror Fold Motor)	I_{RMS_FOLD}	1.8-A
Motor peak current (Mirror Fold Motor)	I_{PEAK_FOLD}	3-A
Motor RMS current (X/Y Direction Motor)	I_{RMS_XY}	200-mA
Motor peak current (X/Y Direction Motor)	I_{PEAK_XY}	800-mA
LED Current	I_{LED}	150-mA
PWM Frequency (Motor)	f_{PWM_MOTOR}	2-kHz (Internal)
PWM Frequency (LED)	f_{PWM_LED}	100-Hz (Internal)
Rise and fall time for continuous mode (SR = 0)	t_{RISE_CONT}, t_{FALL_CONT}	22.5-µs
Rise and fall time for PWM mode (SR = 1)	t_{RISE_PWM}, t_{FALL_PWM}	5.4-µs

9.2.2.2 Detailed Design Procedure

The key-requirement for this application is the selection of number of half-bridges to operate in parallel for the high current motor (mirror-fold) application. Parallel Mode (Continuous Operation) describes the configuration for half-bridges for enabling the parallel mode operation.

9.2.2.2.1 H-Bridge Requirements for Parallel Operation

The selection of number of half-bridges for connecting in parallel operation to support higher current depends on two parameters as:

1. **Peak / Stall Current:** The mirror-fold motor peak current decides the amount of current flowing through a single half-bridge which has to be lower than the minimum OCP (I_{OCP}) threshold limit. A current limiting approach for limiting the peak current of motor can also be implemented as shown in Motor Current Rating section. This section also explains the application of adjusting the OCP deglitch timing for meeting the desired peak currents.
2. **Thermal:** For meeting the desired thermal performance during the peak current / stall condition, the number of half-bridges is increased to reduce the effective $R_{DS(ON)}$.

For this example as shown in 表 93, six half-bridges can be connected in parallel combination (3 half-bridges for high-side and 3 half-bridges for low-side) to support the 3-A peak current requirement. The power dissipation for this can be calculated in similar way as explained in Power Dissipation section.

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9.2.3 Application Curves

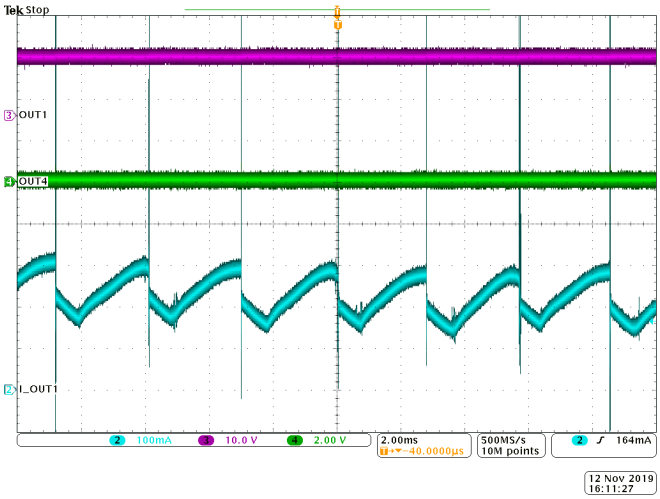


図 136. Motor Operation in Continuous Mode

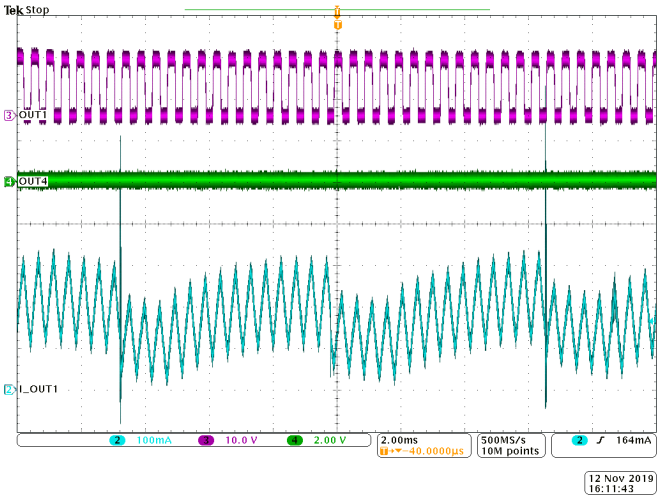


図 137. Motor Operation in PWM Mode

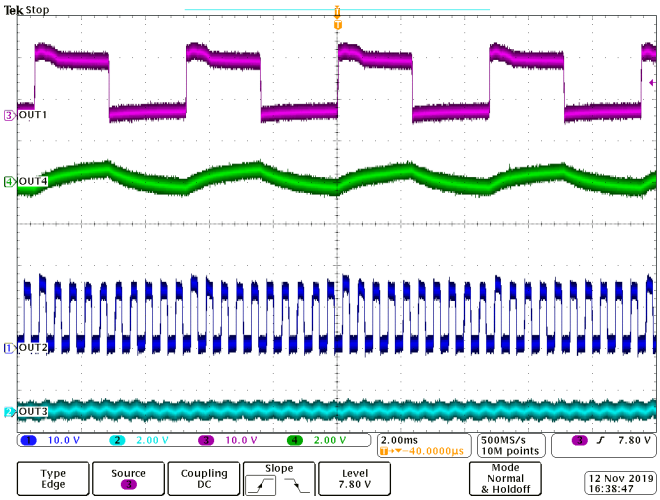


図 138. Multiple Motor Operation in PWM Mode

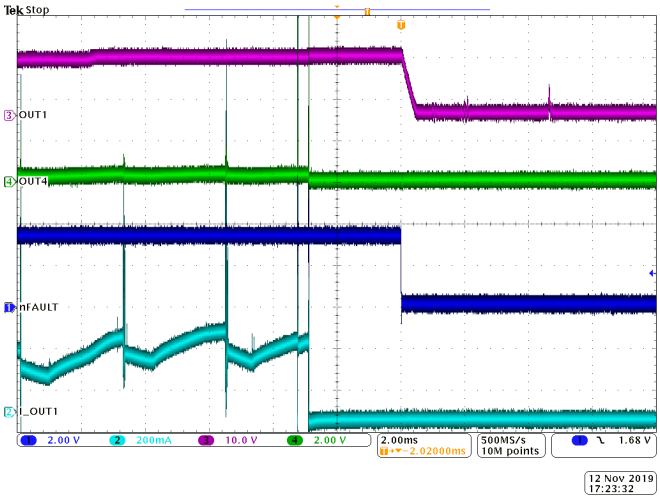


図 139. Active Open-Load Detection

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9.3 Thermal Application

This section presents the power dissipation and thermal analysis of DRV89XX-Q1 device applicable for different types of PCB's.

9.3.1 Power Dissipation

The total power dissipation in the DRV89XX-Q1 device constitutes three main components as the power dissipation in full-bridges (P_{DRV}) due to on-state resistance ($R_{DS(ON)}$), power dissipation due to switching losses in FETs (P_{SW}) and power losses due to quiescent current consumption (P_Q).

9.3.1.1 Power Dissipation Due to Device On-State Resistance ($R_{DS(ON)}$)

The current path for a motor connected in full-bridge is through the high-side FET of one half-bridge and low-side FET of other half-bridge. The power dissipation of DRV89XX-Q1 depends on the amount of current flowing through the full-bridge and the number of such full-bridges which are operating together. The power dissipation (P_{FB_CONT}) in a single full-bridge configuration for continuous mode depends on the motor rms current (I_{RMS}) and high-side ($R_{DS(ON)_HS}$) and low-side ($R_{DS(ON)_LS}$) on-state resistance as shown in 式 1.

$$P_{FB_CONT} = (I_{RMS})^2 \times (R_{DS(ON)_HS} + R_{DS(ON)_LS}) \quad (1)$$

The power dissipation (P_{FB_STALL}) in a single full-bridge configuration for motor is a stall condition depends on the motor peak current (I_{PEAK}) and high-side ($R_{DS(ON)_HS}$) and low-side ($R_{DS(ON)_LS}$) on-state resistance as shown in 式 2.

$$P_{FB_STALL} = (I_{PEAK})^2 \times (R_{DS(ON)_HS} + R_{DS(ON)_LS}) \quad (2)$$

Now, the power dissipation for operating mode and stall mode in single full-bridge for the typical application as shown in 表 92 is calculated in 式 3 and 式 4 respectively.

$$P_{FB_CONT} = (I_{RMS})^2 \times (R_{DS(ON)_HS} + R_{DS(ON)_LS}) = (200\text{-mA})^2 \times (0.75\text{-}\Omega + 0.75\text{-}\Omega) = 60\text{-mW} \quad (3)$$

$$P_{FB_STALL} = (I_{PEAK})^2 \times (R_{DS(ON)_HS} + R_{DS(ON)_LS}) = (800\text{-mA})^2 \times (0.75\text{-}\Omega + 0.75\text{-}\Omega) = 960\text{-mW} \quad (4)$$

For N_F-full bridges in operating condition and N_S-full bridges in stall condition, the total driver power (P_{DRV}) is expressed and calculated as shown in 式 5.

$$P_{DRV} = N_F \times P_{FB_CONT} + N_S \times P_{FB_STALL} = 4 \times 60\text{-mW} + 2 \times 960\text{-mW} = 2.16\text{-W} \quad (5)$$

注

This power calculation is highly dependent on the device temperature which significantly effects the high-side and low-side $R_{DS(ON)}$ of the FETs. For more accurate calculation, consider the dependency of $R_{DS(ON)}$ of FETs with device temperature.

9.3.1.2 Power Dissipation Due to Switching Losses

The power loss due to the PWM switching frequency depends on the slew rates (rise-time (t_{RISE_PWM}) and fall-time (t_{FALL_PWM})), supply voltage (V_{VM}), motor RMS current (I_{RMS}) and the PWM switching frequency (f_{PWM}). Considering a case, where the PWM switching is only applicable for single half-bridge in a full-bridge configuration (see Free-Wheeling Mode (Synchronous Rectification) Disable / Enable), therefore only half of the half-bridges are operating in PWM switching. Hence, the switching losses during rise-time and fall-time is calculated as shown in 式 6 and 式 7.

$$P_{SW_RISE} = (N_F/2) \times 0.5 \times V_{VM} \times I_{RMS} \times t_{RISE_PWM} \times f_{PWM} \quad (6)$$

$$P_{SW_FALL} = (N_F/2) \times 0.5 \times V_{VM} \times I_{RMS} \times t_{FALL_PWM} \times f_{PWM} \quad (7)$$

Putting various parameters from 表 92 in 式 6 and 式 7, the rise-time (P_{SW_RISE}) and fall-time (P_{SW_FALL}) switching losses are calculated as shown in 式 8 and 式 9 as,

$$P_{SW_RISE} = (N_F/2) \times 0.5 \times V_{VM} \times I_{RMS} \times t_{RISE_PWM} \times f_{PWM} = (4/2) \times 0.5 \times 13.5\text{-V} \times 200\text{-mA} \times 9\text{-µs} \times 2\text{-kHz} = 48.6\text{-mW} \quad (8)$$

$$P_{SW_FALL} = (N_F/2) \times 0.5 \times V_{VM} \times I_{RMS} \times t_{FALL_PWM} \times f_{PWM} = (4/2) \times 0.5 \times 13.5\text{-V} \times 200\text{-mA} \times 9\text{-µs} \times 2\text{-kHz} = 48.6\text{-mW} \quad (9)$$

Hence, the total switching power (P_{SW}) is calculated as the sum of rise-time (P_{SW_RISE}) switching losses and fall-time (P_{SW_FALL}) switching losses as shown in 式 10.

$$P_{SW} = P_{SW_RISE} + P_{SW_FALL} = 48.6\text{-mW} + 48.6\text{-mW} = 97.2\text{-mW} \quad (10)$$

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Thermal Application (continued)

注

The rise-time (t_{RISE}) and the fall-time (t_{FALL}) are calculated based on typical values of the slew rate (SR) from Specifications. This parameter is intended to change based on the supply-voltage, temperature and device to device variation.

9.3.1.3 Power Dissipation Due to Quiescent Current

The power dissipation due to the quiescent current taken by the power supply (P_{VM}) and the digital supply (P_{VDD}) depends on the applied voltage (V_{VM} and V_{VDD}) and operating mode currents (I_{VM} and I_{VDD}) and are calculated as shown in 式 11 and 式 12 respectively.

$$P_{VM} = V_{VM} \times I_{VM} \quad (11)$$

$$P_{VDD} = V_{VDD} \times I_{VDD} \quad (12)$$

Putting various parameters from 表 92 in 式 11 and 式 12, the power-supply (P_{VM}) and digital-supply (P_{SW_FALL}) quiescent power losses are calculated as shown in 式 13 and 式 14 as,

$$P_{VM} = V_{VM} \times I_{VM} = 13.5\text{-V} \times 3\text{-mA} = 40.5\text{-mW} \quad (13)$$

$$P_{VDD} = V_{VDD} \times I_{VDD} = 3.3\text{-V} \times 3\text{-mA} = 9\text{-mW} \quad (14)$$

The total quiescent power loss (P_Q) is calculated as the sum of quiescent power loss due to VM and VDD as shown in 式 15 as,

$$P_Q = P_{VM} + P_{VDD} = 40.5\text{-mW} + 9.9\text{-mW} = 50.4\text{-mW} \quad (15)$$

注

The quiescent power is calculated using the typical operating current (I_{VM} and I_{VDD}) which is dependent on supply-voltage, temperature and device to device variation.

9.3.1.4 Total Power Dissipation

The total power dissipation (P_{TOT}) is calculated as the sum of the power dissipation in full-bridges (P_{DRV}), power dissipation due to switching losses in FET's (P_{SW}) and power losses due to quiescent current consumption (P_Q) as shown in 式 16.

$$P_{TOT} = P_{DRV} + P_{SW} + P_Q \quad (16)$$

Now, by putting values of P_{DRV}, P_{SW} and P_Q from 式 5, 式 10 and 式 15 in 式 16, the total power dissipation (P_{TOT}) is calculated as shown in 式 17.

$$P_{TOT} = P_{DRV} + P_{SW} + P_Q = 2.16\text{-W} + 97.2\text{-mW} + 50.4\text{-mW} = 2.3076\text{-W} \quad (17)$$

9.3.2 PCB Types

Thermal analysis in this section is focused for the 2-layer and 4-layer PCB with two different copper thickness (1-oz and 2-oz) and six different copper areas (1-cm^2, 2-cm^2, 4-cm^2, 8-cm^2, 16-cm^2 and 32-cm^2).

図 140 and 図 141 shows the top-layer and bottom-layer which is applicable for both 2/4-layer PCB. 図 142 and 図 143 shows the mid-layer-1 and mid-layer-2 of a 4-layer PCB. The top-layer, mid-layer-1 and bottom-layer of the PCB is filled with ground plane, whereas, the mid-layer-2 is filled with power plane.

The thickness of copper for different PCB layers in different PCB types is summarized in 表 94. The PCB dimension (A) for different PCB copper area is summarized in 表 95.

表 94. PCB Type and Copper Thickness

PCB Type	Copper Thickness	Top Layer	Bottom Layer	Mid-Layer 1	Mid-Layer 2
2-Layer	1-oz PCB	1-oz	1-oz	N/A	
	2-oz PCB	2-oz	2-oz		
4-Layer	1-oz PCB	1-oz	1-oz	1-oz	1-oz
	2-oz PCB	2-oz	2-oz	1-oz	1-oz

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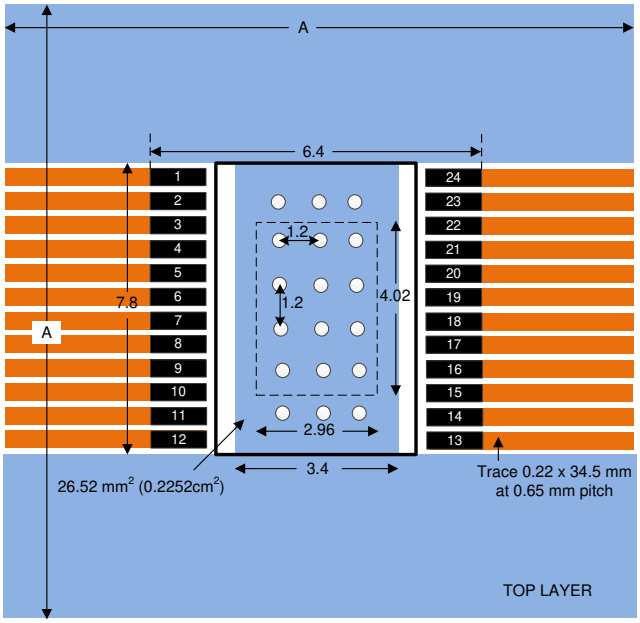


図 140. PCB - Top Layer (4/2-Layer PCB)

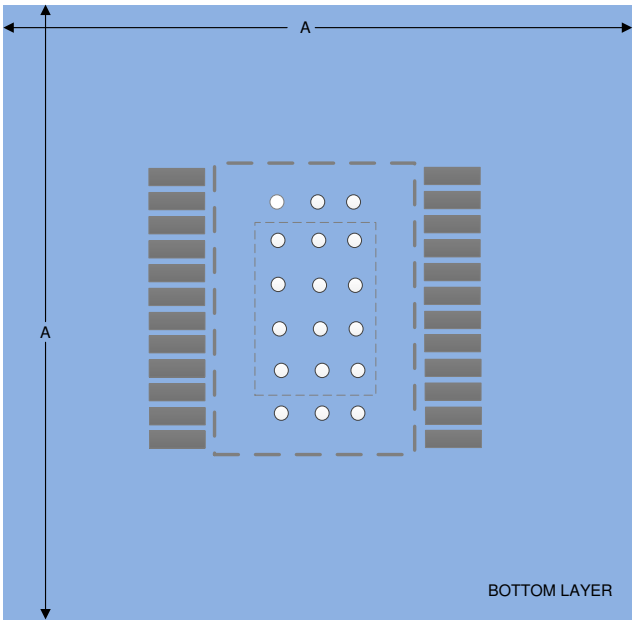


図 141. PCB - Bottom Layer (4/2-Layer PCB)

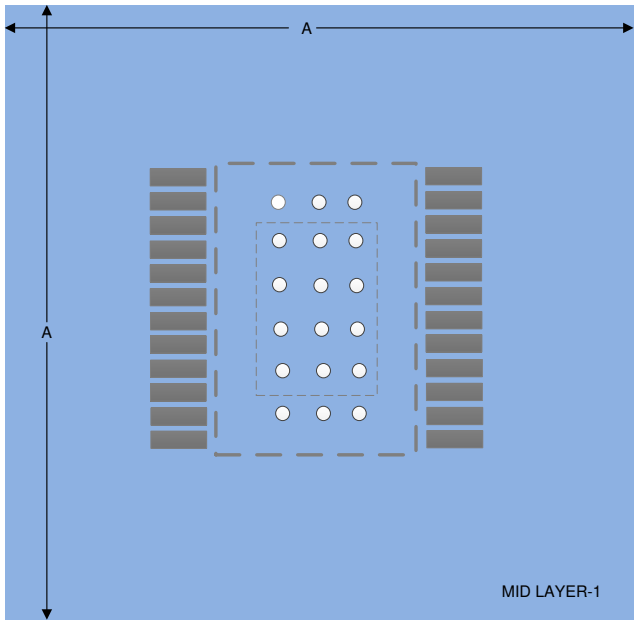


図 142. PCB - Mid Layer-1 (4-Layer PCB)

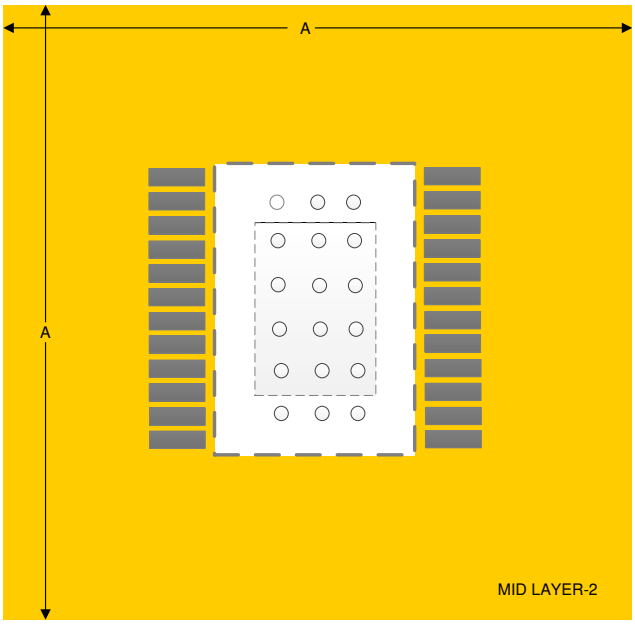


図 143. PCB - Mid Layer-2 (4-Layer PCB)

表 95. PCB Dimension

COPPER AREA (cm^2)	DIMENSION (A) (mm)
1 cm^2	13.31 mm
2 cm^2	17.64 mm
4 cm^2	23.62 mm
8 cm^2	31.98 mm
16 cm^2	43.76 mm
32 cm^2	60.36 mm

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9.3.3 Thermal Parameters

The variation of thermal parameters such as the $R_{\theta JA}$ (Junction-to-Ambient Thermal Resistance) and Ψ_{JB} (Junction-to-Board Characterization Parameter) is highly dependent on the PCB type, copper thickness and the copper pad area.

図 144 and 図 145 shows the variation of the $R_{\theta JA}$ (Junction-to-Ambient Thermal Resistance) and Ψ_{JB} (Junction-to-Board Characterization Parameter) with copper-pad area for 2-layer PCB. As shown in these curves, the thermal resistance is lower for the higher copper thickness PCB and the higher copper pad-area.

Similarly, 図 146 and 図 145 shows the variation of the $R_{\theta JA}$ and Ψ_{JB} with copper-pad area for 4-layer PCB respectively.

注

The thermal parameters ($R_{\theta JA}$ (Junction-to-Ambient Thermal Resistance) and Ψ_{JB} (Junction-to-Board Characterization Parameter)) are calculated considering the ambient temperature of 25°C and with 1.5-W power evenly dissipated between high-side and low-side FET's. The thermal parameters calculated considering the power dissipation at the actual location of the power-FETs rather than an averaged estimation.

The thermal parameters are highly dependent on the external conditions such as altitude, package geometry etc. Refer to Application Report for more details.

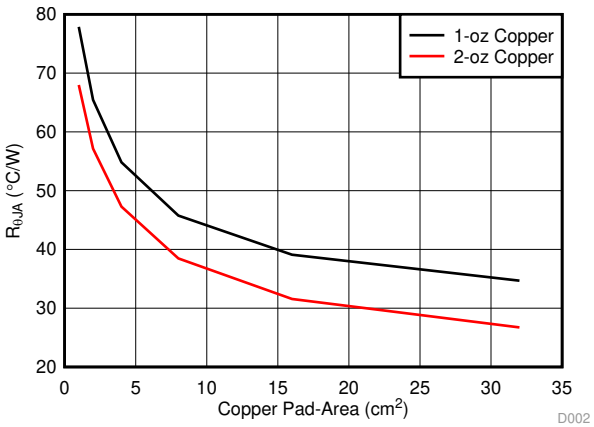


図 144. 2-Layer PCB Junction-to-Ambient Thermal Resistance ($R_{\theta JA}$) vs Copper Area

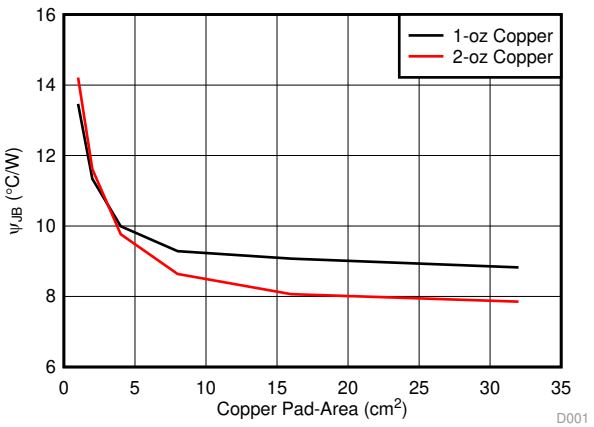


図 145. 2-Layer PCB Junction-to-Board Characterization Parameter (Ψ_{JB}) vs Copper Area

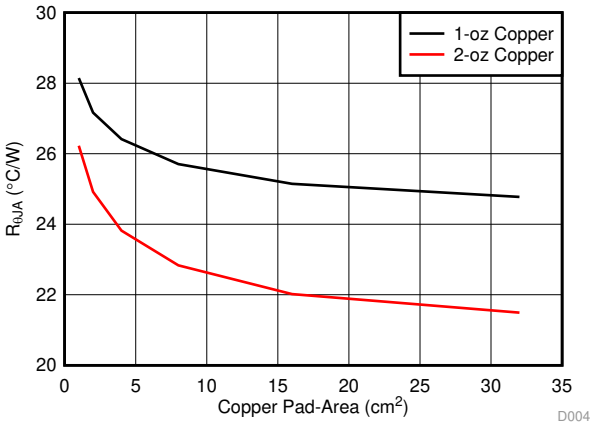


図 146. 4-Layer PCB Junction-to-Ambient Thermal Resistance ($R_{\theta JA}$) vs Copper Area

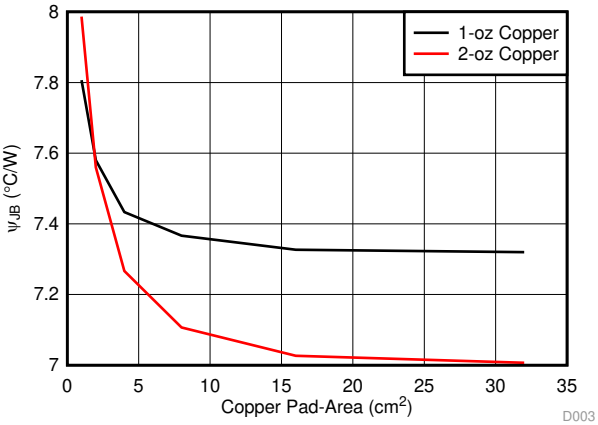


図 147. 4-Layer PCB Junction-to-Board Characterization (Ψ_{JB}) Parameter vs Copper Area

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9.3.4 Transient Thermal

This section presents the variation of transient thermal parameters such as the $Z_{\theta JA}$ (Transient Junction-to-Ambient Thermal Resistance) and $Z_{\Psi JB}$ (Transient Junction-to-Board Characterization Parameter) with time for 4-layer PCB board with different copper pad area.

図 148, 図 149 and 図 150 shows the transient junction-to-ambient thermal resistance ($Z_{\theta JA}$) vs time for 4-Layer PCB with copper-pad area of 4-cm^2, 8-cm^2 and 16-cm^2 respectively.

図 151, 図 152 and 図 153 shows the transient junction-to-ambient thermal resistance ($Z_{\Psi JB}$) vs time for 4-Layer PCB with copper-pad area of 4-cm^2, 8-cm^2 and 16-cm^2 respectively.

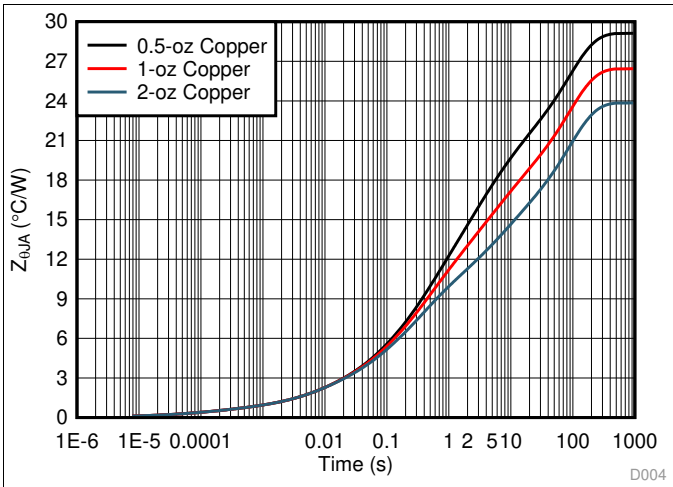


図 148. Transient Junction-to-Ambient Thermal Resistance ($Z_{\theta JA}$) vs Time for 4-Layer PCB with Copper-Pad Area of 4-cm^2

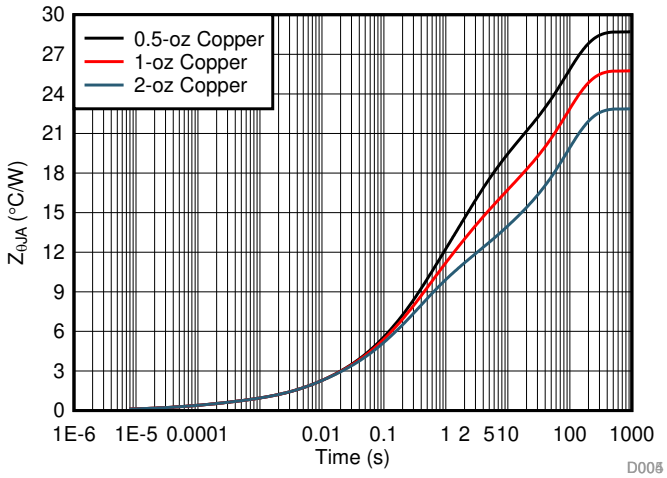


図 149. Transient Junction-to-Ambient Thermal Resistance ($Z_{\theta JA}$) vs Time for 4-Layer PCB with Copper-Pad Area of 8-cm^2

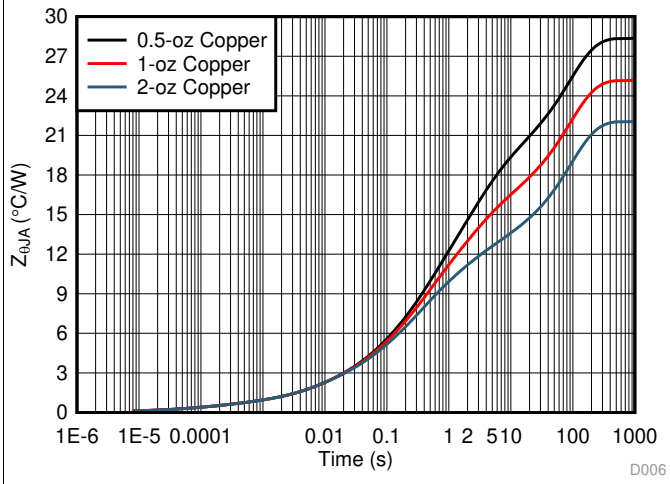


図 150. Transient Junction-to-Ambient Thermal Resistance ($Z_{\theta JA}$) vs Time for 4-Layer PCB with Copper-Pad Area of 16-cm^2

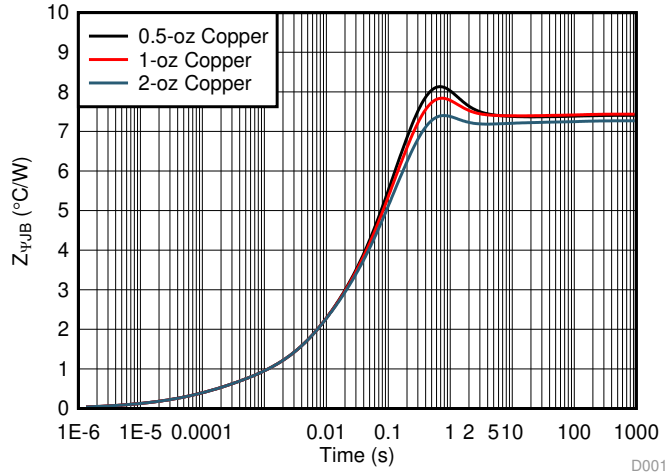


図 151. Transient Junction-to-Board Characterization ($Z_{\Psi JB}$) Parameter vs Time for 4-Layer PCB with Copper-Pad Area of 4-cm^2

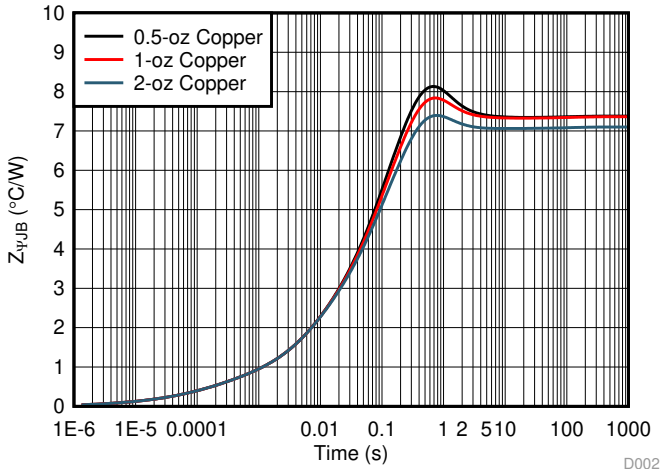


図 152. Transient Junction-to-Board Characterization ($Z_{\Psi JB}$) Parameter vs Time for 4-Layer PCB with Copper-Pad Area of 8-cm^2

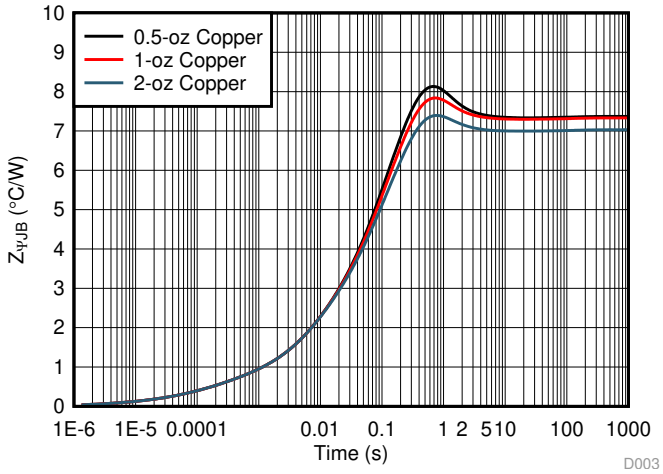


図 153. Transient Junction-to-Board Characterization ($Z_{\Psi JB}$) Parameter vs Time for 4-Layer PCB with Copper-Pad Area of 16-cm^2

9.3.5 Device Junction Temperature Estimation

The device junction temperature (T_J) is calculated by the power dissipation and the thermal parameters (Junction-to-Ambient Thermal Resistance ($R_{\theta JA}$)) for the particular PCB. For an ambient temperature of T_A and total power dissipation (P_{TOT}), the junction temperature (T_J) is calculated as shown in 式 18.

$$T_J = T_A + (P_{TOT} \times R_{\theta JA}) \quad (18)$$

Considering a 4-layer PCB, with copper thickness as 2-oz and copper-pad area as 16-cm^2, the junction-to-ambient thermal resistance ($R_{\theta JA}$) can be taken from 図 146 as 22°C/W.

By putting the value of total power dissipation (P_{TOT}) from 式 17 in 式 18 and taking ambient temperature (T_A) as 25°C, the junction temperature is calculated as shown in 式 19.

$$T_J = T_A + (P_{TOT} \times R_{\theta JA}) = 25°C + (2.3076\text{-W} \times 22°C/W) = 75.77\ °C \quad (19)$$

Hence, the power dissipation of 2.3076-W in the DRV89XX-Q1 device causes the junction temperature (T_J) to increase to 75.77°C. This junction temperature has a margin of 74.23°C before hitting the thermal shutdown limit.

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10 Power Supply Recommendations

The DRV89xx-Q1 device is designed to operate from an input voltage supply (VM) range from 4.5-V to 32-V. A 0.1-µF ceramic capacitor rated for VM must be placed as close to the device as possible. In addition, a bulk capacitor must be included on the VM pin but can be shared with the bulk bypass capacitance for the external power MOSFETs.

10.1 Bulk Capacitance Sizing

Having appropriate local bulk capacitance is an important factor in motor drive system design. It is generally beneficial to have more bulk capacitance, while the disadvantages are increased cost and physical size. The amount of local capacitance depends on a variety of factors including:

- The highest current required by the motor system
- The power supply's type, capacitance, and ability to source current
- The amount of parasitic inductance between the power supply and motor system
- The acceptable supply voltage ripple
- Type of motor (brushed DC, brushless DC, stepper)
- The motor startup and braking methods

The inductance between the power supply and motor drive system will limit the rate of change of current from the power supply. If the local bulk capacitance is too small, the system will respond to excessive current demands or dumps from the motor with a change in voltage. When adequate bulk capacitance is used, the motor voltage remains stable and high current can be quickly supplied.

The data sheet provides a recommended minimum value, but system level testing is required to determine the appropriate sized bulk capacitor.

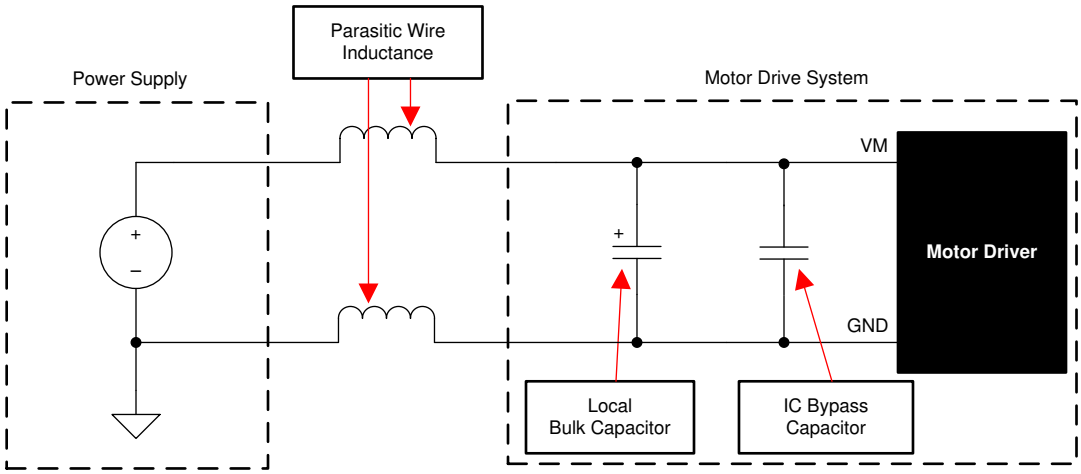


図 154. Motor Drive Power Supply Parasitic Example

11 Layout

11.1 Layout Guidelines

Bypass the VM pin to the GND pin using a low-ESR ceramic bypass capacitor with a recommended value of 0.1 μF. Place this capacitor as close to the VM pin as possible with a thick trace or ground plane connected to the PGND pin. Additionally, bypass the VM pin using a bulk capacitor rated for VM. This component can be electrolytic. This capacitance must be at least 10 μF.

Bypass the VDD pin to the GND pin with a 0.1-μF low-ESR ceramic capacitor rated for 6.3 V (X5R or X7R). Place this capacitor as close to the pin as possible and minimize the path from the capacitor to the AGND pin.

11.2 Layout Example

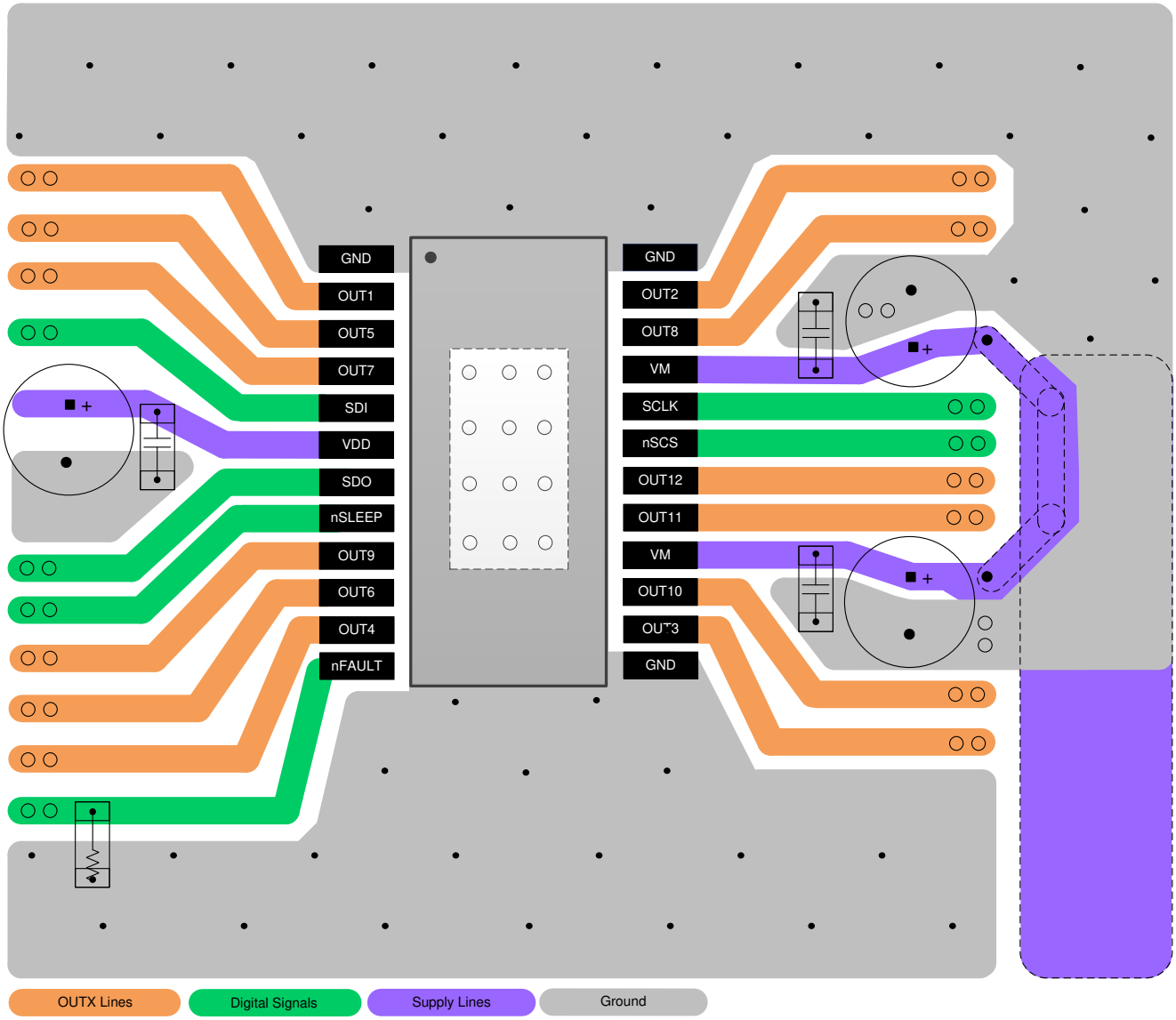


図 155. Layout Example

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12 デバイスおよびドキュメントのサポート

12.1 ドキュメントのサポート

12.1.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、*DRV8912-Q1 マルチ H ブリッジ・モーター・ドライバの評価モジュール*
- テキサス・インスツルメンツ、*『Best Practices for Board Layout of Motor Drivers』アプリケーション・レポート* (英語)

12.2 関連リンク

次の表に、クイック・アクセス・リンクを示します。カテゴリには、技術資料、サポートおよびコミュニティ・リソース、ツールとソフトウェア、およびご注文へのクイック・アクセスが含まれます。

表 96. 関連リンク

製品	プロダクト・フォルダ	ご注文はこちら	技術資料	ツールとソフトウェア	サポートとコミュニティ
DRV8904-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
DRV8906-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
DRV8908-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
DRV8910-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック
DRV8912-Q1	ここをクリック	ここをクリック	ここをクリック	ここをクリック	ここをクリック

12.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

12.4 コミュニティ・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

Linked content is provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

12.5 商標

E2E is a trademark of Texas Instruments.

12.6 静電気放電に関する注意事項

すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

12.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

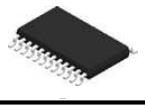
13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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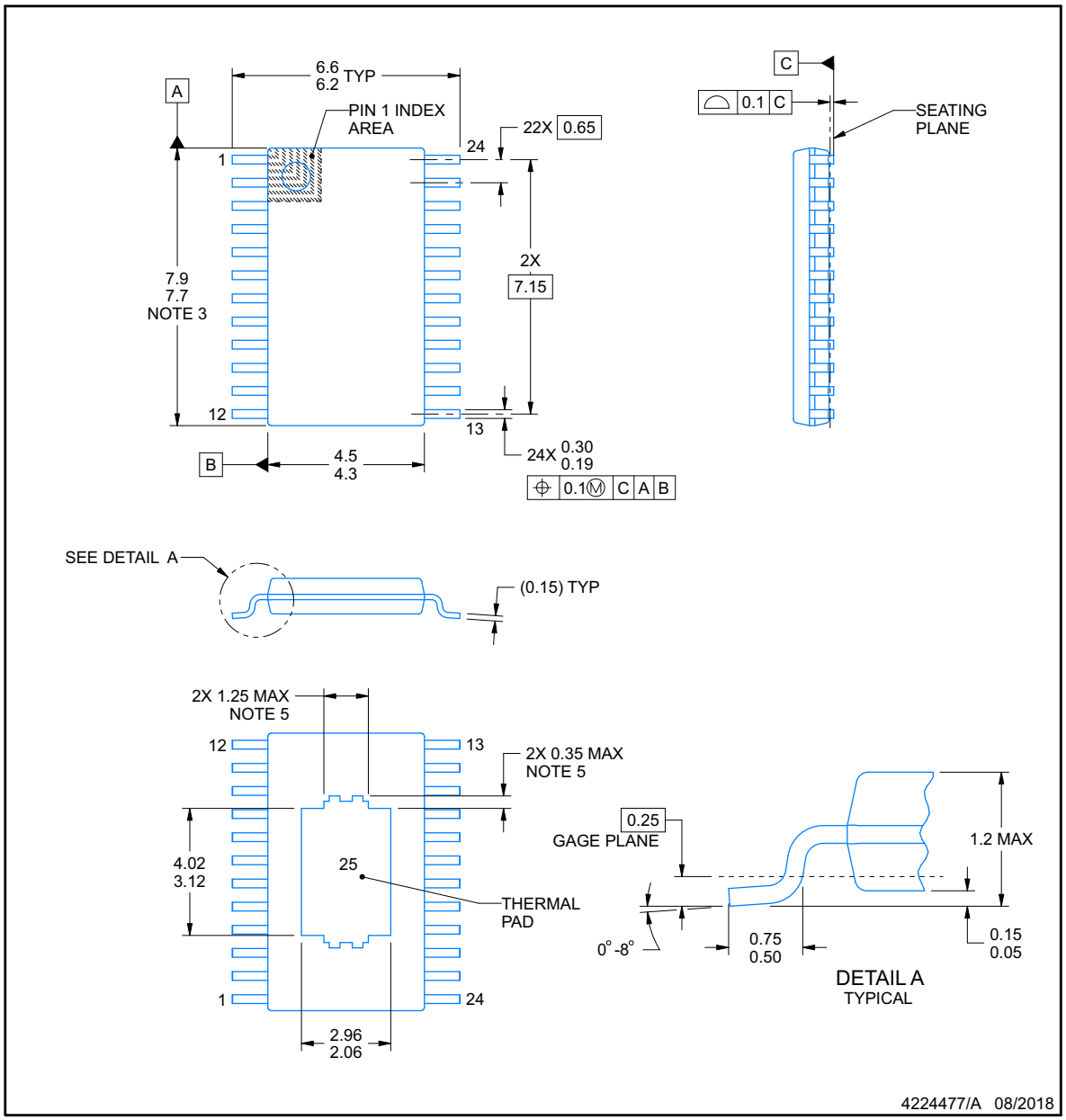
PACKAGE OUTLINE

PWP0024N



PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.

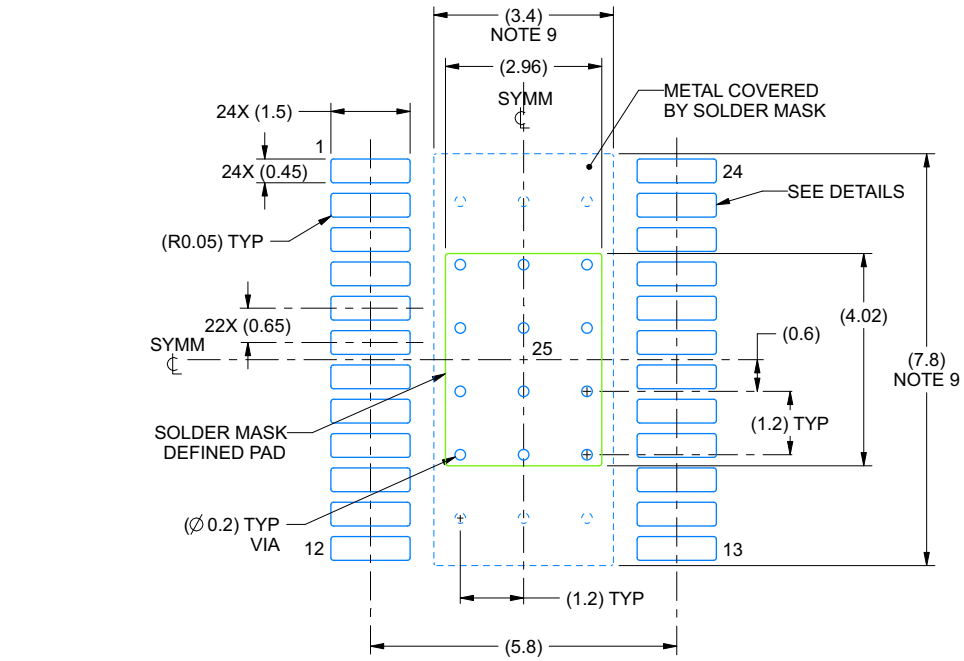
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EXAMPLE BOARD LAYOUT

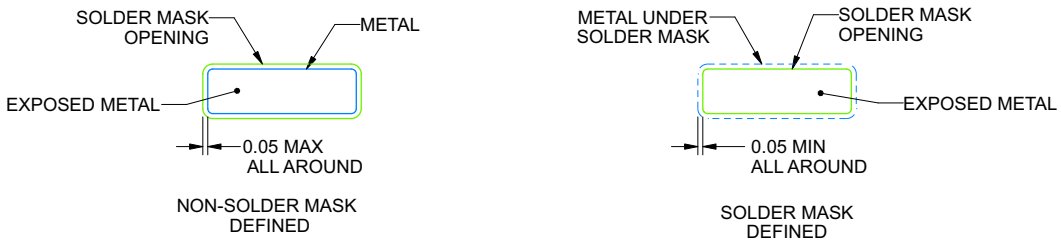
PWP0024N

PowerPAD™ TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



SOLDER MASK DETAILS

4224477/A 08/2018

NOTES: (continued)

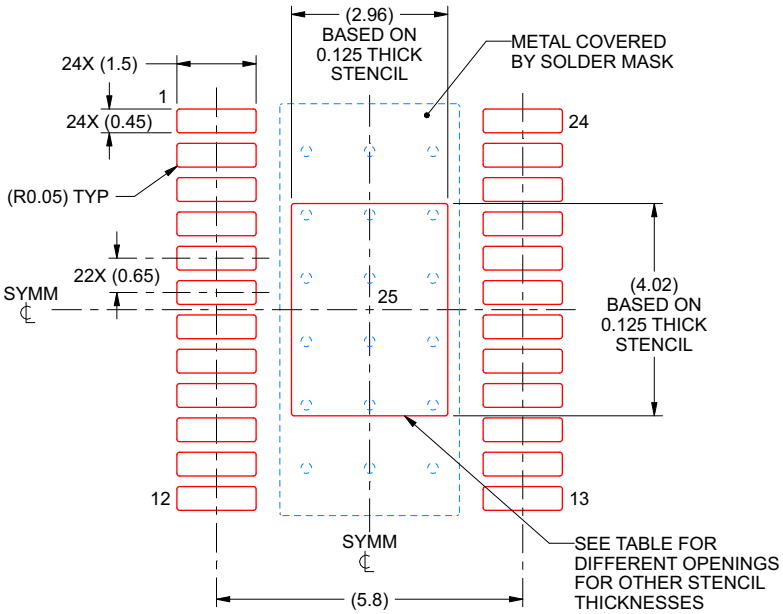
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.

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EXAMPLE STENCIL DESIGN

PWP0024N — **PowerPAD™ TSSOP - 1.2 mm max height**

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.31 X 4.49
0.125	2.96 X 4.02 (SHOWN)
0.15	2.70 X 3.67
0.175	2.50 X 3.40

4224477/A 08/2018

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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13.1 Package Option Addendum

13.1.1 Packaging Information

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish(3)	MSL Peak Temp (4)	Op Temp (°C)	Device Marking(5)(6)
PDRV8912QPWPRQ1	PREVIEW	HTSSOP	PWP	24	2000	TBD	CU NIPDAU	Level-3-260C-168hrs	-40 to 125	P8912

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PRE_PROD Unannounced device, not in production, not available for mass market, nor on the web, samples not available.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

(4) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(5) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device

(6) Multiple Device markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

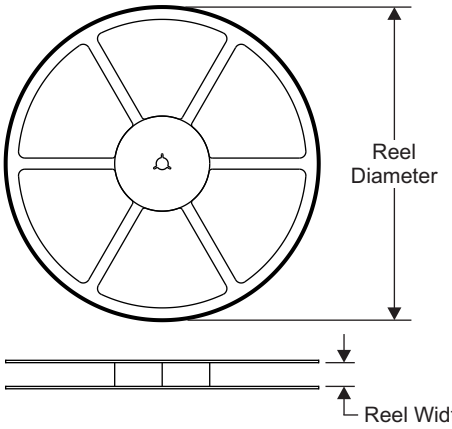
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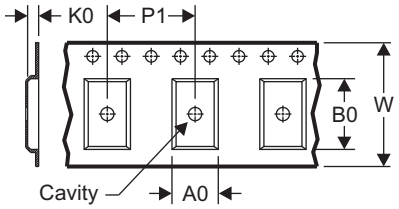
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13.1.2 Tape and Reel Information

REEL DIMENSIONS

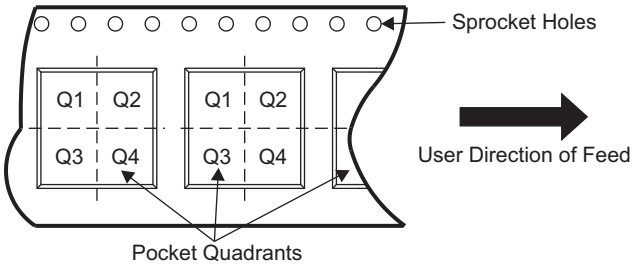


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

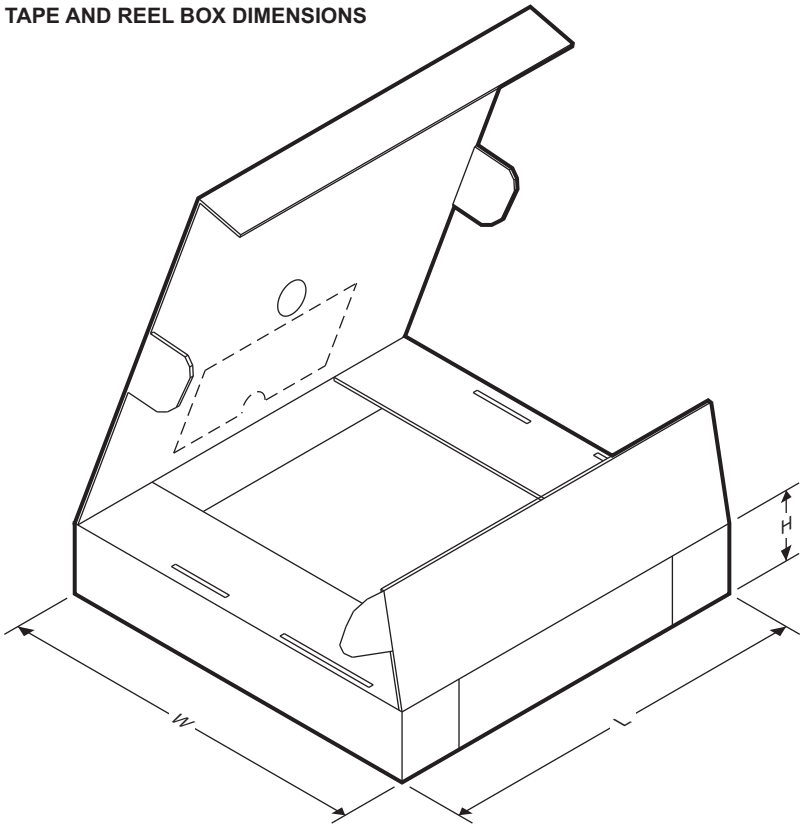
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PDRV8912QPWPRQ1	HTSSOP	PWP	24	2000	330	16.4	6.95	8.3	1.6	8.0	16	Q1

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TAPE AND REEL BOX DIMENSIONS



Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PDRV8912QPWPRQ1	HTSSOP	PWP	24	2000	367	367	38

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DRV8904QPWPRQ1	ACTIVE	HTSSOP	PWP	24	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8904	Samples
DRV8906QPWPRQ1	ACTIVE	HTSSOP	PWP	24	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8906	Samples
DRV8908QPWPRQ1	ACTIVE	HTSSOP	PWP	24	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8908	Samples
DRV8910QPWPRQ1	ACTIVE	HTSSOP	PWP	24	2000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8910	Samples
DRV8912QPWPRQ1	ACTIVE	HTSSOP	PWP	24	3000	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 125	DRV8912	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

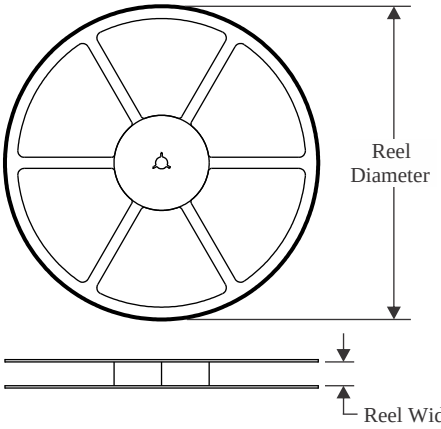
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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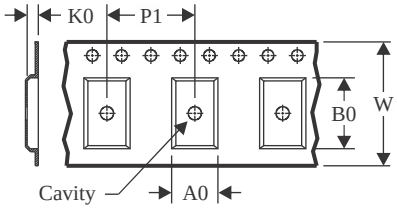
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

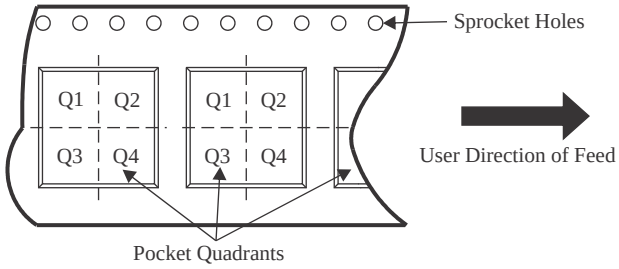


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

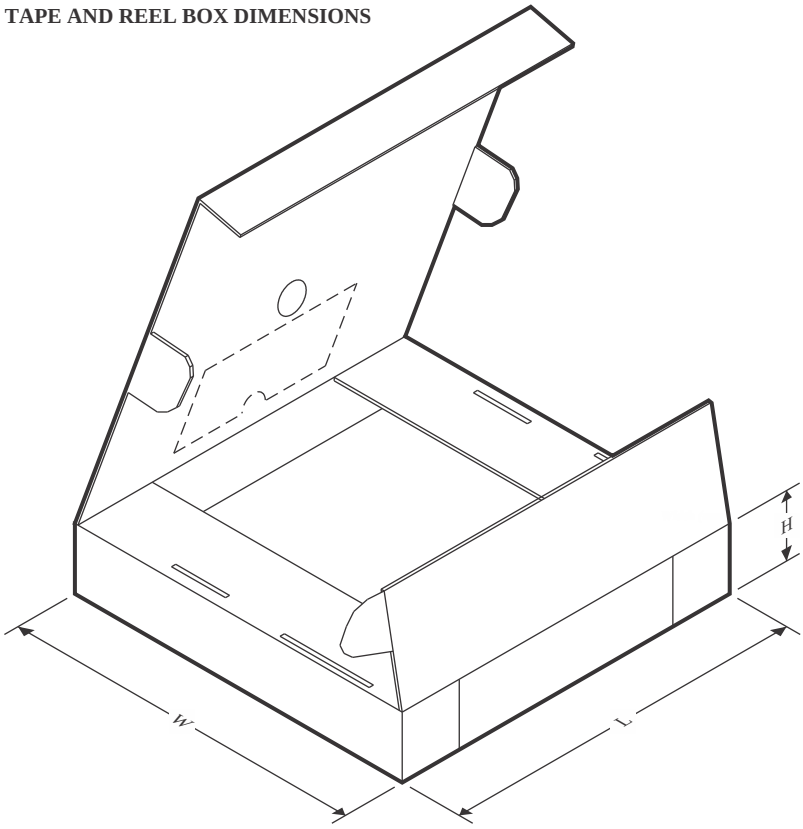
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
DRV8904QPWPRQ1	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
DRV8906QPWPRQ1	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
DRV8908QPWPRQ1	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
DRV8910QPWPRQ1	HTSSOP	PWP	24	2000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1
DRV8912QPWPRQ1	HTSSOP	PWP	24	3000	330.0	16.4	6.95	8.3	1.6	8.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
DRV8904QPWPRQ1	HTSSOP	PWP	24	2000	356.0	356.0	35.0
DRV8906QPWPRQ1	HTSSOP	PWP	24	2000	356.0	356.0	35.0
DRV8908QPWPRQ1	HTSSOP	PWP	24	2000	356.0	356.0	35.0
DRV8910QPWPRQ1	HTSSOP	PWP	24	2000	356.0	356.0	35.0
DRV8912QPWPRQ1	HTSSOP	PWP	24	3000	356.0	356.0	35.0

GENERIC PACKAGE VIEW

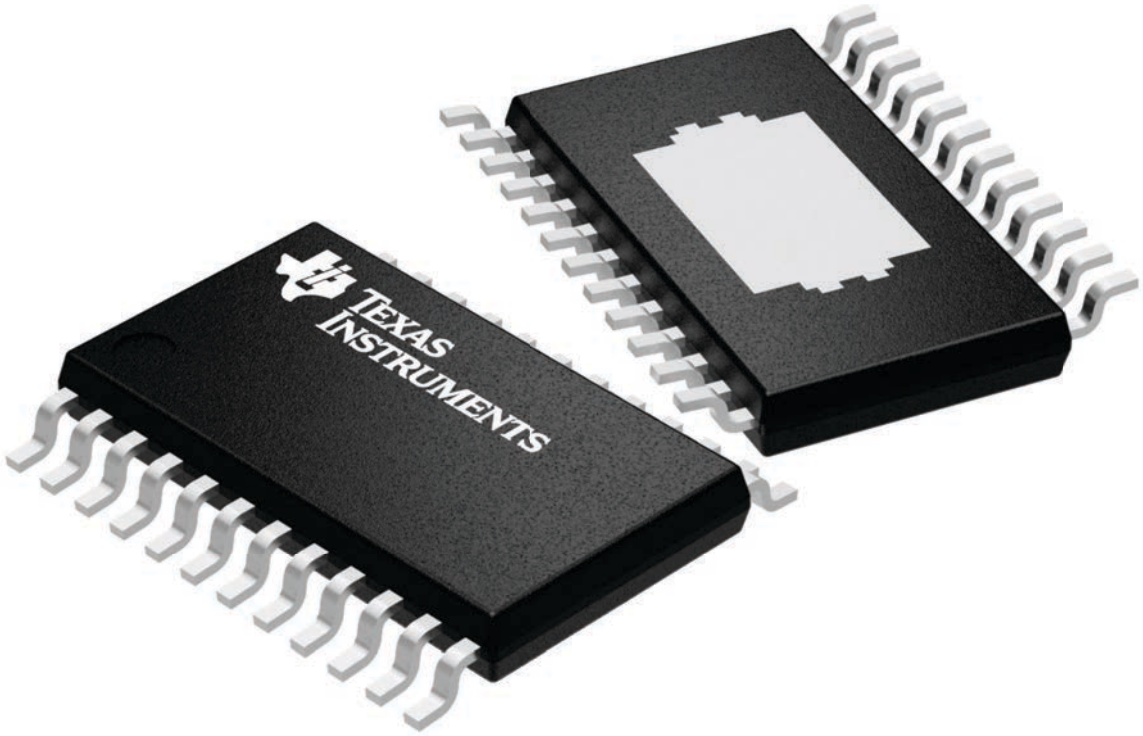
PWP 24

PowerPAD™ TSSOP - 1.2 mm max height

4.4 x 7.6, 0.65 mm pitch

PLASTIC SMALL OUTLINE

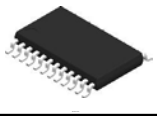
This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224742/B

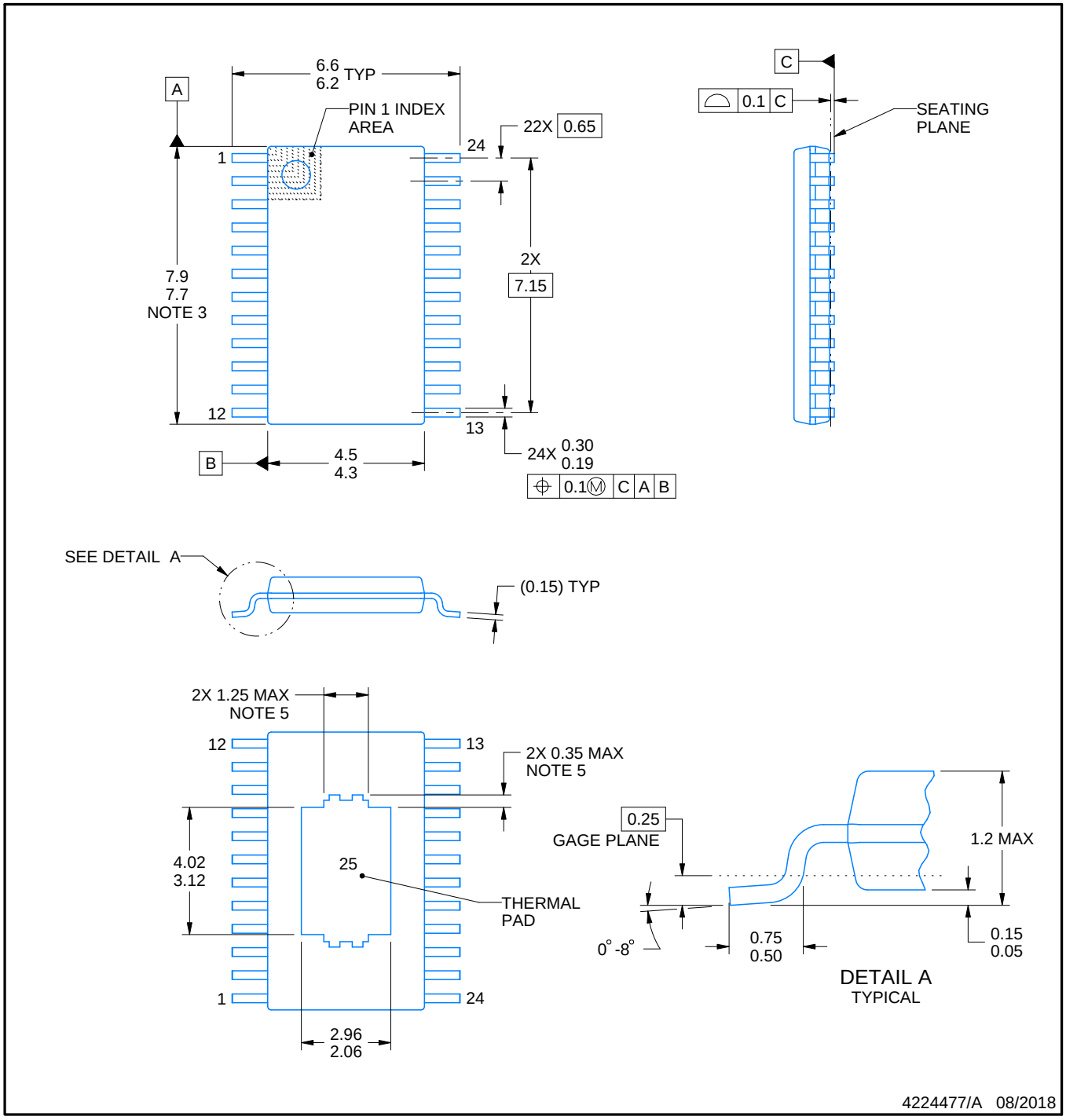
PACKAGE OUTLINE

PWP0024N



PowerPAD™ TSSOP - 1.2 mm max height

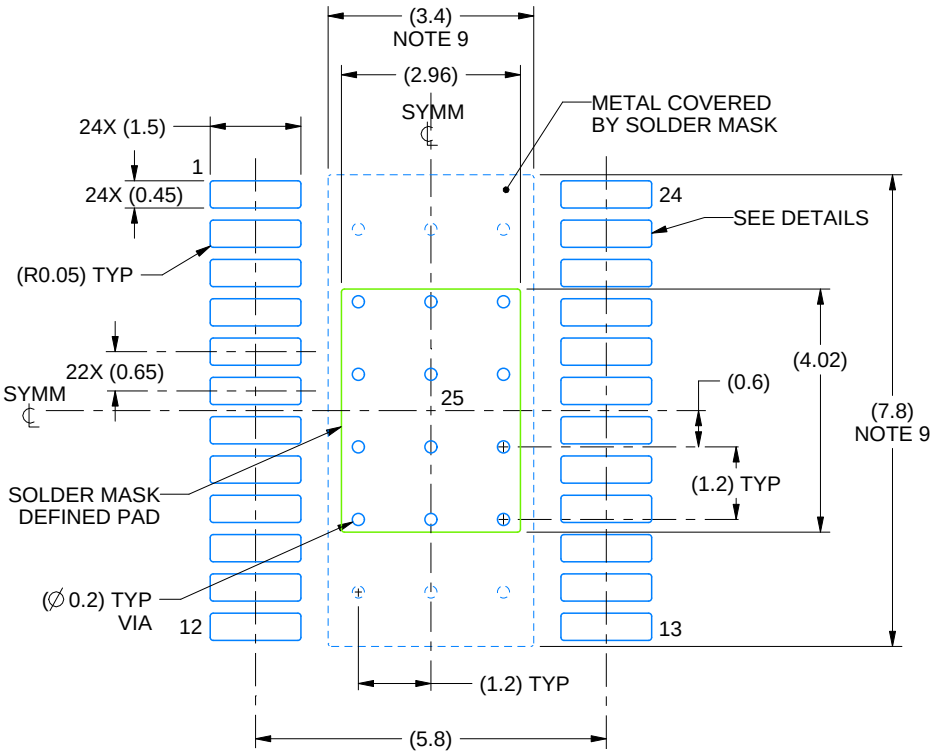
SMALL OUTLINE PACKAGE



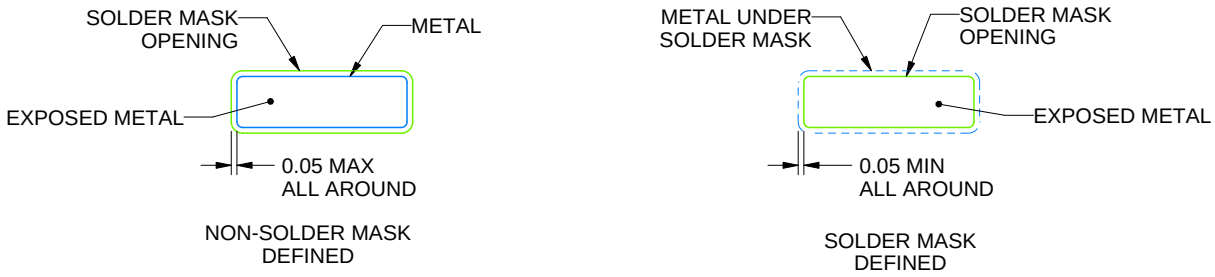
PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. Reference JEDEC registration MO-153.
5. Features may differ or may not be present.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X

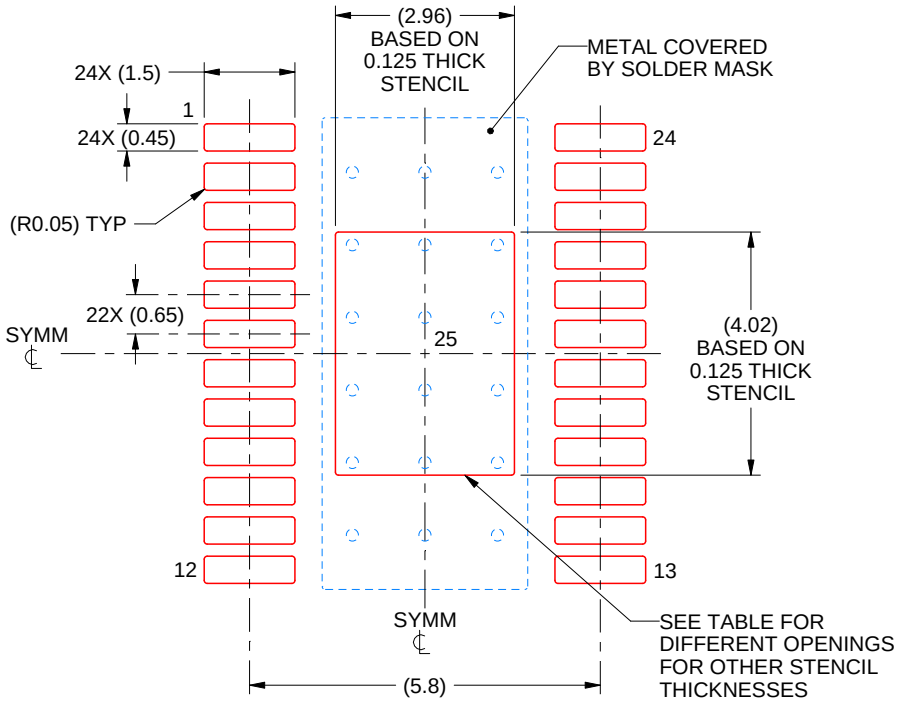


SOLDER MASK DETAILS

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NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature numbers SLMA002 (www.ti.com/lit/slma002) and SLMA004 (www.ti.com/lit/slma004).
9. Size of metal pad may vary due to creepage requirement.
10. Vias are optional depending on application, refer to device data sheet. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 8X

STENCIL THICKNESS	SOLDER STENCIL OPENING
0.1	3.31 X 4.49
0.125	2.96 X 4.02 (SHOWN)
0.15	2.70 X 3.67
0.175	2.50 X 3.40

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NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

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