



AMC1100 完全差動型絶縁アンプ

1 特長

- シャント抵抗に対して最適化された $\pm 250\text{mV}$ の入力電圧範囲
- 非常に小さい非直線性: 0.075% 以下 (5V)
- 小さいオフセット誤差: 1.5mV 以下
- 低ノイズ: $3.1\text{mV}_{\text{RMS}}$ (標準値)
- 小さいハイサイド消費電流:
8mA 以下 (5V)
- 入力帯域幅: 60kHz 以上
- 固定ゲイン: 8 (0.5% 精度)
- 高い同相除去比: 108dB
- ローサイド動作: 3.3V
- 安全関連の認定
 - DIN VDE V0884-11: 2017-01 に準拠した基礎絶縁耐圧: 4250V_{PK}
 - UL 1577 に準拠した絶縁耐圧: $3005\text{V}_{\text{RMS}}$ (1 分間)
 - CAN/CSA 番号 5A - 部品承認通達および DIN EN 61010-1 規格
 - 動作電圧: $1200\text{V}_{\text{PEAK}}$
 - 過渡耐性: $2.5\text{kV}/\mu\text{s}$ 以上
- 拡張産業用温度範囲全体にわたって仕様を完全に規定

2 アプリケーション

次の用途の、シャント抵抗を使用した電流センシング

- 電気メータ
- ストリング・インバータ
- 電力測定アプリケーション

3 概要

AMC1100 は、磁気干渉に高い耐性がある二酸化ケイ素 (SiO_2) のバリアによって入力回路から分離された出力を持つ高精度の絶縁アンプです。この絶縁バリアは、DIN VDE V 0884-11: 2017-01 および UL1577 に準拠した最大 $4250\text{V}_{\text{PEAK}}$ のガルバニック絶縁を備えていることが認定されています。このデバイスを絶縁型電源とともに使用することで、高い同相電圧ラインからノイズ電流がローカル・グランドへ侵入するのを防ぎ、ノイズに敏感な回路への干渉と損傷を防止できます。

AMC1100 の入力は、シャント抵抗またはその他の低電圧レベル信号源と直接接続できるように最適化されています。このデバイスの非常に優れた性能は、電力量計アプリケーションの高精度電流および電圧計測を可能にします。出力信号の同相電圧は、3V と 5V のどちらかのローサイド電源に合わせて自動的に調整されます。

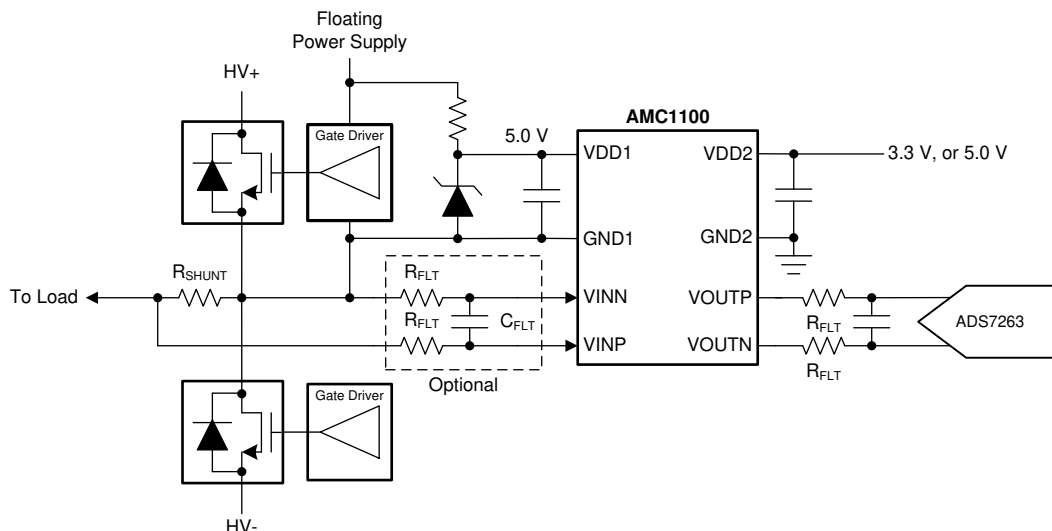
AMC1100 は拡張産業用温度範囲の $-40^\circ\text{C} \sim +105^\circ\text{C}$ で完全に動作が規定されており、SMD 型の幅広 SOIC-8 (DWV) とガルウィング 8 (DUB) パッケージで供給されます。

製品情報⁽¹⁾

型番	パッケージ	本体サイズ(公称)
AMC1100	SOP (8)	9.50 mm×6.57 mm
	SOIC (8)	5.85mm×7.50mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。

概略回路図



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4 改訂履歴

Revision A (December 2014) から Revision B に変更

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・ 「特長」の「安全関連の認定」箇条書き項目で、認定の詳細を ISO 標準に従い 変更	1
・ 「特長」箇条書き項目の標準寿命を 削除	1
・ 最終機器へのリンクを追加して「アプリケーション」セクションを 変更	1
・ 「概要」セクションの IEC60747-5-2 を DIN VDE V 0884-11: 2017-01 に 変更	1
・ ページ 1 の図にタイトルを追加して 変更	1
・ Added Power Ratings table	4
・ Changed Insulation Specifications table per ISO standard	5
・ Added DWV-package related details in Insulation Specifications table	5
・ Changed Safety-Related Certification table per ISO standard	6
・ Changed Safety Limiting Values table per ISO standard	6
・ Deleted VDD1 and VDD2 from Electrical Characteristics table (repeated in Recommended Operating Conditions table)	7
・ Added Insulation Characteristics Curves section	8
・ Changed Zener Diode Based High-Side Supply figure	21

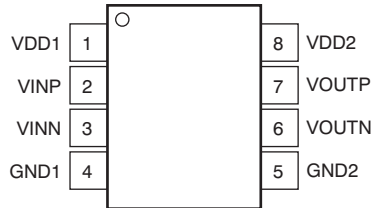
2012年4月発行のものから更新

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・ 最新のデータシート標準に合わせてフォーマットを変更	1
・ 「ESD 定格」表、「機能説明」セクション、「デバイスの機能モード」セクション、「アプリケーションと実装」セクション、「電源に関する推奨事項」セクション、「レイアウト」セクション、「デバイスおよびドキュメントのサポート」セクション、「メカニカル、パッケージ、および注文情報」セクションを追加	1
・ ドキュメントに DWV パッケージを追加	1
・ Deleted Package and Ordering Information section	3

5 Pin Configuration and Functions

**DUB and DWV Packages
SOP-8 and SOIC-8
(Top View)**



Pin Descriptions

PIN		FUNCTION	DESCRIPTION
NAME	NO.		
GND1	4	Power	High-side analog ground
GND2	5	Power	Low-side analog ground
VDD1	1	Power	High-side power supply
VDD2	8	Power	Low-side power supply
VINN	3	Analog input	Inverting analog input
VINP	2	Analog input	Noninverting analog input
VOUTN	6	Analog output	Inverting analog output
VOUTP	7	Analog output	Noninverting analog output

6 Specifications

6.1 Absolute Maximum Ratings

see⁽¹⁾

	MIN	MAX	UNIT
Supply voltage, VDD1 to GND1 or VDD2 to GND2	–0.5	6	V
Analog input voltage at VINP, VINN	GND1 – 0.5	VDD1 + 0.5	V
Input current to any pin except supply pins		±10	mA
Maximum junction temperature, T _J Max		150	°C
Storage temperature range, T _{stg}	–65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

6.2 ESD Ratings

			VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 ⁽¹⁾	±2500	V
		Charged device model (CDM), per JEDEC specification JESD22-C101 ⁽²⁾	±1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.

- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
T_A	Operating ambient temperature range	–40		105	°C
VDD1	High-side power supply	4.5	5.0	5.5	V
VDD2	Low-side power supply	2.7	5.0	5.5	V

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾		AMC1100		UNIT
		DUB (SOP)	DWV (SOIC)	
		8 PINS	8 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	75.1	102.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	61.6	49.8	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	39.8	56.6	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	27.2	16.0	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	39.4	55.2	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	N/A	°C/W

(1) For more information about traditional and new thermal metrics, see the [Semiconductor and IC package thermal metrics application report](#).

6.5 Power Ratings

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
P_D	Maximum power dissipation (both sides)	VDD1 = VDD2 = 5.5 V			82.5	mW
		VDD1 = 5.5 V, VDD2 = 3.6 V			65.6	
P_{D1}	Maximum power dissipation (high-side supply)	VDD1 = 5.5 V			44.0	mW
P_{D2}	Maximum power dissipation (low-side supply)	VDD2 = 5.5 V			38.5	mW
		VDD2 = 3.6 V			21.6	

6.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

PARAMETER		TEST CONDITIONS	VALUE	UNIT
GENERAL				
CLR	External clearance ⁽¹⁾	Shortest pin-to-pin distance through air, DUB package	≥ 7	mm
		Shortest pin-to-pin distance through air, DWV package	≥ 8.5	
CPG	External creepage ⁽¹⁾	Shortest pin-to-pin distance across the package surface, DUB package	≥ 7	mm
		Shortest pin-to-pin distance across the package surface, DWV package	≥ 8.5	
DTI	Distance through insulation	Minimum internal gap (internal clearance) of the insulation	≥ 0.014	mm
CTI	Comparative tracking index	DIN EN 60112 (VDE 0303-11); IEC 60112, DUB package	≥ 400	V
		DIN EN 60112 (VDE 0303-11); IEC 60112, DWV package	≥ 600	
	Material group	According to IEC 60664-1, DUB package	II	
		According to IEC 60664-1, DWV package	I	
	Overvoltage category per IEC 60664-1	Rated mains voltage ≤ 300 V _{RMS}	I-IV	
		Rated mains voltage ≤ 600 V _{RMS}	I-III	
DIN VDE V 0884-11: 2017-01 ⁽²⁾				
V _{IORM}	Maximum repetitive peak isolation voltage	At ac voltage (bipolar)	1200	V _{PK}
V _{IOWM}	Maximum-rated isolation working voltage	At ac voltage (sine wave)	849	V _{RMS}
		At dc voltage	1200	V _{DC}
V _{IOTM}	Maximum transient isolation voltage	V _{TEST} = V _{IOTM} , t = 60 s (qualification test)	4250	V _{PK}
		V _{TEST} = 1.2 × V _{IOTM} , t = 1 s (100% production test)	5100	
V _{IOSM}	Maximum surge isolation voltage ⁽³⁾	Test method per IEC 60065, 1.2/50-μs waveform, V _{TEST} = 1.3 × V _{IOSM} = 6000 V _{PK} (qualification)	4615	V _{PK}
q _{pd}	Apparent charge ⁽⁴⁾	Method a, after input/output safety test subgroup 2 / 3, V _{ini} = V _{IOTM} , t _{ini} = 60 s, V _{pd(m)} = 1.2 × V _{IORM} = 1440 V _{PK} , t _m = 10 s	≤ 5	pC
		Method a, after environmental tests subgroup 1, V _{ini} = V _{IOTM} , t _{ini} = 60 s, V _{pd(m)} = 1.3 × V _{IORM} = 1560 V _{PK} , t _m = 10 s	≤ 5	
		Method b1, at routine test (100% production) and preconditioning (type test), V _{ini} = V _{IOTM} , t _{ini} = 1 s, V _{pd(m)} = 1.5 × V _{IORM} = 1800 V _{PK} , t _m = 1 s	≤ 5	
C _{IO}	Barrier capacitance, input to output ⁽⁵⁾	V _{IO} = 0.5 V _{PP} at 1 MHz	1.2	pF
R _{IO}	Insulation resistance, input to output ⁽⁵⁾	V _{IO} = 500 V at T _A < 85°C	> 10 ¹²	Ω
		V _{IO} = 500 V at 85°C < T _A < 105°C	> 10 ¹¹	
		V _{IO} = 500 V at T _S = 150°C	> 10 ⁹	
	Pollution degree		2	
	Climatic category		40/125/21	
UL1577				
V _{ISO}	Withstand isolation voltage	V _{TEST} = V _{ISO} = 3005 V _{RMS} or 4250 V _{DC} , t = 60 s (qualification), V _{TEST} = 1.2 × V _{ISO} = 3606 V _{RMS} , t = 1 s (100% production test)	3005	V _{RMS}

- (1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves and ribs on the PCB are used to help increase these specifications.
- (2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
- (3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.
- (4) Apparent charge is electrical discharge caused by a partial discharge (pd).
- (5) All pins on each side of the barrier are tied together, creating a two-pin device.

6.7 Safety-Related Certifications

VDE	UL	CSA
Certified according to DIN VDE V 0884-11: 2017-01 and DIN EN 61010-1 (VDE 0411-1) : 2011-07	Recognized under 1577 component recognition program	Recognized under CSA component acceptance NO 5 program, IEC 60950-1, and IEC 61010-1
Basic insulation	Single protection	Basic insulation
Certificate number: 40047657	File number: E181974	Certificate number: 2643952

6.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_S	Safety input, output, or supply current	DUB package, $R_{\theta JA} = 75.1^\circ\text{C/W}$, $T_J = 150^\circ\text{C}$, $T_A = 25^\circ\text{C}$, $VDD1 = VDD2 = 5.5\text{ V}$, see Figure 1			302	mA
		DWV package, $R_{\theta JA} = 102.8^\circ\text{C/W}$, $T_J = 150^\circ\text{C}$, $T_A = 25^\circ\text{C}$, $VDD1 = VDD2 = 5.5\text{ V}$, see Figure 1			221	
P_S	Safety input, output, or total power ⁽¹⁾	DUB package, $R_{\theta JA} = 75.1^\circ\text{C/W}$, $T_J = 150^\circ\text{C}$, $T_A = 25^\circ\text{C}$, see Figure 2			1664	mW
		DWV package, $R_{\theta JA} = 102.8^\circ\text{C/W}$, $T_J = 150^\circ\text{C}$, $T_A = 25^\circ\text{C}$, see Figure 2			1216	mW
T_S	Maximum safety temperature				150	$^\circ\text{C}$

- (1) The maximum safety temperature, T_S , has the same value as the maximum junction temperature, T_J , specified for the device. The I_S and P_S parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of I_S and P_S . These limits vary with the ambient temperature, T_A .

The junction-to-air thermal resistance, $R_{\theta JA}$, in the [Thermal Information](#) table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:

$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.

$T_{J(\text{max})} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(\text{max})}$ is the maximum junction temperature.

$P_S = I_S \times VDD1_{\text{max}} + I_S \times VDD2_{\text{max}}$, where $VDD1_{\text{max}}$ is the maximum high-side supply voltage and $VDD2_{\text{max}}$ is the maximum low-side supply voltage.

6.9 Electrical Characteristics

All minimum and maximum specifications are at $T_A = -40^{\circ}\text{C}$ to $+105^{\circ}\text{C}$ and are within the specified voltage range, unless otherwise noted. Typical values are at $T_A = +25^{\circ}\text{C}$, $V_{DD1} = 5\text{ V}$, and $V_{DD2} = 3.3\text{ V}$.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT						
	Maximum input voltage before clipping	$V_{INP} - V_{INN}$		± 320		mV
	Differential input voltage	$V_{INP} - V_{INN}$	-250		250	mV
V_{CM}	Common-mode operating range		-0.16		V_{DD1}	V
V_{OS}	Input offset voltage		-1.5	± 0.2	1.5	mV
TCV_{OS}	Input offset thermal drift		-10	± 1.5	10	$\mu\text{V/K}$
CMRR	Common-mode rejection ratio	V_{IN} from 0 V to 5 V at 0 Hz		108		dB
		V_{IN} from 0 V to 5 V at 50 kHz		95		dB
C_{IN}	Input capacitance to GND1	V_{INP} or V_{INN}		3		pF
C_{IND}	Differential input capacitance			3.6		pF
R_{IN}	Differential input resistance			28		k Ω
	Small-signal bandwidth		60	100		kHz
OUTPUT						
	Nominal gain			8		
G_{ERR}	Gain error	Initial, at $T_A = +25^{\circ}\text{C}$	-0.5%	$\pm 0.05\%$	0.5%	
			-1%	$\pm 0.05\%$	1%	
TCG_{ERR}	Gain error thermal drift			± 56		ppm/K
	Nonlinearity	$4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$	-0.075%	$\pm 0.015\%$	0.075%	
		$2.7\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$	-0.1%	$\pm 0.023\%$	0.1%	
	Nonlinearity thermal drift			2.4		ppm/K
	Output noise	$V_{INP} = V_{INN} = 0\text{ V}$		3.1		mV _{RMS}
PSRR	Power-supply rejection ratio	vs V_{DD1} , 10-kHz ripple		80		dB
		vs V_{DD2} , 10-kHz ripple		61		dB
	Rise-and-fall time	0.5-V step, 10% to 90%		3.66	6.6	μs
	V_{IN} to V_{OUT} signal delay	0.5-V step, 50% to 10%, unfiltered output		1.6	3.3	μs
		0.5-V step, 50% to 50%, unfiltered output		3.15	5.6	μs
		0.5-V step, 50% to 90%, unfiltered output		5.26	9.9	μs
CMTI	Common-mode transient immunity	$V_{CM} = 1\text{ kV}$	2.5	3.75		kV/ μs
	Output common-mode voltage	$2.7\text{ V} \leq V_{DD2} \leq 3.6\text{ V}$	1.15	1.29	1.45	V
		$4.5\text{ V} \leq V_{DD2} \leq 5.5\text{ V}$	2.4	2.55	2.7	V
	Short-circuit current			20		mA
R_{OUT}	Output resistance			2.5		Ω
POWER SUPPLY						
I_{DD1}	High-side supply current			5.4	8	mA
I_{DD2}	Low-side supply current	$2.7\text{ V} < V_{DD2} < 3.6\text{ V}$		3.8	6	mA
		$4.5\text{ V} < V_{DD2} < 5.5\text{ V}$		4.4	7	mA
P_{DD1}	High-side power dissipation			27.0	44.0	mW
P_{DD2}	Low-side power dissipation	$2.7\text{ V} < V_{DD2} < 3.6\text{ V}$		11.4	21.6	mW
		$4.5\text{ V} < V_{DD2} < 5.5\text{ V}$		22.0	38.5	mW

6.10 Insulation Characteristics Curves

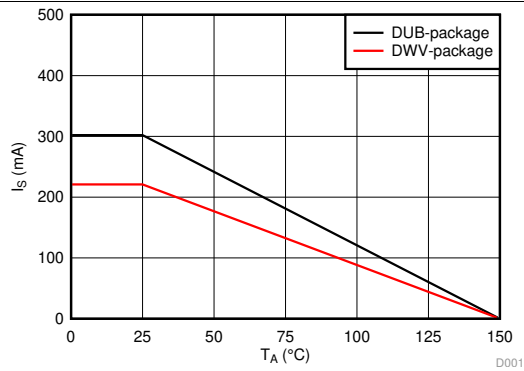


Figure 1. Thermal Derating Curve for Safety-Limiting Current per VDE

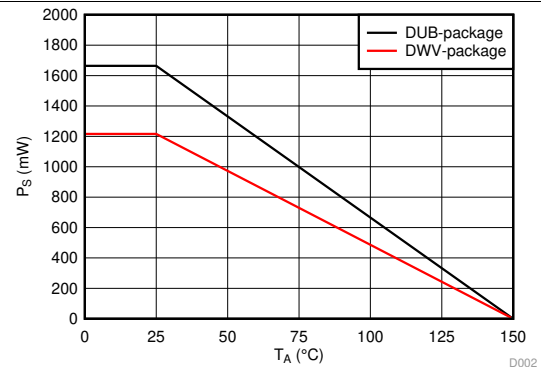


Figure 2. Thermal Derating Curve for Safety-Limiting Power per VDE

6.11 Typical Characteristics

At $V_{DD1} = V_{DD2} = 5\text{ V}$, $V_{INP} = -250\text{ mV}$ to $+250\text{ mV}$, and $V_{INN} = 0\text{ V}$, unless otherwise noted.

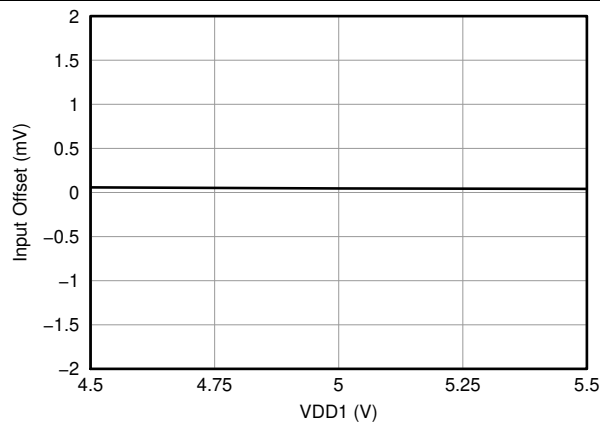


Figure 3. Input Offset vs High-Side Supply Voltage

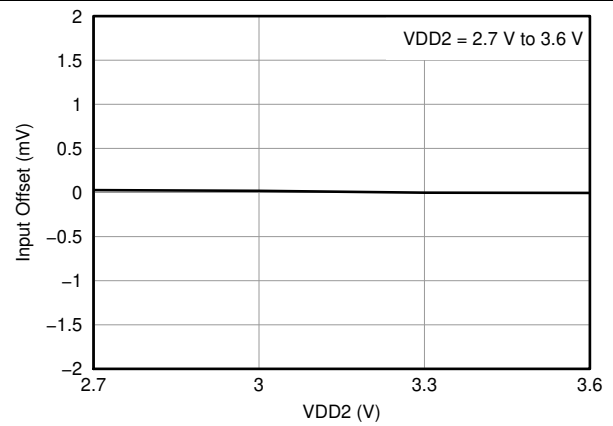


Figure 4. Input Offset vs Low-Side Supply Voltage

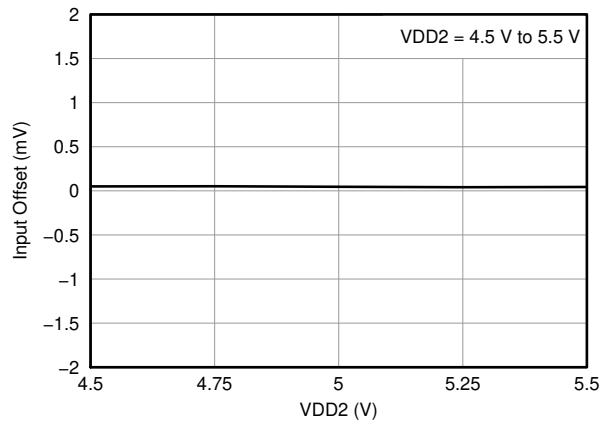


Figure 5. Input Offset vs Low-Side Supply Voltage

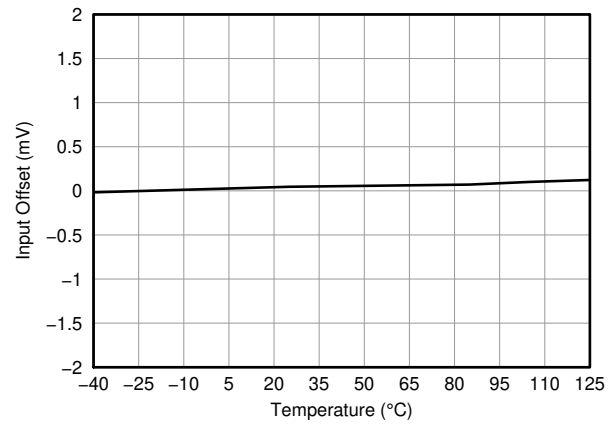


Figure 6. Input Offset vs Temperature

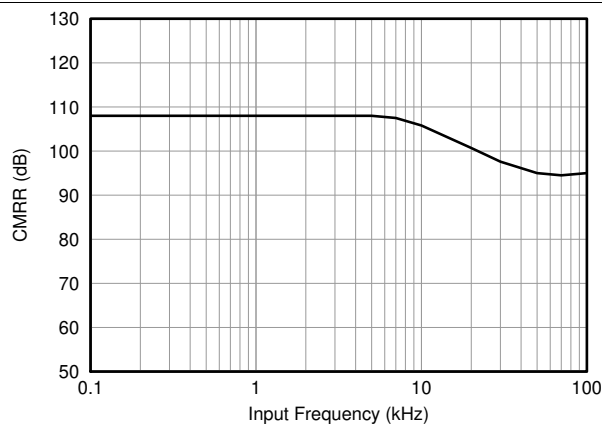


Figure 7. Common-Mode Rejection Ratio vs Input Frequency

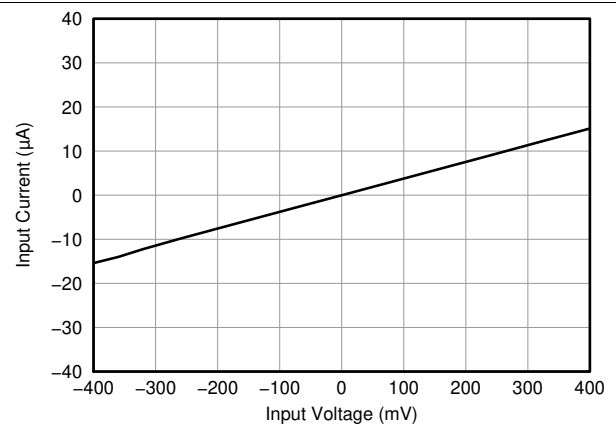


Figure 8. Input Current vs Input Voltage

Typical Characteristics (continued)

At $V_{DD1} = V_{DD2} = 5\text{ V}$, $V_{INP} = -250\text{ mV}$ to $+250\text{ mV}$, and $V_{INN} = 0\text{ V}$, unless otherwise noted.

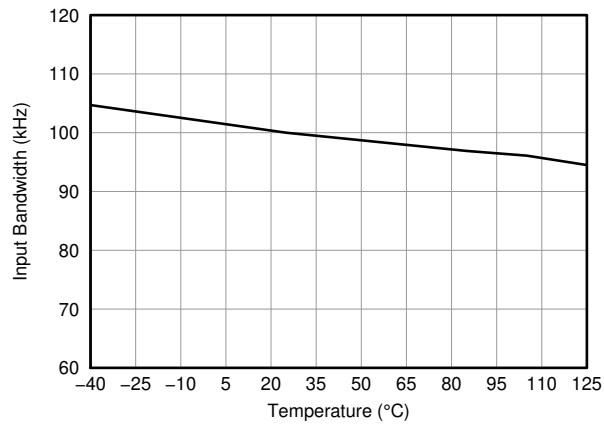


Figure 9. Input Bandwidth vs Temperature

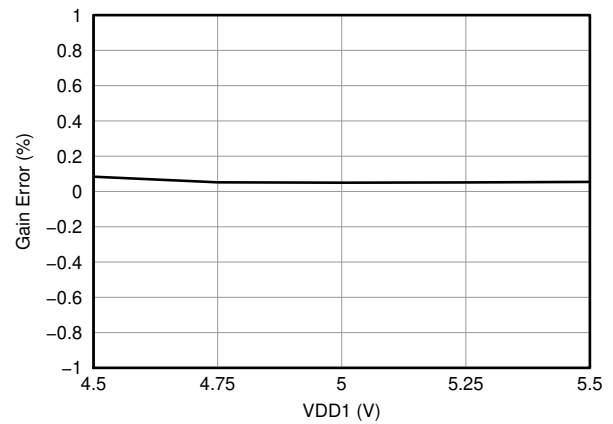


Figure 10. Gain Error vs High-Side Supply Voltage

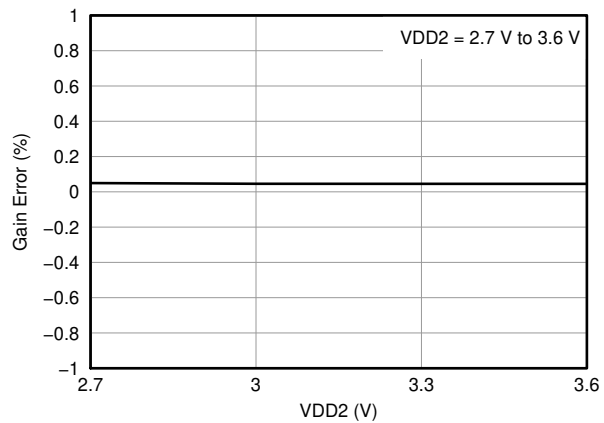


Figure 11. Gain Error vs Low-Side Supply Voltage

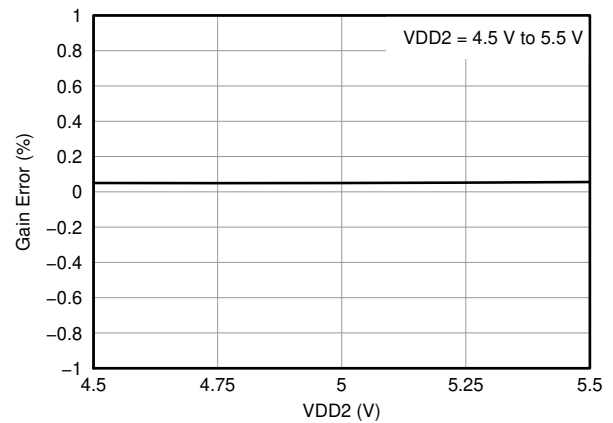


Figure 12. Gain Error vs Low-Side Supply Voltage

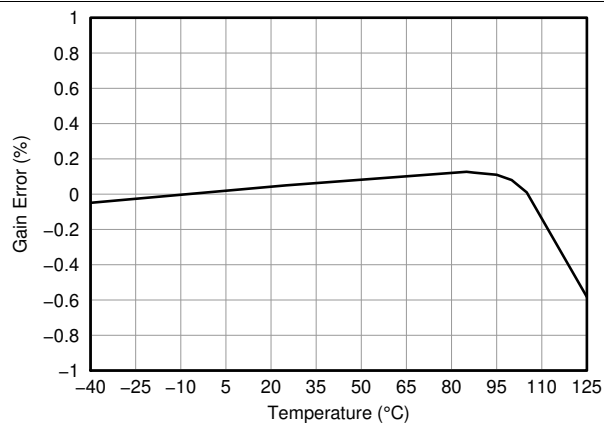


Figure 13. Gain Error vs Temperature

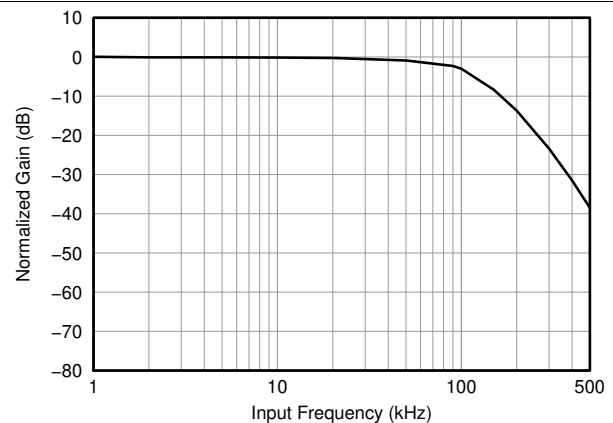


Figure 14. Normalized Gain vs Input Frequency

Typical Characteristics (continued)

At $V_{DD1} = V_{DD2} = 5\text{ V}$, $V_{INP} = -250\text{ mV}$ to $+250\text{ mV}$, and $V_{INN} = 0\text{ V}$, unless otherwise noted.

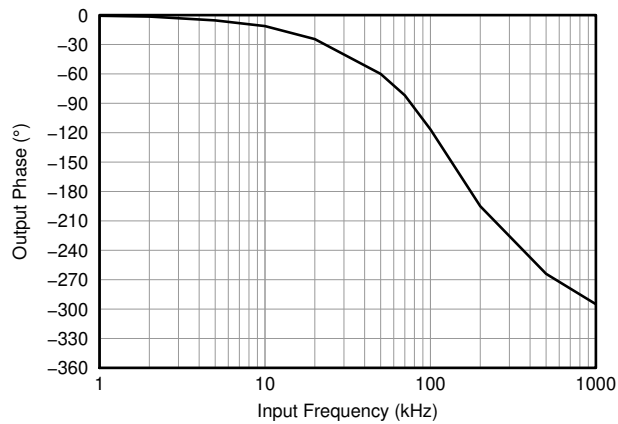


Figure 15. Output Phase vs Input Frequency

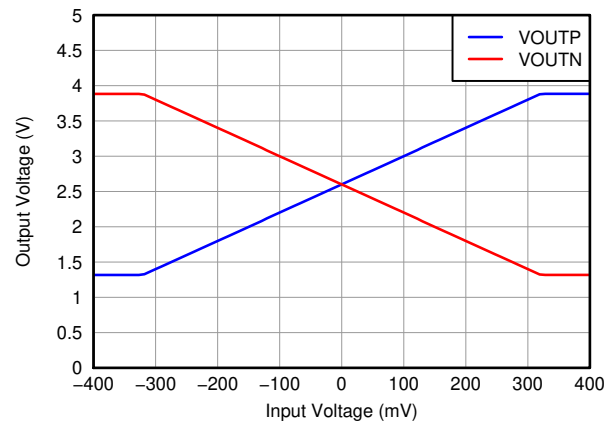


Figure 16. Output Voltage vs Input Voltage

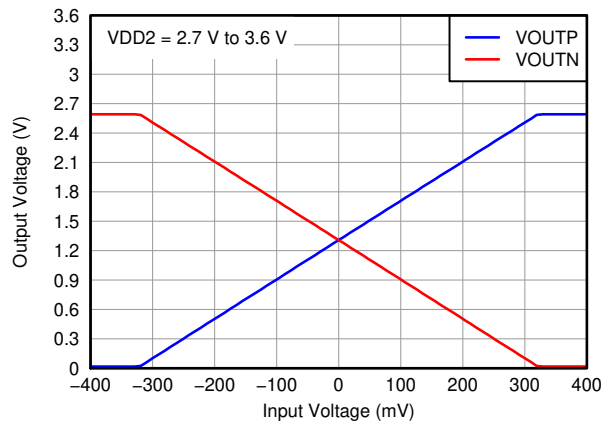


Figure 17. Output Voltage vs Input Voltage

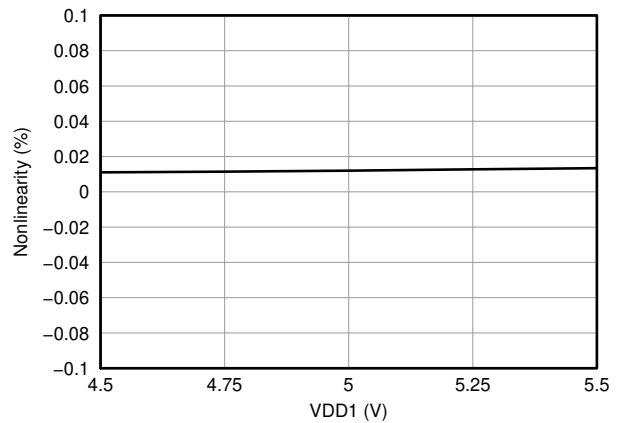


Figure 18. Nonlinearity vs High-Side Supply Voltage

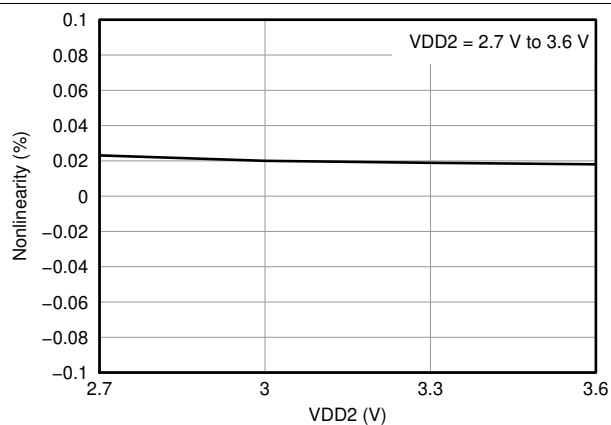


Figure 19. Nonlinearity vs Low-Side Supply Voltage

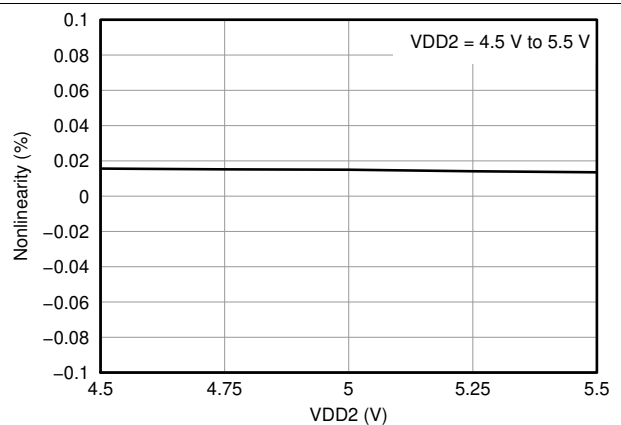


Figure 20. Nonlinearity vs Low-Side Supply Voltage

Typical Characteristics (continued)

At $V_{DD1} = V_{DD2} = 5\text{ V}$, $V_{INP} = -250\text{ mV}$ to $+250\text{ mV}$, and $V_{INN} = 0\text{ V}$, unless otherwise noted.

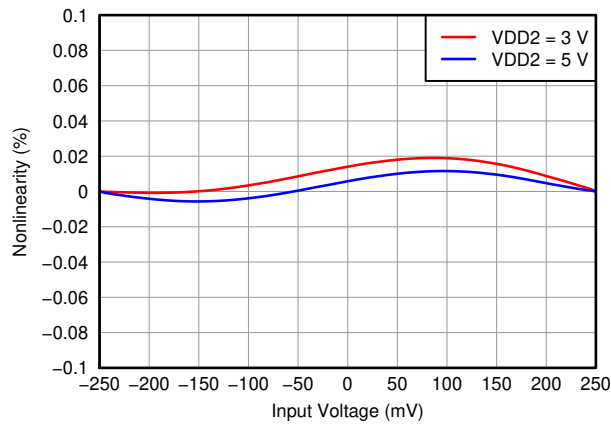


Figure 21. Nonlinearity vs Input Voltage

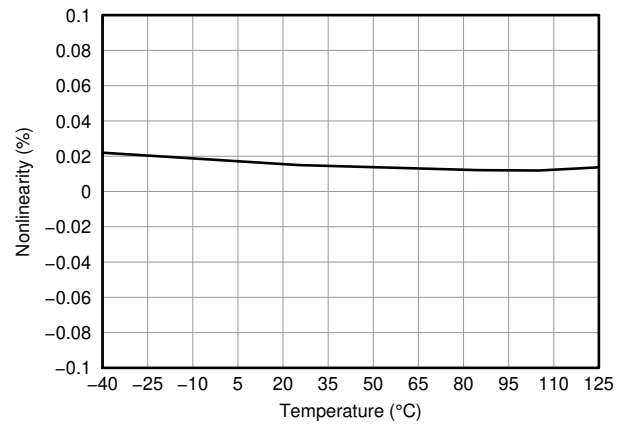


Figure 22. Nonlinearity vs Temperature

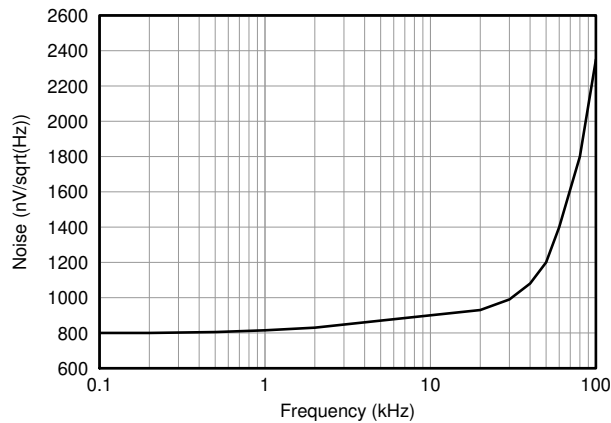


Figure 23. Output Noise Density vs Frequency

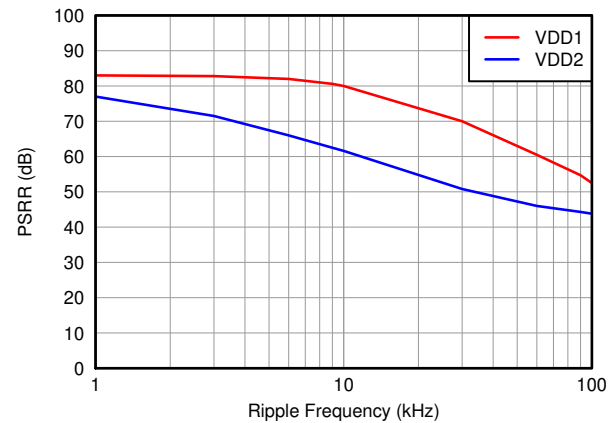


Figure 24. Power-Supply Rejection Ratio vs Ripple Frequency

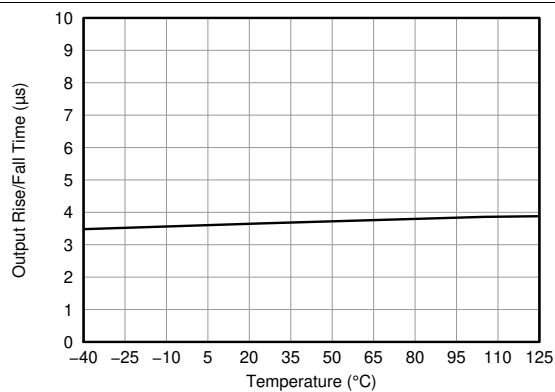


Figure 25. Output Rise and Fall Time vs Temperature

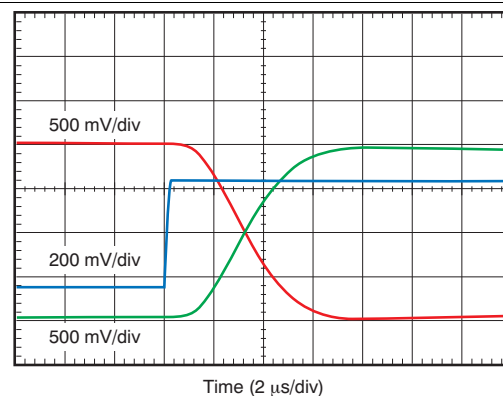


Figure 26. Full-Scale Step Response

Typical Characteristics (continued)

At VDD1 = VDD2 = 5 V, VINP = –250 mV to +250 mV, and VINN = 0 V, unless otherwise noted.

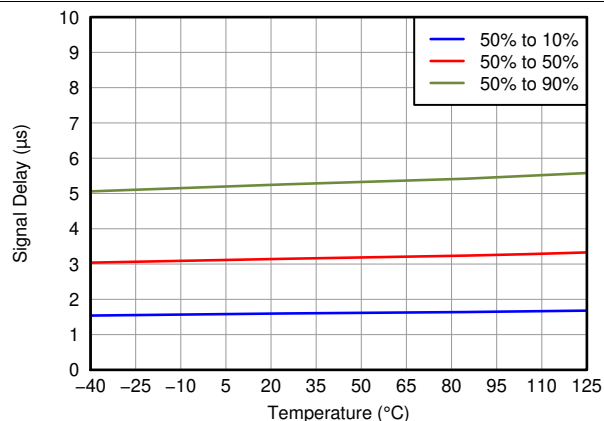


Figure 27. Output Signal Delay Time vs Temperature

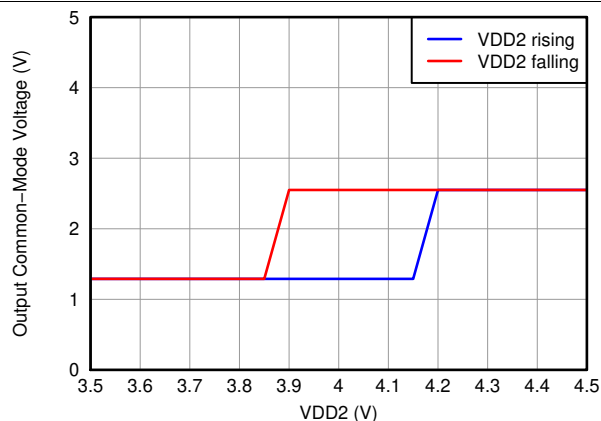


Figure 28. Output Common-Mode Voltage vs Low-Side Supply Voltage

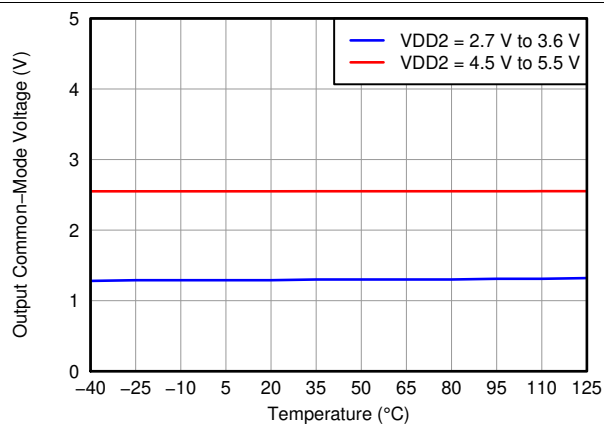


Figure 29. Output Common-Mode Voltage vs Temperature

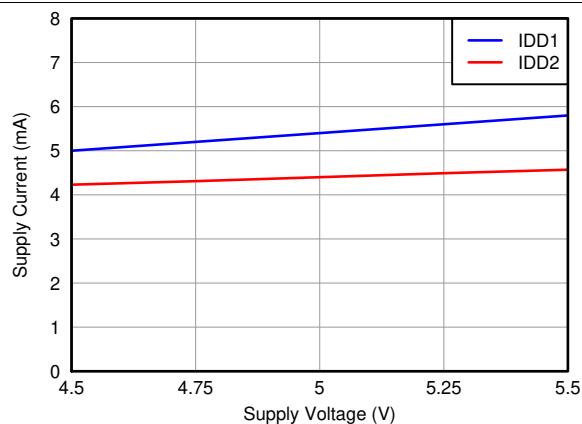


Figure 30. Supply Current vs Supply Voltage

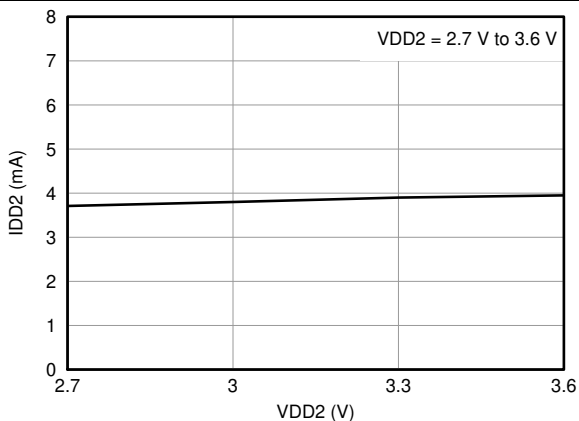


Figure 31. Low-Side Supply Current vs Low-Side Supply Voltage

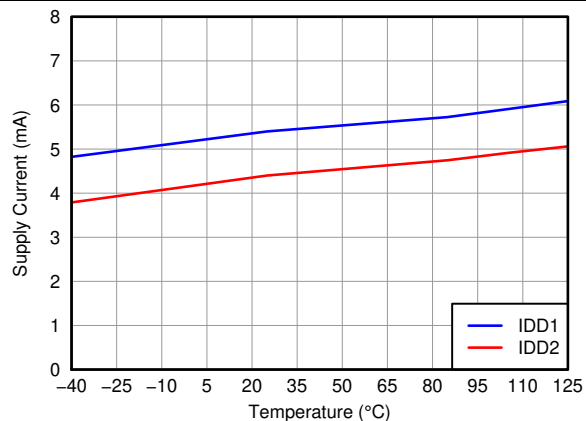


Figure 32. Supply Current vs Temperature

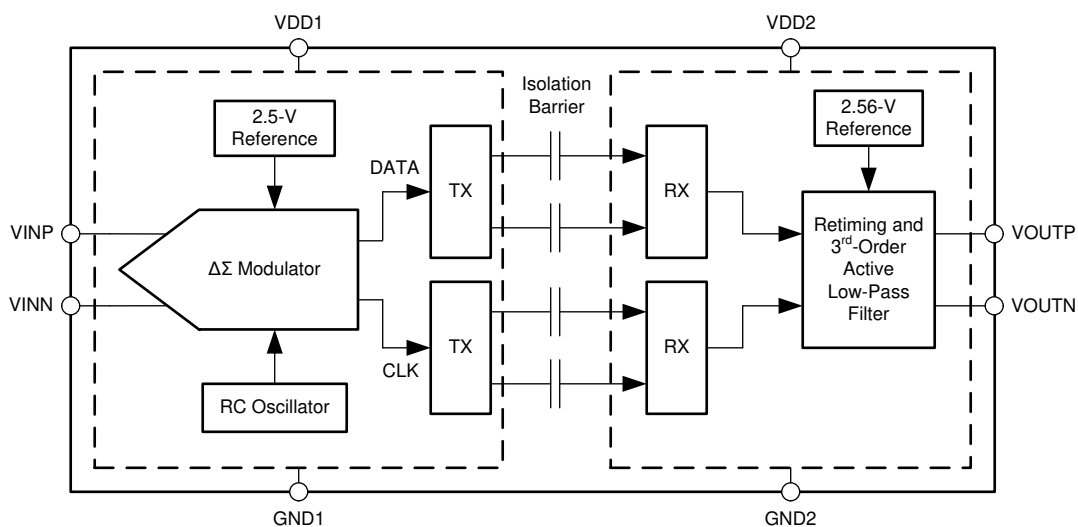
7 Detailed Description

7.1 Overview

The AMC1100 consists of a delta-sigma modulator input stage including an internal reference and clock generator. The output of the modulator and clock signal are differentially transmitted over the integrated capacitive isolation barrier that separates the high- and low-voltage domains. The received bitstream and clock signals are synchronized and processed by a third-order analog filter with a nominal gain of 8 on the low-side and presented as a differential output of the device, as shown in the [Functional Block Diagram](#) section.

The SiO₂-based capacitive isolation barrier supports a high level of magnetic field immunity, as described in application report [SLLA181](#), *ISO72x Digital Isolator Magnetic-Field Immunity* (available for download at www.ti.com).

7.2 Functional Block Diagram



7.3 Feature Description

The differential analog input of the AMC1100 is a switched-capacitor circuit based on a second-order modulator stage that digitizes the input signal into a 1-bit output stream. The device compares the differential input signal ($V_{IN} = V_{INP} - V_{INN}$) against the internal reference of 2.5 V using internal capacitors that are continuously charged and discharged with a typical frequency of 10 MHz. With the S1 switches closed, C_{IND} charges to the voltage difference across V_{INP} and V_{INN} . For the discharge phase, both S1 switches open first and then both S2 switches close. C_{IND} discharges to approximately $GND1 + 0.8$ V during this phase. Figure 33 shows the simplified equivalent input circuitry.

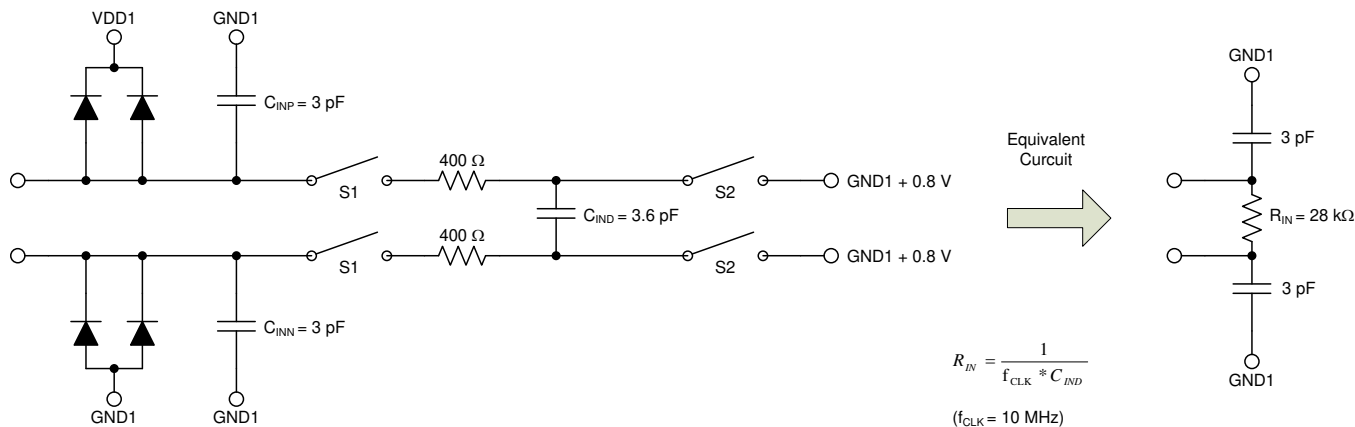


Figure 33. Equivalent Input Circuit

The analog input range is tailored to directly accommodate a voltage drop across a shunt resistor used for current sensing. However, there are two restrictions on the analog input signals, V_{INP} and V_{INN} . If the input voltage exceeds the range $GND1 - 0.5$ V to $VDD1 + 0.5$ V, the input current must be limited to 10 mA to protect the implemented input protection diodes from damage. In addition, the device linearity and noise performance are ensured only when the differential analog input voltage remains within ± 250 mV.

7.4 Device Functional Modes

The AMC1100 is powered on when the supplies are connected. The device is operated off a 5-V nominal supply on the high-side. The potential of the ground reference GND1 can be floating, which is usually the case in shunt-based current-measurement applications. TI recommends tying one side of the shunt to the GND1 pin of the AMC1100 to maintain the operating common-mode range requirements of the device.

The low-side of the AMC1100 can be powered from a supply source with a nominal voltage of 3.0 V, 3.3 V, or 5.0 V. When operated at 5 V, the common-mode voltage of the output stage is set to 2.55 V nominal; in both other cases, the common-mode voltage is automatically set to 1.29 V.

Although usually applied in shunt-based current-sensing circuits, the AMC1100 can also be used for isolated voltage measurement applications, as shown in a simplified way in [Figure 34](#). In such applications, usually a resistor divider (R_1 and R_2 in [Figure 34](#)) is used to match the relatively small input voltage range of the AMC1100. R_2 and the AMC1100 input resistance (R_{IN}) also create a resistance divider that results in additional gain error. With the assumption that R_1 and R_{IN} have a considerably higher value than R_2 , the resulting total gain error can be estimated using [Equation 1](#):

$$G_{ERRTOT} = G_{ERR} + \frac{R_2}{R_{IN}}$$

where:

- G_{ERR} = device gain error.

(1)

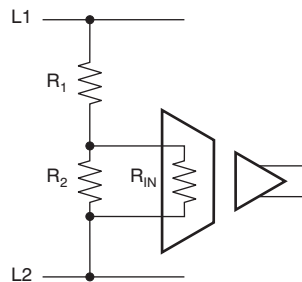


Figure 34. Voltage Measurement Application

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The AMC1100 offers unique linearity, high input common-mode rejection, and low dc errors and drift. These features make the AMC1100 a robust, high-performance isolation amplifier for industrial applications where users and subsystems must be protected from high voltage potentials.

8.2 Typical Applications

8.2.1 The AMC1100 in Frequency Inverters

A typical operation for the AMC1100 is isolated current and voltage measurement in frequency inverter applications (such as industrial motor drives, photovoltaic inverters, or uninterruptible power supplies), as conceptually shown in Figure 35. Depending on the end application, only two or three phase currents are being sensed.

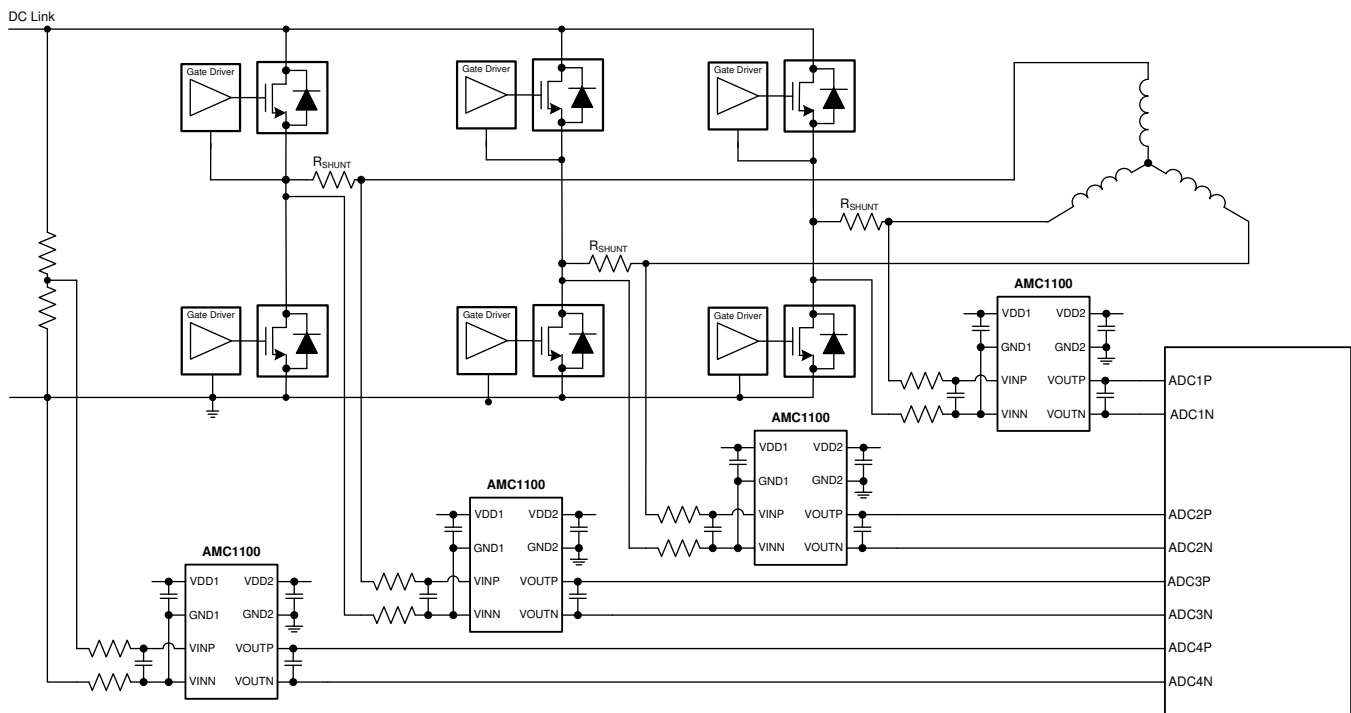


Figure 35. Isolated Current and Voltage Sensing in Frequency Inverters

8.2.1.1 Design Requirements

Current measurement through the phase of a motor power line is done via the shunt resistor R_{SHUNT} (in a two-terminal shunt); see Figure 36. For better performance, the differential signal is filtered using RC filters (components R_2 , R_3 , and C_2). Optionally, C_3 and C_4 can be used to reduce charge dumping from the inputs. In this case, care must be taken when choosing the quality of these capacitors; mismatch in values of these capacitors leads to a common-mode error at the modulator input. Using NP0 capacitors is recommended, if necessary.

Typical Applications (continued)

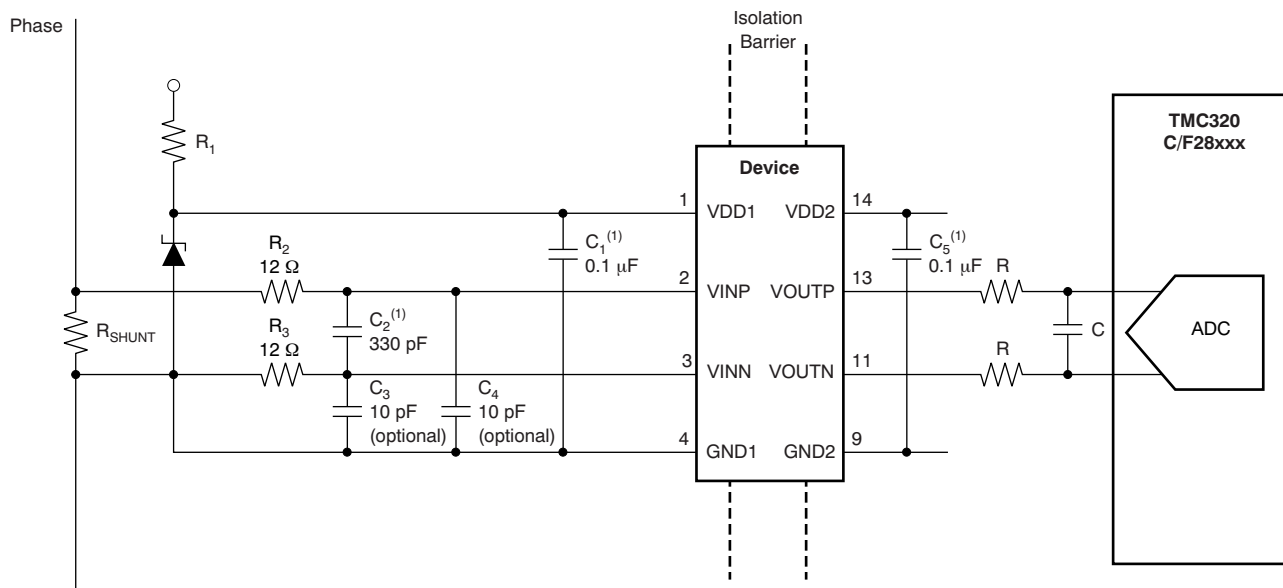


Figure 36. Shunt-Based Current Sensing with the AMC1100

The isolated voltage measurement can be performed as described in the [Device Functional Modes](#) section.

8.2.1.2 Detailed Design Procedure

The floating ground reference (GND1) is derived from the end of the shunt resistor, which is connected to the negative input of the AMC1100 (VINN). If a four-terminal shunt is used, the inputs of the AMC1100 are connected to the inner leads and GND1 is connected to one of the outer shunt leads. The differential input of the AMC1100 ensures accurate operation even in noisy environments.

The differential output of the AMC1100 can either directly drive an analog-to-digital converter (ADC) input or can be further filtered before being processed by the ADC.

8.2.1.3 Application Curve

In frequency inverter applications the power switches must be protected in case of an overcurrent condition. To allow fast powering off of the system, low delay caused by the isolation amplifier is required. [Figure 37](#) shows the typical full-scale step response of the AMC1100.

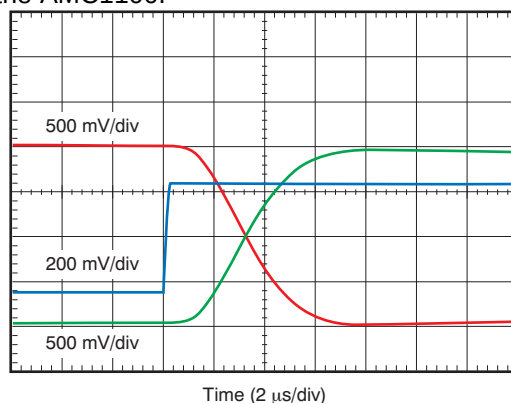


Figure 37. Typical Step Response of the AMC1100

Typical Applications (continued)

8.2.2 The AMC1100 in Energy Metering

Resulting from its immunity to magnetic fields, the AMC1100 can be used for shunt-based current sensing in smart electricity meter (e-meter) designs, as shown in Figure 38. Three AMC1100 devices are used for isolated current sensing. For voltage sensing, resistive dividers are usually used to reduce the common-mode voltage to levels that allow non-isolated measurement.

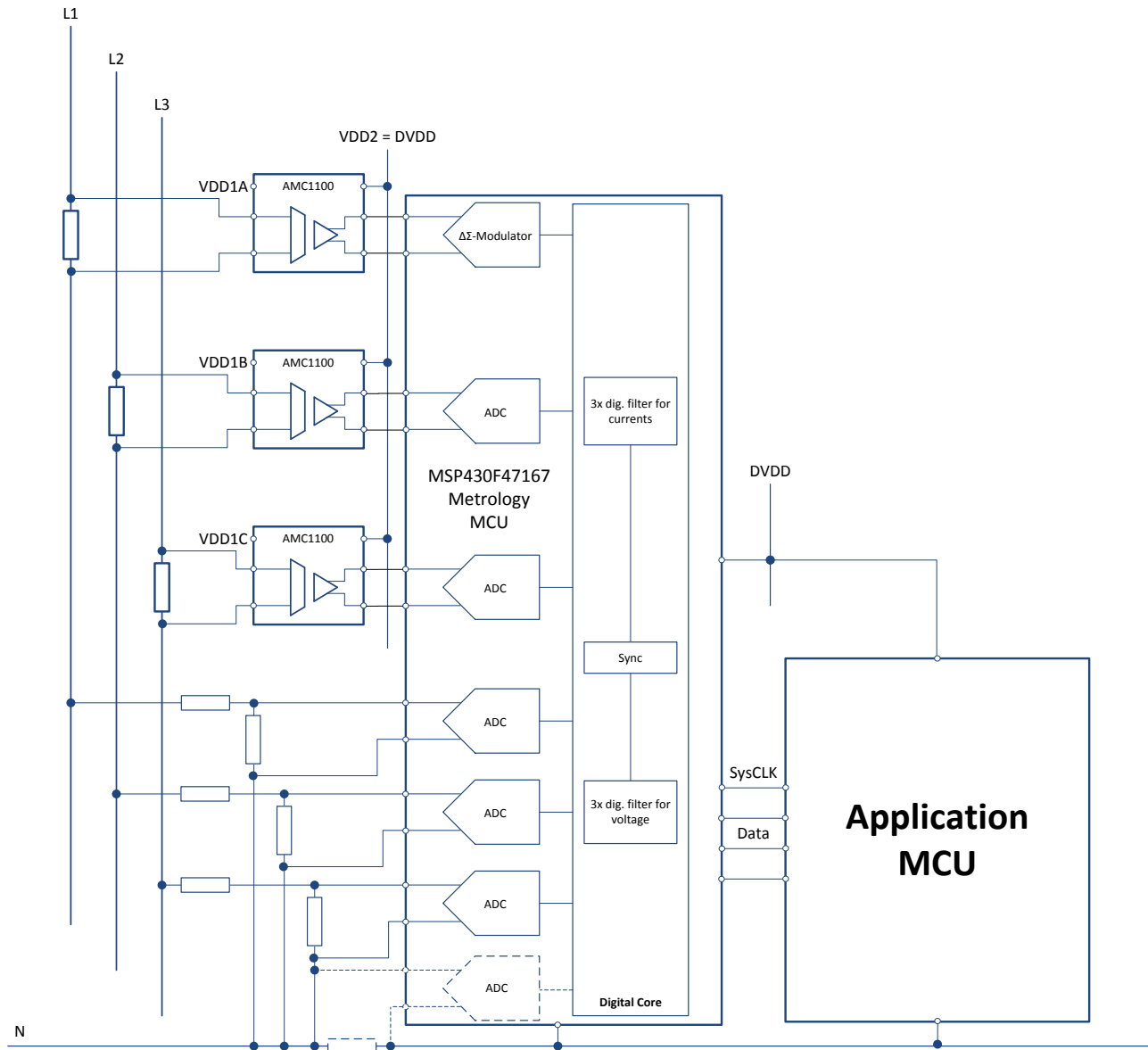


Figure 38. The AMC1100 in an E-Meter Application

8.2.2.1 Design Requirements

For best performance, an RC low-pass filter can be used in front of the AMC1100. Further improvement can be achieved by filtering the output signal of the device. In both cases, the values of the resistors and the capacitors must be tailored to the bandwidth requirements of the system.

Typical Applications (continued)

The analog output of the device is converted to the digital domain using the on-chip analog-to-digital converters (ADCs) of a suitable metrology microcontroller. The architecture of the [MSP430F471x7](#) family of ultra-low power microcontrollers is tailored for this kind of applications. The MSP430F471x7 offers up to seven ADCs for simultaneous sampling: six of which are used for the three phase currents and voltages whereas the seventh channel can be used for additional voltage sensing of the neutral line for applications that require anti-tampering measures.

8.2.2.2 Detailed Design Procedure

The high-side supply for the AMC1100 can be derived from the phase voltage using a capacitive-drop power supply (cap-drop), as shown in [Figure 39](#) and described in the application report [SLAA552](#), *AMC1100: Replacement of Input Main Sensing Transformer in Inverters with Isolate Amplifier*.

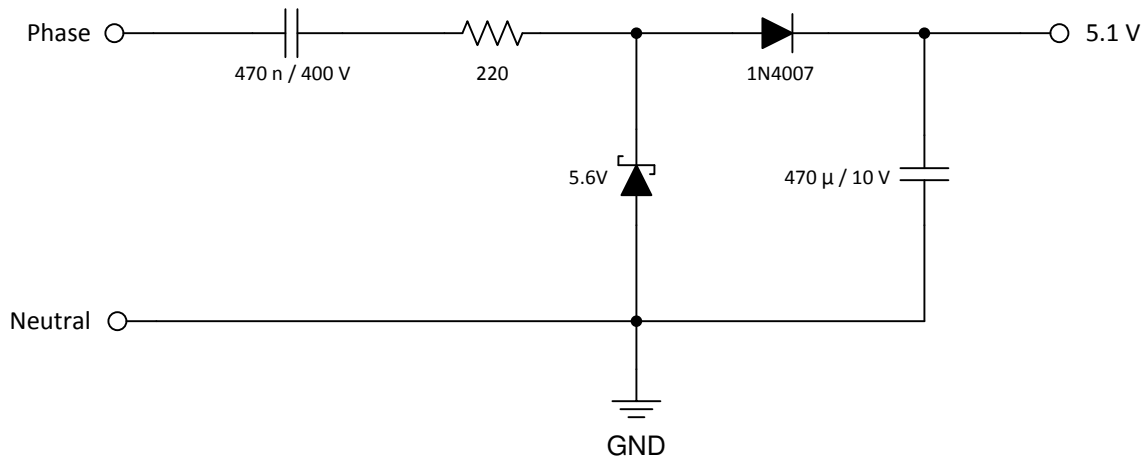


Figure 39. Cap-Drop High-Side Power Supply for the AMC1100

Alternatively, the high-side power supply for each AMC1100 can also be derived from the low-side supply using the [SN6501](#) to drive a transformer, as proven by the TI reference design [TIPD121](#), *Isolated Current Sensing Reference Design Solution*, 5A, 2kV.

8.2.2.3 Application Curve

One of the key parameters of an e-meter is its noise performance, which is mainly influenced by the performance of the ADC and the current sensor. When using a shunt-based approach, the sensor front-end consists of the actual shunt resistor and the isolated amplifier. [Figure 40](#) shows the typical output noise density of the AMC1100 as a basis for overall performance estimations.

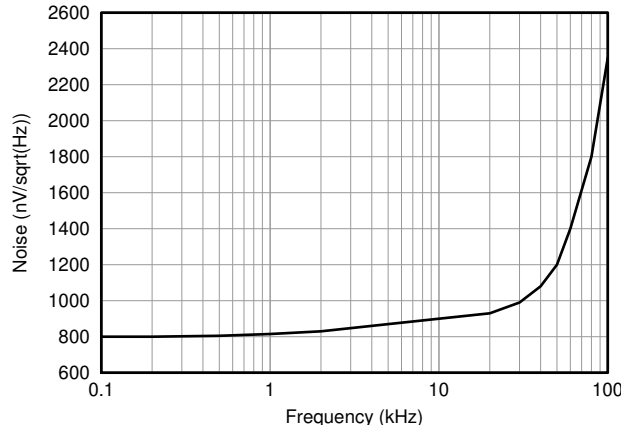


Figure 40. Output Noise Density of the AMC1100

9 Power Supply Recommendations

In a typical frequency inverter application, the high-side power supply for the AMC1100 (VDD1) is derived from the system supply, as shown in Figure 41. For lowest cost, a Zener diode can be used to limit the voltage to 5 V $\pm$ 10%. A 0.1- μ F decoupling capacitor is recommended for filtering this power-supply path. Place this capacitor (C₁) as close as possible to the VDD1 pin for best performance. If better filtering is required, an additional 1- μ F to 10- μ F capacitor can be used.

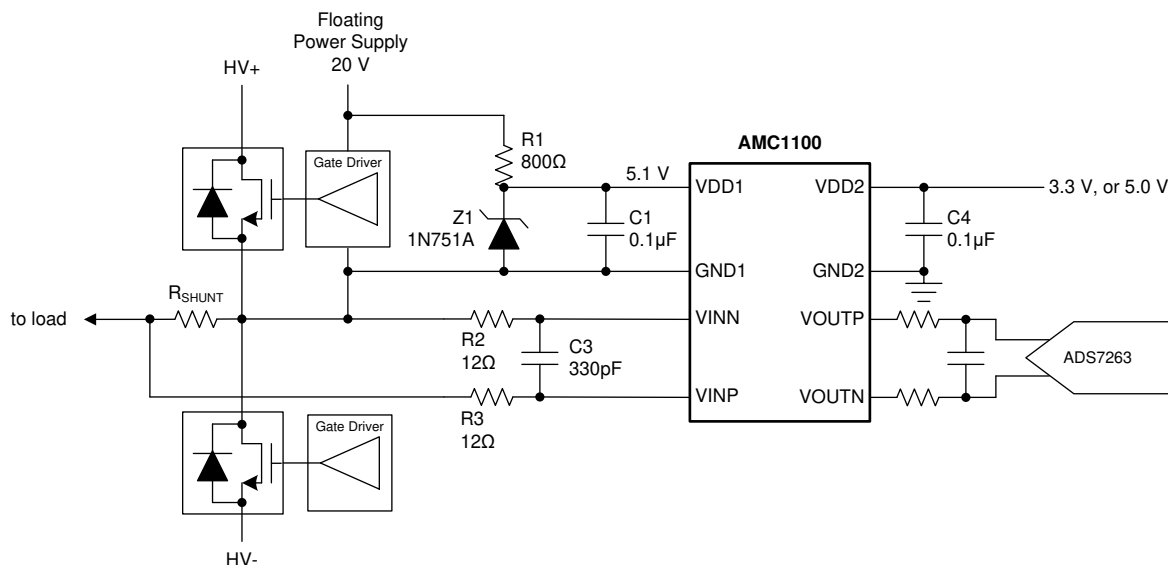


Figure 41. Zener Diode Based High-Side Supply

For higher power efficiency and better performance, a buck converter can be used; an example of such an approach is based on the LM5017. A reference design including performance test results and layout documentation can be downloaded at [PMP9480](#), *Isolated Bias Supplies + Isolated Amplifier Combo for Line Voltage or Current Measurement*.

10 Layout

10.1 Layout Guidelines

A layout recommendation showing the critical placement of the decoupling capacitors that be placed as close as possible to the AMC1100 while maintaining a differential routing of the input signals is shown in [Figure 42](#).

To maintain the isolation barrier and the common-mode transient immunity (CMTI) of the device, keep the distance between the high-side ground (GND1) and the low-side ground (GND2) at a maximum; that is, the entire area underneath the device must be kept free of any conducting materials.

10.2 Layout Example

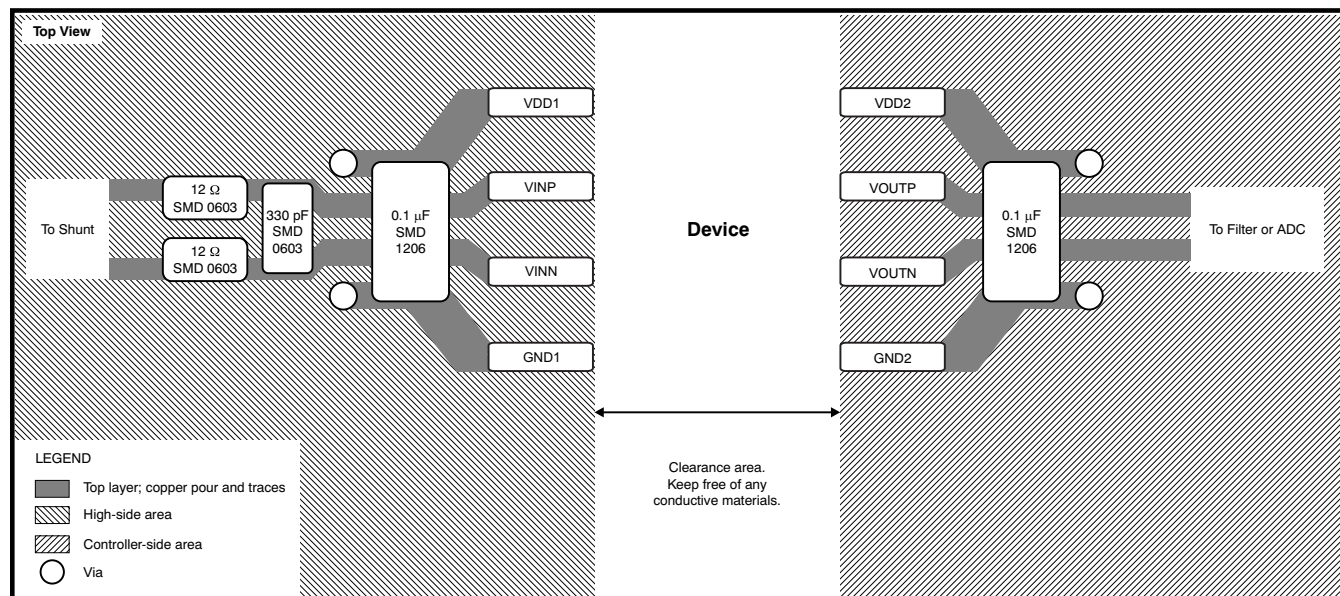


Figure 42. Example Layout

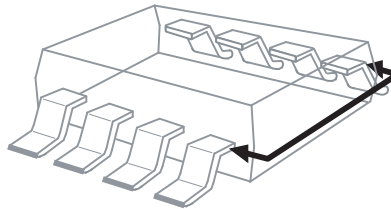
11 デバイスおよびドキュメントのサポート

11.1 デバイス・サポート

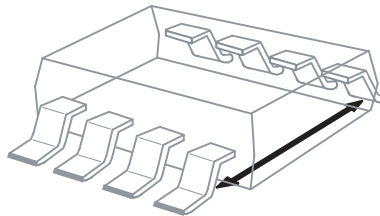
11.1.1 デバイスの項目表記

11.1.1.1 絶縁の用語集

沿面距離: 絶縁体の表面に沿って測定された、入力と出力の 2 本の導電性リード間の最短経路。この最短距離の経路は、パッケージ本体の端部を回り込む形になります。



空間距離: 空気を挟んで (見通しで) 測定された、入力と出力の 2 本の導電性リード間の最短距離。



入出力間バリア容量: 互いに接続されたすべての入力端子と互いに接続されたすべての出力端子の間の総容量。

入出力間バリア抵抗: 互いに接続されたすべての入力端子と互いに接続されたすべての出力端子の間の総抵抗。

1次回路: 外部の商用電源または1次回路の電力を供給するその他の等価な電源に直接接続した内部回路。

2次回路: 別の絶縁された電源から電力を得る、1次電源に直接接続されていない回路。

比較トラッキング指数 (CTI): CTI は、電氣的絶縁材料に使用される指標です。規格試験中にトラッキングによる障害を引き起こす電圧値として定義されます。トラッキングとは、絶縁体の表面上または表面付近で発生した放電現象の結果、絶縁材料の表面上または表面を貫通する局所的な劣化によって、部分的な導電路が発生するプロセスです。絶縁材料の CTI 値が大きいほど、最小沿面距離は小さくできます。

一般に、絶縁破壊は材料を貫通して、材料の表面に沿って、またはその両方で発生します。表面の障害は、フラッシュオーバーの結果、または小さな局所的なスパークによる絶縁体表面の進行性の劣化により発生することがあります。このようなスパークは、導電性汚染物質の表面薄膜が絶縁体上で破壊することで発生します。この薄膜の破壊により漏れ電流が断絶し、その不連続の部分で過電圧が生じ、その結果電氣的スパークが発生します。これらのスパークは多くの場合、絶縁材料の炭化を引き起こし、異なる電位の地点間に炭素経路を形成します。このプロセスをトラッキングと呼びます。

11.1.1.1.1 絶縁

機能絶縁 - 機器の正常な動作に必要な絶縁。

基礎絶縁 - 電氣的ショックに対する基本的な保護を行う絶縁。

付加絶縁 - 基礎絶縁が破れた際に電氣的衝撃に対する保護を確保するため、基礎絶縁に加えて適用される独立した絶縁。

二重絶縁 - 基礎絶縁と付加絶縁の両方で構成される絶縁。

強化絶縁 - 電氣的衝撃に対して二重絶縁と同等の保護を行う単一絶縁システム。

11.1.1.1.2 汚染度

汚染度 1 - 汚染なし、または乾燥した非導電性の汚染のみが発生している。この汚染はデバイス性能に影響を及ぼさない。

デバイス・サポート (continued)

汚染度 2 - 通常、非導電性の汚染のみが発生している。ただし、結露による一時的な導電を見込まなければならない。

汚染度 3 - 導電性の汚染、または結露により導電性になる乾燥した非導電性の汚染が発生している。結露を見込まなければならない。

汚染度 4 - 導電性の塵、雨、その他の湿潤な条件の結果として連続的な導電が発生している。

11.1.1.1.3 設置カテゴリ

過電圧カテゴリ - このセクションは絶縁協調のためのものであり、発生し得る過渡過電圧を識別し、IEC 60664 に示されている下記の異なる 4 レベルを割り当てます。

- I. 信号レベル: 特殊機器、または機器の部品。
- II. 局所レベル: 携帯機器など。
- III. 配電レベル: 固定設備。
- IV. 1 次給電レベル: 架空送電線、ケーブル・システム。

各カテゴリは、その上のカテゴリよりも低い過渡電圧にさらされます。

11.2 ドキュメントのサポート

11.2.1 関連資料

テキサス・インスツルメンツ、『[High-Voltage Lifetime of the ISO72x Family of Digital Isolators](#)』アプリケーション・レポート (英語)

テキサス・インスツルメンツ、『[ISO72x Digital Isolator Magnetic-Field Immunity](#)』アプリケーション・レポート

テキサス・インスツルメンツ、『[AMC1100: Replacement of Input Main Sensing Transformer in Inverters with Isolate Amplifier](#)』アプリケーション・レポート (英語)

テキサス・インスツルメンツ、[活性電源側の絶縁型、電流シャント・モニタのリファレンス・デザイン](#)

テキサス・インスツルメンツ、[PMP9480 絶縁バイアス電源 + 絶縁アンプのコンボ、ライン電圧または電流測定用のリファレンス・デザイン](#)

テキサス・インスツルメンツ、『[TPS6212x 15-V, 75-mA Highly Efficient Buck Converter](#)』データシート (英語)

テキサス・インスツルメンツ、『[MSP430F471x3, MSP430F471x6, MSP430F471x7 MIXED SIGNAL MICROCONTROLLER](#)』データシート (英語)

テキサス・インスツルメンツ、『[SN6501 絶縁電源用の変圧器ドライバ](#)』データシート

テキサス・インスツルメンツ、『[LM5017 100-V, 600-mA Constant On-Time Synchronous Buck Regulator](#)』データシート (英語)

11.3 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

11.4 サポート・リソース

[TI E2E™ support forums](#) are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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11.5 商標

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11.6 静電気放電に関する注意事項



すべての集積回路は、適切なESD保護方法を用いて、取扱いと保存を行うようにして下さい。

静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

11.7 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
AMC1100DUB	ACTIVE	SOP	DUB	8	50	RoHS & Green	NIPDAU	Level-4-260C-72 HR	-40 to 105	AMC1100	Samples
AMC1100DUBR	ACTIVE	SOP	DUB	8	350	RoHS & Green	NIPDAU	Level-3-260C-168 HR	-40 to 105	AMC1100	Samples
AMC1100DWV	ACTIVE	SOIC	DWV	8	64	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	AMC1100	Samples
AMC1100DWVR	ACTIVE	SOIC	DWV	8	1000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 105	AMC1100	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

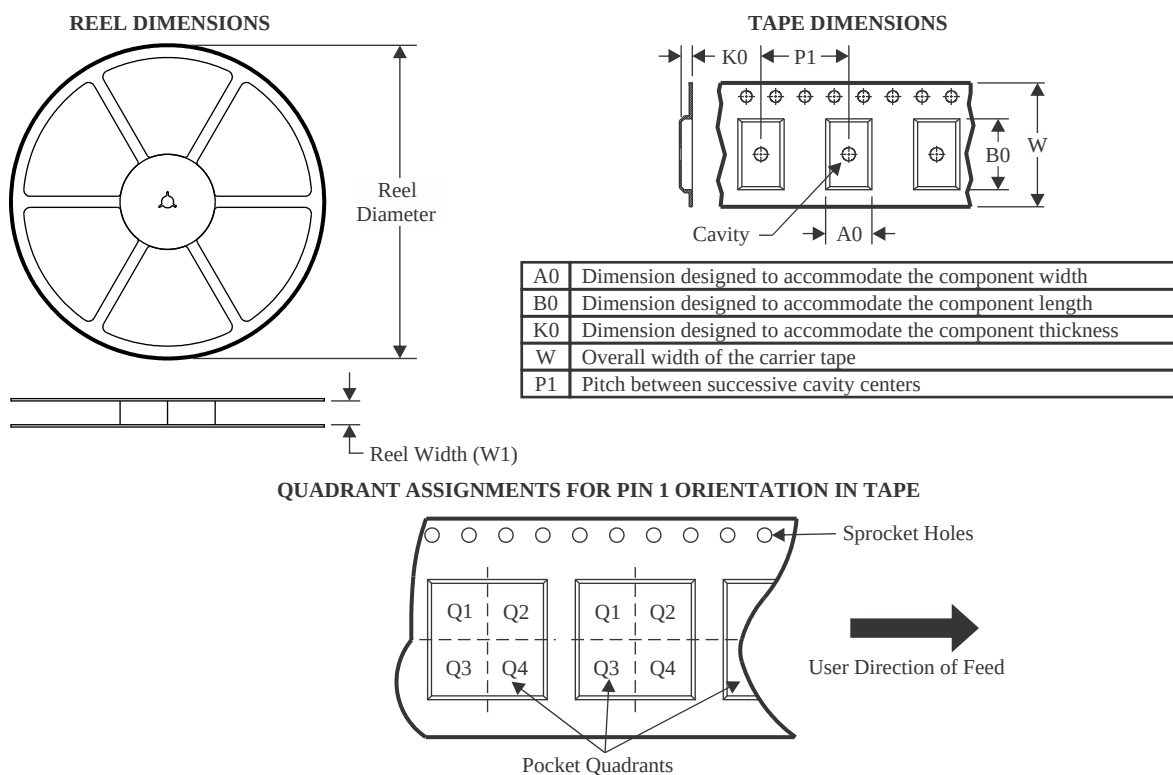
⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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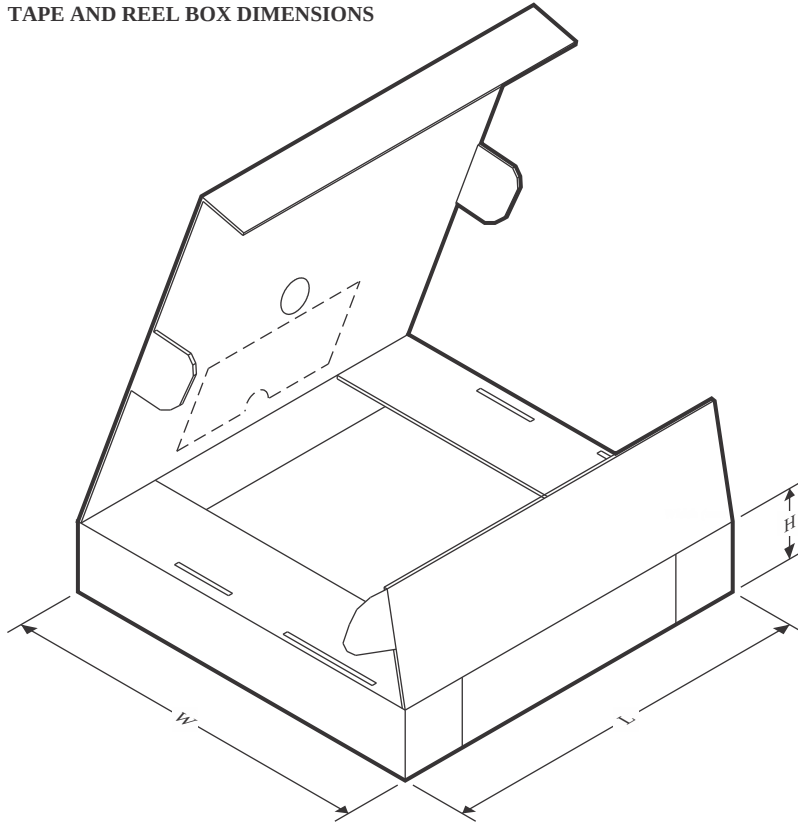
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
AMC1100DUBR	SOP	DUB	8	350	330.0	24.4	13.1	9.75	6.0	16.0	24.0	Q1
AMC1100DWVR	SOIC	DWV	8	1000	330.0	16.4	12.15	6.2	3.05	16.0	16.0	Q1

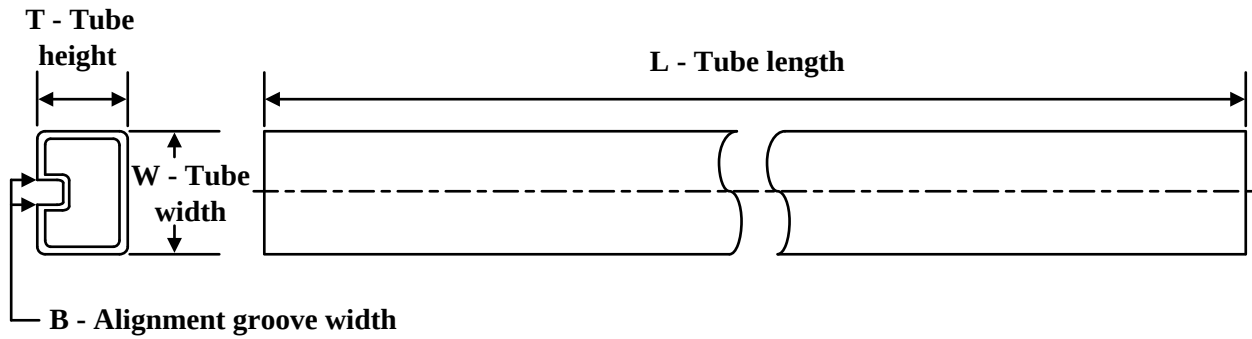
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
AMC1100DUBR	SOP	DUB	8	350	367.0	367.0	45.0
AMC1100DWVR	SOIC	DWV	8	1000	356.0	356.0	35.0

TUBE



*All dimensions are nominal

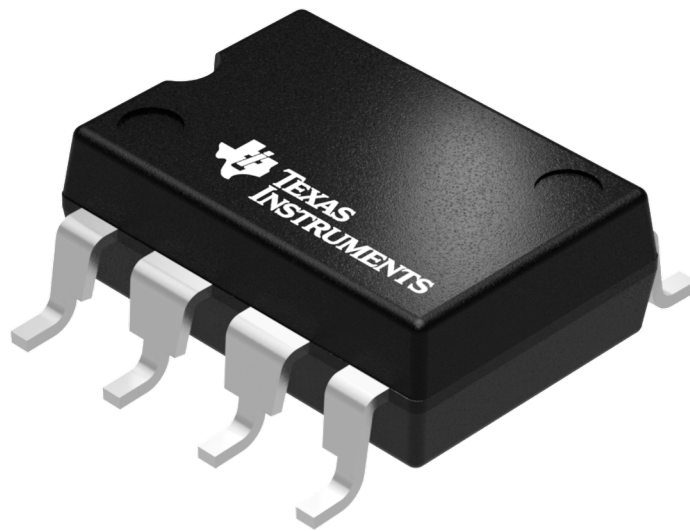
Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
AMC1100DUB	DUB	SOP	8	50	532.13	13.51	7.36	6.91
AMC1100DUB	DUB	SOP	8	50	532.13	13	7300	6.6
AMC1100DWV	DWV	SOIC	8	64	505.46	13.94	4826	6.6

GENERIC PACKAGE VIEW

DUB 8

SOP - 4.85 mm max height

SMALL OUTLINE PACKAGE



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

4207614/E

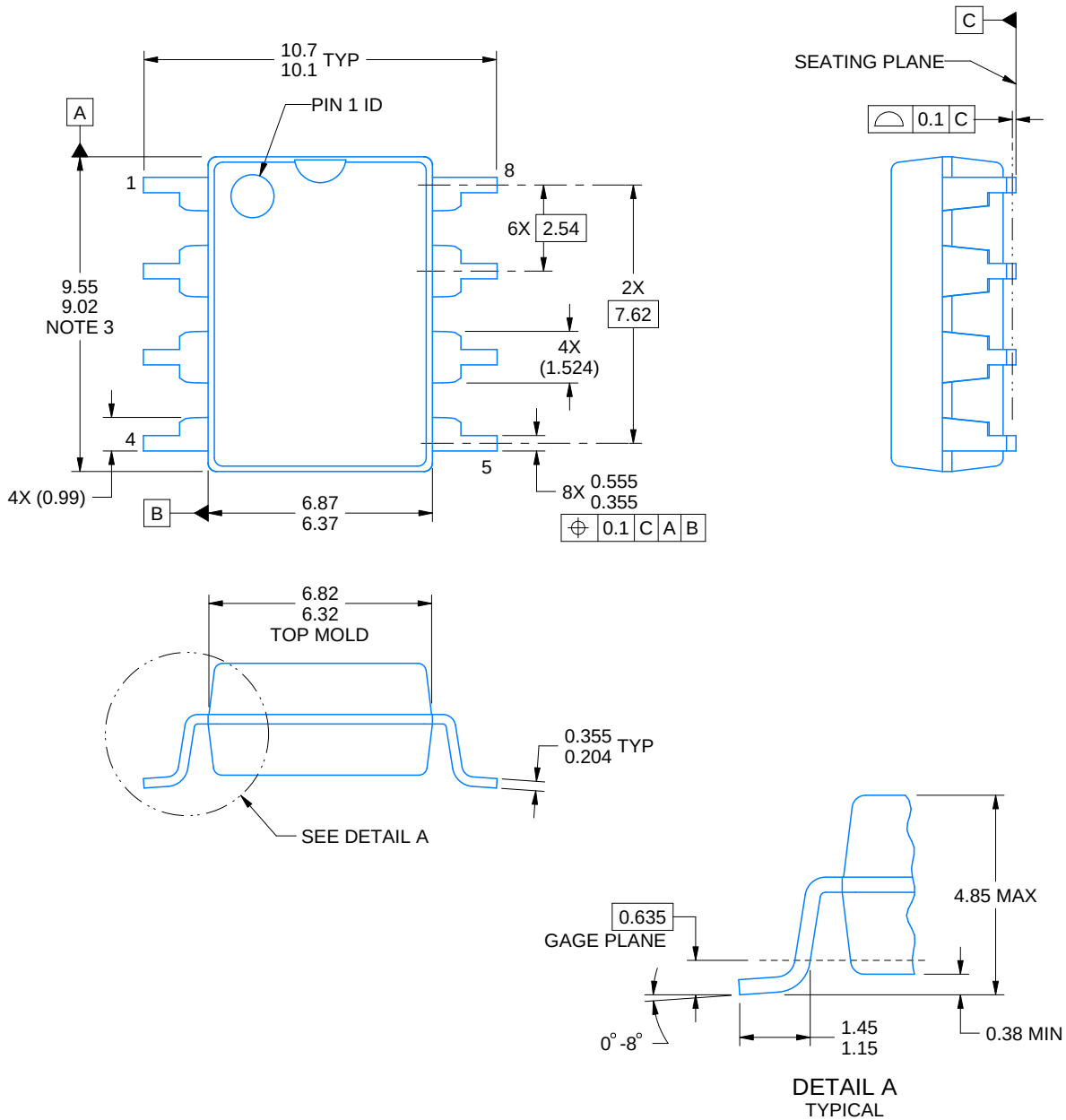
DUB0008A



PACKAGE OUTLINE

SOP - 4.85 mm max height

SMALL OUTLINE PACKAGE



4222355/G 04/2019

NOTES:

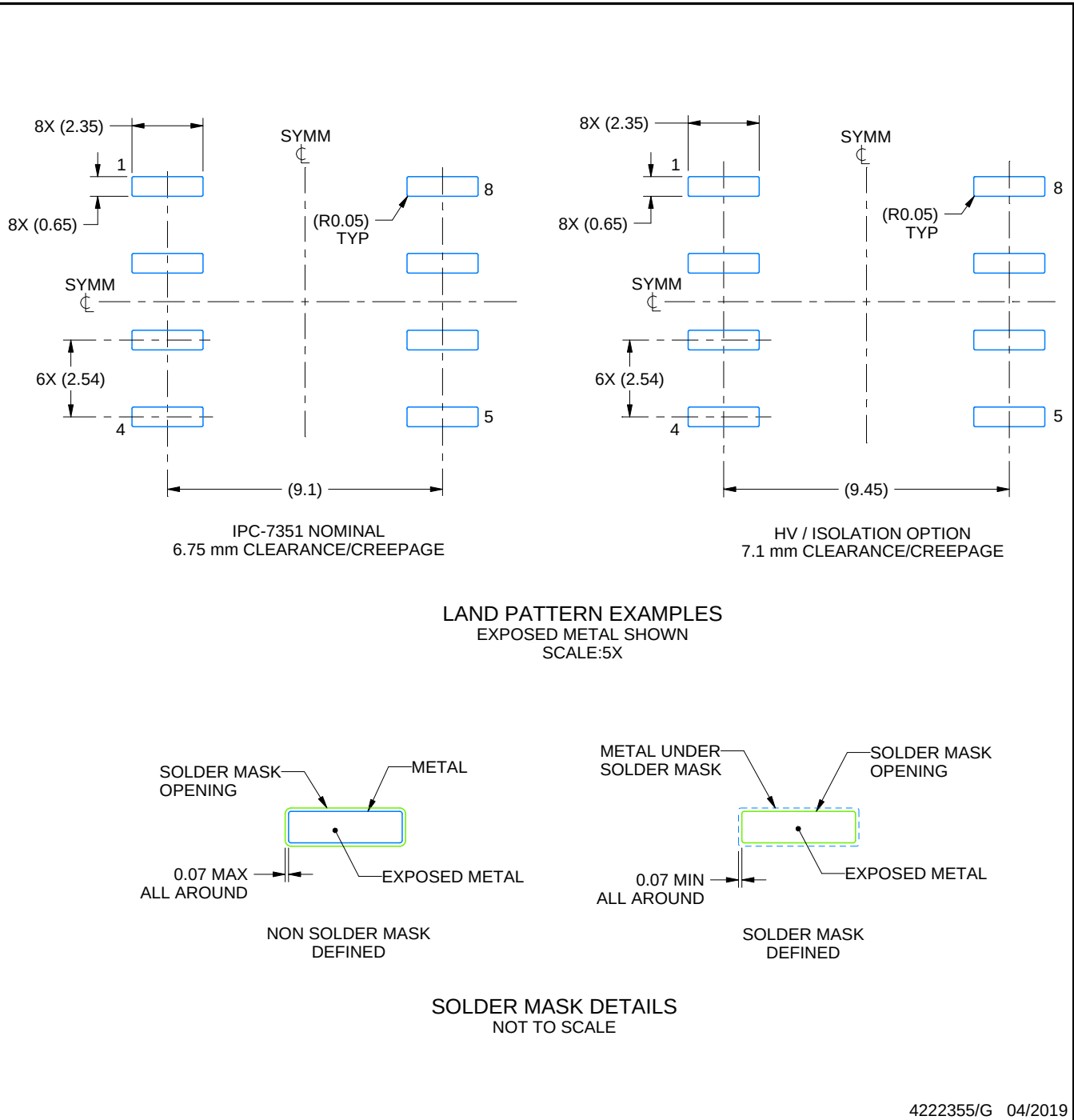
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.254 mm per side.

EXAMPLE BOARD LAYOUT

DUB0008A

SOP - 4.85 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

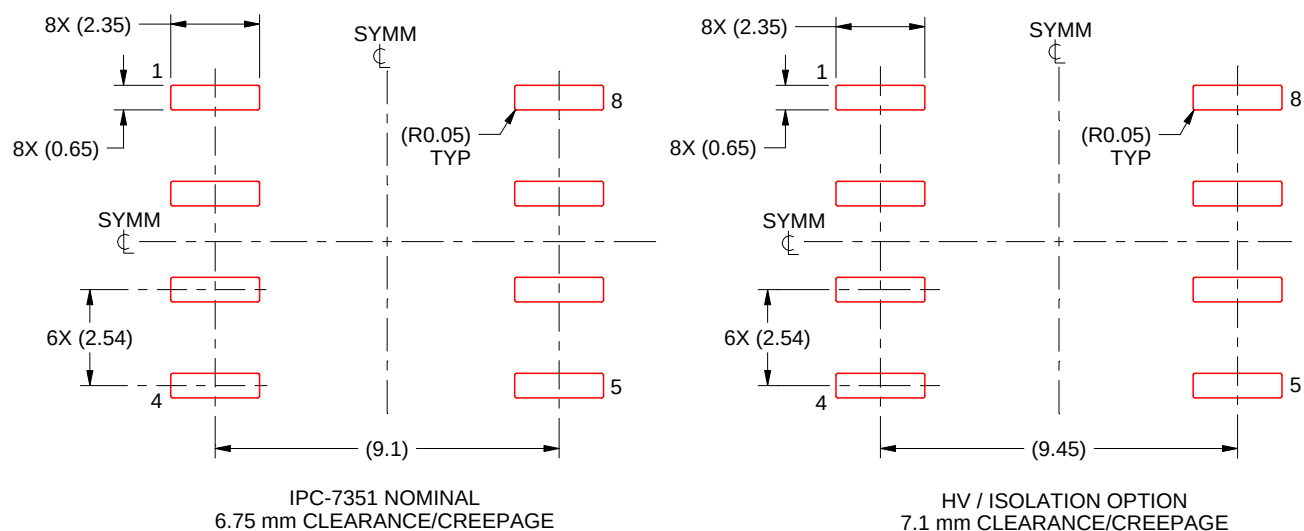
4. Publication IPC-7351 may have alternate designs.
5. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DUB0008A

SOP - 4.85 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:5X

4222355/G 04/2019

NOTES: (continued)

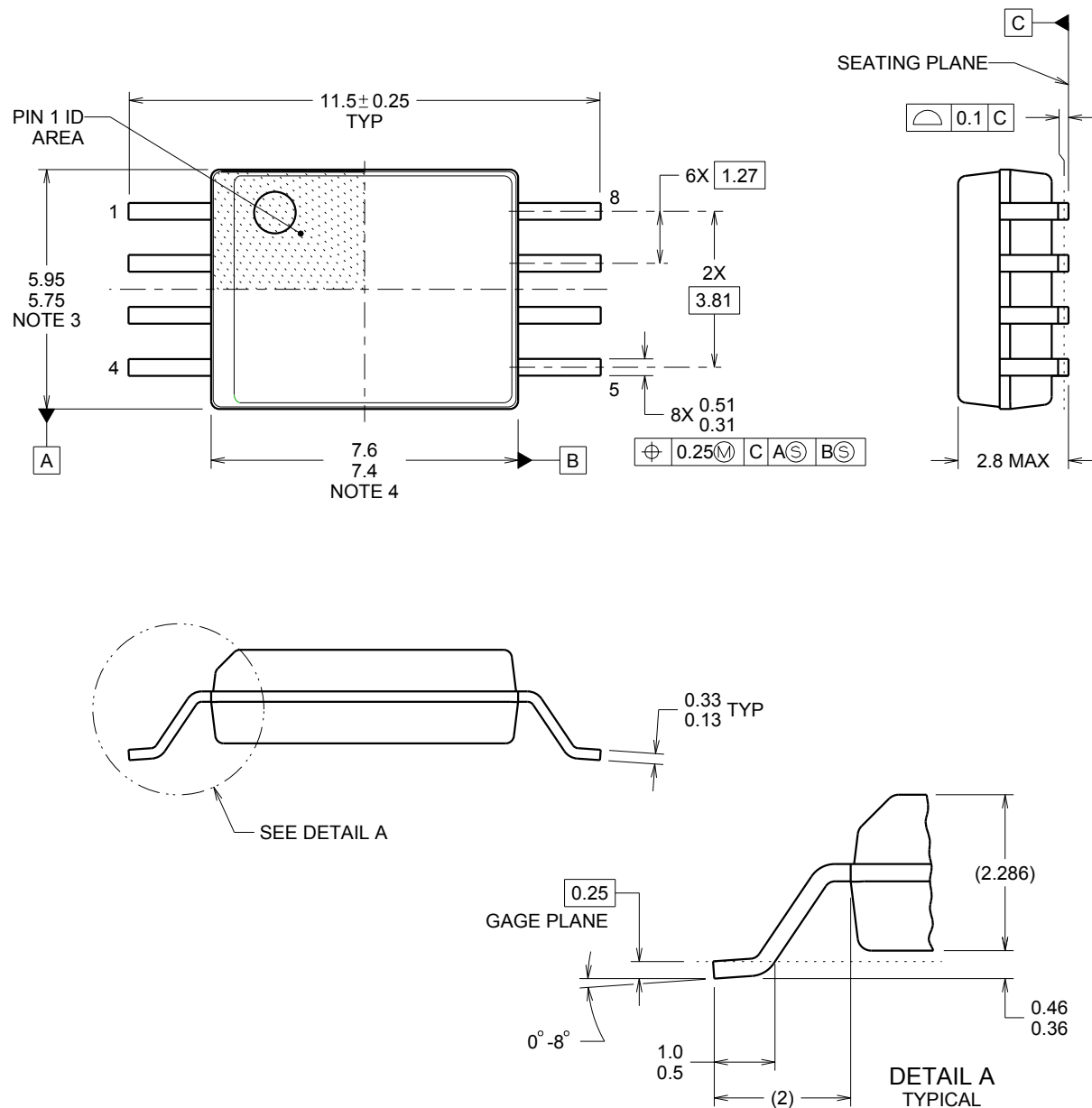
6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
7. Board assembly site may have different recommendations for stencil design.

DWV0008A



SOIC - 2.8 mm max height

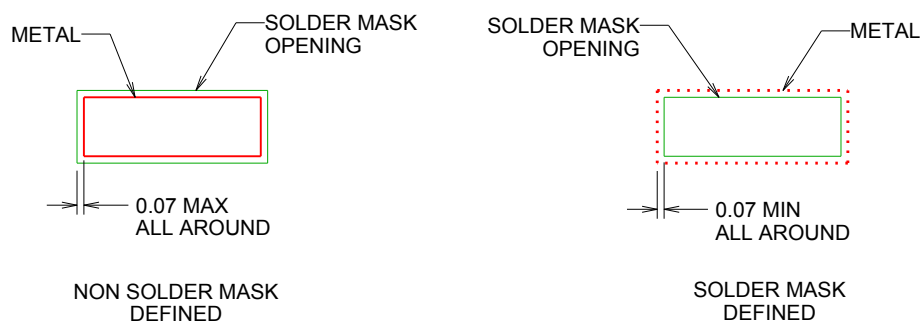
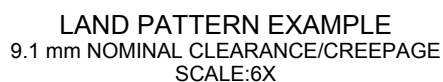
SOIC



4218796/A 09/2013

NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.

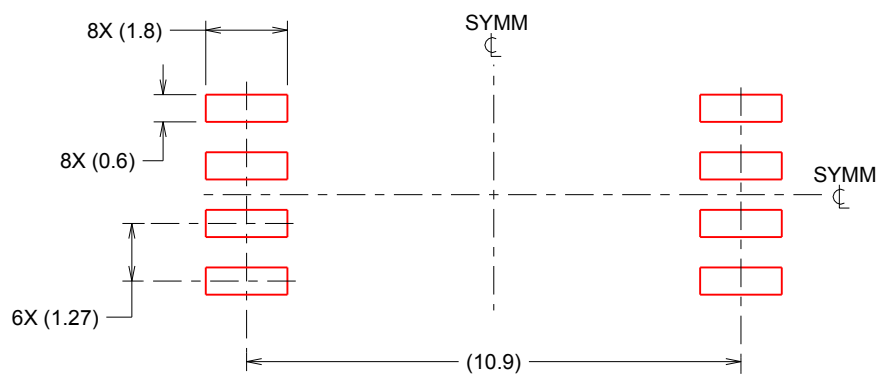


SOLDER MASK DETAILS

4218796/A 09/2013

NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
 BASED ON 0.125 mm THICK STENCIL
 SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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