# AMC1204 電流シャント測定用の 20MHz、2 次、絶縁型デルタ - シグマ変調器

## 1 特長

- シャント抵抗用に最適化された ±250mV の入力電圧範囲
- 安全関連の認定
  - DIN VDE V 0884-11: 2017-01 に準拠した基本絶縁：4250$V_{PK}$ (AMC1204B)
  - UL 1577 に準拠した絶縁耐圧：3005$V_{RMS}$ で 1 分間 (AMC1204B)
  - CAN/CSA No.5A - 部品承認通達および DIN EN 61010-1
  - 動作電圧：1200$V_{PEAK}$
  - 過渡耐性：15kV/µs
- 優れた電磁場耐性 (「SLLA181A アプリケーション・レポート」を参照)
- 優れた AC 特性
  - SNR：84dB 以上
  - THD：–80dB 以下
- 優れた DC 精度
  - INL：±8LSB 以下
  - ゲイン誤差：±2% 以下
- 同期を容易にするための外部クロック入力
- 拡張産業用温度範囲全体にわたって仕様を完全に規定

## 2 アプリケーション

- 次の用途でのシャント抵抗を使用した電流センシング
  - モーター制御
  - 自然エネルギー
  - インバータ・アプリケーション
  - 無停電電源

## 3 概要

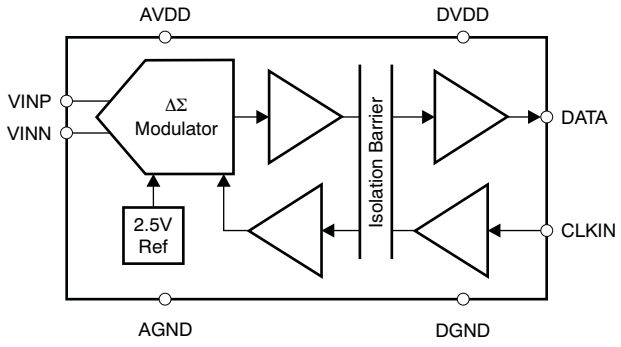
AMC1204 と AMC1204B は、最高 20MHz のクロックで動作できる 1 ビット・デジタル出力の絶縁型デルタ - シグマ (ΔΣ) 変調器です。この変調器の出力は、磁気干渉に対して優れた耐性を持つ二酸化ケイ素 ($SiO_2$) の絶縁障壁によってデジタル絶縁されています。この絶縁障壁は、UL1577、VDE V 0884-11、CSA 規格または仕様に従って最高 4000$V_{PEAK}$ (AMC1204) および 4250$V_{PEAK}$ (AMC1204B) の基本ガルバニック絶縁の要件を満たすことが認定されています。

**製品情報(1)**

| 型番 | パッケージ | 本体サイズ (公称) |
|---|---|---|
| AMC1204 | SOIC (16) | 10.30mm×7.50mm |
| | SOIC (8) | 5.85mm×7.50mm |

(1) 提供されているすべてのパッケージについては、巻末の注文情報を参照してください。

**デバイスのブロック図**




英語版のTI製品についての情報を翻訳したこの資料は、製品の概要を確認する目的で便宜的に提供しているものです。該当する正式な英語版の最新情報は、www.ti.comで閲覧でき、その内容が常に優先されます。TIでは翻訳の正確性および妥当性につきましては一切保証いたしません。実際の設計などの前には、必ず最新版の英語版をご参照くださいますようお願いいたします。

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## 4 改訂履歴

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

**Revision E (September 2015)** から **Revision F** に変更 **Page**

- 「*デジタル絶縁認定済み*」の箇条書き項目を「*安全関連の認定*」に変更、ISO 規格に合わせて詳細を 変更 ... 1
- 「*長い絶縁バリア寿命*」箇条書き項目を「*特長*」セクションから 削除 ... 1
- 「*概要*」セクションの「VDE V 0884-10」を「VDE V 0884-11」に 変更 ... 1
- 「*デバイスのブロック図*」のタイトルを「*概略回路図*」から 変更 ... 1
- Changed *Absolute Maximum Ratings* condition statement ... 6
- Added *Power Ratings* table ... 7
- Changed *Insulation Specifications* table per ISO standard ... 7
- Changed *Safety-Related Certification* table per ISO standard ... 9
- Changed *Safety Limiting Values* table per ISO standard ... 9
- Added *Insulation Characteristics Curves* as per ISO standard ... 12
- 変更 「*関連資料*」セクション ... 31
- 削除 「*関連リンク*」セクション ... 31

**Revision D (December 2013)** から **Revision E** に変更 **Page**

- 「*ESD 定格*」表、「*機能説明*」セクション、「*デバイスの機能モード*」セクション、「*アプリケーションと実装*」セクション、「*電源に関する推奨事項*」セクション、「*レイアウト*」セクション、「*デバイスおよびドキュメントのサポート*」セクション、「*メカニカル、パッケージ、および注文情報*」セクション 追加 ... 1
- 「特長」の「*デジタル絶縁認定済み*」の箇条書きの最初の副項目の「IEC60747-5-5」を「VDE V 0884-10」に 変更 ... 1
- 「*概要*」セクションの最初の段落の「IEC60747-5-5」を「VDE V 0884-10」に 変更 ... 1


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**Revision C (August 2012) から Revision D に変更** **Page**

- 「特長」の「デジタル絶縁認定済み」の箇条書きの最初の副項目の「IEC60747-5-2」を「IEC60747-5-5」に 変更 ..... 1
- チップ写真を 削除 ..... 1
- ドキュメントに DWV (SSO-8) パッケージを 追加 ..... 1
- 「概要」セクションの最初の段落の「IEC60747-5-2」を「IEC60747-5-5」に 変更 ..... 1
- 「概要」セクションの最後の段落を 変更 ..... 1
- Added DWV pin out drawing ..... 5
- Added DWV information to Pin Descriptions table ..... 5
- Added DWV package to Thermal Information table ..... 6
- Changed first paragraph of *Digital Output* section: changed 78.1% to 89.06% and 21.9% to 10.94% ..... 23

**Revision B (August 2011) から Revision C に変更** **Page**

- 「特長」の「デジタル絶縁認定済み」の絶縁電圧の箇条書き項目を 変更 ..... 1
- ドキュメントに AMC1204B を 追加 ..... 1
- 「概要」セクションを AMC1204B を含めるように 変更 ..... 1
- Changed package name from TSSOP to SO ..... 5
- Changed footnote 1 in *Electrical Characteristics* table ..... 10
- Changed Analog Inputs, $V_{CM}$ parameter minimum specification and unit in *Electrical Characteristics* table ..... 10
- Changed Digital Output, $C_{OUT}$ and $C_{LOAD}$ parameters unit specifications in *Electrical Characteristics* table ..... 11
- Updated Figure 53 ..... 28
- Updated Figure 55 ..... 29
- Updated Figure 56 ..... 30

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## 5 概要（続き）

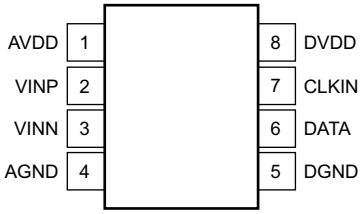
AMC1204 と AMC1204B は、絶縁障壁越しにシャント抵抗の小信号を測定するシングルチップ・ソリューションを提供します。これらのシャント抵抗は、モーター制御インバータ、自然エネルギー発電システム、その他の産業用アプリケーションで電流を検出するためによく使用されます。AMC1204 と AMC1204B の差動入力は、シャント抵抗またはその他の低レベル信号源に簡単に接続できます。内部リファレンスにより、外部部品が不要になります。適切な外部デジタル・フィルタと併用することで、78kSPS のデータ速度で 14ENOB (実効ビット数) を達成できます。

絶縁型デジタル・インターフェイスは 3V、3.3V、5V のいずれかの電源 (DVDD) で動作しますが、この変調器は 5V アナログ電源 (AVDD) を使用します。AMC1204 と AMC1204B は SOIC-16 (DW) および SOIC-8 (DWV) パッケージで供給され、–40℃～105℃ で動作が規定されています。

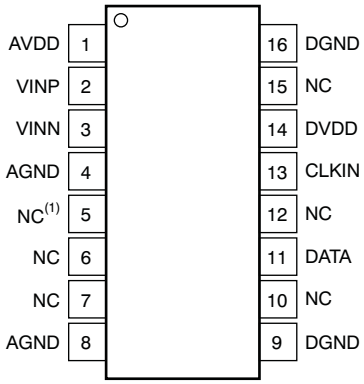

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# 6 Pin Configuration and Functions

**DWV Package**
**8-Pin SOIC**
**Top View**




**DW Package**
**16-Pin SOIC**
**Top View**




NC = no internal connection.

**Pin Functions**

| PIN | | | I/O | DESCRIPTION |
|---|---|---|---|---|
| NAME | NO. | | | |
| | 8 PINS | 16 PINS | | |
| AVDD | 1 | 1 | Power | High-side power supply |
| VINP | 2 | 2 | Analog input | Noninverting analog input |
| VINN | 3 | 3 | Analog input | Inverting analog input |
| AGND | 4 | 4, 8(1) | Power | High-side ground |
| DGND | 5 | 9, 16 | Power | Controller-side ground |
| DATA | 6 | 11 | Digital output | Modulator data output |
| CLKIN | 7 | 13 | Digital input | Modulator clock input |
| DVDD | 8 | 14 | Power | Controller-side power supply |
| NC | — | 5-7, 10, 12, 15 | — | No internal connection; can be tied to any potential or left unconnected |

(1) Both pins are connected internally via a low-impedance path; thus, only one of the pins must be tied to the ground plane.

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# 7 Specifications

## 7.1 Absolute Maximum Ratings

see (1)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply voltage, AVDD to AGND or DVDD to DGND | –0.3 | 6 | V |
| Analog input voltage at VINP, VINN | AGND – 0.5 | AVDD + 0.5 | V |
| Digital input voltage at CLKIN | DGND – 0.3 | DVDD + 0.3 | V |
| Input current to any pin except supply pins | –10 | 10 | mA |
| Maximum virtual junction temperature, $T_J$ | | 150 | °C |
| Operating ambient temperature, $T_{OA}$ | –40 | 125 | °C |
| Storage temperature, $T_{stg}$ | –65 | 150 | °C |

(1) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under the *Electrical Characteristics* is not implied. Exposure to absolute maximum rated conditions for extended periods may affect device reliability.

## 7.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human-body model (HBM), per JEDEC standard 22, test method A114-C.01 (1) | ±3000 | V |
| | | Charged-device model (CDM), per JEDEC standard 22, test method C101 (2) | ±1500 | |
| | | Machine model (MM), per JEDEC standard 22, test method A115A | ±200 | |

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

## 7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $T_A$ | Operating ambient temperature | –40 | | 105 | °C |
| AVDD | High-side (analog) supply voltage | 4.5 | 5 | 5.5 | V |
| DVDD | Controller-side (digital) supply voltage | 2.7 | 3.3 | 5.5 | V |

## 7.4 Thermal Information

| THERMAL METRIC (1) | | AMC1204, AMC1204B | | UNIT |
|---|---|---|---|---|
| | | DW (SOIC) | DWV (SOIC) | |
| | | 16 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 78.5 | 106.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 41.3 | 53.6 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 50.2 | 60.3 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 11.5 | 18.5 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 41.2 | 58.9 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | n/a | n/a | °C/W |

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC package thermal metrics* application report.


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## 7.5 Power Ratings

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $P_D$ | Maximum power dissipation (both sides) | AVDD = DVDD = 5.5 V | | | 115.5 | mW |
| | | AVDD = 5.5 V, DVDD = 3.6 V | | | 102.4 | |
| $P_{D1}$ | Maximum power dissipation (high-side supply) | AVDD = 5.5 V | | | 88.0 | mW |
| $P_{D2}$ | Maximum power dissipation (low-side supply) | DVDD = 5.5 V | | | 27.5 | mW |
| | | DVDD = 3.6 V | | | 14.4 | |

## 7.6 Insulation Specifications

over operating ambient temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | VALUE | UNIT |
|---|---|---|---|---|
| **GENERAL** | | | | |
| CLR | External clearance(1) | Shortest pin-to-pin distance through air, DW package | ≥ 8 | mm |
| | | Shortest pin-to-pin distance through air, DWV package | ≥ 8.5 | |
| CPG | External creepage(1) | Shortest pin-to-pin distance across the package surface, DW package | ≥ 8 | mm |
| | | Shortest pin-to-pin distance across the package surface, DWV package | ≥ 8.5 | |
| DTI | Distance through insulation | Minimum internal gap (internal clearance) of the insulation | ≥ 0.014 | mm |
| CTI | Comparative tracking index | DIN EN 60112 (VDE 0303-11); IEC 60112, DW package | ≥ 400 | V |
| | | DIN EN 60112 (VDE 0303-11); IEC 60112, DWV package | ≥ 175 | |
| | Material group | According to IEC 60664-1, DW package | II | |
| | | According to IEC 60664-1, DWV package | III | |
| | Overvoltage category per IEC 60664-1 | Rated mains voltage ≤ 300 $V_{RMS}$ | I-IV | |
| | | Rated mains voltage ≤ 600 $V_{RMS}$ | I-III | |
| **DIN VDE V 0884-11: 2017-01(2)** | | | | |
| $V_{IORM}$ | Maximum repetitive peak isolation voltage | At ac voltage (bipolar) | 1200 | $V_{PK}$ |
| $V_{IOWM}$ | Maximum-rated isolation working voltage | At ac voltage (sine wave) | 849 | $V_{RMS}$ |
| | | At dc voltage | 1200 | $V_{DC}$ |
| $V_{IOTM}$ | Maximum transient isolation voltage | $V_{TEST} = V_{IOTM}$, t = 60 s (qualification test), AMC1204B | 4250 | $V_{PK}$ |
| | | $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production test), AMC1204B | 5100 | |
| | | $V_{TEST} = V_{IOTM}$, t = 60 s (qualification test), AMC1204 | 4000 | |
| | | $V_{TEST} = 1.2 \times V_{IOTM}$, t = 1 s (100% production test), AMC1204 | 4800 | |
| $V_{IOSM}$ | Maximum surge isolation voltage(3) | Test method per IEC 60065, 1.2/50-µs waveform, $V_{TEST} = 1.3 \times V_{IOSM} = 6000\ V_{PK}$ (qualification) | 4615 | $V_{PK}$ |

(1) Apply creepage and clearance requirements according to the specific equipment isolation standards of an application. Care must be taken to maintain the creepage and clearance distance of a board design to ensure that the mounting pads of the isolator on the printed circuit board (PCB) do not reduce this distance. Creepage and clearance on a PCB become equal in certain cases. Techniques such as inserting grooves and ribs on the PCB are used to help increase these specifications.
(2) This coupler is suitable for *safe electrical insulation* only within the safety ratings. Compliance with the safety ratings shall be ensured by means of suitable protective circuits.
(3) Testing is carried out in air or oil to determine the intrinsic surge immunity of the isolation barrier.

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## Insulation Specifications (continued)

over operating ambient temperature range (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | VALUE | UNIT |
|---|---|---|---|---|
| $q_{pd}$ | Apparent charge(4) | Method a, after input/output safety test subgroup 2 / 3, $V_{ini} = V_{IOTM}$, $t_{ini} = 60$ s, $V_{pd(m)} = 1.2 \times V_{IORM} = 1440\ V_{PK}$, $t_m = 10$ s | ≤ 5 | pC |
| | | Method a, after environmental tests subgroup 1, $V_{ini} = V_{IOTM}$, $t_{ini} = 60$ s, $V_{pd(m)} = 1.3 \times V_{IORM} = 1560\ V_{PK}$, $t_m = 10$ s | ≤ 5 | |
| | | Method b1, at routine test (100% production) and preconditioning (type test), $V_{ini} = V_{IOTM}$, $t_{ini} = 1$ s, $V_{pd(m)} = 1.5 \times V_{IORM} = 1800\ V_{PK}$, $t_m = 1$ s | ≤ 5 | |
| $C_{IO}$ | Barrier capacitance, input to output(5) | $V_{IO} = 0.5\ V_{PP}$ at 1 MHz | 1.2 | pF |
| $R_{IO}$ | Insulation resistance, input to output(5) | $V_{IO} = 500$ V at $T_A < 85°C$ | $> 10^{12}$ | Ω |
| | | $V_{IO} = 500$ V at $85°C < T_A < 105°C$ | $> 10^{11}$ | |
| | | $V_{IO} = 500$ V at $T_S = 150°C$ | $> 10^9$ | |
| | Pollution degree | | 2 | |
| | Climatic category | | 40/125/21 | |
| **UL1577** | | | | |
| $V_{ISO}$ | Withstand isolation voltage | $V_{TEST} = V_{ISO} = 3005\ V_{RMS}$ or $4250\ V_{DC}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 3606\ V_{RMS}$, t = 1 s (100% production test), AMC1204B | 3005 | $V_{RMS}$ |
| | | $V_{TEST} = V_{ISO} = 2500\ V_{RMS}$ or $4000\ V_{DC}$, t = 60 s (qualification), $V_{TEST} = 1.2 \times V_{ISO} = 2800\ V_{RMS}$, t = 1 s (100% production test), AMC1204 | 2500 | |

(4) Apparent charge is electrical discharge caused by a partial discharge (pd).
(5) All pins on each side of the barrier are tied together, creating a two-pin device.


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## 7.7 Safety-Related Certifications

| VDE | UL | CSA |
|---|---|---|
| Certified according to DIN VDE V 0884-11: 2017-01 and DIN EN 61010-1 (VDE 0411-1): 2011-07 | Recognized under 1577 component recognition program | Recognized under CSA component acceptance NO 5 program, IEC 60950-1, and IEC 61010-1 |
| Basic insulation | Single protection | Basic insulation |
| Certificate number: 40047657 | File number: E181974 | Certificate number: 2350550 |

## 7.8 Safety Limiting Values

Safety limiting intends to minimize potential damage to the isolation barrier upon failure of input or output circuitry.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $I_S$ | Safety input, output, or supply current | DW-package, $R_{\theta JA}$ = 78.5°C/W, $T_J$ = 150°C, $T_A$ = 25°C, AVDD = DVDD = 5.5 V, see Figure 2 | | | 289 | mA |
| | | DWV-package, $R_{\theta JA}$ =106.5°C/W, $T_J$ = 150°C, $T_A$ = 25°C, AVDD = DVDD = 5.5 V, see Figure 2 | | | 213 | |
| $P_S$ | Safety input, output, or total power(1) | DW-package, $R_{\theta JA}$ = 78.5°C/W, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 3 | | | 1592 | mW |
| | | DWV-package, $R_{\theta JA}$ = 106.5°C/W, $T_J$ = 150°C, $T_A$ = 25°C, see Figure 3 | | | 1173 | mW |
| $T_S$ | Maximum safety temperature | | | | 150 | °C |

(1) The maximum safety temperature, $T_S$, has the same value as the maximum junction temperature, $T_J$, specified for the device. The $I_S$ and $P_S$ parameters represent the safety current and safety power, respectively. Do not exceed the maximum limits of $I_S$ and $P_S$. These limits vary with the ambient temperature, $T_A$.
The junction-to-air thermal resistance, $R_{\theta JA}$, in the *Thermal Information* table is that of a device installed on a high-K test board for leaded surface-mount packages. Use these equations to calculate the value for each parameter:
$T_J = T_A + R_{\theta JA} \times P$, where P is the power dissipated in the device.
$T_{J(max)} = T_S = T_A + R_{\theta JA} \times P_S$, where $T_{J(max)}$ is the maximum junction temperature.
$P_S = I_S \times AVDD_{max} + I_S \times DVDD_{max}$, where $AVDD_{max}$ is the maximum high-side supply voltage and $DVDD_{max}$ is the maximum controller-side supply voltage.

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## 7.9 Electrical Characteristics

All minimum/maximum specifications at $T_A$ = –40°C to 105°C, AVDD = 4.5 V to 5.5 V, DVDD = 2.7 V to 5.5 V, VINP = –250 mV to 250 mV, VINN = 0 V, and sinc$^3$ filter with OSR = 256, unless otherwise noted.
Typical values are at $T_A$ = 25°C, AVDD = 5 V, and DVDD = 3.3 V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **RESOLUTION** | | | | | | |
| | Resolution | | 16 | | | Bits |
| **DC ACCURACY** | | | | | | |
| INL | Integral linearity error(1) | $T_A$ = –40°C to 85°C | –8 | ±2 | 8 | LSB |
| | | $T_A$ = –40°C to 105°C | –16 | ±5 | 16 | LSB |
| DNL | Differential nonlinearity | | –1 | | 1 | LSB |
| $V_{OS}$ | Offset error(2) | | –1 | ±0.1 | 1 | mV |
| $TCV_{OS}$ | Offset error thermal drift | | –3.5 | ±1 | 3.5 | µV/°C |
| $G_{ERR}$ | Gain error(2) | | –2% | ±0.5% | 2% | |
| $TCG_{ERR}$ | Gain error thermal drift | | | ±30 | | ppm/°C |
| PSRR | Power-supply rejection ratio | | | 79 | | dB |
| **ANALOG INPUTS** | | | | | | |
| FSR | Full-scale differential voltage input range | VINP – VINN | | ±320 | | mV |
| | Specified FSR | | –250 | | 250 | mV |
| $V_{CM}$ | Operating common-mode signal(3) | | –160 | | AVDD | mV |
| $C_I$ | Input capacitance to AGND | VINP or VINN | | 7 | | pF |
| $C_{ID}$ | Differential input capacitance | | | 3.5 | | pF |
| $R_{ID}$ | Differential input resistance | | | 12.5 | | kΩ |
| $I_{IL}$ | Input leakage current | VINP – VINN = ±250 mV | –10 | | 10 | µA |
| | | VINP – VINN = ±320 mV | –50 | | 50 | µA |
| CMTI | Common-mode transient immunity | | 15 | | | kV/µs |
| CMRR | Common-mode rejection ratio | $V_{IN}$ from 0 V to 5 V at 0 Hz | | 108 | | dB |
| | | $V_{IN}$ from 0 V to 5 V at 100 kHz | | 114 | | dB |
| **EXTERNAL CLOCK** | | | | | | |
| $t_{CLKIN}$ | Clock period | | 45.5 | 50 | 200 | ns |
| $f_{CLKIN}$ | Input clock frequency | | 5 | 20 | 22 | MHz |
| $Duty_{CLKIN}$ | Duty cycle | 5 MHz ≤ $f_{CLKIN}$ < 20 MHz | 40% | 50% | 60% | |
| | | 20 MHz ≤ $f_{CLKIN}$ ≤ 22 MHz | 45% | 50% | 55% | |
| **AC ACCURACY** | | | | | | |
| SINAD | Signal-to-noise + distortion | $f_{IN}$ = 1kHz, $T_A$ = –40°C to 85°C | 78 | 87 | | dB |
| | | $f_{IN}$ = 1kHz, $T_A$ = –40°C to 105°C | 70 | 87 | | dB |
| SNR | Signal-to-noise ratio | $f_{IN}$ = 1kHz, $T_A$ = –40°C to 85°C | 84 | 88 | | dB |
| | | $f_{IN}$ = 1kHz, $T_A$ = –40°C to 105°C | 83 | 88 | | dB |
| THD | Total harmonic distortion | $f_{IN}$ = 1kHz, $T_A$ = –40°C to 85°C | | –96 | –80 | dB |
| | | $f_{IN}$ = 1kHz, $T_A$ = –40°C to 105°C | | –96 | –70 | dB |
| SFDR | Spurious-free dynamic range | $f_{IN}$ = 1kHz, $T_A$ = –40°C to 85°C | 82 | 96 | | dB |
| | | $f_{IN}$ = 1kHz, $T_A$ = –40°C to 105°C | 72 | 96 | | dB |
| **DIGITAL INPUTS(3)** | | | | | | |
| $I_{IN}$ | Input current | $V_{IN}$ = DVDD to DGND | –10 | | 10 | µA |
| $C_{IN}$ | Input capacitance | | | 5 | | pF |
| **CMOS Logic Family (CMOS With Schmitt-Trigger)** | | | | | | |
| $V_{IH}$ | High-level input voltage | DVDD = 4.5V to 5.5V | 0.7DVDD | | DVDD + 0.3 | V |
| $V_{IL}$ | Low-level input voltage | DVDD = 4.5V to 5.5V | –0.3 | | 0.3DVDD | V |
| **LVCMOS Logic Family** | | | | | | |
| $V_{IH}$ | High-level input voltage | DVDD = 2.7 V to 3.6 V | 2 | | DVDD + 0.3 | V |

(1) Integral nonlinearity is defined as the maximum deviation from a straight line passing through the end-points of the ideal ADC transfer function expressed as number of LSBs or as a percent of the specified 500-mV input range.
(2) Maximum values, including temperature drift, are ensured over the full specified temperature range.
(3) Ensured by design.


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## Electrical Characteristics (continued)

All minimum/maximum specifications at $T_A$ = –40°C to 105°C, AVDD = 4.5 V to 5.5 V, DVDD = 2.7 V to 5.5 V, VINP = –250 mV to 250 mV, VINN = 0 V, and $sinc^3$ filter with OSR = 256, unless otherwise noted.
Typical values are at $T_A$ = 25°C, AVDD = 5 V, and DVDD = 3.3 V.

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Low-level input voltage | DVDD = 2.7 V to 3.6 V | –0.3 | | 0.8 | V |
| **DIGITAL OUTPUTS**(3) | | | | | | |
| $C_{OUT}$ | Output capacitance | | | 5 | | pF |
| $C_{LOAD}$ | Load capacitance | | | | 30 | pF |
| **CMOS Logic Family** | | | | | | |
| $V_{OH}$ | High-level output voltage | DVDD = 4.5 V, $I_{OH}$ = –100 µA | 4.4 | | | V |
| $V_{OL}$ | Low-level output voltage | DVDD = 4.5 V, $I_{OL}$ = 100 µA | | | 0.5 | V |
| **LVCMOS Logic Family** | | | | | | |
| $V_{OH}$ | High-level output voltage | $I_{OH}$ = 20 µA | DVDD – 0.1 | | | V |
| | | $I_{OH}$ = –4 mA, 2.7 V ≤ DVDD ≤ 3.6 V | DVDD – 0.4 | | | V |
| | | $I_{OH}$ = –4 mA, 4.5 V ≤ DVDD ≤ 5.5 V | DVDD – 0.8 | | | V |
| $V_{OL}$ | Low-level output voltage | $I_{OL}$ = 20 µA | | | 0.1 | V |
| | | $I_{OL}$ = 4 mA | | | 0.4 | V |
| **POWER SUPPLY** | | | | | | |
| AVDD | High-side supply voltage | | 4.5 | 5 | 5.5 | V |
| DVDD | Controller-side supply voltage | | 2.7 | 3.3 | 5.5 | V |
| $I_{AVDD}$ | High-side supply current | 4.5 V ≤ AVDD ≤ 5.5 V | | 11 | 16 | mA |
| $I_{DVDD}$ | Controller-side supply current | 2.7 V ≤ DVDD ≤ 3.6 V | | 2 | 4 | mA |
| | | 4.5V ≤ DVDD ≤ 5.5 V | | 2.8 | 5 | mA |
| $P_D$ | Power dissipation | AVDD = 5.5 V, DVDD = 3.6 V | | 61.6 | 102.4 | mW |

## 7.10 Timing Requirements

Over recommended ranges of supply voltage and operating free-air temperature, unless otherwise noted. (See Figure 1)

| | | MIN | NOM | MAX | UNIT |
|---|---|---|---|---|---|
| $t_{CLK}$ | CLKIN clock period | 45.5 | 50 | 200 | ns |
| $t_{HIGH}$ | CLKIN clock high time | 20 | 25 | 120 | ns |
| $t_{LOW}$ | CLKIN clock low time | 20 | 25 | 120 | ns |
| $t_D$ | Delayed falling edge of CLKIN to DATA valid | 2 | | 15 | ns |

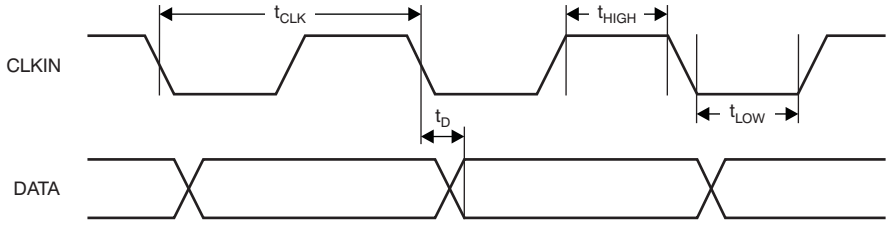



**Figure 1. Modulator Output Timing**

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## 7.11 Insulation Characteristics Curves

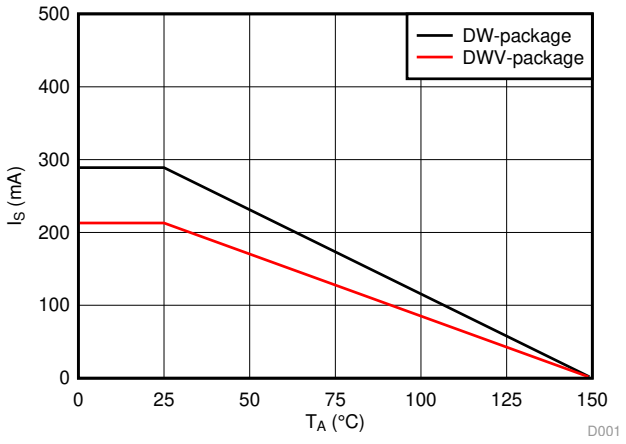



**Figure 2. Thermal Derating Curve for Safety-Limiting Current per VDE**

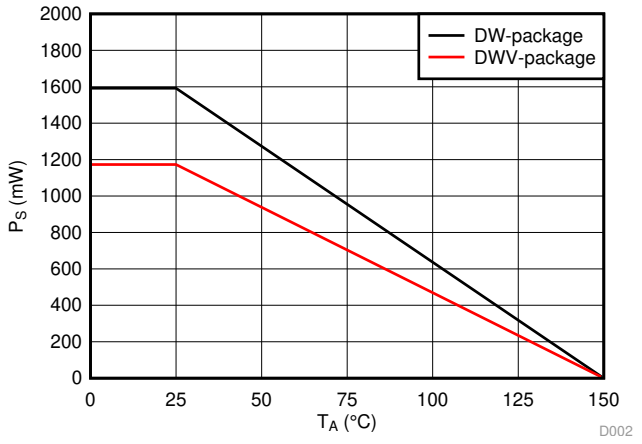



**Figure 3. Thermal Derating Curve for Safety-Limiting Power per VDE**


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## 7.12 Typical Characteristics

at AVDD = 5 V, DVDD = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and sinc$^3$ filter with OSR = 256 (unless otherwise noted)

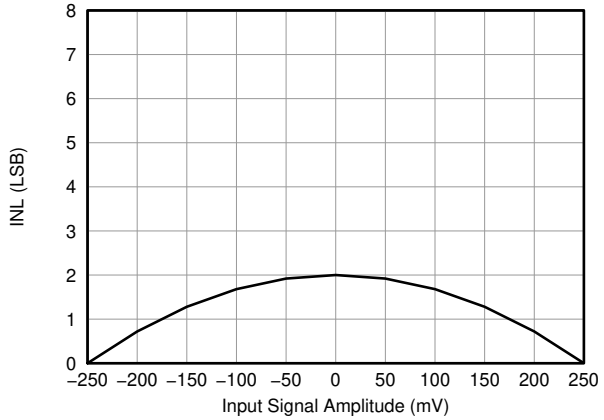



**Figure 4. Integral Nonlinearity vs Input Signal Amplitude**

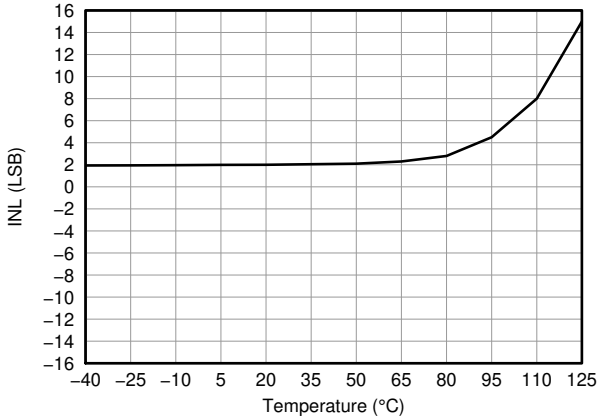



**Figure 5. Integral Nonlinearity vs Temperature**

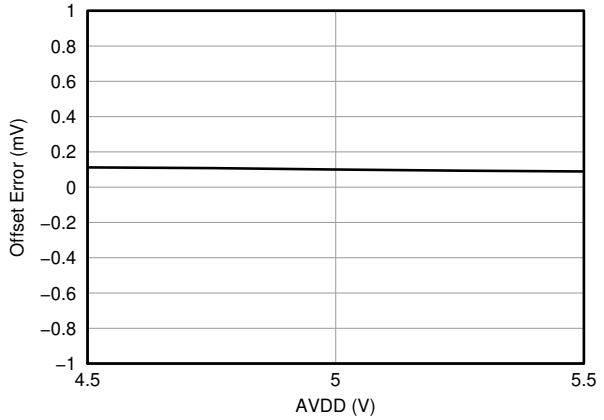



**Figure 6. Offset Error vs Analog Supply Voltage**

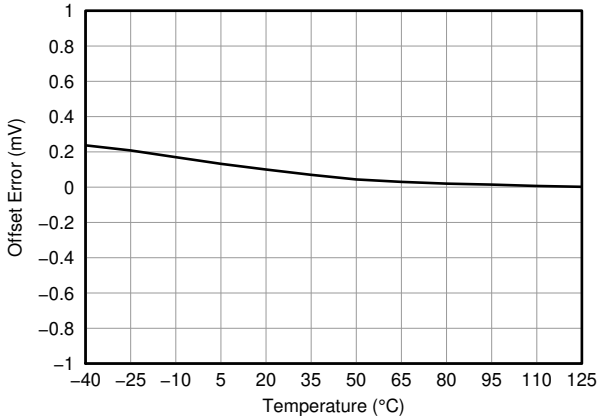



**Figure 7. Offset Error vs Temperature**

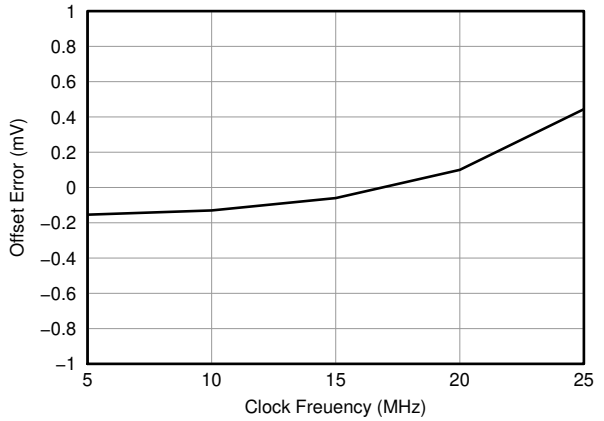



**Figure 8. Offset Error vs Clock Frequency**

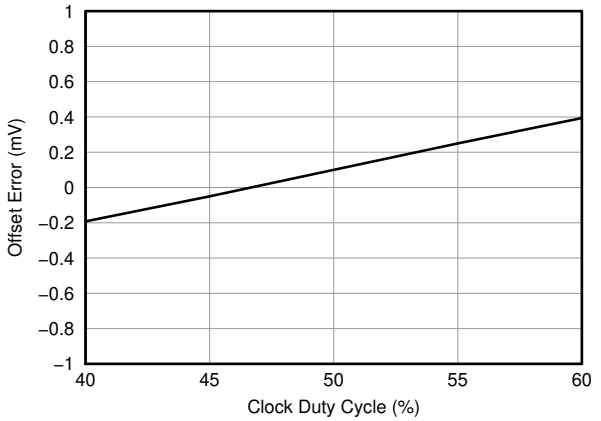



**Figure 9. Offset Error vs Clock Duty Cycle**

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## Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and sinc$^3$ filter with OSR = 256 (unless otherwise noted)

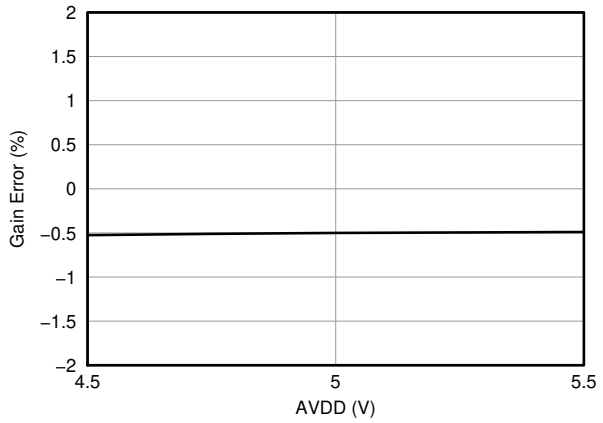



**Figure 10. Gain Error vs Analog Supply Voltage**

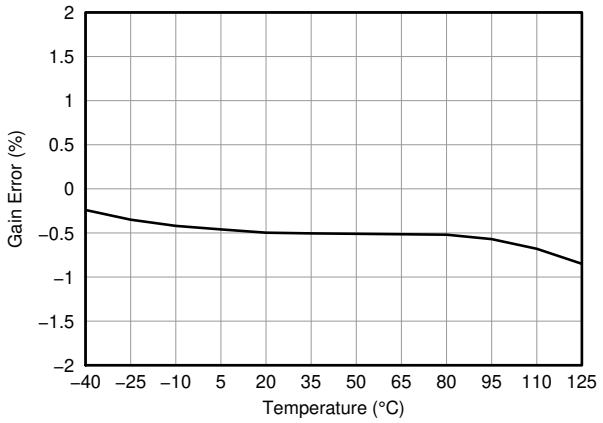



**Figure 11. Gain Error vs Temperature**

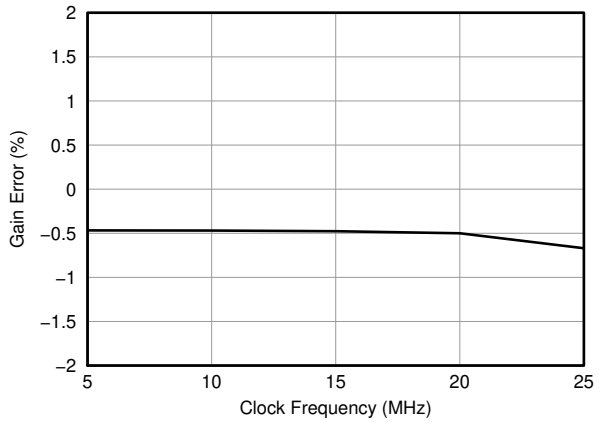



**Figure 12. Gain Error vs Clock Frequency**

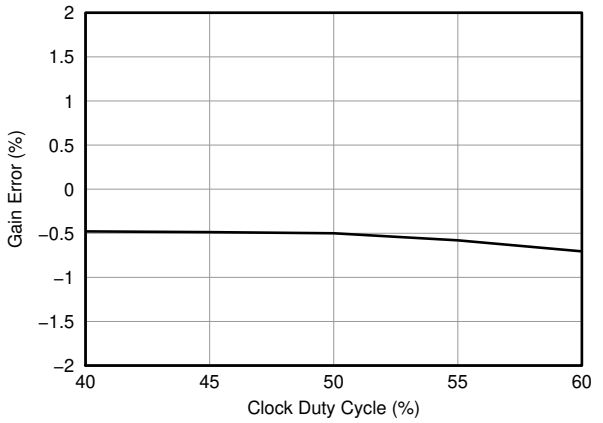



**Figure 13. Gain Error vs Clock Duty Cycle**

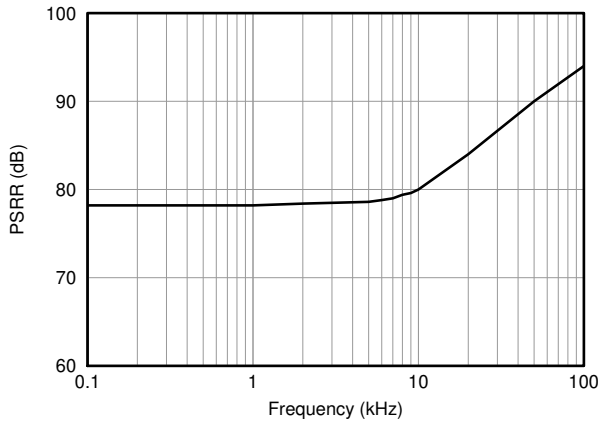



**Figure 14. Power-Supply Rejection Ratio vs Frequency**

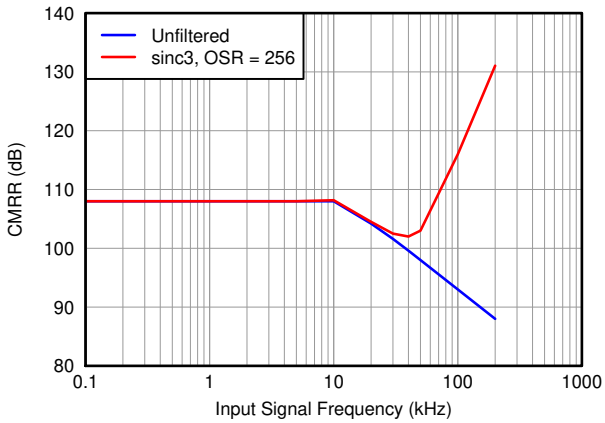



**Figure 15. Common-Mode Rejection Ratio vs Input Signal Frequency**


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## Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and sinc$^3$ filter with OSR = 256 (unless otherwise noted)

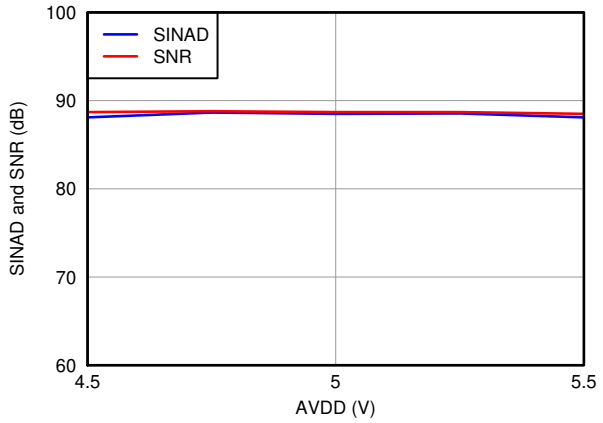



**Figure 16. SINAD and SNR vs Analog Supply Voltage**

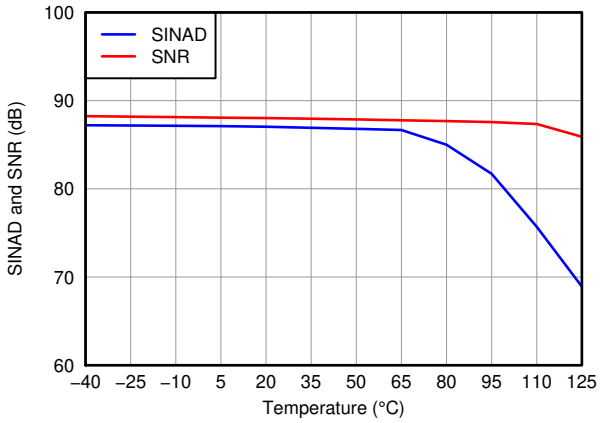



**Figure 17. SINAD and SNR vs Temperature**

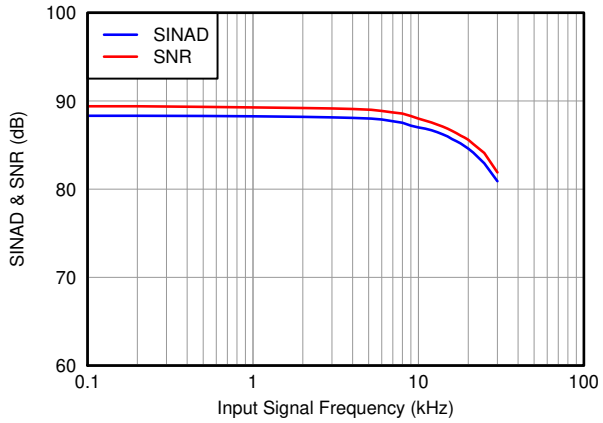



**Figure 18. SINAD and SNR vs Input Signal Frequency**

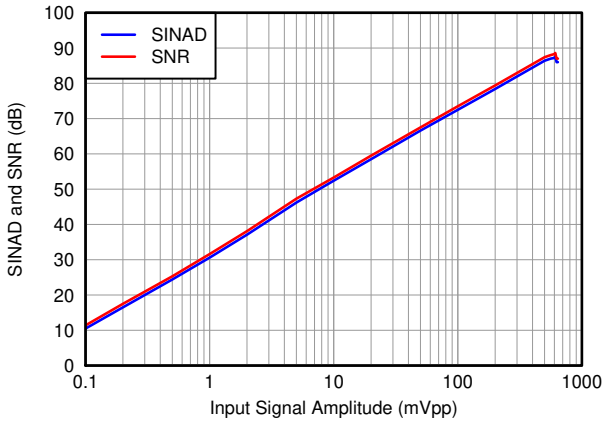



**Figure 19. SINAD and SNR vs Input Signal Amplitude**

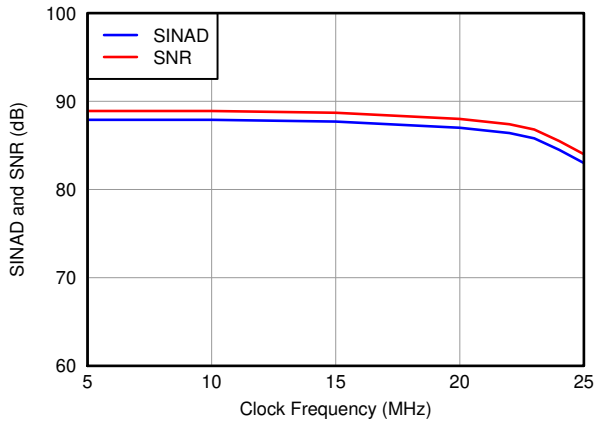



**Figure 20. SINAD and SNR vs Clock Frequency**

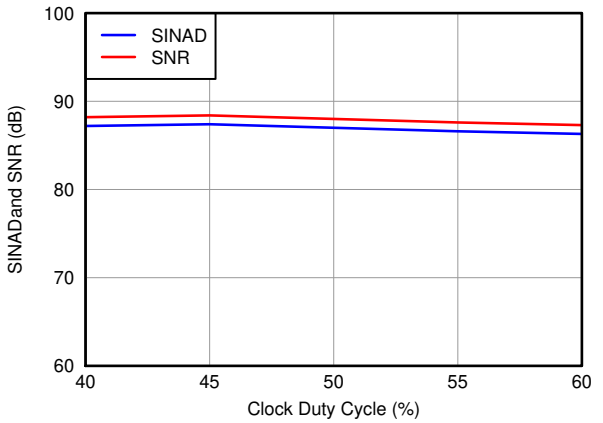



**Figure 21. SINAD and SNR vs Clock Duty Cycle**

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## Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and sinc$^3$ filter with OSR = 256 (unless otherwise noted)

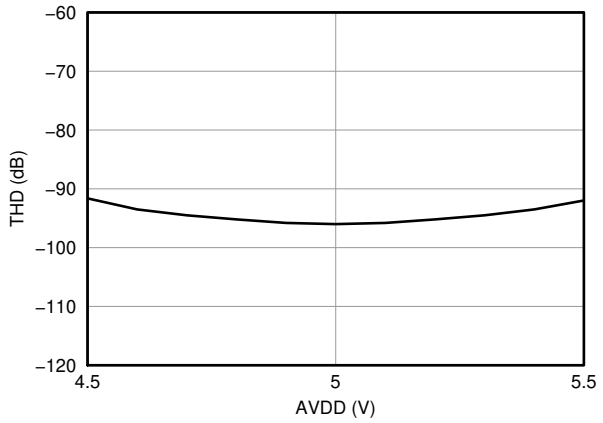



**Figure 22. Total Harmonic Distortion vs Analog Supply Voltage**

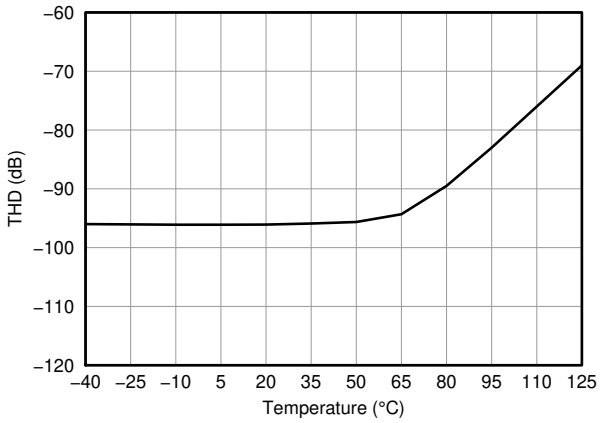



**Figure 23. Total Harmonic Distortion vs Temperature**

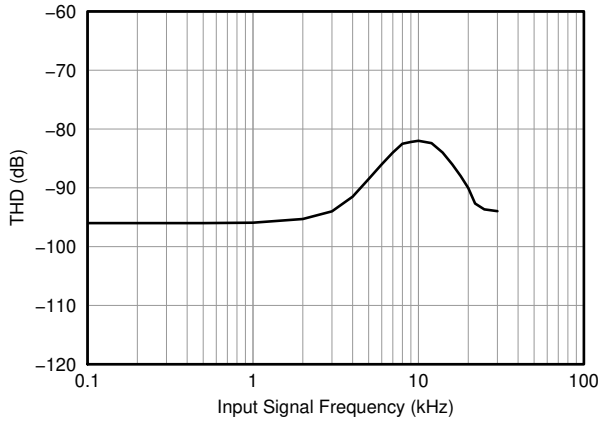



**Figure 24. Total Harmonic Distortion vs Input Signal Frequency**

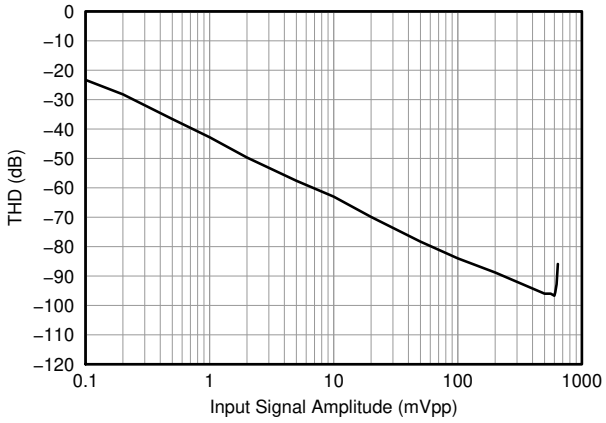



**Figure 25. Total Harmonic Distortion vs Input Signal Amplitude**

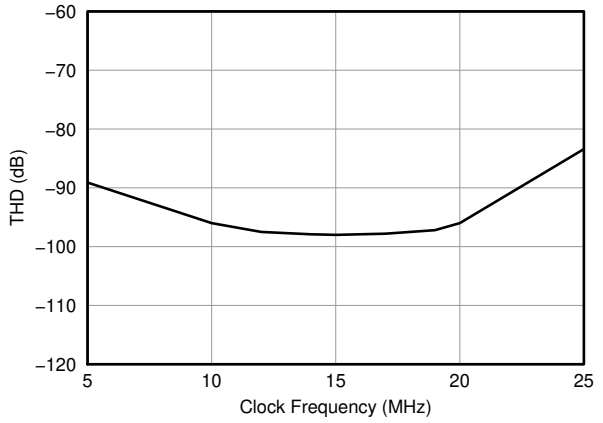



**Figure 26. Total Harmonic Distortion vs Clock Frequency**

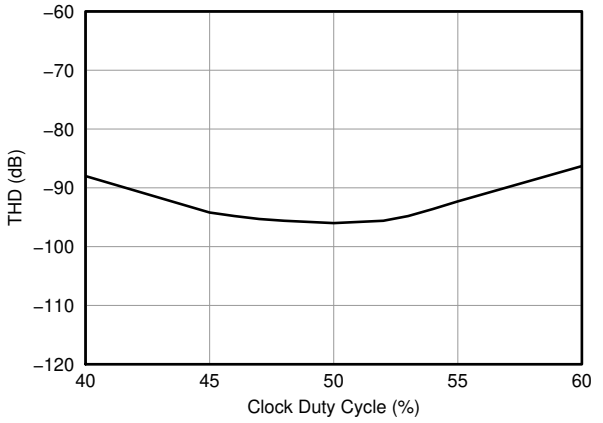



**Figure 27. Total Harmonic Distortion vs Clock Duty Cycle**


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## Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and sinc$^3$ filter with OSR = 256 (unless otherwise noted)

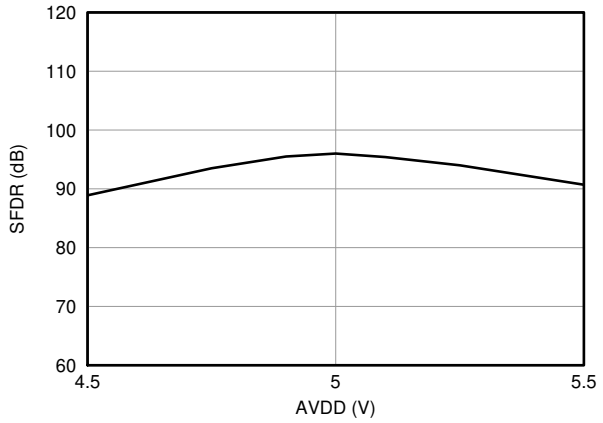



**Figure 28. Spurious-Free Dynamic Range vs Analog Supply Voltage**

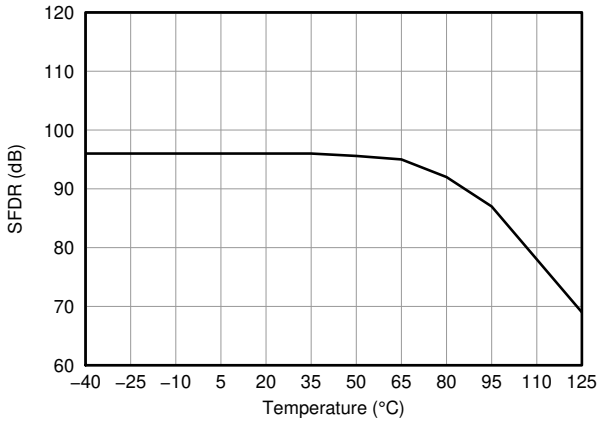



**Figure 29. Spurious-Free Dynamic Range vs Temperature**

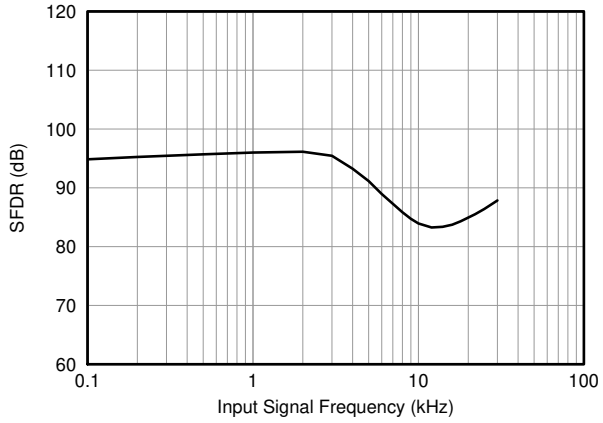



**Figure 30. Spurious-Free Dynamic Range vs Input Signal Frequency**

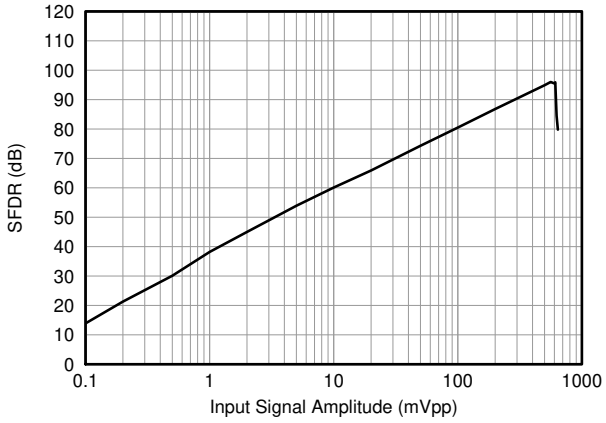



**Figure 31. Spurious-Free Dynamic Range vs Input Signal Amplitude**

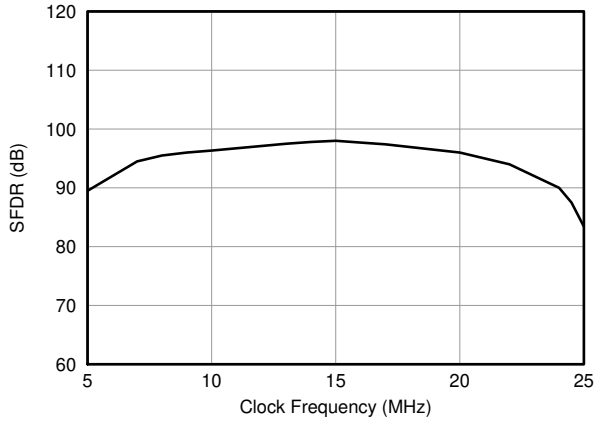



**Figure 32. Spurious-Free Dynamic Range vs Clock Frequency**

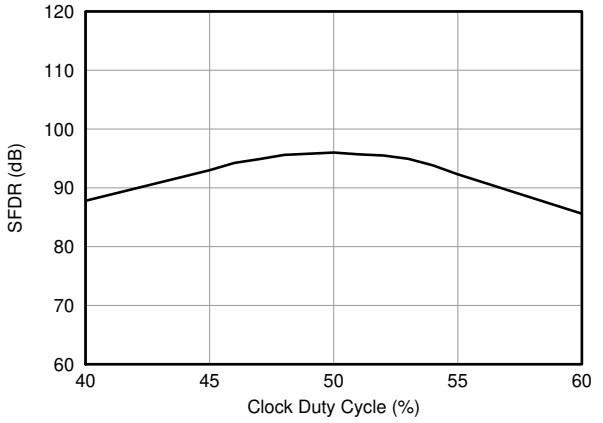



**Figure 33. Spurious-Free Dynamic Range vs Clock Duty Cycle**

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## Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and sinc$^3$ filter with OSR = 256 (unless otherwise noted)

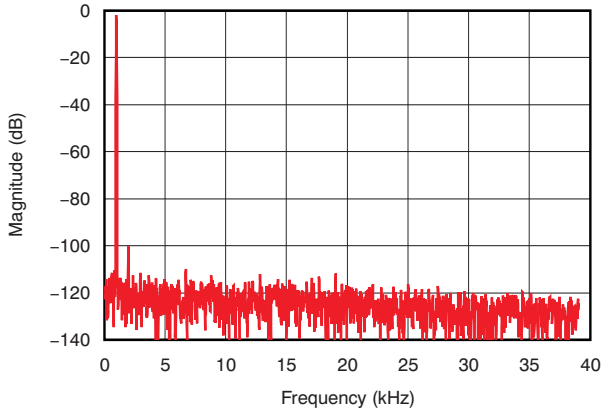



**Figure 34. Frequency Spectrum (4096 Point FFT, $f_{IN}$ = 1 kHz, 0.56 $V_{PP}$)**

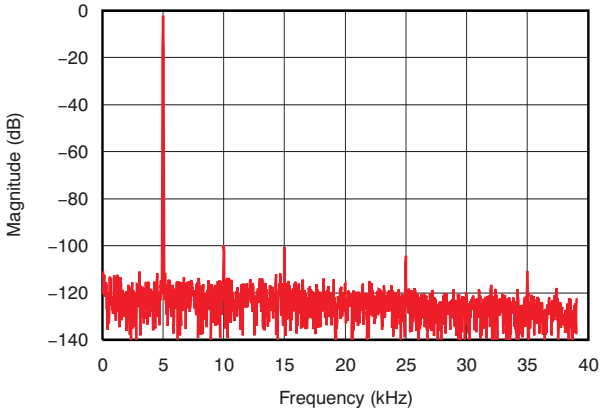



**Figure 35. Frequency Spectrum (4096 Point FFT, $f_{IN}$ = 5 kHz, 0.56 $V_{PP}$)**

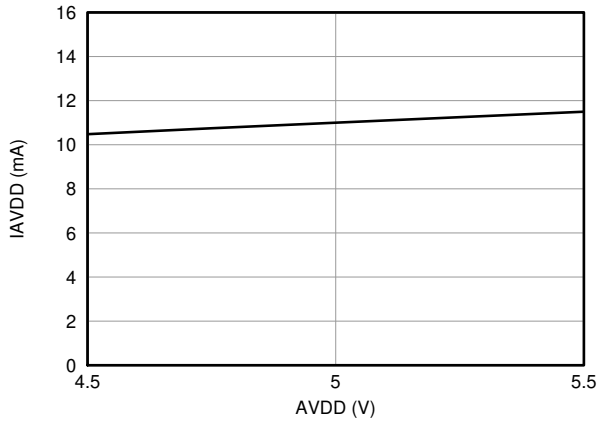



**Figure 36. Analog Supply Current vs Analog Supply Voltage**

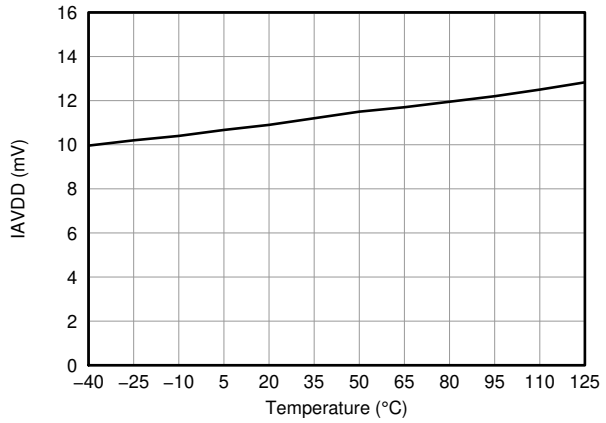



**Figure 37. Analog Supply Current vs Temperature**

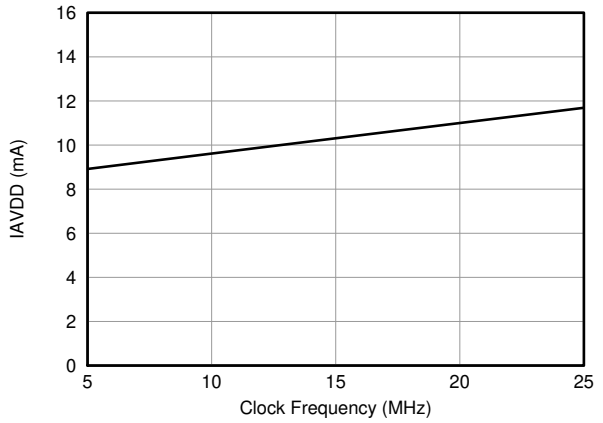



**Figure 38. Analog Supply Current vs Clock Frequency**

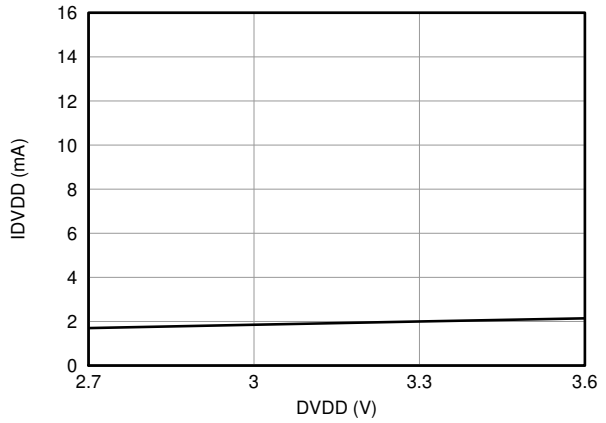



**Figure 39. Digital Supply Current vs Digital Supply Voltage (3 V)**


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## Typical Characteristics (continued)

at AVDD = 5 V, DVDD = 3.3 V, VINP = –250 mV to 250 mV, VINN = 0 V, and sinc$^3$ filter with OSR = 256 (unless otherwise noted)

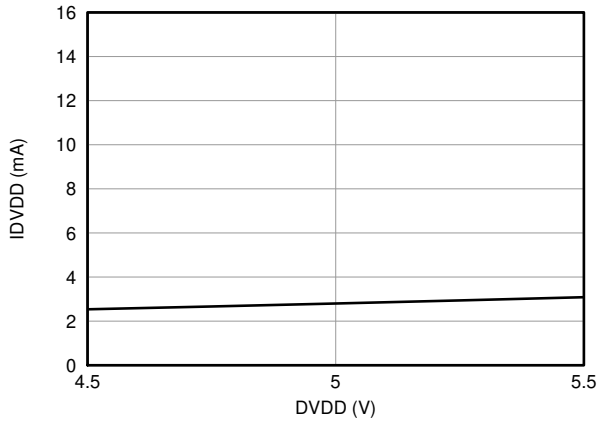



**Figure 40. Digital Supply Current vs Digital Supply Voltage (5 V)**

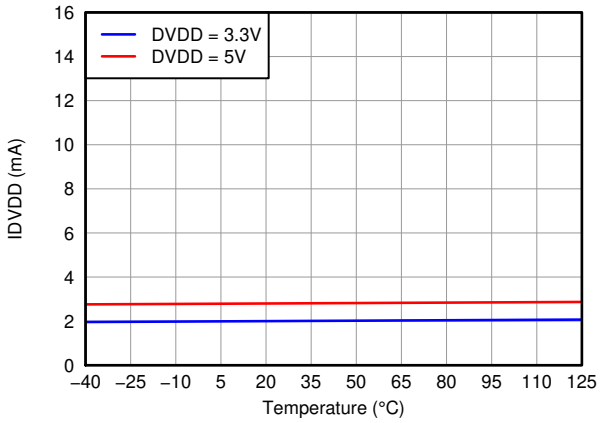



**Figure 41. Digital Supply Current vs Temperature**

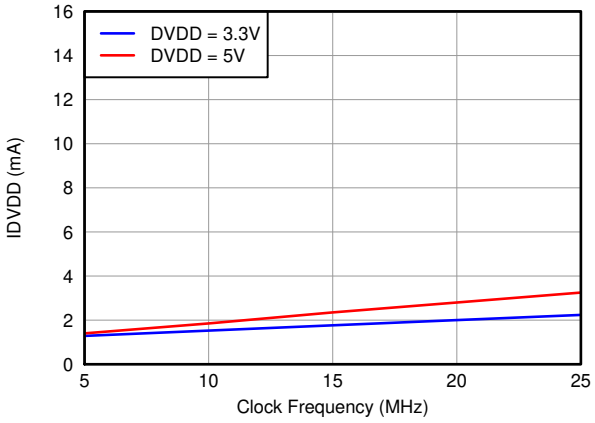



**Figure 42. Digital Supply Current vs Clock Frequency**

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# 8 Detailed Description

## 8.1 Overview

The AMC1204 and AMC1204B are single-channel, second-order, delta-sigma (ΔΣ) modulators designed for medium- to high-resolution analog-to-digital conversions. The isolated output of the converter (DATA) provides a stream of digital ones and zeros accurately representing the analog input voltage over time. The time average of this serial output is proportional to the analog input voltage.

The *Functional Block Diagram* shows a detailed block diagram of the AMC1204 and AMC1204B. The analog input range is tailored to directly accommodate the voltage drop across a shunt resistor used for current sensing. The $SiO_2$-based capacitive isolation barrier supports a high level of magnetic field immunity as described in the *ISO72x Digital Isolator Magnetic-Field Immunity* application report. The external clock input simplifies the synchronization of multiple current sense channels on system level. The extended frequency range of up to 20 MHz supports higher performance levels compared to the other solutions available on the market.

## 8.2 Functional Block Diagram

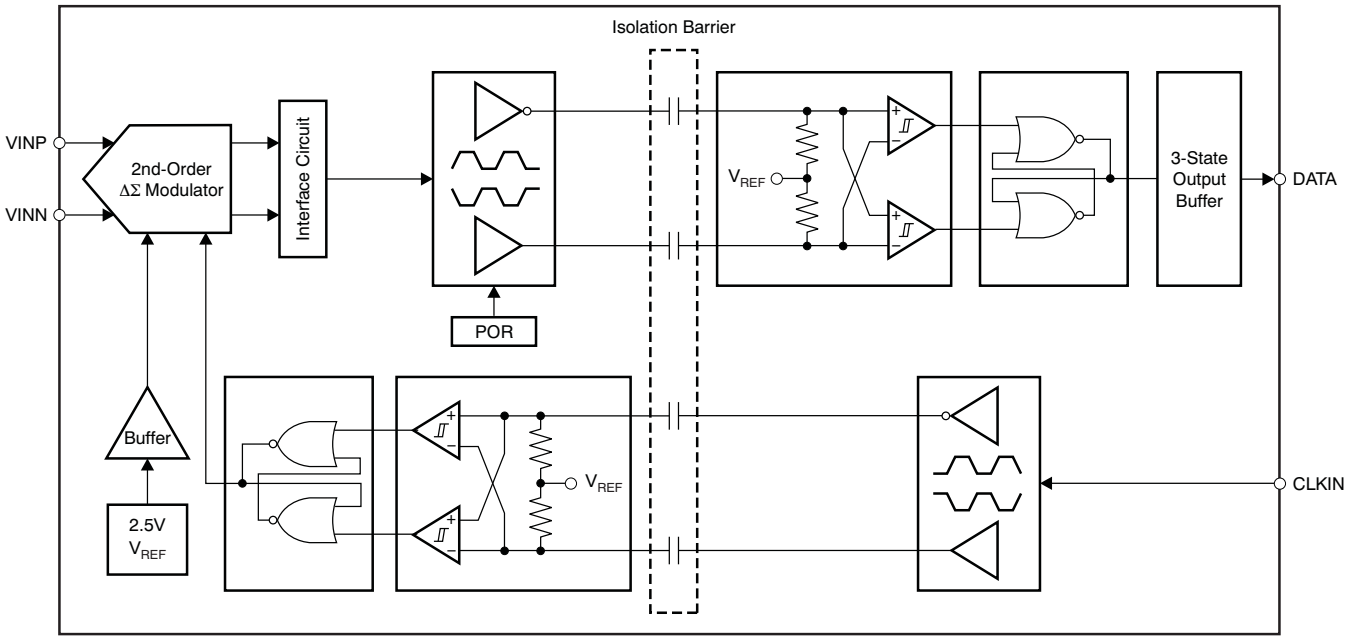



**Figure 43. Detailed Block Diagram**


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## 8.3 Feature Description

### 8.3.1 Analog Input

The differential analog input of the AMC1204 and AMC1204B is implemented with a switched-capacitor circuit.

The AMC1204 and AMC1204B measure the differential input signal $V_{IN}$ = (VINP – VINN) against the internal reference of 2.5 V using internal capacitors that are continuously charged and discharged. Figure 44 shows the simplified schematic of the AMC1204 and AMC1204B input circuitry; the right side of Figure 44 illustrates the input circuitry with the capacitors and switches replaced by an equivalent circuit.

In Figure 44, the $S_1$ switches close during the input sampling phase. With the $S_1$ switches closed, $C_{DIFF}$ charges to the voltage difference across VINP and VINN. For the discharge phase, both $S_1$ switches open first and then both $S_2$ switches close. $C_{DIFF}$ discharges approximately to AGND + 0.8 V during this phase. This two-phase sample/discharge cycle repeats with a period of $t_{CLKIN} = 1/f_{CLKIN}$. $f_{CLKIN}$ is the operating frequency of the modulator. The capacitors $C_{IP}$ and $C_{IN}$ are of parasitic nature and caused by bonding wires and the internal ESD protection structure.

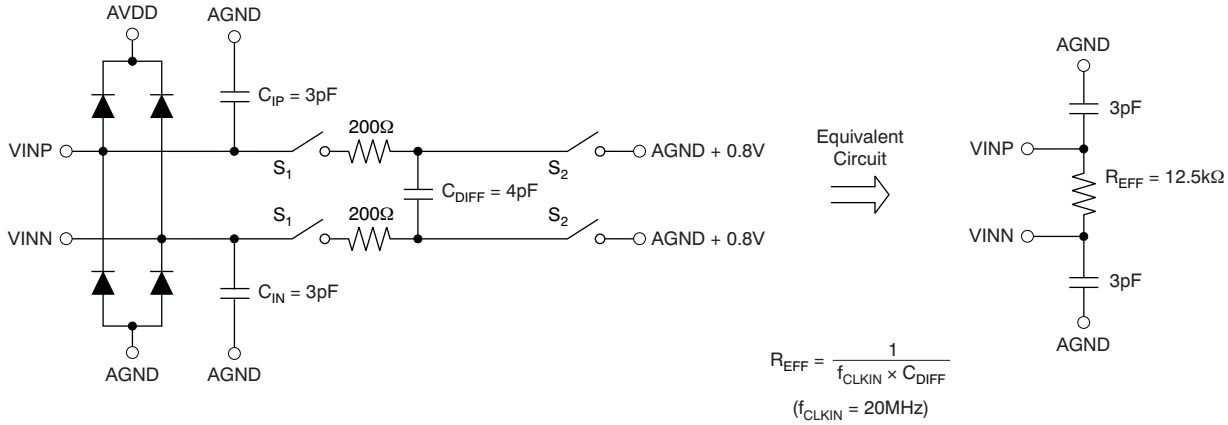



**Figure 44. Equivalent Analog Input Circuit**

There are two restrictions on the analog input signals VINP and VINN. First, if the input voltage exceeds the range AGND – 0.5 V to AVDD + 0.3 V, the input current must be limited to 10 mA because the input protection diodes on the front end of the converter begin to turn on. In addition, the linearity and the noise performance of the device are ensured only when the differential analog input voltage remains within ±250 mV.

### 8.3.2 Modulator

The modulator topology of the AMC1204 and AMC1204B is fundamentally a second-order, switched-capacitor, ΔΣ modulator, such as the one conceptualized in Figure 45. The analog input voltage ($X_{(t)}$) and the output of the 1-bit digital-to-analog converter (DAC) are differentiated, providing an analog voltage ($X_2$) at the input of the first integrator or modulator stage. The output of the first integrator is further differentiated with the DAC output; the resulting voltage ($X_3$) feeds the input of the second integrator stage. When the value of the integrated signal ($X_4$) at the output of the second stage equals the comparator reference voltage, the output of the comparator switches from high to low, or vice versa, depending on its previous state. In this case, the 1-bit DAC responds on the next clock pulse by changing its analog output voltage ($X_6$), causing the integrators to progress in the opposite direction, while forcing the value of the integrator output to track the average of the input.

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## Feature Description (continued)

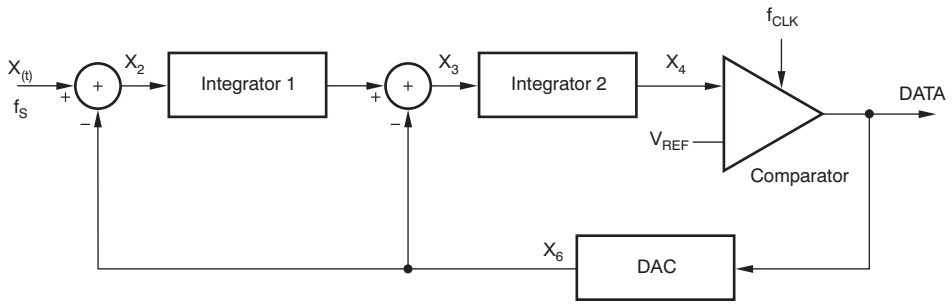



**Figure 45. Block Diagram Of A Second-Order Modulator**

The modulator shifts the quantization noise to high frequencies, as shown in Figure 46; therefore, a low-pass digital filter should be used at the output of the device to increase the overall performance. This filter is also used to convert from the 1-bit data stream at a high sampling rate into a higher-bit data word at a lower rate (decimation). A digital signal processor (DSP), microcontroller (µC), or field programmable gate array (FPGA) can be used to implement the filter.

TI's microcontroller family TMS320F28x7x offers a suitable programmable, hardwired filter structure termed a *sigma-delta filter module* (SDFM) optimized for usage with the AMC1204, AMC1304 and AMC1305 devices. Also, the SD24_B converters on the MSP430F677x microcontrollers offer a path to directly access the integrated sinc-filters, thus offering a system-level solution for multichannel isolated current sensing. Another option is to use a suitable application-specific device such as the AMC1210, a four-channel digital sinc-filter.

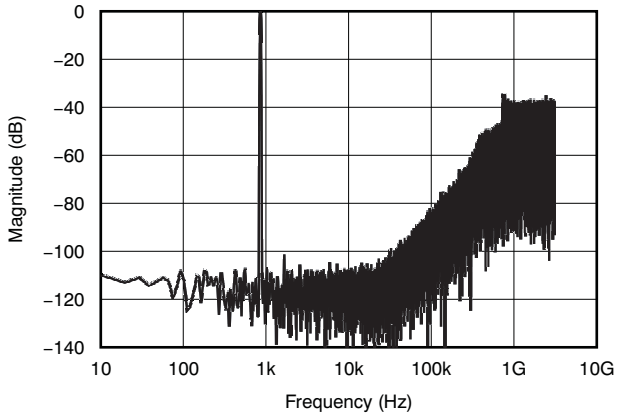



**Figure 46. Quantization Noise Shaping**


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## Feature Description (continued)

### 8.3.3 Digital Output

A differential input signal of 0 V ideally produces a stream of ones and zeros that are high 50% of the time and low 50% of the time. A differential input of 250 mV produces a stream of ones and zeros that are high 89.06% of the time. A differential input of –250 mV produces a stream of ones and zeros that are high 10.94% of the time. This is also the specified linear input range of the modulator with the performance as specified in this data sheet. The range between 250 mV and 320 mV (absolute values) is the non-linear range of the modulator. The output of the modulator clips with a stream of only zeros with an input less than or equal to –320 mV or with a stream of only ones with an input greater than or equal to 320 mV. The input voltage versus the output modulator signal is shown in Figure 47.

The system clock of the AMC1204 and AMC1204B is typically 20 MHz and is provided externally at the CLKIN pin. The data are synchronously provided at 20 MHz at the DATA output pin. The data are changing at the falling edge of CLKIN; for more details see the *Timing Requirements* section.

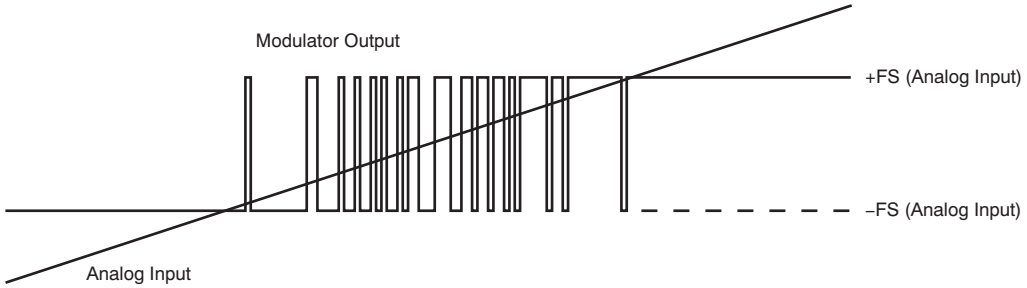



**Figure 47. Analog Input Versus Amc1204 Modulator Output**

## 8.4 Device Functional Modes

The AMC1204 is operational when the power supplies AVDD and DVDD are applied as specified in the *Recommended Operating Conditions* section.

The AMC1204 has no additional functional modes.

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# 9 Application and Implementation

**NOTE**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

## 9.1 Application Information

### 9.1.1 Digital Filter Usage

The modulator generates a bit stream that is processed by a digital filter to obtain a digital word similar to a conversion result of a conventional analog-to-digital converter (ADC). A very simple filter, built with minimal effort and hardware, is a sinc$^3$-type filter, as shown in Equation 1:

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}}\right)^3 \quad (1)$$

This filter provides the best output performance at the lowest hardware size (count of digital gates). For an oversampling rate (OSR) in the range of 16 to 256, this filter is a good choice. All the characterization in this document is also done with a sinc$^3$ filter with OSR = 256 and an output word width of 16 bits.

In a sinc$^3$ filter response (shown in Figure 48 and Figure 49), the location of the first notch occurs at the frequency of output data rate $f_{DATA} = f_{CLK}/OSR$. The –3-dB point is located at half the Nyquist frequency or $f_{DATA}/4$. For some applications, it may be necessary to use another filter type with different frequency response. Performance can be improved, for example, by using a cascaded filter structure. The first decimation stage could be built of a sinc$^3$ filter with a low OSR and the second stage using a high-order filter.

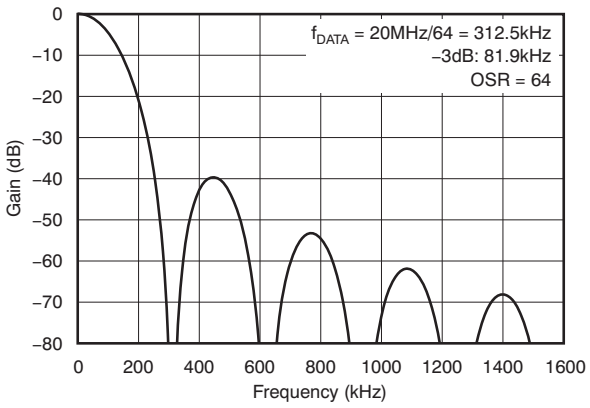



**Figure 48. Frequency Response Of The Sinc$^3$ Filter**

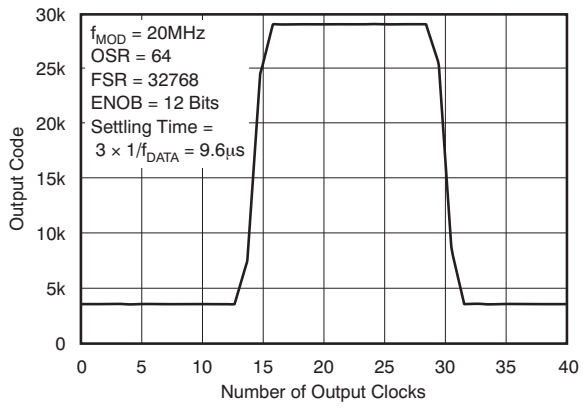



**Figure 49. Pole Response Of The Sinc$^3$ Filter**

The effective number of bits (ENOB) is often used to compare the performance of ADCs and ΔΣ modulators. Figure 51 illustrates the ENOB of the AMC1204 and AMC1204B with different oversampling ratios. In this data sheet, this number is calculated from SNR using Equation 2:

$$SNR = 1.76dB + 6.02dB \times ENOB \quad (2)$$

An example code for an implementation of a sinc$^3$ filter in an FPGA follows. For more information, see the *Combining ADS1202 with FPGA Digital Filter for Current Measurement in Motor Control Applications* application note, available for download at www.ti.com.


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## Application Information (continued)

```
library IEEE;
use IEEE.std_logic_1164.all;
use IEEE.std_logic_unsigned.all;

entity FLT is
  port(RESN, MOUT, MCLK, CNR : in std_logic;
       CN5 : out std_logic_vector(23 downto 0));
end FLT;

architecture RTL of FLT is
  signal DN0, DN1, DN3, DN5 : std_logic_vector(23 downto 0);
  signal CN1, CN2, CN3, CN4 : std_logic_vector(23 downto 0);
  signal DELTA1 : std_logic_vector(23 downto 0);
begin

process(MCLK, RESn)
  begin
    if RESn = '0' then
      DELTA1 <= (others => '0');
    elsif MCLK'event and MCLK = '1' then
      if MOUT = '1' then
        DELTA1 <= DELTA1 + 1;
      end if;
    end if;
  end process;

process(RESN, MCLK)
  begin
    if RESN = '0' then
      CN1 <= (others => '0');
      CN2 <= (others => '0');
    elsif MCLK'event and MCLK = '1' then
      CN1 <= CN1 + DELTA1;
      CN2 <= CN2 + CN1;
    end if;
  end process;

process(RESN, CNR)
  begin
    if RESN = '0' then
      DN0 <= (others => '0');
      DN1 <= (others => '0');
      DN3 <= (others => '0');
      DN5 <= (others => '0');
    elsif CNR'event and CNR = '1' then
      DN0 <= CN2;
      DN1 <= DN0;
      DN3 <= CN3;
      DN5 <= CN4;
    end if;
  end process;

CN3 <= DN0 - DN1;
CN4 <= CN3 - DN3;
CN5 <= CN4 - DN5;

end RTL;
```

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## 9.2 Typical Application

### 9.2.1 Frequency Inverter Application

Because of their high AC and DC performance, isolated ΔΣ modulators are being widely used in new generation frequency inverter designs. Frequency inverters are critical parts of industrial motor drives, photovoltaic inverters (string and central inverters), uninterruptible power supplies (UPS), electrical and hybrid vehicles, and other industrial applications. The input structure of the AMC1204 is optimized for use with low-impedance shunt resistors and is therefore tailored for isolated current sensing using shunts.

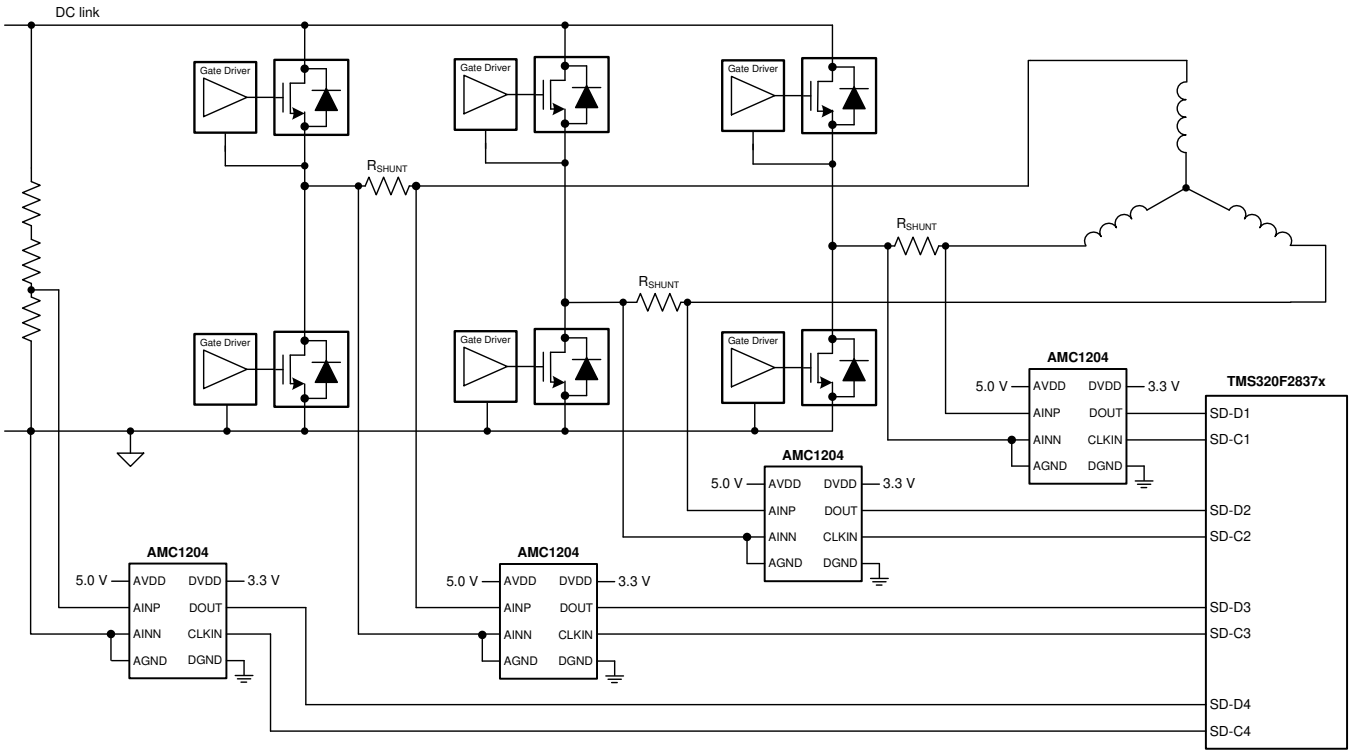



**Figure 50. AMC1204 in a Frequency Inverter Application**

#### *9.2.1.1 Design Requirements*

Figure 50 shows a diagram of the AMC1204 in a typical frequency inverter. When the inverter stage is part of a motor drive system, measurement of the motor phase current is done via the shunt resistors ($R_{SHUNT}$). Depending on the system design, either all three or only two phase currents are sensed.

In this example, an additional AMC1204 is used for isolated sensing of the DC link voltage. This high DC link voltage is reduced using a high-impedance resistive divider before being sensed by the AMC1204 across a smaller resistor. It is important to consider that the value of the resistor in the voltage divider can potentially degrade the performance of the measurement. Such phenomenon is described in the *Isolated Voltage Sensing* section.

#### *9.2.1.2 Detailed Design Procedure*

For modulator output bit-stream filtering, TI recommends a device from TI's TMS320F28x7x family of MCUs. This family supports up to eight channels of dedicated hardwired filter structures that significantly simplify system level design by offering two filtering paths per channel: one providing high accuracy results for the control loop and one fast response path for overcurrent detection.


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## Typical Application (continued)

### 9.2.1.3 Application Curves

In motor control applications, a very fast response time for overcurrent detection is required. The time for fully settling the filter in case of a step-signal at the input of the modulator depends on its order; that is, a $sinc^3$ filter requires three data updates for full settling (with $f_{DATA} = f_{CLK} / OSR$). Therefore, for overcurrent protection, filter types other than $sinc^3$ might be better choices. An alternative is, for example, the $sinc^2$ filter. Figure 52 compares the settling times of different filter orders.

Sincfast is a modified $sinc^2$ filter whose transfer function follows Equation 3.

$$H(z) = \left(\frac{1 - z^{-OSR}}{1 - z^{-1}}\right)^2 (1 + z^{-2OSR}) \quad (3)$$

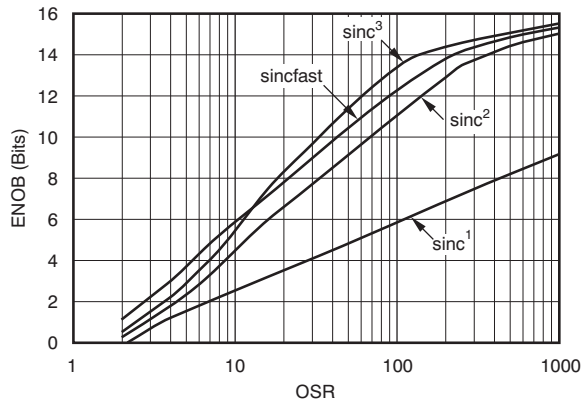



**Figure 51. Measured Effective Number Of Bits Versus Oversampling Ratio**

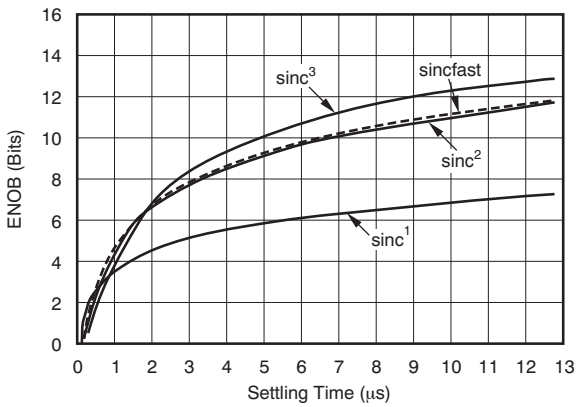



**Figure 52. Measured Effective Number of Bits Versus Settling Time**

In the case of a continuous signal fed into a sinc filter, the time delay for such signal corresponds to half of the settling time shown in Figure 52.

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## Typical Application (continued)

### 9.2.2 Example of a Resolver-Based Motor Control Analog Front End

Figure 53 shows an example of two AMC1204 and AMC1204B devices and one ADS1209 (a dual-channel, 10-MHz, non-isolated modulator) connected to an AMC1210, building the entire analog front end of a resolver-based motor control application.

For detailed information on the ADS1209 and AMC1210, visit the respective device product folders at www.ti.com.

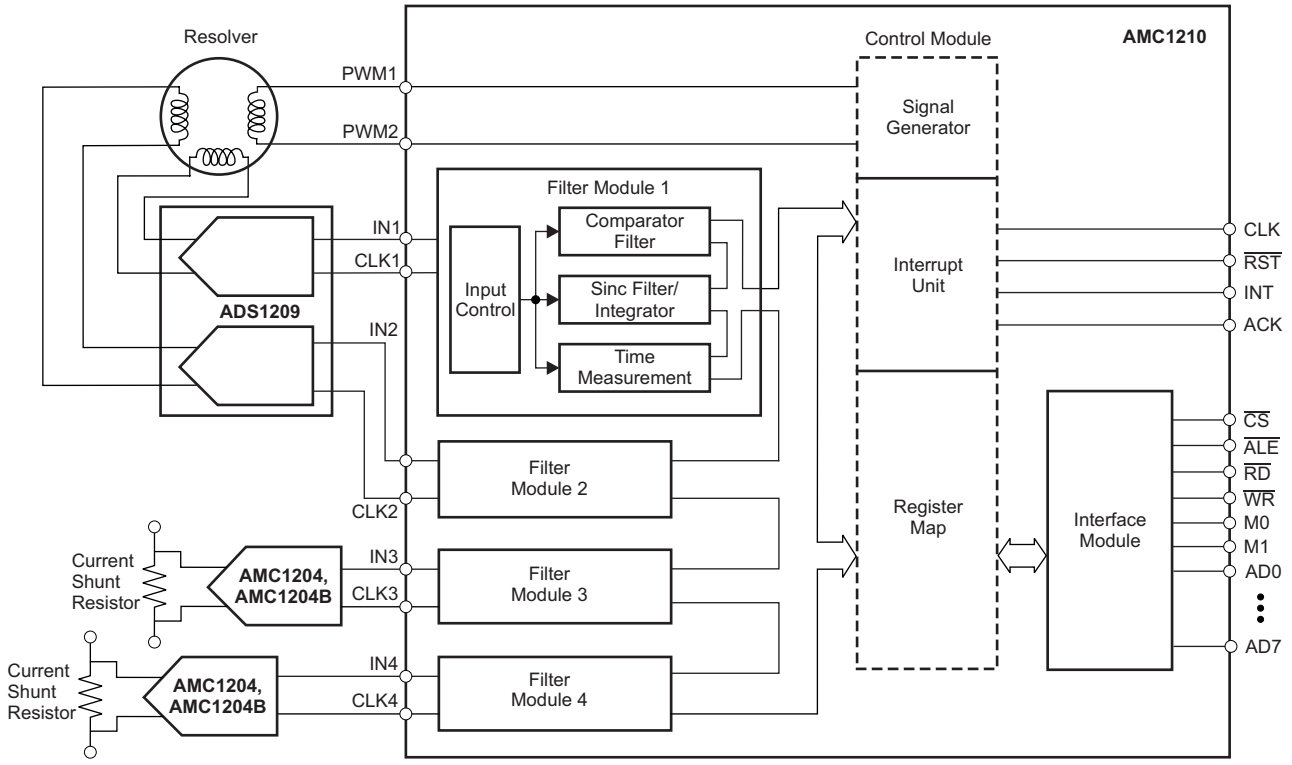



**Figure 53. Example of a Resolver-Based Motor Control Analog Front End Schematic**

### 9.2.3 Isolated Voltage Sensing

The AMC1204 is optimized for current-sensing applications using low-impedance shunts. However, the device can also be used in isolated voltage-sensing applications if the impact of the (usually higher) impedance of the resistor used in this case is considered. Figure 54 shows a simplified circuit typically used in high-voltage sensing applications.

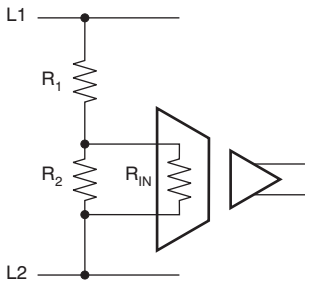



**Figure 54. Voltage Measurement Application**


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## Typical Application (continued)

### 9.2.3.1 Design Requirements

In such applications, a resistor divider ($R_1$ and $R_2$) is used to match the relatively small input voltage range of the AMC device. $R_2$ and the input resistance $R_{IN}$ of the AMC1204 also create a resistor divider resulting in additional gain error. With the assumption that $R_1$ and $R_{IN}$ have a considerably higher value than $R_2$, use Equation 4 to estimate the resulting total gain error.

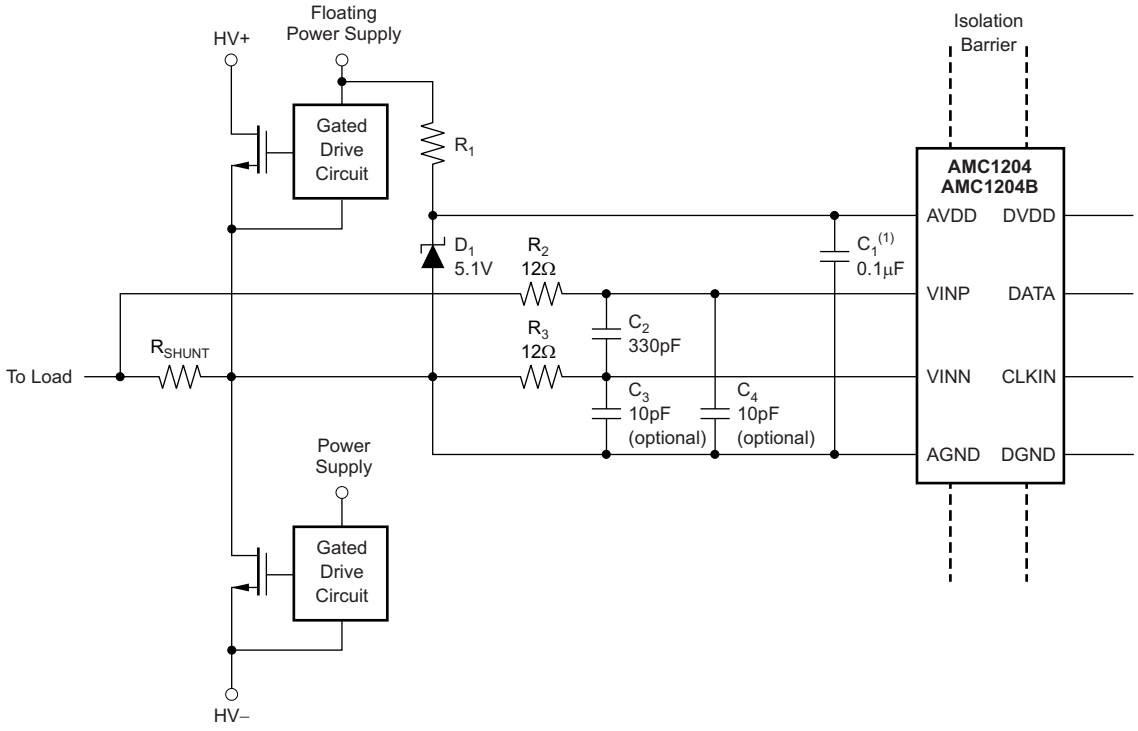
$$G_{ERRTOT} = G_{ERR} + \frac{R_2}{R_{IN}} \quad (4)$$

where

- $G_{ERR}$ = the gain error of AMC device.

## 10 Power Supply Recommendations

In a typical frequency inverter application, the high-side power supply (AVDD) for the AMC1204 and AMC1204B is derived from the power supply of the upper gate driver. For lowest cost, a Zener diode can be used to limit the voltage to 5 V ±10%. TI recommends a decoupling capacitor of 0.1 µF for filtering this power-supply path. This capacitor ($C_1$ in Figure 55) should be placed as close as possible to the AVDD pin for best performance. If better filtering is required, an additional 1-µF to 10-µF capacitor can be used. The floating ground reference AGND is derived from the end of the shunt resistor, which is connected to the negative input (VINN) of the AMC1204 and AMC1204B. If a four-terminal shunt is used, the inputs of AMC1204 and AMC1204B are connected to the inner leads, while AGND is connected to one of the outer leads of the shunt. Both digital signals, CLKIN and DATA, can be directly connected to a digital filter.




(1) Place $C_1$ close to the AMC1204 and AMC1204B.

**Figure 55. Zener-Diode-Based High-Side Power Supply**

For better performance, the differential input signal is filtered using RC filters (components $R_2$, $R_3$, and $C_2$). Optionally, $C_3$ and $C_4$ can be used to reduce charge dumping from the inputs. In this case, care should be taken when choosing the quality of these capacitors: any mismatch in the capacitor values can cause a common-mode error at the input of the modulator.

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# 11 Layout

## 11.1 Layout Guidelines

- Place the decoupling capacitors for AVDD and DVDD as close as possible to the AMC1204.
- Ensure that the traces that connect the shunt resistor to the RC filter on the VINP terminal are symmetrical to and have the same length as the traces connecting to the VINN terminal.
- The top and bottom PCB layers underneath the AMC1204 must be kept free of any conductive materials in order to comply with the creepage and clearance distances shown in the section.

## 11.2 Layout Example

Figure 56 shows the recommended layout and placement of the decoupling capacitors and other components required by the AMC1204 and AMC1204B.

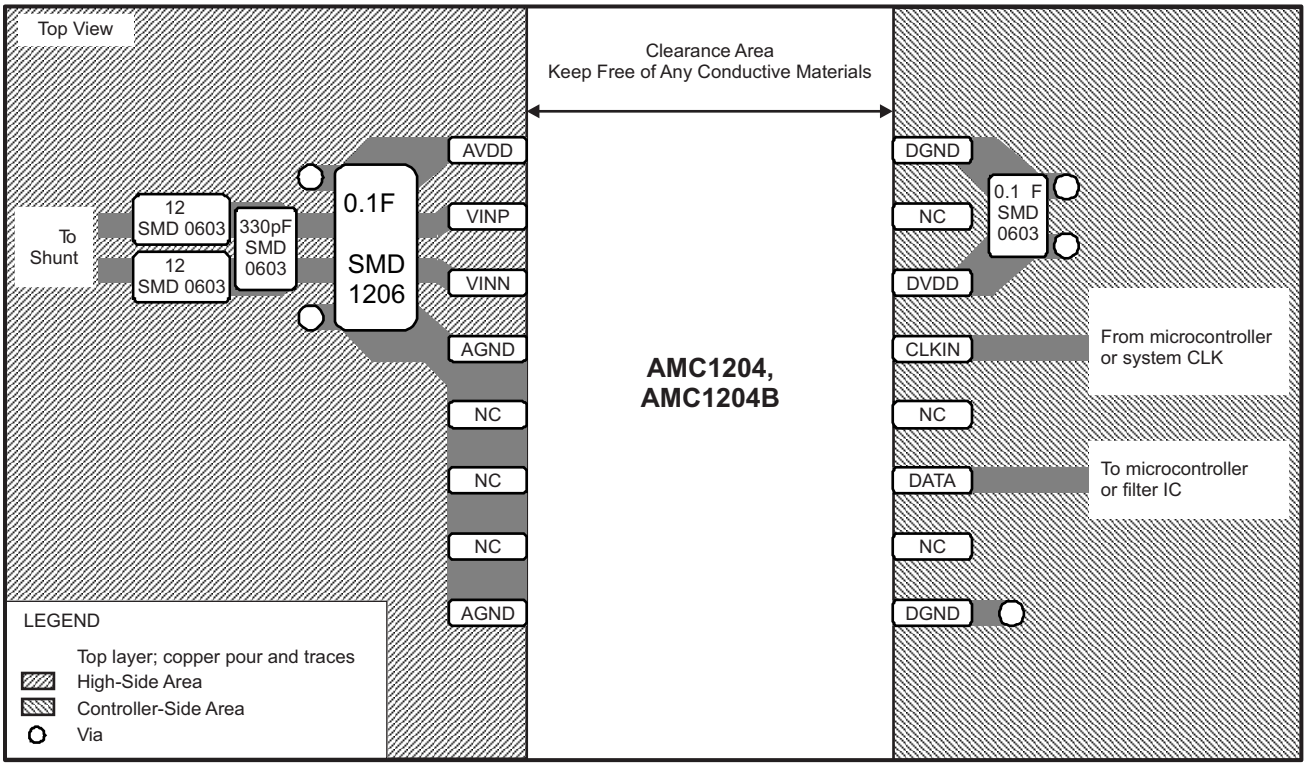



**Figure 56. Recommended Layout**


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# 12 デバイスおよびドキュメントのサポート

## 12.1 ドキュメントのサポート

### 12.1.1 関連資料

関連資料については、以下を参照してください。

- テキサス・インスツルメンツ、『TMS320F2837xD デュアル・コアDelfino™ マイクロコントローラ』データシート
- テキサス・インスツルメンツ、『MSP430F677x、MSP430F676x、MSP430F674x 多相メータリング SoC』データシート
- テキサス・インスツルメンツ、『TMS320F2837xD デュアル・コアDelfino™ マイクロコントローラ』データシート
- テキサス・インスツルメンツ、『AMC1210 2次デルタ-シグマ変調器用のクワッド・デジタル・フィルタ』データシート
- テキサス・インスツルメンツ、『ADS1209 Two 1-Bit, 10MHz, 2nd-Order Delta-Sigma Modulators』データシート (英語)
- テキサス・インスツルメンツ、『ISO72x デジタルアイソレータ磁界耐性』アプリケーション・レポート
- テキサス・インスツルメンツ、『Combining the ADS1202 with an FPGA Digital Filter for Current Measurement in Motor Control Applications』アプリケーション・レポート (英語)
- テキサス・インスツルメンツ、『絶縁の用語集』アプリケーション・レポート

## 12.2 ドキュメントの更新通知を受け取る方法

ドキュメントの更新についての通知を受け取るには、ti.comのデバイス製品フォルダを開いてください。右上の「アラートを受け取る」をクリックして登録すると、変更されたすべての製品情報に関するダイジェストを毎週受け取れます。変更の詳細については、修正されたドキュメントに含まれている改訂履歴をご覧ください。

## 12.3 サポート・リソース

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 12.5 静電気放電に関する注意事項

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静電気放電はわずかな性能の低下から完全なデバイスの故障に至るまで、様々な損傷を与えます。高精度の集積回路は、損傷に対して敏感であり、極めてわずかなパラメータの変化により、デバイスに規定された仕様に適合しなくなる場合があります。

## 12.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 13 メカニカル、パッケージ、および注文情報

以降のページには、メカニカル、パッケージ、および注文に関する情報が記載されています。この情報は、そのデバイスについて利用可能な最新のデータです。このデータは予告なく変更されることがあり、ドキュメントが改訂される場合もあります。本データシートのブラウザ版を使用されている場合は、画面左側の説明をご覧ください。

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## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| AMC1204BDW | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 1204B | Samples |
| AMC1204BDWR | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | 1204B | Samples |
| AMC1204BDWV | ACTIVE | SOIC | DWV | 8 | 64 | RoHS & Green | SN | Level-3-260C-168 HR | -40 to 125 | AMC1204B | Samples |
| AMC1204BDWVR | ACTIVE | SOIC | DWV | 8 | 1000 | RoHS & Green | Call TI \| SN | Level-3-260C-168 HR | -40 to 125 | AMC1204B | Samples |
| AMC1204DW | ACTIVE | SOIC | DW | 16 | 40 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | AMC1204 | Samples |
| AMC1204DWR | ACTIVE | SOIC | DW | 16 | 2000 | RoHS & Green | NIPDAU | Level-3-260C-168 HR | -40 to 125 | AMC1204 | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF AMC1204 :**

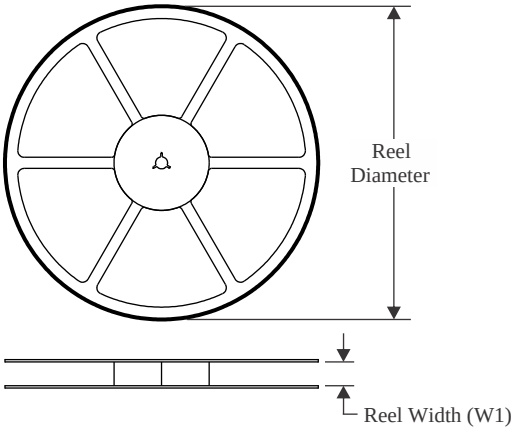
- Automotive : AMC1204-Q1

NOTE: Qualified Version Definitions:

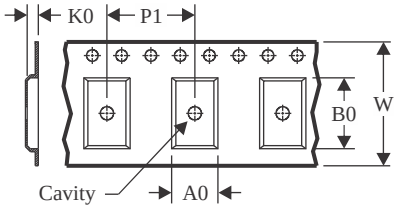
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

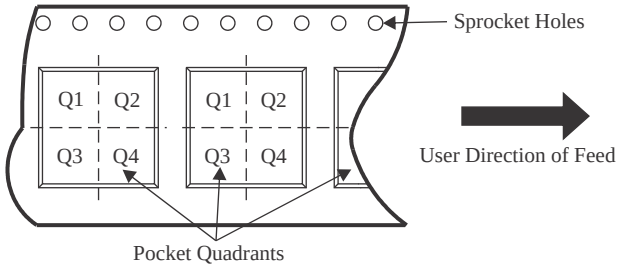



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

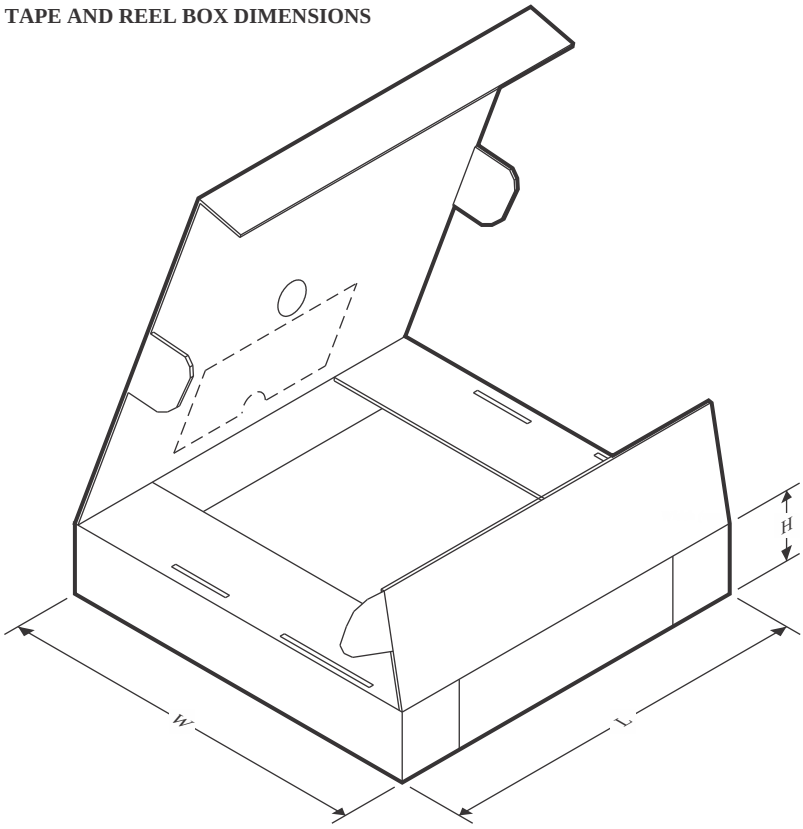
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| AMC1204BDWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |
| AMC1204BDWVR | SOIC | DWV | 8 | 1000 | 330.0 | 16.4 | 12.05 | 6.15 | 3.3 | 16.0 | 16.0 | Q1 |
| AMC1204DWR | SOIC | DW | 16 | 2000 | 330.0 | 16.4 | 10.75 | 10.7 | 2.7 | 12.0 | 16.0 | Q1 |

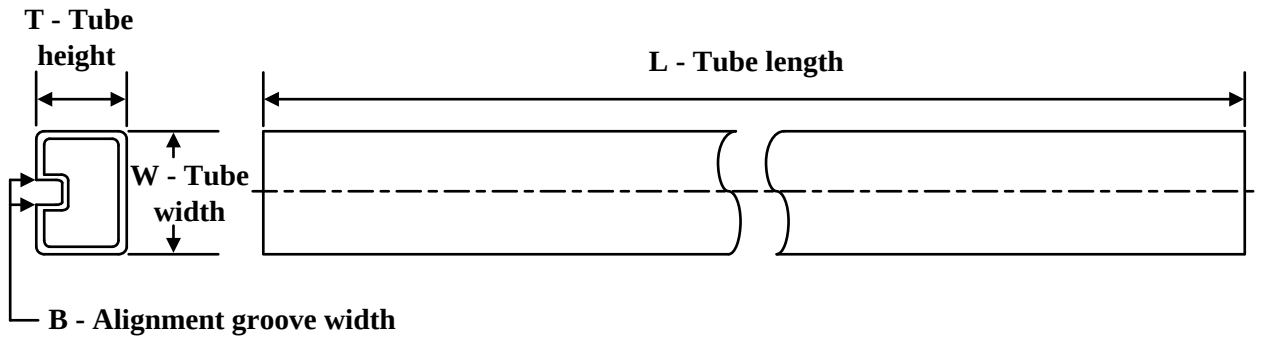
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| AMC1204BDWR | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |
| AMC1204BDWVR | SOIC | DWV | 8 | 1000 | 350.0 | 350.0 | 43.0 |
| AMC1204DWR | SOIC | DW | 16 | 2000 | 356.0 | 356.0 | 35.0 |

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| AMC1204BDW | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| AMC1204BDW | DW | SOIC | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |
| AMC1204BDWV | DWV | SOIC | 8 | 64 | 505.46 | 13.94 | 4826 | 6.6 |
| AMC1204DW | DW | SOIC | 16 | 40 | 507 | 12.83 | 5080 | 6.6 |
| AMC1204DW | DW | SOIC | 16 | 40 | 506.98 | 12.7 | 4826 | 6.6 |

# GENERIC PACKAGE VIEW

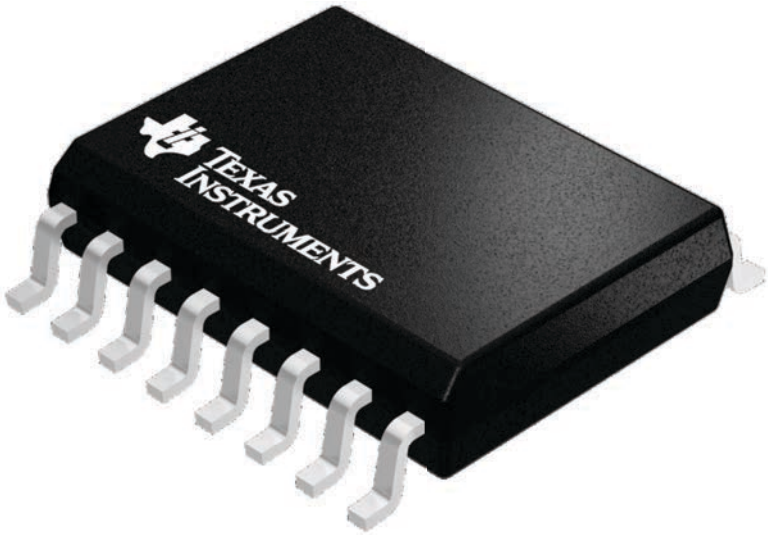
## DW 16

## SOIC - 2.65 mm max height

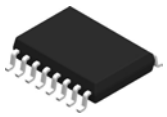
**7.5 x 10.3, 1.27 mm pitch**

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.




4224780/A

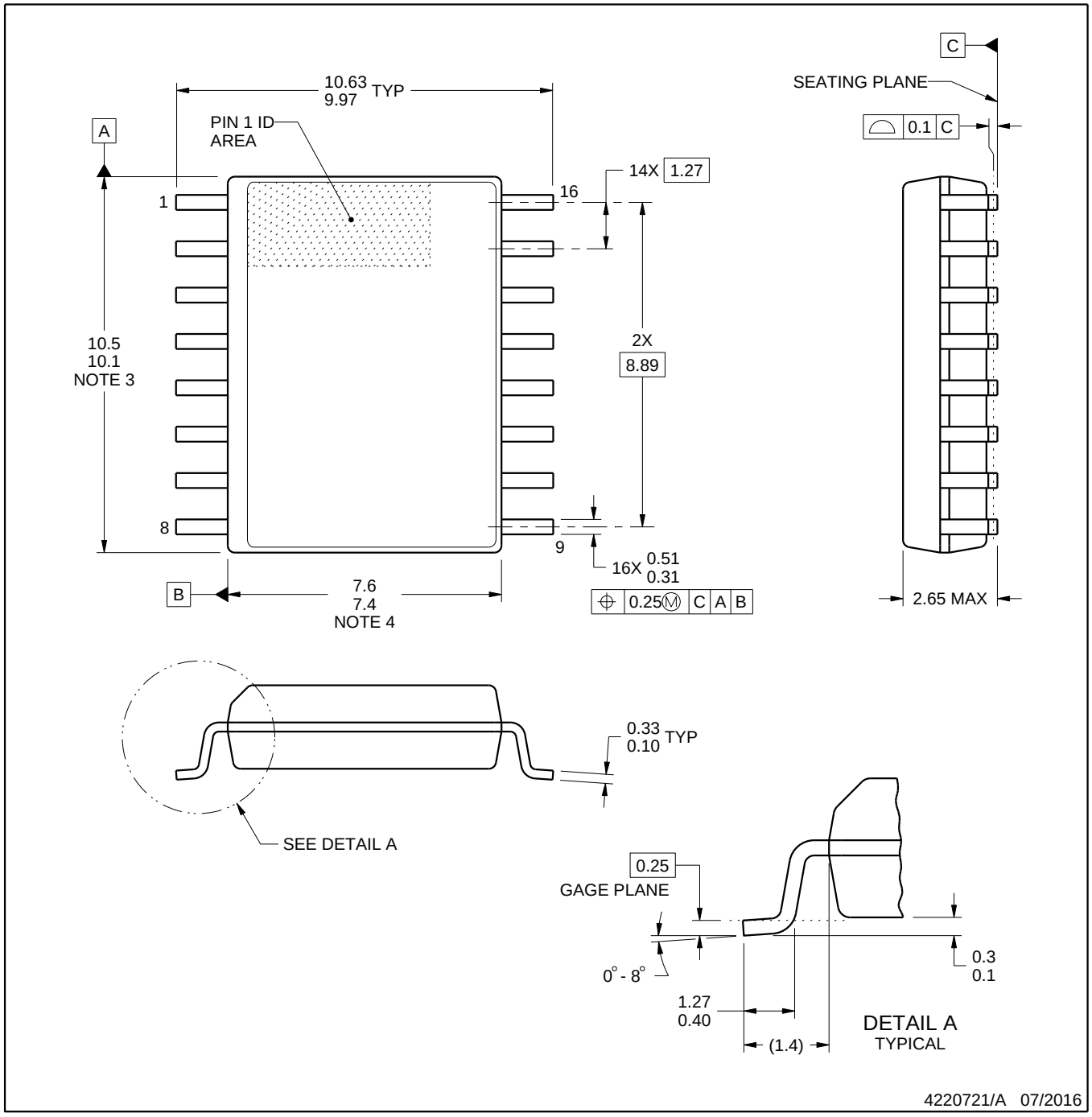


# PACKAGE OUTLINE

## DW0016A

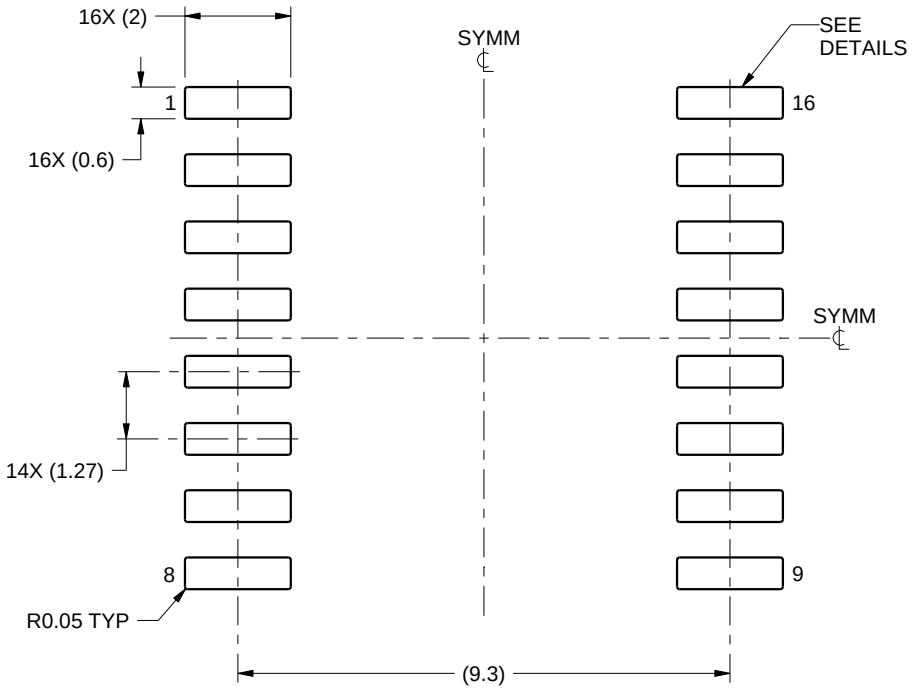
## SOIC - 2.65 mm max height

SOIC

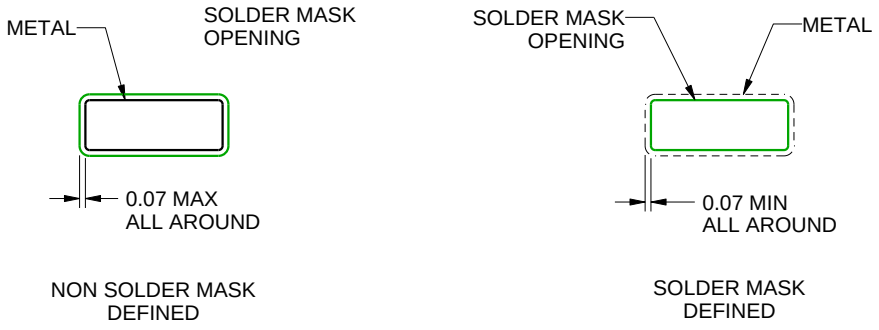



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:7X

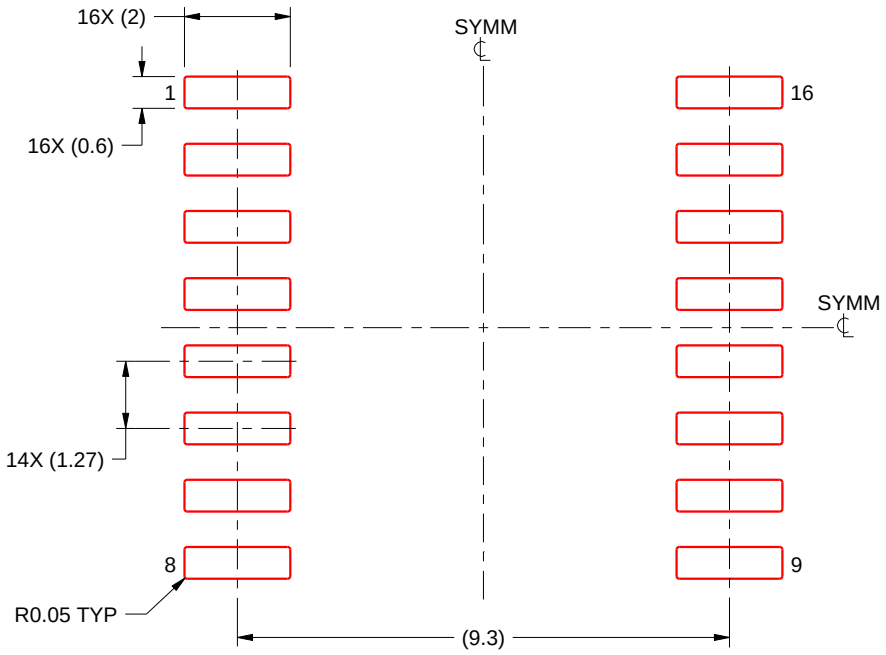



SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



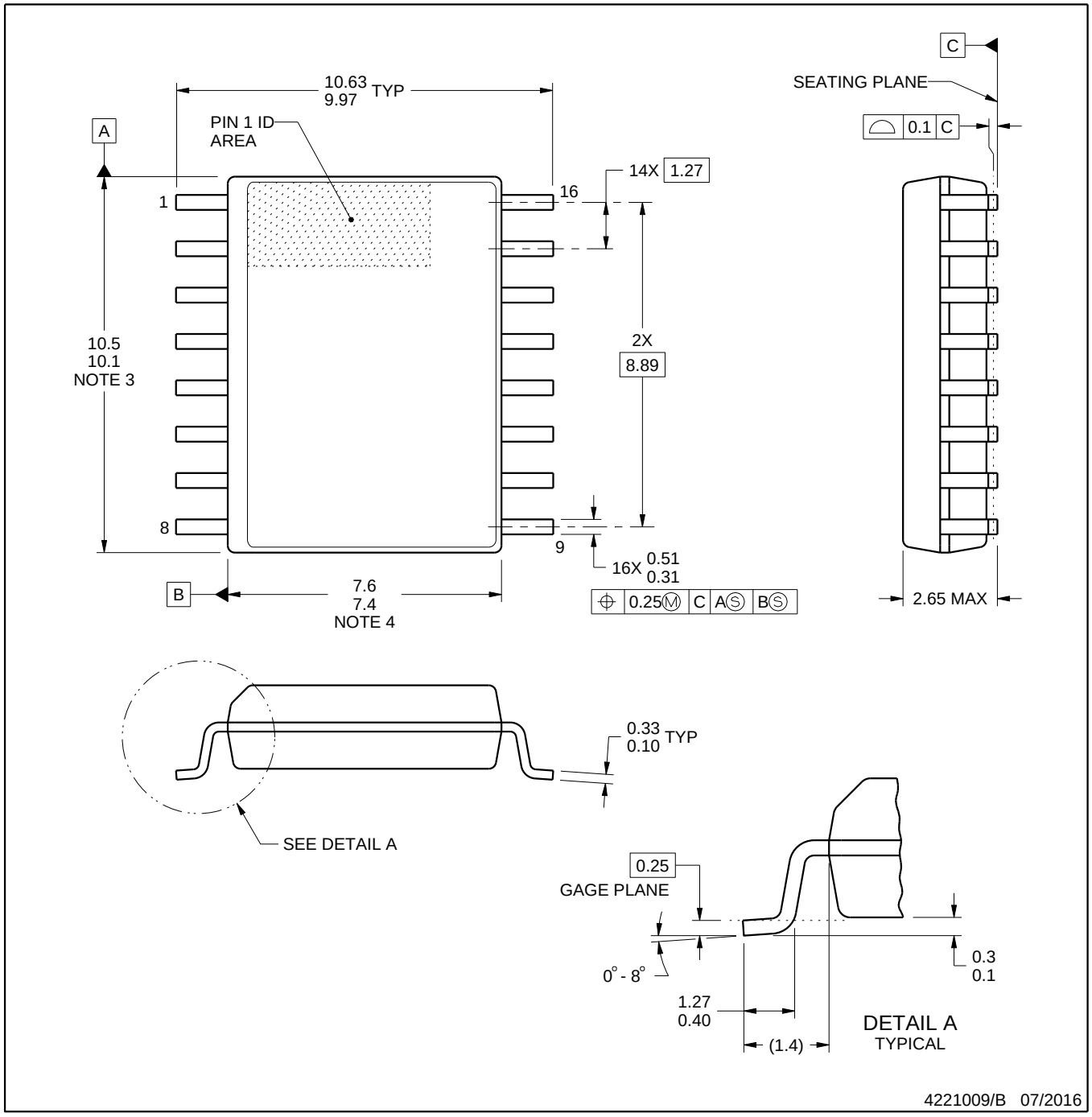

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

NOTES: (continued)

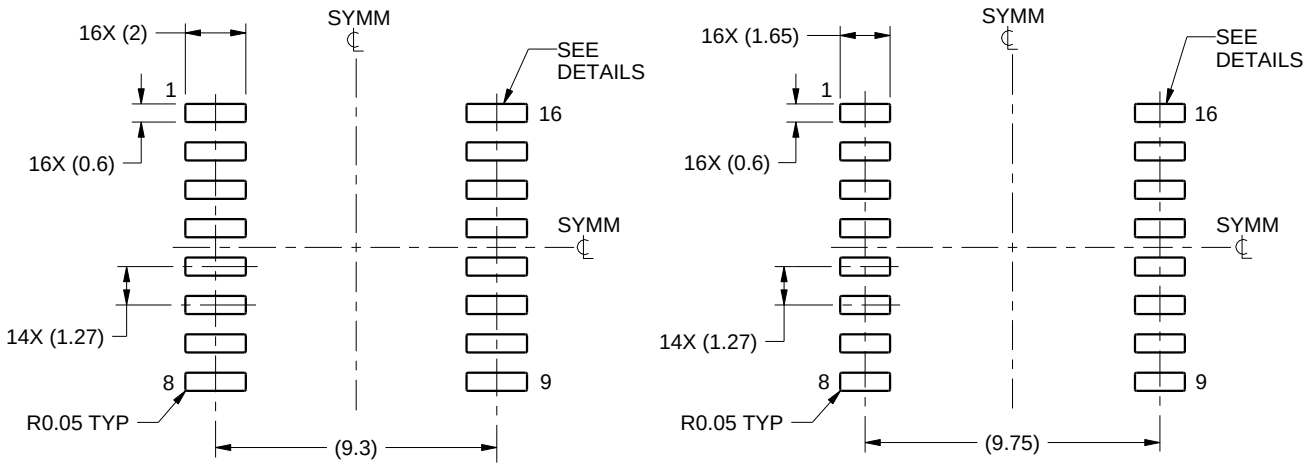
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

SOIC




NOTES:

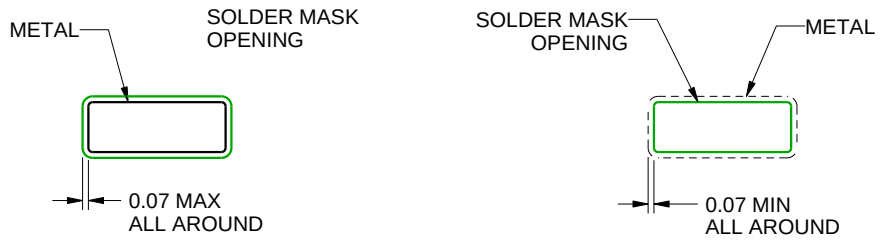
1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.




IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

LAND PATTERN EXAMPLE
SCALE:4X




NON SOLDER MASK DEFINED

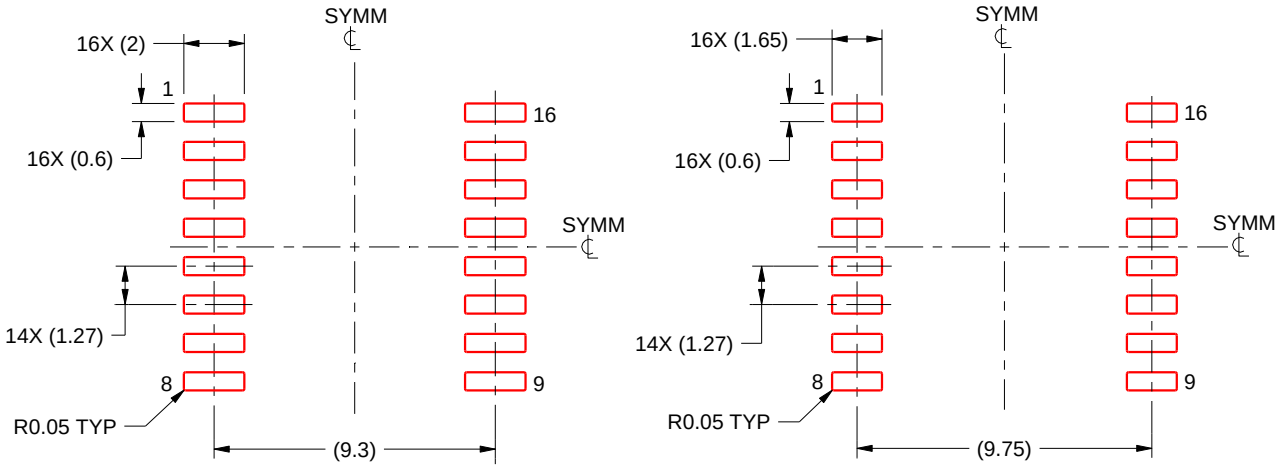
SOLDER MASK DEFINED

SOLDER MASK DETAILS

4221009/B 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




IPC-7351 NOMINAL
7.3 mm CLEARANCE/CREEPAGE

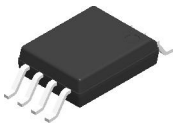
HV / ISOLATION OPTION
8.1 mm CLEARANCE/CREEPAGE

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:4X

4221009/B 07/2016

NOTES: (continued)

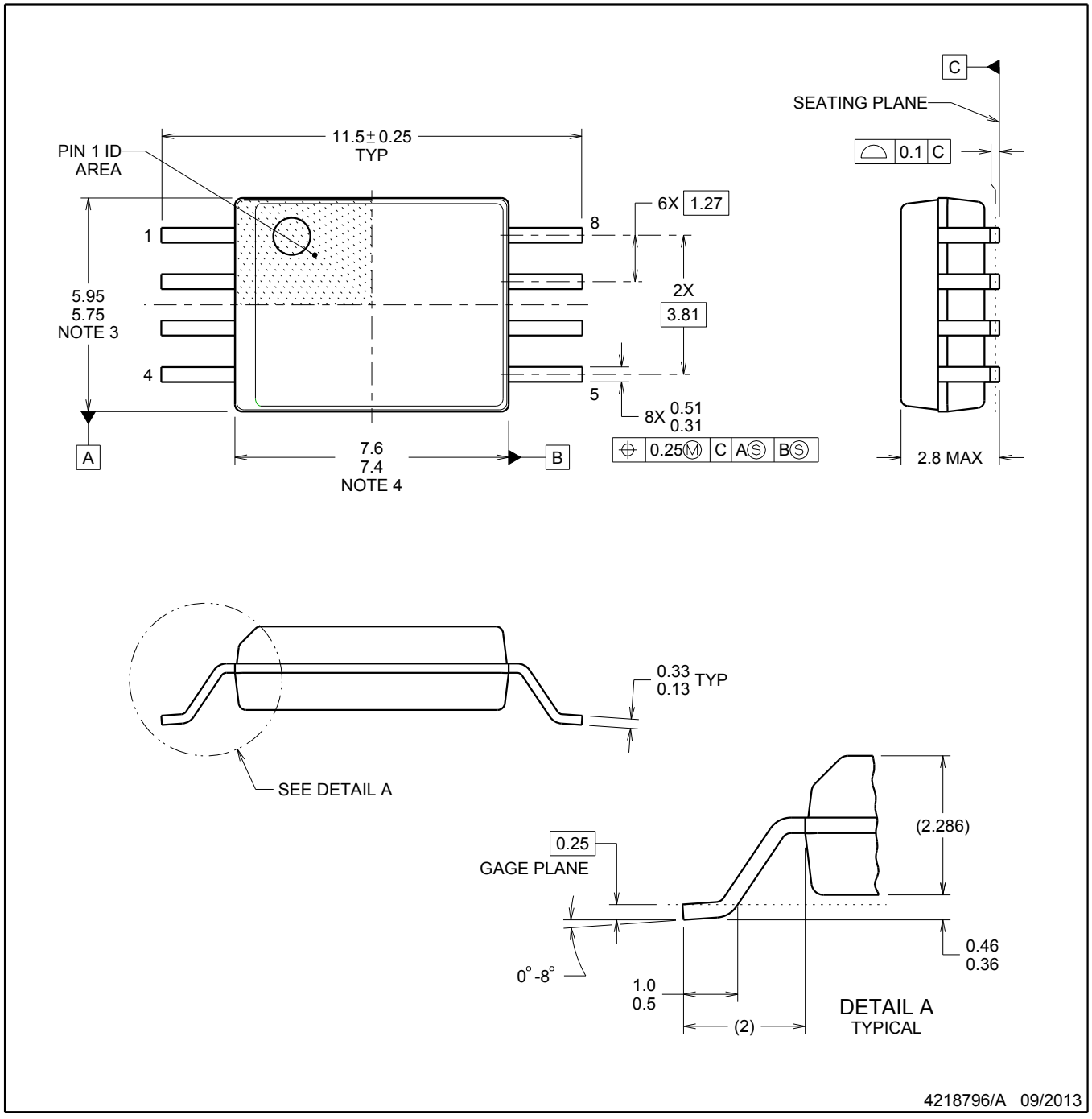
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.



# DWV0008A

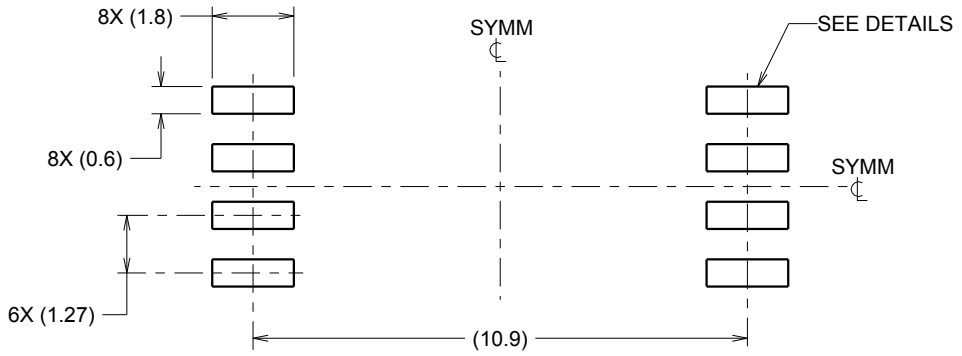
## SOIC - 2.8 mm max height

SOIC

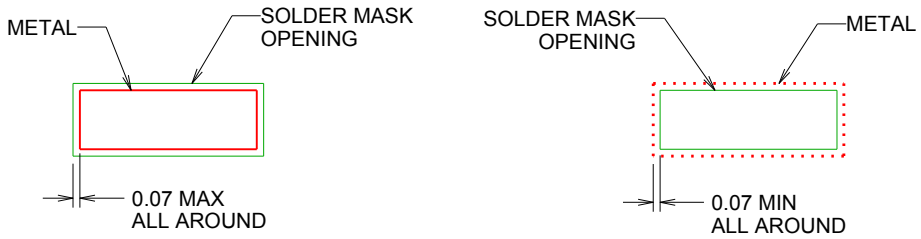



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.




LAND PATTERN EXAMPLE
9.1 mm NOMINAL CLEARANCE/CREEPAGE
SCALE:6X




SOLDER MASK DETAILS

4218796/A 09/2013

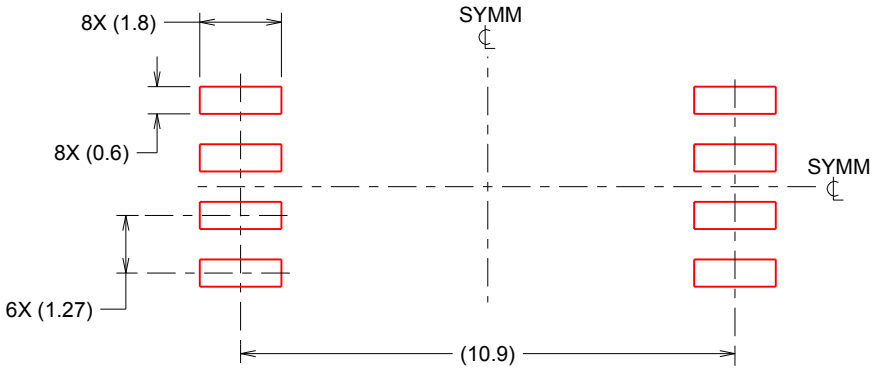
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

DWV0008A

SOIC - 2.8 mm max height

SOIC




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4218796/A 09/2013

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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