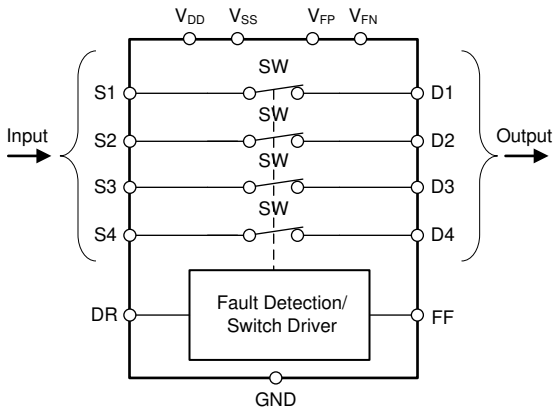
TMUX7462F ±60V、フォルト保護、ラッチアップ・フリー、クワッド・チャネル・プロテクタ、可変フォルト・スレッショルドおよび 1.8V ロジック付き

1 特長

- 広い電源電圧範囲:8V～44V シングル電源
  ±5V～±22V デュアル電源
- チャネルごとの専用選択ピンを必要としないチャネル・プロテクタ
  - PCB 全体で配線すべき制御ロジック信号数を低減
- フォルト保護機能を搭載:
  - 過電圧保護、ソース - 電源間またはソース - ドレイン間:±85V
  - 過電圧保護:±60V
  - 電源オフ保護:±60V
  - フォルト状態を示す割り込みフラグ
  - 調整可能な過電圧トリガ・スレッショルド
    - V_{FP}:3V～V_{DD}、V_{FN}:0V～V_{SS}
  - フォルト時の出力動作 (クランプまたはオープン) を調整可能
- デバイス構造に基づくラッチアップ耐性
- 人体モデル (HBM) ESD 定格:6kV
- 低オン抵抗:8.3Ω (標準値)
- フラットなオン抵抗:5mΩ (標準値)
- 業界標準の TSSOP と小型の WQFN パッケージ

2 アプリケーション

- ファクトリ・オートメーション / 制御
- プログラマブル・ロジック・コントローラ (PLC)
- アナログ入力モジュール
- 半導体試験用機器
- バッテリ試験装置
- サーボ・ドライブ制御モジュール
- データ・アクイジション・システム (DAQ)



ブロック図

3 概要

TMUX7462F は、過電圧フォルトに起因する損傷から下流の敏感な部品を保護するために信号路のフロント・エンドに配置できる 4 チャネル・プロテクタです。外部から制御しなくても、過電圧フォルトが発生すると自動的にオフになる内部スイッチが 4 つのチャネルにそれぞれ備わっています。そのため、デバイスの各チャネルの制御信号が不要であり、堅牢なシステム・レベル保護機能を簡単に設計できます。電源を入れた状態でも切った状態でも過電圧保護機能を利用できるため、電源シーケンスを正確に制御できないアプリケーションにも TMUX7462F は適しています。

本デバイスの電源がフローティングである場合、接地されている場合、低電圧 (UV) スレッショルドを下回るレベルである場合のいずれでも、スイッチの入力条件にかかわらず、スイッチのチャネルは高インピーダンス状態に維持されます。通常動作時に、いずれかの Sx ピンの信号レベルがフォルト電源 (V_{FP} または V_{FN}) をスレッショルド電圧 (V_T) 分上回ると、その Sx ピンは高インピーダンスになり、出力フォルト・フラグが LOW にアサートされることでフォルト状態を示します。ドレイン・ピン (Dx) は、DR 制御ロジックに応じて、超過したフォルト電源電圧にプルされるか、フローティング状態に維持されます。

このデバイスは、デュアル電源 (±5V～±22V)、シングル電源 (8V～44V)、非対称電源のいずれでも動作します。TMUX7462F は、オン抵抗が低くフラットであるため、優れた直線性と低歪みが重要なデータ・アクイジション・アプリケーションにとって優れたソリューションになります。

パッケージ情報

部品番号	パッケージ(1)	パッケージ・サイズ (2)
TMUX7462F	PW (TSSOP、16)	5mm × 6.4mm
	RRP (WQFN、16)	4mm × 4mm

(1) 利用可能なすべてのパッケージについては、このデータシートの末尾にある注文情報を参照してください。
(2) パッケージ・サイズ (長さ×幅) は公称値であり、該当する場合はピンも含まれます。

Table of Contents

4 Revision History

資料番号末尾の英字は改訂を表しています。その改訂履歴は英語版に準じています。

Changes from Revision A (October 2021) to Revision B (November 2022) — **Page**

- PW パッケージのステータスをプレビューからアクティブに変更 ... 1
- 「パッケージ情報」表のフォーマットを更新し、パッケージ・リードを追加 ... 1

Changes from Revision * (March 2021) to Revision A (October 2021) — **Page**

- データシートのステータスを*事前情報*から*量産データ*に変更 ... 1

5 Pin Configuration and Functions

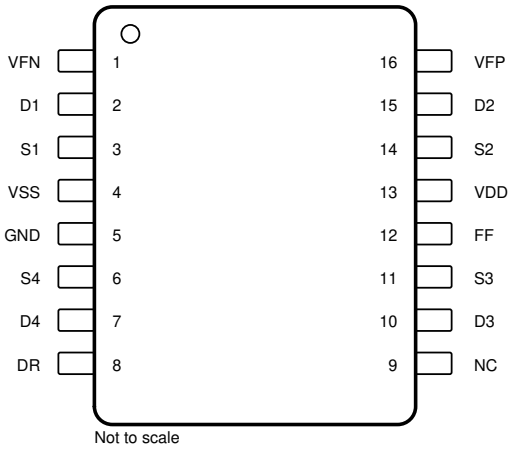


図 5-1. PW Package, 16-Pin TSSOP (Top View)

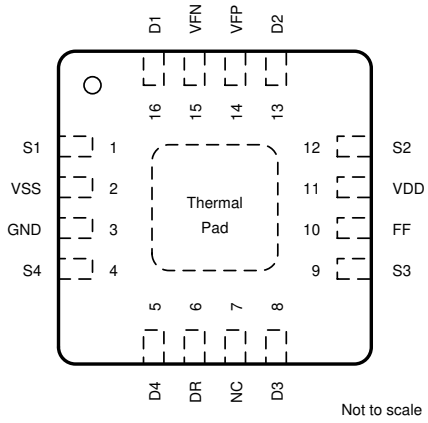


図 5-2. RRP Package, 16-Pin WQFN (Top View)

表 5-1. Pin Functions

PIN			TYPE(1)	DESCRIPTION
NAME	TSSOP	WQFN		
D1	2	16	I/O	Drain pin 1 can be an input or output. The drain pin is not overvoltage protected and shall remain within the recommended operating range.
D2	15	13	I/O	Drain pin 2 can be an input or output. The drain pin is not overvoltage protected and shall remain within the recommended operating range.
D3	10	8	I/O	Drain pin 3 can be an input or output. The drain pin is not overvoltage protected and shall remain within the recommended operating range.
D4	7	5	I/O	Drain pin 4 can be an input or output. The drain pin is not overvoltage protected and shall remain within the recommended operating range.
DR	8	6	I	Drain Response (DR) input. Tying the DR pin to GND enables the drain to be pulled to V_{FP} or V_{FN} through a 40 kΩ resistor during an overvoltage fault event. The drain pin becomes open circuit when the DR pin is a logic high or left floating.
FF	12	10	O	General fault flag. This pin is an open drain output and is asserted low when overvoltage condition is detected on any of the source (Sx) pins. Connect this pin to an external supply (1.8 V to 5.5 V) through a 1 kΩ pull-up resistor.
GND	5	3	P	Ground (0 V) reference.
N.C.	9	7	—	No internal connection
S1	3	1	I/O	Overvoltage protected source pin 1 can be an input or output.
S2	14	12	I/O	Overvoltage protected source pin 2 can be an input or output.
S3	11	9	I/O	Overvoltage protected source pin 3 can be an input or output.
S4	6	4	I/O	Overvoltage protected source pin 4 can be an input or output.
V_{DD}	13	11	P	Positive power supply. This pin is the most positive power-supply potential. Connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{DD} and GND for reliable operation.
V_{FP}	16	14	P	Positive fault voltage supply that determines the overvoltage protection triggering threshold on the positive side. Connect to V_{DD} if the triggering threshold is the same as the device's positive supply. Connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{FP} and GND for reliable operation.
V_{FN}	1	15	P	Negative fault voltage supply that determines the overvoltage protection triggering threshold on the negative side. Connect to V_{SS} if the triggering threshold is the same as the device's negative supply. Connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{FN} and GND for reliable operation.
V_{SS}	4	2	P	Negative power supply. This pin is the most negative power-supply potential. This pin can be connected to ground in single-supply applications. Connect a decoupling capacitor ranging from 0.1 µF to 10 µF between V_{SS} and GND for reliable operation.
Thermal Pad			—	The thermal pad is not connected internally. No requirement to solder this pad. For best performance it is recommended that the pad be tied to GND or VSS.

(1) I = input, O = output, I/O = input and output, P = power.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
V_{DD} to V_{SS}	Supply voltage		48	V
V_{DD} to GND		–0.3	48	V
V_{SS} to GND		–48	0.3	V
V_{FP} to GND	Fault clamping voltage	–0.3	V_{DD} + 0.3	V
V_{FN} to GND		VSS – 0.3	0.3	V
V_S to GND	Source input pin (Sx) voltage to GND	–65	65	V
V_S to V_{DD}	Source input pin (Sx) voltage to V_{DD} or V_D	–90		V
V_S to V_{SS}	Source input pin (Sx) voltage to V_{SS} or V_D		90	V
V_D	Drain pin (Dx) voltage	V_{FN}–0.7	V_{FP}+0.7	V
V_{DR}	Logic input pin (DR) voltage(2)	GND –0.7	48	V
V_{FF}	Logic output pin (FF) voltage(2)	GND –0.7	6	V
I_{DR}	Logic input pin (DR) current(2)	–30	30	mA
I_{FF}	Logic output pin (FF) current(2)	–10	10	mA
I_S or $I_{D\ (CONT)}$	Source or drain continuous current (Sx or Dx)	I_{DC} ± 10 %(3)	I_{DC} ± 10 %(3)	mA
T_{stg}	Storage temperature	–65	150	°C
T_A	Ambient temperature	–55	150	°C
T_J	Junction temperature		150	°C
P_{tot} (4)	Total power dissipation (QFN)		1600	mW

(1) Stresses beyond those listed under *Absolute Maximum Rating* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Condition*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Stresses have to be kept at or below both voltage and current ratings at all time.
(3) Refer to Recommended Operating Conditions for I_{DC} ratings.
(4) For QFN package: P_{tot} derates linearly above T_A = 70°C by 23.5 mW/°C

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins(1)	±6000	V
		Charged device model (CDM), per ANSI/ESDA/JEDEC JS-002, all pins(2)	±750	V

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Thermal Information

THERMAL METRIC[1]		TMUX7462F		UNIT
		PW (TSSOP)	RRP (WQFN)	
		16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	100.4	42.8	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	31.3	28.5	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	46.4	17.9	°C/W
Ψ_{JT}	Junction-to-top characterization parameter	1.7	0.3	°C/W
Ψ_{JB}	Junction-to-board characterization parameter	45.8	17.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	N/A	4.0	°C/W

(1) For more information about traditional and new thermal metrics, see the Semiconductor and IC Package Thermal Metrics application report.

6.4 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	NOM	MAX	UNIT
$V_{DD} – V_{SS}$ (1)	Power supply voltage differential		8		44	V
V_{DD}	Positive power supply voltage		5		44	
V_{FP}	Positive fault clamping voltage		3		V_{DD}	
V_{FN}	Negative fault clamping voltage		V_{SS}		0	
V_S	Source pin (Sx) voltage (non-fault condition)		V_{FN}		V_{FP}	V
V_S to GND	Source pin (Sx) voltage to GND (fault condition)		–60		60	
V_S to V_{DD} (2)	Source pin (Sx) voltage to V_{DD} or V_D (fault condition)		–85			
V_S to V_{SS} (2)	Source pin (Sx) voltage to V_{SS} or V_D (fault condition)				85	
V_D	Drain pin (Dx) voltage		V_{FN}		V_{FP}	
V_{DR}	Logic input pin (DR) voltage		GND		44	V
V_{FF} (3)	Logic output pin (FF) voltage		GND		5.5	
T_A	Ambient temperature		–40		125	°C
I_{DC}	Continuous current through switch, WQFN package	T_A = 25°C			150	mA
		T_A = 85°C			100	
		T_A = 125°C			60	

(1) V_{DD} and V_{SS} can be any value as long as 8 V ≤ (V_{DD} – V_{SS}) ≤ 44 V, and the minimum V_{DD} is met.
(2) Source pin voltage (Sx) under a fault condition may not exceed 85 V from supply pins (V_{DD} and V_{SS}.) or drain pins (D, Dx).
(3) Logic output pin (FF) is an open drain output and should be pulled up to a voltage within the max ratings

6.5 Electrical Characteristics (Global)

at T_A = 25°C (unless otherwise noted)
Typical at V_{DD} = 15 V, V_{SS} = –15 V, GND = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
V_T	Threshold voltage for fault detector		25°C		0.7		V
LOGIC INPUT/ OUTPUT							
V_{IH}	High-level input voltage	DR pin	–40°C to +125°C	1.3			V
V_{IL}	Low-level input voltage	DR pin	–40°C to +125°C			0.8	V
I_{IH}	High-level input current	V_{DR} = logic high	–40°C to +125°C		0.4	3	µA
I_{IL}	Low-level input current	V_{DR} = logic low	–40°C to +125°C	–1	–0.65		µA
$V_{OL(FLAG)}$	Low-level output voltage	FF pin, I_O = 5 mA	–40°C to +125°C			0.35	V

6.5 Electrical Characteristics (Global) (continued)

at T_A = 25°C (unless otherwise noted)
Typical at V_{DD} = 15 V, V_{SS} = –15 V, GND = 0 V (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
POWER SUPPLY							
V_{UVLO}	Undervoltage lockout (UVLO) threshold voltage (V_{DD} – V_{SS})	Rising edge, single supply	–40°C to +125°C	5.1	5.8	6.4	V
		Falling edge, single supply	–40°C to +125°C	5	5.7	6.3	V
V_{HYS}	V_{DD} Undervoltage lockout (UVLO) hysteresis	Single supply	–40°C to +125°C		0.2		V
$R_{D(OVP)}$	Drain resistance to fault supply during overvoltage protection when enabled by DR pin		25°C		40		kΩ

6.6 ±15 V Dual Supply: Electrical Characteristics

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –10 V to +10 V I_D = –10 mA	25°C		8.3	10.7	Ω
			–40°C to +85°C			13.5	
			–40°C to +125°C			16	
ΔR_{ON}	On-resistance mismatch between channels	V_S = –10 V to +10 V I_D = –10 mA	25°C		0.05	0.45	Ω
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.6	
R_{FLAT}	On-resistance flatness	V_S = –10 V to +10 V I_D = –10 mA	25°C		0.005	0.4	Ω
			–40°C to +85°C			0.4	
			–40°C to +125°C			0.4	
R_{ON_DRIFT}	On-resistance drift	V_S = 0 V, I_S = –10 mA	–40°C to +125°C		0.04		Ω/°C
$I_{S(ON)}$, $I_{D(ON)}$	Channel on leakage current (1)	Switch state is on, V_{DD} = 16.5 V, V_{SS} = –16.5 V, V_S = V_D = ±10 V	25°C	–0.7	0.1	0.7	nA
			–40°C to +85°C	–2		2	
			–40°C to +125°C	–15		15	
FAULT CONDITION							
$I_{S(FA)}$	Input leakage current during overvoltage	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{FP} = 16.5 V, V_{SS} = V_{FN} = –16.5 V	–40°C to +125°C		±110		µA
$I_{S(FA)\ Grounded}$	Input leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = V_{FP} = V_{FN}= 0 V	–40°C to +125°C		±135		µA
$I_{S(FA)\ Floating}$	Input leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = V_{FP} = V_{FN}= floating,	–40°C to +125°C		±140		µA
$I_{D(FA)}$	Output leakage current during overvoltage	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{FP} = 16.5 V, V_{SS} = V_{FN} = –16.5 V, V_{DR} = 5 V or floating	25°C	–20	±0.1	20	nA
			–40°C to +85°C	–30		30	
			–40°C to +125°C	–60		60	
$I_{D(FA)\ Grounded}$	Output leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = V_{FP} = V_{FN} = 0 V	25°C	–30	±0.01	30	nA
			–40°C to +85°C	–50		50	
			–40°C to +125°C	–90		90	
$I_{D(FA)\ Floating}$	Output leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = V_{FP} = V_{FN} = floating	25°C		±0.6		µA
			–40°C to +85°C		±1.2		
			–40°C to +125°C		±2.2		

6.6 ±15 V Dual Supply: Electrical Characteristics (continued)

V_{DD} = +15 V ± 10%, V_{SS} = –15 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +15 V, V_{SS} = –15 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SWITCHING CHARACTERISTICS							
$t_{RESPONSE}$	Fault response time	V_{FP} = 10 V, V_{FN} = –10 V, R_L = 300 Ω, C_L= 12 pF	25°C		100	350	ns
			–40°C to +85°C			380	
			–40°C to +125°C			400	
$t_{RECOVERY}$	Fault recovery time	V_{FP} = 10 V, V_{FN} = –10 V, R_L = 300 Ω, C_L= 12 pF	25°C		1600	4500	ns
			–40°C to +85°C			4800	
			–40°C to +125°C			4800	
$t_{RESPONSE(FLAG)}$	Fault flag response time	V_{FP} = 10 V, V_{FN} = –10 V, V_{PU} = 5 V, R_{PU} = 1 kΩ, C_L= 12 pF	25°C		250		ns
$t_{RECOVERY(FLAG)}$	Fault flag recovery time	V_{FP} = 10 V, V_{FN} = –10 V, V_{PU} = 5 V, R_{PU} = 1 kΩ, C_L= 15 pF	25°C		1.2		µs
$t_{RESPONSE(DR)}$	Fault output response time	V_{FP} = 10 V, V_{FN} = –10 V, V_{PU} = 5 V, C_L= 12 pF	25°C		2.7		µs
X_{TALK}	Intra-channel crosstalk	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–100		dB
BW	–3 dB bandwidth (WQFN Package)	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V	25°C		650		MHz
BW	–3 dB bandwidth (TSSOP Package)	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V	25°C		580		MHz
I_{LOSS}	Insertion loss	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–0.7		dB
THD+N	Total harmonic distortion plus noise	R_S = 50 Ω, R_L = 10 kΩ, V_S = 15 V_{PP}, V_{BIAS} = 0 V, f = 20 Hz to 20 kHz	25°C		0.0006		%
$C_{S(ON)}$, $C_{D(ON)}$	Input/Output on-capacitance	f = 1 MHz, V_S = 0 V	25°C		14		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = V_{FP} = 16.5 V, V_{SS} = V_{FN} = –16.5 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		0.32	0.5	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.6	
I_{SS}	V_{SS} supply current	V_{DD} = V_{FP} = 16.5 V, V_{SS} = V_{FN} = –16.5 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		0.26	0.4	mA
			–40°C to +85°C			0.4	
			–40°C to +125°C			0.5	
I_{GND}	GND current	V_{DD} = V_{FP} = 16.5 V, V_{SS} = V_{FN} = –16.5 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		0.06		mA
I_{FP}	V_{FP} supply current	V_{DD} = V_{FP} = 16.5 V, V_{SS} = V_{FN} = –16.5 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		10		µA
I_{FN}	V_{FN} supply current	V_{DD} = V_{FP} = 16.5 V, V_{SS} = V_{FN} = –16.5 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		10		µA
$I_{DD(FA)}$	V_{DD} supply current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 16.5 V, V_{SS} = V_{FN} = –16.5 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		0.27	0.5	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.6	
$I_{SS(FA)}$	V_{SS} supply current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 16.5 V, V_{SS} = V_{FN} = –16.5 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		0.2	0.3	mA
			–40°C to +85°C			0.3	
			–40°C to +125°C			0.4	
$I_{GND(FA)}$	GND current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 16.5 V, V_{SS} = V_{FN} = –16.5 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		0.15		mA
$I_{FP(FA)}$	V_{FP} supply current under fault		25°C		10		µA
$I_{FN(FA)}$	V_{FN} supply current under fault		25°C		10		µA

(1) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.7 ±20 V Dual Supply: Electrical Characteristics

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = –15 V to +15 V I_D = –10 mA	25°C		8.3	10.5	Ω
			–40°C to +85°C			14	
			–40°C to +125°C			17	
ΔR_{ON}	On-resistance mismatch between channels	V_S = –15 V to +15 V I_D = –10 mA	25°C		0.05	0.35	Ω
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.5	
R_{FLAT}	On-resistance flatness	V_S = –15 V to +15 V I_D = –10 mA	25°C		0.006	0.4	Ω
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.5	
R_{ON_DRIFT}	On-resistance drift	V_S = 0 V, I_S = –10 mA	–40°C to +125°C		0.04		Ω/°C
$I_{S(ON)}$, $I_{D(ON)}$	Channel on leakage current (1)	Switch state is on, V_{DD} = 22 V, V_{SS} = –22 V V_S = V_D = ±15 V	25°C	–0.7	0.1	0.7	nA
			–40°C to +85°C	–2		2	
			–40°C to +125°C	–15		15	
FAULT CONDITION							
$I_{S(FA)}$	Input leakage current during overvoltage	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{FP} = 22 V, V_{SS} = V_{FN} = –22 V	–40°C to +125°C		±95		µA
$I_{S(FA)\ Grounded}$	Input leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0V, V_{DD} = V_{SS} = V_{FP} = V_{FN} = 0 V	–40°C to +125°C		±135		µA
$I_{S(FA)\ Floating}$	Input leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0V, V_{DD} = V_{SS} = V_{FP} = V_{FN} = floating	–40°C to +125°C		±140		µA
$I_{D(FA)}$	Output leakage current during overvoltage	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{FP} = 22 V, V_{SS} = V_{FN} = –22 V, V_{DR} = 5 V or floating	25°C	–50	±10	50	nA
			–40°C to +85°C	–70		70	nA
			–40°C to +125°C	–90		90	nA
$I_{D(FA)\ Grounded}$	Output leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = V_{FP} = V_{FN} = 0 V	25°C	–700	±500	700	nA
			–40°C to +85°C	–700		700	nA
			–40°C to +125°C	–700		700	nA
$I_{D(FA)\ Floating}$	Output leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = V_{FP} = V_{FN} = floating	25°C		±0.6		µA
			–40°C to +85°C		±1.3		µA
			–40°C to +125°C		±2.3		µA

6.7 ±20 V Dual Supply: Electrical Characteristics (continued)

V_{DD} = +20 V ± 10%, V_{SS} = –20 V ±10%, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +20 V, V_{SS} = –20 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SWITCHING CHARACTERISTICS							
$t_{RESPONSE}$	Fault response time	V_{FP} = 10 V, V_{FN} = –10 V, R_L = 300 Ω, C_L= 12 pF	25°C		150	400	ns
			–40°C to +85°C			430	
			–40°C to +125°C			450	
$t_{RECOVERY}$	Fault recovery time	V_{FP} = 10 V, V_{FN} = –10 V, R_L = 300 Ω, C_L= 12 pF	25°C		1100	4500	ns
			–40°C to +85°C			4900	
			–40°C to +125°C			4900	
$t_{RESPONSE(FLAG)}$	Fault flag response time	V_{FP} = 10 V, V_{FN} = –10 V, V_{PU} = 5 V, R_{PU} = 1 kΩ, C_L= 12 pF	–40°C to +125°C		220		ns
$t_{RECOVERY(FLAG)}$	Fault flag recovery time	V_{FP} = 10 V, V_{FN} = –10 V, V_{PU} = 5 V, R_{PU} = 1 kΩ, C_L= 12 pF	–40°C to +125°C		1.1		µs
$t_{RESPONSE(DR)}$	Fault output response time	V_{FP} = 10 V, V_{FN} = –10 V, V_{PU} = 5 V, C_L= 12 pF	–40°C to +125°C		2.7		µs
X_{TALK}	Intra-channel crosstalk	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–100		dB
BW	–3 dB bandwidth (WQFN Package)	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V	25°C		650		MHz
BW	–3 dB bandwidth (TSSOP Package)	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V	25°C		590		MHz
I_{LOSS}	Insertion loss	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 0 V, f = 1 MHz	25°C		–0.7		dB
THD+N	Total harmonic distortion plus noise	R_S = 50 Ω, R_L = 10 kΩ, V_S = 20 V_{PP}, V_{BIAS} = 0 V, f = 20 Hz to 20 kHz	25°C		0.0006		%
$C_{S(ON)}$, $C_{D(ON)}$	Input/Output on-capacitance	f = 1 MHz, V_S = 0 V	25°C		14		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = V_{FP} = 22 V, V_{SS} = V_{FN} = –22 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		0.32	0.5	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.6	
I_{SS}	V_{SS} supply current	V_{DD} = V_{FP} = 22 V, V_{SS} = V_{FN} = –22 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		0.26	0.4	mA
			–40°C to +85°C			0.4	
			–40°C to +125°C			0.5	
I_{GND}	GND current	V_{DD} = V_{FP} = 22 V, V_{SS} = V_{FN} = –22 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		0.07		mA
I_{FP}	V_{FP} supply current	V_{DD} = V_{FP} = 22 V, V_{SS} = V_{FN} = –22 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		10		µA
I_{FN}	V_{FN} supply current	V_{DD} = V_{FP} = 22 V, V_{SS} = V_{FN} = –22 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		10		µA
$I_{DD(FA)}$	V_{DD} supply current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 22 V, V_{SS} = V_{FN} = –22 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		0.27	0.5	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.6	
$I_{SS(FA)}$	V_{SS} supply current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 22 V, V_{SS} = V_{FN} = –22 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		0.2	0.3	mA
			–40°C to +85°C			0.3	
			–40°C to +125°C			0.4	
$I_{GND(FA)}$	GND current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 22 V, V_{SS} = V_{FN} = –22 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		0.15		mA
$I_{FP(FA)}$	V_{FP} supply current under fault		25°C		10		µA
$I_{FN(FA)}$	V_{FN} supply current under fault		25°C		10		µA

(1) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.8 12 V Single Supply: Electrical Characteristics

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25℃ (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 7.8 V, I_S = –10 mA	25°C		8.3	11	Ω
		V_S = 0 V to 7.8 V, I_S = –10 mA	–40°C to +85°C			15	Ω
		V_S = 0 V to 7.8 V, I_S = –10 mA	–40°C to +125°C			18	Ω
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 7.8 V, I_S = –10 mA	25°C		0.05	0.5	Ω
			–40°C to +85°C			0.6	
			–40°C to +125°C			0.7	
R_{FLAT}	On-resistance flatness	V_S = 0 V to 7.8 V, I_S = –10 mA	25°C		0.05	0.4	Ω
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.5	
R_{ON_DRIFT}	On-resistance drift	V_S = 6 V, I_S = –10 mA	–40°C to +125°C		0.04		Ω/°C
$I_{S(ON)}$, $I_{D(ON)}$	Output on leakage current(1)	Switch state is on, V_{DD} = 13.2 V, V_{SS} = 0 V, V_S = V_D = 1 V/ 10 V,	25°C	–0.7	0.1	0.7	nA
			–40°C to +85°C	–2		2	
			–40°C to +125°C	–14		14	
FAULT CONDITION							
$I_{S(FA)}$	Input leakage current during overvoltage	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V,	–40°C to +125°C		±145		μA
$I_{S(FA)\ Grounded}$	Input leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = V_{FP} = V_{FN} = 0 V	–40°C to +125°C		±135		μA
$I_{S(FA)\ Floating}$	Input leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = V_{FP} = V_{FN} = floating	–40°C to +125°C		±140		μA
$I_{D(FA)}$	Output leakage current during overvoltage	V_S = ± 60 V, GND = 0V, V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{DR} = 5 V or floating	25°C	–20	±2	20	nA
			–40°C to +85°C	–30		30	
			–40°C to +125°C	–50		50	
$I_{D(FA)\ Grounded}$	Output leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = V_{FP} = V_{FN} = 0 V	25°C	–30	±10	30	nA
			–40°C to +85°C	–50		50	
			–40°C to +125°C	–90		90	
$I_{D(FA)\ Floating}$	Output leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = V_{FP} = V_{FN} = floating	25°C		±0.6		μA
			–40°C to +85°C		±1.3		
			–40°C to +125°C		±2.3		

6.8 12 V Single Supply: Electrical Characteristics (continued)

V_{DD} = +12 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +12 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SWITCHING CHARACTERISTICS							
$t_{RESPONSE}$	Fault response time	V_{FP} = 8 V, V_{FN} = 0 V, R_L = 300 Ω, C_L= 12 pF	25°C		500	600	ns
			–40°C to +85°C			650	
			–40°C to +125°C			700	
$t_{RECOVERY}$	Fault recovery time	V_{FP} = 8 V, V_{FN} = 0 V, R_L = 300 Ω, C_L= 12 pF	25°C		850	2400	ns
			–40°C to +85°C			2900	
			–40°C to +125°C			2900	
$t_{RESPONSE(FLAG)}$	Fault flag response time	V_{FP} = 8 V, V_{FN} = 0 V, V_{PU} = 5 V, R_{PU} = 1 kΩ, C_L= 12 pF	–40°C to +125°C		110		ns
$t_{RECOVERY(FLAG)}$	Fault flag recovery time	V_{FP} = 8 V, V_{FN} = 0 V, V_{PU} = 5 V, R_{PU} = 1 kΩ, C_L= 12 pF	–40°C to +125°C		0.8		µs
$t_{RESPONSE(DR)}$	Fault output response time	V_{FP} = 8 V, V_{FN} = 0 V, R_L = 1 kΩ, C_L= 12 pF	–40°C to +125°C		3		µs
X_{TALK}	Inter-channel crosstalk	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 2 V, f = 1 MHz	25°C		–100		dB
BW	–3 dB bandwidth (WQFN Package)	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 2 V	25°C		620		MHz
BW	–3 dB bandwidth (TSSOP Package)	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 2 V	25°C		560		MHz
I_{LOSS}	Insertion loss	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 2 V, f = 1 MHz	25°C		–0.7		dB
THD+N	Total harmonic distortion plus noise	R_S = 50 Ω, R_L = 10 kΩ, V_S = 6 V_{PP}, V_{BIAS} = 6 V, f = 20 Hz to 20 kHz	25°C		0.0007		%
$C_{S(ON)}$, $C_{D(ON)}$	Input/Output on-capacitance	f = 1 MHz, V_S = 6 V	25°C		16		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		0.3	0.5	mA
			–40°C to +85°C			0.5	mA
			–40°C to +125°C			0.6	mA
I_{GND}	GND current	V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		0.06		mA
I_{FP}	V_{FP} supply current	V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		10		µA
I_{FN}	V_{FN} supply current	V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		10		µA
$I_{DD(FA)}$	V_{DD} supply current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		0.32	0.5	mA
			–40°C to +85°C			0.5	mA
			–40°C to +125°C			0.6	mA
$I_{GND(FA)}$	GND current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		0.16		mA
$I_{FP(FA)}$	V_{FP} supply current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		10		µA
$I_{FN(FA)}$	V_{FN} supply current under fault	V_S = ± 60 V, V_{DD} = V_{FP} = 13.2 V, V_{SS} = V_{FN} = 0 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		10		µA

(1) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

6.9 36 V Single Supply: Electrical Characteristics

V_{DD} = +36 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +36 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
ANALOG SWITCH							
R_{ON}	On-resistance	V_S = 0 V to 30 V, I_S = –10 mA	25°C		8.3	11	Ω
			–40°C to +85°C			14	
			–40°C to +125°C			17	
ΔR_{ON}	On-resistance mismatch between channels	V_S = 0 V to 30 V, I_S = –10 mA	25°C		0.05	0.5	Ω
			–40°C to +85°C			0.6	
			–40°C to +125°C			0.7	
R_{FLAT}	On-resistance flatness	V_S = 0 V to 30 V, I_S = –10 mA	25°C		0.06	0.9	Ω
			–40°C to +85°C			1.1	
			–40°C to +125°C			1.3	
R_{ON_DRIFT}	On-resistance drift	V_S = 18 V, I_S = –10 mA	–40°C to +125°C		0.04		Ω/°C
$I_{S(ON)}$, $I_{D(ON)}$	Output on leakage current[1]	Switch state is on, V_{DD} = 39.6 V, V_{SS} = 0 V, V_S = V_D = 1 V/ 30 V	25°C	–0.7	0.2	0.7	nA
			–40°C to +85°C	–2		2	
			–40°C to +125°C	–15		15	
FAULT CONDITION							
$I_{S(FA)}$	Input leakage current during overvoltage	V_S = 60 / –40 V, GND = 0 V, V_{DD} = V_{FP} = 39.6 V, V_{SS} = V_{FN} = 0 V	–40°C to +125°C		±98		µA
$I_{S(FA)\ Grounded}$	Input leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = V_{FP} = V_{FN} = 0 V	–40°C to +125°C		±135		µA
$I_{S(FA)\ Floating}$	Input leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = V_{FP} = V_{FN} = floating	–40°C to +125°C		±140		µA
$I_{D(FA)}$	Output leakage current during overvoltage	V_S = 60 / –40 V, GND = 0 V, V_{DD} = V_{FP} = 39.2 V, V_{SS} = V_{FN} = 0 V, V_{DR} = 5 V or floating	25°C	–20	±2	20	nA
			–40°C to +85°C	–30		30	
			–40°C to +125°C	–50		50	
$I_{D(FA)\ Grounded}$	Output leakage current during overvoltage with grounded supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = V_{FP} = V_{FN} = 0 V	25°C	–30	±10	30	nA
			–40°C to +85°C	–50		50	
			–40°C to +125°C	–90		90	
$I_{D(FA)\ Floating}$	Output leakage current during overvoltage with floating supply voltages	V_S = ± 60 V, GND = 0 V, V_{DD} = V_{SS} = V_{FP} = V_{FN} = floating	25°C		±0.6		µA
			–40°C to +85°C		±1.3		
			–40°C to +125°C		±2.3		

6.9 36 V Single Supply: Electrical Characteristics (continued)

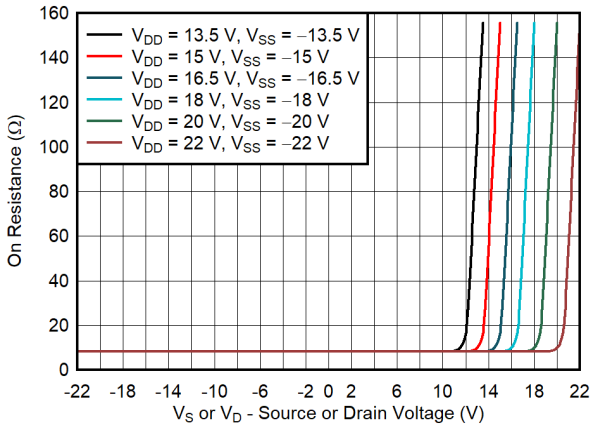
V_{DD} = +36 V ± 10%, V_{SS} = 0 V, GND = 0 V (unless otherwise noted)
Typical at V_{DD} = +36 V, V_{SS} = 0 V, T_A = 25°C (unless otherwise noted)

PARAMETER		TEST CONDITIONS	T_A	MIN	TYP	MAX	UNIT
SWITCHING CHARACTERISTICS							
$t_{RESPONSE}$	Fault response time	V_{FP} = 18 V, V_{FN} = 0 V, R_L = 300 Ω, C_L= 12 pF	25°C		150	310	ns
			–40°C to +85°C			330	
			–40°C to +125°C			350	
$t_{RECOVERY}$	Fault recovery time	V_{FP} = 18 V, V_{FN} = 0 V, R_L = 300 Ω, C_L= 12 pF	25°C		1100	2200	ns
			–40°C to +85°C			2700	
			–40°C to +125°C			2700	
$t_{RESPONSE(FLAG)}$	Fault flag response time	V_{FP} = 18 V, V_{FN} = 0 V, V_{PU} = 5 V, R_{PU} = 1 kΩ, C_L= 12 pF	–40°C to +125°C		110		ns
$t_{RECOVERY(FLAG)}$	Fault flag recovery time	V_{FP} = 18 V, V_{FN} = 0 V, V_{PU} = 5 V, R_{PU} = 1 kΩ, C_L= 12 pF	–40°C to +125°C		0.8		µs
$t_{RESPONSE(DR)}$	Fault output response time	V_{FP} = 8 V, V_{FN} = 0 V, R_L = 1 kΩ, C_L= 12 pF	–40°C to +125°C		2.7		µs
X_{TALK}	Inter-channel crosstalk	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200m V_{RMS}, V_{BIAS} = 2 V, f = 1 MHz	25°C		–100		dB
BW	–3 dB bandwidth (WQFN Package)	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 2 V	25°C		600		MHz
BW	–3 dB bandwidth (TSSOP Package)	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 2 V	25°C		580		MHz
I_{LOSS}	Insertion loss	R_S = 50 Ω, R_L = 50 Ω, C_L = 5 pF, V_S = 200 mV_{RMS}, V_{BIAS} = 2 V, f = 1 MHz	25°C		–0.7		dB
THD+N	Total harmonic distortion plus noise	R_S = 50 Ω, R_L = 10 kΩ, V_S = 18 V_{PP}, V_{BIAS} = 18 V, f = 20 Hz to 20 kHz	25°C		0.0006		%
$C_{S(ON)}$, $C_{D(ON)}$	Input/Output on-capacitance	f = 1 MHz, V_S = 18 V	25°C		17		pF
POWER SUPPLY							
I_{DD}	V_{DD} supply current	V_{DD} = V_{FP} = 39.6 V, V_{SS} = V_{FN} = 0 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		0.3	0.5	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.6	
I_{SS}	V_{SS} supply current	V_{DD} = V_{FP} = 39.6 V V_{SS} = V_{FN} = 0 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		0.25		mA
I_{GND}	GND current	V_{DD} = V_{FP} = 39.6 V, V_{SS} = V_{FN} = 0 V, V_{DR} = 5 V, or V_{DD}	25°C		0.07		mA
I_{FP}	V_{FP} supply current	V_{DD} = V_{FP} = 39.6 V, V_{SS} = V_{FN} = 0 V, V_{DR} = 5 V, or V_{DD}	25°C		10		µA
I_{FN}	V_{FN} supply current	V_{DD} = V_{FP} = 39.6 V, V_{SS} = V_{FN} = 0 V, V_{DR} = 5 V, or V_{DD}	25°C		10		µA
$I_{DD(FA)}$	V_{DD} supply current under fault	V_S = 60 / –40 V, V_{DD} = V_{FP} = 39.6 V, V_{SS} = V_{FN} = 0 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		0.32	0.5	mA
			–40°C to +85°C			0.5	
			–40°C to +125°C			0.6	
$I_{SS(FA)}$	V_{SS} supply current under fault	V_S = 60 / –40 V, V_{DD} = V_{FP} = 39.6 V, V_{SS} = V_{FN} = 0 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		0.18		mA
$I_{GND(FA)}$	GND current under fault	V_S = 60 / –40 V, V_{DD} = V_{FP} = 39.6 V, V_{SS} = V_{FN} = 0 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		0.12		mA
$I_{FP(FA)}$	V_{FP} supply current under fault	V_S = 60 / –40 V, V_{DD} = V_{FP} = 39.6 V, V_{SS} = V_{FN} = 0 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		10		µA
$I_{FN(FA)}$	V_{FN} supply current under fault	V_S = 60 / –40 V, V_{DD} = V_{FP} = 39.6 V, V_{SS} = V_{FN} = 0 V, V_{DR} = 0 V, 5 V, or V_{DD}	25°C		10		µA

(1) When V_S is at a voltage potential, V_D is floating, or when V_D is at a voltage potential, V_S is floating.

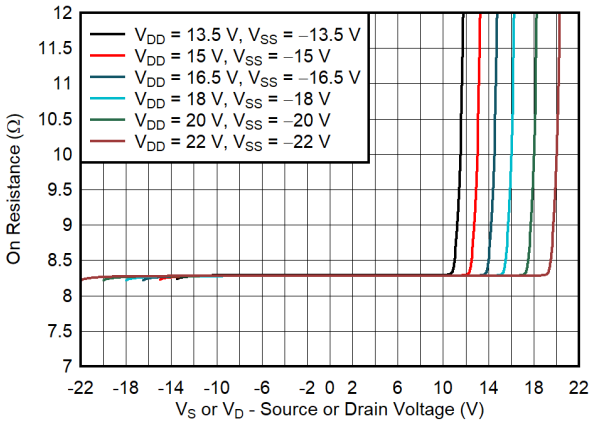
6.10 Typical Characteristics

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)



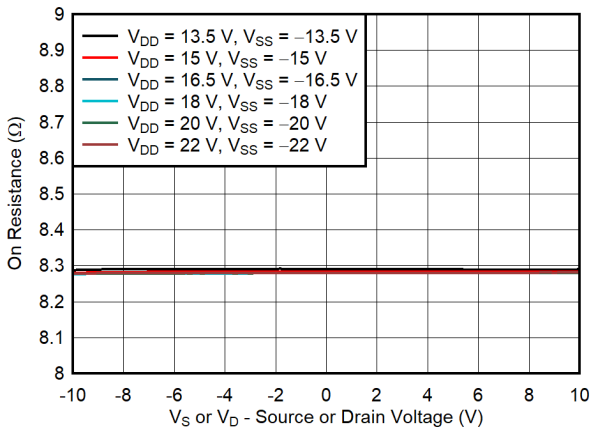
Dual Supply Voltages

図 6-1. On-Resistance vs Source or Drain Voltage



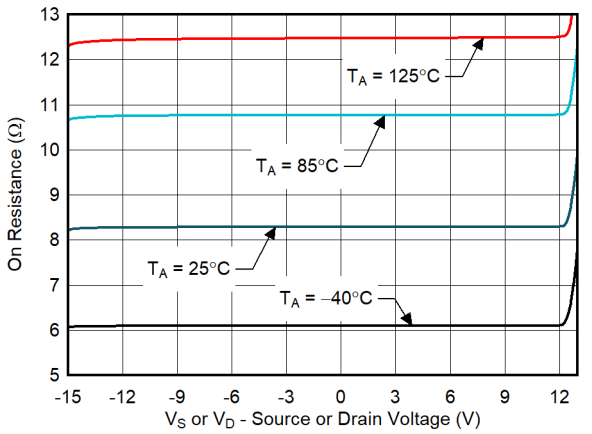
Dual Supply Flat Ron Region

図 6-2. On-Resistance vs Source or Drain Voltage



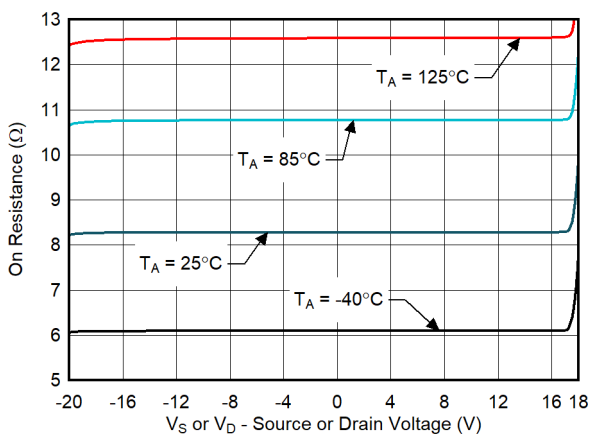
Flattest R_{ON} region for all supply voltages shown

図 6-3. On-Resistance vs Source or Drain Voltage



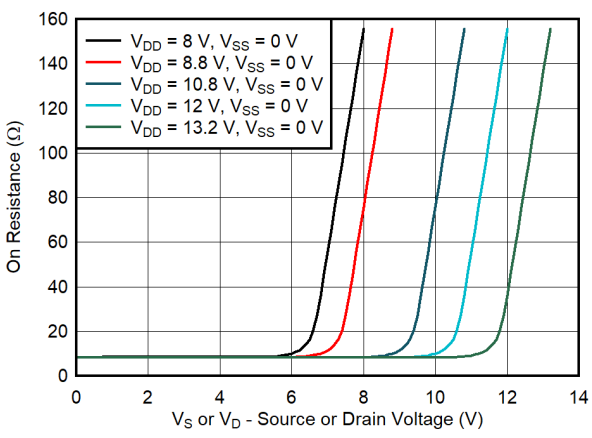
±15 V Supply Flattest Ron Region

図 6-4. On-Resistance vs Source or Drain Voltage



±20 V Supply Flattest Ron Region

図 6-5. On-Resistance vs Source or Drain Voltage

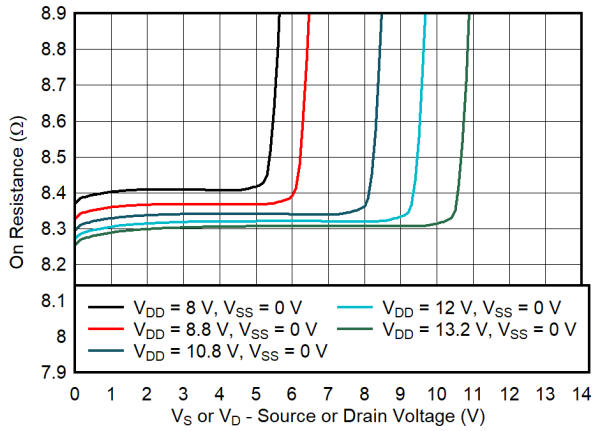


Single Supply Voltages

図 6-6. On-Resistance vs Source or Drain Voltage

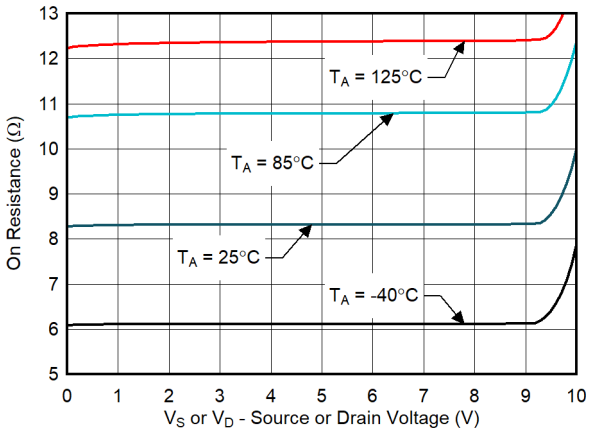
6.10 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)



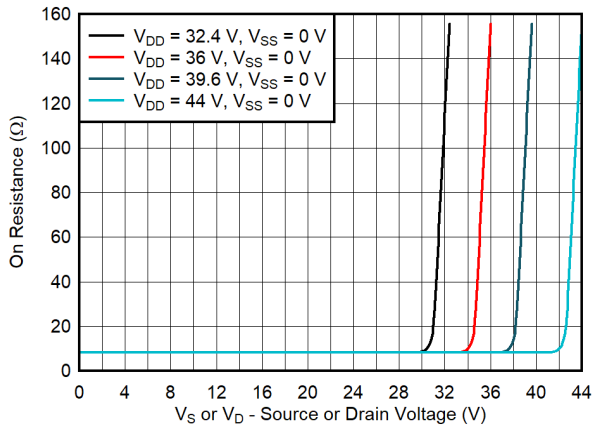
Single Supply Flat Ron Region

図 6-7. On-Resistance vs Source or Drain Voltage



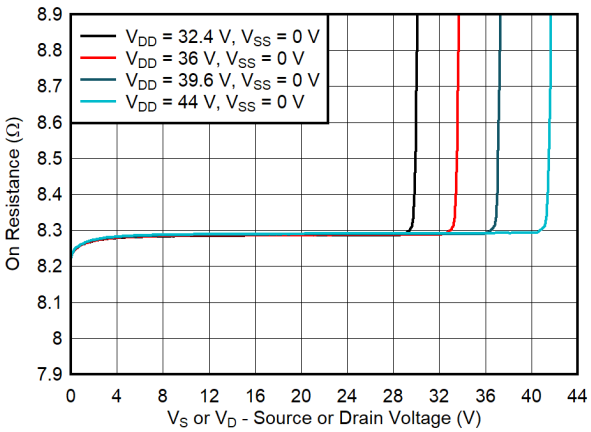
12 V V_{DD} Flattest Ron Region

図 6-8. On-Resistance vs Source or Drain Voltage



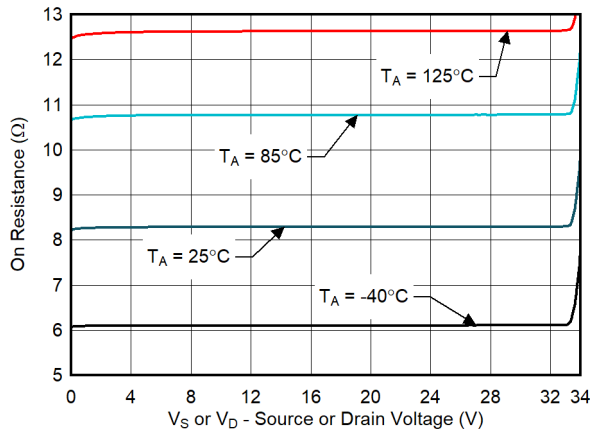
Single Supply Voltages

図 6-9. On-Resistance vs Source or Drain Voltage



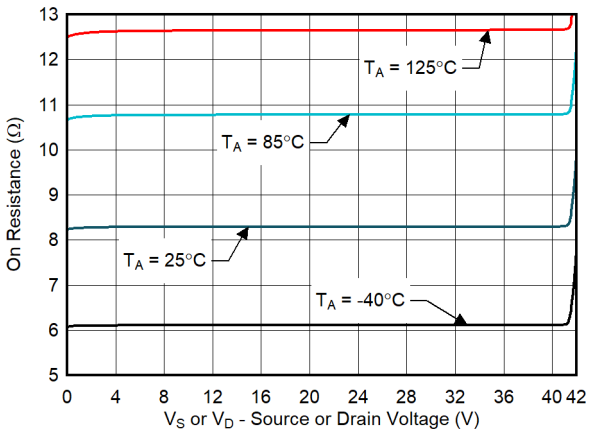
Single Supply Flat Ron Region

図 6-10. On-Resistance vs Source or Drain Voltage



36 V V_{DD} Flattest Ron Region

図 6-11. On-Resistance vs Source or Drain Voltage

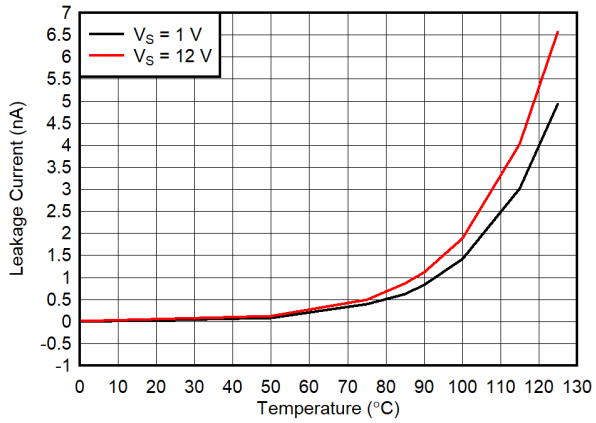


44 V V_{DD} Flattest Ron Region

図 6-12. On-Resistance vs Source or Drain Voltage

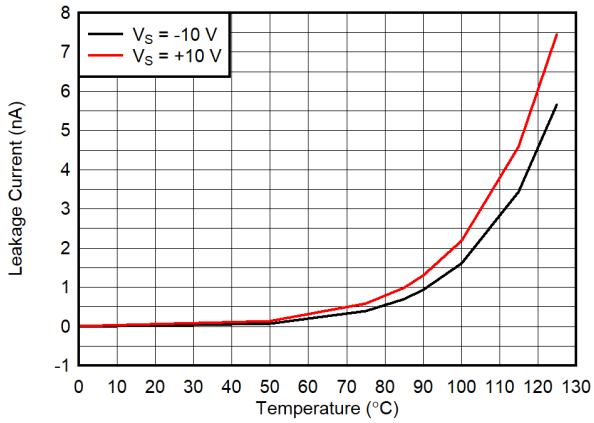
6.10 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)



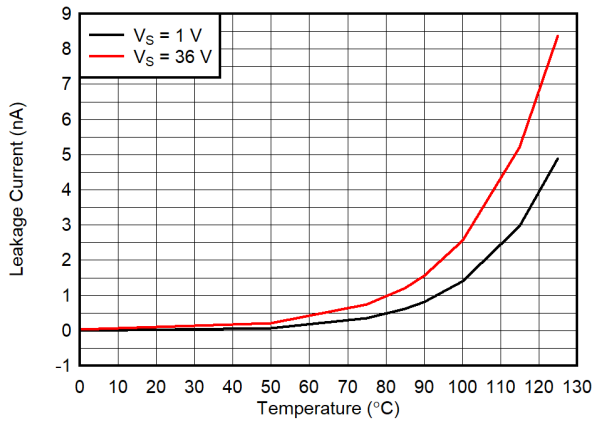
V_{DD} = 12 V, V_{SS} = 0 V

図 6-13. I_{ON} Leakage Current vs Temperature



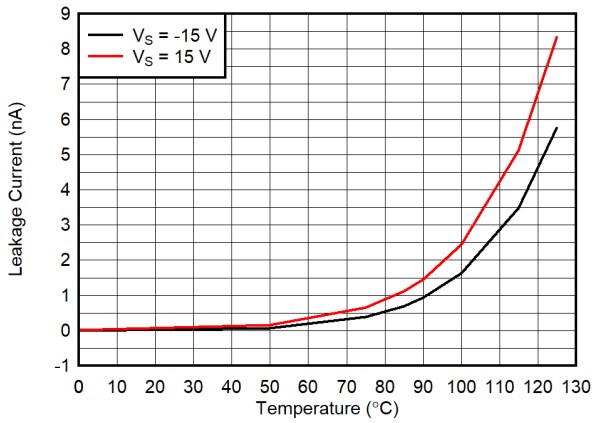
V_{DD} = 15 V, V_{SS} = -15 V

図 6-14. I_{ON} Leakage Current vs Temperature



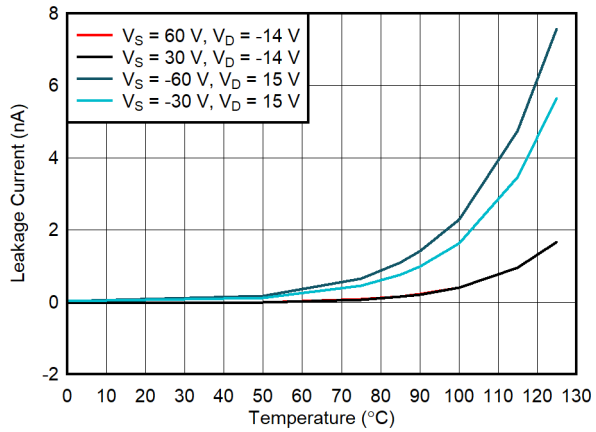
V_{DD} = 36 V, V_{SS} = 0 V

図 6-15. I_{ON} Leakage Current vs Temperature



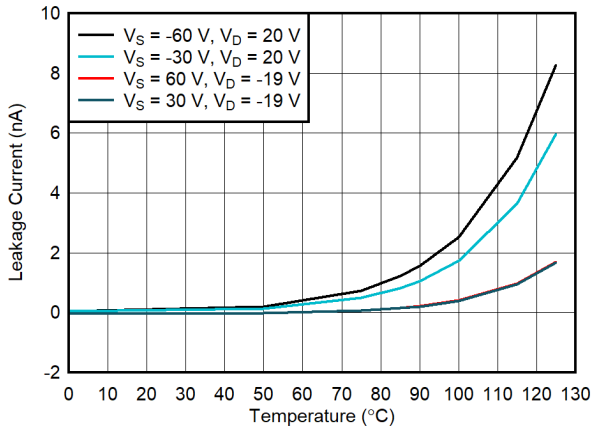
V_{DD} = +20 V, V_{SS} = -20 V

図 6-16. I_{ON} Leakage Current vs Temperature



±15 V Dual Supply

図 6-17. $I_{D(FA)}$ Overvoltage Leakage Current vs Temperature

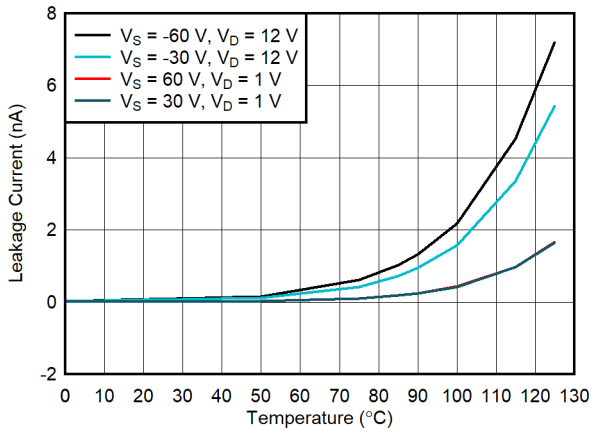


±20 V Dual Supply

図 6-18. $I_{D(FA)}$ Overvoltage Leakage Current vs Temperature

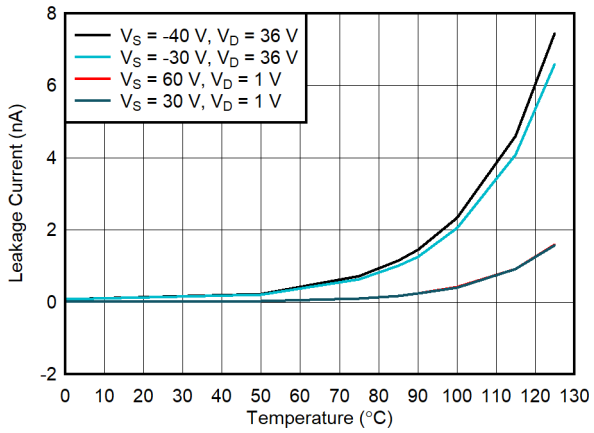
6.10 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)



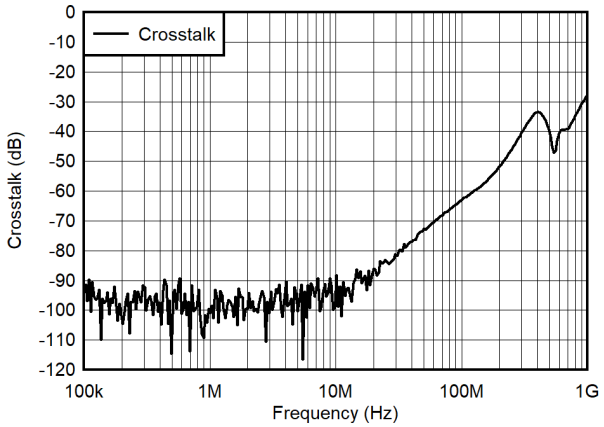
V_{DD} = 12 V Single Supply

図 6-19. $I_{D(FA)}$ Overvoltage Leakage Current vs Temperature



V_{DD} = 36 V Single Supply

図 6-20. $I_{D(FA)}$ Overvoltage Leakage Current vs Temperature



±15 V Dual Supply

図 6-21. Crosstalk vs Frequency

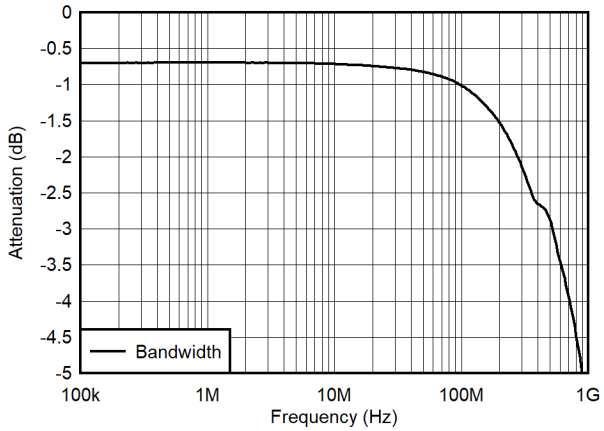


図 6-22. Insertion Loss vs Frequency

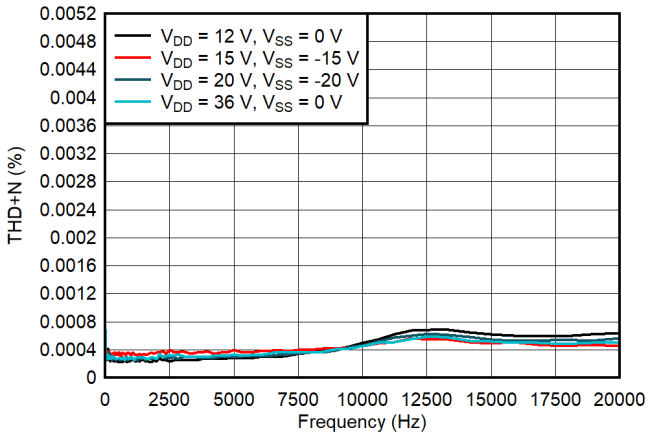


図 6-23. THD+N vs Frequency

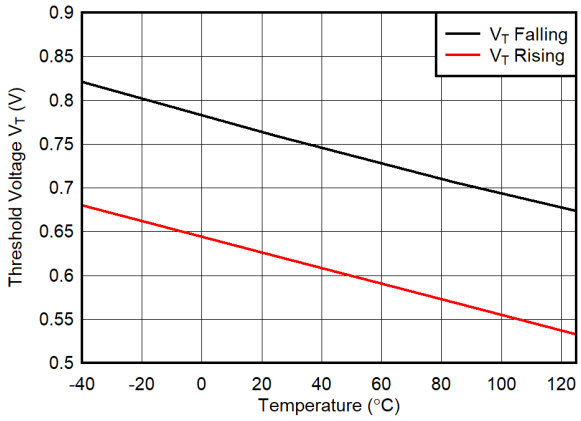
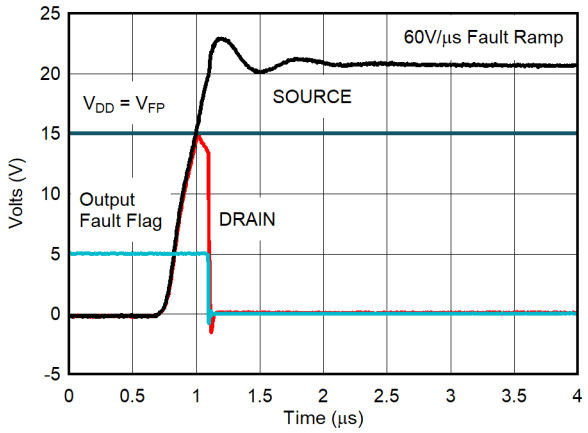


図 6-24. Threshold Voltage vs Temperature

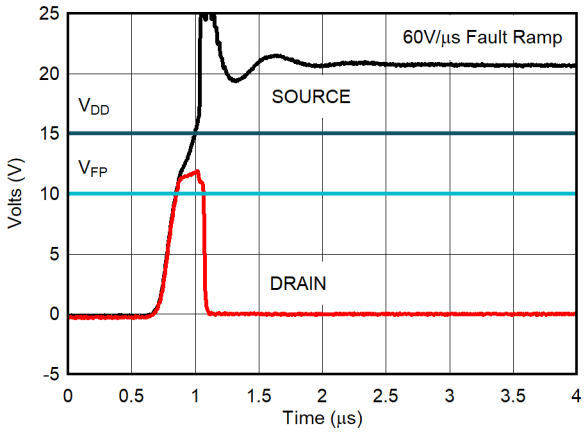
6.10 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)



V_{DD} = V_{FP} = 15 V

図 6-25. Drain Output Response - Positive Overvoltage



V_{DD} = 15 V, V_{FP} = 10 V

図 6-26. Drain Output Response - Positive Overvoltage

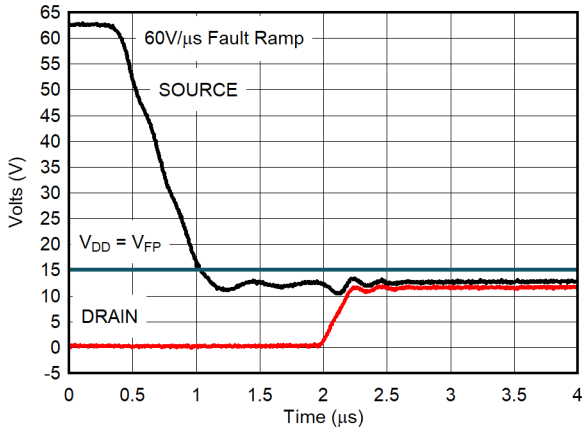


図 6-27. Drain Output Recovery - Positive Overvoltage

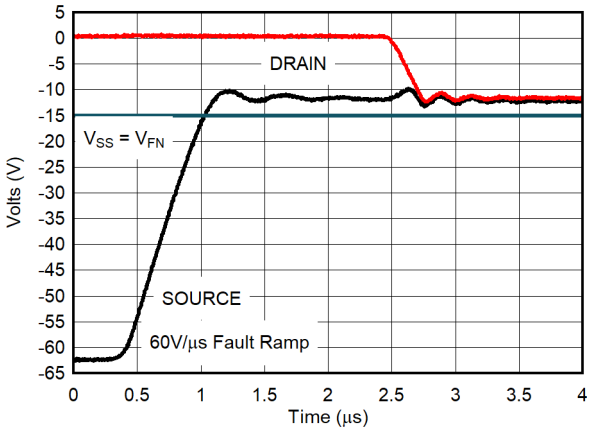


図 6-28. Drain Output Recovery - Negative Overvoltage

6.10 Typical Characteristics (continued)

at T_A = 25°C, V_{DD} = 15 V, and V_{SS} = –15 V (unless otherwise noted)

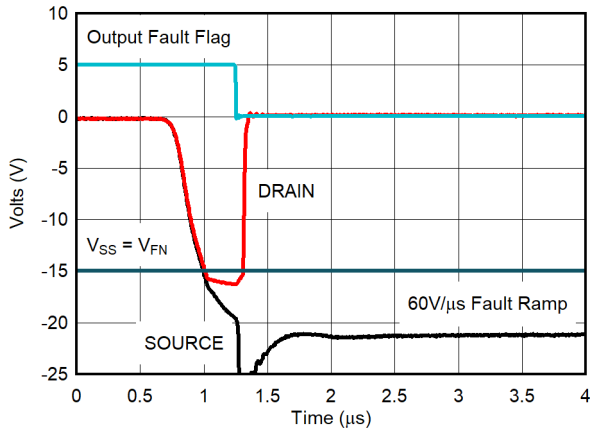


図 6-29. Drain Output Response - Negative Overvoltage

7 Parameter Measurement Information

7.1 On-Resistance

The TMUX7462F's on-resistance is the ohmic resistance across the source (Sx) and drain (Dx) pins of the device. The on-resistance varies with input voltage and supply voltage. The symbol R_{ON} is used to denote on-resistance. The measurement setup used to measure R_{ON} is shown in 図 7-1. ΔR_{ON} represents the difference between the R_{ON} of any two channels, while R_{ON_FLAT} denotes the flatness that is defined as the difference between the maximum and minimum value of on-resistance measured over the specified analog signal range.

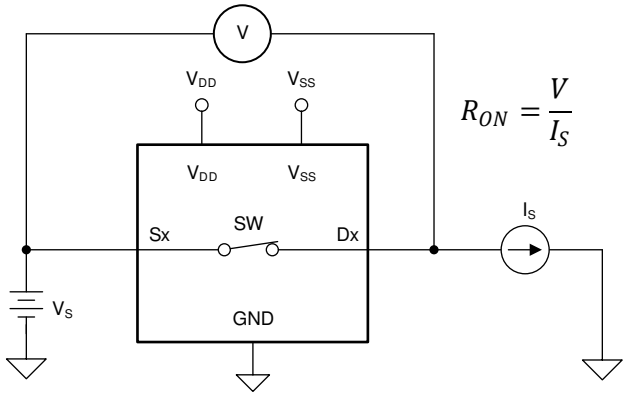


図 7-1. On-Resistance Measurement Setup

7.2 On-Leakage Current

Source on-leakage current ($I_{S(ON)}$) and drain on-leakage current ($I_{D(ON)}$) denotes the channel leakage currents when the switch is in the on state. $I_{S(ON)}$ is measured with the drain floating, while $I_{D(ON)}$ is measured with the source floating. 図 7-2 shows the circuit used for measuring the on-leakage currents.

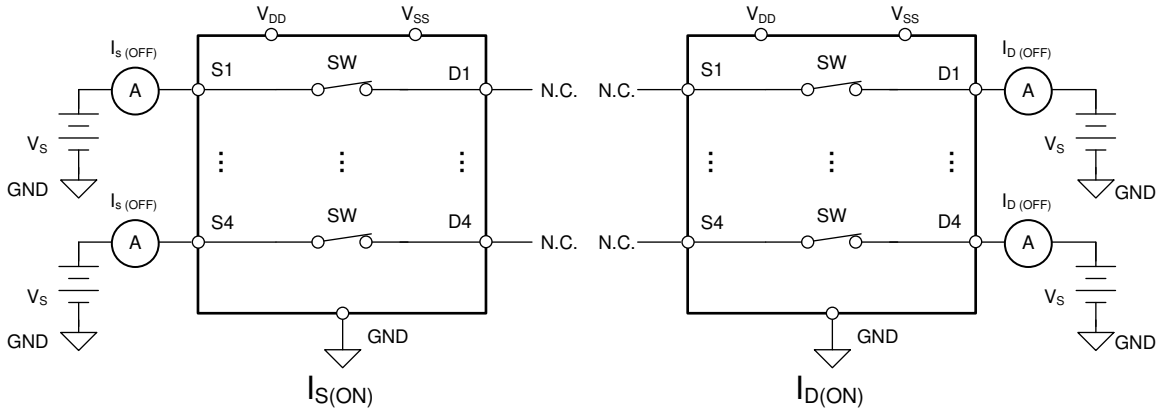


図 7-2. On-Leakage Measurement Setup

7.3 Input and Output Leakage Current under Overvoltage Fault

If any of the source pin voltage goes above the fault supplies (V_{FP} or V_{FN}) by one threshold voltage (V_T), the TMUX7462F's overvoltage protection feature is triggered to turn off the switch under fault, keeping the fault channel in the high-impedance state. $I_{S(FA)}$ and $I_{D(FA)}$ denotes the input and output leakage current under overvoltage fault conditions, respectively. The supply (or supplies) can either be in normal operating condition (図 7-3) or abnormal operating condition (図 7-4) when the overvoltage fault occurs. The supply (or supplies) can either be unpowered (V_{DD}= V_{SS} = V_{FN} = V_{FP} = 0 V), floating (V_{DD}= V_{SS} = V_{FN} = V_{FP} = No Connection), or at any level that is below the undervoltage (UV) threshold during abnormal operating conditions.

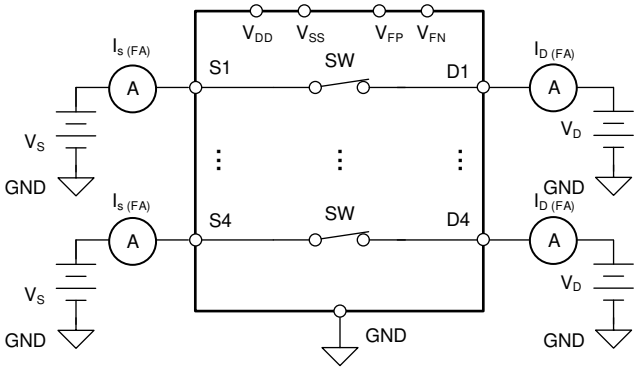


図 7-3. Measurement Setup for Input and Output Leakage Current Under Overvoltage Fault with Normal Supplies

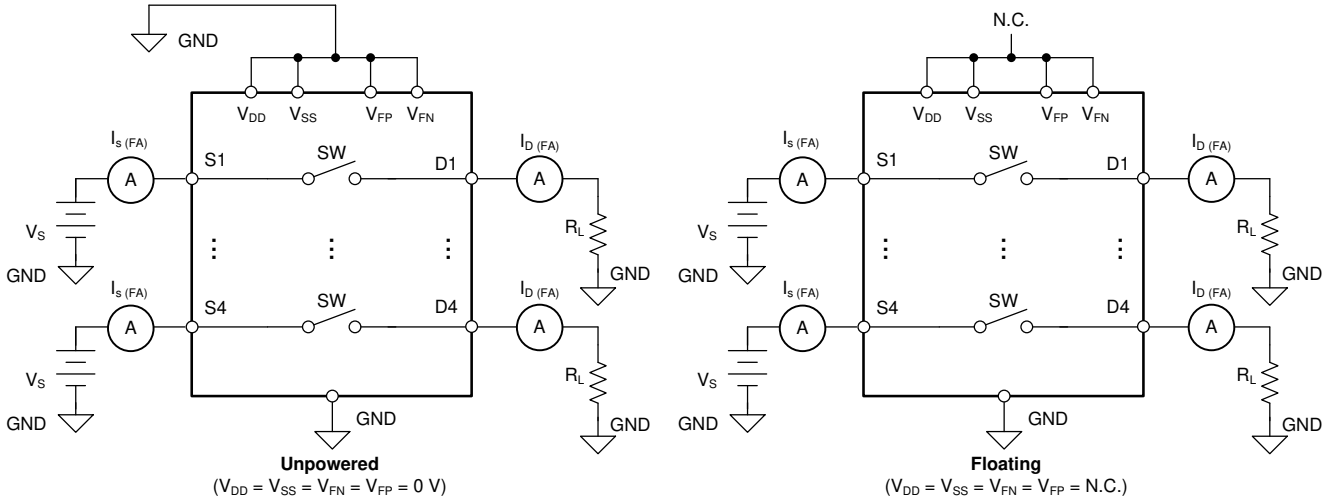


図 7-4. Measurement Setup for Input and Output Leakage Current Under Overvoltage Fault with Unpowered or Floating Supplies

7.4 Fault Response Time

Fault response time ($t_{RESPONSE}$) measures the delay between the source voltage exceeding the fault supply voltage (V_{FP} or V_{FN}) by 0.5V and the drain voltage failing to 90% of the fault supply voltage exceeded. 図 7-5 shows the setup used to measure $t_{RESPONSE}$.

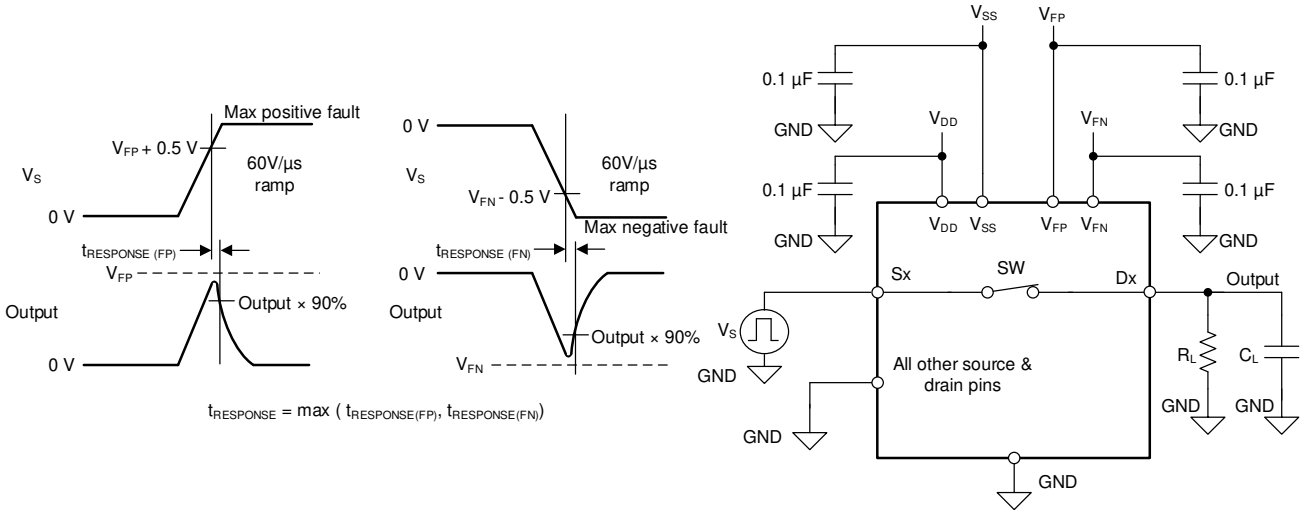


図 7-5. Fault Response Time Measurement Setup

7.5 Fault Recovery Time

Fault recovery time ($t_{RECOVERY}$) measures the delay between the source voltage falling from overvoltage condition to below fault supply voltage (V_{FP} or V_{FN}) plus 0.5 V and the drain voltage rising from 0V to 50% of the fault supply voltage exceeded. 図 7-6 shows the setup used to measure $t_{RECOVERY}$.

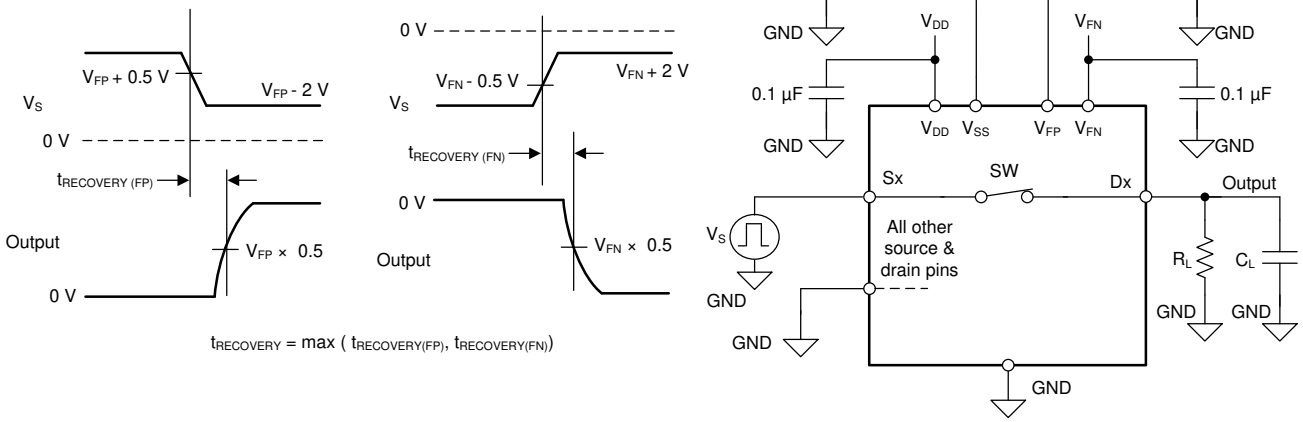


図 7-6. Fault Recovery Time Measurement Setup

7.6 Fault Flag Response Time

Fault flag response time ($t_{RESPONSE(FLAG)}$) measures the delay between the source voltage exceeding the fault supply voltage (V_{FP} or V_{FN}) by 0.5 V and the general fault flag (FF) pin to go below 10% of its original value. 図 7-7 shows the setup used to measure $t_{RESPONSE(FLAG)}$.

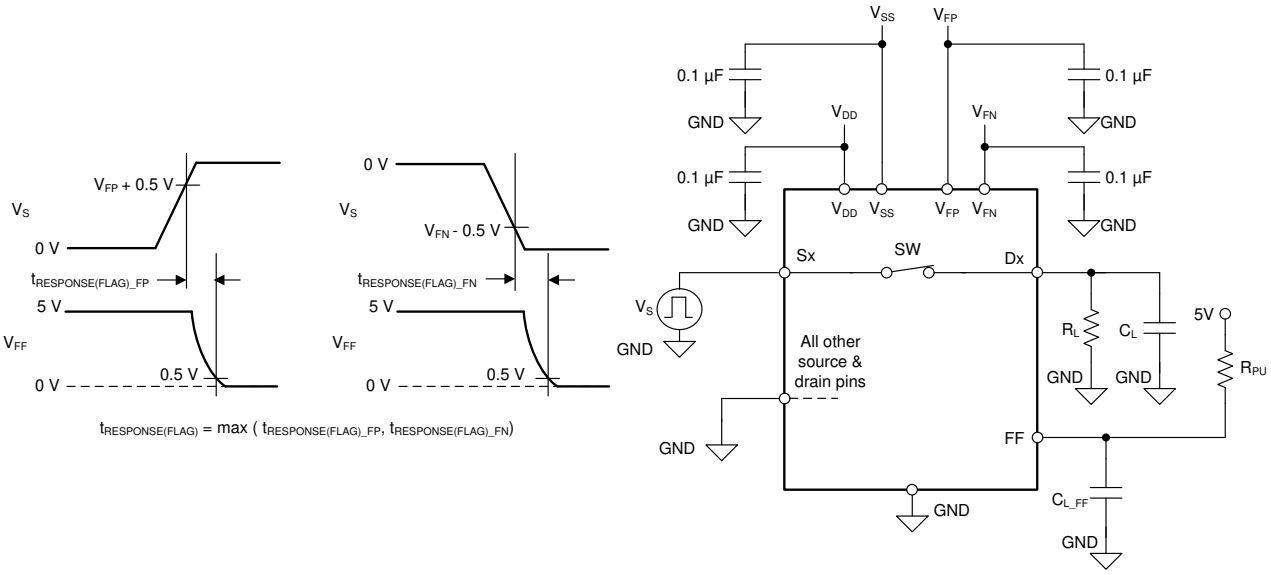


図 7-7. Fault Flag Response Time Measurement Setup

7.7 Fault Flag Recovery Time

Fault flag recovery time ($t_{RECOVERY(FLAG)}$) measures the delay between the source voltage falling from the overvoltage condition to below the fault supply voltage (V_{FP} or V_{FN}) plus 0.5 V and the general fault flag (FF) pin to rise above 3 V with 5 V external pull-up. 図 7-8 shows the setup used to measure $t_{RECOVERY(FLAG)}$.

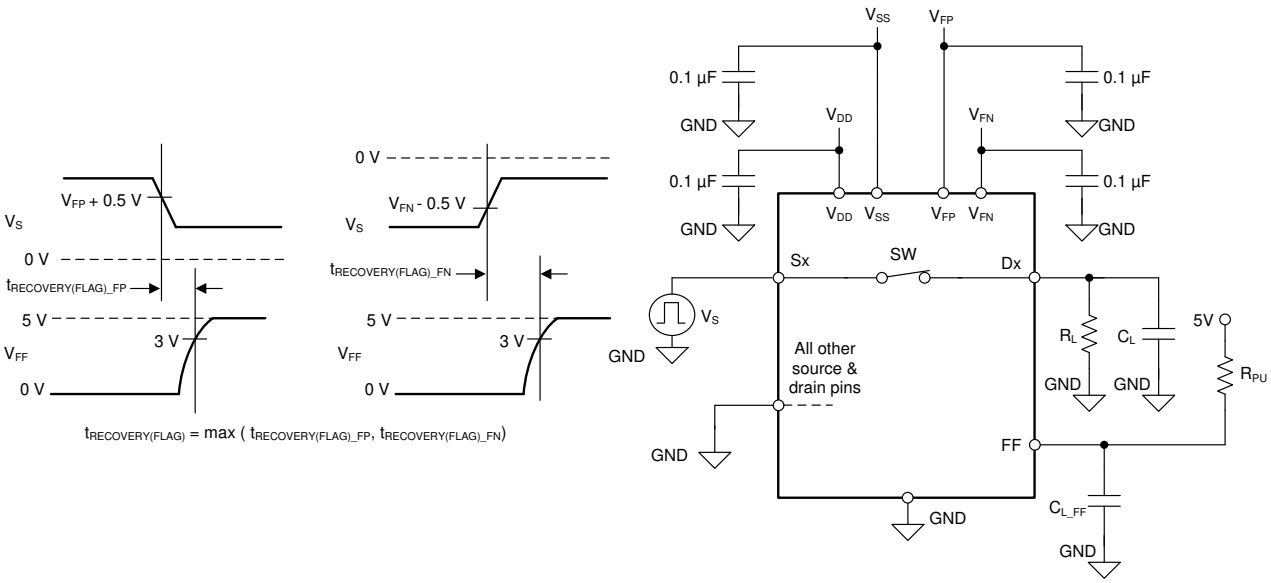


図 7-8. Fault Flag Recovery Time Measurement Setup

7.8 Fault Drain Enable Time

$t_{RESPONSE(DR)}$ represents the delay between the voltage at the DR pin falling from a high to low signal and the output of the drain pin reaching 90% of the fault supplies (V_{FP} or V_{FN}). $t_{RESPONSE(DR)}$ is a measure of how quickly the internal pull-up engages in response to the DR pin. 図 7-9 shows the setup used to measure $t_{RESPONSE(DR)}$.

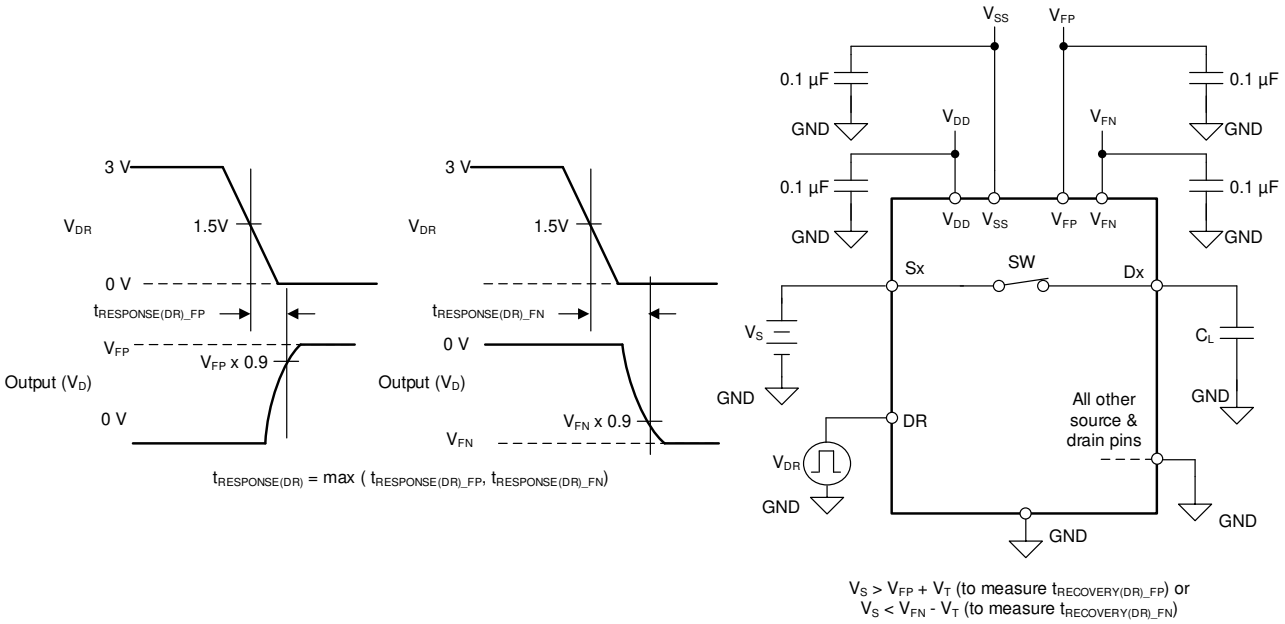


図 7-9. Fault Drain Enable Time Measurement Setup

7.9 Inter-Channel Crosstalk

図 7-10 and 式 1 shows how the inter-channel crosstalk ($X_{TALK(INTER)}$) is measured as the voltage at the source pin (Sx) of an on-switch input, when a 1-V_{RMS} signal is applied at the source pin of an on-switch input in a different channel.

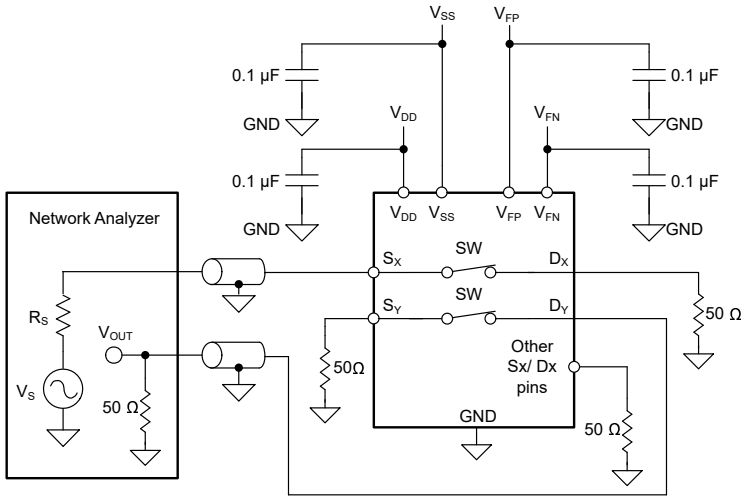


図 7-10. Inter-Channel Crosstalk Measurement Setup

$$Inter-channel\ Crosstalk = 20 \times Log \frac{V_{OUT}}{V_S} \quad (1)$$

7.10 Bandwidth

Bandwidth (BW) is defined as the range of frequencies that are attenuated by < 3 dB when the input is applied to the source pin (Sx) of an on-channel, and the output is measured at the TMUX7462F's drain pin (D or Dx). 図 7-11 and 式 2 shows the setup used to measure bandwidth of the switch.

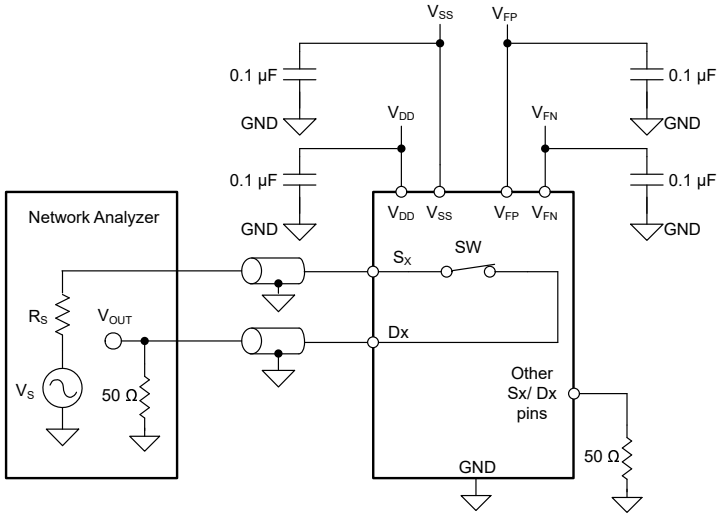


図 7-11. Bandwidth Measurement Setup

$$Bandwidth = 20 \times Log \frac{V_{OUT}}{V_S} \quad (2)$$

7.11 THD + Noise

The total harmonic distortion (THD) of a signal is a measurement of the harmonic distortion, and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency at the multiplexer output. The on-resistance of the TMUX7462F varies with the amplitude of the input signal and results in distortion when the drain pin is connected to a low-impedance load. Total harmonic distortion plus noise is denoted as THD+N. 図 7-12 shows the setup used to measure THD+N of the devices.

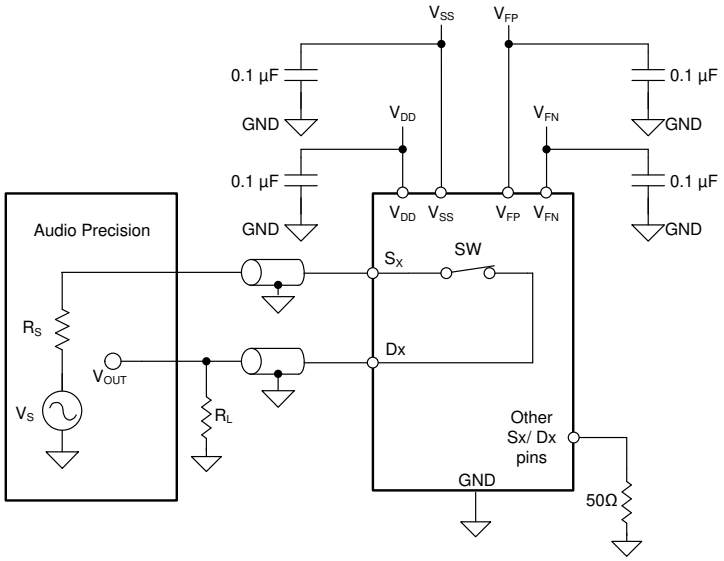


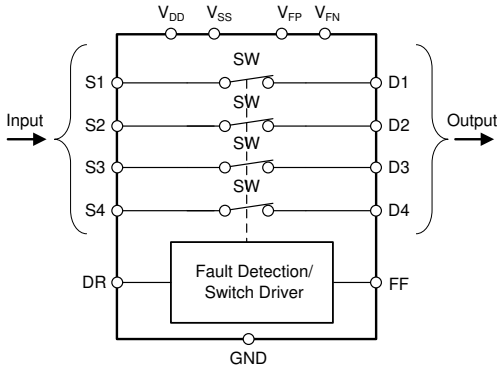
図 7-12. THD+N Measurement Setup

8 Detailed Description

8.1 Overview

The TMUX7462F is a four-channel protector that can be placed in series with the signal path to protect sensitive components downstream from overvoltage faults. The channel protector prevents overvoltages in both powered and powered-off conditions, making it suitable for applications where correct power supply sequencing cannot be precisely controlled. The powered-off condition includes floating power supplies, grounded power supplies, or power supplies at any level that are below the undervoltage (UV) threshold. The internal switch is turned-on and turned-off autonomously based on the fault situation without the need of external controls, making the device extremely easy to implement in the system. The primary supply voltages define the on-resistance profile, while the secondary supply voltages define the voltage level at which the overvoltage protection engages. The device works well with dual supplies (±5 V to ±22 V), a single supply (8 V to 44 V), or asymmetric supplies (such as V_{DD} = 12 V, V_{SS} = –5 V).

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Flat ON-Resistance

The TMUX7462F are designed with a special switch architecture to produce ultra-flat on-resistance (R_{ON}) across most of the switch input operation region. The flat R_{ON} response allows the device to be used in precision sensor applications since the R_{ON} is controlled regardless of the signals sampled. The architecture is implemented without a charge pump so no unwanted noise is produced from the device to affect sampling accuracy.

8.3.2 Protection Features

The TMUX7462F offers a number of protection features to enable robust system implementations.

8.3.2.1 Input Voltage Tolerance

The maximum voltage that can be applied to any source input pin is +60 V or -60 V, allowing the device to handle typical voltage fault conditions in industrial applications. Take caution: the device has different maximum stress ratings across different pin combinations and are defined as the following:

1. **Between source pins and supply rails: 85 V**

   For example, if the device is powered by V_{DD} supply of 25 V, then the maximum negative signal level on any source pin is –60 V. If the device is powered by V_{DD} supply of 40 V, then the maximum negative signal level on any source pin is reduced to –45 V to maintain the 85 V maximum rating across the source pin and the supply.
2. **Between source pins and drain pin of the same channel: 85 V**

   For example, if the DR pin is left floating and an overvoltage voltage fault of –60 V occurs on the source pin S1, then the maximum positive voltage signal level driven on the drain pin channel D1 is 25 V to maintain the 85 V maximum rating across the source pin and the drain pin.

8.3.2.2 Powered-Off Protection

The source (Sx) pins of the device remain in the high impedance (Hi-Z) state, and the device performance remains within the leakage performance specifications when the supplies of TMUX7462F are removed (V_{DD}/ V_{SS} = 0 V or floating) or at a level that is below the undervoltage (UV) threshold. Powered-off protection minimizes system design complexity by removing the need to control the system's power supply sequencing. The feature prevents errant voltages on the input source pins from reaching the rest of the system and maintains isolation when the system is powering up. Without powered-off protection, signal on the input source pins can back-power the supply rails through internal ESD diodes and cause potential damage to the system.

A GND reference must always be present to for proper operation. Source and drain voltage levels of up to ±60 V are blocked in the powered-off condition.

8.3.2.3 Fail-Safe Logic

Fail-Safe logic circuitry allows voltages on the control input pin (DR) to be applied before the supply pins. This eliminates the need for power sequencing of the logic signals and protects the device from potential damage. The control inputs are protected against positive faults of up to +44 V in the powered-off condition, but do not offer protection against a negative overvoltage condition.

8.3.2.4 Overvoltage Protection and Detection

The TMUX7462F detects overvoltage inputs by comparing the voltage on a source pin (Sx) with the fault supplies (V_{FP} and V_{FN}). A signal is considered overvoltage if it exceeds the fault supply voltages by the threshold voltage (V_T).

The switch automatically turns OFF and the source pin becomes high impedance so that only small leakage currents flow through the switch when an overvoltage is detected. The drain pin (Dx) behavior can be adjusted by controlling the drain response (DR) pin in the following ways:

1. **DR pin floating or driven above V_{IH}:**

   If the DR pin is driven about VIH level of the pin, then the drain pin becomes high impedance (Hi-Z) upon overvoltage fault.
2. **DR driven below V_{IL}:**

   If the DR pin is driven below VIL level of the pin, then the drain pin (Dx) is pulled to the supply that was exceeded. For example, if the source voltage exceeds V_{FP}, then the drain output is pulled to V_{FP}. If the source voltage exceeds V_{FN}, then the drain output is pulled to V_{FN}. The pull-up impedance is approximately 40 kΩ, and as a result, the drain current is limited to roughly 1 mA during a shorted load (to GND) condition.

図 8-1 shows a detailed view of the how the DR pin controls the output state of the drain pin under a fault scenario.

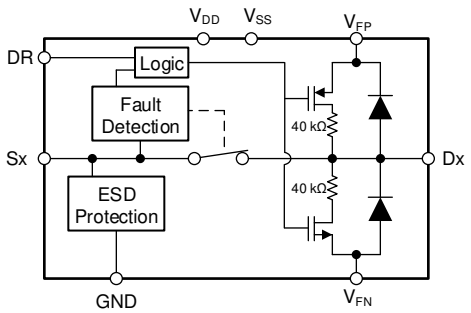


図 8-1. Detailed Functional Diagram

V_{FP} and V_{FN} are required fault supplies that set the level at which the overvoltage protection is engaged. V_{FP} can be supplied from 3 V to V_{DD}, while the V_{FN} can be supplied from V_{SS} to 0 V. If the fault supplies are not available in the system, then the V_{FP} pin must be connected to V_{DD}, while the V_{FN} pin must be connected to V_{SS}. In this case, the overvoltage protection then engages at the primary supply voltages V_{DD} and V_{SS}.

8.3.2.5 Latch-Up Immunity

Latch-up is a condition where a low impedance path is created between a supply pin and ground. This condition is caused by a trigger (current injection or overvoltage), but once activated, the low impedance path remains even after the trigger is no longer present. This low impedance path may cause system upset or catastrophic damage due to excessive current levels. The Latch-up condition typically requires a power cycle to eliminate the low impedance path.

An insulating oxide layer is placed on top of the silicon substrate to prevent any parasitic junctions from forming in the TMUX7462F devices. As a result, the devices are latch-up immune under all circumstances by device construction.

8.3.2.6 EMC Protection

The TMUX7462F is not intended for standalone electromagnetic compatibility (EMC) protection in industrial applications. There are three common high voltage transient specifications that govern industrial high voltage transient specifications: IEC61000-4-2 (ESD), IEC61000-4-4 (EFT), and IEC61000-4-5 (surge immunity). A transient voltage suppressor (TVS), along with some low-value series current limiting resistor, are required to prevent source input voltages from going above the rated ±60 V limits.

It is critical to ensure that the maximum working voltage is greater than the normal operating range of the input source pins protected and any known system common-mode overvoltage that may be present due to incorrect wiring, loss of power, or short circuit when selecting a TVS protection device. 図 8-2 shows an example of the proper design window when selecting a TVS device.

Region 1 denotes the normal operation region of TMUX7462F, where the input source voltages stay below the fault supplies V_{FP} and V_{FN}. Region 2 represents the range of possible persistent DC (or long duration AC overvoltage fault) presented on the source input pins. Region 3 represents the margin between any known DC overvoltage level and the absolute maximum rating of the TMUX7462F. The TVS breakdown voltage must be selected to be less than the absolute maximum rating of the TMUX7462F, but greater than any known possible persistent DC or long duration AC overvoltage fault to avoid triggering the TVS inadvertently. Region 4 represents the margin the system designers must impose when selecting the TVS protection device to prevent accidental triggering the ESD cells of the TMUX7462F.

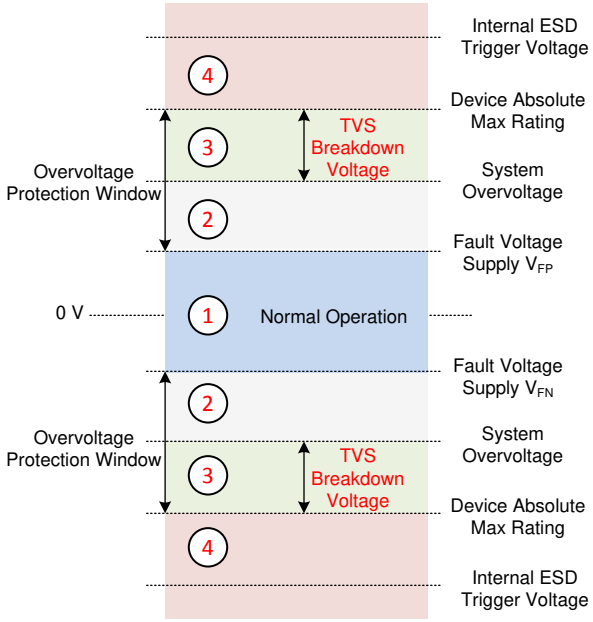


図 8-2. System Operation Regions and Proper Region of Selecting a TVS Protection Device

8.3.3 Overvoltage Fault Flags

The voltages on TMUX7462F's source input pins are continuously monitored, and the status of whether an overvoltage condition occurs is indicated by an active low general fault flag (FF). The voltage on the FF pin indicates if any of the source input pins are experiencing an overvoltage condition. If any source pin voltage exceeds the fault supply voltages by a V_T, the FF output is pulled-down to below V_{OL}. The FF pin is an open-drain output, and external pull-up resistors of 1 kΩ are recommended. The pull-up voltage can be in the range of 1.8 V to 5.5 V, depending on the controller voltage the device interfaces with.

8.3.4 Bidirectional Operation

The TMUX7462F conducts equally well from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). Each signal path has very similar characteristics in both directions; however, it is noted that the overvoltage protection is implemented only on the source (Sx) side. The voltage on the drain is only allowed to swing between V_{FP} and V_{FN} and no overvoltage protection is available on the drain side.

The primary supplies (V_{DD} and V_{SS}) define the on-resistance profile of the switch channel, whereas the fault voltage supplies (V_{FP} and V_{FN}) define the signal range that can be passed through from source to drain of the device. It is good practice to use voltages on V_{FP} and V_{FN} that are lower than V_{DD} and V_{SS} to take advantage of the flat on-resistance region of the device for better input-to-output linearity. The flattest on-resistance region extends from V_{SS} to roughly 3 V below V_{DD}. Once the signal is within 3 V of V_{DD} the on-resistance will exponentially increase and may impact desired signal transmission.

8.4 Device Functional Modes

The TMUX7462F offers two modes of operation (Normal mode and Fault mode) depending on whether any of the input pins experience an overvoltage condition.

8.4.1 Normal Mode

In Normal mode operation, signals of up to V_{FP} and V_{FN} can be passed through the switch from source (Sx) to drain (Dx) or from drain (Dx) to source (Sx). The following conditions must be satisfied for the switch to stay in the ON condition:

- The difference between the primary supplies ($V_{DD} – V_{SS}$) must be higher or equal to 8 V.
- V_{FP} must be between 3 V and V_{DD}, and V_{FN} must be between V_{SS} and 0 V.
- The input signals on the source (Sx) or the drain (Dx) must be between V_{FP}+ V_T and $V_{FN} – V_T$.

8.4.2 Fault Mode

The TMUX7462F enters into the Fault mode when any of the input signals on the source (Sx) pins exceed V_{FP} or V_{FN} by a threshold voltage V_T. The switch input experiencing the fault automatically turns off, and the source pin becomes high impedance with negligible amount of leakage current flowing through the switch under the overvoltage condition. For how the drain pin (Dx) behavior under the Fault mode can be programmed, refer to セクション 8.3.2.4. The general fault flag (FF) is asserted low in the Fault mode.

The overvoltage protection is provided only for the source (Sx) input pins. The drain (Dx) pin, if used as signal input, must stay in between V_{FP} and V_{FN} at all time since no overvoltage protection is implemented on the drain pin.

8.4.3 Truth Table

表 8-1 provides the truth tables for the TMUX7462F. Each switch is independently controlled by its own select pin.

表 8-1. TMUX7462F Truth Table

DR PIN STATE	Dx State During Fault Condition
0	Pulled up to V_{FP} or V_{FN}
1	Open (HI-Z)

9 Application and Implementation

注

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9.1 Application Information

The TMUX7462F is part of the fault protected switches and multiplexers family of devices. The ability to protect downstream components from overvoltage events up to ±60 V and latch-up immunity features makes these switches and multiplexers suitable for harsh environments.

9.2 Typical Application

The need to monitor remote sensors is common among factory automation control systems. For example, an analog input module or mixed module (AI, AO, DI, and DO) of a programmable logic controller (PLC) will interface to a field transmitter to monitor various process sensors at remote locations around the factory. A switch or multiplexer is often used to connect multiple inputs from the system and reduce the number of downstream channels.

There are a number of fault cases that may occur that can be damaging to many of the integrated circuits. Such fault conditions may include, but are not limited to, human error due to miswiring, component failure, wire shorts, electromagnetic interference (EMI), transient disturbances, and more.

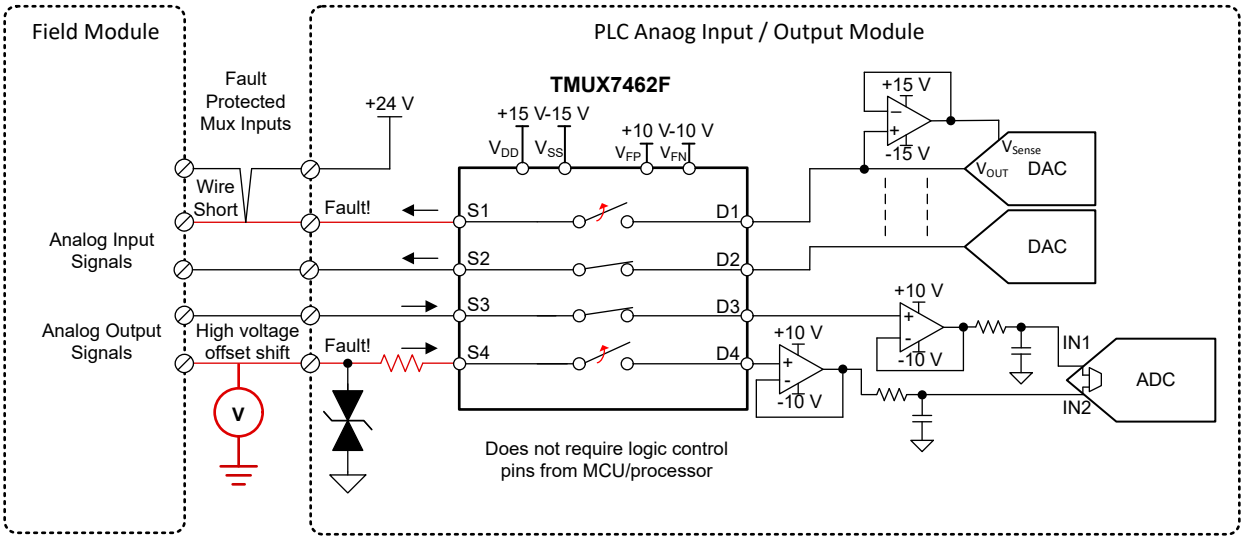


図 9-1. Typical Application

9.2.1 Design Requirements

表 9-1. Design Parameters

PARAMETER	VALUE
Positive supply (V_{DD}) mux	+15 V
Negative supply (V_{SS}) mux	-15 V
Power board supply voltage	24 V
Input or output signal range non-faulted	-10 V to 10 V
Overvoltage protection levels	-60 V to 60 V
Control logic thresholds	1.8 V compatible, up to 44 V
Temperature range	-40°C to +125°C

9.2.2 Detailed Design Procedure

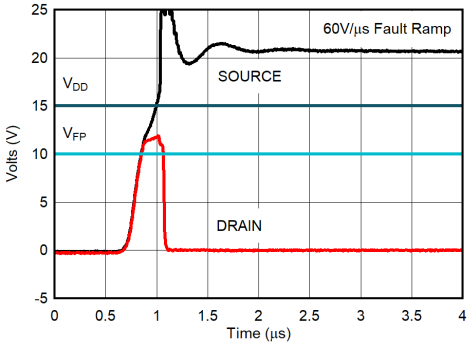
The TMUX7462F device's normal operation is to provide fault protection for the system while minimizing the control logic signals required to route across the PCB. The device works as a channel protector by allowing the signals to pass when in the valid voltage range, and opening the switch if there is a fault case. A fault protected switch can add extra robustness to the system against fault conditions while also reducing the number of components required to interface with the physical input channels.

The application shows two channels of the TMUX7462F connected as analog outputs and two channels connected as analog inputs to the PLC system. The analog input channels utilize the TMUX7462F to protect down stream operational amplifiers that are operating at a lower supply voltage than the multiplexer. The TMUX7462F only has overvoltage protection on the source pins, therefore these pins are connected to the external system connector on the analog output channels. If there is a miswiring or wire short issue on the connectors, the channel protector will open the switch channel to help prevent long term fault conditions from damaging the DAC.

If there is a fault condition, the drain pin of the channels can either be pulled up to the fault supply voltage (V_{FP} and V_{FN}) through a 40 kΩ resistor or be left floating depending on the state of the DR pin. This can be configured to match the system requirements on how to handle a fault condition.

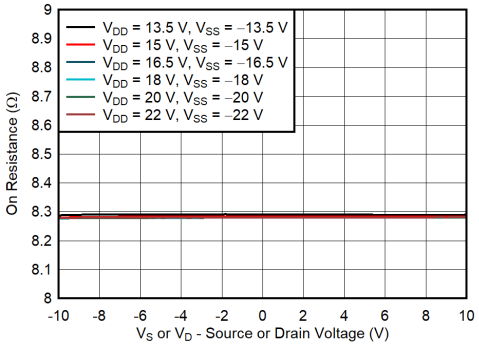
9.2.3 Application Curves

The example application utilizes adjustable fault threshold voltages of the TMUX7462F to allow for protection of downstream components operating on lower supply voltages. 図 9-2 shows an example of positive overvoltage fault response with a fast fault ramp rate of 60 V/us. 図 9-3 shows the extremely flat on-resistance across source voltage while operating within the fault threshold voltage levels for many supply voltage scenarios. These features make the TMUX7462F an excellent solution for data acquisition applications that may face various fault conditions but also require excellent linearity and low distortion.



V_{DD} = 15 V, V_{FP} = 10 V

図 9-2. Positive Overvoltage Response



V_{FP} = 10 V, V_{FN} = -10 V

図 9-3. R_{ON} Flatness in Non-Fault Region

9.3 Power Supply Recommendations

The TMUX7462F operates across a wide supply range of ±5 V to ±22 V (8 V to 44 V in single-supply mode). The device also performs well with asymmetrical supplies such as V_{DD} = 12 V and V_{SS}= –5 V. For improved supply noise immunity, use a supply decoupling capacitor ranging from 1 µF to 10 µF at the V_{DD} and V_{SS} pins to ground. Always ensure the ground (GND) connection is established before supplies are ramped.

The fault supplies (V_{FP} and V_{FN}) provide the current required to operate the fault protection, and thus, must be low impedance supplies. They can be derived from the primary supplies by using a resistor divider and buffer or be an independent supply rail. The fault supplies must not exceed the primary supplies as it might cause unexpected behavior of the switch. Use a supply decoupling capacitor ranging from 1 µF to 10 µF at the V_{FP} and V_{FN} pins to ground for improved supply noise immunity.

The positive supply, V_{DD}, must be ramped before the positive fault rail, V_{FP}, for proper power sequencing of the TMUX7462F. Similarly, the negative supply, V_{SS}, must be ramped before the negative fault voltage rail, V_{FN}.

9.4 Layout

9.4.1 Layout Guidelines

The following images shows an example of a PCB layout with the TMUX7462F. Some key considerations are as follows:

- Decouple the V_{DD} and V_{SS} pins with a 1-µF capacitor, placed as close to the pin as possible. Make sure that the capacitor voltage rating is sufficient for the supplies.
- Multiple decoupling capacitors can be used if their is a lot of noise in the system. For example, a 0.1-µF and 1-µF can be placed on the supply pins. If multiple capacitors are used, then it is recommended to place the lowest value capacitor closest to the supply pin.
- Keep the input lines as short as possible.
- Use a solid ground plane to help distribute heat and reduce electromagnetic interference (EMI) noise pickup.
- Do not run sensitive analog traces in parallel with digital traces. Avoid crossing digital and analog traces if possible, and only make perpendicular crossings when necessary.

9.4.2 Layout Example

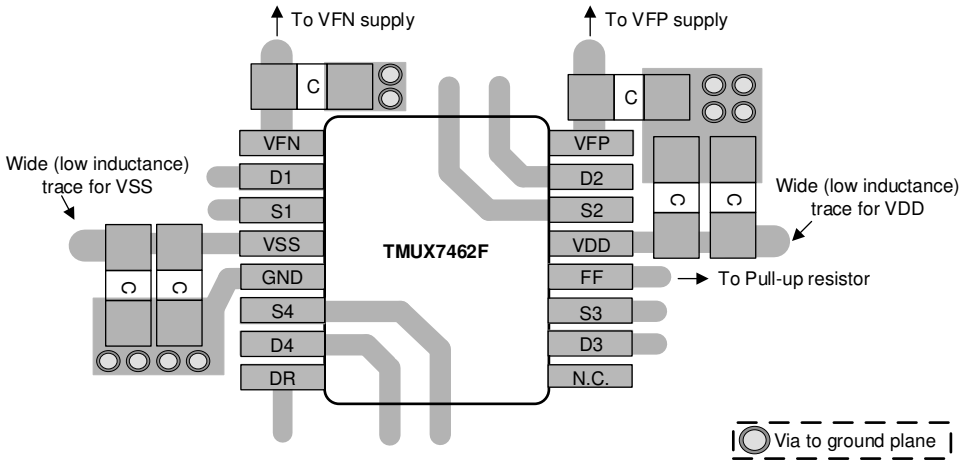


図 9-4. TSSOP Layout Example

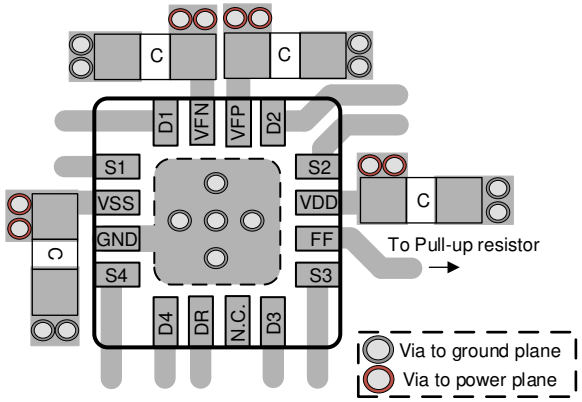


図 9-5. WQFN Layout Example

10 Device and Documentation Support

10.1 Documentation Support

10.1.1 Related Documentation

- Texas Instruments, *Multiplexers and Signal Switches Glossary*
- Texas Instruments, *Protection Against Overvoltage Events, Miswiring, and Common Mode Voltages*
- Texas Instruments, *Improving Analog Input Modules Reliability Using Fault Protected Multiplexers*
- Texas Instruments, *Using Latch-Up Immune Multiplexers to Help Improve System Reliability*

10.2 ドキュメントの更新通知を受け取る方法

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10.3 サポート・リソース

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10.5 静電気放電に関する注意事項

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10.6 用語集

テキサス・インスツルメンツ用語集　　この用語集には、用語や略語の一覧および定義が記載されています。

11 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TMUX7462FPWR	ACTIVE	TSSOP	PW	16	3000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	TM7462F	Samples
TMUX7462FRRPR	ACTIVE	WQFN	RRP	16	3000	RoHS & Green	NIPDAU	Level-2-260C-1 YEAR	-40 to 125	TMUX 7462F	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

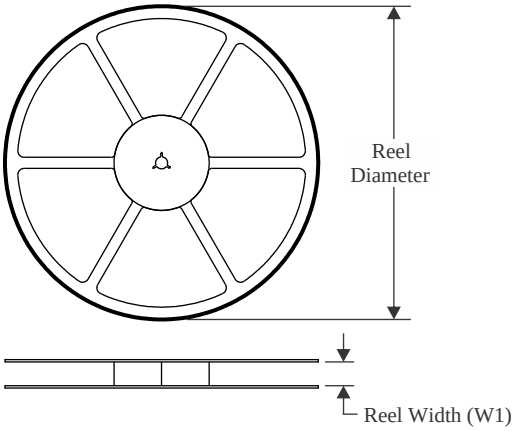
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

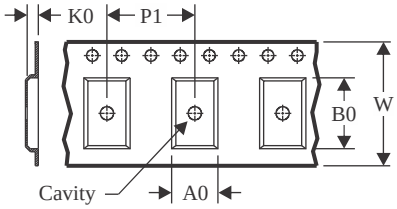
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

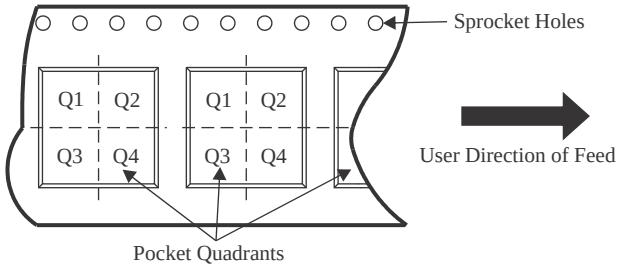


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

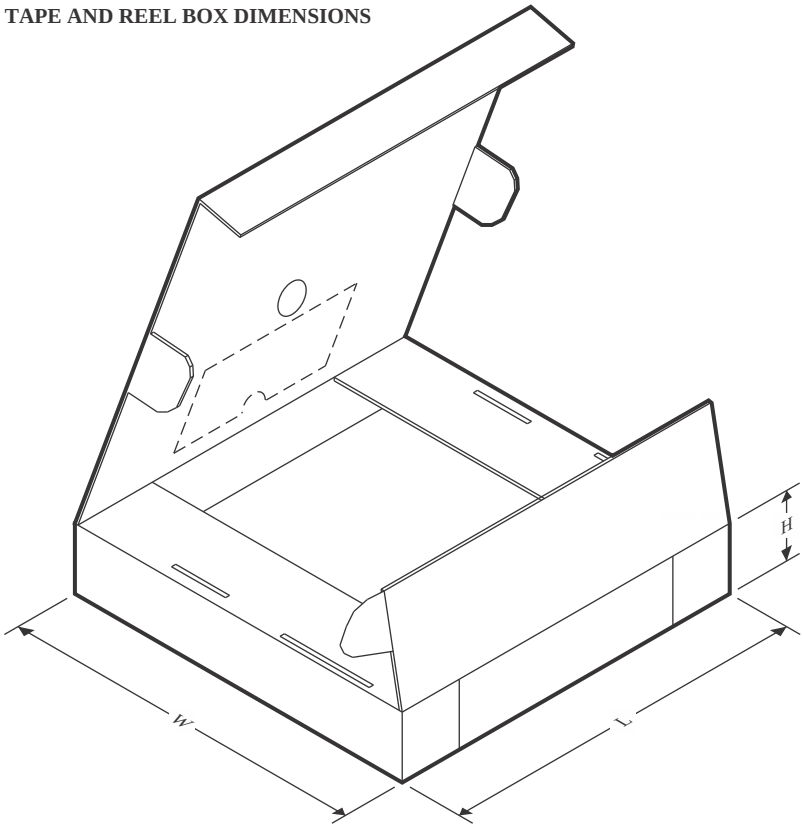
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TMUX7462FRRPR	WQFN	RRP	16	3000	330.0	12.4	4.25	4.25	1.15	8.0	12.0	Q2

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

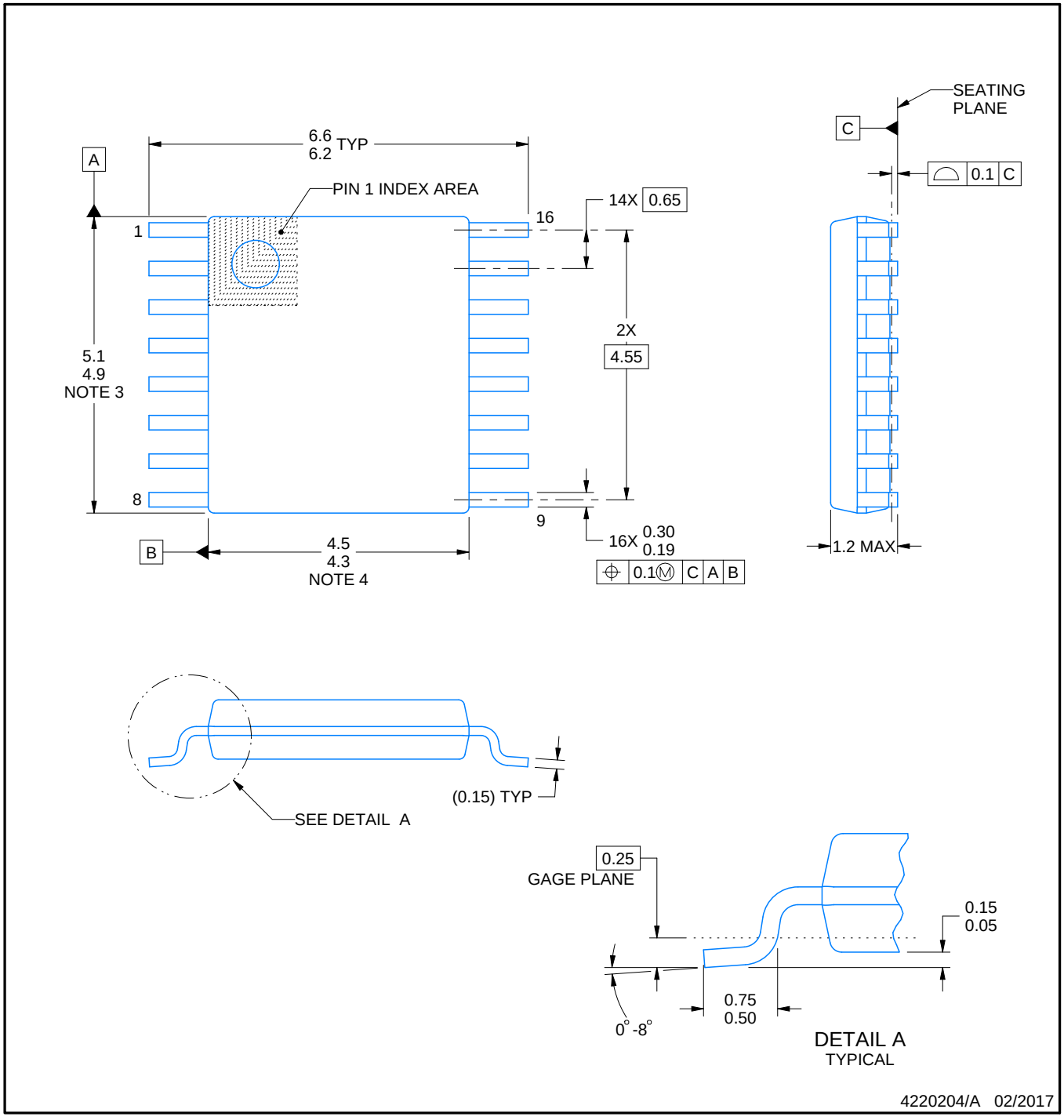
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TMUX7462FRRPR	WQFN	RRP	16	3000	367.0	367.0	35.0

PACKAGE OUTLINE

PW0016A

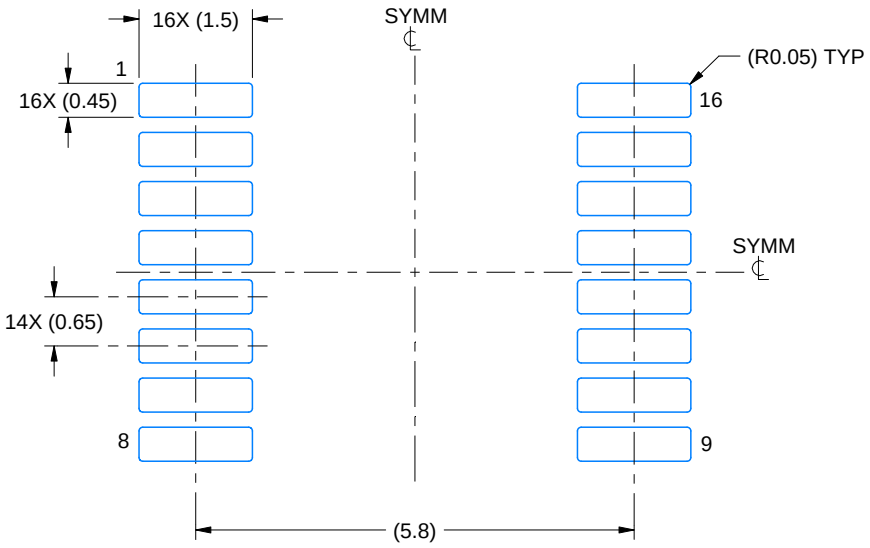
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE

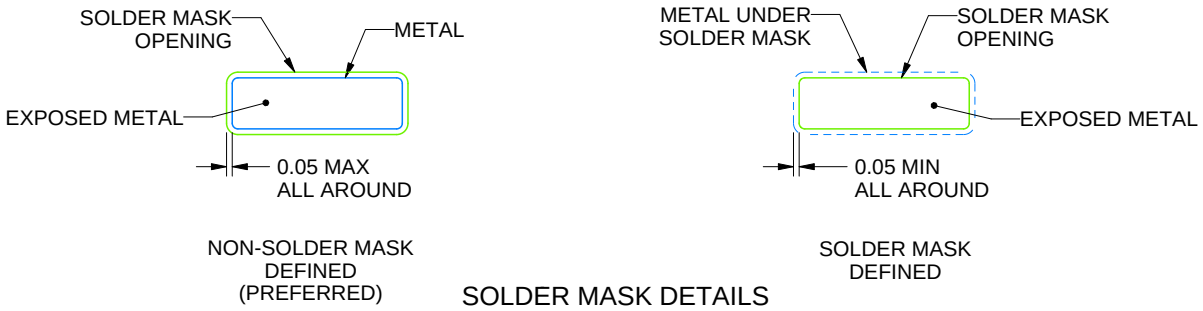


NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

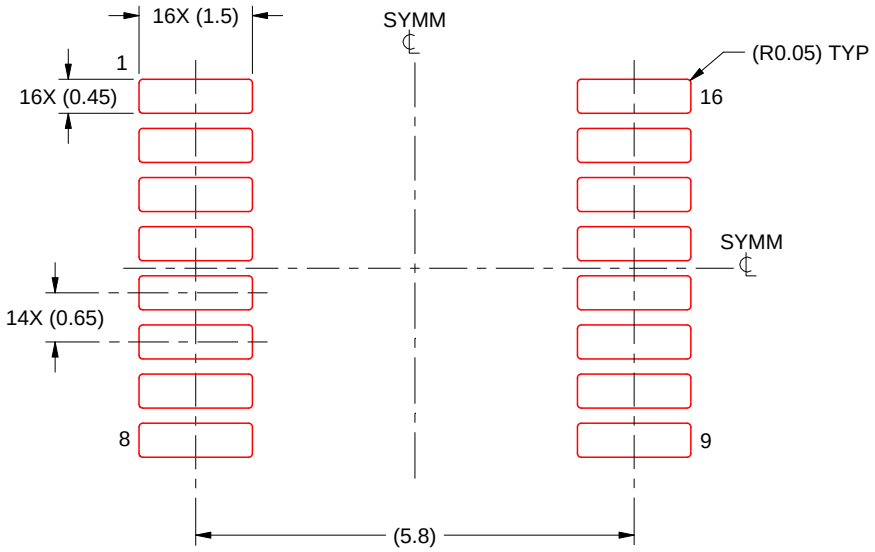


SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

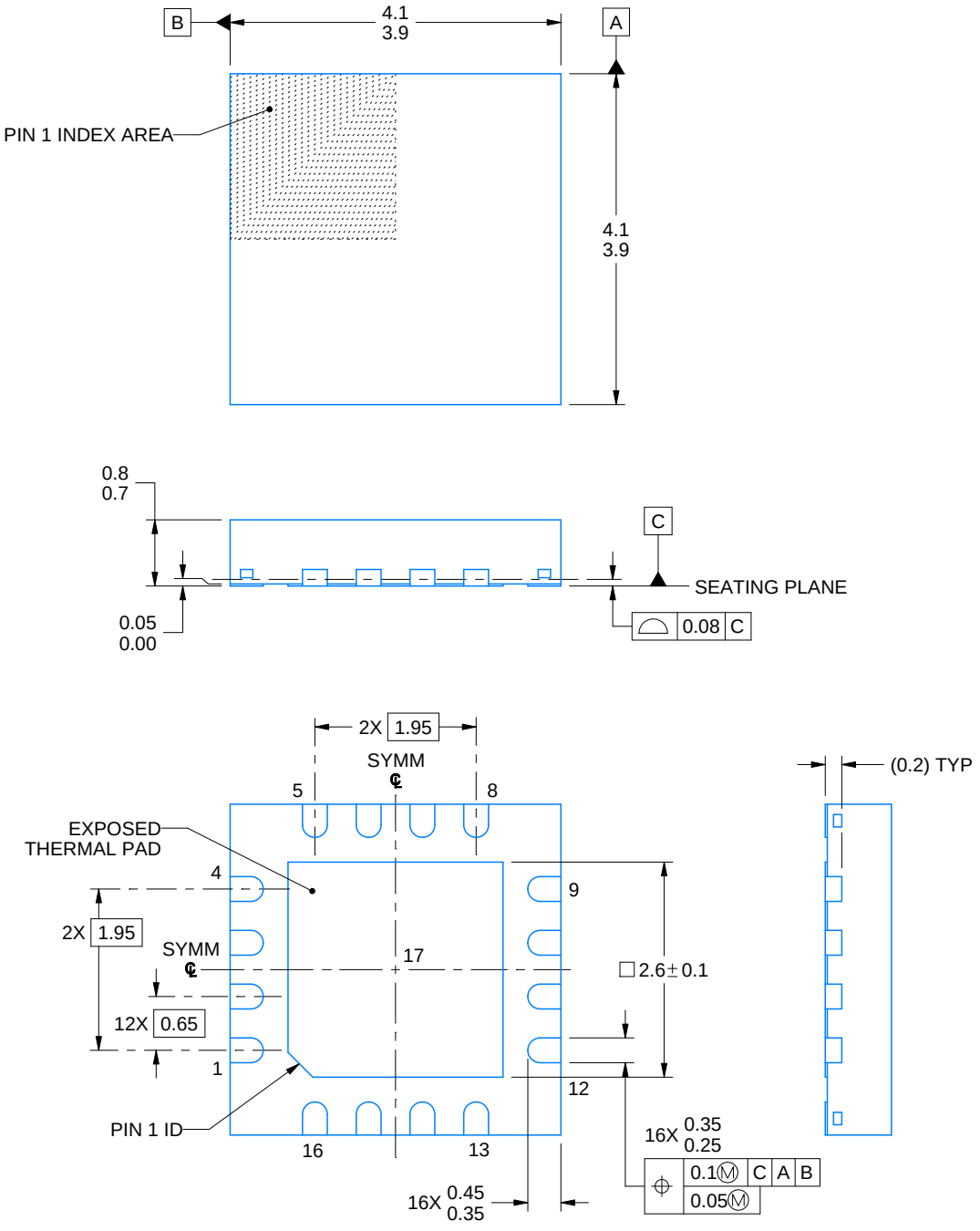
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PACKAGE OUTLINE

RRP0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



NOTES:

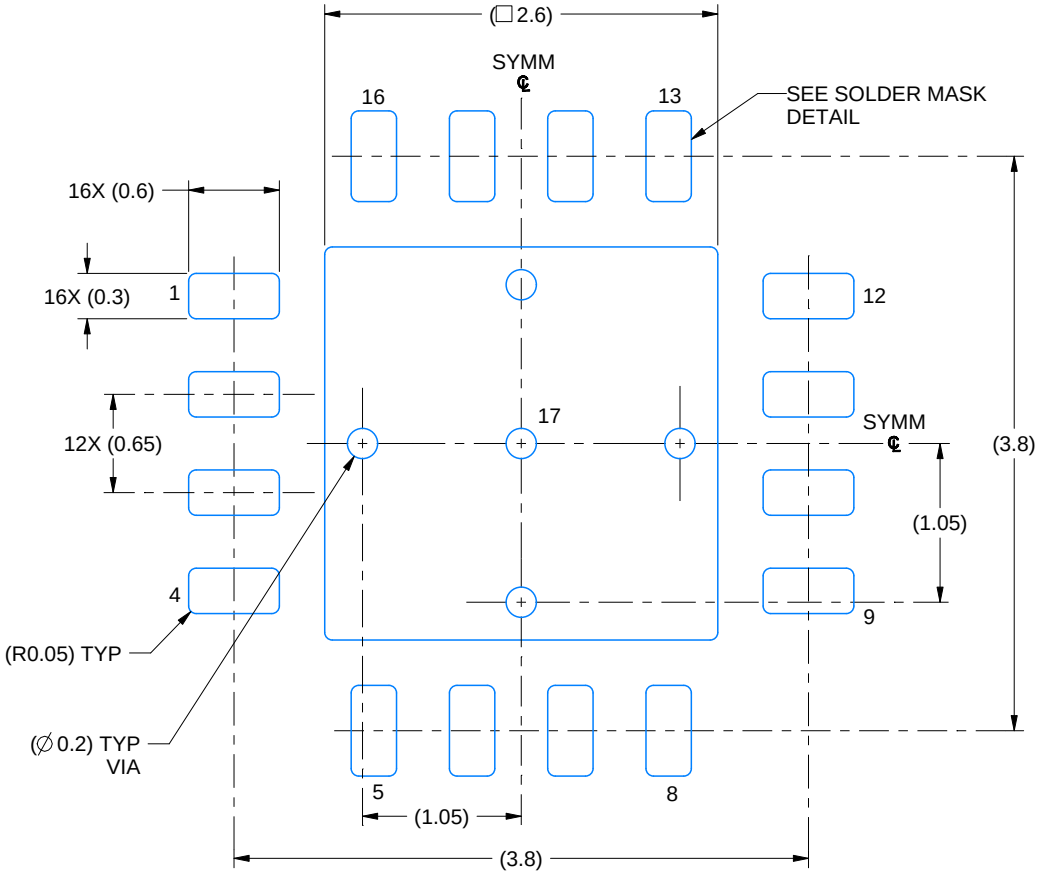
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.

EXAMPLE BOARD LAYOUT

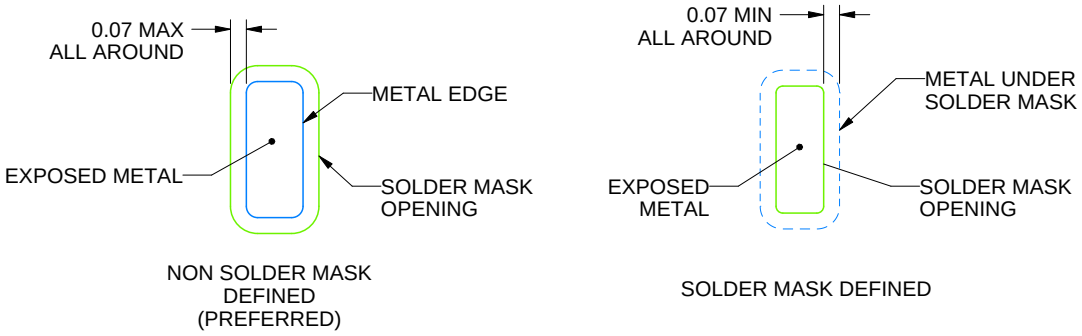
RRP0016A

WQFN - 0.8 mm max height

PLASTIC QUAD FLATPACK - NO LEAD



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

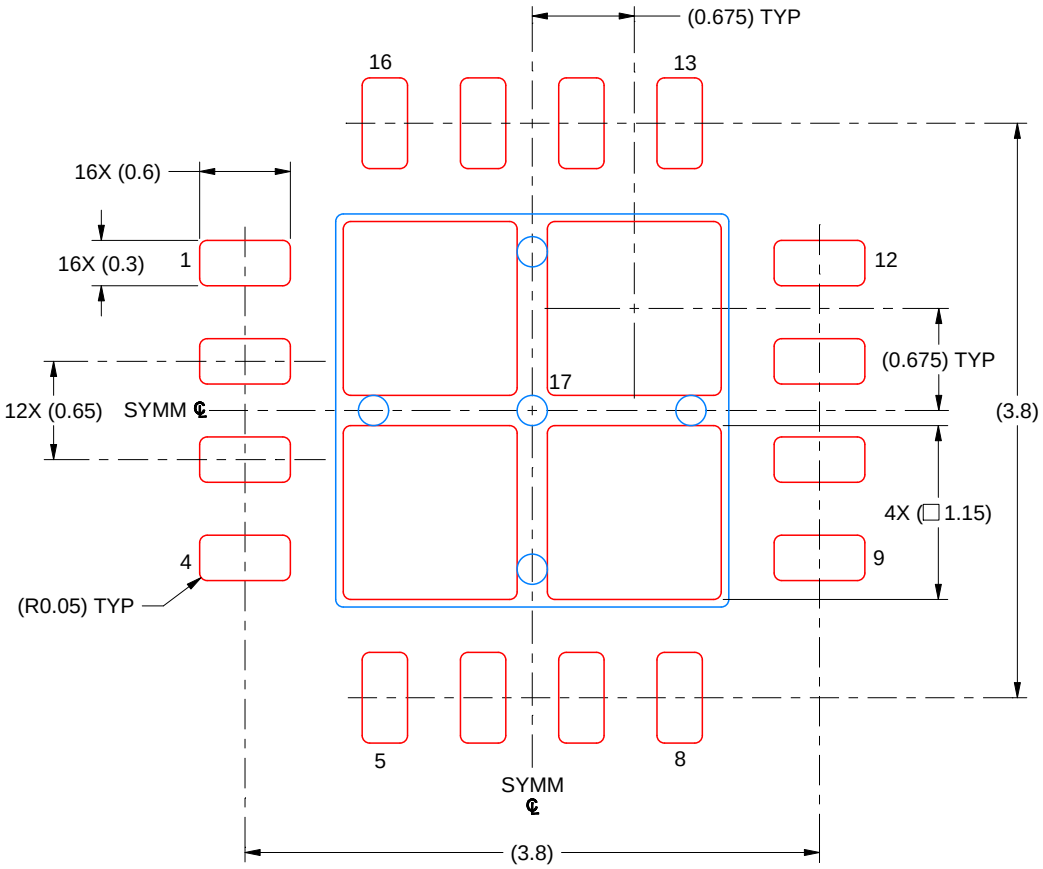


SOLDER MASK DETAILS

4224816/A 02/2019

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).
5. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.



SOLDER PASTE EXAMPLE
BASED ON 0.125 MM THICK STENCIL
SCALE: 20X

EXPOSED PAD 17
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE

4224816/A 02/2019

NOTES: (continued)

6. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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